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Title of the thesis: Analytical Modeling and Simulation of Some Ultra-thin Non-Conventional MOSFET Structures

Abstract

The current era of unimpeded progress that is being witnessed by the modern semiconductor device manufacturing industries is marked by incessant modernization of devices to offer excellent performance. Significantly automation-inclined contemporary lifestyle of present day human civilization is one of the principal reasons that drives the necessity to continue technical renovation in the associated field of advanced electronic devices. The interminable demands of current day consumer markets have prominently pointed out the inevitable and desirable attributes such as miniaturization/ portability, cost-efficacy, improved speed of operation and lower power consumption that a modern day electronic device is anticipated to possess. Scientific evolution, over the decades, has exhibited device downscaling, which is employed to reduce device dimensions, currently in the nanometer scale in accordance with Moore's law, as an inexorable tool to achieve the above stated attractive device features. Scaling device dimensions permits miniaturization, enhancing integration density on a single chip to boost functionality without negatively impacting the fabrication cost. However, every technology is bound by some limitations and device scaling, alone, has proved to be not sufficient when device dimensions are radically scaled down to nanometer limits. Such aggressive scaling is accompanied by a cluster of detrimental effects that tend to degrade the device performance significantly. Such effects, collectively recognized as the Short Channel Effects (SCEs), are of different forms, such as Drain-induced barrier lowering (DIBL), Hot carrier effects (HCE), threshold voltage roll-off (TVRO), subthreshold slope degradations, increased off-state leakages etc. that work cumulatively to increase power consumption of the device, deteriorate its speed of operation thereby making the device inefficient for low power applications. Owing to its weaker resistance to SCEs, the bulk MOSFETs could no longer provide upgraded performance even after device scaling and hence the conventional MOSFET geometry needs to be modified along with incorporation of some pioneering technologies like incorporation of multi-gate, gate work function engineering (GWFE), channel, dielectric engineering schemes that target some SCEs for amendments and rectifications.

This thesis embodies the comprehensive analysis of some advanced, non-conventional, ultra-thin MOSFET structures where their electrical characteristics like potential, threshold voltage, short channel response and in some cases, drain current have been investigated and highlighted in detail through proper analytical modeling and the results of these mathematical modeling have been verified using proper simulation software outputs.

Pritha Banerjee 05/07/2022

Signature of the Candidate with date

Jayoti Das 05/07/2022

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