ANALYTICAL MODELING AND SIMULATION OF SOME ULTRA-THIN NON-CONVENTIONAL MOSFET STRUCTURES

Thesis submitted for the degree of
Doctor of Philosophy (Science)
of
Jadavpur University

By
PRITHA BANERJEE

Department of Physics
Faculty Council of Science
Jadavpur University
Kolkata, India
2022

CERTIFICATE FROM THE SUPERVISOR

This is to certify that the thesis entitled "***Analytical Modeling and Simulation of Some Ultra-thin Non-Conventional MOSFET Structures***" Submitted by ***Smt. Pritha Banerjee*** who got her name registered on ***14.03.2018*** for the award of Ph. D. (Science) Degree of Jadavpur University, is absolutely based upon her own work under the supervision of ***Prof. (Dr.) Jayoti Das*** and that neither this thesis nor any part of it has been submitted for either any degree / diploma or any other academic award anywhere before.

Jayoti Das 05/07/2022

(Signature of the Supervisor, date with official seal)

Dr. Jayoti Das
Professor
Department of Physics
Jadavpur University
Kolkata - 700 032

Contents

List of Publications

Peer-reviewed International SCI/SCIE Journals: 18

1) **Pritha Banerjee**, Jayoti Das, "Analytical Exploration and Simulation of Dual-Material Gate Macaroni Channel MOSFET biosensor using dielectric-modulation technique", **Micro and Nanostructures**, **Elsevier**, Volume 165, 2022, 207196, ISSN 2773-0123, https://doi.org/10.1016/j.micrna.2022.207196.

2) **Pritha Banerjee** and Jayoti Das, "Threshold Voltage Modeling of Gaussian-doped Dual work function Material Cylindrical Gate-All-Around (CGAA) MOSFET considering the effect of temperature and Fixed Interface Trapped Charges", **Microelectronics Journal, Elsevier**, Volume 120, February 2022, 105354, DOI: 10.1016/j.mejo.2021.105354

3) **Pritha Banerjee** and Jayoti Das, "Gate Work Function-Engineered Graded-Channel Macaroni MOSFET: Exploration of Temperature and Localized Trapped Charge-Induced Effects with GIDL Analysis", **Journal of Electronic Materials, Springer**, Vol.51, pp: 1512-1523, December 2021.

4) **Pritha Banerjee** and Jayoti Das, "Gate Work Function Engineered Trigate MOSFET with a Dual-Material Bottom Gate for Biosensing Applications: A Dielectric-Modulation based Approach", **Silicon, Springer**, 14, 419–428, 2022, https://doi.org/10.1007/s12633-020-00823-5

5) Priyanka Saha, **Pritha Banerjee**, Dinesh Kumar Dash & Subir Kumar Sarkar , "Interface Trap Charge Induced Threshold Voltage Modeling of WFE High-K SOI MOSFET", **Silicon, Springer**, 12, 2893–2900, 2020, DOI: 10.1007/s12633-020-00386-5

6) **Pritha Banerjee** and Subir Kumar Sarkar, " Performance Analysis and Investigation of Subthreshold Short-Channel Behavior of a Dual-Material Elliptical Gate-All-Around MOSFET", **Journal of Electronic Materials, Springer**, 48, pp. 3270–3275 March 2019, https://doi.org/10.1007/s11664-019-07082-0

7) **Pritha Banerjee** and Subir Kumar Sarkar, "Analysis of short channel characteristics in graded channel dual-material elliptical gate-all-around (GC DM EGAA) MOSFET", DOI: 10.1088/1361-6641/aafc86, **Semiconductor Science and Technology, IOP**, 34 035010, January 2019

8) **Pritha Banerjee** and Subir Kumar Sarkar, “Modeling and Analysis of a Front High-k gate stack Dual-Material Tri-gate Schottky Barrier Silicon-on-Insulator MOSFET with a dual-material bottom gate”, DOI: 10.1007/s12633-018-9940-y, 11, pp. 513–519, **Silicon, Springer**, July 2018

9) Priyanka Saha, **Pritha Banerjee** and Subir Kumar Sarkar, “ 2D modeling based comprehensive analysis of short channel effects in DMG strained VSTB FET”, **Superlattices and Microstructures, Elsevier**, Volume 118, Pages 16-28, June 2018, DOI: 10.1016/j.spmi.2018.03.070

10) Priyanka Saha, **Pritha Banerjee**, Dinesh Kumar Dash and Subir Kumar Sarkar, "Exploring the short channel characteristics of Asymmetric Junctionless Double Gate Silicon On Nothing MOSFET", **Journal of Materials Engineering and Performance, Springer**, , Volume 27, Issue 6, pp 2708–2712, June 2018, DOI: 10.1007/s11665-018-3281-2

11) **Pritha Banerjee**, Priyanka Saha and Subir Kumar Sarkar, "Analytical Modelling and Performance Analysis of Gate Engineered Tri-gate SON MOSFET", accepted in **IET Circuits, Devices & Systems, IET**, Volume 12, Issue 5, p. 557 – 562, March 2018, DOI: 10.1049/iet-cds.2017.0473

12) **Pritha Banerjee** and Subir Kumar Sarkar, “Comprehensive analysis of subthreshold short channel behavior of a Dual-material gate strained Trapezoidal FinFET”, **Superlattices and Microstructures, Elsevier**, Volume 117, Pages 527-537, May 2018, DOI: 10.1016/j.spmi.2018.02.034

13) **Pritha Banerjee**, Tripty Kumari and Subir Kumar Sarkar, "2-D modeling and analysis of short-channel behavior of a front high-K gate stack triple-material gate SB SON MOSFET", **Applied Physics A, Springer**, 124, 153 (2018). https://doi.org/10.1007/s00339-018-1567-8

14) Aman Mahajan ,Dinesh Kumar Dash, **Pritha Banerjee** and Subir Kumar Sarkar, “Analytical Modeling of Triple Metal Hetero Dielectric DG SON TFET”, **Journal of Materials Engineering and Performance, Springer**, vol:27, Issue 3, pp. 2693–2700, January 2018, DOI: 10.1007/s11665-018-3225-x

15) **Pritha Banerjee**, Priyanka Saha and Subir Kumar Sarkar, "Two dimensional analytical modeling of a high-K gate stack triple-material double gate strained silicon-on-nothing MOSFET with a vertical Gaussian doping", **Journal of Computational**

Electronics, Springer, Volume 17, Issue 1, pp 172–180, November 2017, DOI: 10.1007/s10825-017-1089-1

16) **Pritha Banerjee**, Anup Sarkar and Subir Kumar Sarkar, "Exploring the short channel characteristics and performance analysis of DMDG SON MOSFET", **Microelectronics Journal, Elsevier**, Volume 67, Pages 50-56, September 2017, DOI: 10.1016/j.mejo.2017.07.005

17) **Pritha Banerjee** and Subir Kumar Sarkar, "3-D analytical modeling of high-k gate stack dual-material tri-gate strained silicon-on-nothing MOSFET with dual-material bottom gate for suppressing short channel effects", **Journal of Computational Electronics, Springer**, Vol.16.No.3,pp-631-639,May 2017, DOI: 10.1007/s10825-017-1002-y

18) **Pritha Banerjee** and Subir Kumar Sarkar, "3D Analytical Modeling of Dual Material Triple Gate Silicon-on Nothing MOSFET", **IEEE Transactions on Electron Devices, IEEE**, Vol.64,Issue 2,pp-368-375,February 2017, DOI: 10.1109/TED.2016.2643688

International Conference Publications: 11

1) **Pritha Banerjee**, Priyanka Saha, Dinesh Kumar Dash and Subir Kumar Sarkar, "Surface potential based Analytical Modeling of Graded Channel Strained High-k Gate stack Dual-Material Double Gate MOSFET", ", in 3rd international conference "**2019 Devices for Integrated Circuit (DevIC)**", Kalyani Government Engineering College from March 23-24, 2019, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and technically co-sponsored by IEEE EDS Kolkata Chapter.

2) Priyanka Saha, **Pritha Banerjee**, Dinesh Kumar Dash and Subir Kumar Sarkar, "Impact of trapped interface charges on short channel characteristics of WFE high-K SOI MOSFET", in 3rd international conference "**2019 Devices for Integrated Circuit (DevIC)**, Kalyani Government Engineering College from March 23-24, 2019, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and technically co-sponsored by IEEE EDS Kolkata Chapter.

3) **Pritha Banerjee**, Priyanka Saha, Dinesh Kumar Dash, Ankush Ghosh and Subir Kumar Sarkar, "Analytical Modeling and Performance Analysis of Graded Channel Strained Dual-Material Double Gate MOSFET", **4th International Conference on**

Computing Communication and Automation 2018 (ICCCA 2018) organized by IEEE UP Section, 14th-15th December, 2018, Galgotias University, Greater Noida, NCR-New Delhi, India.

4) Priyanka Saha , Pritha Banerjee, Dinesh Kumar Dash and Subir Kumar Sarkar, "Modeling short channel behavior of proposed Work Function Engineered High-k gate stack DG MOSFET with vertical Gaussian doping", **IEEE Electron Device Kolkata Conference [EDKCON 2018]**, organized by IEEE EDS Kolkata Chapter at The Pride Hotel, Kolkata, West Bengal on 24th – 25th November, 2018.

5) Pritha Banerjee, Priyanka Saha, Dinesh Kumar Dash and Subir Kumar Sarkar, "A Study of Short Channel Behavior of Dual Material strained silicon Trigate (DM Strained-Si TG) SOI MOSFET", **IEEE International Conference On Computing, Power And Communication Technologies 2018 (GUCON 2018)**, organized by IEEE UP section at Radisson Blu Hotel, Greater Noida, Uttar Pradesh on 28th -29th September, 2018

6) Dinesh Dash, Priyanka Saha, Pritha Banerjee and Subir Kumar Sarkar, "Analytical Modeling of Graded Metal Graded Dielectric Silicon-On-Nothing TFET -A Comparative Study", Best Paper Award, **IEEE International Conference On Computing, Power And Communication Technologies 2018 (GUCON 2018)**, organized by IEEE UP section at Radisson Blu Hotel, Greater Noida, Uttar Pradesh on 28th -29th September, 2018 [Best Paper Award]

7) Priyanka Saha, Pritha Banerjee and Subir Kumar Sarkar," 3D Modeling based performance analysis of Gate Engineered Trigate SON TFET with SiO2/HfO2 stacked gate oxide" in **IEEE Conference CONECCT**, organized by IEEE Bangalore Section at Hyatt Regency on16-17th , March 2018

8) Pritha Banerjee , Priyanka Saha and Subir Kumar Sarkar,"3-D Analytical Modeling and comprehensive analysis of SCEs of a high-K gate stack dual-material tri-gate Silicon-On-Insulator MOSFET with dual-material bottom gate", **IEEE Calcutta Conference, CALCON 2017**,Lalit Great Eastern, Dalhousie Square, Kolkata-69, 2-3rd,December 2017

9) Pritha Banerjee, Anup Sarkar, Dinesh Kumar Dash and Subir Kumar Sarkar, "Performance Analysis of High-K Dual Material Tri-gate SON MOSFET", **International Conference on Communication Devices and Networking (ICCDN) 2017**, Sikkim Manipal Institute of Technology, Majhitar, Sikkim, 3-4th June, 2017 [Published as a book chapter in Advances In Communication, Devices And Networking, Lecture Notes in Electrical Engineering – Springer, DOI: https://doi.org/10.1007/978-981-10-7901-6_9, Online ISBN: 978-981- 10-7901-6]

10) Pritha Banerjee, Aman Mahajan and Subir Kumar Sarkar,"3-D Analytical Modeling of Gate Engineered Tri-gate SON MOSFET", **IEEE International Conference on Devices for Integrated Circuits (DEVIC-17)**,Kalyani Govt. Engg. College, 23-24 March, 2017

11) Pritha Banerjee, Aman Mahajan and Subir Kumar Sarkar, "2-D Analytical Modeling of Dual-Material Double Gate Silicon-On-Nothing MOSFET", in **1st International Conference on VLSI Device, Circuit and System (VLSI DCS 2016)**, 19th-20th /October, 2016, Meghnad Saha Institute of Technology, Kolkata, India [Extended paper published in Advances in Industrial Engineering and Management, ASP, Vol. 6, No.1,11-16, 2017]

List of Paper Presentations in National/International Conferences: 03

1) 1st International Conference on VLSI Device, Circuit and System **(VLSI DCS 2016)**, 19th-20th October, 2016, Meghnad Saha Institute of Technology, Kolkata, India

2) 4th International Conference on Computing Communication and Automation 2018 **(ICCCA 2018)** organized by IEEE UP Section, 14th-15th December, 2018, Galgotias University, Greater Noida, NCR-New Delhi, India.

3) 3rd International Conference "2019 Devices for Integrated Circuit (**DevIC**)", Kalyani Government Engineering College from March 23-24, 2019, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and technically co-sponsored by IEEE EDS Kolkata Chapter

Dedicated

To

My Parents

Shri Siba Prasad Banerjee & Smt. Madhumita Banerjee

For their profound affection, continuous mental support & true motivation

Acknowledgement

I would like to take this opportunity to express my impassioned gratitude and infinite indebtedness to my Guide, Supervisor and Mentor Dr. Jayoti Das, Professor, Department of Physics, Jadavpur University for her esteemed guidance, constant motivation and endless support throughout the entire journey of my PhD Research work. My Respected Mentor is a quintessential source of inspiration and an exemplary personification of the word Mentor, enriching the Philosophy of my life.

I have been extremely lucky to have been showered with the priceless love and blessings of my Respected, Motherly Figure, Dr. Snehamanju Basu, Professor and Registrar, Jadavpur University. Our Honorable Registrar Madam has continuously encouraged and motivated me during my blues that made me realize this dream of mine into reality. She has been a True Idol of Women Empowerment to me. I also express my heartfelt gratefulness to Prof. Chiranjib Bhattacharjee, Honorable Pro-Vice Chancellor, Jadavpur University, for his precious blessings to continue my research work with unimpeded progress and significant development.

I would like to express my great regards to all the Respected Professors of my Research Advisory Committee, for their patience, valuable time and priceless scholarly inputs that helped me in maintaining an unhindered development of my research work. I express my gratefulness to all the members and staff of the Department of Physics, Jadavpur University for providing me with all the necessary infrastructural facilities that helped me to smoothly carry out my research work.

I would like to express my special thanks to the Department of Science & Technology, Ministry of Science & Technology, Government of India for selecting me for the DST Women Scientist (A) Fellowship, for offering me the opportunity to work as the Principal Investigator of a three year Project related to my PhD work and providing me with financial research grants and fellowship without any lag.

I would like to extend my sincere thanks to all of my lab mates, Diparati Basu, Tanusree Sarkar, Mintu Mallick and Kaustav Sen for providing encouragement throughout this journey of my research work. I wish them success and happiness in all their future endeavors.

I would forever remain indebted to my parents, Smt. Madhumita Banerjee and Shri Siba Prasad Banerjee who stood before me firmly and never let anything challenging to come in the path between me and my PhD. Completion of this thesis is largely a result of their unfathomable love, self-sacrifices and immense co-operation. I am out of my words to express my deepest love and respect for them.

I would like to thank my maternal uncle, Shri Partha Chakraborty for providing me with constant moral support and encouragement to continue with my research work in an unhindered manner.

The Journey of PhD is an amalgamation of several ups and downs that governs the inevitable growth of a human mind adding the qualities and flavors of perseverance, hard work, honest effort, sincerity, knowledge, wisdom and humility. I would like to thank The Omnipotent, Adidev Mahadev & Adidevi Durga, for choosing and blessing me to experience this unparalleled lesson of mind metamorphosis and guiding me throughout the journey that ultimately granted me with wisdom and strength to complete this thesis.

Pritha Banerjee

Abstract

Technology Modernization in the current decade is presently witnessing an unhindered progress sparked by continuous innovation in the field of electronic industrialization. Modern day lifestyle has become more automation-inclined which drives the necessity for technological rejuvenation in terms of advanced electronic devices. Considering the recent demands of the present day consumer market, faster, miniaturized, cost-effectiveness, reduced power consumption etc. are some of the key features, a modern day electronic device is expected to possess. These features can be obtained through device-downscaling, which is employed to reduce device dimensions currently down to sub-nanometer limits in accordance with the Moore's Law. Device downscaling is implemented with a target to accomplish miniaturization, higher integration density on a single chip for augmented functionality coupled with reduced or unaffected fabrication cost. However, every technology has its limitations. Device-downscaling is also no exception. Aggressive downscaling in nanometer regime also possesses negative consequential effects leading to elevated complexities in device fabrication at such low dimensions paired up with the inexorable short channel effects (SCEs) that tend to degrade the device performance severely. The conventional CMOS technology, owing to its restricted immunity to SCEs, needs to be partially or fully-modified to achieve fabrication-feasible, advanced devices with boosted resistance to SCEs. Speaking of this technological evolution, the first technology, to be mentioned in this context, is of Silicon-on-Insulator (SOI). The technology, as its name suggests, features the incorporation of SiO_2 insulator sandwiched between the Si channel and Si substrate in the basic MOSFET geometry. This miniscule modification in the basic MOSFET structure works wonders resulting in diminished parasitic capacitances, improved speed of operation, radiation hardness, ameliorated SCE resisting capability, etc. Retaining all the advantages of SOI and additionally providing highest dielectric isolation between channel and substrate coupled with subsequent device performance enhancement, Silicon-on-Nothing (SON) technology became more popular than SOI. Replacing the SiO_2 layer with air between the channel and the substrate results in SON geometry.

Researchers have always targeted to achieve boosted gate control over the channel since this catalyzes the process of alleviating the SCEs in many ways. The technology of Gate Work Function Engineering (GWFE), which is featured with the employment of two or more materials placed adjacently as a single gate electrode, proved to be a remarkable innovation contributing to escalated gate control, reduced SCEs like Drain-induced barrier lowering (DIBL), Hot carrier effect (HCE) etc.

The gradual evolution of MOSFET devices from basic single gate MOS devices to Multi-Gate MOS devices such as Dual-Gate, Tri-Gate, Gate-All-Around MOSFET has played a pivotal role in significantly contributing to enriched device performance. The multiple gate technology allows greater coverage of the surface area of the conducting channel thereby enabling developed SCE attenuation, assuring superior threshold voltage characteristics, boosting the current driving capability etc.

In addition to this, several strategies such as channel and dielectric engineering can significantly enhance the device performance. Moreover, schemes like dielectric engineering can be suitably implemented to explore biosensing properties of advanced MOSFET biosensors. Apart from all this, consistency in reliability of device performance needs to be parallely considered in order to assure successful implementation of the device in advanced, future generation low power VLSI circuits in a wide temperature varying environment. Hence, the thermal device behavior needs to be considered equally at varying ambient temperatures. Furthermore, some interface trapped charges cause detrimental effects on device performance and this need to be mathematically modeled and simulated to consider the effect of these trap charges on the electrostatics of such advanced MOSFETs.

List of Figures

Chapter 1

Chapter 1: Introduction, Literature Survey & Organization of Thesis

---

1.1 Introduction

Technological Renaissance currently witnessed by the contemporary semiconductor industry, to keep pace with the modern day consumer demands, is marked by the innovation of advanced MOSFET devices. Modern day lifestyle is being encompassed and linked to technological advancement that assures countless benefits ranging from comfort, offering a laborsaving regime with safety, security to accessing medical facilitations, entertainment, high speed wireless communications and many more. However, this limitless reliance of human civilization on process-automation has led to the creation of research avenues thereby driving more modernization in the field of MOSFET devices. Renovation of existing electronics systems for enhanced functionality associates amalgamation of an enormous number of MOSFET devices on a single wafer. Hence, to achieve a higher integration density, at an unaltered or cheaper fabrication cost, so as to fit prodigious counts of chips on a single Integrated Circuit (IC), device dimensions need to be scaled down rigorously [1.1]. Device downscaling contributes largely to the reduction of circuit area, diminished power consumption and heightened speed of operation.

The Moore's law, which steers the direction for the entire semiconductor manufacturing industry, dates back to 1965 [1.2]. It states that the number of transistors per chip doubles about every two years. The recent transition of the microelectronics industry to nano-electronic device fabrications is an inevitable phase, the semiconductor industry is currently going through, as governed by Moore's Law and this trend is going to continue in the foreseeable future without any further deviations. This transition phase from microelectronics to nanoelectronics has been marked by several technology nodes based on semiconductor manufacturing process and design rules [1.3]. Each node refers to a generation of MOSFET device design having characteristic gate length. The International Technology Roadmap for Semiconductors (ITRS) provides the assistance and guidelines for each technology node, to be followed by the semiconductor industry. The technology node [1.4], which normally refers to the device gate length, ranges from a value as large as 10 μm to a value as low as 5nm and also exhibits the gradual recorded evolution in the basic

MOSFET geometry owing to continuous shrinkage in device dimensions as a consequence of the Moore's law.

Dating back to 1960, an Egyptian engineer Mohamed Atalla and Korean engineer Dawon Kahng demonstrated the first MOSFET device with a gate length of 10 μm [1.5]. Device scaling continued with the help of available fabrication facilities to achieve higher integration density and upgraded device performance. Basic bulk MOSFET was continuously scaled through 6 μm in 1974, 1 μm in 1984, 600nm in 1990 to 130nm in 2001 [1.6]. However, several unfavorable consequences started to crop up concerning aggressive scaling in nanometer regime. With extremely diminished device dimensions with nanometer limits, bulk MOSFET was exposed to the detrimental consequences as a result of the performance degrading short channel effects (SCEs). Researchers were thus constrained to extend their focus beyond the conventional CMOS technology to basic, bulk MOSFET geometry modification to successfully battle against the SCEs thereby boosting the gate control over the channel.

The 90nm technology node beheld the first breakthrough from the traditional technology of bulk MOSFET to modifying the basic MOS structure by implementation of Silicon-on-Insulator (SOI) in conventional MOSFET. Iranian Engineer Shahidi's research at IBM marked the advent and commercialization of SOI technology in the 90nm technology node [1.7]. SOI technology comprises of a simple modification of sandwiching an SiO_2 insulating layer between the channel and the substrate. The resulting structure exhibits excellent capability of suppressing SCEs, reduced parasitic capacitances, significantly higher speed of operation leading to lower propagation delay, improved radiation hardness, better threshold voltage characteristics causing diminished off-state leakages, improved subthreshold slope, reduced circuit area, latch-up inhibition etc. [1.8 – 1.10]. Inspite of providing countless benefits, SOI technology suffers from some major drawbacks such as self-heating effects, dynamic floating body effect, lack of superior interface quality of buried oxide and channel resulting in increased interface scattering, requirement of critical design adjustments of SOI structures etc. [1.11 – 1.12]. Hence, this research progressed to a step

forward by extemporizing the SOI structure to a Silicon-on-Nothing (SON) structure where the buried SiO_2 layer is replaced with a layer of air (the unity value dielectric). SON technology offers the highest dielectric isolation between the channel and the substrate and drastically reduces the junction capacitances propelling the circuit speed significantly. SON structures have higher immunity to SCEs, have low noise and can be easily fabricated with the state-of-the-art fabrication facilities available in the modern semiconductor industries [1.13 – 1.15]. Researches on SON are still under progress and probability of SON replacing SOI in forthcoming advanced devices are high.

However, persistent demands for further miniaturized devices with reduced power consumption and faster speed unlocked new research avenues in search of advanced devices with developed performance supporting further scalability. In this context, the Multi-gate MOSFET technology caught the center of attention for their unparalleled heightened gate control over the channel. Increasing the channel surface area for greater coverage by the gate enables superior dominance over SCEs allowing ameliorated device performance. Multi-gate MOSFETs such as Double Gate, Trigate, Gate-all-around (GAA), Omega gate, Pi gate MOSFETs are popular for their excellent resistance to SCEs, better threshold voltage characteristics enabling reduced off-state leakages, reduced Drain-induced barrier lowering (DIBL), amended subthreshold characteristics, higher current driving capability, improved scalability etc. [1.16 – 1.20].

Incorporation of innovative technologies in advanced Multi-gate MOSFETs targeting the improvement of some particular performance worsening SCEs have been widely explored by researchers and experimenting with such technologies for further advancement of existing devices are still under consideration. One such technology is Gate work function engineering (GWFE) [1.21 – 1.23] that has worked wonders and unlocked doors to radical improvements in device characteristics. GWFE employs two or more materials having different work function placed adjacent to work as a single gate electrode. This magnificently pioneering concept is the source behind the genesis of unique step profile (at the interface of two or more gate material) in the potential distribution of a device. This

technology single-handedly dominates over major SCEs like DIBL, Hot carrier effect (HCE), Gate-induced drain leakage (GIDL) etc. The technology drastically rectifies the threshold voltage characteristics of the device thereby reducing the threshold voltage roll-off (TVRO) [1.24 – 1.25]. GWFE has enabled better scalability of advanced devices thereby enabling continuation of advanced semiconductor device manufacturing in line with the Moore's law.

Researches encompassing material property improvement in advanced MOSFET devices targeting to control some major SCEs have gained equal importance for playing a crucial role for device characteristics rectification. Material property improvement is one type of the channel engineering scheme, such as addition of strain (Ge content) in the channel for selective feature enhancement of the device. Strained channel MOSFETs provide a prodigious boost to carrier mobility thereby enhancing the channel conductivity. Moreover, suitable selection of strain value in the channel allows suitable tuning of the threshold voltage to a preferred value allowing easy access to suppress some performance worsening SCEs. Strained devices are potential contenders when it comes to high speed circuit operations [1.26 – 1.27]. Graded channel engineering is another established strategy that falls under the scheme of channel engineering. The strategy is accompanied by selective doping in the channel region with high and low concentrations [1.28]. Normally, the region towards the source has high doping, whereas the region near the drain has low doping. The higher doping towards the source allows the source-channel barrier to have greater height compared to the drain-channel barrier. This allows the graded channel architecture to have greater threshold voltage thereby allowing nominal off-state leakages. The strategy also provides an added advantage. The higher doping towards the source side can be tactfully selected allowing to acquire a preferred value of threshold voltage thereby permitting dominance over some SCEs and the lower doping towards the drain reduces impact ionization thereby eliminating parasitic Bipolar Junction Transistor (BJT) effect [1.29].

Apart from channel engineering, dielectric engineering scheme has also been fully exercised by the researchers for selective improvement of the device characteristics from some performance weakening SCEs. Gate dielectric engineering started with the introduction of the 45nm technology node and continued through the 32nm, 22nm

nodes and onwards. Transistor sizes have been reduced to nanometer regime to achieve upgraded device performance while the insulating layer between the gate and the channel has reduced to five atomic layers resulting increased gate oxide leakage currents and boron penetration and makes the transistor unreliable. So instead of scaling the oxide thickness down, the material has to be exchanged. Therefore, the oxide thickness is exchanged by the Effective Oxide Thickness (EOT) with respect to SiO_2 thickness [1.30]. The material is actually thicker than silicon dioxide requires, but exhibits at the same time a much higher k-value. Thus, the gate leakage can be suppressed, while maintaining control over the channel. However, the High-K oxide selection should be done considering the following criteria: high dielectric constant and barrier height, thermodynamic stability, interface quality, gate compatibility, process compatibility, etc. Sometimes, to improve the interface quality, an interfacial layer (such as SiO_2 below the high-k insulator) is used to reduce the scattering effects in the device [1.31 – 1.32]. Dielectric engineering scheme is, nowadays, suitably implemented to devise a bio sensing MOSFET device, and through the process of dielectric modulation, advanced MOSFET are explored and made to function as efficient biosensors [1.33 – 1.34].

Device function reliability is an extremely important parameter that determines the suitability of its operation in fluctuating ambient thermal conditions. Temperature has a colossal effect on device characteristics [1.35 – 1.36]. Existing literature survey reports that a number of silicon channel device properties such as band gap, intrinsic concentration, permittivity of the silicon etc. change within a temperature range of 100K – 500K. At cryogenic temperatures, below 100K, impurity deionization starts to occur whereas at higher temperatures above 500K, the gate oxide starts to show dependence on temperature [1.37]. Thus, at temperature variant environments, the device characteristics show alterations and this necessitates to devise the thermal behavior of the device in order to investigate its temperature-based performance reliability.

The quality of the Si-SiO_2 interface plays a significant role in determining the reliability of device operation. The interface tends to get damaged due to several stress, hot carrier and radiation induced damages. This causes the formation of interface traps

resulting in the generation of positive/negative fixed localized trapped charges at the interface. These charges significantly modify the device features thereby affecting reliable device operation [1.38]. Thus, it highlights the requirement to explore the device features in presence of these charges. Existing literature records exhibit that basic device features like potential, threshold voltage, drain current etc. are significantly altered due to the presence of trap charges [1.39]. Hence, this implies the importance to explore the physics governing the operation of advanced MOSFET devices considering these fixed interface trapped charges.

The comprehensive deliberation presented above guides the track that leads to enormous research avenues for innovative MOSFETs geometry concoctions having grander performance that can be impeccable replacements for suitable implementations in future generation hi-tech VLSI circuit applications.

1.2 Literature Survey

Technological progress has remain unconstrained ever since the demand for faster, miniaturized, cost-effective, power-efficient devices started originating owing to the ceaseless boom, detected more prominently in the past few decades, in the modern semiconductor device manufacturing industries. In this regard, Moore's law [1.40] has been the leading guiding principle for device innovation, which is currently witnessing device architectures being fabricated and scaled down to nanometer limits. This not only leads to miniaturization but also boosts the speed of operation producing low power consuming devices. Device scaling could have been a magical wand for meeting the expectations of the current day consumer markets, however, this technology is also accompanied by some performance deteriorating Short channel effects (SCEs) such drain-induced barrier lowering, hot carrier degradation, increased threshold voltage roll-off, increased gate-induced drain leakage mechanisms, weakened subthreshold characteristics, boron penetration, reduced gate-channel coupling, enhanced junction leakages and parasitic capacitances, [1.41 – 1.43] etc. Continuation of Moore's law coupled with unrestrained pace of aggressive device miniaturization, can incessantly progress only through a blend of device scaling, new device architectures and extemporized device

materials. This has now led to the creation of a gigantic count of research avenues centralizing non-conventional nanodevices with a target to escalate the functionality of the device without negatively impacting the fabrication cost.

1.2.1 Nanodevices: A Brief Compendium

Several nanodevices, each governed by its specific principle of operation, has been highlighted by researchers with an aim to heighten device performances. Some nanodevices take the advantages offered by quantum mechanical phenomena that start to dominate in the nano-scale regime, these mainly include solid state quantum effect devices, single electron devices and molecular electronic devices [1.44].

- ***Solid-state quantum-effect devices, single electron devices***:

The architectural similarity that these devices have in common is a small "island" composed of semiconductor or metal in which electrons may be confined [1.45]. The extent of electronic confinement in these islands give rise to the following different category of nanoelectronic devices.

- ***Quantum Dots (QD)***: Here the island confines electrons with zero classical degrees of freedom remaining [1.46]
- ***Resonant Tunneling Devices (RTD)***: In this case, the island confines electrons with one or two classical degrees of freedom [1.47]
- ***Single-Electron Devices (SET)***: In these devices, the island confines electrons with three classical degrees of freedom [1.48].

Various features such as composition, shape and size of the island give rise to different types of solid-state nanoelectronic devices having their individual properties. The passage of the electrons on and off to the island can be controlled effectively by controlling the above features of the island. This strategy allows to control major device features, for instance, the conductivity of electrons can be boosted by increasing the mean free path to decrease carrier collision or the conductivity can be suppressed as well by quantum mechanical interference. Nowadays, solid-state nanoelectronic devices include the incorporation of channel improvised III-V semiconductor devices where the mobility of

electron is very high and it is also easier to fabricate defect-free junction in these devices compared to the Si or Ge semiconductors [1.49].

- ***Molecular Electronic Devices:*** The search for individual molecule that would behave as an electrical switch dates back to 1974 when researchers Aviram and Ratner proposed the Molecular rectification Theory [1.50]. The research gained momentum during 1990 when Tour et al. exhibited synthesis of spiro-switch proposed by Aviram [1.51 – 1.52]. The acceleration of research in this field can be attributed to the search of innovative devices that support nano-scale miniaturization. Some of these devices include ***Molecular wires***, ***Quantum Effect Molecular Electronic Devices, Electromechanical Molecular Electronic Devices, Electric field controlled Molecular Electronic Devices, Electrochemical Molecular Electronic Devices*** etc. [1.53 – 1.55].

  FET based Nanodevices, such as **Carbon Nanotube FETs**, **III-V channel improvised FET devices**, **Ge channel FET devices**, **Nanowire Field-Effect Transistors (NWFETs)**, etc. have gained significant attention for nanodevice performance up gradation since these are easy to fabricate and supports cost-effectiveness [1.56 – 1.57]. Hence, the endeavor to recognize non-conventional devices to support further scaling in nanometer regime is an interminable process and would continue to enrich the research associated with the field of device innovation. This thesis is also a strive to take a step further for modernization and realization of ultra-thin, non-conventional, nano-scaled, innovative device modeling and simulation to comprehend advanced device performance in overpowering major challenges associated with device downscaling.

1.2.2. Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET): A Brief Synopsis

Among all the FET devices, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [1.59] has proved to be the most propitious structure when it comes to continuation of Moore's law to support higher packaging density coupled with up graded device performance. Invented (in the year 1959) and successfully fabricated for the first time by Mohamed M. Atalla and Dawon Kahng, this device provides a whole host of advantages such as its relatively compact nature compared to other contemporary planar junction

transistors, ease of mass-production, etc. [1.60-1.62]. This device, also known as the "workhorse of the electronics industry", allows elevated scalability with significant miniaturization, consumes less power, offers faster switching operations, comprises of less fabrication steps enabling high manufacturing yield. MOSFET is the fundamental building block in Digital and Analog ICs.

The word "MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor" offers a structural implication about the device architecture. The "Metal", "Oxide", "Semiconductor" implies the operation of a capacitor which is the heart of the working principle of the device [1.63]. The oxide layer (normally SiO_2) is sandwiched between the metal gate electrode and the bulk silicon substrate. The device also has highly doped source and drain regions.

A basic MOSFET device has four terminals namely Source, Drain, Gate and Body/Substrate. In most cases, the Substrate and the Source are connected together making the device, a three terminal one. The device is mainly used for switching and amplification purposes [1.64]. Depending on the nature of the bulk substrate and the type of doping in the source and drain regions, a MOSFET can be of both n-channel and p-channel MOSFET.

For an n-channel MOSFET, heavily doped n-type source and drain regions are implanted into a comparatively lightly doped p-type substrate, the channel between the source and drain is n-type with electrons as majority charge carriers. For a p-channel MOSFET, source and drain are heavily doped p-type regions implanted into a lightly doped n-type substrate, the channel between the source and drain is p-type with holes as majority charge carriers [1.65]. For both channel types of MOSFET, a thin layer of insulator (normally SiO_2) is grown over the region between source and drain, and is called the gate-oxide. Gate-oxide is covered by a metal that forms the gate of MOSFET device. Initially polycrystalline silicon was chosen as the gate material. However, due to limitations in operational speed, a metal is now favored and chosen as gate material instead of polycrystalline silicon gate [1.66]. The metal gate remains insulated from the conducting channel by the sandwiched insulating layer and thus, "no current flows through the gate", which results in very high input impedance in the device.

1.2.2.1. Modes/Types of MOSFET

Based on the nature of operation, MOSFET can be of two types: Depletion-mode MOSFET (can be both n-channel and p-channel) and Enhancement-mode MOSFET [1.67] (can be both n-channel and p-channel).

1.2.2.2. Regions of MOSFET Operation

Based on the applied gate voltage, MOSFET can operate in three regions listed below [1.68]:

i. Cut-off Region:

MOSFET is said to be working in cut-off region if the applied gate-to-source voltage (V_{GS}) is less than the threshold voltage (V_{th}) of the device. In such a situation, no current flows (I_{DS}=0) and the transistor is said to be operating in the cut-off region, acting as an open circuit.

ii. Linear or Ohmic Region:

MOSFET is said to be working in the linear region when the applied gate-to-source voltage is greater than the threshold voltage (V_{GS}> V_{th}) of the device. In such a situation, a channel is induced and current starts to increase linearly for a drain voltage (V_{DS}=0) greater than zero but less than the applied gate-source voltage. The transistor is then said to operate in linear region as a (gate) voltage controlled resistor.

iii. Saturation Region:

MOSFET is said to be working in the saturation region when the applied drain voltage is greater than the saturation drain voltage (V_{Dsat}= V_{GS}-V_{th}) and the applied gate voltage is well above the threshold voltage. The drain current stops to increase linearly and saturates to a constant value. The transistor is then to be "Fully ON".

1.2.3. Complementary Metal-Oxide Semiconductor Field-Effect Transistor (CMOS)

Complementary Metal-Oxide Semiconductor Field-Effect Transistor (CMOS) works based on the complementary mode operation of a p-channel and n-channel MOSFET. This is one of the most popular technology followed to design computer chip and widely used in Integrated Circuits in numerous applications. In CMOS, both types of MOSFET (p and n-channel) are

never ON together at the same time. Thus, CMOS has only OFF state power dissipation which results in overall low power consumption and higher level of noise immunity [1.69].

1.2.4. Limitations associated with MOSFET Scaling

The strategy of device miniaturization has contributed to the technical boom, the modern day semiconductor industry is going through. Continuous extemporizations in the field of device innovation to increase functionality per chip without impacting the fabrication cost has been the main target followed by VLSI Giant industries. However, rigorous device scaling in nanometer regime has its own drawbacks that associate fabrication complexities coupled with some device performance deteriorating alarming effects collectively known as the Short Channel Effects (SCEs).

In miniaturized MOSFET devices, with shrinking channel lengths, the gate loses control over the channel due to increased charge sharing from source/drain [1.70]. This affects the basic device characteristics such as potential distribution, threshold voltage, drain current, device subthreshold characteristics etc. This implies the requirement and incorporation of innovation/renovation in device geometries, device material property improvement, gate-oxide engineering strategies to successfully battle against the various SCEs to achieve upgraded device performances.

As device dimensions get limited to extremely smaller dimensions, circuits become denser and complex. Hence, several fabrication complexities such as creating high doping concentrations in ultra-shallow source/drain regions, precise lithography, proper interconnects and processing become extremely difficult to achieve. Moreover, interface gets damaged and trap charges are produced as a result of enhanced fabrication issues. Apart from these physical challenges, major quandaries are encountered during design, testing and packaging of highly dense ICs. This calls for the necessity of introduction and application of evolutionary/revolutionary device structures to keep the pace of the technological development unhindered as much as possible.

1.2.5. Some of the Different Types of Short Channel Effects (SCEs)

A MOSFET is said to be Short channel MOSFET when its effective channel length is the same order of magnitude as the depletion-layer widths of source and drain [1.71]. In order to keep pace with Moore's law to support unhindered progress of the current semiconductor industry, MOSFETs are being continuously scaled down which results in some inevitable performance deteriorating effects collectively known as the Short channel effects (SCEs). Hence, researchers are in continuous pursuit of device innovation to keep these SCEs in check. A detailed insight of these effects are listed below [1.72].

1] Electric Field becomes 2-D in Short channel MOSFET

In long channel MOSFETs, the drain current flowing in the channel between source and drain is controlled by the gate and hence, only the vertical field is dominant. However, in short channel MOSFETs, the source and drain come close to each other, hence apart from the vertical field imposed by the gate bias, the horizontal electric field due to the drain bias also come into play. Thus the current flowing between source and drain gets controlled by both the vertical and horizontal electric field resulting in the advent of a series of unwanted SCEs. This constrains the use of Gradual Channel Approximation (GCA) [1.73] for evaluation of device characteristics in a short channel MOSFET.

- ***Threshold Voltage Roll-Off (TVRO) and Drain-Induced Barrier Lowering (DIBL):***

  In short channel MOSFETs, the channel length is the same order of magnitude as of the source and drain depletion regions. Due to incessant scaling of channel length, these depletion regions of source and drain come close to each other resulting in charge sharing. Hence the charge in the channel is no more solely controlled by the gate. The charge sharing between source and drain strengthens the horizontal electric field and thereby the charges in the silicon channel encounter a two-dimensional charge sharing exerted by the gate bias and drain bias respectively. It is well-known that to trigger current conduction in the channel, the channel needs to be inverted first. In long channel devices, application of gate bias, greater than the device threshold voltage, is solely responsible for channel inversion, however in short channel MOSFETs, the inversion is now controlled by the drain bias in

parallel to the gate bias. Hence, as the drain bias comes into play to create channel inversion, a small amount of gate bias is enough to reach threshold causing channel inversion implying a consequent reduction in device threshold voltage. This phenomenon is termed as the threshold voltage reduction causing threshold voltage roll-off (TVRO) [1.74] as an immediate outcome of channel scaling. This effect can be clearly comprehended from the surface potential distribution of the short channel MOSFET also.

In long channel MOSFET, a uniform potential barrier exists across the device and source and drain electric fields are influential near source and drain ends only due to enough large separation between source and drain. Thus applying a gate bias greater than threshold voltage inverts the channel triggering conduction. However, in short channel MOSFETs, the source and drain being close to each other, the drain potential now interferes and reduces the source-channel barrier, thereby allowing transportation of carriers from source to channel by overcoming the potential barrier. In this situation, application of a small gate bias triggers conduction even before the threshold condition is reached. This results in drain-induced unwanted enhancement of subthreshold current increasing the power consumption of the device. This phenomenon is termed as Drain-induced barrier lowering (DIBL) [1.75] which is one of the major challenges in short channel MOSFETs. The strength of DIBL is usually measured as the difference in threshold voltage V_{th} between a low (approximately 50-100mV) and a high drain bias [1.76]. A hefty value of DIBL represents a device having poor SCE immunity with worsened threshold voltage characteristics such as increased TVRO and high subthreshold current.

- ***Reduction in Mobility due to Gate-induced surface fields:***

Device downsizing encompasses not only channel length scaling but also parallel scaling of the gate-oxide thickness. This proportional scaling of gate-oxide thickness results in a highly dominant transverse electric field exerted by the gate directed towards the channel. Thus the carrier in the channel experience a pull towards the gate, experience high level collision and get speeded towards the semiconductor-gate-oxide interface. This phenomenon impacted due to the strong transverse gate exerted electric field is known as surface scattering [1.77] which is responsible for reduction in carrier mobility in the channel to a

great extent making it increasingly difficult for the carriers to flow parallel to the interface. It has been scientifically observed that even a small increase in this gate induced transverse field results in additional scattering causing the average surface mobility to get diminished to half of the bulk mobility.

- ***Gate-induced Drain Leakage (GIDL)***

GIDL is one of the primary leakage mechanisms that highly contribute to increase in off-state power dissipation and heating in the short-channel MOSFETs [1.78]. When the gate voltage is zero or negative and the drain voltage is positive, the region near the n+ drain is depleted. Due to high doping in the n+ drain, the depletion region is narrower causing the electric field lines to crowd near the drain causing the electrons to tunnel into the drain. While the holes tunnel into the channel creating a path for the off-state leakage current known as the GIDL current. Considering an NMOS transistor having a p-type substrate, when the gate voltage is zero or negative, the channel is in the accumulation mode with accumulation of holes near the oxide-channel interface. Thus the surface region acts as heavily p-doped region compared to the substrate. Thus the depletion region due to the heavily doped p-type surface and heavily doped n+ type drain at the drain-channel interface is thinner. This thin depletion region along with high electric field lines crowding in this region assists the GIDL current in the device.

2] <u>Electric-field strength becomes very high in the channel</u>

If the supply voltage is not scaled down proportionally with the scaling down of channel length in MOSFETs, the channel electric field becomes substantially high. This results in some unwanted SCEs that deteriorate device performance [1.79].

- ***Carrier Velocity Saturation***

When the supply voltage is not scaled down with the scaling of the channel length, the channel electric field significantly increases resulting in carrier velocity saturation. At such high electric fields, the linear relationship between the velocity and electric field fails to exist, instead the velocity saturates as a direct outcome of optical phonon induced increased scattering rate [1.80] of highly energized carriers. Normally, a 100KV/cm electric field

causes velocity saturation of electrons and holes. In submicron MOSFETs, the electric field can be as high as 400KV/cm, hence the average electron velocity in such a device is much larger than that in the bulk.

- ***Impact ionization near drain***

Impact ionization in short channel MOSFETs is one of the major SCEs that causes device performance deterioration by creating a parasitic BJT within the MOSFET [1.81]. Impact ionization is mostly common with n-channel MOSFETs rather than p-channel MOSFET due to higher mobility of electrons. When the applied drain-source voltage is considerably high, the electric field near the drain end exceeds its maximum value imparting a large kinetic energy to the carrier electron which can now easily knock out other electrons from their bound state and promoting them to their conduction state. This phenomenon causes the creation of a large number of electron-hole pairs.

These electrons are then accelerated towards drain under the influence of the drain bias whereas the holes are collected in the substrate thereby creating an n-p-n parasitic BJT, where the source and drain regions act as emitter and collector and the substrate acts as the base. The holes resulting from this avalanche breakdown creates a voltage drop, which when exceeds 0.6V, then the source-substrate junction becomes forward biased resulting in current conduction, in form of electron injection from source (emitter) to substrate (base). As these electrons reach the drain, more electron-hole pairs are generated making the process of impact ionization a cumulative one.

- ***Hot Electron Effect***

As the device is being continuously scaled down, the horizontal electric field substantially increases imparting a large kinetic energy to the electrons in the channel [1.82]. The term "hot electron" basically implies to an electron having sufficient kinetic energy. These electrons are capable of even penetrating the semiconductor material instead of their usual conduction through the channel. While penetrating, the excess energy of the electrons is given off in the form of phonons. Very high electric field near the drain end enables the

electron to jump into gate or substrate resulting is increased leakage currents and enhanced power dissipation.

- **Parasitic Bipolar Effect**

Impact ionization at the drain end results in creation of a large number of electron-hole pairs through avalanche multiplication [1.83]. These holes accumulate in the substrate region thereby increasing the net positive charge of the substrate with respect to the source which is grounded. Thus the source (n-type) - substrate (p-type) junction gets forward biased resulting in the formation of a parasitic BJT, where the n-type source acts as emitter, the p-type substrate acts as the base and the n-type drain acts as the collector. Due to forward biasing of the source-substrate junction, electrons from the source are injected into the substrate underneath the inversion layer causing substantial enhancement in the drain current. These electrons on reaching the drain end again create numerous electron-hole pairs through avalanche multiplication. The net positive feedback that exists between the avalanche breakdown mechanism and the parasitic bipolar action results in breakdown at much lower drain voltage.

- **Gate-oxide Charging**

Channel downscaling in MOSFETs results in considerable increment in the vertical and horizontal electric fields that impart sufficient kinetic energy to create "hot electron" in the channel. These "hot electrons" can now easily overcome the potential barrier exiting at the channel-gate-oxide interface. Over the time, the quality of the oxide gets compromised due to a gradual accumulation of such electrons and ultimately causes oxide breakdown. This phenomenon in short channel MOSFETs is termed as **time dependent destructive breakdown (TDDB)** or **hot electron ageing** [1.84]. This phenomenon can be avoided to a large extent by replacing the conventional SiO_2 with some alternative oxides having much higher dielectric constant than SiO_2. Hence, the same gate capacitance can be obtained with a thicker gate oxide. However, in considering these oxide replacement in short channel devices, some important parameters like stability, reliability, breakdown voltage as silicon dioxide etc. has to be considered to keep the performance of the device superior compared

to the devices with conventional SiO_2. The alternative oxides considered as good replacements of SiO_2 are Al_2O_3, ZrO, TiO_2, HfO_2 etc.

3] <u>Diminished Physical Separation between Source and Drain</u>

Due to device miniaturization, there is an inevitable reduction in the physical separation between source and drain. This leads to some inexorable SCEs to crop up thereby deteriorating device performance. Some of these effects are summarized as follows [1.85]:

- **Channel-length Modulation**

Channel-length Modulation (CLM) [1.86] is common form of SCE that occurs in a short channel MOSFET with a low-doped body. When the drain bias in such a device is increased, the depletion region around the drain increases which results in decrease of the effective channel length. The resulting channel length is approximately equal to the actual/metallurgical length minus the source and drain depletion widths. CLM has significant effect on the output characteristics of a device.

- **Punch through**

Punch through [1.87] is an extreme case of CLM. When the drain bias is very high, the depletion region around the drain extends and merges with the depletion region of the source hence reducing the effective channel length to zero. This phenomenon is known as Punch Through. Current conduction in the channel is then entirely controlled by drain bias and rapidly increases with the increase in drain bias.

1.2.6. Some Innovative Technologies to Enhance MOSFET SCE Immunization

Unconstrained development in the contemporary semiconductor and VLSI industries is only possible through device scaling and innovation combined with material property improvement. The bulk MOSFET device could no longer battle against the performance worsening SCEs making it inevitable for continuing relentless researches to find advanced MOSFET devices.

1.2.6.1. Silicon-On-Insulator (SOI) MOSFET

Silicon-on-Insulator (SOI) [1.88] technology has been widely favored since it not only supports further scaling but also provides additional advantages to upgrade device performance. Though the concept of SOI technology was first provided by C.W. Miller and P.H. Robinson back in 1964, however, the first commercially viable SOI devices was first demonstrated by Ghavam G. Shahidi, the chief architect of SOI technology at IBM Microelectronics.

This technology is accompanied by incorporation of a thick layer (hundreds of nanometer) of silicon dioxide between a thin layer (tens of nanometer) of silicon channel and a thick layer of silicon substrate. The oxide layer that isolates the channel from the bulk substrate is generally called the Buried Oxide (BOX) layer. Fabrication of such BOX layer is normally done using oxidation of silicon substrate or by oxygen implantation into silicon. If the thin channel is mono-crystalline silicon then the resulting device is called Silicon-On-Insulator (SOI) MOSFET [1.89].

- ***Operating Modes of SOI MOSFETs*:**

SOI MOSFET devices have two modes of operation, Partially Depleted (PD) SOI MOSFET [1.90] and Fully Depleted (FD) MOSFET [1.91].

In PD SOI MOSFET, the depletion layer under the gate-oxide does not cover the entire channel layer. Thin, undepleted layers of neutral charge exists beneath the depleted layer, even after the channel inversion mode is achieved after proper bias application. Hence, it can be easily comprehended that the silicon channel thickness is greater than the gate depletion width and the neutral region that still exists beneath this depleted layer is called “body”. In FD SOI MOSFET, the channel thickness is less than the depletion gate width, so that the entire channel gets covered by the depletion layer when gate bias is applied (even before reaching threshold condition). In this way, the floating body effect can be completely eliminated in FD SOI MOSFET [1.92].

FD SOI MOSFETs have a number of advantages compared to the PD SOI ones. Attractive benefits such as protection from kink effect [1.93] due to absence of floating body, diminished power consumption that contributes to upgraded subthreshold features which in turn increases the circuit speed, soft-error immunization [1.94], use of lesser number of masks leading to ease of fabrication [1.95] etc. can be obtained with FD SOI MOSFETs and are hence a common selection for incorporation in advanced VLSI circuit operations.

SOI has gained parallel popularity in the research field as well where researchers have presented extensive investigation of the physics that govern the operation of such devices. Agarwal et al. [1.96] presented a compact analytical surface potential model using 1-D Poisson's equation for all three surfaces (gate oxide–silicon film interface, silicon-film–buried oxide interface, and buried Oxide–substrate interface). Whereas, K. K. Young [1.97] has considered the channel potential to be parabolic at low drain-source voltage in short channel FDSOI MOSFET. Through the solution of 2-D Poisson's equation, potential distribution of the device has been explored along with a short channel immunization investigation revealing that FDSOI MOSFETs offer better immunity than the bulk devices in terms of SCEs. Zhang et al. [1.98] conducted and published a research considering a vertical Gaussian doping profile in the channel of an FD SOI MOSFET. Whereas Rao et al. [1.99] studied the impact of random dopant fluctuations effects in FD SOI MOSFET by analytical modeling.

SOI architectures are fabrication feasible. The detailed step-by-step fabrication is explained and detailed in US patent US6627519B2 [1.100]. The fabrication step comprises of preparing a silicon wafer of desired thickness and diameter, generating an alumina or other dielectric film to work as an insulator on the top of the wafer using processes like ALE, ALCVD, ALD, ASCVD etc. This is followed by bonding the first wafer having the insulator with another silicon wafer using bonding techniques such as Unibond. Then one of the bonded wafers is cut using the Smart Cut method or other suitable methods. The cut surface of the bonded wafer is then polished to make it smooth. The new SOI wafers will be fabricated with less than $2/3^{rd}$ of the heat actually required for the SiO_2 process. This enables to cut down the cost of fabrication and enhances quality of the Si film and buried insulator. The process also

enables to suppress leakage current by more than 1000 times compared to that in SiO_2 process.

Another invention namely US patent 5,882,987 [1.101] (Smart Cut process with thin film semiconductor material on insulating film) claims manufacturing of SOI wafers using Smart Cut process and CMP process to address non-uniform surface and thin film formation problems normally associated with the Smart Cut processes. In case where SiO_2 is the buried insulator, then it is controlled using conventional oxidation technologies.

- ***Advantages of SOI Architecture***

Incorporation of BOX layer in bulk MOSFETs can drastically enhance device performance which is obvious due to a whole host of benefits that SOI devices offer. Some of the benefits are listed as follows:

Reduced Parasitic Capacitance [1.102], Ideal Device Isolation [1.103], Smaller Layout Area [1.104], Latch-up Inhibition [1.105], Enhanced SCE Immunity [1.106] etc. Additionally, SOI devices have exhibited radiation hardness, good soft error immunity, stacked gate speed improvement [1.107] etc.

- ***Disadvantages of SOI MOSFETs***

In spite of exhibiting commendable benefits, SOI devices still suffer from some drawbacks, which are listed below:

i) Floating body in PD SOI MOSFET results in "kink effect" that causes drain-current overshoot in switching circuits.

ii) Dynamic floating body effect and parasitic bipolar effect degrade the device performance to a large extent that necessitates to renovate SOI structure further.

iii) Forward biasing of source-substrate junction results in substantial off-state leakage currents.

iv) Requirement of many critical design adjustments for fabricating ultra-thin films for FD SOI devices.

v) Near to ideal interface quality of BOX and silicon is needed to minimize surface scattering effects.

vi) Self-heating effect in SOI leads to weakened device performance reliability.

However, a substitute structure to SOI MOSFET has been brought to the forefront namely Silicon-On-Nothing (SON) MOSFET which has some appreciable advantages over other SOI structures to successfully suppress the performance deteriorating short channel effects. Even though some experimental structures of SON have been projected but significant research on analytical modeling of SON devices is still being continued and it is anticipated that SON may replace SOI devices in the forthcoming device innovation scenario.

1.2.6.2. Silicon-On-Nothing (SON) Structure

In order to overcome the disadvantages of SOI devices, innovation was made to progress a step further with the introduction of Silicon-on-Nothing (SON) technology [1.108]. Skotnicki et al. [1.109] reported a research on SON technology where the fabrication process is also highlighted. Using the epitaxial growth technique, SiGe layer can be sandwiched between mono-Si layers without modifying their conduction characteristics. SiGe layer is used as a sacrificial layer and then by selective lateral etching of SiGe layer, the thin Si channel can be isolated from the substrate using a cavity. Jurczak et al. [1.110] presented the step-by-step key fabrication process of SON technology and also demonstrated the advantages of SON over SOI and bulk devices.

To continue with device downsizing without negatively impacting the device performance, SOI structure has been further improvised to Silicon-On-Nothing (SON) structure by replacing the BOX layer of SiO_2 with the unity value dielectric, i.e. air. This simple modification can effectively upgrade SCE immunization exhibiting superior electrical performance. SON supports commendable scalability that asserts sustenance of Moore's law contributing further progress of modern semiconductor and VLSI industries.

- ***Advantages of SON Architecture***

SON architecture provides the highest dielectric isolation, compared to FD SOI, between the active channel and the substrate regions. The unity value dielectric of the buried air layer, owing to its lower permittivity, diminishes the electrostatic coupling and thus relaxes the requirement of an ultra-thin film silicon channel layer in the device. The parasitic capacitances of source-substrate and drain-substrate are radically reduced due to the buried

air layer, hence an improved circuit speed is the immediate result of the reduced parasitic capacitances. SON structure retains all the advantages offered by SOI architecture [1.111]. In addition, SON offers better scalability, reduced power consumption, improved speed of operation, superior SCE immunity, radiation hardness in extreme environments, low noise, etc.

1.2.7. Multi-Gate MOSFETs for Better Electrostatic Gate Control

Significant alleviation of device performance worsening SCEs can be achieved through superior gate-channel electrostatic coupling that allows precise control over the carriers flowing through the channel. This allows better threshold voltage characteristics paired with improved subthreshold behavior of the device. Better gate control causes the DIBL to get significantly suppressed which reduces various leakage currents enabling diminished power consumption and dissipation. In this context, Multi-gate MOSFETs play a pivotal role where presence of more than one gate radically improves the device characteristics [1.112]. Some examples of Multi-gate MOSFETs that have considerably excelled in lessening SCEs are Double-gate MOSFETs, Trigate MOSFETs, Surrounding Gate-all-around (GAA) MOSFETs etc.

1.2.7.1. Planar Double-Gate MOSFET

Double-Gate (DG) MOSFET [1.113] is one of the most promising Multi-gate architectures for advanced applications in VLSI circuits. These devices are basically two dimensional or planar MOSFETs. Addition of one extra gate to the architecture doubles the gate-channel coupling thereby mitigating the SCEs to a large extent. Other benefits of DG architecture includes high transconductance, up graded subthreshold swing characteristics. In DG MOSFETs, two gates simultaneously control the channel, thus availability of the two channels results in improved threshold voltage characteristics that offers better current drivability. Finally, lightly doped, ultra-thin layers are available for DG architectures thus enabling better scaling capabilities with these devices.

Liang et al. [1.114] exhibited DG MOSFET features by solving a 2-D Poisson's equation mathematically and through simulation. Expressions for the potential and drain current in subthreshold region have been obtained. The results exhibit reduced SCEs like threshold voltage roll-off, subthreshold slope. Chiang et al. [1.115] demonstrated a

scaling parameter dependent model for subthreshold swing of Double gate MOSFET. A detailed subthreshold characteristics investigation has been exhibited by solution of 2-D Poisson's equation following proper boundary conditions. Double gate MOSFETs also offer high transconductance, improved subthreshold operation, double gate control over the thin channel allows higher current driving capability.

1.2.7.2. 3-D Trigate MOSFETs

Technology transition from planar 2-D MOSFET to a non-planar 3-D Trigate MOSFET has been a revolutionary step that has been first introduced by Intel [1.116]. This avant-garde technological breakthrough has set a benchmark in satisfactory device performance enabling further continuation with the Moore's law. The main advantage of the device lies in its architecture where the gate wraps around three surfaces, enabling an increase in three times the surface area for the electrons to travel. The gate control over the channel (on three sides) gets dramatically enhanced which contributes to significant alleviation in SCEs. DIBL, HCE are substantially reduced owing to enhanced gate control. Various leakage currents are minimized that lead to better subthreshold characteristics. Preferred value of threshold voltages can be obtained with these devices that enables higher switching speed and requirement of lower supply voltage. It has been exhibited by Intel that Trigate transistors show 37% speed enhancement compared to the planar transistors. Also, these ground-breaking technology based devices exhibit 50% reduction in power consumption compared to their planar contemporaries and also offer higher drive currents and supports low cost of fabrication compared to FDSOI technology [1.117].

Tsormpatzoglou et al. [1.118] presented a semi-analytical modeling of short channel effects in a lightly doped Trigate MOSFET. The 3-D potential distribution has been obtained by solving the 2-D Poisson's equation for two double gate MOSFETs. Solution of 3-D Poisson's equation has been tactfully avoided in the research presentation by considering the Trigate MOSFET of square or rectangular cross-section as two independent double gate MOSFETs, one with symmetric and the other with asymmetric gates. The two side gates consist of the symmetric DG MOSFET whereas the top gate and the bottom oxide corresponds to the asymmetric gate with zero bias applied to the bottom gate. The 3-D

potential distribution expression has been obtained by solving 2-D Poisson's equation separately for the asymmetric and symmetric DG MOSFETs followed by the Superposition principle. Comprehensive analyses of potential, drain current, threshold voltage roll-off, subthreshold swing and DIBL have been presented where the device channel thickness is considered as one of the main variation parameters. Later, Ghanatian et al. [1.119] presented an analytical modeling and simulation of the subthreshold swing characteristics of a Trigate SOI MOSFET. Through a solution of 3-D Poisson's equation, the solution for surface potential is obtained and subsequent calculation of subthreshold swing reveal upgraded device characteristics. Considering the solution of 3-D Poisson's equation for potential expression in TG MOSFETs is tedious, however, the accuracy is quite appreciated.

1.2.7.3. Surrounding Gate-All-Around MOSFET

Dramatic device performance enhancement has been observed with the strategy of completely wrapping the channel by the gate through the gate-oxide. This remarkable device, popularly known as the Surrounding Gate-all-around (GAA) MOSFET [1.120] has excelled its contemporary devices in successfully suppressing various performance weakening SCEs. The gate wrap around the channel that significantly reduces the leakage currents thereby leading to lower power consumption and dissipation in the device. Precise gate control over the channel regulates and rectifies threshold voltage characteristics, diminishes DIBL, suppresses HCE and subthreshold swing. The wrap around structures support further scaling thereby proving themselves as perfect alternatives for successful implementation in future generation VLSI circuits.

Surrounding GAA MOSFETs can be quadruple GAA MOSFETs [1.121] with square cross-section or cylindrical GAA MOSFETs with circular cross-section [1.122].

- **Quadruple GAA MOSFETs**

Quadruple GAA MOSFETs have the gate wrapped all around the channel on four sides. The device normally has a square cross-section. QD GAA MOSFETs offers excellent gate control over the channel thereby offering a boost to the current drivability, mobility enhancement, effective suppression of major SCEs, higher packaging density etc. In spite of offering a whole

host of advantages, these devices suffer from a major drawback known as the corner effects that arise due to electrostatic coupling of the two adjacent gates at the corners. This causes device degradation by increasing the off-state leakage currents thereby resulting in increased power dissipation and device heating. The effect can be eliminated by rounding off the corners, which is however, a very delicate and complex process. Thus, using Cylindrical GAA MOSFETs having ideal circular cross-section can eliminate this corner effect and offer better device performances. [1.123].

- ***Cylindrical GAA MOSFETs***

Cylindrical GAA (CGAA) MOSFETs [1.124] exhibit better SCE resistance coupled with upgraded device performance as compared to Quadruple Gate MOSFETs since the later device suffers from corner effects. CGAA MOSFETs demonstrate strong field confinement, enhanced gate-channel coupling thus offering elevated electrostatic control that aids SCE immunization. DIBL, HCE, Subthreshold swing characteristics get radically rectified making the device a supreme one in terms of offering enhanced device characteristics. The device is extremely popular for enabling continuation of further device scalability enabling higher packaging density.

A latest innovation in the architecture of CGAA MOSFET has been noticeable in the current day literature. This structure is popularly known as Macaroni GAA MOSFET which is featured with a hollow insulating pillar at the channel center. Literature reports exhibit that this simple architectural modification in CGAA MOSFET has resulted in remarkable short channel effect immunization and ameliorated device performance compared to the conventional CGAA MOSFETs [1.125]. This geometry enables precise and enhanced gate control over the channel and this will be further evident from researches related to this thesis.

1.2.8. Some Pioneering Strategies for Device Performance Enhancement

A significant boost in nano-scaled advanced multi-gate MOSFET device performance has been enabled by researchers using various ground-breaking techniques such as Gate Work Function Engineering (GWFE), Channel Engineering, Dielectric Engineering etc. These

schemes are implemented in advanced MOSFET devices to amend device properties through rectification of some targeted SCEs as well as to tune device features to preferable values. Through these pioneering technologies, significant gate-channel coupling is aimed so as to suppress major detrimental SCEs thereby upgrading the device characteristics as a whole. Some of these technologies are listed as follows:

1.2.8.1. Gate Work Function Engineering

The pioneering Gate work function engineering (GWFE) scheme, where the gate electrode is made of two or more materials having different work functions, has drastically set the performance of ultra-scaled devices to very high levels. The technology single-handedly allows significant dominance over major SCEs like DIBL, HCE, GIDL, etc. This unlocked another door to device innovation and advancement by providing excellent immunity to SCEs and contributing to further scalability. Researchers have widely explored the GWFE scheme and exhibited evidences of remarkable progress in device performances. GWFE scheme ranges from employment of Double Materials in gate, hence naming the technology as Dual-Material Gate (DMG) to Triple Material in gate thereby naming the technology as Triple Material Gate (TMG). The DMG technology is accompanied by incorporation of a high work function gate material towards the source side followed by a low work function material gate at the drain side. This allows formation of a unique step-profile (at the interface of two dissimilar materials) in the potential distribution of the channel along with a formation of source-shifted minimum. This permits to have major dominance over SCEs like DIBL. Also, the slope reduction in potential distribution towards drain end allows superior immunity over HCE compared to devices without GWFE. Also, the low work function material towards the drain end significantly work towards the reduction of GIDL in these devices. The leakage mechanisms are remarkably suppressed leading to better threshold and subthreshold characteristics. TMG employs three gate materials, the gate material with highest work function is placed towards the source followed by a lower work function material at the center after which the lowest work function material is placed at the drain end [1.126]. This includes two step-profiles in the potential distribution, and the more the steps, the higher is the immunity towards SCEs. However, fabrication of TMG in ultra-scaled

nano MOSFET devices is quite challenging and hence requires careful optimization considering the state-of-the-art fabrication amenities. Researchers have strategically implemented GWFE in advanced nano-scaled MOSFETs and every time, the scheme has exhibited evidences of grander performance. Reddy et al. [1.127] presented a detailed analytical modeling and simulation Dual-Material DG SOI MOSFET where the authors illustrated a comparative investigation of SCEs in DM (GWFE) and SM (without GWFE) devices. Through solution of 2-D Poisson's equation and following Young's popular parabolic potential approximation, the solutions for surface potential, threshold voltage and subsequent drain current are obtained. The GWFE device excelled the SM device in terms of SCE immunity, the projected device showed better threshold voltage, drain current performances, portrayed extreme dominance over DIBL, TVRO, HCE etc. This can be attributed to the fact that the projected device has a unique step profile due to GWFE whereas this feature being absent in SM devices, the latter are extremely prone to major SCEs. GWFE has been successfully implemented in advanced devices and still remains one of the smartest technology till date for effective reduction of major SCEs.

1.2.8.2. Channel Engineering

Apart from the GWFE technology, effective schemes like channel and dielectric-engineering are also of high interest to the researchers, since these schemes are highly effective in diminishing some targeted SCEs in nano-scaled advanced MOSFETs. Graded channel MOSFETs, halo doped MOSFETs and strained channel MOSFETs are some common ways of channel engineering. These innovative technologies have successfully suppressed the SCEs as evident from the researches already presented.

- **Graded Channel MOSFET**

This technology is accompanied by a high doping region towards the source side and a low doping region towards the drain side. The high doping towards the source region increases the source-to-channel barrier height and thus considerably reduces SCEs. Careful selection of the graded concentrations (high and low) can help is effective suppression of major SCEs

like TVRO, thereby rectifying the threshold voltage characteristics. It also helps tuning of threshold voltage to a preferred value, not too high, not too low [1.128].

- **Halo doped MOSFET**

In this technology, the small pocket regions near the source and drain are highly doped which results in reduced SCEs. Halo implantation devices show excellent output characteristics with low DIBL, higher drive currents, improved saturation characteristics, and slightly higher breakdown voltages compared to the conventional MOSFET [1.129].

- **Strained Channel MOSFET**

In this technology, the atoms of silicon are stretched beyond their interatomic distance. This can be achieved by placing a layer of silicon atoms over the Silicon Germanium (SiGe) substrate. The atoms in the SiGe layer are arranged quite a distance apart. Thus when the layer of Si atoms are placed over the SiGe substrate, the Si atoms are stretched further apart and hence resulting in decreased interatomic distances and interatomic forces that interfere with the movement of electrons. Hence, electron in the strained Si channel move 70% faster resulting in an enhanced transistor switching of 35% compared to the normal MOSFET. Apart from the boosted carrier mobility, strained MOSFETs are also capable of decreasing the severe SCEs and offering upgraded device performances [1.130].

1.2.8.3 Dielectric Engineering

Dielectric engineering associates different types of dielectric configurations that are implemented strategically for performing different set of targeted functions. One of the configurations include use of a high-k gate stack in advanced MOSFETs. The gate stack is formed using a high-k oxide placed over an interfacial layer of silicon dioxide. The continuous scaling of the devices in nanometer regime requires parallel scaling of the SiO_2 gate-oxide because thicker gate-oxide results in diminished gate control over the channel leading to weak gate-channel coupling. On the other hand, the ultra-thin, scaled gate-oxide fails to perform satisfactorily due to increased gate-oxide leakages and boron penetration thereby radically affecting the device operation reliability. This can be efficiently avoided using the

gate-stack technology, where the effective oxide thickness (EOT) is much lesser leading to a strong gate-channel coupling along with enhanced gate-capacitance due to high-k material [1.131]. The configuration has been extensively used by researchers since the technology is popular for efficient upliftment of subthreshold characteristics, reducing off-state leakages, improves carrier mobility by reducing phonon scattering, etc. [1.132 – 1.133]. Another technology of dielectric engineering includes placing two different gate-oxides side by side, together forming the gate-oxide system for the device. The gate capacitance for each gate-oxide changes which is reflected in the basic characteristics such as potential, threshold voltage, drain current etc. of the device. The technology has been successfully explored and incorporated in advanced MOSFETs to make the devices work as an efficient Biosensor [1.134]. The method is popularly known as dielectric modulation, where each k-value of the dielectric corresponds to the k-value of the bio molecule, and by varying the oxide, the k-value changes and alters a device characteristic, which then acts as a metric to detect the type of biomolecule used.

1.2.9 Some Factors Controlling Device Performance Reliability

Reliability of device performance is an extremely vital part of successful device application in modern day VLSI circuits. Ideally unaffected device performance is extremely hard to achieve, however, this also necessitates the investigation of physics concerning the major factors on which device consistency depend. Short channel advanced MOSFETs along with innovative technology incorporation are devised with an expectation of achieving remarkable device performance over a wide range of temperature. However, it is a well-known fact that thermal fluctuations are highly responsible for device behavior alterations, which thus necessitates thermal characterization of the device. Additionally, Si-SiO_2 interface quality is another parameter on which device behavior is found to depend significantly. An ideal Si-SiO_2 interface is extremely difficult to achieve, since the interface tends to get damaged due to fabrication related process parameters, hot carrier induced effects, radiation damages etc. These give rise to fixed local trapped charges at the interface thereby substantially affecting reliable device performance. Hence, physics behind such

damaged interface induced device behavior shift demand equivalent consideration in pursuit of efficacious device operation.

- ***Thermal Characterization:***

Thermal characterization of device operation has been significantly under consideration, since the device features are observed to have extensive dependence on temperature. A number of silicon channel parameters such as band gap, intrinsic concentration, Fermi level, flat-band voltages etc. are temperature dependent and are inevitable to alter under fluctuating temperature conditions [1.135]. Higher temperatures have different effects on device parameters and features whereas at lower temperatures, other physical phenomenon starts to occur in the devices. At cryogenic temperatures below 100K, device suffers from impurity deionization and thus, realization of such physical phenomenon requires an altogether different mathematical modeling approach. Whereas, at high temperatures above 500K, the permittivity of gate-oxide SiO_2 starts exhibiting temperature dependence [1.136]. Even this temperature range from 100K-500K has significant effect on device features where, it has been observed that high temperatures tend to increase leakages by lowering device threshold voltage leading to prominent SCEs in the device [1.137]. Thus, thermal characterization of a device provides a detailed insight about the device reliability and its associated device operation.

- ***Fixed Interface Trapped Charges***

The Si-SiO_2 interface in short channel MOSFETs tend to get damaged owing to several stresses associated with fabrication related process parameters, radiation and hot carrier effects [1.138-1.139]. These damages are responsible for the formation of traps at the interface. For an acceptor type trap, its energy level is located below the Fermi level. If this trap accepts an electron, it will behave as a negative type trap charge. However, if the energy level of the trap is above the Fermi level for a donor type trap, it will lose an electron becoming a positive type trap charge. These trap charges significantly alter the flat-band voltage of the device, which, in consequence, severely affect the potential distribution, threshold voltage, drain current of the device [1.140]. Thus trap-based mathematical

modeling provides a comprehensive understanding of the trap-based reliability of device operation.

Thus this section has presented extensive insights to the basics of nano devices starting from the bulk MOSFET to advanced innovation in short channel MOSFETs. Device operation of nano scaled MOSFET is relentlessly deteriorated owing to various short channel effects discussed comprehensively in this section. Hence to upgrade device performance, copious unconventional nano MOSFET devices are being currently under investigation by researchers which have also been highlighted concisely here to provide an impression about the contemporary progresses in the arena of semiconductor MOSFET devices.

1.3. Organization of Thesis

The thesis has been organized as different chapters to highlight and segregate the advanced Nano MOSFET devices based on the several types of technologies that have been strategically implemented to suppress several short channel effects (SCEs) without negatively impacting the associated fabrication costs and to upgrade the device performance. The thesis starts with chapter 1 encompassing a brief literature survey about the associated field of research, followed by chapter 2, 3, 4 and 5 that highlight several researches conducted to project advanced Nano MOSFET devices along with introduction of successful implementation of several novel technologies through analytical modeling and simulation. The thesis finally ends with a concluding chapter 6 that also includes some future scopes of the research work.

- **Chapter 1** presents a comprehensive overview of on the fundamental concepts of nanodevices, long channel bulk conventional MOSFET device, the problems associated with device miniaturization and innovative, fabrication feasible technologies that can be incorporated in short channel advanced MOSFETs to achieve ameliorated device performance.

- **Chapter 2** demonstrates the analytical modeling and simulation of an advanced Nano MOSFET biosensor where novel strategies like a Dual-Material Trigate and also a Dual-Material bottom gate have been considered. Dual-Material gate introduces step profile that causes suppression of major SCEs like Drain-induced barrier lowering (DIBL), hot carrier effect (HCE), etc. A high-K gate stack has been incorporated towards the drain side that allows upgraded subthreshold slope characteristics. The biosensor works on the Dielectric-modulation technique. In this technique, a small nanogap is etched below the gate material and above the channel, and this nanogap acts as the site for biomolecules. By placing neutral biomolecules having different K-value, the gate capacitance changes that causes the device features like potential, threshold voltage etc. to change and this change offers a metric to detect the biomolecule type. For charged biomolecules, the charges are considered as fixed

interface oxide charges at the nanogap-channel interface. For most cases, the nanogap is placed over an interfacial layer of silicon dioxide that helps in adhesion of the biomolecules causing their immobilization. Thus, using this technique several device features as well as sensitivity have been also formulated and this has been comprehensively presented in this chapter.

- **Chapter 3** deals with the fixed interface trap charge induced thermal characterization of a Dual-Material Cylindrical Gate-all-around (CGAA) MOSFET having a Gaussian-doped distribution in the channel. CGAA MOSFETs have been the foremost choice of researchers for the device's inherent capability of offering upgraded performances. The device is widely used for practical applications like biosensor. However, this chapter deals with an advanced CGAA MOSFET whose detailed device characteristics have been examined so as to implement the device in practical applications. Moreover, the existing current research exhibits that thermal variations within a range of 100K – 500K have a colossal effect on the inherent characteristics of the silicon channel such as bandgap, intrinsic concentration, Fermi level etc. Below 100K, impurity deionization starts to occur and above 500K, permittivity of silicon dioxide starts to exhibit strong dependence on temperature. Thus, the conducted research demonstrates the temperature-induced effects on electrical characteristics of the proposed device. Also, the Si-SiO_2 interface tends to get damaged due to stress, radiation, hot carrier effects and fabrication process related damages. These damages result in the formation of interface trapped charges (positive/negative), these charges modify the flat-band voltage which consequently modulates the source-channel barrier height thereby affecting the threshold voltage of the device. Thus, the mathematical modeling has been conducted considering the effect of these charges and exhibit comparative studies of device features between the damaged and the undamaged one. Finally, the Gaussian-distribution parameters such as the peak doping, Projected range and straggle parameters have been found to profoundly

impact device characteristics and the same has been highlighted in the current chapter.

♣ Currently Macaroni GAA architectures have surpassed the conventional CGAA architectures in terms of offering upgraded device performance. So, a part of this research encompasses a strategically designed advanced Macaroni-channel GAA MOSFET and its device characteristics have been thoroughly investigated so that the planned device can be explored and implemented to work as an efficient biosensor. Moreover, fixed interface trap charge and temperature-induced effects on the device characteristics of the planned Dual-Material Gate Macaroni channel MOSFET have been exhibited in **chapter 4**. Gate work function engineering (GWFE) incorporation contributes to significant suppression of DIBL, HCE. Another leakage mechanism namely Gate-induced drain leakage (GIDL) drain current has been analyzed and results exhibit GWFE has significantly alleviates GIDL. Graded channel engineering scheme strategically implement evidently allowed suitable selection of threshold voltage. Moreover, comparative studies of the projected device with its Graded channel Dual-Material CGAA counterpart exhibits the superior device performance of the former over the latter.

♣ **Chapter 5** illustrates the mathematical modeling and simulation of a Dual-Material Gate Macaroni channel MOSFET biosensor using dielectric-modulation technique. Full channel Cylindrical Gate-all-around (CGAA) MOSFETs have been the primary choice of researchers as the basic geometry to implement biosensor applications. This is inevitably due to the fact that CGAA MOSFETs have excellent immunity to SCEs, stronger field confinement, high packaging density, lower power consumption due to reduced leakage issues, upgraded subthreshold slope characteristics etc. However, Macaroni MOSFETs have evidently outclassed CGAA MOSFETs in terms of SCE immunization and associated device performance enrichment as also observed in chapter 4. Thus, the research presented in this chapter has illustrated a Dual-Material

Gate Macaroni channel MOSFET Biosensor using dielectric-modulation technique. The Dual-material gate offers SCE resistance and a high-K gate stack has been implemented towards the drain side that contributes to better subthreshold swing characteristics. Detailed sensitivity analysis exhibits that the recommended biosensor offers higher sensitivity to biomolecules (both neutral and charged) compared to its full channel CGAA counterpart.

Results of all mathematical modeling have been validated using simulation results from Atlas, Silvaco.

♣ **Chapter 6** presents the concluding remarks and future scope of the research work.

References

[1.1] S. C. Williams, R. B. Hulfachor, K. W. Kim, M. A. Littlejohn and W. C. Holton, "Scaling trends for device performance and reliability in channel-engineered n-MOSFETs," in IEEE Transactions on Electron Devices, vol. 45, no. 1, pp. 254-260, Jan. 1998, doi: 10.1109/16.658839.

[1.2] Gordon E. Moore, "Cramming more components onto integrated circuits", Electronics, Volume 38, Number 8, April 19, 1965

[1.3] Inderdeep Singh Bhatia, Ashish Raman and Nanhe Lal, "The Shift from Microelectronics to Nanoelectronics – A Review", International Journal of Advanced Research in Computer and Communication Engineering, Vol. 2, Issue 11, November 2013

[1.4] What is Technology Node, https://www.igi-global.com/dictionary/technology-node/44459

[1.5] 1960: Metal Oxide Semiconductor (MOS) Transistor Demonstrated, https://www.computerhistory.org/siliconengine/metal-oxide-semiconductor-mos-transistor-demonstrated/

[1.6] Technology Node, https://en.wikichip.org/wiki/technology_node

[1.7] Ghavam Shahidi, https://en.wikipedia.org/wiki/Ghavam_Shahidi

[1.8] Silicon-on-insulator - SOI technology and ecosystem - Emerging SOI applications by Horacio Mendez, Executive Director of the SOI Industry Consortium, April 9, 2009

[1.9] Narayan Murty Kodeti,"Silicon On Insulator (SOI) Implementation", October 2010, http://www.infotech-enterprises.com/fileadmin/infotech enterprises.com/assets/downloads/White_Papers/Infotech_SOI_Paper_Oct_2010.pdf

[1.10] Krishna Seshan, "Scaling and Its Implications for the Integration and Design of Thin Film and Processes", in Handbook of Thin Film Deposition (Third Edition), 2012

[1.11] Shakti Verma, Mohd. Abdullah. "Review of SOI MOSFET Design and Fabrication Parameters and its Electrical Characteristics", International Journal of Computer Applications (0975 – 8887) Volume 130 – No.17, November 2015

[1.12] D.E. Ioannou ,"Scaling limits and reliability of SOI CMOS technology ", Journal of Physics: Conference Series 10 (2005) 1–6, doi:10.1088/1742-6596/10/1/001

[1.13] P. Kasturi, M. Saxena, M. Gupta and R. S. Gupta, "Dual Material Double-Layer Gate Stack SON MOSFET: A Novel Architecture for Enhanced Analog Performance—Part I: Impact of Gate Metal Workfunction Engineering," in IEEE Transactions on Electron Devices, vol. 55, no. 1, pp. 372-381, Jan. 2008, doi: 10.1109/TED.2007.910564.

[1.14] P. Kasturi, M. Saxena, M. Gupta and R. S. Gupta, "Dual-Material Double-Layer Gate Stack SON MOSFET: A Novel Architecture for Enhanced Analog Performance—Part II: Impact of Gate-Dielectric Material Engineering," in IEEE Transactions on Electron Devices, vol. 55, no. 1, pp. 382-387, Jan. 2008, doi: 10.1109/TED.2007.910567.

[1.15] P. Lakhera, S. Sundriyal and B. Kumar, "Performance analysis of Silicon-On-Nothing MOSFET under 100nm technology nodes," 2016 International Conference on Emerging Trends in Communication Technologies (ETCT), 2016, pp. 1-5, doi: 10.1109/ETCT.2016.7882986.

[1.16] S. K. Gupta, G. G. Pathak, D. Das and C. Sharma, "Double Gate MOSFET and its application for efficient digital circuits," 2011 3rd International Conference on Electronics Computer Technology, 2011, pp. 33-36, doi: 10.1109/ICECTECH.2011.5941650.

[1.17] T. Chiang, "A New Subthreshold Current Model for Junctionless Trigate MOSFETs to Examine Interface-Trapped Charge Effects," in IEEE Transactions on Electron Devices, vol. 62, no. 9, pp. 2745-2750, Sept. 2015, doi: 10.1109/TED.2015.2456040.

[1.18] K. Yılmaz, G. Darbandy, B. Iñíguez, F. Lime and A. Kloes, "Equivalent Length Concept for Compact Modeling of Short-Channel GAA and DG MOSFETs," 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), 2019, pp. 1-4, doi: 10.1109/EUROSOI-ULIS45800.2019.9041912.

[1.19] T. Chiang, "A Novel Quasi-3D Interface-Trapped-Charge-Degraded Threshold Voltage Model for Omega-Gate MOSFETs," in IEEE Transactions on Device and Materials Reliability, vol. 15, no. 1, pp. 35-39, March 2015, doi: 10.1109/TDMR.2014.2371050.

[1.20] T. Chiang, "A New Quasi-3-D Compact Threshold Voltage Model for Pi-Gate (ΠG) MOSFETs With the Interface Trapped Charges," in IEEE Transactions on Nanotechnology, vol. 14, no. 3, pp. 555-560, May 2015, doi: 10.1109/TNANO.2015.2416198.

[1.21] K. Bhol, B. Jena, U. Nanda and S. Tayal, "Work-Function Modulated GAA MOSFET for Improved Electrostatic Controllability in Lower Technology Node," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 270-274, doi: 10.1109/DevIC50843.2021.9455868.

[1.22] M. R. Hasan et al., "Metal Gate Work Function Engineering: Sub-Nano Regime Double Gate MOSFETs," 2019 International Conference on Electrical, Computer and Communication Engineering (ECCE), 2019, pp. 1-5, doi: 10.1109/ECACE.2019.8679134.

[1.23] G. Dhiman and R. Pourush, "Analysis on Variations of Metal Gate Work Function on Junctionless Double Gate MOSFET with High-k Spacers," 2020 International Conference on Emerging Trends in Communication, Control and Computing (ICONC3), 2020, pp. 1-4, doi: 10.1109/ICONC345789.2020.9117425.

[1.24] P. Razavi and A. A. Orouji, "Dual material gate oxide stack symmetric double gate MOSFET: Improving short channel effects of nanoscale double gate MOSFET," 2008 11th International Biennial Baltic Electronics Conference, 2008, pp. 83-86, doi: 10.1109/BEC.2008.4657483.

[1.25] Sanjay, Prasad, B. & Vohra, A. Dual Material Gate Engineering to Reduce DIBL in Cylindrical Gate All Around Si Nanowire MOSFET for 7-nm Gate Length. Semiconductors 54, 1490–1495 (2020). https://doi.org/10.1134/S1063782620110111

[1.26] Strained silicon, https://en.wikipedia.org/wiki/Strained_silicon

[1.27] J. L. Hoyt et al., "Strained silicon MOSFET technology," Digest. International Electron Devices Meeting,, 2002, pp. 23-26, doi: 10.1109/IEDM.2002.1175770.

[1.28] Ferhati, H., Djeffal, F., “Graded channel doping junctionless MOSFET: a potential high performance and low power leakage device for nanoelectronic applications.”, J Comput Electron 17, 129–137 (2018). https://doi.org/10.1007/s10825-017-1052-1

[1.29] Kaur H, Kabra S, Haldar S, Gupta RS, “An analytical drain current model for graded channel cylindrical/surrounding gate MOSFET”, Microelectron J 38(3):352–359, 2007.

[1.30] F. J. Garcia Ruiz, I. M. Tienda-Luna, A. Godoy, L. Donetti and F. Gamiz, "Equivalent Oxide Thickness of Trigate SOI MOSFETs With High- κ Insulators," in IEEE Transactions on Electron Devices, vol. 56, no. 11, pp. 2711-2719, Nov. 2009, doi: 10.1109/TED.2009.2030713.

[1.31] P. Srinivasan, B.P. Linder, V. Narayanan, D. Misra, E. Cartier, "Impact of high-κ and SiO2 interfacial layer thickness on low-frequency (1/f) noise in aggressively scaled metal gate/HfO2 n-MOSFETs: role of high-κ phonons", Microelectronic Engineering, Volume 84, Issues 9–10, 2007, Pages 2274-2277, ISSN 0167-9317, https://doi.org/10.1016/j.mee.2007.04.103.

[1.32] Zhenping Wen et al., "Ultrathin interfacial SiO2 layer process research for high-k gate last gate stacks," 2015 China Semiconductor Technology International Conference, 2015, pp. 1-3, doi: 10.1109/CSTIC.2015.7153410

[1.33] R. Gautam, M. Saxena, R. S. Gupta and M. Gupta, "Numerical Model of Gate-All-Around MOSFET With Vacuum Gate Dielectric for Biomolecule Detection," in IEEE Electron Device Letters, vol. 33, no. 12, pp. 1756-1758, Dec. 2012, doi: 10.1109/LED.2012.2216247.

[1.34] A. Goel, S. Rewari, S. Verma and R. S. Gupta, "Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA)for DNA Bio-Molecule Detection," 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 2018, pp. 337-340, doi: 10.1109/EDKCON.2018.8770406.

[1.35] Neha Goel, "Temperature effects on Threshold Voltage and Mobility for Partially Depleted SOI MOSFET", International Journal of Computer Applications (0975 – 8887) Volume 42– No.21, March 2012

[1.36] M. H. Bhuyan, F. Ferdous and Q. D. M. Khosru, "Temperature effects on subthreshold current of pocket implanted nano scale n-MOSFET," 2012 7th International Conference on Electrical and Computer Engineering, 2012, pp. 686-689, doi: 10.1109/ICECE.2012.6471643.

[1.37] Sze S. Physics of semiconductor devices. Wiley-Interscience; 2007. p. 26–7.

[1.38] Y. S. Yu, N. Cho, S. W. Hwang and D. Ahn, "Analytical Threshold Voltage Model Including Effective Conducting Path Effect (ECPE) for Surrounding-Gate MOSFETs (SGMOSFETs) With Localized Charges," in IEEE Transactions on Electron Devices, vol. 57, no. 11, pp. 3176-3180, Nov. 2010, doi: 10.1109/TED.2010.2066278.

[1.39] Gautam Rajni, Saxena Manoj, Gupta RS, Gupta Mridula, "Two dimensional analytical subthreshold model of nanoscale cylindrical surrounding gate MOSFET including impact of localized charges", J Comput Theoretical Nanosci 2012;9:602–10.

[1.40] Moore's law, https://en.wikipedia.org/wiki/Moore%27s_law

[1.41] Khanna, V.K., "Short-Channel Effects in MOSFETs". In: Integrated Nanoelectronics. NanoScience and Technology. Springer, New Delhi, 2016 https://doi.org/10.1007/978-81-322-3625-2_5

[1.42] A. Gill, C. Madhu and P. Kaur, "Investigation of short channel effects in Bulk MOSFET and SOI FinFET at 20nm node technology," 2015 Annual IEEE India Conference (INDICON), 2015, pp. 1-4, doi: 10.1109/INDICON.2015.7443263.

[1.43] G. Dhiman, A. Routray, S. Singh and G. Singh, "Analysis of Short Channel Effects for Junction Less MOSFET With Metal Gates and High-κ Spacers," 2021 2nd International Conference for Emerging Technology (INCET), 2021, pp. 1-5, doi: 10.1109/INCET51464.2021.9456340.

[1.44] D. Goldhaber-Gordon, M. S. Montemerlo, J. C. Love, G. J. Opiteck and J. C. Ellenbogen, "Overview of nanoelectronic devices," in Proceedings of the IEEE, vol. 85, no. 4, pp. 521-540, April 1997, doi: 10.1109/5.573739.

[1.45] Nazim F. Habbani and Sharief F. Babikir, "Coherence of oscillations generated by single-electronic two-dimensional arrays of tunnel junctions", AIMS Electronics and Electrical Engineering, 4(2): 188–199, DOI: 10.3934/ElectrEng.2020.2.188

[1.46] R. Turton, The Quantum Dot: A Journey into the Future of Microelectronics. Oxford, UK: Oxford Univ. Press, 1995

[1.47] A. C. Seabaugh, J. H. Luscombe, and J. N. Randall, "Quantum functional devices: Present status and future prospects," Future Electron Devices (FED) J., vol. 3, suppl. 1, pp. 9–20, 1993

[1.48] M. A. Kastner, "The single-electron transistor," Rev. Modern Physics, vol. 64, pp. 849–858, 1992

[1.49] W. R. Frensley, "Gallium arsenide transistors," Sci. Amer., pp. 80–87, Feb. 1987.

[1.50] A. Aviram and M. A. Ratner, "Molecular rectifiers," Chem. Phys. Lett., vol. 29, pp. 277–283, 1974

[1.51] J. M. Tour, R. Wu, and J. S. Schumm, "Approaches to orthogonally fused conducting polymers for molecular electronics," J. Amer. Chem. Soc., vol. 112, pp. 5662–5663, 1990

[1.52] J. M. Tour, R. Wu, and J. S. Schumm, "Extended orthogonally fused conducting oligomers for molecular electronic devices," J. Amer. Chem. Soc., vol. 113, pp. 7064–7066, 1991.

[1.53] S. Nespurek and J. Sworakowski, "Electroactive and photochromic molecular materials for wires, switches, and memories," IEEE Eng. Medicine Bio., vol. 13, no. 1, pp. 45–57, 1994.

[1.54] M. Aizawa, "Molecular interfacing for protein molecular devices and neurodevices," IEEE Eng. Medicine Bio., vol. 13, no. 1, pp. 94–102, 1994.

[1.55] C. Joachim and J. Gimzewski, "An electromechanical amplifier using a single molecule," Chem. Phys. Lett., vol. 265, pp. 353–357, 1997

[1.56] Physical Properties of a MOSFET, https://www.norwegiancreations.com/2019/01/physical-properties-of-a-mosfet/

[1.57] Bishop, M.D., Hills, G., Srimani, T. et al., "Fabrication of carbon nanotube field-effect transistors in commercial silicon manufacturing facilities", Nat Electron 3, 492–501 (2020). https://doi.org/10.1038/s41928-020-0419-7

[1.58] Md. Shafayat Hossain, Saeed Uz Zaman Khan, Md. Obaidul Hossen, Fahim Ur Rahman, R. Zaman and Q. D. M. Khosru, "Analytical modeling of potential profile and threshold voltage for rectangular gate-all-around III–V nanowire MOSFETs with ATLAS verification," 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC), 2012, pp. 1-3, doi: 10.1109/EDSSC.2012.6482770.

[1.59] Ian Sinclair,"Active Components and Integrated Circuits", in Electronics Simplified (Third Edition), 2011

[1.60] G. Gildenblat, Z. Zhu, C.C. McAndrew, "Surface potential equation for bulk MOSFET", Solid-State Electron. 53(1), 11–13 (2009).

[1.61] C.T. Sah, "A History of MOS Transistor Compact Modeling", Proc. Tech. WCM 2005, 347–385, 2005.

[1.62] Sung Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata Mc Graw Hill.

[1.63] MOS Capacitor | MOS Capacitance C V Curve, https://www.electrical4u.com/mos-capacitor-mos-capacitance-c-v-curve

[1.64] MOSFET applications, https://en.wikipedia.org/wiki/MOSFET_applications

[1.65] Introduction to MOSFET | Enhancement, Depletion, Amplifier, Applications, https://www.electronicshub.org/mosfet/

[1.66] E. Erben, K. Hempel, and D. Triyoso, "Work Function Setting in High-k Metal Gate Devices", in Complementary Metal Oxide Semiconductor. London, United Kingdom:

IntechOpen, 2018 , https://www.intechopen.com/chapters/61888 doi: 10.5772/intechopen.78335

[1.67] How many Types of MOSFET Transistor?, https://oxscience.com/the-mosfet

[1.68] MOSFET Characteristics (VI And Output Characteristics), https://www.electrical4u.com/mosfet-characteristics/

[1.69] Complementary metal-oxide semiconductor, https://www.britannica.com/technology/complementary-metal-oxide-semiconductor

[1.70] Romana Yousuf , Hakeem Najeeb-ud-Din, "Analysis of charge sharing in MOSFET's in view of available scaling trends", IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 12, Issue 6, Ver. II (Nov.- Dec. 2017), PP 44-52

[1.71] Short-channel effect, https://en.wikipedia.org/wiki/Short-channel_effect

[1.72] R. S. Muller and T. I. Kamins with M. Chan, Device Electronics for Integrated Circuits, 3rd edn., New York: John Wiley & Sons, 2003.

[1.73] Murray, Hugues; Martin, Patrick; Bardy, Serge (2010). Taylor Expansion of Surface Potential in MOSFET: Application to Pao-Sah Integral. Active and Passive Electronic Components, 2010, 1–11. doi:10.1155/2010/268431

[1.74] Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, Lluís F. Marsal, "Two-dimensional analytical threshold voltage roll-off and subthreshold swing models for undoped cylindrical gate all around MOSFET", Solid-State Electronics, Volume 50, Issue 5, 2006, Pages 805-812, ISSN 0038-1101, https://doi.org/10.1016/j.sse.2006.04.020.

[1.75] R. R. Troutman, "VLSI limitation from drain-induced barrier lowering , IEEE Trans. Electron Devices, vol. ED-26, pp. 461–469, April 1979.

[1.76] L. Zhang, L. Li, J. He and M. Chan, "Modeling Short-Channel Effect of Elliptical Gate-All-Around MOSFET by Effective Radius," in IEEE Electron Device Letters, vol. 32, no. 9, pp. 1188-1190, Sept. 2011, doi: 10.1109/LED.2011.2159358.

[1.77] Amit Agarwal, Raushan Tiwari, Shreya Ranjan, P.C. Pradhan and B.P. Swain, "2D Analytical Modeling of Surface Potential for GaAs based Nanowire Gate All Around MOSFET", IOP Conf. Series: Materials Science and Engineering 377 (2018) 012103 doi:10.1088/1757-899X/377/1/012103

[1.78] Ja-Hao Chen, Shyh-Chyi Wong and Yeong-Her Wang, "An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET," in IEEE Transactions on Electron Devices, vol. 48, no. 7, pp. 1400-1405, July 2001, doi: 10.1109/16.930658.

[1.79] C. Galup-Montoro and M. C. Schneider, MOSFET Modeling for Circuit Analysis and Design, Hackensack, NJ: World Scientific, 2007.

[1.80] Veena Misra, Mehmet C. Öztürk, "Field Effect Transistors", in The Electrical Engineering Handbook, 2005

[1.81] Sorin Cristoloveanu,"Emerging devices",in Fully Depleted Silicon-On-insulator, 2021

[1.82] Insaf Lahbib, Aziz Doukkali, Patrick Martin, Guy Imbert, Philippe Descamps, Dominique Defossez, "8 - Simulation of Degradation Phenomena in Semiconductor Components in order to Ensure the Reliability of Integrated Circuits," Editor(s): Abdelkhalak El Hami, David Delaux, Henri Grzeskowiak, Reliability of High-Power Mechatronic Systems 1, Elsevier, 2017, Pages 143-185, ISBN 9781785482601, https://doi.org/10.1016/B978-1-78548-260-1.50008-X.

[1.83] Alberto Castellazzi, York C. Gerstenmaier, Rainer Kraus, and Gerhard K. M. Wachutka, Reliability Analysis and Modeling of Power MOSFETs in the 42-V-PowerNet", IEEE Transactions on Power Electronics, VOL. 21, NO. 3, MAY 2006

[1.84] Lee, Ho Joon; Kim, Kyung Ki (2011). [IEEE 2011 International SoC Design Conference (ISOCC 2011) - Jeju, Korea (South) (2011.11.17-2011.11.18)] 2011 International SoC Design

Conference - Analysis of time dependent dielectric breakdown in nanoscale CMOS circuits. , 440–443. doi:10.1109/isocc.2011.6138626

[1.85] C. Galup-Montoro, M. C. Scheider, A. I. A. Cunha et al., "The advanced compact MOSFET (ACM) model for circuit analysis and design," IEEE Custom Integrated Circuits Conference, Sep. 2007.

[1.86] Channel length modulation, https://en.wikipedia.org/wiki/Channel_length_modulation

[1.87] Henry Radamson, Lars Thylén, "Moore's Law for Photonics and Electronics", in Monolithic Nanoscale Photonics–Electronics Integration in Silicon and Other Group IV Elements, 2015

[1.88] H.R. Huff, "Silicon", in Encyclopedia of Materials: Science and Technology, 2001

[1.89] Y. Taur, "ULSI Scaling Toward 10nm Gate-lengths: Challenges and Opportunities",in Encyclopedia of Materials: Science and Technology, 2001

[1.90] Morin Dehan; Jean-Pierre Raskin, "Dynamic threshold voltage MOS in partially depleted SOI technology: a wide frequency band analysis", 49(1), 67–72, 2005 doi:10.1016/j.sse.2004.07.003

[1.91] Wei, Hui Wai; Ruslan, Siti Hawa (2019). AIP Conference Proceedings [AIP Publishing ADVANCES IN ELECTRICAL AND ELECTRONIC ENGINEERING: FROM THEORY TO APPLICATIONS (SERIES 2): Proceedings of the International Conference of Electrical and Electronic Engineering (ICon3E 2019) - Putrajaya, Malaysia (24–25 June 2019)] Advances In Electrical And Electronic Engineering: From Theory To Applications (SERIES 2): Proceedings of the International Conference of Electrical and Electronic Engineering (ICon3E 2019) - Investigation of FDSOI and PDSOI MOSFET characteristics. , 2173(), 020005–. doi:10.1063/1.5133920

[1.92] Hafez, I.M.; Ghibaudo, G.; Balestra, F., "Analysis of the kink effect in MOS transistors", IEEE Transactions on Electron Devices, 37(3), 818–821, 1990 doi:10.1109/16.47796

[1.93] S. Cristoloveanu, S. Li, Electrical Characterization of SOI Materials and Devices, Kluwer Academic Publishers, 1995

[1.94] M.Current, S.Bebell, I.Malik, L.Feng, F.Henley, "What is the future of sub-100nm CMOS: Ultrashallow junctions or ultrathin SOI?", Solid State Technology, 2000; 43,

[1.95] H. Onishi, K. Imai, H. Nakamura, Y. Matsubara, Y. Yamada, T. Tamura, T. Sakai, T. Horiuchi, "A 5-mask CMOS technology," Symposium VLSI Tech., pp. 33-34, 1997.

[1.96] P. Agarwal, G. Saraswat and M. J. Kumar, "Compact Surface Potential Model for FD SOI MOSFET Considering Substrate Depletion Region," in IEEE Transactions on Electron Devices, vol. 55, no. 3, pp. 789-795, March 2008, doi: 10.1109/TED.2007.914834.

[1.97] Young, K. K. (1989). Short-channel effect in fully depleted SOI MOSFETs. IEEE Transactions on Electron Devices, 36(2), 399–402. doi:10.1109/16.19942

[1.98] G. Zhang, Z. Shao and K. Zhou, "Threshold Voltage Model of Short-Channel FD-SOI MOSFETs With Vertical Gaussian Profile," in IEEE Transactions on Electron Devices, vol. 55, no. 3, pp. 803-809, March 2008, doi: 10.1109/TED.2007.914832.

[1.99] R. Rao, N. Das Gupta and A. Das Gupta, "Study of Random Dopant Fluctuation Effects in FD-SOI MOSFET Using Analytical Threshold Voltage Model," in IEEE Transactions on Device and Materials Reliability, vol. 10, no. 2, pp. 247-253, June 2010, doi: 10.1109/TDMR.2010.2044180.

[1.100] Yong-Bum KwonJong-Hyun Lee, "Method of manufacturing an SOI (silicon on insulator) wafer", US6627519B2, Comtecs Co Ltd, https://patents.google.com/patent/US6627519B2/en

[1.101] Kris V. Srikrishnan, "Smart-cut process for the production of thin semiconductor material films", US5882987A, Soitec SA, https://patents.google.com/patent/US5882987A/en

[1.102] Aakanksha Lakhanpal, Shashi B.Rana, Ashwani K.Rana, "Performance Analysis Of Fdsoi Mosfet For Different Metal Gate Workfunction", International Journal of Engineering Applied Sciences and Technology, 2016, Vol. 1, Issue 8, ISSN No. 2455-2143, Pages 317-322

[1.103] Hui Wai Wei and Siti Hawa Ruslana, "Investigation of FDSOI and PDSOI MOSFET

Characteristics", AIP Conference Proceedings 2173, 020005 (2019); https://doi.org/10.1063/1.5133920

[1.104] Future Outlook: The Advantages of Fully Depleted Silicon on Insulator (FD-SOI) Technology, https://www.coventor.com/blog/future-outlook-the-advantages-of-fully-depleted-silicon-on-insulator-fd-soi-technology/

[1.105] O. Faynot et al., "Advanced SOI technologies: advantages and drawbacks," 2006 International Workshop on Junction Technology, 2006, pp. 200-203, doi: 10.1109/IWJT.2006.220892.

[1.106] T. Hiramoto, T. Nagumo and T. Ohtou, "Low-power device design of fully-depleted SOI MOSFETs," International Semiconductor Device Research Symposium, 2003, 2003, pp. 388-389, doi: 10.1109/ISDRS.2003.1272148.

[1.107] Pavan H Vora, Ronak Lad, "A Review Paper on CMOS, SOI and FinFET Technology",https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html

[1.108] M. Jurczak et al., "Silicon-on-Nothing (SON)-an innovative process for advanced CMOS," in IEEE Transactions on Electron Devices, vol. 47, no. 11, pp. 2179-2187, Nov. 2000, doi: 10.1109/16.877181

[1.109] T. Skotnicki and S. Monfray, "Silicon-on-nothing (SON) technology," 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings, 2006, pp. 11-14, doi: 10.1109/ICSICT.2006.306043.

[1.110] Jurczak, M.; Skotnicki, T.; Paoli, M.; Tormen, B.; Martins, J.; Regolini, J.L.; Dutartre, D.; Ribot, P.; Lenoble, D.; Pantel, R.; Monfray, S. , "Silicon-on-Nothing (SON)-an innovative process for advanced CMOS" , 47(11), 2179–2187, 2000, doi:10.1109/16.877181

[1.111] R. Chauhan, Abhinav, A. Kumar and S. Rai, "A comparative study of junctionless dual material double gate silicon on insulator (SOI) and silicon on nothing (SON) MOSFET," 2017 4th International Conference on Power, Control & Embedded Systems (ICPCES), 2017, pp. 1-7, doi: 10.1109/ICPCES.2017.8117648.

[1.112] T. Poiroux; M. Vinet; O. Faynot; J. Widiez; J. Lolivier; T. Ernst; B. Previtali; S. Deleonibus, "Multiple gate devices: advantages and challenges" , 80, 378–385., 2005, doi:10.1016/j.mee.2005.04.095

[1.113] Ankita Wagadre, Shashank Mane, "Design & Performance Analysis of DG-MOSFET for Reduction of Short Channel Effect over Bulk MOSFET at 20nm", Int. Journal of Engineering Research and Applications, ISSN: 2248-9622, Vol. 4, Issue 7(Version 1), pp.30-34, July 2014

[1.114] Xiaoping Liang; Yuan Taur (2004). A 2-D analytical solution for SCEs in DG MOSFETs. , 51(9), 1385–1391. doi:10.1109/ted.2004.832707

[1.115] Chiang, T K, "A novel scaling-parameter-dependent subthreshold swing model for double-gate (DG) SOI MOSFETs: including effective conducting path effect (ECPE)", Semiconductor Science and Technology, 19(12), 1386–1390, 2004, doi:10.1088/0268-1242/19/12/010

[1.116] Cartwright, J.: "Intel enters the third dimension", Nature (2011). doi:10.1038/news.2011.274.,http://www.nature.com/news/2011/110506/full/news.2011.274.html

[1.117] K.V.Naveen Kumar , T. Bhargav ,T.Sandeep, T.S.R.Prasad, T.Ravi, "New Generation Transistors", International Journal of Engineering Research & Technology (IJERT) Vol. 1 Issue 9, November- 2012, ISSN: 2278-0181

[1.118] Tsormpatzoglou, A., Dimitriadis, C. A., Clerc, R., Pananakakis, G., & Ghibaudo, G. "Semianalytical Modeling of Short-Channel Effects in Lightly Doped Silicon Trigate

MOSFETs", IEEE Transactions on Electron Devices, 55(10), 2623–2631, 2008 doi:10.1109/ted.2008.2003096

[1.119] Ghanatian, H., & Hosseini, S. E., "Analytical modeling of subthreshold swing in undoped trigate SOI MOSFETs", Journal of Computational Electronics, 15(2), 508–515, 2016, doi:10.1007/s10825-016-0817-2

[1.120] A. Aouaj, A. Bouziane and A. Nouaçry, "Dual material gate-graded channel-gate stack (DMG-GC-Stack) surrounding gate MOSFET: Analytical threshold voltage (VTH) and subthreshold swing (S) models," 2011 International Conference on Multimedia Computing and Systems, 2011, pp. 1-4, doi: 10.1109/ICMCS.2011.5945711.

[1.121] D. Sharma and S. K. Vishvakarma, "Precise Analytical Model for Short-Channel Quadruple-Gate Gate-All-Around MOSFET," in IEEE Transactions on Nanotechnology, vol. 12, no. 3, pp. 378-385, May 2013, doi: 10.1109/TNANO.2013.2251895.

[1.122] S. Gupta, N. Pandey and R. S. Gupta, "Investigation of Dual-Material Double Gate Junctionless Accumulation-Mode Cylindrical Gate All Around (DMDG-JLAM-CGAA) MOSFET with High-k Gate Stack for low Power Digital Applications," 2020 IEEE 17th India Council International Conference (INDICON), 2020, pp. 1-4, doi: 10.1109/INDICON49873.2020.9342380

[1.123] Santanu Sharma , Kabita Chaudhury, "A Novel Technique for Suppression of Corner Effect in Square Gate All Around MOSFET", Electrical and Electronic Engineering, p-ISSN: 2162-9455, e-ISSN: 2162-8459, 2012; 2(5): 336-341, doi: 10.5923/j.eee.20120205.14

[1.124] Abdi M A, Djeffal F, Dibi Z and Arar D, "A two dimensional analytical Subthreshold behavior analysis including hot-carrier effect for nanoscale gate stack gate all around (GASGAA) MOSFETs", J Comput Electron, 10, 179–85, 2011.

[1.125] Q. Nguyen-Gia, M. Kang, J. Jeon and H. Shin, "Characteristic Length of Macaroni Channel MOSFET," in IEEE Electron Device Letters, vol. 40, no. 11, pp. 1720-1723, Nov. 2019, doi: 10.1109/LED.2019.2942619.

[1.126] Darwin, S., & Samuel, T. S. A., "Mathematical Modeling of Junctionless Triple Material Double Gate MOSFET for Low Power Applications", Journal of Nano Research, 56, 71–79, 2018.

[1.127] G. V. Reddy and M. J. Kumar, "A new dual-material double-gate (DMDG) nanoscale SOI MOSFET-two-dimensional analytical modeling and simulation," in IEEE Transactions on Nanotechnology, vol. 4, no. 2, pp. 260-268, March 2005, doi: 10.1109/TNANO.2004.837845.

[1.128] Chattopadhyay, A., Dutta, A., Kundu, A., & Sarkar, C. K. , "Influence on the analog/RF performance in graded channel Gate Stack DG-MOSFETs", 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS). doi:10.1109/icdcsyst.2016.7570653

[1.129] Gupta, C., Agarwal, H., Dey, S., Hu, C., & Chauhan, Y. S., "Analysis and modeling of capacitances in halo-implanted MOSFETs", 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM). doi:10.1109/edtm.2017.7947563

[1.130] Sharma, R., Rana, A. K., Kaushal, S., King, J. B., & Raman, A., "Analysis of Underlap Strained Silicon on Insulator MOSFET for Accurate and Compact Modeling", Silicon. doi:10.1007/s12633-021-01059-7

[1.131] Das, S. K., Nanda, U., Biswal, S. M., Pandey, C. K., & Giri, L. I. , "Performance Analysis of Gate-Stack Dual-Material DG MOSFET Using Work-Function Modulation Technique for Lower Technology Nodes", Silicon, 2021, doi:10.1007/s12633-021-01095-3

[1.132] Padmanaban, B., Ramesh, R., Nirmal, D., Sathiyamoorthy, S., "Numerical modeling of triple material gate stack gate all-around (TMGSGAA) MOSFET considering quantum mechanical effects", Superlattices Microstruct. 82, 40–54 (2015)

[1.133] Koley K, Dutta A, Saha SK, Sarkar CK, "Analysis of high- K spacer asymmetric Underlap DG-MOSFET for SOC application", IEEE Trans Electron Dev 62(6):1733–1738, 2015

[1.134] Pratap, Y., Kumar, M., Kabra, S., Haldar, S., Gupta, R. S., & Gupta, M., "Analytical modeling of gate-all-around junctionless transistor based biosensors for detection of neutral

biomolecule species", Journal of Computational Electronics, 17(1), 288–296, 2017. doi:10.1007/s10825-017-1041-4

[1.135] Kranti, A., Haldar, S., & Gupta, R. S., "Temperature-dependent threshold voltage analysis of surrounding/cylindrical gate fully depleted thin film SOI MOSFET in the range 77 to 520 K", Microelectronic Engineering, 49(3-4), 273–286, 1999, doi:10.1016/s0167-9317(99)00446-3

[1.136] Sze S. Physics of semiconductor devices. Wiley-Interscience; 2007. p. 26–7.

[1.137] Wong, H., Yu, Q., Dong, S., Kakushima, K., & Iwai, H. (2017). Geometry and temperature effects on the threshold voltage characteristics of silicon nanowire MOS transistors. Solid-State Electronics, 138, 35–39. doi:10.1016/j.sse.2017.07.005

[1.138] Suddapalli, S. R., & Nistala, B. R., "A center-potential-based threshold voltage model for a graded-channel dual-material double-gate strained-Si MOSFET with interface charges", Journal of Computational Electronics, 2019, doi:10.1007/s10825-019-01377-5

[1.139] Chiang Te-Kuang., "A New Interface-Trapped-Charge-Degraded Subthreshold Current Model for Quadruple-Gate MOSFETs", IEEE Transactions on Electron Devices, 61(5), 1611–1614, 2014, doi:10.1109/ted.2014.2312936

[1.140] T. Chiang, "A Novel Quasi-3D Interface-Trapped-Charge-Degraded Threshold Voltage Model for Omega-Gate MOSFETs," in IEEE Transactions on Device and Materials Reliability, vol. 15, no. 1, pp. 35-39, March 2015, doi: 10.1109/TDMR.2014.2371050.

Chapter 2

Chapter 2: GWFE Trigate MOSFET with a Dual-Material Bottom Gate for Biosensing Applications: A Dielectric-Modulation based Approach

---

2.1. Introduction

The transition from bulk, conventional single gate MOSFET to the pioneering technology of Double-Gate MOSFET has proved to be significantly appreciating in terms of short channel effect immunity, better electrostatic control, improved scalability, reduced off-state leakages etc. [2.1]. DG MOSFETs are fabrication feasible and the detailed step by step fabrication process is provided in US patent US6855588B1 [2.2]. In spite of offering advanced device performance, Double gate structures still suffer from some major fabrication related complexities [2.3]. Hence, to overcome major barriers associated with Double Gate architecture and to add significant boost to the device performance, Trigate devices have been introduced with the aim to support further scalability in continuation with the Moore's law. It has been reported that Trigate devices enhance speed of operation by 37% and lower the power consumption by 50% compared to the planar architecture MOSFETs.

Trigate (or Triple Gate) MOSFETs are first introduced by Intel along with detailed fabrication steps claimed in US patent US20040094807A1 [2.4]. The device with an insulating film beneath the channel consists of a semiconductor body on the insulating film (SOI/SON) having top surface and laterally opposite sidewalls formed on a substrate. The gate dielectric layer is then deposited on the top surface and on the top of the laterally opposite sidewalls. The gate electrode is then deposited over this gate dielectric and this is followed by formation of source/drain extensions. This, in short, provides the idea of the Trigate MOSFET fabrication.

The Dual-Material gate, a technique of Gate Work Function Engineering (GWFE), can be formed by following fabrication steps detailed in US patent US6972224B2 [2.5]. The first step comprises of considering a semiconductor substrate having a surface area with a first area and the second area. This is followed by formation of gate dielectric on the surface of the first area and the second area. Then a sacrificial layer of SiO_2 is formed over the gate dielectric. The sacrificial layer is then patterned so that the gate dielectric on first area is exposed and rest of the gate-dielectric over the second area is protected. This is followed by deposition of first metal gate conductor over the exposed dielectric and also on the

remaining portion of the sacrificial layer. This is then followed by dry etching of the first metal gate conductor from the top of the sacrificial layer on the second area and exposing the remaining portion of the sacrificial layer. The remaining portion of the sacrificial layer is then removed using a wet chemical etch thereby exposing the gate dielectric over the second area. Finally, the second metal gate conductor material is deposited on the gate dielectric on the second area thereby resulting in the structure of Dual-Metal Gate. Thus, GWFE comprising of Dual-Material Gate is highly fabrication feasible.

Thus, Trigate (3D) MOSFETs are revolutionary invention since the device allows excellent SCE immunity, higher packaging density, higher speed and significantly lower power consumption compared to the 2-D MOSFETs. Incorporation of GWFE and a Dual-Material Bottom gate can provide a further boost to the overall device performance.

Considering the advantages coupled with fabrication feasibility, a Dual-Material Trigate MOSFET with a Dual-Material bottom gate has been considered as the basic device to work as an effective biosensor.

Thus, performance escalation of aggressively scaled MOSFET devices has been made possible to a great extent by incorporating the ground-breaking technology of Trigate architecture, where the employed gates play pivotal role in enhancing the electrostatic control over the channel. Improved gate-channel coupling effectively reduces major short channel effects (SCEs) since the channel area covered by the gates through the gate-oxide increases to a large extent.

Apart from the Multi-gate and GWFE scheme, researchers have introduced innovative schemes for refinements or rectifications of some targeted SCEs and to selectively boost specific device characteristics. One such popular scheme namely the dielectric engineering scheme has successfully achieved to gain the attention of researchers owing to the scheme's noteworthy advantages and its incorporation for rectification of some targeted SCEs and selective refinement of some of the device features. Dielectric engineering can be of two configurations: (a) high-K gate stack configuration (b) lateral hetero-dielectric configuration. As the device channel length has been aggressively scaled down to achieve miniaturization, the gate-oxide thickness needs to be scaled down at the same pace.

However, oxides like SiO_2 when scaled down to below 2nm, the hot electrons that gain the high kinetic energy from the substantially high electric fields, tend to tunnel the oxide causing oxide breakdown [2.6]. This causes high power consumption and degraded device reliability. Thus SiO_2 needs to be replaced by some high-K oxide that enhances gate capacitance thereby permitting better gate control. In most cases, an interfacial layer of SiO_2 is grown first (to reduce phonon scattering) and then the high-K oxide is placed over this SiO_2 layer [2.7]. This configuration of two gate-oxides placed one above the other is called high-K gate stack configuration which is highly favorable to reduce subthreshold swing, DIBL in short channel MOSFET devices [2.8]. (b) Lateral hetero-dielectric configuration in MOSFET is mainly used where the MOSFET device is employed to work as a biosensor [2.9]. In this configuration, the region beneath the gate and above the channel and towards the source is etched to form a nanogap where biomolecules of different K-value is placed [2.10]. Laterally, beside the nanogap, towards the drain, the gate-oxide is grown filling the region beneath the gate and above the channel. In most cases, the nanogap and the drain-side gate-oxide (normally a high-K gate oxide) is placed above a layer of SiO_2. Thus the gate capacitance towards the source is different than that near the drain. Now, by placing biomolecules with different K-values in the nanogap, the gate capacitance is varied that impacts the device potential, threshold voltage, drain current etc. which then provides a metric for efficient detection of the biomolecules [2.11-2.13]. Now, considering the advantages offered by the above two types of gate-oxide configuration, these technologies have been tactfully incorporated in a Dual-Material Trigate SOI MOSFET with a Dual-Material bottom gate that has also been discussed expansively in the following section.

2.2. Overview

The strategy of dielectric engineering has been widely explored for its implementation as a biosensing property in advanced MOSFET devices. However, employment of dielectric engineering in this case of research is somewhat different from the high-K gate stack technology. In the high-K gate stack system, the high-K is placed over an SiO_2 layer forming

stack like configuration. Whereas, when dielectric engineering is employed for biosensing property, the dielectrics are placed side by side, rather than one above another [2.14].

High-K gate stack systems are fabrication feasible. Ling Et al. [2.15] mentioned the detailed step by step fabrication of a high-K gate stack system on a p-type substrate. Firstly, the substrate is RCA cleaned and then a field oxide (SiO_2) is grown thermally. Then high-K oxide is deposited using ALD. After the high-K oxide is deposited, annealing is used to improve the electrical property of the high-K thin film. After this, metal gate is deposited and patterned. Finally gas annealing is done for interface states passivation. Finally source/drain ion implantation and dopant activation annealing are done.

The operation of a MOSFET biosensor works on the principle of change of device features due to a change in the gate capacitance due to an alteration in K-value of biomolecule placed in a nanogap in place of a fixed gate-oxide, the method is widely popular and is termed as dielectric-modulation technique [2.16]. Thus the gate-oxide configuration of the MOSFET biosensor is different here. A small region under the gate and above the channel is etched and this region acts as the site for placing the biomolecules. This region is called the nanogap [2.17]. When the biomolecule having a certain K-value is placed in the nanogap, the gate capacitance has a certain value, which changes if another biomolecule having another K-value is now placed in the nanogap. In simulation, presence of neutral biomolecules is realized by introducing a material having dielectric constant similar to that of the biomolecule (for eg: K-value of biomolecule streptavidin is 2.1, that of protein is 2.50, biotin has K=2.63, APTES has K=3.57, Keratin has K=5-10 and so on). For charged biomolecule having a certain K-value, the material having that K-value is placed in the nanogap and the charge is considered as fixed interface trap charges at the SiO_2-Air interface [2.18].

Beside this nanogap, there is another high-K oxide that fills the rest of the region between the channel and the gate. Thus, here the nanogap containing a certain biomolecule having a fixed K-value and another high-K oxide is placed side by side. Sometimes, both the nanogap and the high-K oxide is placed over a very thin layer of SiO_2. This layer of SiO_2 acts as adhesion for biomolecules and it serves as the interfacial layer for the high-K oxide thus forming a high-K gate stack [2.19-2.20]. The fabrication feasibility of

the nanogap region has been mentioned by Kim et al. [2.21]. Following the fabrication steps mentioned in this published research, after the channel, source and drain extensions for the Trigate structure are grown using photolithography and ion implantation, for the current (our) research, TiO_2 (only for region 2), SiO_2, Cr and gate metals are to be subsequently grown and deposited using the thin film processes. SiO_2 forms the gate dielectric/adhesion layer in region 1, Cr is the sacrificial layer that leaves the nanogap after selective wet etching. After the above three layers (for region with first gate material, and four layers for region with second gate material) are deposited, they are patterned by photolithography and subsequent etching processes. The nanogap is now formed by lateral wet etching of Cr.

Thus, fabrication feasibility of the nanogap coupled with exploration of dielectric engineering scheme for biosensing property are the prime motivations behind the mathematical modeling and simulation of a GWFE incorporated Trigate biosensor with a dual-material bottom gate that has been discussed in detail as follows.

2.3. Analytical Modeling

Fig.2.1. presents the 3-D schematic representation of a Dual-Material (DM) (GWFE incorporated) Trigate MOSFET with a Dual-Material bottom gate to act as an effective biosensor.

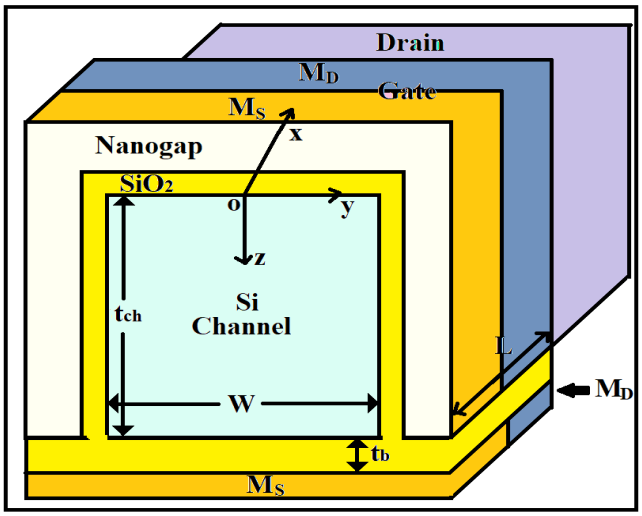


Fig.2.1. 3-D Schematic illustration of the proposed biosensor

The Dual-Material gate is made up of two materials namely M_S (having work function $\phi_{M_S} = 5.35eV$ and gate length L_1=30nm) placed towards the source and M_D (having work function $\phi_{M_D} = 4.4eV$ and gate length L_2=30nm) placed towards the drain. The channel has a uniform concentration of $N_{ch}=10^{17}cm^{-3}$ and channel length is L=60nm.

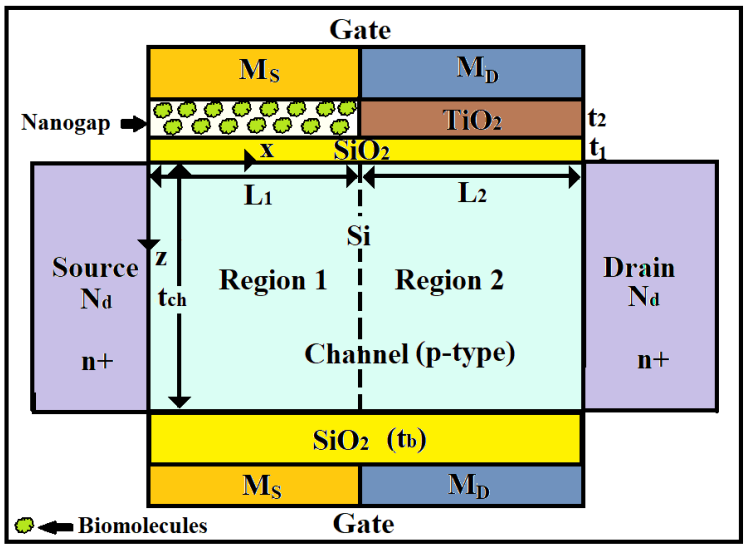


Fig.2.2. 2-D Cross-sectional view of the proposed biosensor

The gate-oxide under M_D is TiO_2 (K=40) placed over an interfacial SiO_2 layer. The gate-oxide under M_S comprises of a nanogap (that acts as the site of biomolecules) placed over a layer of SiO_2 that acts as adhesion for the biomolecules. The channel is placed over a layer of SiO_2 having thickness (t_b) of 2nm. Thickness of the nanogap is denoted as t_{bio}=11nm, thickness of TiO_2 layer is t_2=11nm and thickness of interfacial SiO_2 layer is t_1=1nm. Channel thickness is t_{ch}=10nm. Width of the trigate device is w=5nm. The 2-D cross-sectional view of the proposed biosensor is presented in Fig.2.2.

2.3.1. Surface Potential Modeling

In order to investigate the electrical characteristics of the proposed biosensor, the expression for surface potential of the device needs to be obtained. For this, the 3-D Poisson's equation needs to be solved as follows [2.22]

$$\frac{\partial^2 \varphi_i(x,y,z)}{\partial x^2}+\frac{\partial^2 \varphi_i(x,y,z)}{\partial y^2}+\frac{\partial^2 \varphi_i(x,y,z)}{\partial z^2}=\frac{qN_{ch}}{\varepsilon_{Si}} \tag{2.1}$$

Here i stands for the i[th] region. For the ease of calculation, the channel region is divided into two parts: i=1 for region 1 with boundaries $0 \le x \le L_1, -\frac{w}{2} \le y \le \frac{w}{2}, 0 \le z \le t_{ch}$ and i=2 for region 2 with boundaries $L_1 \le x \le L_1 + L_2 (= L), -\frac{w}{2} \le y \le \frac{w}{2}, 0 \le z \le t_{ch}$. $\varphi_i(x,y,z)$ is the potential for the i[th] region.

Potential distribution between the side-walls is assumed to be parabolic which mathematically leads to

$$\varphi_i(x,y,z) \approx c_{i0}(x,z) + c_{i1}(x,z)\,y + c_{i2}(x,z)\,y^2 \tag{2.2}$$

For low drain voltages, potential distribution is parabolic in the z-direction. At y=0, the expression obtained for potential is [2.23]:

$$\varphi_i(x,0,z) = c_{i0}(x,z) \approx \varphi_{spi}(x) + k_{i1}(x)\,z + k_{i2}(x)\,z^2 \tag{2.3}$$

At the front and lateral interfaces, potential which is actually the surface potential is given using the following expression:

$$\varphi_i(x,0,0) = c_{i0}(x,0) = \varphi_{spi}(x) \tag{2.4}$$

Potential at the back channel-oxide (SiO_2) interface is given as:

$$\varphi_i(x,0,t_{ch}) = c_{i0}(x,t_{ch}) \approx \varphi_{spi}(x) + k_{i1}(x)\,t_{ch} + k_{i2}(x)\,t_{ch}^{\,2} = \varphi_{sbi}(x) \tag{2.5}$$

Symmetry along the y-direction leads to:

$$\varphi_i\left(x,-\frac{w}{2},z\right) = \varphi_i\left(x,+\frac{w}{2},z\right) \tag{2.6}$$

Solution of the above equation mathematically leads to:

$$c_{i1}(x,z) = 0 \tag{2.7}$$

Therefore, using equation (2.2) and equation (2.7), the following expression of potential is obtained:

$$\varphi_i\left(x,\pm\frac{w}{2},z\right)=c_{i0}(x,z)+c_{i2}(x,z)\frac{w^2}{4}=\varphi_{spi}(x) \tag{2.8}$$

Hence, $c_{i2}(x,z)=\frac{4}{w^2}\left[\varphi_{spi}(x)-c_{i0}(x,z)\right]$ (2.9)

The boundary conditions required to evaluate the coefficients in equation (2.3) are listed as follows [2.24]:

In Region 1, the coefficients obtained are:

$$k_{11}(x)=\left.\frac{d\varphi_1}{dz}\right|_{y=0,z=0}=\frac{\varepsilon_{ox_1}}{\varepsilon_{Si}t_{g_{eff}}}\left[\varphi_{sp1}(x)-V_{gs1}{}'\right] \tag{2.10}$$

$$\left.\frac{d\varphi_1}{dz}\right|_{y=0,z=t_{ch}}=\frac{\varepsilon_b}{\varepsilon_{Si}t_b}\left[V_{gs1}{}''-\varphi_{sb1}(x)\right] \tag{2.11}$$

Here, $\varepsilon_{ox_1}=\varepsilon_b$

Using the boundary condition in equation (2.11), another coefficient for region 1 thus obtained is as follows:

$$k_{12}(x)=\frac{V_{gs1}{}''-\varphi_{sp1}(x)\left(1+\frac{C_{eff}}{C_{Si}}+\frac{C_{eff}}{C_b}\right)+V_{gs1}{}'\left(\frac{C_{eff}}{C_{Si}}+\frac{C_{eff}}{C_b}\right)}{t_{ch}{}^2\left(1+\frac{2C_{Si}}{C_b}\right)} \tag{2.12}$$

In Region 2, the coefficients obtained are:

$$k_{21}(x)=\left.\frac{d\varphi_2}{dz}\right|_{y=0,z=0}=\frac{\varepsilon_{ox_1}}{\varepsilon_{Si}t_{eff}}\left[\varphi_{sp2}(x)-V_{gs2}{}'\right] \tag{2.13}$$

$$\left.\frac{d\varphi_2}{dz}\right|_{y=0,z=t_{ch}}=\frac{\varepsilon_b}{\varepsilon_{Si}t_b}\left[V_{gs2}{}'-\varphi_{sb2}(x)\right] \tag{2.14}$$

Equation (2.14) mathematically leads to

$$k_{22}(x)=\frac{\left[V_{gs2}{}'-\varphi_{sp2}(x)\right]\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_b}\right]}{t_{ch}{}^2\left(1+\frac{2C_{Si}}{C_b}\right)} \tag{2.15}$$

Where, $V_{gs1}{}' = V_{gs} - V_{FBf_1}{}'$, $V_{FBf_1}{}' = V_{FB_1} - \frac{qN_f}{C_{eff}}$, in region 1 the front channel-oxide flat-band voltage is given as $V_{FB_1} = \phi_{M_S} - \phi_{Si}$, the density of the charged biomolecules is given as N_f, the effective oxide capacitance comprising the nanogap dielectric and the interfacial SiO_2 (ε_{ox_1}) layer is denoted as C_{eff} and is given by:

$C_{eff} = \frac{\varepsilon_{ox_1}}{t_{g_{eff}}}$, Where effective oxide thickness (EOT) under gate M_S, $t_{g_{eff}} = t_1 + t_{bio}\frac{\varepsilon_{ox_1}}{\varepsilon_{bio}}$, $C_b = \frac{\varepsilon_b}{t_b}$,

$C_{ox} = \frac{\varepsilon_{ox_1}}{t_{eff}}$, Where effective oxide thickness (EOT) under gate M_D, $t_{eff} = t_1 + t_2\frac{\varepsilon_{ox_1}}{\varepsilon_{TiO_2}}$ and

$V_{gs1}{}'' = V_{gs} - V_{FBb_1}$ where $V_{FBb_1} = V_{FB_1}$, $V_{gs2}{}' = V_{gs} - V_{FB_2}$, $V_{FB_2} = \phi_{M_D} - \phi_{Si}$

Thus, using equations (2.10) and (2.12) in equation (2.2) and (2.3), the expression of potential in region 1 is given as follows:

$$\varphi_1(x,y,z) = A_1\varphi_{sp1}(x) + B_1V_{gs1}{}' + C_1V_{gs1}{}'' \tag{2.16}$$

Where, $A_1 = 1 + K_1z - K_2z^2 - K_3zy^2 + K_4z^2y^2$, $B_1 = -K_5z + K_6z^2 + K_7zy^2 - K_8z^2y^2$,

$C_1 = \frac{z^2}{K} - \frac{4}{w^2}\frac{z^2}{K}y^2$. Here, $K = t_{ch}{}^2\left(1 + \frac{2C_{Si}}{C_b}\right)$, $K_1 = \frac{\varepsilon_{ox_1}}{\varepsilon_{Si}t_{g_{eff}}}$, $K_2 = \frac{1 + \frac{C_{eff}}{C_{Si}} + \frac{C_{eff}}{C_b}}{K}$, $K_3 = \frac{4}{w^2}K_1$,

$K_4 = \frac{4}{w^2}K_2$, $K_5 = K_1$, $K_6 = \frac{\frac{C_{eff}}{C_{Si}} + \frac{C_{eff}}{C_b}}{K}$, $K_7 = \frac{4}{w^2}K_1$, $K_8 = \frac{4}{w^2}K_6$

Similarly using equation (2.13) and (2.15) in equation (2.2) and (2.3), expression for potential obtained for region 2 is given as follows:

$$\varphi_2(x,y,z) = A_2\varphi_{sp1}(x) + B_2V_{gs2}{}' \tag{2.17}$$

Here, $A_2 = 1 + K_1'z - K_2'z^2 - K_3'zy^2 + K_4'z^2y^2$, $B_2 = -K_5'z + K_6'z^2 + K_7'zy^2 - K_8'z^2y^2$, where

$K_1' = \frac{\varepsilon_{ox_1}}{\varepsilon_{Si}t_{eff}}$, $K_2' = \frac{1 + \frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_b}}{K}$, $K_3' = \frac{4}{w^2}K_1'$, $K_4' = \frac{4}{w^2}K_2'$, $K_5' = K_1'$, $K_6' = K_2'$, $K_7' = \frac{4}{w^2}K_1'$,

$K_8' = \frac{4}{w^2}K_6'$

Substituting equation (2.16) in equation (2.1), the differential equation for region 1 thus obtained is given as:

$$\frac{d^2\varphi_{sp_1}(x)}{dx^2} - \gamma_1\varphi_{sp_1}(x) = \theta_1 \tag{2.18}$$

Here, $\gamma_1 = \frac{2K_2 + 2K_3z - 2K_4z^2 - 2K_4y^2}{A_1}$, $\theta_1 = \frac{qN_{ch}}{A_1\varepsilon_{Si}} + \frac{V_{gs1}'\left(-2K_6 - 2K_7z + 2K_8z^2 + 2K_8y^2\right)}{A_1} + \frac{V_{gs1}''}{A_1}\left(\frac{8z^2}{w^2} + \frac{8y^2}{w^2} - 2\right)$

Substituting equation (2.17) in equation (2.1), the differential equation for region 2 thus obtained is given as:

$$\frac{d^2\varphi_{sp_2}(x)}{dx^2} - \gamma_2\varphi_{sp_2}(x) = \theta_2 \tag{2.19}$$

Here, $\gamma_2 = \frac{2K_2' + 2K_3'z - 2K_4'z^2 - 2K_4'y^2}{A_2}$, $\theta_2 = \frac{qN_{ch}}{A_2\varepsilon_{Si}} + \frac{V_{gs2}'\left(-2K_6' - 2K_7'z + 2K_8'z^2 + 2K_8'y^2\right)}{A_2}$

The general solution to equation (2.18) and equation (2.19) are respectively given as follows [2.25-2.26]:

In Region 1: $\varphi_{sp_1}(x) = P_Ie^{\delta_1 x} + Q_Ie^{-\delta_1 x} - \omega_1$ (2.20)

Where, $\delta_1 = \sqrt{\gamma_1}$, $\omega_1 = \frac{\theta_1}{\gamma_1}$

In Region 2: $\varphi_{sp_2}(x) = P_{II}e^{\delta_2(x-L_1)} + Q_{II}e^{-\delta_2(x-L_1)} - \omega_2$ (2.21)

Where, $\delta_2 = \sqrt{\gamma_2}$, $\omega_2 = \frac{\theta_2}{\gamma_2}$

In order to find the coefficients P_I, Q_I, P_{II} and Q_{II}, the following boundary conditions need to be satisfied [2.27]

Continuity of surface potential at the interface of the two dissimilar materials leads to:

$$\varphi_{sp_1}(x)\Big|_{x=L_1} = \varphi_{sp_2}(x)\Big|_{x=L_1} \tag{2.22}$$

Continuity of electric flux at the interface of the two dissimilar materials leads to:

$$\frac{d\varphi_{sp_1}(x)}{dx}\Bigg|_{x=L_1} = \frac{d\varphi_{sp_2}(x)}{dx}\Bigg|_{x=L_1} \tag{2.23}$$

At source-channel end, potential is given by:

$$\varphi_{sp1}(0) = V_{Bi} \tag{2.24}$$

At drain-channel end, potential is given by:

$$\varphi_{sp2}(L) = V_{Bi} + V_{ds} \tag{2.25}$$

V_{Bi} is the built-in potential.

The expressions of coefficients in equations (2.20) and (2.21) thus obtained using the above listed boundary conditions are listed as follows:

$$Q_{II} = \frac{bP_I e^{\delta_1 L_1} + aQ_I e^{-\delta_1 L_1} - \omega_{12}}{2}, \qquad P_{II} = \frac{aP_I e^{\delta_1 L_1} + bQ_I e^{-\delta_1 L_1} - \omega_{12}}{2}, \qquad P_I = V_{Bi} + \omega_1 - Q_I \qquad \text{and}$$

$$Q_I = \frac{(V_{Bi} + \omega_1)(ae^c + be^d) - 2(V_{Bi} + V_{ds} + \omega_2) - 2\omega_{12}\cosh\delta_2 L_2}{2(a\sinh c + b\sinh d)}$$

Here, $a = 1+\delta_{12}, b = 1-\delta_{12}$, $c = \delta_1 L_1 + \delta_2 L_2$, $d = \delta_1 L_1 - \delta_2 L_2$

2.3.2. Threshold Voltage Modeling

The gate voltage at which the minimum surface potential is twice the Fermi potential is termed as the threshold voltage [2.28]. To obtain the minimum surface potential, the position of minimum surface potential needs to be determined. Surface potential minimum for all cases, except for the case N_f=0, K=1, occurs in region 1, hence the position of minimum surface potential can be obtained as follows:

$$\frac{\partial\phi_{sp_1}(x)}{\partial x}\Bigg|_{x=x_{MIN}} = 0 \tag{2.26}$$

Hence the position of minimum surface potential thus obtained is as follows:

$$x_{MIN} = \frac{1}{2\delta_1} \ln \frac{Q_I}{P_I} \tag{2.27}$$

Thus the threshold voltage for all the cases except for N_f=0, K=1 can be obtained using the following equation:

$$\varphi_{sp_1}\left(x_{MIN}\right) = 2\varphi_F \tag{2.28}$$

For N_f=0, K=1, surface potential minimum occurs in region 2 and thus the position of minimum surface can be obtained using the following equation as follows:

$$\left.\frac{\partial \phi_{sp_2}\left(x\right)}{\partial x}\right|_{x=x_{MIN}} = 0 \tag{2.29}$$

The position of minimum surface potential thus obtained is as follows:

$$x_{MIN} = \frac{1}{2\delta_2} \ln \frac{Q_{II}}{P_{II}} + L_1 \tag{2.30}$$

Threshold voltage, in this case, can be obtained using the following equation:

$$\varphi_{sp_2}\left(x_{MIN}\right) = 2\varphi_F \tag{2.31}$$

2.3.3. Short Channel Effect Modeling

- DIBL (mV) [2.29] is given as follows:

$$DIBL = V_{thr,lin} - V_{thr,sat} \tag{2.32}$$

Where, $V_{thr,lin}$ and $V_{thr,sat}$ are respectively threshold voltages in linear and saturation regions.

- Subthreshold swing (SS in mV/dec) [2.30] is given as follows:

$$SS = 2.3V_t \left[\left. \frac{d\varphi_{sp}\left(x\right)}{dV_{gs}} \right|_{x=x_{MIN}} \right]^{-1} \tag{2.33}$$

Hot carrier effect (HCE) can be analyzed from the lateral electric field distribution of the proposed device. Lateral electric field can be obtained using the following expression [2.31]:

$$E_x = -\frac{d\varphi_{sp}\left(x\right)}{dx} \tag{2.34}$$

2.3.4. Sensitivity Analysis

Sensitivity for neutral biomolecules is given as follows:

$$S_{N_{Bio}} = \left| \frac{V_{thr}(K=1) - V_{thr}(K>1)}{V_{thr}(K=1)} \right| \tag{2.35}$$

Sensitivity for charged biomolecules is given as follows:

$$S_{C_{Bio}} = \left| \frac{V_{thr}(Bio_{neutral}) - V_{thr}(Bio_{charged})}{V_{thr}(Bio_{neutral})} \right| \tag{2.36}$$

2.4. Results & Discussions

Verification of analytical results has been carried out using simulation outputs from Silvaco Atlas. Fig. 2.3 demonstrates the surface potential distribution along the channel for different types of neutral biomolecules placed in the nanogap. When the nanogap has no biomolecule present in it, that is, when the nanogap is filled with air, the surface potential minimum (which occurs in region 2) attains the highest value, the source-channel barrier height is greatly reduced that leads to lowest value of threshold voltage for N_f=0, K=1. This can be clearly understood if the physics concerned can be explained. When the nanogap is filled with air, the effective oxide thickness (EOT) under gate M_S increases that, in turn, reduces the gate-control over the channel leading to reduced threshold voltage. Whereas when the nanogap is filled with biomolecule (K>1), the effective oxide thickness decreases leading to enhanced gate-control over the channel. Source-channel barrier height increases compared to the case K=1, this leads to increased threshold voltage which also prevent leakages in the proposed device. Thus as the K-value in the nanogap increases, gate-channel coupling increases, source-channel barrier height increases gradually leading to enhanced threshold voltages at higher K. Also, for K=1, proposed biosensor has a particular threshold voltage, for K>1, proposed biosensor has a particular threshold voltage for a fixed K, this shift in threshold voltage compared to the case when K=1 offers a metric to effectively detect the biomolecule type. It is important to mention here that significant change in surface potential occurs in Region 1 under gate M_S due to variation of dielectric constant of biomolecules in the nanogap above the fixed SiO_2 layer. The surface potential in Region 2 remains almost unchanged due to the fixed gate stack TiO_2 - SiO_2 configuration under M_D. Fig.2.4 demonstrates the surface potential distribution along the channel position for charged biomolecules (negative, positive) having a particular value of K (=5). For the case, N_f=0, K=5,

the source-channel barrier height is already high leading to higher threshold voltage. Now, charge of the biomolecules is considered as the presence of fixed interface trapped charges having charge density N_f . As this charge becomes more and more positive, then as per equation $V_{FBf_1}{}' = V_{FB_1} - \frac{qN_f}{C_{eff}}$ (already mentioned in Surface potential modeling section), the effective flat-band voltage decreases. Thus, for a high value of positive charge, effective flat-band voltage decreases and applied gate voltage (as per equation $V_{gs1}{}' = V_{gs} - V_{FBf_1}{}'$) easily works towards accumulation of charge carriers for inversion leading to a lower source-channel barrier height and finally a reduced threshold voltage.

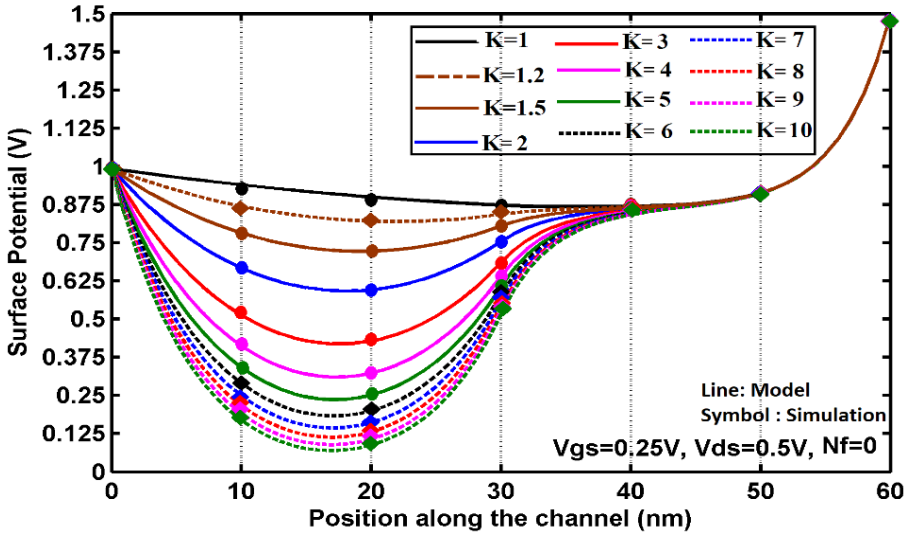


Fig. 2.3 Surface potential distribution along the channel length for the proposed biosensor for variation of neutral biomolecules in the nanogap

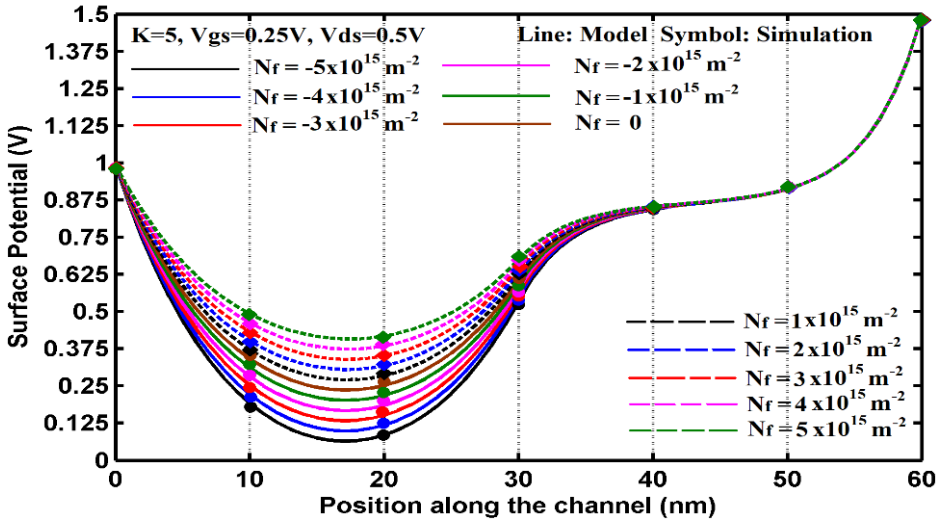


Fig.2.4 Surface potential distribution along the channel length for the proposed biosensor for variation of charged biomolecules (K=5) in the nanogap

This effect can be easily observed in fig. 2.4. Now, for higher values of negative charge, the effective flat-band voltage increases. Thus, for a high value of negative charge, the effective flat-band voltage increases, so at a particular gate voltage, the source-channel barrier height is quite high implying a greater threshold voltage necessitating application of more V_{gs} to trigger conduction. Fig. 2.5. portrays the graphical illustration of surface potential distribution along the channel length for both neutral and charged biomolecules for proposed GWFE incorporated biosensor and its Single-Material Gate (SMG) Counterpart. For the proposed biosensor for a charged as well as neutral biomolecule with K=5 placed in the nanogap, the surface potential distribution possesses a unique step profile along with a source-shifted minimum. This unique step profile screens the minimum from getting affected from drain voltage alterations. However, for the SMG counterpart, the absence of GWFE does not lead to the formation of any step profile and also the minimum is much more shifted towards the drain causing it highly susceptible to changes due to drain volatge alterations. This implies that the proposed GWFE incorporated biosensor has higher immunity towards DIBL compared to its SMG contemporary. Also, the graphical illustration shows that the surface potential has steeper slope for SMG device compared to the proposed biosensor. This will cause elevated hot carrier effect (HCE) in SMG devices compared to the proposed biosensor. Surface potential distribution along the channel length for both neutral

and charged biomolecule, for different ratio of L_{gap}:L_1, where L_{gap} is the length of the nanogap/gate M_s, is exhibitted in fig. 2.6. For the case with L_{gap}:L_1=2:1, the source-channel barrier height greatly increases leading to highest threshold voltage, also the minimum gets shifted more towards drain and the step profile becomes less prominent. For L_{gap}:L_1=1:1, the source-channel barrier height is preferable with not so high, not so low value of threshold voltage. Also, the minimum is shifted more towards the source and a prominent step profile can be obtained that altogether leads to higher DIBL immunity. Finally, for the case, L_{gap}:L_1=1:2, the source-channel barrier height is significantly reduced that lowers the threshold voltage to a great extent, this may induce leakages leading to more power consumption. Thus, even with a source-shifted minimum and a prominent step profile, the ratio L_{gap}:L_1=1:2 is not prefereable due to significantly reduced threshold voltage. Fig.2.7 exhibits the variation of threshold voltage vs. dielectric constant of neutral biomolecules for two different channel lengths and for two different heights of nanogap up to which the neutral biomolecules are filled. The nanogap has a fixed height of 11nm. The figure exhibits that as the biomolecules fully fill the nanogap, threshold voltage is found to decrease whereas when the biomolecules fill up to 9nm of the nanogap out of 11nm, threshold voltage increases. Threshold voltage also increases for a channel length of 100nm.

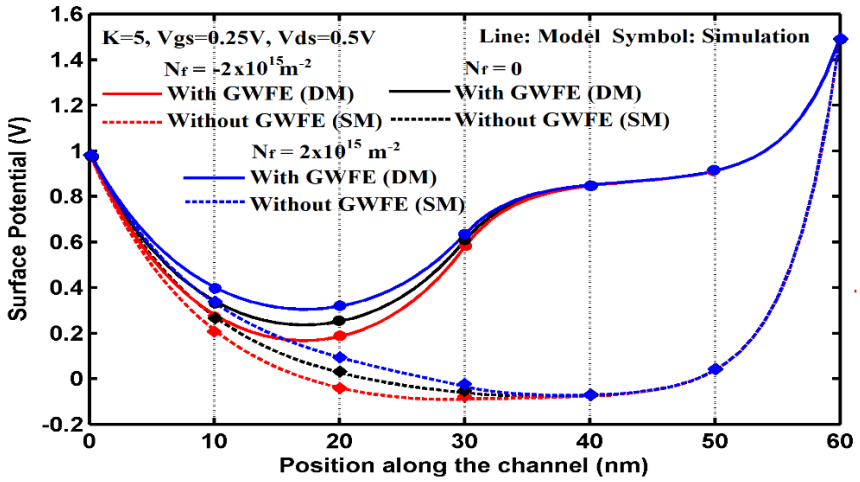


Fig. 2.5 Surface potential distribution along the channel length for both charged and neutral biomolecules for the proposed GWFE incorporated biosensor and its Single-Material Gate (SMG) Counterpart

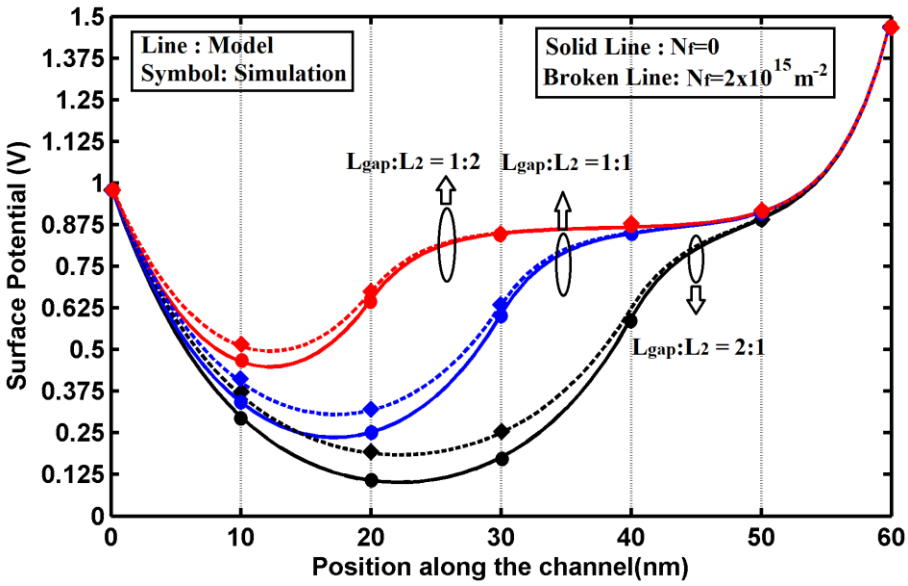


Fig. 2.6 Surface potential distribution along the channel length for proposed biosensor for neutral and charged biomolecules for different ratios of L_{gap}:L_1

However, when the channel length is scaled down to 60nm, several SCEs start to appear that reduces the threshold voltage. Finally, threshold voltage is lower for biomolecules with lower K and gradually starts increasing for biomolecules with higher K since, source-channel barrier height in surface potential distribution increases as K-value increases as already discussed in fig. 2.3.

Fig. 2.8 exhibits the graphical illustration of threshold voltage variation vs. dielectric constant of neutral biomolecules for different L_{gap}:L_1 ratio and for two different channel lengths. Firstly, threshold voltage, for all L and L_{gap}:L_1 ratio value, increases for neutral biomolecules having higher K-value, as already discussed earlier. Threshold voltage for higher channel length of 100nm is greater for all L_{gap}:L_1 ratio values, compared to the case for L=60nm. At a scaled channel length, SCE starts appearing which causes threshold voltage lowering and an increased threshold voltage roll-off compared to the case for L=100nm, this can be clearly observed from the graph. Now, as discussed for fig. 2.6, for ratio L_{gap}:L_1 = 2:1, source-channel barrier height being highest, threshold voltage is highest, for L_{gap}:L_1 = 1:1, threshold voltage is moderate, not so high, not so low, however for L_{gap}:L_1 =1:2, source-channel barrier height being lowest, threshold voltage is significantly reduced that paves the path for increased leakages in the proposed biosensor. Fig.2.9 demonstrates the graphical

illustration of threshold voltage variation vs. charge of biomolecules (K=5) for different L_{gap}:L_1 ratio and two different channel lengths. Firstly, as explained for fig. 2.4, the more negative the charge, the greater is the source-channel barrier height and greater is the threshold voltage, and the more positive the charge, the lower is the source-channel barrier height and lower is the threshold voltage. This is clearly evident through the plot in fig.2.9. Now, for all ratio of L_{gap}:L_1 , threshold voltage increases for L=100nm compared to the case for L=60nm. Now, similar to the case explained in fig.2.6, source-channel barrier height is highest for L_{gap}:L_1 =2:1, hence threshold voltage is highest in this case. For L_{gap}:L_1 =1:1, threshold voltage is moderate and lowest for the case with L_{gap}:L_1 =1:2 for lowest source-channel barrier height. Fig. 2.10 exhibits the threshold voltage variation vs. charge of biomolecules for two types of charged biomolecules having K=5 and K=2.1. Firstly, for both types of charged biomolecule, threshold voltage is higher for more negatively charged biomolecule and lower for more positively charged biomolecule. Now for K=2.1, source-channel barrier height is much reduced which causes the threshold voltage to reduce, whereas for K=5, source-channel barrier height is much higher leading to increased threshold voltage (also evident from fig. 2.3, 2.4). Fig. 2.11 exhibits the variation of DIBL vs. channel lengths for the proposed biosensor for two different widths and also for the proposed biosensors's SMG counterpart. Comparative DIBL studies of proposed biosensor and its SMG counterpart (both having widths w=5nm) exhibit reduced DIBL in proposed GWFE incorporated biosensor, where its unique step profile in its surface potential distribution, shields the minimum from drain voltage alterations. GWFE being absent in SMG devices, no such shielding of minimum can be obtained, this causes higher DIBL in SMG devices. DIBL is also found to vary considerably with device width. For reduced device width w=5nm, the gate has elevated control over the channel which leads to lower DIBL compared to the case with w=7nm. Fig. 2.12 exhibits the subthreshold slope variation of proposed biosensor for different channel lengths, for different widths of the device and different high-K oxides placed above SiO_2 layer in region 2 under M_D. Keeping the device width fixed at w=5nm, with increasing value of K of the oxide placed above SiO_2, the effective oxide thickness gradually decreases leading to enhanced gate-channel coupling. This enhanced gate-channel coupling plays the major role in dimishing major SCEs like subthreshold swing.

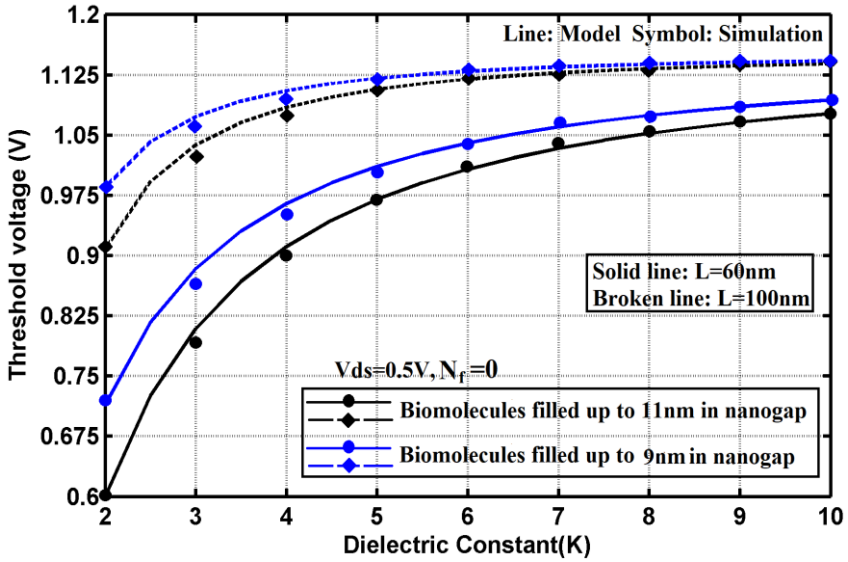


Fig.2.7 Threshold voltage variation vs. dielectric constant for neutral biomolecules for two different channel lengths and two different nanogap heights up to which the neutral biomolecules are filled

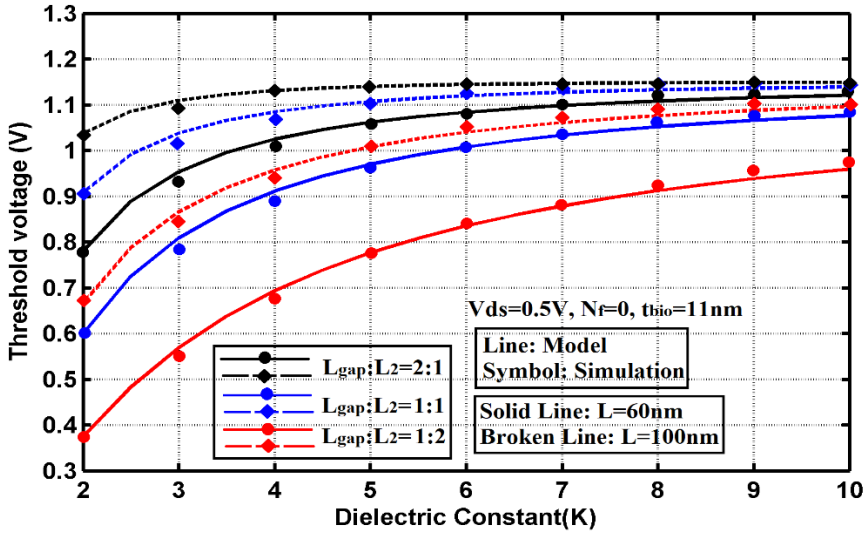


Fig.2.8 Threshold voltage variation vs. dielectric constant of neutral biomolecules for different L_{gap}:L_1 ratio and for two different channel lengths

Thus, among all the cases, when TiO_2 (K=40) is placed above SiO_2, the subthreshold swing is minimum and with increasing channel length, SS saturates to almost 60mV/dec, ideal value for short channel MOSFETs. However, with the same high-K gate stack configuration of TiO_2 (K=40) placed above SiO_2, SS largely increases when device width increases from w=5nm to

w=7nm, owing to reduced gate-channel coupling. Fig.2.13 reveals the graphical illustration of Sensitivity variation vs. dielectric constant of neutral biomolecules for two different channel lengths of the proposed biosensor. Sensitivity for neutral biomolecule is mathematically analyzed using equation (2.35). Threshold voltage is lowest for the case when nanogap is fully filled with air (K=1) as per fig. 2.3. The more the K-value, the higher the threshold voltage and higher is the deviation from the threshold voltage for the case with K=1. This explains the reason behind the gradual increase in sensitivity with increase in dielectric constant of the neutral biomolecules. Also, sensitivity is much greater for L=100nm compared to the case with L=60nm. Sensitivity variation vs. charge of biomolecules of two different types (K=5, K=2.1) for the proposed biosensor is shown in fig.2.14 where the sensitivity is mathematically analyzed using equation (2.36). As per fig.2.10, the change of threshold voltage for a charged molecule with K=2.1 from that of the neutral biomolecule with K=2.1 is much higher compared to the case for K=5. Hence, the more the variation, the greater the sensitivity. This explains the reason behind the escalated sensitivity for K=2.1 compared to the case with K=5. Also, the device is found to be more sensitive to negatively charged biomolecule compared to the positively charged ones (with lower K like 2.1). Fig. 2.15 – 2.17 illustrate the graphical plots for lateral electric field along the channel length for proposed GWFE incorporated biosensor and its SMG contemporary for neutral, negatively and positively charged biomolecules respectively.

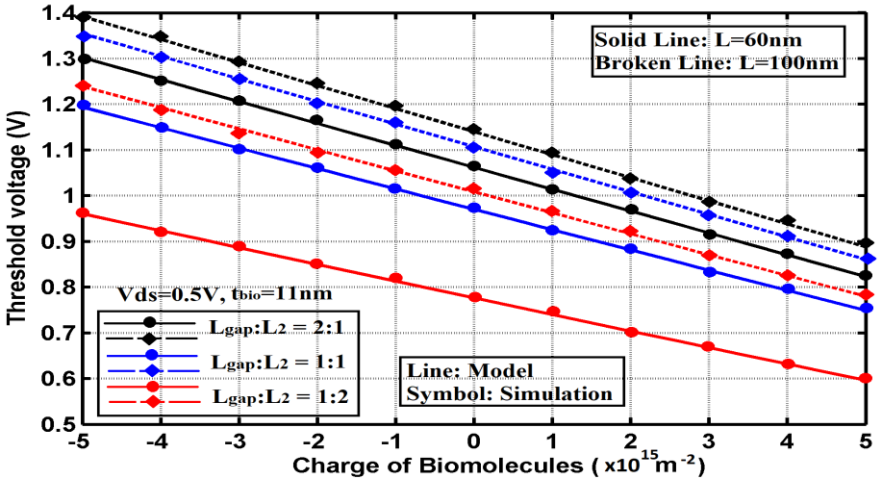


Fig.2.9 Threshold voltage variation vs. dielectric constant of charged biomolecules (K=5) for different L_{gap}:L_1 ratio and for two different channel lengths

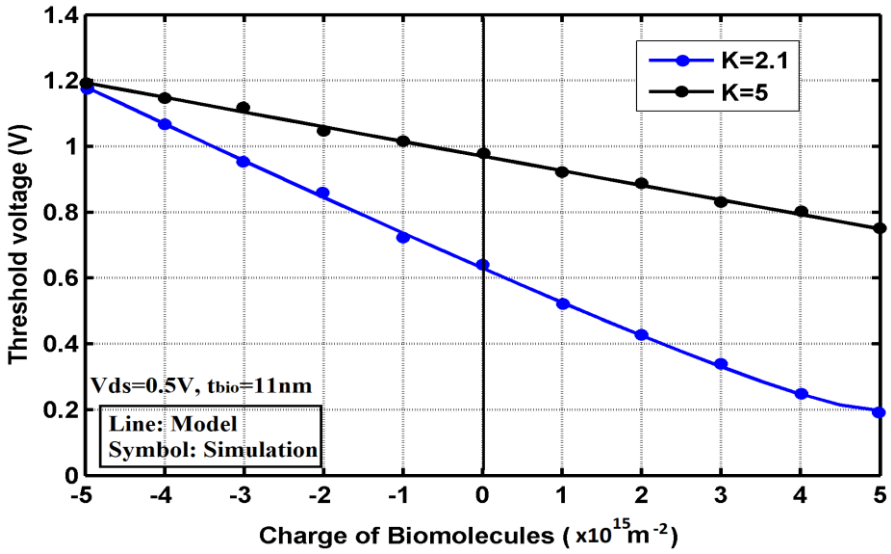


Fig.2.10 Threshold voltage variation vs. charge of biomolecules for two types of charged biomolecules having K=5 and K=2.1

Lateral electric field, for all the three cases, is considerably reduced for the proposed GWFE incorporated biosensor compared to its SMG counterpart. This happens since the proposed biosensor has a reduced slope of surface potential owing to the Dual-Material incorporation in its gate whereas the surface potential slope is quite steep in SMG biosensor. The steep slope results in higher electric field at the drain end causing performance degradation due to hot carrier effect (HCE), which is much reduced in the proposed biosensor. Also, a peak in the lateral electric field distribution of the proposed biosensor is observed at the interface of the two dissimilar gate materials. This peak results in improved transport efficiency. For all the three cases of neutral, positive and negatively charged biomolecule, electric field distribution is found to remain same for both the proposed biosensor and its SMG counterpart. Analytical results match well with Atlas outputs.

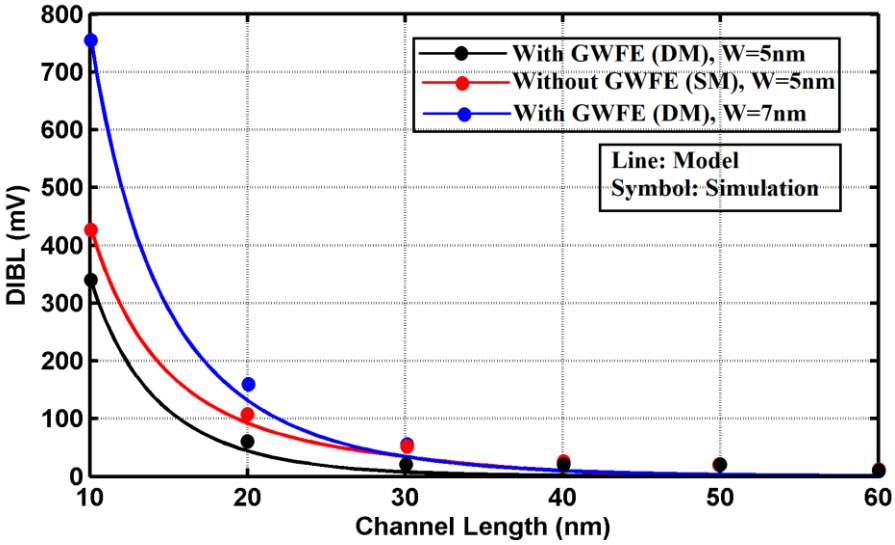


Fig.2.11 DIBL variation for different channel lengths for the proposed biosensor and its SMG contemporary and for two different device widths

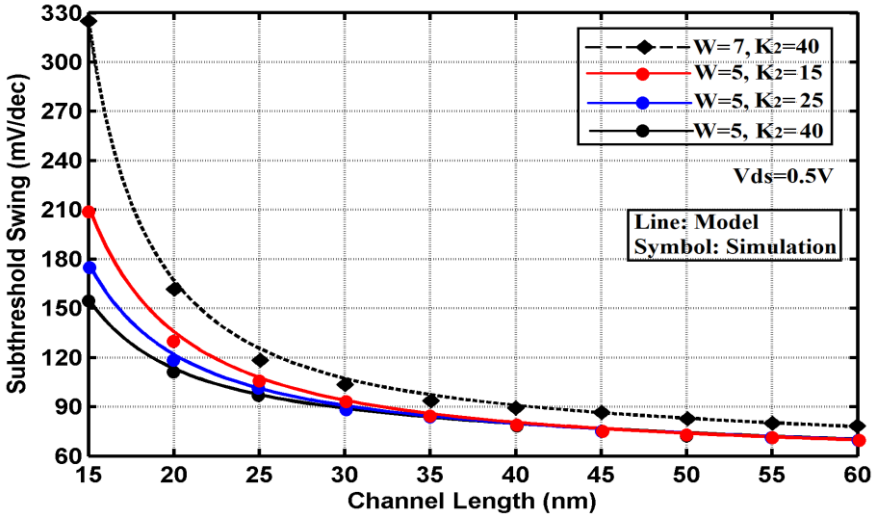


Fig.2.12 Subthreshold Swing variation for different channel lengths for different widths and different high-k oxides placed above SiO_2 in region 2 under M_D

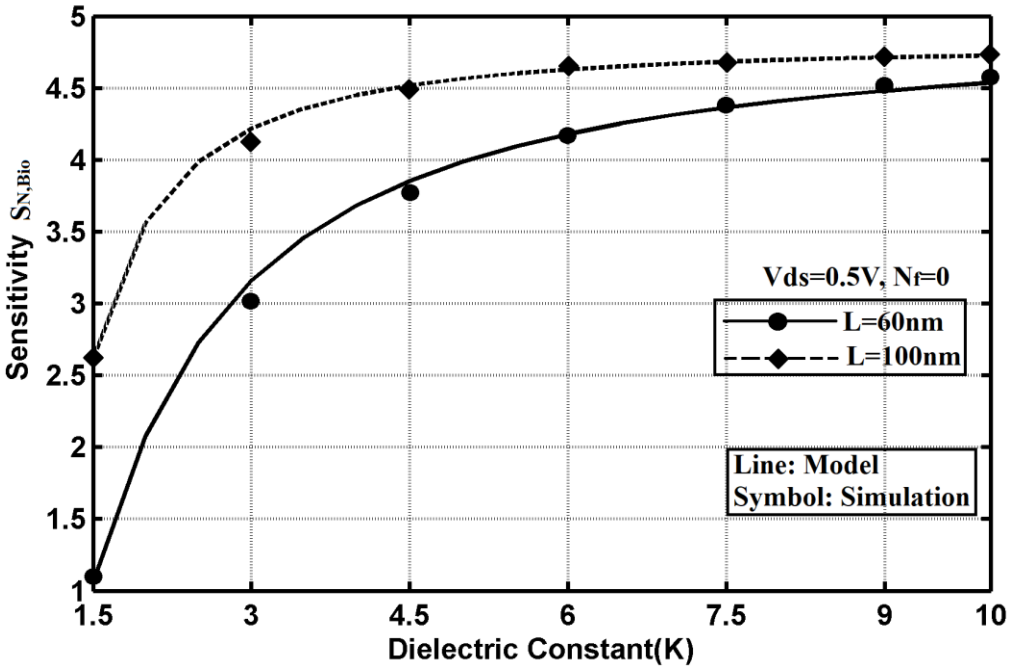


Fig.2.13 Sensitivity variation vs. dielectric constant of neutral biomolecules for two different channel lengths of the proposed biosensor

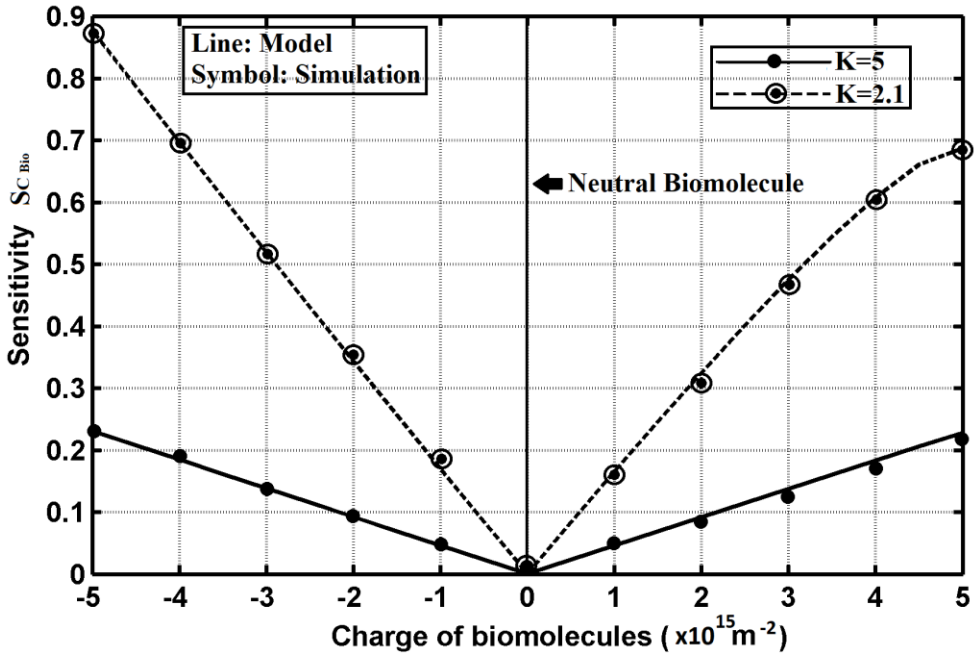


Fig.2.14 Sensitivity variation vs. charge of biomolecules of two different types (K=5, K=2.1) for the proposed biosensor.

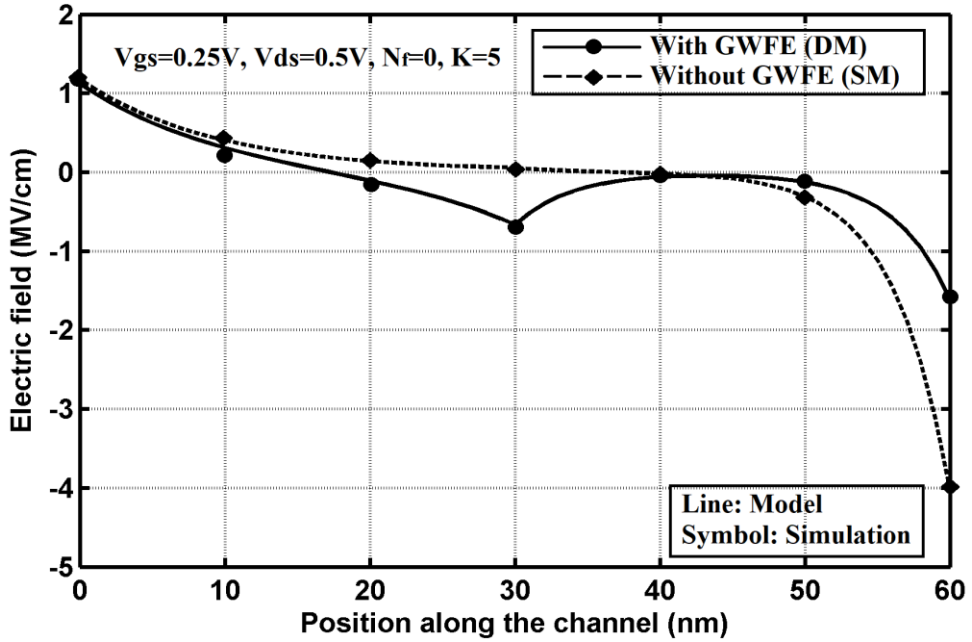


Fig.2.15 Lateral electric field distribution along the channel length for proposed biosensor and its SMG counterpart having neutral biomolecules (K=5) placed in the nanogap

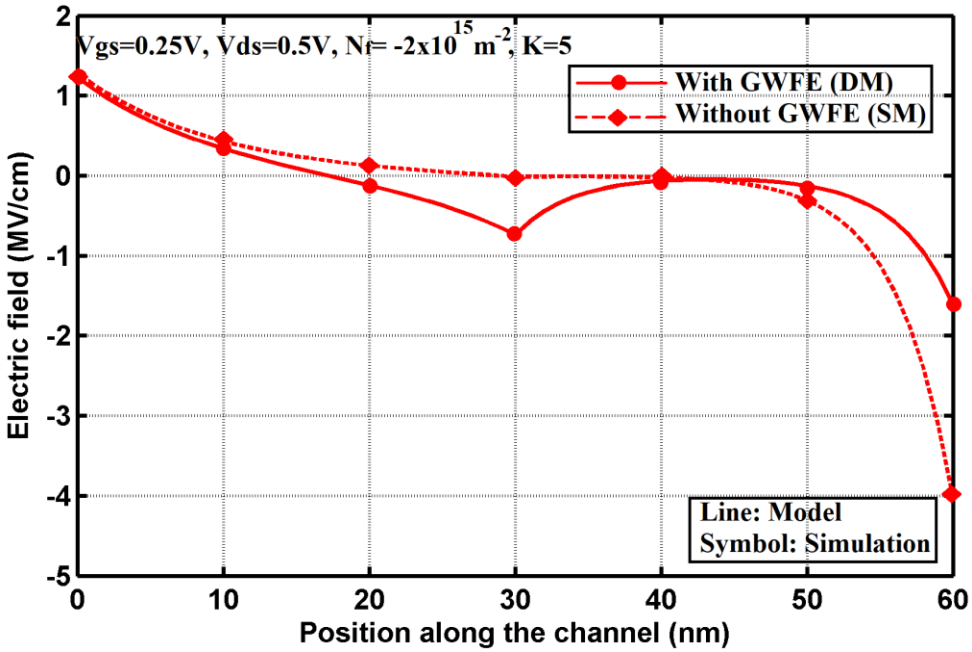


Fig.2.16 Lateral electric field distribution along the channel length for proposed biosensor and its SMG counterpart having negatively charged biomolecules (K=5) placed in the nanogap

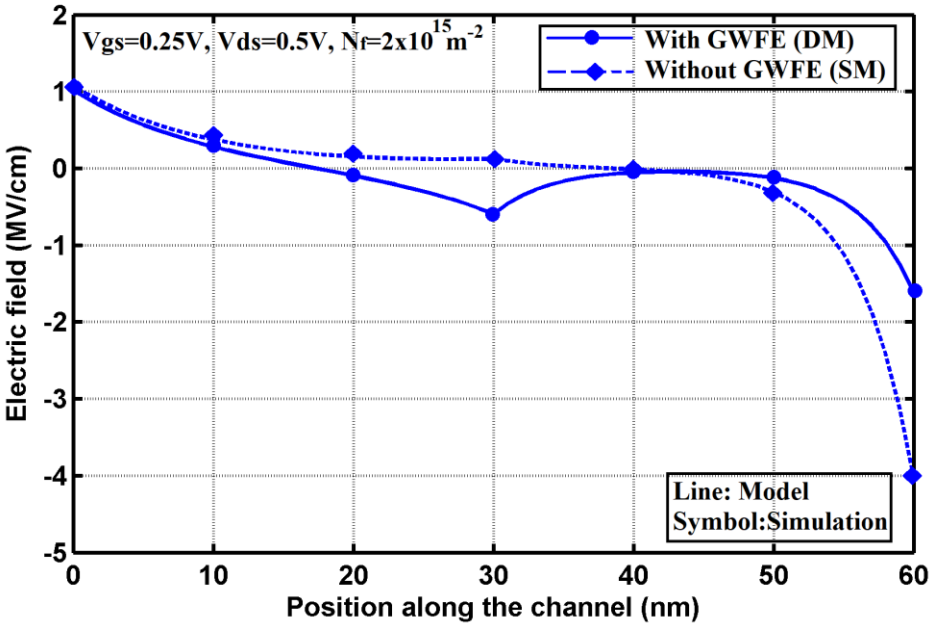


Fig.2.17 Lateral electric field distribution along the channel length for proposed biosensor and its SMG counterpart having positively charged biomolecules (K=5) placed in the nanogap

2.5. Conclusion

Current research illustrates Dielectric-Modulated Dual-Material Trigate MOSFET with a Dual-Material Bottom gate as an effective biosensor of both neutral and charged biomolecules placed in a nanogap. Threshold voltage shifts are observed for different K-values of different neutral/charged biomolecules in the nanogap (due to source-channel barrier height modulations as a direct consequence of flat-band voltage alterations) compared to the case when the nanogap has air (K=1). Shifts in threshold voltages offer a metric to detect the biomolecule type. Also GWFE incorporation in the proposed biosensor offers high quality shielding effects from major SCEs like DIBL, HCE as compared to its Single-Material gate (SMG) counterpart. Selection of TiO_2 – SiO_2 gate stack under gate M_D offers better subthreshold swing characteristics. The proposed biosensor offers higher sensitivity for biomolecules having higher value of K for neutral biomolecules. For charged biomolecules with lower K-value, the biosensor is found to be slightly more sensitive to

negatively charged biomolecules. These evidences fortify the certitude that the proposed biosensor serves as an outstanding detector offering propitious applications for hassle-free, fast and advanced practical-life implementations in biomedical fields.

Relevant Publication

Pritha Banerjee and Jayoti Das, "Gate Work Function Engineered Trigate MOSFET with a Dual-Material Bottom Gate for Biosensing Applications: A Dielectric-Modulation based Approach", **Silicon, Springer**, 14, 419–428, 2022, https://doi.org/10.1007/s12633-020-00823-5 [SCIE, IF: 2.67]

References

[2.1] Pritha Banerjee, Anup Sarkar and Subir Kumar Sarkar, "Exploring the short channel characteristics and performance analysis of DMDG SON MOSFET", Microelectronics Journal, Elsevier, Volume 67, Pages 50-56, September 2017

[2.2] Wen-Shiang Liao, Wei-Tsun Shiau, 2004, "Method of fabricating a double gate MOSFET device", US6855588B1, United Microelectronics Corp, https://patents.google.com/patent/US6855588B1/en

[2.3] W. Cho, Jong-Heon Yang, C. Ahn, K. Im, Jihoon Oh, I. Baek, Seongjae Lee, "Fabrication of SOI p-MOSFET with a 35-nm gate length by using PBF-SPD process", Journal of the Korean Physical Society, Vol. 45, December 2004, pp. S816-S81

[2.4] Robert Chau, Brian Doyle, Jack Kavalieros, Douglas Barlage, Suman Datta, 2016, Tri-gate devices and methods of fabrication, US20040094807A1, https://patents.google.com/patent/US20040094807A1/en

[2.5]David C. Gilmer, Srikanth B. Samavedam, Philip J. Tobin, 2005, Method for fabricating dual-metal gate device, US6972224B2, NXP USA Inc, https://patents.google.com/patent/US6972224

[2.6] "ULSI Process Integration II: Proceedings of the International Symposium", edited by Cor L. Claeys

[2.7] Padmanaban, B., Ramesh, R., Nirmal, D., Sathiyamoorthy, S., "Numerical modeling of triple material gate stack gate all-around (TMGSGAA) MOSFET considering quantum mechanical effects", Superlattices Microstruct. 82, 40–54, 2015

[2.8] Bansal J., Sharma N., Kumar S. P., Chaujar R., Gupta M., Gupta R.S., "Two-dimensional analytical sub-threshold model of Double Gate MOSFET with gate stack", International Conference on Recent Advances in Microwave Theory and Applications , 847–849. doi:10.1109/AMTA.2008.4763136

[2.9] B. Buvaneswari, N.B. Balamurugan, "2D analytical modeling and simulation of dual material DG MOSFET for biosensing application", AEU - International Journal of Electronics and Communications, vol. 99, 2019, Pages 193-200, ISSN 1434-8411, https://doi.org/10.1016/j.aeue.2018.11.039.

[2.10] Rahul Das, Ankush Chattopadhyay, Manash Chanda, Chandan K. Sarkar and Chayanika Bose, "Analytical Modeling of Sensitivity Parameters Influenced by Practically Feasible Arrangement of Bio-Molecules in Dielectric Modulated FET Biosensor", Silicon (2022). https://doi.org/10.1007/s12633-021-01617-z

[2.11] Parija, S.K., Swain, S.K., Biswal, S.M. et al., "Performance Analysis of Gate Stack DG-MOSFET for Biosensor Applications", Silicon (2022). https://doi.org/10.1007/s12633-021-01622-2

[2.12] Ajay, R. Narang, M. Saxena and M. Gupta, "Analytical model of gate underlap Double Gate Junctionless MOSFET as a bio-sensor," 2016 3rd International Conference on Devices, Circuits and Systems (ICDCS), 2016, pp. 152-156, doi: 10.1109/ICDCSyst.2016.7570649

[2.13] Kumari, M., Singh, N.K., Sahoo, M. et al., "2-D Analytical Modeling and Simulation of Dual Material, Double Gate, Gate Stack Engineered, Junctionless MOSFET based Biosensor with Enhanced Sensitivity", Silicon (2021). https://doi.org/10.1007/s12633-021-01223-z

[2.14] Ji-Min Choi; Jin-Woo Han; Sung-Jin Choi; Yang-Kyu Choi, "Analytical Modeling of a Nanogap-Embedded FET for Application as a Biosensor", 57, 12, 3477–3484, 2010, doi:10.1109/ted.2010.2076152

[2.15] Wu, Ling, "Advanced CMOS technologies (high-k/metal gate stacks) for sub-22nm node", https://hdl.handle.net/10356/54848, 10.32657/10356/54848

[2.16] Im, Hyungsoon; Huang, Xing-Jiu; Gu, Bonsang; Choi, Yang-Kyu, "A dielectric-modulated field-effect transistor for biosensing", 2(7), 430–434, 2007, doi:10.1038/nnano.2007.180

[2.17] Ajay, R. Narang, M. Saxena and M. Gupta, "Analytical modeling of a split-gate dielectric modulated metal-oxide-semiconductor field-effect transistor for application as a biosensor,"

2014 2nd International Conference on Devices, Circuits and Systems (ICDCS), 2014, pp. 1-6, doi: 10.1109/ICDCSyst.2014.6926183.

[2.18] Pratap, Yogesh; Kumar, Manoj; Kabra, Sneha; Haldar, Subhasis; Gupta, R. S.; Gupta, Mridula, "Analytical modeling of gate-all-around junctionless transistor based biosensors for detection of neutral biomolecule species", Journal of Computational Electronics, 2017, doi:10.1007/s10825-017-1041-4

[2.19] S. Yadav, A. Gedam and S. Tirkey, "A Dielectric Modulated Biosensor for SARS-CoV-2," IEEE Sensors Journal, vol. 21, no. 13, pp. 14483-14490, 1 July1, 2021, doi: 10.1109/JSEN.2020.3019036.

[2.20] Kumari, M., Singh, N.K., Sahoo, M. et al., "Work function optimization for enhancement of sensitivity of dual-material (DM), double-gate (DG), junctionless MOSFET-based biosensor", Appl. Phys. A 127, 130, 2021, https://doi.org/10.1007/s00339-020-04256-0

[2.21] Chang-Hoon Kim, Cheulhee Jung, Hyun Gyu Park & Yang-Kyu Choi, "Novel Dielectric-Modulated Field-Effect Transistor for Label-Free DNA Detection", Biochip Journal, Vol. 2, No. 2, 127-134, June 2008

[2.22] Pritha Banerjee and Subir Kumar Sarkar, "3D Analytical Modeling of Dual Material Triple Gate Silicon-on Nothing MOSFET", IEEE Transactions on Electron Devices, Vol.64, Issue 2, pp-368-375, February 2017

[2.23] Ghanatian, H., & Hosseini, S. E., "Analytical modeling of subthreshold swing in undoped trigate SOI MOSFETs", Journal of Computational Electronics, 15(2), 508–515, 2016, doi:10.1007/s10825-016-0817-2

[2.24] P. Banerjee, P. Saha, D. K. Dash and S. Kumar Sarkar, "A Study of Short Channel Performance of Dual Material strained silicon Trigate (DM Strained-Si TG) SOI MOSFET," 2018 International Conference on Computing, Power and Communication Technologies (GUCON), 2018, pp. 101-104, doi: 10.1109/GUCON.2018.8674997.

[2.25] Gao, Hong-Wun; Wang, Yeong-Her; Chiang, Te-Kuang, "A Quasi-3-D Scaling Length Model for Trapezoidal FinFET and Its Application to Subthreshold Behavior Analysis", IEEE

Transactions on Nanotechnology, 16(2), 281–289, 2017, doi:10.1109/TNANO.2017.2662018

[2.26] Pritha Banerjee and Subir Kumar Sarkar, “Analysis of short channel characteristics in graded channel dual-material elliptical gate-all-around (GC DM EGAA) MOSFET”, Semiconductor Science and Technology, IOP, January 2019, DOI: 10.1088/1361-6641/aafc86

[2.27] Ganapati, R., Samoju, V. R., & Jammu, B. R. , “Analytical Modeling of Threshold Voltage for Dual-Metal Double-Gate Gate-All-Around (DM-DG-GAA) MOSFET”, Silicon, 13(9), 2869–2880, 2020, doi:10.1007/s12633-020-00602-2

[2.28] C. Te-Kuang, "A Novel Quasi-3-D Interface-Trapped-Charge-Induced Threshold Voltage Model for Quadruple-Gate MOSFETs, Including Equivalent Number of Gates," in IEEE Transactions on Electron Devices, vol. 61, no. 5, pp. 1615-1618, May 2014, doi: 10.1109/TED.2014.2312922.

[2.29] W. Cho, Jong-Heon Yang, C. Ahn, K. Im, Jihoon Oh, I. Baek, Seongjae Lee, "Fabrication of SOI p-MOSFET with a 35-nm gate length by using PBF-SPD process", Journal of the Korean Physical Society, Vol. 45, December 2004, pp. S816-S81

[2.30] D. Fayçal, A. Mohamed Amir, A. Djemai and B. Toufik, "Surface- potential- based model to study the subthreshold swing behavior including hot-carrier effect for nanoscale GASGAA MOSFETs," 5th International Conference on Design & Technology of Integrated Systems in Nanoscale Era, 2010, pp. 1-4, doi: 10.1109/DTIS.2010.5487573

[2.31] Pritha Banerjee, Priyanka Saha and Subir Kumar Sarkar, "Analytical Modelling and Performance Analysis of Gate Engineered Tri-gate SON MOSFET", IET Circuits, Devices & Systems, Volume 12, Issue 5, 2018 , p. 557 - 562, DOI 10.1049/iet-cds.2017.0473 March 2018

Chapter 3

Chapter 3: *Gaussian-doped GWFE Cylindrical Gate-All-Around (CGAA) MOSFET: Mathematical Modeling & Simulation considering the effect of Temperature and Fixed interface trap charges*

3.1. Introduction

In the previous chapter, the exploration of GWFE incorporated Trigate MOSFET with a dual-material bottom gate as an efficient biosensor for label-free detection of both neutral and charged biomolecules has been presented. The basic device geometry to be selected for biosensing applications needs to be featured with easy label-free method of detection through dielectric-modulation approach, excellent SCE immunization, higher sensitivity, mass production, low-cost manufacturing, easy integration into portable and wearable devices, diminished power consumption and reduced off-state leakages to ensure minimized off-state power dissipation. Trigate MOSFET geometry is found to possess the above stated characteristics to a large extent and thus has been considered in the previous chapter to work as an efficient biosensor.

However, Gate-all-around (GAA) MOSFETs are currently the foremost choice when it comes to offering significantly grander SCE resistance, radically higher packaging density, higher current driving capability and diminished on and off-state leakages [3.1]. However, GAA devices with ideal circular cross-sections are more preferred over quadruple GAA devices since the latter is found to substantially suffer from corner effects and thus include additional fabrication steps for corner-rounding to minimize serious concerns related to leakage mechanisms [3.2-3.3]. Thus, considering the fact that CGAA MOSFET offers a whole host of benefits, advanced CGAA MOSFET can be thus effectively employed in real-time applications such as biosensor.

However, before any advanced CGAA device can be employed for practical applications, it is important to conduct a detailed short channel effect investigation along with parallel in-depth studies of the characteristics like potential, threshold voltage, electric field etc. of the planned advanced CGAA device.

Incessant innovation in CMOS technology in search of upgraded devices characterized by high speed, miniaturization, cost-efficacy and lower power consumption has been the key reason behind the semiconductor industrial and technological resurgence. Device scaling has been a boon in achieving the desired device features. However, aggressive device scaling in nanometer regime causes the performance

attenuating short channel effects (SCEs) to come into play. These SCEs such as Drain-induced barrier lowering (DIBL), hot carrier effect (HCE), threshold voltage roll-off (TVRO), subthreshold slope degradation [3.4] etc. causes deterioration in device performance and initiates various leakage mechanisms that highly increases the power consumption in the device. Overpowering these SCEs comprises the steps that constitute innovative technology incorporation and material property improvement. However, it is equally important to consider the gate-oxide-channel interface quality of the advanced device. The Si-SiO_2 interface plays a significant role in determining the electrical properties of a device. An ideal Si-SiO_2 interface is very rare in fabrication since the interface tends to get damaged due to several fabrication related processes apart from hot carrier induced damages. This can give rise to various unwanted fixed localized interface trap charges. These charges that arise as a result of fabrication process related damages can be present at the interface along the entire channel and hence significantly modify the flat-band voltage that severely affects the device stability in terms of potential, threshold voltage and many more device properties. Whereas the fixed localized trap charges that are created as a result of hot carrier induced damages because of high electric field, occur at the Si-SiO_2 interface but are confined towards the drain region of the channel.

Existing literature reports such as [3.5] states that the fixed localized trapped charges, arising out of fabrication related process damages, exhibit strong dependencies on oxidation processing variables such as whether the oxidation environment is of dry oxygen or steam, the oxidation temperature, silicon orientation used, annealing temperature etc. Now, as reported by Garg et al. [3.6], the localized interface trapped charges arising out of fabrication related process damages can be present at the Si-SiO_2 interface, throughout the entire channel. Saha et al. [3.7] reported the interface trap charge induced threshold voltage modelling of a Gate work function engineered MOSFET where the trap charges are considered to be present at the interface along the entire channel. Moreover, Srivastava et al. [3.8] has modelled the interface trap charge induced electrical performance of an advanced FD-SOI MOSFET where the trapped charges arising out of radiation, fabrication process and hot carrier induced damages have been considered at the oxide-semiconductor interface along the entire channel. Likewise, the localized interface trapped charges that

result out of damages related to fabrication processes, radiation and hot carrier effect have also been considered in the following researches included in this chapter to accurately model the electrical characteristics of both damaged and undamaged projected device under consideration.

Damaged Si-SiO_2 interface causes accumulation of interface traps. These traps will accept an electron if the trap energy level is located beneath the Fermi level for an acceptor-type trap and will be acting as a localized/fixed negative trap charge. The trap accepts a hole for a donor-type trap with trap energy level located above the Fermi level and will act as a localized/fixed positive trap charge [3.9]. These charges considerably modify the flat-band voltage which subsequently impacts the device characteristics like potential, threshold voltage, drain current etc. Thus modeling the mathematics related to the electrical features of the damaged device followed by subsequent comparison with those of the undamaged device offers comprehensive ideas regarding the trap charge induced behavior of the device. This provides a detailed insight to the extent of reliability of device performance in case of presence of trap charges.

Thermal behavior of the device needs parallel attention when the parameter of reliability is being discussed. For suitable implementation of the device assuring performance consistency over a wide range of temperature necessitates the mathematical temperature-based modeling and subsequent evaluation of the device electrical features. Within a temperature range of 100K – 500K, a number of parameters such as intrinsic concentration, permittivity of silicon, bandgap of silicon, Fermi levels, built-in potentials etc. are found to change. This significantly affects device characteristics and thus need to be considered while investigating the device response. Moreover, many researches have exhibited the fact that localized trap charges have significant effect on the thermal behavior of the device [3.10] and thus, motivated by these facts, this section of research deals with the thermal behavior modeling of advanced GWFE incorporated Cylindrical Gate-all-around architecture MOSFETs including the influence of localized/fixed interface trap charges.

3.2. Overview

The avant-garde technology of GWFE has been prevalent for its incredible ability to suppress major SCEs like DIBL, HCE, [3.11-3.12] etc. Researchers use this popular strategy in Multi-gate MOSFETs to significantly upgrade device performance [3.13-3.14]. However, consistency of this upgraded performance should be assured simultaneously for reliable implementation of these advanced devices for future generation VLSI applications. Consistency or reliability of the device performance largely depends on Si-SiO_2 interface quality since it tends to get damaged due to stress, fabrication related processes, hot carrier injection etc. Damaged interface causes the formation of interface trapped charges that modulate the flat-band voltage and alter device characteristics [3.15].

In the following research exertion, an advanced geometry MOSFET namely Cylindrical Gate-all-around (CGAA) MOSFET has been considered for exploration. CGAA MOSFETs are pioneering MOSFET structures that have high immunity to SCEs, strong field confinement, supports scalability ensuring high packaging density [3.16]. One of the most favored scheme of Dual-Material Gate has been employed in a CGAA MOSFET.

The fabrication feasibility of Dual-material gate has already been discussed in chapter 2. CGAA MOSFETs are also fabrication feasible and the step by step fabrication process are detailed in the research by Mukaiyama et al. [3.17]. Both conventional and a new technique of fabricating GAA MOSFETs have been highlighted in this research. In the conventional process, etching masks are patterned using usual photo-lithography and silicon is etched by dry etching process. Then silicon regions are made narrow using some additional processes and subsequently silicon wires are formed. Buried oxide near the channel region is etched and free-standing silicon wires are formed. Then gate-oxidation is done followed by metal/polysilicon deposition which is done using normal MOSFET process and the final structure is a GAA MOSFET.

The new process comprises of silicon nitride patterning using usual photo-lithography, followed by anisotropic silicon etching using TMAH at 75 degree Centigrade. Then selective

oxidation is done followed by silicon nitride removal using hot phosphoric acid at 180 degree centigrade with the anisotropic etching performed again. Thus two silicon wires are formed. Then buried oxide etching is done using HF, gate oxidation and polysilicon/metal deposition is done to form the new GAA structure.

Now, the reliability of the device has been investigated in presence of trap charges and compared with the results of the undamaged device. In addition to this, the thermal behavior of the device has also been modeled for successful implementation in a varying temperature range of 100K – 500K. However, at temperatures below 100K, impurity deionization occurs followed and at temperatures above 500K, relative permittivity of SiO_2 starts exhibiting strong dependence on temperature. So the investigation has been confined within the temperature limits of 100K – 500K.

However, the channel in the structure has a Gaussian-doping instead of the uniform doping. It has been reported by Zhang et al. [3.18] that most practical MOSFETs have a Gaussian-doped channel and thus, Gaussian-distribution parameters like Peak doping, Projected range and straggle are also considered and varied to estimate their effects on the device characteristics.

3.3. Analytical Modeling

Fig.3.1 presents the 2-D schematic representation of the Dual-Material Cylindrical Gate-all-around (DM CGAA) MOSFET with a Gaussian-doped channel. The gate material towards source is M_S with work function 4.6eV and gate length L_1 (=30nm), gate material towards the drain end is M_D with work function 4.4eV and gate length L_2 (=30nm). The gate-oxide SiO_2 has a thickness (t_{ox}) of 2nm. The channel is a Gaussian-doped p-type with total channel length (L_1+ L_2=L=60nm). R denotes the channel radius.

3.3.1. Center Potential Modeling

The Gaussian-doping distribution in the channel region is expressed using the [3.19]:

$$N_c(r) = \frac{Q}{\sigma_p \sqrt{2\pi}} \exp\left(\frac{-\left(r - R_p\right)^2}{2\sigma_p{}^2} \right) \tag{3.1}$$

Here Q denotes the implantation dose per unit area, R_p denotes the Projected range and σ_p denotes the straggle of the Gaussian-distribution. For ease of calculation, the channel is divided into two regions, region 1 with boundaries $0 \le z \le L_1, 0 \le r \le R$ and region 2 with boundaries $L_1 \le z \le L, 0 \le r \le R$.

In order to obtain the expression of center potential, 2-D Poisson's equation needs to be solved in the channel region. The 2-D Poisson's equation for j[th] region (where j=1 for region 1 and 2 for region 2) is expressed as follows [3.20]:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\left(\phi_j(r,z)\right)}{\partial r}\right)+\frac{\partial^2\phi_j(r,z)}{\partial z^2}=\frac{qN_c(r)}{\varepsilon_{Si}(T)} \tag{3.2}$$

Where $\phi_j(r,z)$ is the potential distribution in the j[th] region. $\varepsilon_{Si}(T)=\left(11.4+\left(1+\left(1.2\times10^{-4}\right)T\right)\right)\varepsilon_0$ is the temperature-dependent dielectric permittivity of the silicon channel.

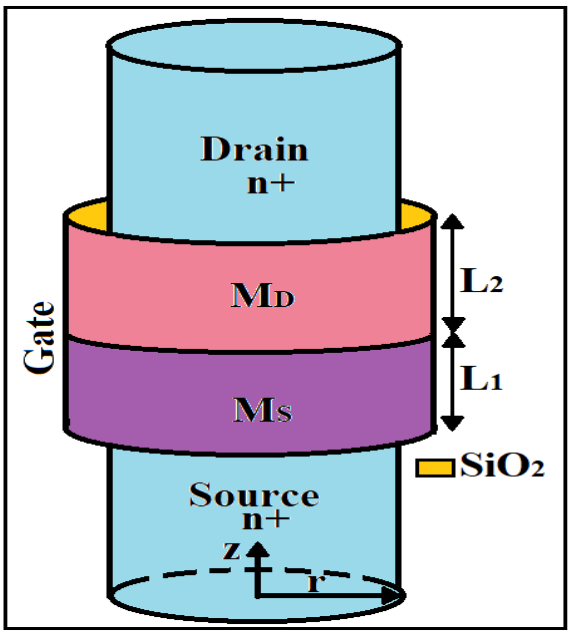


Fig.3.1 Schematic 2-D Representation of the proposed device

The potential in the channel is parabolic in the radial direction as per Young's Parabolic Potential Approximation [3.21], therefore:

$$\phi_j(r,z) = C_{0j}(z) + C_{1j}(z)r + C_{2j}(z)r^2 \tag{3.3}$$

In order to evaluate the expressions of the coefficients in equation (3.3), the following boundary conditions are to be considered [3.22]:

The device under consideration is symmetric in radial direction that causes the electric field at the channel center to be zero.

$$\left.\frac{\partial \phi_j(r,z)}{\partial r}\right|_{r=0} = C_{1j} = 0 \tag{3.4}$$

At r=R, the potential is actually the surface potential and is given as:

$$\phi_j(R,z) = \phi_{sj}(z) \tag{3.5}$$

At r=0, the potential is actually the center potential and is given as:

$$\phi_j(0,z) = C_{0j}(z) \tag{3.6}$$

Continuity of electric field at r=R (at Si-SiO_2) interface leads to:

$$\left.\frac{\partial \phi_j}{\partial r}\right|_{r=R} = \frac{C_{ox}}{\varepsilon_{Si}(T)}\left[V_{gs_j}{}' - \phi_{sj}(z)\right] \tag{3.7}$$

Where $C_{ox} = \dfrac{\varepsilon_{ox}}{R\ln\left(1+\frac{t_{ox}}{R}\right)}$, $V_{gs_j}{}' = V_{gs} - V_{fbj}{}'$, V_{gs} is the gate-to-source voltage, $V_{fbj}{}'$ is the effective flat-band voltage in the j[th] region and is given as $V_{fb_j}{}' = V_{fb_j} - \dfrac{qN_f}{C_{ox}}$, here $V_{fb_j} = \phi_{M_{S(j=1)orD(j=2)}} - \phi_{si}(T)$, where $\phi_{si}(T) = \chi + \dfrac{E_g(T)}{2} + \phi_{f_{Si}}(T)$ is the temperature-dependent Si work function, Fermi potential is given as $\phi_{f_{Si}}(T) = \dfrac{KT}{q}\ln\left(\dfrac{N_c(r=R)}{n_i(T)}\right)$, intrinsic carrier concentration is given as $n_i(T) = (1.706\times10^{25}).\left(\dfrac{T}{300}\right)^{3/2}.\exp\left(\dfrac{-qE_g(T)}{2KT}\right)$ [3.23]. N_f is the fixed interface trap charge density.

The coefficient $C_{2j}(z)$ in equation (3.3) thus obtained is as follows:

$$C_{2j} = \frac{V_{gs_j}' - C_{0j}(z)}{R^2\left(1+\frac{2\varepsilon_{Si}(T)}{RC_{ox}}\right)} \tag{3.8}$$

Substituting the expressions for $C_{1j}(z)$ and $C_{2j}(z)$ in equation (3.3) and then in equation (3.2), the differential equation thus obtained is as follows:

$$\frac{d^2C_{0j}(z)}{dz^2} - \alpha C_{0j}(z) = \beta_j \tag{3.9}$$

Here, $\alpha = \frac{4}{R^2\left(1+\frac{2\varepsilon_{Si}(T)}{RC_{ox}}\right)}$, $\beta_j = \frac{qN_c(r=0)}{\varepsilon_{Si}(T)} - \alpha V_{gs_j}'$

Solution to equation (3.9) gives the expression of center potential in region 1 and 2. These are given as follows:

In region 1, $C_{01}(z) = A_1e^{\eta z} + B_1e^{-\eta z} - \sigma_1$ (3.10)

In region 2, $C_{02}(z) = A_2e^{\eta(z-L_1)} + B_2e^{-\eta(z-L_1)} - \sigma_2$ (3.11)

Here, $\eta = \sqrt{\alpha}, \sigma_1 = \frac{\beta_1}{\alpha}, \sigma_2 = \frac{\beta_2}{\alpha}$

To evaluate the expressions of the coefficients A_1, B_1, A_2, B_2, the following boundary conditions need to be considered [3.24]:

Continuity of potential at the interface of two materials leads to:

$$C_{01}(z)\big|_{z=L_1} = C_{02}(z)\big|_{z=L_1} \tag{3.12}$$

Continuity of electric flux at the interface of two materials leads to:

$$\left.\frac{dC_{01}(z)}{dz}\right|_{z=L_1} = \left.\frac{dC_{02}(z)}{dz}\right|_{z=L_1} \tag{3.13}$$

At source end, $C_{01}(z=0) = V_{bi}(T) = \frac{KT}{q}\ln\left(\frac{N_c(r=0)N_d}{n_i^2(T)}\right)$ (3.14)

At Drain end, $C_{02}(L) = V_{bi}(T) + V_{ds}$ (3.15)

The expressions of A_1, B_1, A_2, B_2 thus obtained are:

$$A_1 = \theta_1 + \gamma_1 V_{gs} \tag{3.16}$$

$$B_1 = \theta_2 + \gamma_2 V_{gs} \tag{3.17}$$

$$A_2 = A_1 e^{\eta L_1} - (\sigma_1 - \sigma_2) \tag{3.18}$$

$$B_2 = B_1 e^{-\eta L_1} - (\sigma_1 - \sigma_2) \tag{3.19}$$

Here, $\theta_2 = \dfrac{V_{bi}(T) + \dfrac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)}\left(e^{\eta L} - 1\right) + V_{fb_1}' e^{\eta L} - V_{fb_2}' - \left(V_{bi}(T) + V_{ds}\right) - (\sigma_1 - \sigma_2)\cosh \eta L_2}{2 \sinh \eta L}$,

$\gamma_2 = \dfrac{1 - e^{\eta L}}{2 \sinh \eta L}$, $\theta_1 = V_{bi}(T) + \dfrac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)} + V_{fb_1}' - \theta_2$, $\gamma_1 = -1 - \gamma_2$

3.3.2. Threshold Voltage Modeling

The value of V_{gs} at which the minimum center potential is equal to $2\phi_{f_{Si}}(T)$ is termed as the threshold voltage. Thus, in order to evaluate the expression for minimum center potential, the position for minimum center potential needs to be found out first. It, thus, can be evaluated using the following equation:

$$\left.\frac{dC_{o1}}{dz}\right|_{z=z_{\min}} = 0 \tag{3.20}$$

Thus the position of minimum center potential is given as:

$$z_{\min} = \frac{1}{2\eta} \ln\left(\frac{B_1}{A_1}\right) \tag{3.21}$$

Thus the expression of threshold voltage can be evaluated using the following equation:

$$C_{01}(z_{\min}) = 2\phi_{f_{Si}}(r=0) \tag{3.22}$$

The expression for threshold voltage of the proposed device is as follows:

$$V_{thr} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{3.23}$$

Here $a = 4\gamma_1\gamma_2 - 1$, $b = 2\left[2(\theta_1\gamma_2 + \theta_2\gamma_1) + \left(2\phi_{f_{Si}}(r=0) + \frac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)} + V_{fb_1}{}'\right)\right]$,

$$c = 4\theta_1\theta_2 - \left(2\phi_{f_{Si}}(r=0) + \frac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)} + V_{fb_1}{}'\right)^2$$

3.3.3. Short Channel Effect Modeling

DIBL (in mV) is given as [3.25]:

$$DIBL = V_{thr_{lin}} - V_{thr_{sat}} \tag{3.24}$$

Here, $V_{thr_{lin}}$ and $V_{thr_{sat}}$ are threshold voltages in linear and saturation regions respectively.

Subthreshold Swing (in mV/dec) is given as [3.26]:

$$SS = 2.3\frac{KT}{q}\left[\frac{dC_{01_{\min}}}{dV_{gs}}\right]^{-1} \tag{3.25}$$

Lateral Electric Field is given as [3.27]: $E_z = -\frac{dC_{oj}}{dz}$ (3.26)

3.4. Results & Discussions

Several physics-based simulation models in Silvaco Atlas have been used to obtain the simulation outputs followed by subsequent verification of the analytical results. Some of these models include band-to-band tunneling (BBT.STD) for considering the tunneling effect of charge carriers, drift-diffusion for carrier transport, CVT (Lombardi) mobility, Shockley-Read-Hall recombination for fixed lifetimes, concentration and temperature-dependent ANALYTIC, HEI, parallel electric field-dependent FLDMOB, Auger recombination, concentration-dependent CONMOB and IMPACT SELB to consider the impact ionization effect. The INTERFACE statement is used to define the type and density of localized/fixed charges. Fig. 3.2 demonstrates the graphical illustration of center potential distribution vs. different channel positions. The channel has a vertical Gaussian-doping of implant dose Q = $10^{16}/m^2$.The selected Projected range is 2.5 nm and straggle parameter is chosen to be 2 nm. Channel radius R=5 nm. Data have been obtained for both low temperature of T = 100 K and for a high temperature of T= 500 K. For both the cases, it can be distinguished that for positive trap charges, there is a decrease in source-channel barrier height in center potential

which consequently reduces the threshold voltage of the device. The case is reverse for negative trap charges where the source-channel barrier height increases causing augmented threshold voltage. Now considering the impact of temperature, it can be noticed that for lower temperature like 100K, the center potential increases and for higher temperature like T=500K, it decreases. However, the temperature effects on the device features can be more precisely predicted from threshold voltage plots. Fig. 3.3 illustrates the graphical plots of center potential distribution along different channel positions for both damaged and undamaged device by varying Projected range, channel radius R = 5 nm and straggle parameter is set to 2 nm. For both negative, positive trap charges (for damaged device) and also with no trap charges (for undamaged device), center potential follows the same trend as found in Fig.3.2. For both damaged and undamaged device, when Rp = 0, which implies that the peak doping is located at the channel center, there is an increase in the source-

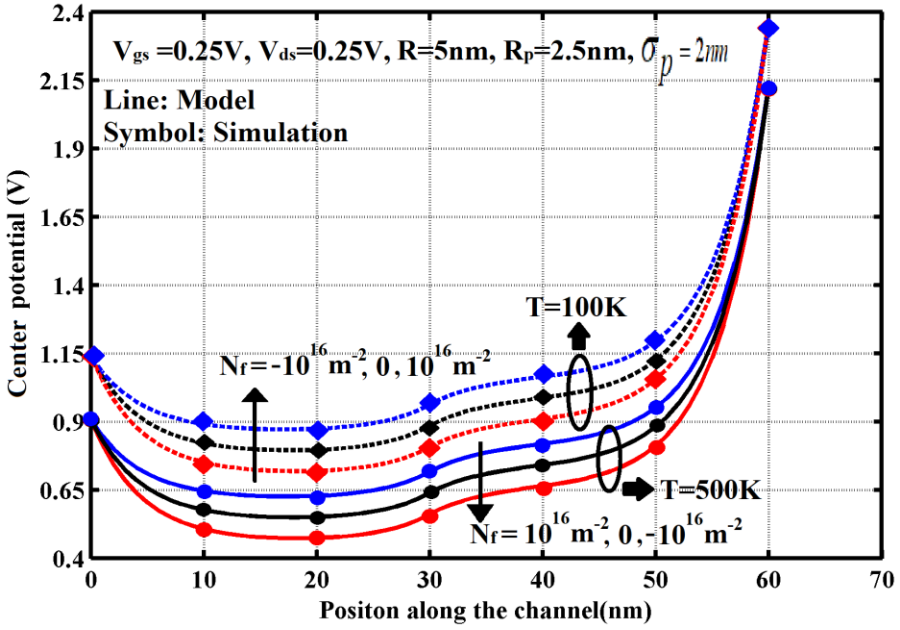


Fig. 3.2 Center potential distribution vs. channel position for the proposed device for an implant dose of Q=10^{16}/m^2 with and without fixed interface trapped charges and for T=100K and 500K

channel barrier height which results in higher threshold voltage. As the value of Projected range decreases and goes to 0, the peak doping gradually moves towards the center causing an augmented threshold voltage. This rationalizes the fact that threshold voltage elevates

with increase in doping at channel center and with a decrease in Projected range. When Rp = 5 nm, peak doping moves away from the center causing the source-channel barrier height to reduce which consequently reduces the threshold voltage. Thus reduction in threshold voltage occurs when the Projected range increases.

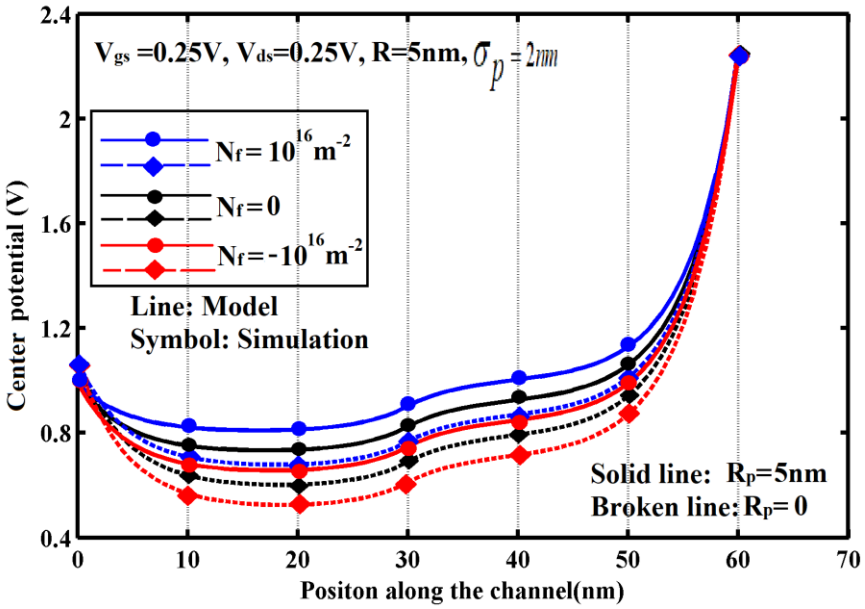


Fig.3.3 Center potential distribution along different channel positions for two different values of Projected Range

The influence of temperature on threshold voltage (V_{thr}) of both damaged and undamaged device for two sets of Gaussian doping parameters and channel radius is illustrated in fig.3.4. For both the set of Gaussian parameters, threshold voltage is found to decrease with increase in temperature. The source-channel barrier height being reduced for positive trap charges, threshold voltage is also diminished compared to the case for negative trap charges. While, for negative trap charges, higher source-channel barrier height causes an enhanced threshold voltage. For a radius R = 5 nm, the gate control being robust and since the Projected range is 2.5nm, the peak doping being near to the center, threshold voltage increases for a straggle of 2nm. For R=10nm, gate –channel coupling gets weakened compared to the case with R=5nm. Also, projected range being 5nm, peak doping moves away from channel center causing the threshold voltage to decrease for a straggle of 3nm. However, the decrease of threshold voltage with temperature is much stable for R=5nm, Projected range=2.5nm and

straggle of 2nm compared to the case with R=10nm, Projected range of 5nm and straggle of 3nm. This can be easily comprehended from the roll-off (RO) plots of threshold voltage with temperature. For R = 10 nm, RO is greater indicating more temperature-dependent variability of V_{thr} when compared to the case for R = 5 nm. This suggests that V_{thr} reliability, in terms of temperature influence, can be obtained more with smaller channel radius due to increased gate control. It is to be noted that in both the cases of R =5nm/10 nm, Gaussian configuration is so chosen that Projected range is half of the radius for ease of result comparison. Fig. 3.5 highlights the impact of a lower density of fixed interface trapped charges ($N_f = -5, 5, -1, 1 \times 10^{15} m^{-2}$) on the threshold voltage of the device for different temperatures. The nature of plot follows the same trend for varying temperature as observed in Fig. 3.4. Now a lower density of trapped charges such as $N_f = -1, 1 \times 10^{15}\ m^{-2}$, has reduced impact on the flat-band voltage of the device. However, with the increase in the density of fixed interface trap charges from $N_f = -1, 1 \times 10^{15} m^{-2}$ to $N_f = -5, 5 \times 10^{15} m^{-2}$, the flat-band voltage gets considerably impacted and the greater the flat-band voltage inflection,

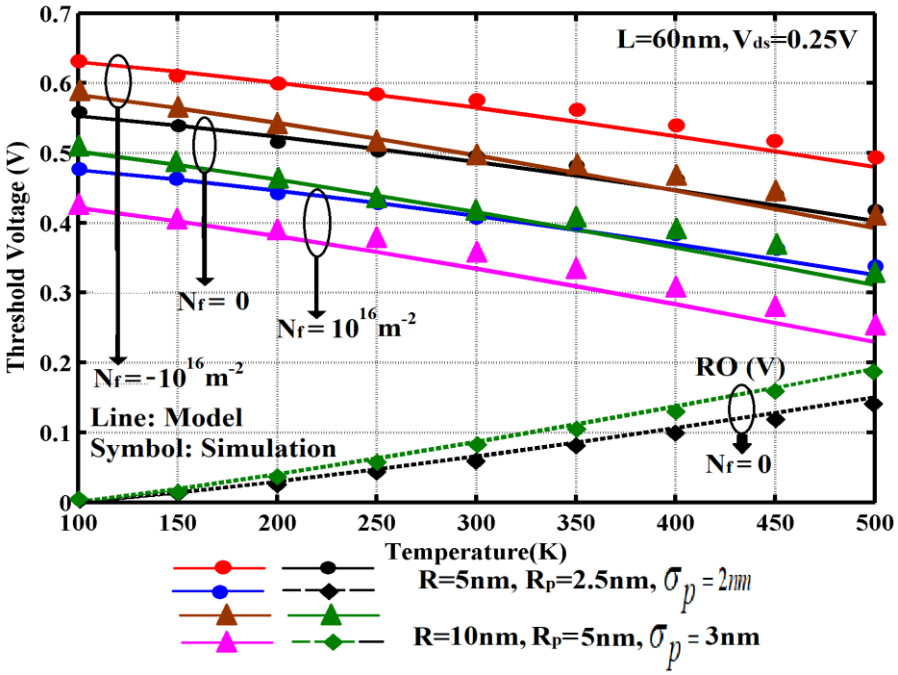


Fig.3.4 Threshold voltage variation vs. temperature for proposed device (both damaged & undamaged) and Roll-off with temperature for two different sets of Gaussian parameters and channel radius

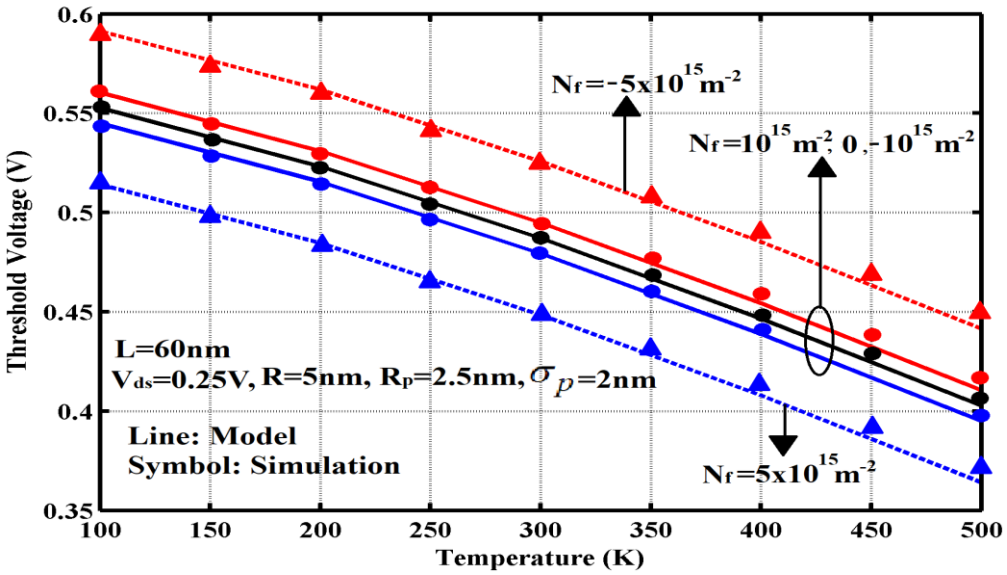


Fig.3.5 Threshold voltage versus Temperature for damaged (having lower density of fixed interface trapped charges) and undamaged device.

the higher is the source-channel height modulation and the greater is the shift (increase for negative trap charges and decrease for positive trap charges) of threshold voltage of the damaged device compared to the ideal/undamaged device. Variation of Gaussian parameters (Projected Range and straggle) on threshold voltage for both damaged and undamaged device is displayed in Fig. 3.6. Threshold voltage for positive, neutral and negative charges follow the same trend as depicted in Fig.3.4. Now, keeping the radius fixed at R = 5nm, V_{thr} is found to reduce with increase in Projected Range value which is obvious as per fig.3.3. With increase of Projected range from 0, peak doping shifts away from center leading to decreased source-channel barrier height in center potential thereby causing the threshold voltage to decrease. This justifies the plot in Fig. 3.6. Straggle parameter gives a measure of the profile spreading. As the straggle parameter elevates, the profile becomes more widely spread. Thus, the rate of decrease of threshold voltage with Projected range (Roll-Off in terms of Projected range) is much decreased for σ_p = 3nm compared to σ_p = 2nm. This implies that proper selection of Gaussian parameters can effectively improve performance reliability of the device thereby offering upgraded device performances. This is also exhibited and can be comprehended in the reported research by Goel et al. [3.28]. Fig.3.7 exhibits the graphical illustration of threshold voltage vs. channel length for both damaged and undamaged device

for two different values of implant doses. For a greater implant dose, threshold voltage increases due to an augmented source-channel barrier height in the center potential distribution. This is an established fact as reported in other researches as well [3.29]. Hence apt choice of implant dose aids reliable tuning of threshold voltage to a preferred value. The Subthreshold Swing (SS) variation for different channel length at different temperatures for proposed, undamaged device is plotted in Fig. 3.8. It can be observed that high SS escalations occur with increase in temperature. For greater channel lengths, SS attains nearly 100mV/dec at T = 500 K whereas it gets considerably diminished, about 20mV/dec for T = 100 K. However, for T = 300 K, SS attains a value of about 60mV/dec (the ideal value for short channel MOSFETs at T=300K) for channel lengths 40 nm or above. At diminished temperatures, the rate of impact ionization is lower compared to that at escalated temperatures and this aids in improved subthreshold characteristics that in turn improves SS of the device at lower temperatures.

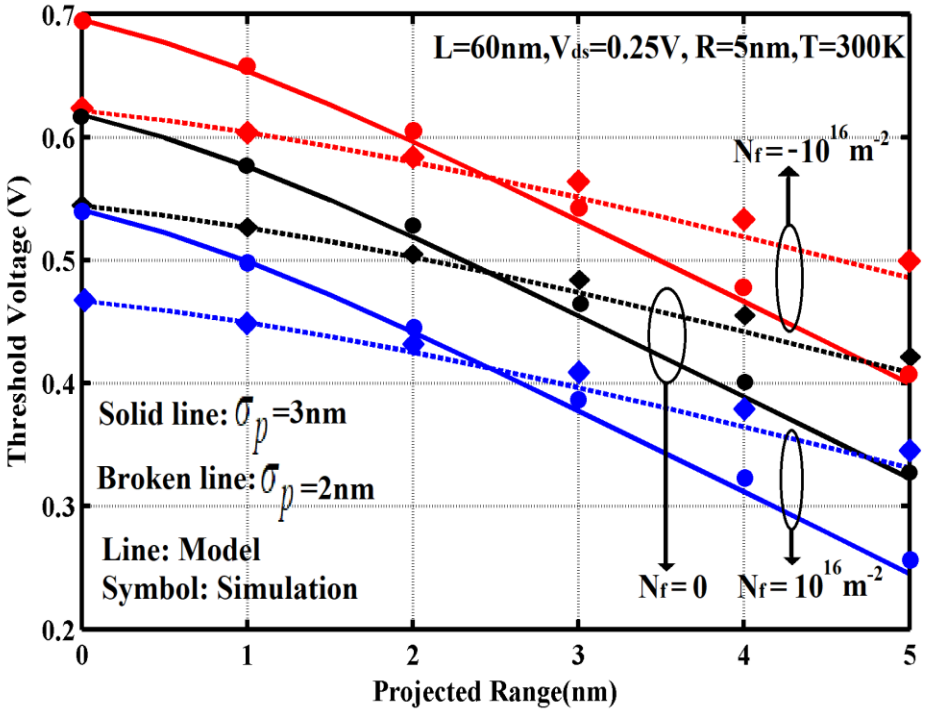


Fig.3.6 Threshold voltage vs. Projected Range for both damaged and undamaged device for two different straggle parameters

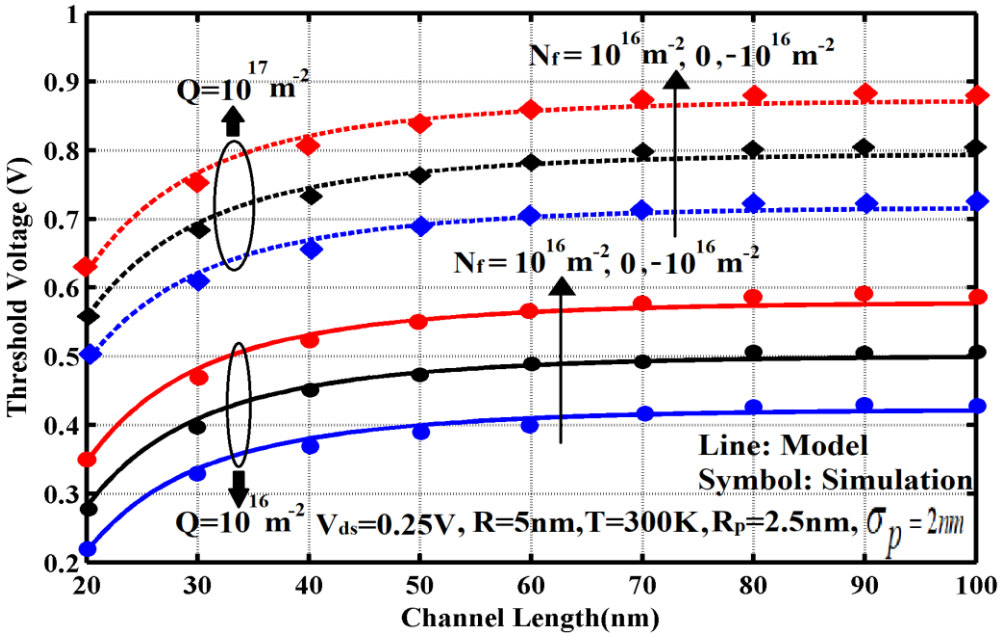


Fig.3.7 Threshold voltage vs. channel length for both damaged and undamaged device for two different values of implanted dose (Q)

Graphical illustration of SS vs. channel length for two different channel radius values and at two different Projected range values is demonstrated in Fig.3.9. With increase in channel radius from 5nm to 7nm, SS value significantly increases for channel lengths lower than 30nm. When the channel radius is increased, gate-channel coupling gets weakened since the gate gradually loses control over the channel thereby resulting in higher SS. However, in both the cases, when Projected range increases from Rp=0 to Rp=5nm, SS increases. At Rp=0, the peak doping is located at the channel center. As a result, the source-channel barrier height increases in center potential which enhances the threshold voltage and suppresses subthreshold leakages thereby improving the device characteristics. A shift of peak doping from center results in lower source-channel barrier height in center potential thereby causing the threshold voltages to get lowered leading to increased subthreshold leakages. Fig.3.10 demonstrates the graphical exploration of DIBL variation for different channel lengths of the proposed, undamaged device and its Single-Material Gate (SMG, without GWFE) contemporary. The center potential distribution of the GWFE incorporated, proposed device possesses a unique step profile that screens the minimum from getting affected from drain voltage alterations. Thus, even when the drain bias is increased, minimum remains

unaffected, source-channel barrier height remains unaltered and the threshold voltage lowering does not occur. This allows high resistance to DIBL. GWFE being absent in SMG architecture, the SMG configuration is highly prone to DIBL.

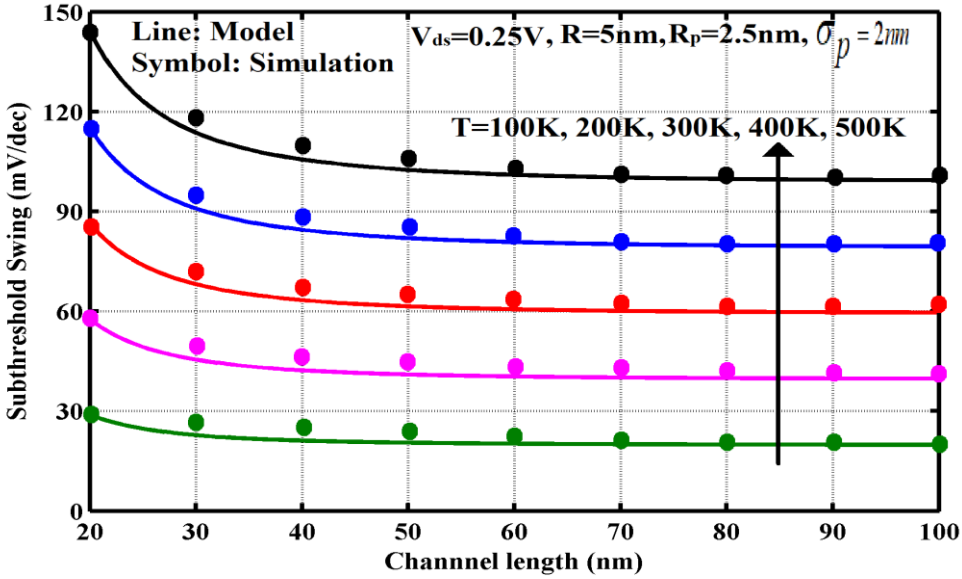


Fig.3.8 Subthreshold Swing vs. channel length for proposed, undamaged device at different temperatures

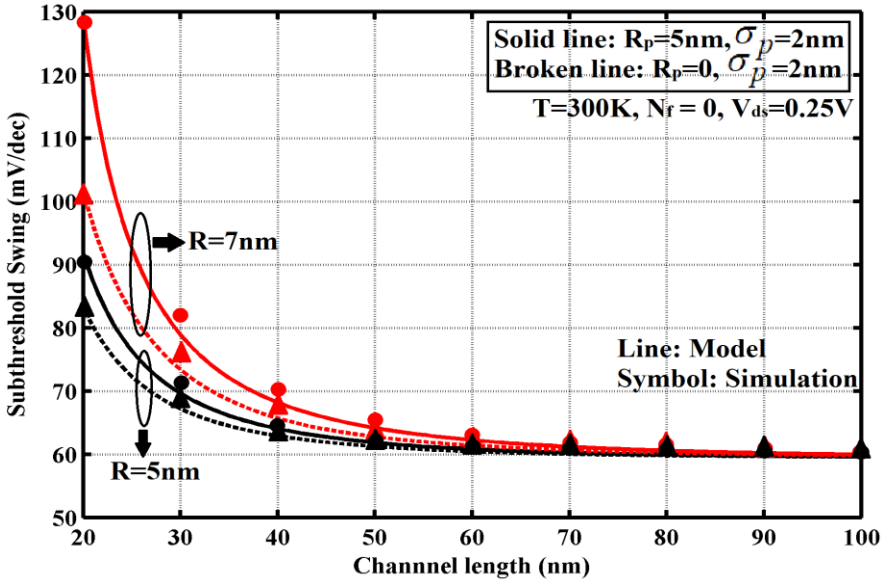


Fig.3.9 Subthreshold Swing vs. Channel length for proposed, undamaged device for two different Projected Range values and two values of channel radius.

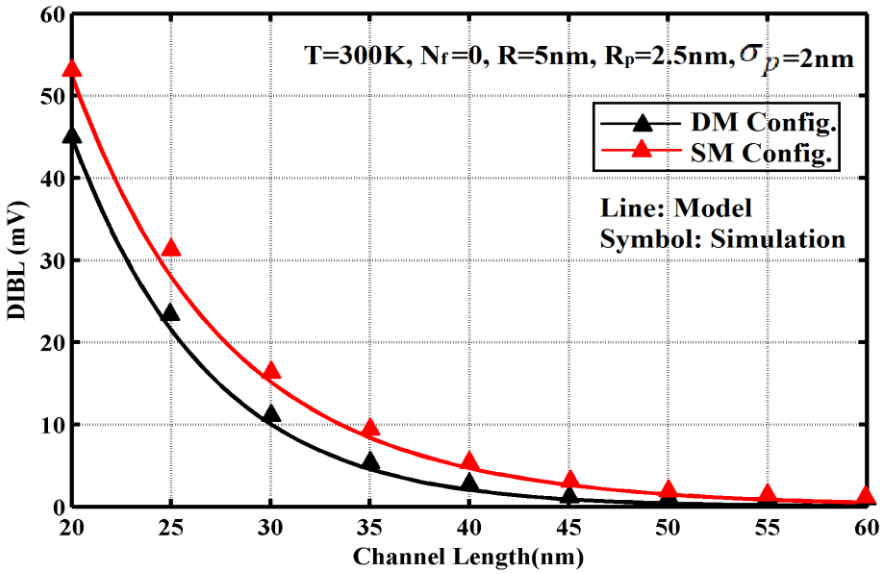


Fig.3.10 DIBL variation for different channel lengths for the proposed, undamaged device and its Single-Material Gate (SMG) Counterpart

Lateral Electric field distribution along different channel positions of both damaged and undamaged, proposed device and its SMG damaged and undamaged counterparts is plotted in Fig.3.11 (a) - 3.11(c). For all three cases, the DM configuration possesses a reduced electric field at drain end and a peak at the interface of two dissimilar materials. The center potential distribution in the proposed (damaged and undamaged) device has a reduced slope towards drain end due to GWFE. This weakens the HCE in the device. Secondly, work function engineering leads to the formation of a peak at the interface of two dissimilar materials giving a major boost to the transport efficiency in the proposed device. SM configuration being devoid of GWFE suffers from increased electric field at drain end leading to aggravated HCE in the device.

The analytical results are validated through simulation outputs from Atlas.

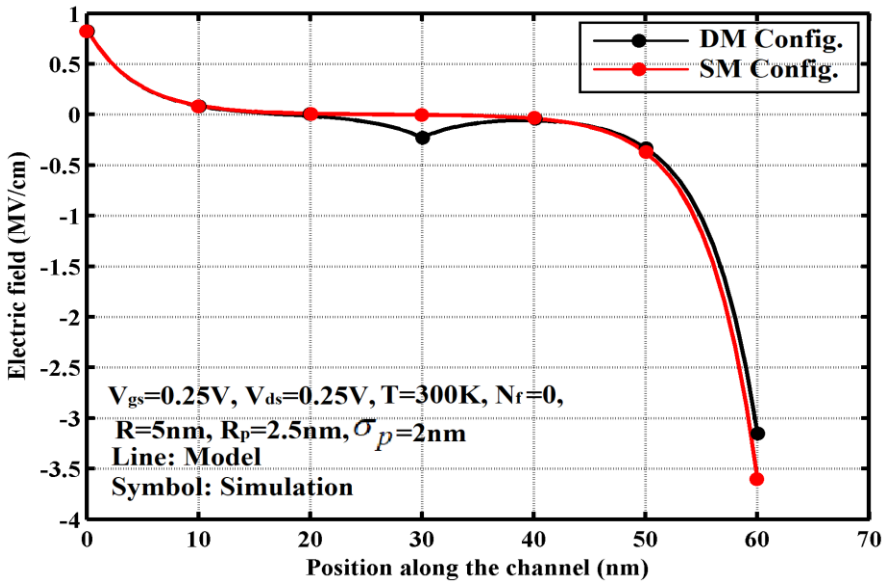


Fig.3.11 (a)

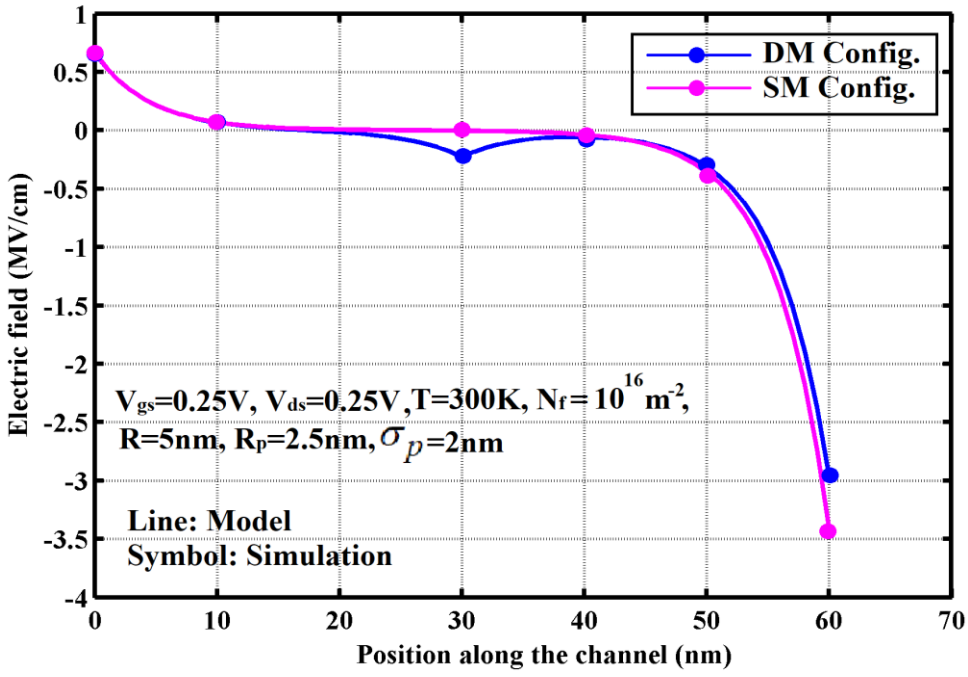


Fig.3.11 (b)

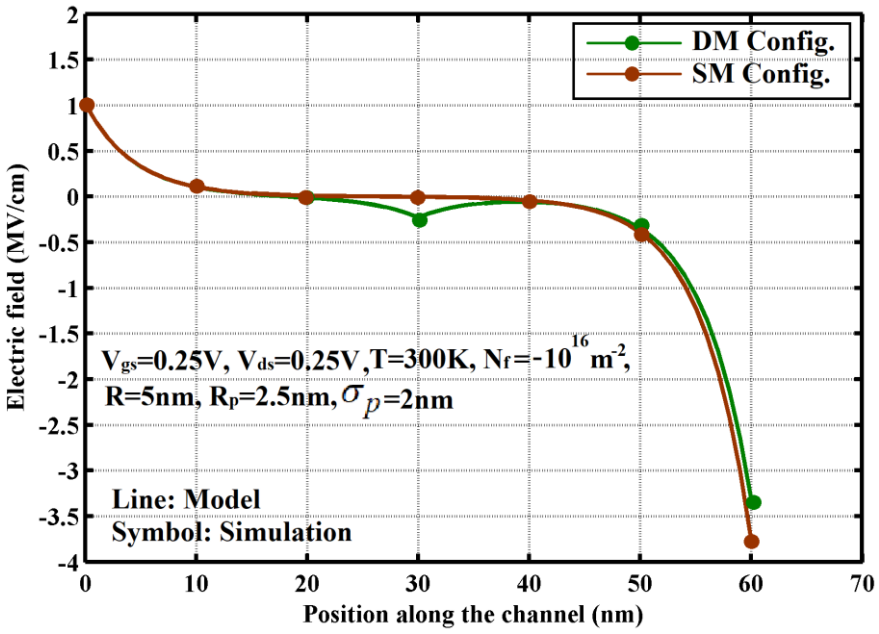


Fig.3.11 (c)

Lateral Electric Field Distribution along channel position for DM and SM Device Config. for (a) undamaged, (b) positive trap charges and (c) negative trap charges.

3.5. Conclusion

The current research mainly emphasizes the mathematical modeling encompassing the formulation of the threshold voltage of a Dual work function Material Cylindrical Gate-all-around MOSFET characterized with a channel having vertical Gaussian-doping, in presence/absence of fixed interface trap charges, in a varying thermal environment. Consequences of variation of Gaussian parameters, interface trap charges (& density) and temperature on the threshold voltage have been thoroughly explored. Gaussian parameter variations such as Projected Range alterations modulate the source-channel barrier heights of center potential thereby impacting the threshold voltage, whereas, careful choice of straggle parameter value can effectually control the performance worsening threshold voltage roll-off. Interface trap charges, whether positive or negative, inexorably alter the device flat-band voltage that causes considerable changes in threshold voltage. Further, graphical demonstrations of device characteristics in a varying temperature environment delivers comprehensive particulars of the thermal-dependence of device performance

reliability. In addition, a brief short channel effect investigation has also been highlighted that inspects the DIBL, Subthreshold Swing and Hot Carrier Effect based-behavior of the Gaussian-doped device. Comparative exploration of features of the device and its Gaussian-doped Single Material Gate complement reveals the former's enriched and trustworthy performance reliability over the latter. Simulation outputs from Atlas further validate the center-potential based mathematical model.

Relevant Publication

Pritha Banerjee and Jayoti Das, "Threshold Voltage Modeling of Gaussian-doped Dual work function Material Cylindrical Gate-All-Around (CGAA) MOSFET considering the effect of temperature and Fixed Interface Trapped Charges", **Microelectronics Journal, Elsevier**, Volume 120, February 2022, 105354, DOI: 10.1016/j.mejo.2021.105354 [SCIE, IF: 1.605]

References

[3.1] M.A. Abdi, F. Djeffal, Z. Dibi, D. Arar, "A two dimensional analytical subthreshold behavior analysis including hot-carrier effect for nanoscale Gate Stack Gate All Around (GASGAA) MOSFETs", J. Comput. Electron. 10, 179–185, 2011

[3.2] Amit Agarwal, Raushan Tiwari, Shreya Ranjan, P.C. Pradhan and B.P. Swain, "2D Analytical Modeling of Surface Potential for GaAs based Nanowire Gate All Around MOSFET", IOP Conf. Series: Materials Science and Engineering 377 (2018) 012103 doi:10.1088/1757-899X/377/1/012103

[3.3] Biswajit Ray and Santanu Mahapatra, "Modeling and Analysis of Body Potential of Cylindrical Gate-All-Around Nanowire Transistor", IEEE Transactions on Electron Devices, Vol. 55, NO. 9, September 2008

[3.4] El Hamid, Hamdy Abd; Iñiguez, Benjamin; Kilchytska, Valeria; Flandre, Denis; Ismail, Yehea , "An analytical 3D model for short-channel effects in undoped FinFETs", Journal of Computational Electronics, 14(2), 500–505, 2015 doi:10.1007/s10825-015-0678-0

[3.5] Susan C. Vitkavage and Eugene A. Irene, "An investigation of Si-SiO2 interface charges in thermally oxidized (100), (110), (111), and (511) silicon", Journal of Applied Physics 68, 5262 (1990)

[3.6] N. Garg, Y. Pratap, M. Gupta and S. Kabra, "Analysis of Interface Trap Charges of Double Gate Junctionless Nanowire Transistor (DG-JNT) for Digital Circuit Applications," 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 2018, pp. 563-567, doi: 10.1109/EDKCON.2018.8770427

[3.7] Saha, P., Banerjee, P., Dash, D.K. et al., "Interface Trap Charge Induced Threshold Voltage Modeling of WFE High-K SOI MOSFET", Silicon 12, 2893–2900, 2020 https://doi.org/10.1007/s12633-020-00386-5

[3.8] Nilesh Anand Srivastava, Anjali Priya, Ram Awadh Mishra, "Interface trap charge-based reliability assessment of high-k dielectric-modulated nanoscaled FD SOI MOSFET for low

power digital ICs: Modeling and simulation", Superlattices and Microstructures, Volume 154, 2021, 106871

[3.9] Gautam, Rajni; Saxena, Manoj; Gupta, R.S.; Gupta, Mridula, "Temperature dependent subthreshold model of long channel GAA MOSFET including localized charges to study variations in its temperature sensitivity' Microelectronics Reliability, 54(1), 37–43, 2014, doi:10.1016/j.microrel.2013.09.014

[3.10] V.S Lysenko; I.P Tyagulski; Y.V Gomeniuk; I.N Osiyuk, "Effect of oxide–semiconductor interface traps on low-temperature operation of MOSFETs", 40(4-5), 735–738, 2000 doi:10.1016/s0026-2714(99)00295-4

[3.11] Baral, Biswajit; Das, Aloke Kumar; De, Debashis; Sarkar, Angsuman, "An analytical model of triple-material double-gate metal-oxide-semiconductor field-effect transistor to suppress short-channel effects", International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2014, doi:10.1002/jnm.2044

[3.12] Das, S.K., Biswal, S.M., Swain, S.K., Baral, B., "Analysis of Junction-Less Triple-Material Cylindrical Surrounding Gate MOSFET.", In: Gunjan, V., Garcia Diaz, V., Cardona, M., Solanki, V., Sunitha, K. (eds) ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management. ICICCT 2019. Springer, Singapore. 2020, https://doi.org/10.1007/978-981-13-8461-5_92

[3.13] Menaria, Asmita; Pandey, Rahul; Kumar, Ramesh, "An investigation on a triple material double gate cylindrical gate all around (TMDG-CGAA) MOSFET for enhanced device performance", Materials Today: Proceedings, S2214785320335781–, 2020, doi:10.1016/j.matpr.2020.04.899

[3.14] Rewari, Sonam; Nath, Vandana; Haldar, Subhasis; Deswal, S. S.; Gupta, R. S. "Novel design to improve band to band tunneling and gate induced drain leakages (GIDL) in cylindrical gate all around (GAA) MOSFET", Microsystem Technologies, 2017, doi:10.1007/s00542-017-3446-1

[3.15] Fortunato Pezzimenti; Hichem Bencherif; Giuseppe De Martino; Lakhdar Dehimi; Riccardo Carotenuto; Massimo Merenda;Francesco G. Della Corte; "Study and Assessment of Defect and Trap Effects on the Current Capabilities of a 4H-SiC-Based Power MOSFET" Electronics, 2021, doi:10.3390/electronics10060735

[3.16] M.A. Abdi, F. Djeffal, Z. Dibi, D. Arar, "A two dimensional analytical subthreshold behavior analysis including hot-carrier effect for nanoscale Gate Stack Gate All Around (GASGAA) MOSFETs", J. Comput. Electron. 10, 179–185, 2011

[3.17] Toshikazu Mukaiyama; Ken-ichi Saito; Hiroki Ishikuro; Makoto Takamiya; Takuya Saraya; Toshiro Hiramoto, "Fabrication of gate-all-around MOSFET by silicon anisotropic etching technique" , 42(7-8), 1623–1626, 1998 doi:10.1016/s0038-1101(98)00082-3

[3.18] G. Zhang, Z. Shao and K. Zhou, "Threshold Voltage Model of Short-Channel FD-SOI MOSFETs With Vertical Gaussian Profile," in IEEE Transactions on Electron Devices, vol. 55, no. 3, pp. 803-809, March 2008, doi: 10.1109/TED.2007.914832.

[3.19] Sood, Himangi; Srivastava, Viranjay M.; Singh, Ghanshyam, "Performance analysis of undoped and Gaussian doped cylindrical surrounding-gate MOSFET with it's small signal modeling", Microelectronics Journal, 57, 66–75, 2016 doi:10.1016/j.mejo.2016.10.001

[3.20] S. Preethi;M. Venkatesh;M. Karthigai Pandian;G. Lakshmi Priya; "Analytical Modeling and Simulation of Gate-All-Around Junctionless Mosfet for Biosensing Applications", Silicon, 2021, doi:10.1007/s12633-021-01301-2

[3.21] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," in IEEE Transactions on Electron Devices, vol. 36, no. 2, pp. 399-402, Feb. 1989, doi: 10.1109/16.19942.

[3.22] Preethi, S.; Balamurugan, N. B, "Analytical Modeling of Surrounding Gate Junctionless MOSFET Using Finite Differentiation Method", Silicon, 2020, doi:10.1007/s12633-020-00653-5

[3.23] A. Goel, S. Rewari, S. Verma and R. S. Gupta, "Temperature-Dependent Gate-Induced Drain Leakages Assessment of Dual-Metal Nanowire Field-Effect Transistor—Analytical

Model," in IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2437-2445, May 2019, doi: 10.1109/TED.2019.2898444

[3.24] Ganapati, R., Samoju, V.R. & Jammu, B.R. "Analytical Modeling of Threshold Voltage for Dual-Metal Double-Gate Gate-All-Around (DM-DG-GAA) MOSFET", Silicon 13, 2869–2880, 2021. https://doi.org/10.1007/s12633-020-00602-2

[3.25] K. Liu and Y. Hsieh, "Investigation of the dimension effects of 30-nm below multiple-gate SOI MOSFETs by TCAD simulation," The 4th IEEE International Nanoelectronics Conference, 2011, pp. 1-2, doi: 10.1109/INEC.2011.5991679.

[3.26] Goel, E., "Impact of High-K Gate Stack on Subthreshold Performance of Double-Gate (DG) MOSFETs", Silicon, 2022, https://doi.org/10.1007/s12633-022-01891-5

[3.27] Suddapalli, S.R., Nistala, B.R., "A center-potential-based threshold voltage model for a graded-channel dual-material double-gate strained-Si MOSFET with interface charges", J Comput Electron 18, 1173–1181, 2019, https://doi.org/10.1007/s10825-019-01377-5

[3.28]Goel, E., Singh, B., Kumar, S. et al. Analytical threshold voltage modeling of ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs. Indian J Phys 91, 383–390 (2017). https://doi.org/10.1007/s12648-016-0918-6

[3.29] Sarvesh Dubey, Pramod Kumar Tiwari, S. Jit, A two-dimensional model for the potential distribution and threshold voltage of short-channel double-gate metal-oxide-semiconductor field-effect transistors with a vertical Gaussian-like doping profile, J. Appl. Phys. 108 (2010), 034518, https://doi.org/10.1063/1.3460796

Chapter 4

Chapter 4: GWFE Graded Channel Macaroni MOSFET: Analytical Modeling and Simulation of Temperature & Localized Trap Charge induced Device Characteristics including GIDL Current

---

4.1. Introduction

Researchers, over the decades, have introduced various innovative strategies that contribute to significantly boost the device performance through improved gate-channel coupling. The better the coupling, the more minimized the short channel effects in the device that assists higher speed, reduced power consumption, improved scalability etc. Noteworthy performance amelioration has been achieved by suitable implementation of the pioneering technology of Gate Work Function Engineering (GWFE) Scheme as already discussed in the previous chapters. Apart from GWFE scheme, various novel schemes are being tactically implemented for refinements or rectifications of some targeted SCEs and to selectively boost specific device characteristics. One such scheme, which falls under the channel engineering technology, is the implementation of graded channel in advanced MOSFET devices. In this scheme, the channel region towards the source has a high doping concentration whereas the channel region near the drain has a lower doping concentration. The high doping concentration towards the source causes the source-channel barrier height to increase thereby increasing the threshold voltage. This not only allows reduced off-state leakages and diminished power consumption but also offers the flexibility to tune the threshold voltage to a preferable value by selecting suitable doping concentration towards the source [4.1]. The low doping towards the drain effectively reduces impact ionization thereby permitting better resistance to SCEs like parasitic BJT effect.

When it comes to improved gate-channel coupling, another ground-breaking technology namely the Multi-gate MOSFET has been the prime technology that single-handedly suppress major SCEs and offer superior device performance. A type of Multi-gate namely Cylindrical Gate-all-around (CGAA) structures have been the foremost choice of the researchers since these devices offer excellent SCE immunization coupled with lower power consumption, higher packaging density, better current driving capability and reduced leakage issues. The fabrication feasibility of CGAA MOSFETs with circular cross-sections are already discussed in chapter 3.

However, Cylindrical GAA MOSFET, especially the ones with Macaroni channel architecture plays a pivotal role in significantly suppressing the SCE

deterrents and propel better gate-channel coupling. Macaroni channel GAA MOSFETs are topologically identical with the CGAA MOSFETs with the only exception that, in Macaroni MOSFETs, that the channel center has a hollowed pillar filled with dielectric. Thus the channel is thinner enabling superior gate control. Also, due to the presence of the hollow pillar, the field lines from drain penetrate in a smaller region into the channel. This contributes to better device performance, upgraded subthreshold characteristics, minimized power consumption, enhanced scalability etc.

Till date, CGAA MOSFETs have been highly preferable for their implementation to work as a biosensor enabling easy label-free detection of both neutral and charged biomolecules. However, since Macaroni GAA MOSFETs have outclassed the CGAA MOSFETs in terms of offering advanced and significantly improved device performance, hence the former structures are ideal replacements of the CGAA MOSFET devices in practical applications such as label-free biosensing. However, before the planned advanced Macaroni channel GAA MOSFET can be employed in real-time applications such as biosensing, the electrical characteristics of the device has to be investigated in detail so as to assure its successful implementation in biosensing applications.

In addition to this, device performance has been analyzed by considering a graded channel doping concentration. Research on performance reliability of the above projected device has been conducted by considering the thermal characterization in a temperature varying environment of 100K – 500K and interface trapped charge based reliability has been tested additionally. Comparative studies of the damaged and undamaged device exhibits the necessity of fixed interface trap charge modelling in the device, also the impact of these charges on the thermal behavior of the device has been comprehensively presented in the following section.

4.2. Overview

Macaroni-architecture MOSFETs are increasingly gaining popularity nowadays as superior replacements of Full-channel CGAA MOSFETs having radius same as the outer radius of the Macaroni configuration. Macaroni MOSFETs are not only fabrication feasible but are characterized with inherent capability of high resistance to major SCEs. Incorporation of

GWFE in Macaroni MOSFETs can further upgrade the device characteristics thereby contributing a boost to the device performance. Benefits of graded channel have already been discussed earlier and is thus skillfully incorporated in the current research also.

For multiple times, researchers have explained the detailed fabrication steps of macaroni channels in their reported researches. Delhougne et al. [4.2], for the first time, demonstrated the step by step fabrication of monocrystalline silicon macaroni channel device. First the cylindrical hole is formed by dry etching, then the ONO stack layer is deposited by LPCVD. This is subsequently followed by the deposition of an amorphous silicon (a-Si) protection layer in a vertical furnace. Then the ONO and the protection layer are etched anisotropically for opening the bottom of the created hole, while the ONO remains protected at the sidewalls. An a-Si sacrificial layer is then deposited as dummy channel. The a-Si bottom opening etch has to be sufficiently long to ensure atleast 50nm recess in the substrate. This recess enables to strongly anchor the central oxide pillar used as template during EPI growth. The remaining of the hole is filled with PEALD oxide followed by a controlled recess to uncover the top of the sacrificial dummy channel. The channel replacement processing was performed in an Intrepid XPTM RPCVD epi cluster from ASM by the authors. Then the removal of the native oxide is conducted at low temperature. The sacrificial a-Si is etched with Cl_2 at 575 ºC for ~10 min down to the silicon substrate, forming typical [111] facets. The Cl_2 etch has to be carefully conducted to remove all a-Si but at the same time, any undercut of the oxide pillar has to be avoided. The subsequent selective epitaxial Si regrowth was done at 810 ºC for ~15 min using a conventional $SiCl_2H_4$/HCl process. Top Drain contact is then formed by using doped polysilicon followed by staircase patterning, passivation, metallization and finally forming gas anneal. Hence, the published research provided a clear idea about the detailed step by step fabrication of the Macaroni channel devices.

Graded channel in MOSFETs are fabrication feasible. Pavanello et al. [4.3] has highlighted the technological aspects of graded channel fabrication having high doping towards source side only and with natural doping towards drain side. In this process, after the gate-oxide of preferable thickness is grown, the threshold voltage ionic implantation is carried out using

photolithography for necessary adjustment of this implantation in the Graded channel devices and keep the region near the drain with natural doping. After gate patterning, the source, drain regions are formed by arsenic ionic implantation and thermal annealing. However Ma et al. [4.4], in their reported research, mentioned the detailed fabrication process of bilateral graded channel devices where the region towards the drain is doped at a low concentration. In such a case, the threshold voltage adjust implant is replaced by the graded channel implantation. The GC implant has generally a shallower profile to control the threshold voltage so addition threshold voltage adjust implant is no more necessary. Thus, using the detailed fabrication methods explained in the above reference, graded channel in MOSFET can be fabricated with the state-of-the-art technologies and has been one of the prime technologies for performance upgradation in advanced MOSFET devices. The technology has been explored in detail in the following research and its role has been precisely highlighted in rectification and improvement of device characteristics.

In the following research, a Dual-Material Gate Macaroni MOSFET has been considered and its thermal and localized/fixed interface trap charge induced electrical characteristics have been analyzed in detail. Fabrication feasibility of Dual-Material gate has already been discussed in chapter 2. Recently, several leakage mechanisms are being thoroughly investigated since leakage mechanisms increase the power consumption of the device and make it unsuitable for low power applications. Power dissipation issues are major concern in ultra-scaled devices and this also turns the device hot. Gate-induced drain leakage (GIDL) is one such leakage mechanism [4.5-4.6]. With a positive drain voltage and near zero or negative gate voltage, the region near the n+ drain becomes depleted. Heavy doping of drain causes the depletion region to become narrower. This results in crowding of the field lines in the vicinity of the drain causing electrons tunneling into the drain. While, holes from drain tunnel into the channel creating a path for Off-state GIDL current. In the current research, the drain current has been modeled considering the GIDL effects.

4.3. Analytical Modeling

Macaroni MOSFET is basically a Cylindrical Gate-all-around MOSFET with a hollow pillar of insulator (filler) along the channel center. The schematic 3-D and 2-D representations of the

projected device is shown in Fig.4.1-4.3. The gate consists of material M_S with work function 4.6eV (gate length L_1=30nm) placed towards the source and material M_D with work

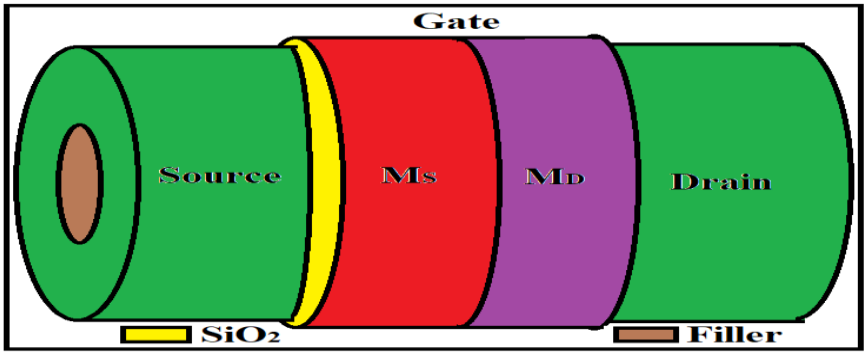


Fig.4.1 Diagrammatic 3-D illustration of proposed device

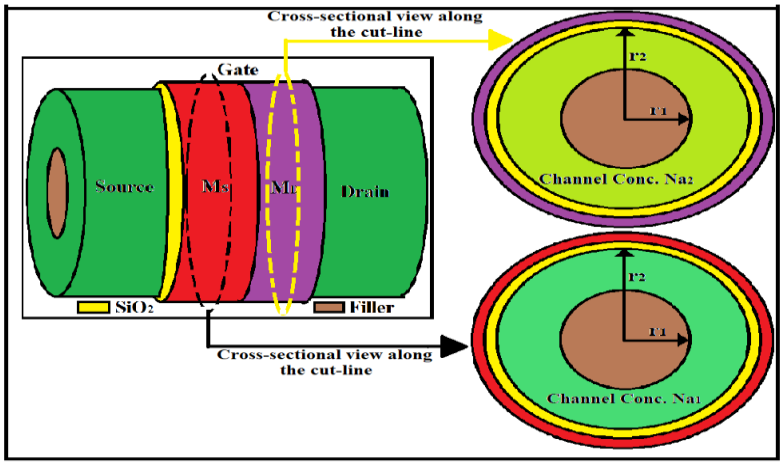


Fig.4.2 2-D cross-sectional view of proposed device along the cut-lines

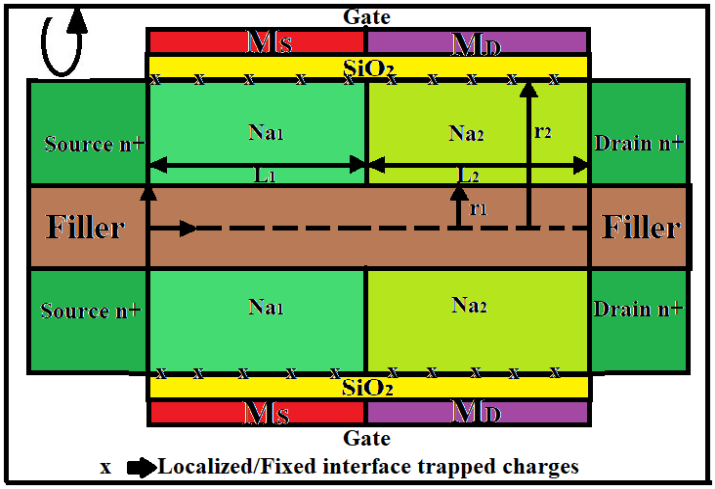


Fig.4.3 Cross-sectional view of the proposed device for mathematical modeling

function 4.4eV (gate length L_2=30nm) placed towards the drain. Channel length is L (=L_1+ L_2) is 60nm. Channel thickness is denoted by $t_{Si}=2(r_2-r_1)$ where r_2 (=15nm) is the outer radius of the channel and filler radius is r_1 (=10nm). Gate oxide (SiO_2) has thickness t_{ox}=2nm.

4.3.1. Inner Potential Modeling

The temperature-dependent parameters are listed as follows [4.7]:

$$E_g(T) = E_g(300) + E_{g\alpha}\left(\frac{300^2}{300+E_{g\beta}} - \frac{T^2}{T+E_{g\beta}}\right) \tag{4.1}$$

Here, $E_g(T)$ denotes the temperature-dependent bandgap of silicon, $E_g(300) = 1.08eV, E_{g\alpha} = 4.73\times10^{-4} eV/K, E_{g\beta} = 636K$

The temperature-dependent intrinsic concentration is given as:

$$n_i(T) = (1.706\times10^{25}).\left(\frac{T}{300}\right)^{3/2}.\exp\left(\frac{-qE_g(T)}{2K_BT}\right) \tag{4.2}$$

The temperature-dependent permittivity of silicon is given as:

$$\varepsilon_{Si}(T) = \left(11.4+\left(1+\left(1.2\times10^{-4}\right)T\right)\right)\varepsilon_0 \tag{4.3}$$

In order to obtain an expression of the potential in the channel, the 3-D Poisson's equation needs to be solved. Since the channel potential does not vary along the radial plane (along θ), hence the 3-D Poisson's equation is now actually a 2-D Poisson's equation which is as follows [4.8]:

$$\frac{\partial^2\Psi_i(r,z)}{\partial r^2} + \frac{1}{r}\frac{\partial\Psi_i(r,z)}{\partial r} + \frac{\partial^2\Psi_i(r,z)}{\partial z^2} = \frac{qNa_i}{\varepsilon_{Si}(T)} \tag{4.4}$$

Where $\Psi_i(r,z)$ denotes the channel potential, i stands for the i^{th} region. The channel is divided into two regions, region 1 having boundaries $0 \le z \le L_1, r_1 \le r \le r_2$ with doping concentration $N_{a_1} = 1x10^{17} cm^{-3}$ and region 2 having boundaries $L_1 \le z \le L, r_1 \le r \le r_2$ with doping concentration $N_{a_2} = 1x10^{16} cm^{-3}$.

Now, the potential distribution in the channel is parabolic along the radius which yields [4.9]:

$$\Psi_i(r,z) = C_{1i}(z) + C_{2i}(z)r + C_{3i}(z)r^2 \tag{4.5}$$

Here, $C_{1i}(z), C_{2i}(z), C_{3i}(z)$ are z-dependent coefficients.

The boundary conditions required to evaluate the expressions of the above coefficients are listed as follows [4.10]:

$$\left.\frac{\partial \Psi_i(r,z)}{\partial r}\right|_{r=r_1} = C_{2i}(z) + 2r_1 C_{3i}(z) = 0 \tag{4.6}$$

This mathematically leads to:

$$C_{2i}(z) = -2r_1 C_{3i}(z) \tag{4.7}$$

$$\left.\frac{\partial \Psi_i(r,z)}{\partial r}\right|_{r=r_2} = C_{2i}(z) + 2r_2 C_{3i}(z) = \frac{C_{ox}}{\varepsilon_{Si}(T)}\left[V_{gs_i}{}' - \Psi_i(r_2,z)\right] \tag{4.8}$$

Here, $C_{ox} = \dfrac{\varepsilon_{ox}}{r_2 \ln\left(1+\dfrac{t_{ox}}{r_2}\right)}$, here ε_{ox} is the gate-oxide permittivity, $V_{gsi}{}' = V_{gs} - V_{fb_i}{}'$ where V_{gs} is the gate-to-source voltage, $V_{fb_i}{}' = V_{fbi} - \dfrac{qN_f}{C_{ox}}$, where V_{fbi} is the flat-band voltage for the ith region, $V_{fbi} = \left[\phi_{M_{S/D}}\left(=\phi_{M_{S\,for\,Reg.1}}\ or \phi_{M_{D\,for\,Reg.2}}\right)\right] - \phi_{Si_i}(T)$, N_f is the localized/fixed interface trapped charge density, $\phi_{Si_i}(T) = \chi + \dfrac{E_g(T)}{2} + \phi_{f_i}(T)$

Using the above stated boundary conditions, coefficient $C_{3i}(z)$ thus obtained is as follows:

$$C_{3i}(z) = \frac{4C_{ox}\left(V_{gsi}{}' - \psi_{0i}(z)\right)}{4\varepsilon_{Si}(T)t_{Si} + C_{ox}t_{Si}{}^2} \tag{4.9}$$

Here, $\psi_{0i}(z)$ is the inner potential at the channel-filler interface in the ith region.

Substituting the expressions (4.7) and (4.9) in (4.5) and then in (4.4), the differential equation thus obtained is as follows:

$$\frac{\partial^2 \psi_{0i}}{\partial z^2} + 2C_{3i}(z) = \frac{qNa_i}{\varepsilon_{Si}(T)} \tag{4.10}$$

General solution to equation (4.10) is given as:

In region 1:

$$\psi_{01}(z) = A\exp(z/\lambda) + B\exp(-z/\lambda) + \varphi_{01} \tag{4.11}$$

In region 2:

$$\psi_{02}(z) = C\exp((z - L_1)/\lambda) + D\exp(-(z - L_1)/\lambda) + \varphi_{02} \tag{4.12}$$

Here, $\varphi_{0i} = V_{gsi}{}' - \dfrac{qNa_i\lambda^2}{\varepsilon_{Si}(T)}$, $\lambda = \sqrt{\dfrac{4\varepsilon_{Si}(T)t_{Si} + C_{ox}t_{Si}{}^2}{8C_{ox}}}$

In order to evaluate the expressions of A, B, C, D, the boundary conditions need to be considered [4.11]:

$$\psi_{01}(z = 0) = V_{bi_1}(T) \tag{4.13}$$

Where $V_{bi_1}(T)$ is the built-in potential at the source-channel end.

$$\psi_{02}(z = L) = V_{bi_2}(T) + V_{ds} \tag{4.14}$$

Here, $V_{bi_2}(T)$ is the built-in potential at the drain-channel end, $V_{bi_1}(T) \neq V_{bi_2}(T)$ due to different channel grading concentrations at source and drain sides.

Potential in the channel is continuous at the interface of two dissimilar materials that yields:

$$\psi_{01}(z)\big|_{z=L_1} = \psi_{02}(z)\big|_{z=L_2} \tag{4.15}$$

Electric flux in the channel is continuous at the interface of two dissimilar materials that yields:

$$\left.\frac{\partial\psi_{01}(z)}{\partial z}\right|_{z=L_1} = \left.\frac{\partial\psi_{02}(z)}{\partial z}\right|_{z=L_1} \tag{4.16}$$

The coefficients' expressions thus obtained are as follows:

$$A = \alpha_1 + \beta_1 V_{gs} \tag{4.17}$$

$$B = \alpha_2 + \beta_2 V_{gs} \tag{4.18}$$

$$C = A\exp(L_1/\lambda) + \left(\frac{\varphi_{01} - \varphi_{02}}{2}\right) \tag{4.19}$$

$$D = B\exp(-L_1/\lambda) + \left(\frac{\varphi_{01} - \varphi_{02}}{2}\right) \tag{4.20}$$

Here,

$$\alpha_2 = \left[\frac{\left\{ (V_{bi_1}(T)\exp(L/\lambda)) - (V_{bi_2}(T) + V_{ds}) \right\} + S_{12}\cosh(L_2/\lambda) + \left(V_{fb_1}{}' + \frac{qNa_1\lambda^2}{\varepsilon_{Si}(T)} \right)\exp(L/\lambda) - \left(V_{fb_2}{}' + \frac{qNa_2\lambda^2}{\varepsilon_{Si}(T)} \right)}{2\sinh(L/\lambda)} \right],$$

$$\beta_2 = \left(\frac{1-\exp(L/\lambda)}{2\sinh(L/\lambda)} \right),\ \alpha_1 = \left(V_{bi_1} - \alpha_2 + V_{fb_1}{}' + \frac{qNa_1\lambda^2}{\varepsilon_{Si}(T)} \right),\ \beta_1 = -1-\beta_2,\ S_{12} = \varphi_{01} - \varphi_{02}$$

4.3.2. Threshold Voltage Modeling

The value of V_{gs} at which the inner potential minimum is equal to twice the Fermi potential $2\phi_{f_1}(T) = 2\frac{KT}{q}\ln\left(\frac{Na_1}{n_i(T)}\right)$, is termed as the threshold voltage. Thus the position of minimum inner potential can be obtained as follows:

$$\left.\frac{d\psi_{01}(z)}{dz}\right|_{z=z_{\min}} = 0 \tag{4.21}$$

Thus, $z_{\min} = \frac{\lambda}{2}\ln\left(\frac{B}{A}\right)$ (4.22)

Therefore, threshold voltage can be evaluated as follows:

$$\psi_{01\min} = 2\frac{KT}{q}\ln\left(\frac{Na_1}{n_i(T)}\right) \tag{4.23}$$

The expression of threshold voltage thus obtained is as follows:

$$V_{th} = \frac{-b-\sqrt{b^2-4ac}}{2a} \tag{4.24}$$

Here, $a = 4\beta_1\beta_2 - 1$, $b = 2\left[\left\{ 2(\alpha_1\beta_2 + \alpha_2\beta_1) + \left(2\phi_{f_1}(T) + V_{fb_1}{}' + \frac{qNa_1\lambda^2}{\varepsilon_{Si}(T)} \right) \right\} \right]$,

$$c = \left[4(\alpha_1\alpha_2) - \left(2\phi_{f_1}(T) + V_{fb_1}{}' + \frac{qNa_1\lambda^2}{\varepsilon_{Si}(T)} \right)^2 \right]$$

4.3.3. Short Channel Effect Modeling

DIBL (in mV) [4.12] is given as follows:

$$DIBL = V_{th_{linear}} - V_{th_{saturation}} \tag{4.25}$$

Subthreshold Swing (in mV/dec) [4.13] is given as:

$$SS = \frac{KT}{q}\left[\frac{d\psi_{01\min}}{dV_{gs}}\right]^{-1} \tag{4.26}$$

Hot Carrier Effect (HCE) [4.14] in the device can be analyzed from the lateral electric field distribution as follows:

$$E_{iz} = -\frac{d\psi_{0i}(z)}{dz} \tag{4.27}$$

4.3.4. Drain Current Modeling

A unified drain current modelling for different regimes of operation is expressed as [4.15]:

$$I_{ds} = \begin{bmatrix} I_{gidl}, -0.3 \le V_{gs} \le 0 \\ I_{sub,} 0 \le V_{gs} \le V_{th} \\ I_{lin}, V_{th} \le V_{gs} \le V_{sat} \\ I_{sat}, V_{sat} \le V_{gs} \le 1.0 \end{bmatrix} \tag{4.28}$$

Gate-induced drain leakage (GIDL) current is given as [4.16]:

$$I_{gidl} = A' E_i^{\,2}\left(0.5t_{Si}, L_1 + L_2\right)\exp\left(\frac{-B'}{E_i\left(0.5t_{Si}, L_1 + L_2\right)}\right) \tag{4.29}$$

Here, expressions/values of A', B' have been considered using [4.17].

Subthreshold Current within the limit $0 \le V_{gs} \le V_{th}$ is given as follows [4.18]:

$$I_{DS}(z) = \int_{r_1}^{r_2} 2\pi R J(r,z)\, dr \tag{4.30}$$

The diffusion current density is given as follows:

$$J(r,z) = \frac{\mu_n'}{1+\theta\left(V_{gs} - V_{THR}\right)} q n_i(T)\exp\left(\frac{\psi_{01\min} - V}{V_T}\right)\frac{dV(z)}{dz} \tag{4.31}$$

Where, $V_T = \dfrac{KT}{q}$

Substituting eq.(4.31) in (4.30), the equation thus obtained is as follows:

$$I_{DS}\int_0^L dz(z) = \frac{\mu_n'}{1+\theta\left(V_{gs} - V_{THR}\right)}\pi\left(r_2^{\,2} - r_1^{\,2}\right) q n_i(T)\int_0^{V_{ds}} \exp\left(\frac{\psi_{01\min} - V}{V_T}\right) dV(z) \tag{4.32}$$

Finally the expression for subthreshold drain current in the device is given as:

$$I_{DS} = \frac{\mu_n'}{1+\theta\left(V_{gs}-V_{THR}\right)}\pi\frac{\left(r_2^{\,2}-r_1^{\,2}\right)}{L}qn_i\left(T\right)\exp\left(\frac{\psi_{01\min}}{V_T}\right)V_T\left[1-\exp\left(-V_{ds}/V_T\right)\right] \tag{4.33}$$

Where, $\mu_n' = \frac{\mu_n}{\sqrt{\left(1+\frac{Na_1}{N_{ref}+Na_1S_1}\right)}}$, μ_n being the electron mobility, S_1, θ are fitting parameters.

Drain current in linear region is given as:

$$I_{lin} = \frac{2\pi\left(r_2-r_1\right)\mu_{eff}C_{ox}E_c}{\left(E_cL+V_{ds}\right)}\left[\left(V_{gs}-V_{ths}\right)^{\frac{\alpha}{2}}V_{ds}-\frac{\theta_{short}V_{ds}^{\,2}}{2}\right] \tag{4.34}$$

Where, E_c is the critical electric field for long channel device, $\alpha = 2$ to $\alpha = 1$ for short channel device, $\theta_{short} = \frac{0.1}{\left[\frac{d\psi_{01\min}}{dV_{gs}}\right]}$ at $V_{gs} = V_{th}$, $V_{ths} = V_{th}\left(1-\theta_{short}\right)$

Short channel effects have been incorporated using $E_c, \theta_{short}, V_{ths}$.

Saturation current is given as:

$$I_{sat} = \frac{2\pi\left(r_2-r_1\right)\mu_{eff}C_{ox}}{\left(1+\frac{V_{dsat}}{E_c(L-L_{sat})}\right)\left(L-L_{sat}\right)}\left[\beta\left(V_{gs}-V_{ths}\right)^{\frac{\alpha}{2}}V_{dsat}-\frac{\theta_{short}V_{dsat}^{\,2}}{2}\right] \tag{4.35}$$

Here V_{ds} is replaced using V_{dsat}, $V_{dsat} = V_{gs}-V_{ths}$. β is a technology dependent empirical parameter.

4.4. Results & Discussions

Several physics-based simulation models have been enabled as discussed in Section 3.4 to obtain the simulation outputs and subsequent verification of the analytical results. Fig.4.4 illustrates the Inner potential distribution of the proposed, damaged and undamaged device along the channel length for three different temperatures. For all the cases of thermal variation, an increment in the source-channel barrier height of the inner potential distribution is noted for negative trap charges compared to that with no trap charges (the Si-SiO_2 interface is an ideal one). This indicates a corresponding enhancement in the threshold voltage for negatively trapped charges at Si-SiO_2 interface compared to the ideal interface

case (for no traps). For positive trap charges, the source-channel barrier height reduces compared to the ideal interface case thus offering implications of diminished threshold voltage with positive trapped charges at the interface. Now, with gradual increase in temperature from 100K to 500K, the whole inner potential decreases. Influences of such a trend on threshold voltage of the device can be comprehended from threshold voltage plots exhibited in this section. Additionally, GWFE in the device has resulted in unique step profile formation in the channel at the junction of the different materials and this highly aids in suppressing major SCEs like drain-induced barrier lowering (DIBL) and hot carrier effect (HCE). Fig.4.5 (a) shows the inner potential variation for the proposed, damaged and undamaged device, for two different outer radii values (filler radius is fixed at 10nm). The device exhibits analogous behavior for positive, negative and zero trap charges as depicted in Fig.4.4. Now, with an outer radius equal to15nm, the step profile in the inner potential distribution becomes more prominent when compared to case with outer radius equal to 20nm. A more prominent step profile offers appreciable shielding effect from drain voltage alterations. Also, the inner potential minimum is found to be more moved towards the source when the outer radius is 15nm compared to the case when it is 20nm. Thus the inner potential minimum for outer radius 15nm gets highly protected from drain voltage variations and this is an extremely necessary feature which a device is anticipated to own. The cause for such a behavior is that, when filler radius is 10nm and outer radius is 15nm, the channel thickness is lesser and the extent of gate-channel coupling is substantial. For a configuration with an outer radius 20nm, the channel thickness gets increased and the gate – channel coupling weakens paving the path for major short channel effects (SCEs). Also, for an outer radius 15nm (compared to r_2=20nm), source-channel barrier height gets augmented which indicates a greater threshold voltage and lessened power dissipation caused by subthreshold leakages (as a result of increased gate-channel control). Fig.4.5 (b) illustrates inner potential distribution of the proposed, damaged and undamaged device for two different filler radii (outer radius fixed at 15nm). The device displays alike behavior for positive, negative and zero trap charges as depicted in Fig.4.4. The step profile is more noticeable for filler radius r_1=10nm compared to the case with r_1=5nm (for a fixed outer radius of r_2=15nm). For filler radius r_1=10nm, outer radius of r_2=15nm, the channel thickness shrinks causing enhanced gate control over the channel. This also consequences in

higher threshold voltage, reduced off-state leakages. Inner potential variation of the proposed device for various densities of positive and negative trap charges and also without trap charge is revealed in Fig.4.6. The plot is also presented for two different channel lengths, L=60nm and a scaled channel length, L=40nm. Inner potential for both the channel lengths displays that the source-channel barrier height considerably drops with enhancement in the positive trap charge density. This will lower the threshold voltage causing substantial off-state leakages. This will be thus accompanied by deterioration of the device performance as this augments power dissipation. Whereas, with negative trap charges density increment, the source-channel barrier height significantly increases that will substantially elevate the threshold voltage causing worsened circuit speed and amplified power consumption. Moreover, with the channel length being scaled down to 40nm, the source-channel barrier height is impacted, the height declines further leading to reduction of threshold voltage. Variation of Inner Potential along the channel positions of the proposed, undamaged device and its full channel Cylindrical Gate-All-Around (GAA) complement is displayed in Fig.4.7. The step profile in proposed device is much more prominent compared to its cylindrical

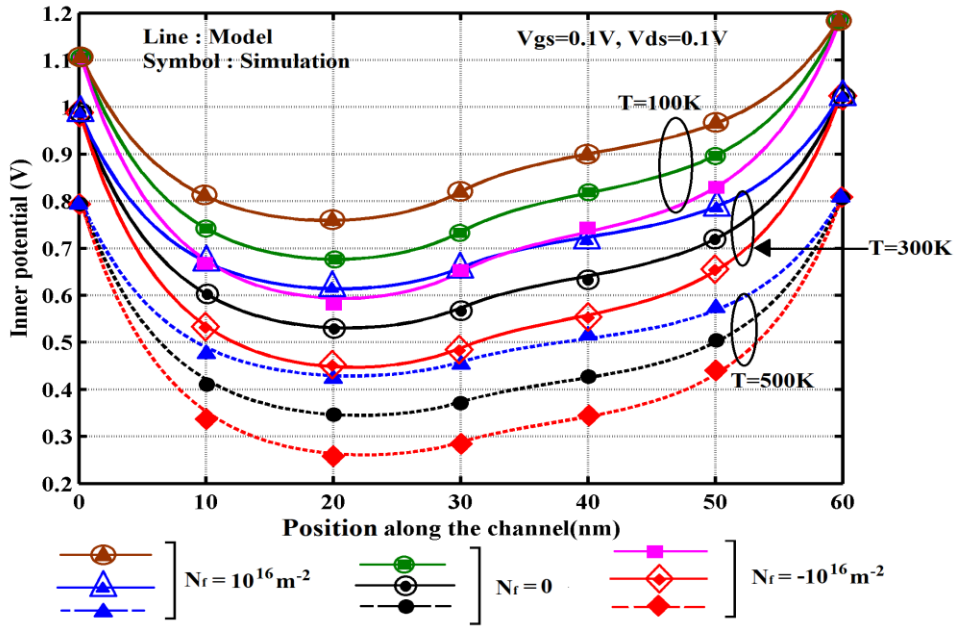


Fig. 4.4 Inner potential distribution along channel length of the proposed, damaged and undamaged device at different temperatures.

full channel counterpart. This inevitably leads to improved shielding effect to potential minimum from changing drain voltages in the proposed device that causes weakened SCEs

and enriched device performance. Also, the source-channel barrier height being larger in the proposed device (compared to the cylindrical complement), threshold voltage will be higher in the projected device causing lesser leakages and lessened off-state power dissipation. Fig.4.8 offers graphical demonstration of variation of threshold voltage of the damaged and undamaged configuration of the projected device for different temperatures.

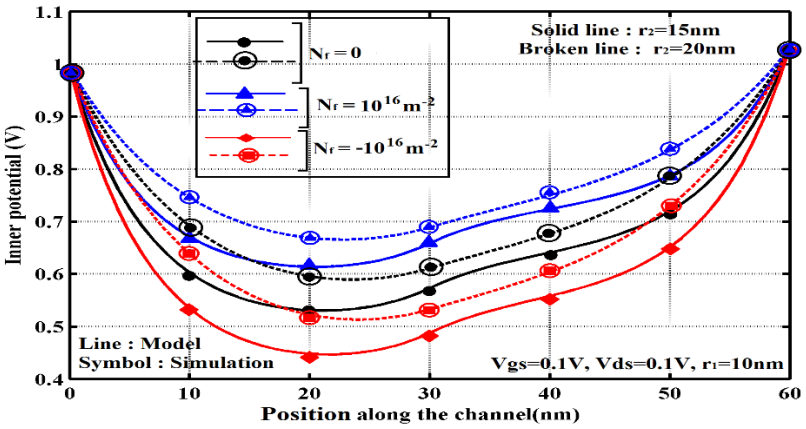


Fig.4.5 (a)

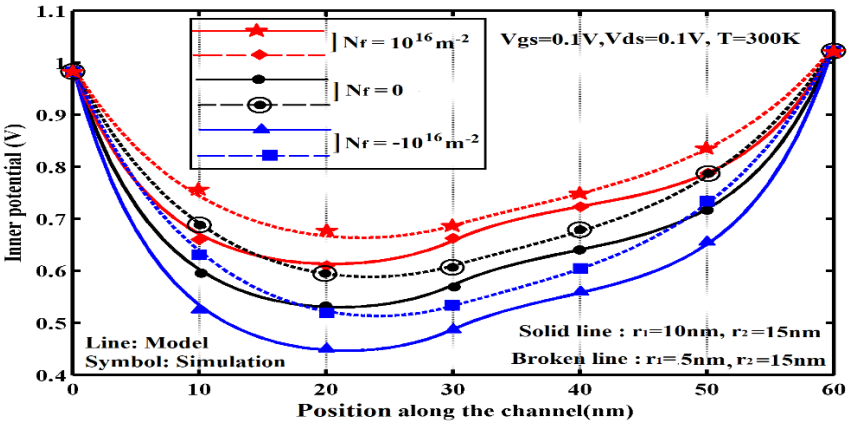


Fig.4.5 (b)

Fig.4.5 (a) Inner potential distribution along the channel position of the proposed, damaged and undamaged device for two different values of outer radius keeping the filler radius fixed at 10 nm (T = 300 K), (b) Inner potential distribution along the channel position of the proposed, damaged and undamaged device for two different values of filler radius keeping the outer radius fixed at 15 nm (T = 300 K).

For negative trap charges, source-channel barrier height being higher contributes significantly to elevate the threshold voltage while, source-channel barrier height being much diminished for positive trap charges, threshold voltage significantly decreases as in

Fig.4.4. With rise in temperature, threshold voltage for both damaged and undamaged device gradually decreases. This can be credited to the circumstance that at heightened temperatures, carrier generation is greater and therefore, a considerably lower gate voltage can turn the device to On-state. Fig.4.9 shows the graphical illustration of the threshold voltage variation for both damaged and undamaged configuration of the projected device and for different values of outer radius with filler radius fixed at 10nm and at T=300K. With gradual elevation in outer radius value, with filler radius fixed at 10nm, the threshold voltage steadily reduces initiating augmented leakages and depreciated device performances. With higher outer radius, channel thickness increases causing enfeebled gate control over the channel. This feature has been apparently observed in Fig.4.5 a. Figure 4.10 demonstrates the graphical illustration of threshold voltage vs. different filler radius with the outer radius fixed at 15 nm. With increment in the filler radius at a fixed outer radius fixed at 15 nm, the channel thickness gradually drops contributing to improved gate control of the channel. Thus the threshold voltage substantially elevates, and the off-state leakages are suppressed effectively. This feature has already been observed in Fig. 4.5 (b). In short, with the filler radius fixed, threshold voltage decreases as the outer radius increases, and with a fixed outer radius, threshold voltage increases when the filler radius increases. Fig.4.11 demonstrates the variation of threshold voltage for different positive and negative trap charge densities and for three different channel lengths of proposed device. As observed from fig.4.6, at a scaled channel length of 40nm, a decrement in the source-channel barrier is noted due to the encroaching SCEs which causes the threshold voltage to diminish compared to that with L=60nm. Thus, threshold voltage is maximum for L=100nm, intermediate for L=60nm and lowest for L=40nm, whatever the positive/negative trap charge density is and also for no trap charges (N_f=0). Now, as observed from fig. 4.6, with elevation in negative trap charge density, threshold voltage also shoots up due to increased source-channel barrier height, and attains maximum for the density -3x$10^{16}$$m^{-2}$, and with increment in positive charge density, source-channel barrier height significantly lessens contributing to a reduction in the threshold voltage which attains lowest value for density of 3x$10^{16}$$m^{-2}$. Fig.4.12 exhibits the variation of threshold voltage of the proposed, undamaged device and its full channel cylindrical gate-all-around (GAA) complement. As formerly discussed for Fig. 4.7, threshold

voltage for the projected device is greater relative to its cylindrical equivalent because of augmented source-channel barrier height in the former's inner potential distribution.

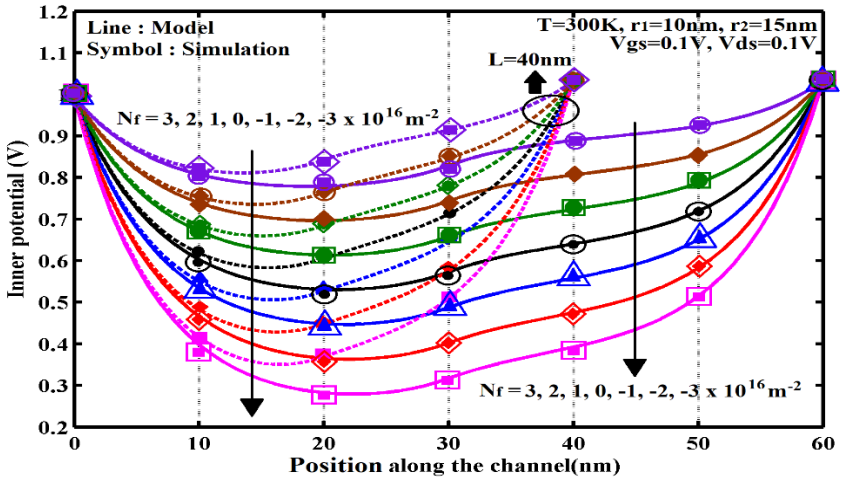


Fig.4.6 Inner potential distribution vs. channel position of the proposed device for variation in densities of positive and negative trap charges, and without trap charges, for two channel lengths (T = 300 K).

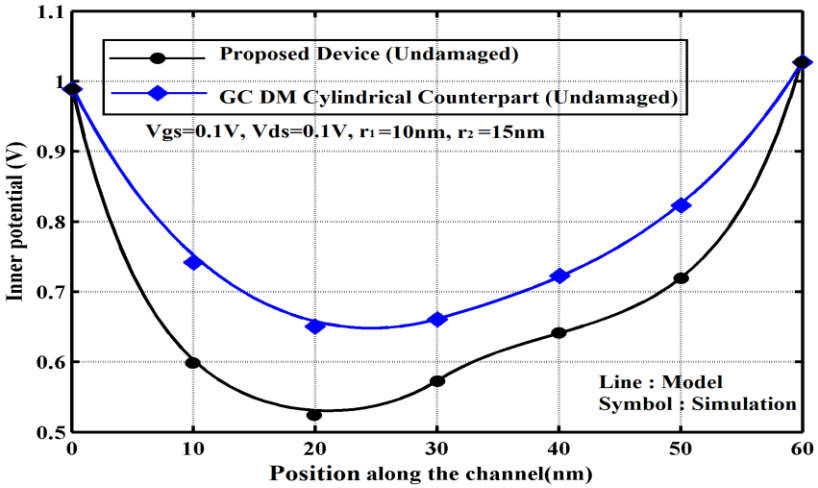


Fig.4.7 Inner potential distribution along the channel length in Proposed, undamaged device and its cylindrical full-channel GAA counterpart with the with the same radius as the outer radius of the proposed Device (T = 300 K, N_f = 0)

Additionally, a source-shifted minimum and noticeably sharp step profile in the projected device contributes to lower threshold voltage roll-off which is substantially high in its full-channel cylindrical equivalent since the latter does not possess the abovementioned properties in its inner potential distribution. Fig.4.13 elucidates the graphical exploration of

threshold voltage variation vs. channel length for graded and non-graded/uniformly doped channels of the proposed, damaged and undamaged device. For positive, negative and zero trap charges, threshold voltage trails the same fashion as illustrated previously. Now, for uniformly doped channel device, threshold voltage minimizes, and when the channel is graded with high doping near the source, threshold voltage upsurges warranting steady lessening of leakages. Hence, the graded channel strategy with apposite doping concentration value selection permits proper regulation of threshold voltage, thereby sanctioning the effective suppression of SCEs and leakages. One of the prime benefits of using a dual-material gate over single material is clearly highlighted in Fig.4.14 which demonstrates the DIBL variation for the proposed, undamaged device, its SM configuration and its full channel CGAA equivalent for different temperatures. Step profiles being absent for devices without GWFE results in higher DIBL and step profile being prominent in DM devices permit a high shielding effect to DIBL. The inner potential minimum in the latter is shielded by the step profile from being impacted upon by drain voltage variations, thereby letting the device to be able to offer excellent resistance to DIBL compared to its single-material (SM) gate counterpart. Also, the DIBL variation at diverse temperatures for the GC DM full-channel cylindrical equivalent of the proposed device is exhibited in the same graph. With rise in temperature, DIBL also increases. Fig.4.12 evidently shows that, as channel length is scaled down, the threshold voltage for the GC DM full-channel cylindrical MOSFET radically decreases compared to that in the proposed device. The roll-off is higher in the GC DM full-channel cylindrical MOSFET, and at 100nm channel length, on comparing the plots, the threshold voltage for the above device is still lower than the proposed device. This lower threshold voltage denotes an increased DIBL in the GC DM cylindrical device, which aggravates when the channel length is scaled down to as low as 40 nm. This is revealed in Fig.4.14 where the DIBL values for 100K–500 K for the GC DM equivalent is considerably greater than both the proposed device and its SM contemporary at a scaled channel length of 30 nm. Hence, among the three devices, the recommended device, which displays the minimum DIBL, has admirable invulnerability against major SCEs such as DIBL. Reduced temperatures are a reason behind lower impact ionization rate compared to that at heightened temperatures which causes better subthreshold swing characteristics in the proposed device as revealed in Fig.4.15. A number of researchers have testified reports on

short-channel MOSFETs highlighting the subthreshold swing characteristics at low temperatures of 100 K and 200 K. Ghibaudoa et al. [4.19] reported much lower subthreshold swing values of about 20 mV/dec at 100K and about 40 mV/dec at 200 K. Biswas et al. [4.20] exhibited subthreshold swing values as low as 20 mV/dec at 100 mV and about 40mV/dec at 200 K for both strained and unstrained channel configurations in short channel MOSFETs. The trend of subthreshold swing as obtained in the current case closely ties with the trend of SS shown by MOSFET devices at low temperatures of 100K and 200K. Hence, subthreshold swing is radically influenced by changes in temperature and decreases (increases) with a decrease (increase) in temperature. A relative Subthreshold Swing investigation of the proposed, undamaged device and its GC DM full-channel cylindrical complement is exhibited through a graphical investigation in Fig.4.16. The figure shows that SS in proposed, undamaged device for aggressively scaled channel lengths of 40 nm, is about 70 mV/dec, whereas, for its GC DM full-channel cylindrical equivalent, SS at 40-nm channel length is quite high about 110 mV/dec.

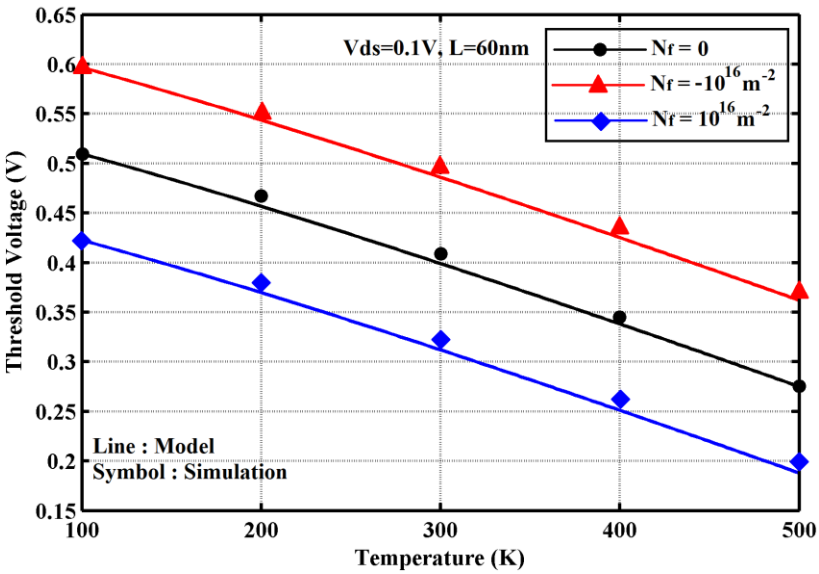


Fig. 4.8 Threshold voltage variation vs. temperature of the proposed, damaged and undamaged device

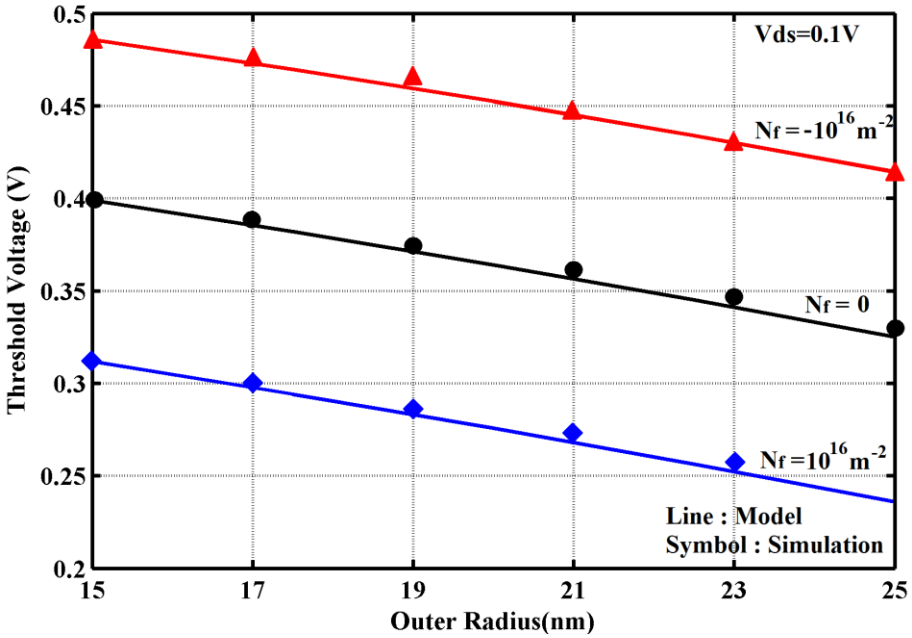


Fig.4.9 Threshold voltage variation vs. outer radius of the proposed, damaged and undamaged device (filler radius = 10 nm, L = 60 nm, T = 300 K).

Also, with long channel lengths of 100 nm, SS for the proposed device saturates to 60 mV/dec (the ideal value of SS for short-channel MOSFETs), while that for its GC DM full-channel cylindrical equivalent, the SS value saturates to as high as about 65 mV/dec at 100-nm channel length. Another prime gain of GWFE scheme incorporation can be perceived from Fig.4.17 where the lateral electric field is much reduced at the drain end for the undamaged configuration of the proposed device compared to its SM counterpart. Electric field at drain side being much diminished results in weakened HCE. In addition to this, the electric field peaks at the interface of two dissimilar materials for the projected device, thereby contributing a boost to the transport efficiency. However, lateral electric field at drain end increases for both the device, with increase in drain bias. Fig.4.18 demonstrates the analysis of drain current of the projected device with varying gate bias for different positive and negative trapped charge densities. For negative trapped charges, threshold voltage is maximum among the three cases (negative, positive and zero trap charges), off-state leakages are radically reduced which, in turn, reduces the subthreshold current, whereas the gate-induced drain leakage (GIDL) current gets enhanced. For no trap charges, threshold voltage gets reduced compared to the negative trap charge case, hence subthreshold current upsurges compared to the previous case of negative trap charges.

However, GIDL decreases. Threshold voltage, for positive trap charges, is lowest among the three cases, this causes the subthreshold current to augment, whereas GIDL current largely decreases.

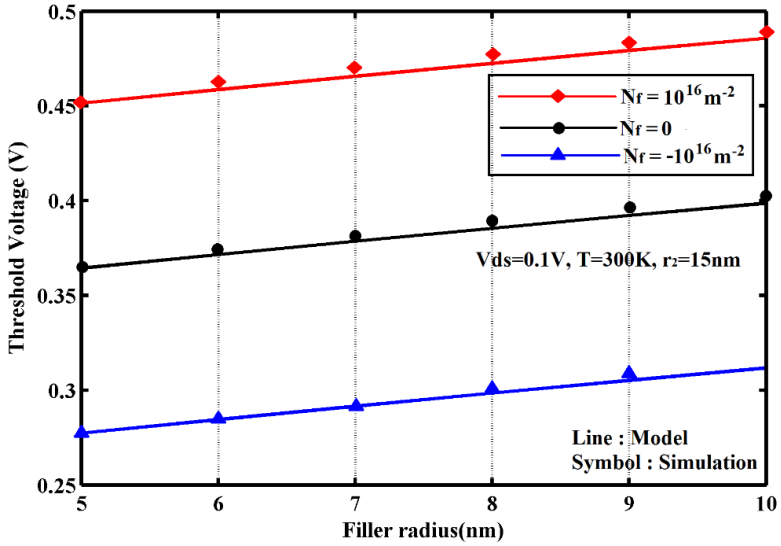


Fig.4.10 Threshold voltage variation versus values of filler radius of the proposed device for both damaged and undamaged configurations (outer radius = 15 nm, L = 60 nm, T = 300 K).

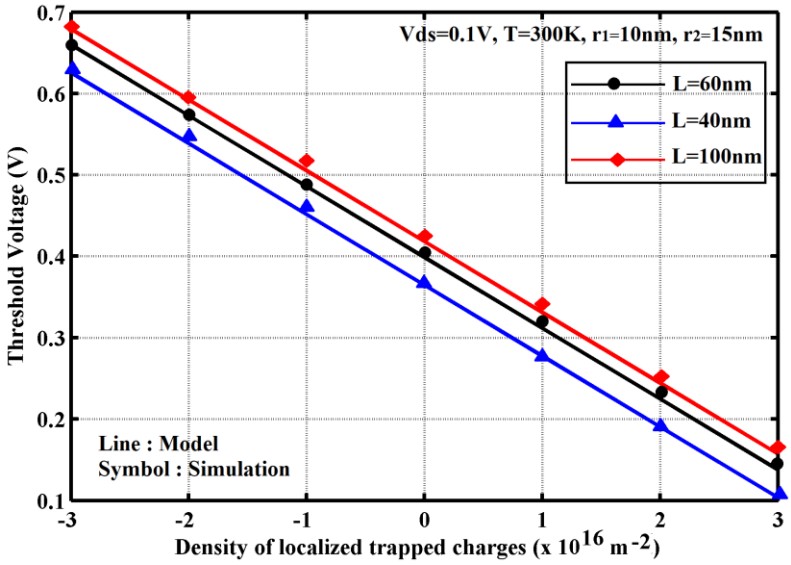


Fig.4.11 Threshold voltage variation vs. positive and negative trap charge densities for the proposed device and for three different channel lengths.

Further, with enhancement in the density of negative trapped charges, threshold voltage highly gets increased. For a density of $3x10^{16}$ m^{-2}, subthreshold current gets radically

diminished thereby plummeting the off-state leakages while the reverse case takes place for the highest density of positive trapped charges. When a gate material having lower work function (relative to the work function of a gate material at the source side) is used towards the drain side, it aids in decreasing the electric field at the drain end thereby lessening the electrons' speed at the drain end, and this, in turn, contributes to lower the tunneling phenomenon of minority carriers from the drain into the channel. From the expression of flat-band voltage, it is clearly evident that the flat-band voltage is actually directly proportional to the gate material work function, thus it can be stated that a lesser flat-band voltage at the drain side is the reason behind effective clampdown of minority carriers tunneling from the drain, hence refining and lessening the GIDL effect and sinking the GIDL current. According to the equation, $V_{fb_i}{}' = V_{fbi} - \frac{qN_f}{C_{ox}}$ [4.21-4.23] (with a gate material having a lower work function towards the drain), the presence of positively charged traps adds a diminution to the flat-band voltage further at drain end thereby contributing to enormous decrease of GIDL current.

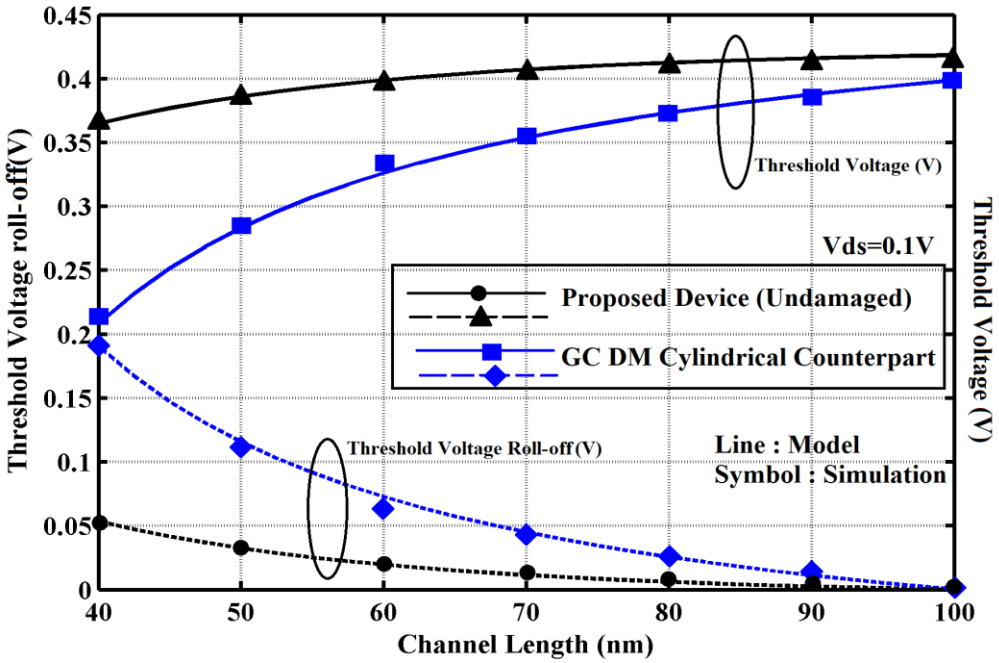


Fig. 4.12 Threshold voltage roll-off (TVRO) and threshold voltage variation vs. channel length for the proposed, undamaged device and its GC DM cylindrical equivalent with the same radius as the outer radius of the proposed device

For negative trapped charges, flat-band voltage at the drain augments permitting substantial minority carrier tunneling and waning device performance by the aggravating increase in the GIDL current. This clearly establishes the physics governing the graphical illustration in Fig. 4.18. As evident from fig.4.19, GIDL current is quite high in the single-material (SM) gate device relative to the proposed device owing to increased flat-band voltage at the drain end in the SM device, which results in a high electric field at drain end thereby permitting large number of minority carriers to tunnel from the drain into the channel. Also, the SM device undergoes performance weakening due to DIBL which intensifies the subthreshold leakage current in the device unlike the proposed GWFE device.

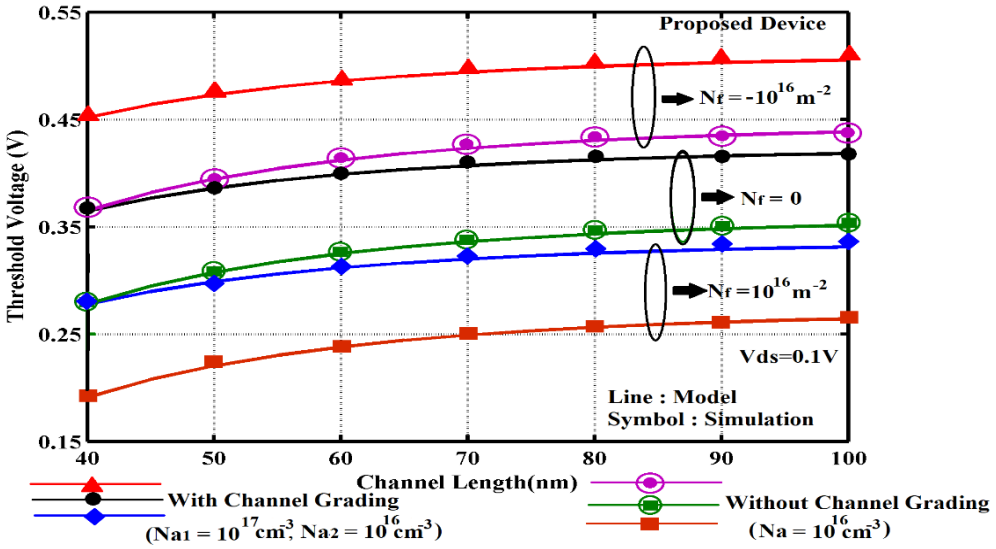


Fig.4.13 Variation of Threshold voltage versus channel length of the graded and non-graded channel of the proposed, damaged and undamaged device in the presence and absence of trap charges.

These graphical illustrations endorse the superiority and excellence of the proposed device in terms of performance and generates significant avenues for the recommended device to be employed in the forthcoming generation VLSI circuital applications. Results of this section are corroborated using simulation outputs from Silvaco TCAD, and the results unveil the superiority of the proposed device over the existing modern-day devices.

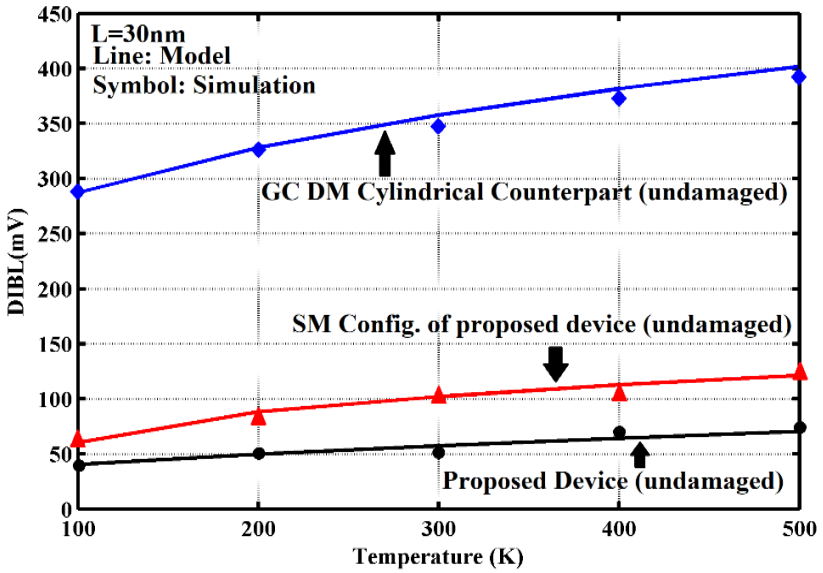


Fig.4.14 DIBL variation for different temperatures for the proposed, undamaged device, its SM counterpart and GC DM full-channel cylindrical counterpart with a radius similar to the outer radius of the proposed device (T = 300 K).

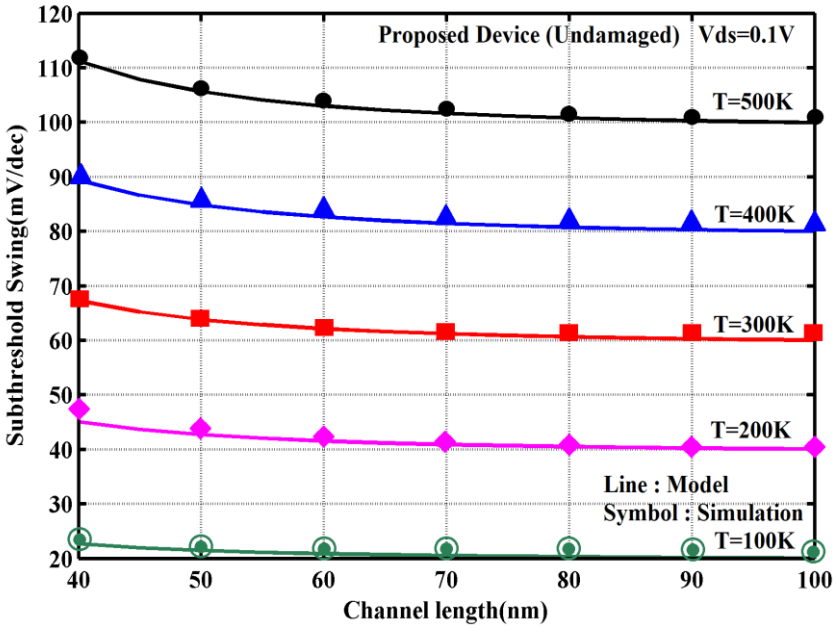


Fig.4.15 Subthreshold swing variation versus channel length for the proposed, undamaged device at different temperatures.

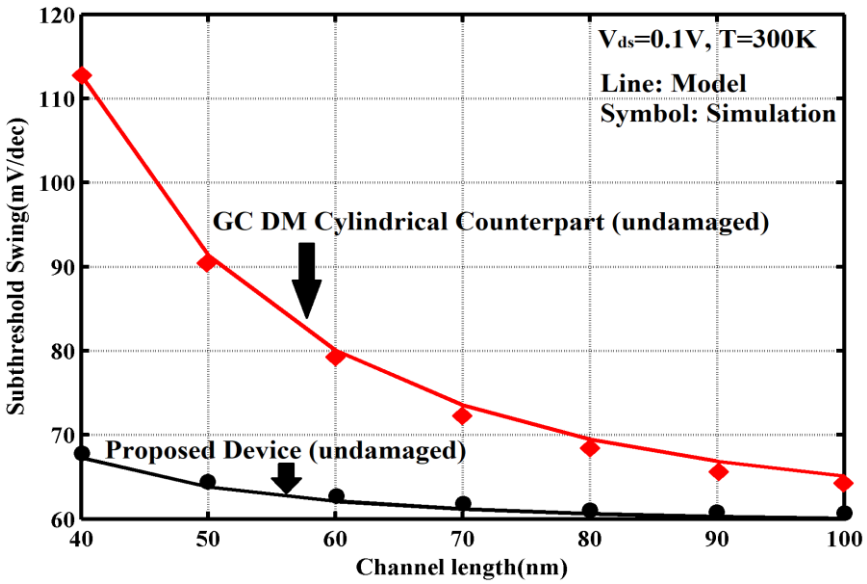


Fig.4.16 Subthreshold swing variation vs. channel length for the proposed, undamaged device and its GC DM full channel cylindrical counterpart.

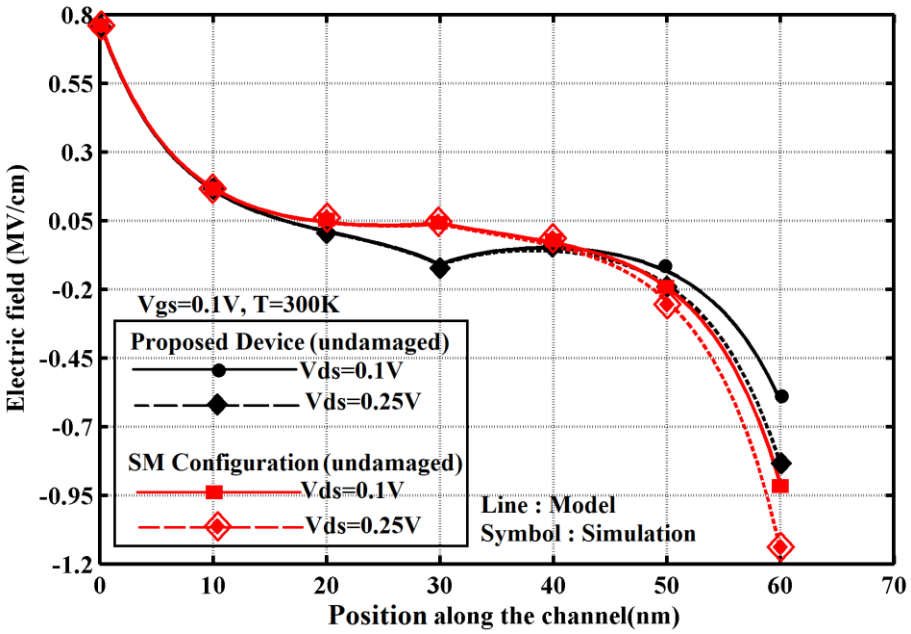


Fig.4.17 Variation of Lateral electric field along channel position for drain voltages alterations of the proposed, undamaged device and its SM counterpart with the same radius as the outer radius of the proposed device

(T = 300 K, N_f = 0).

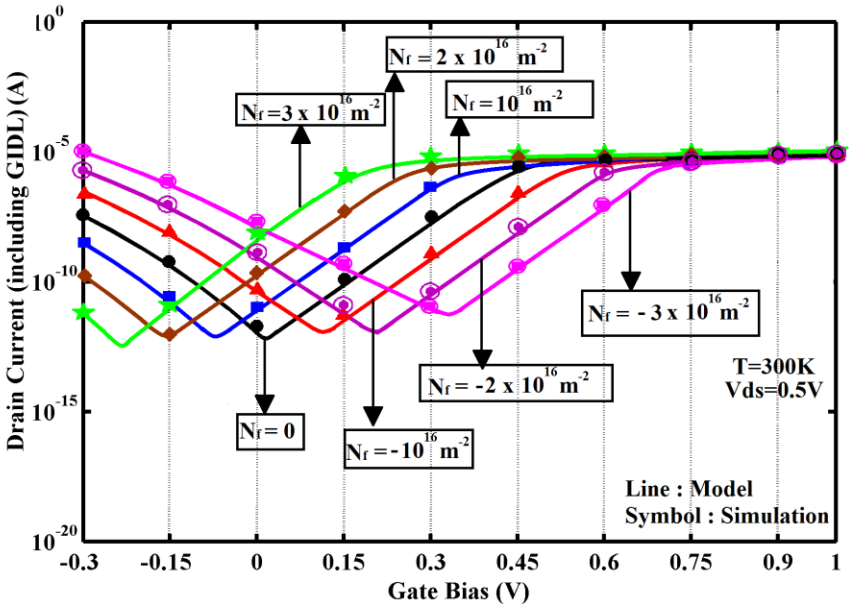


Fig.4.18 Variation of drain current with gate bias for different positive and negative trap charge densities for the proposed device (L = 60nm)

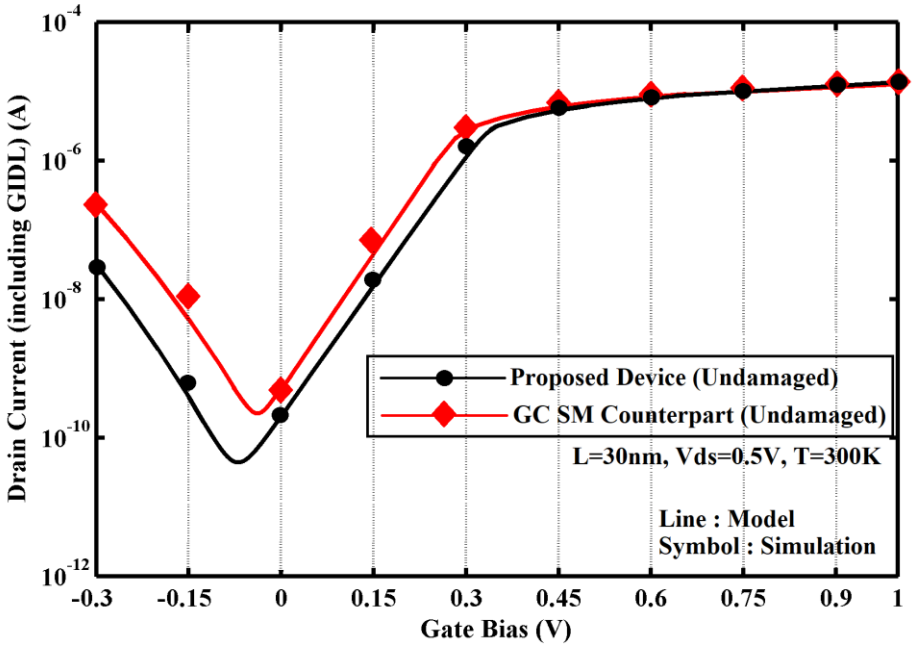


Fig.4.19 Variation of drain current with gate bias for the proposed, undamaged device and its SM counterpart.

4.5. Conclusion

The current research exploration offers the localized trap charge induced analytical modelling and simulation of a graded-channel dual-material gate macaroni MOSFET. Thermal-dependence of the extent of device performance consistency of the proposed device with both damaged and undamaged configurations has been precisely investigated from the inner potential distribution, threshold voltage and short-channel effect response. Trap charges considerably modify device flat-band voltage which subsequently impacts device features. Drain current exploration including the gate-induced drain leakage (GIDL) effect has been provided for both the damaged and undamaged configurations and outcomes exhibit substantial drain current changes when the trap charges are present. This reveals the necessity to investigate damaged device features relative to the undamaged one. The recommended device unveils improved short channel performance when related to its full-channel gate-all-around (GAA) cylindrical equivalent in terms of threshold voltage, threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold swing (SS) that showcases the benefits of macaroni architecture, making it a potential replacement for full-channel GAA cylindrical MOSFFETs. Further, comparative study of short-channel effects (SCEs), gate-induced drain leakage (GIDL) analysis considering the proposed device and its single-material counterpart (even at a scaled length of 30 nm) clearly evident the rewards of gate work function engineering (GWFE) in the former, recommended device over the latter. Further, results validate that appropriate choice of channel grading concentrations can befittingly tune the threshold voltage in the proposed graded-channel device. Simulation outputs are in good agreement with analytical results thereby authenticating the proposed device as a prospective candidate for future generation VLSI applications.

Relevant Publication

Pritha Banerjee and Jayoti Das, "Gate Work Function-Engineered Graded-Channel Macaroni MOSFET: Exploration of Temperature and Localized Trapped Charge-Induced Effects with GIDL Analysis", **Journal of Electronic Materials**, **Springer**, 51, 1512–1523, 2022, https://doi.org/10.1007/s11664-021-09419-0. [SCI, SCIE, IF:1.938]

References

[4.1] A. Cerdeira, M. A. Aleman, M. A. Pavanello, J. A. Martino, L. Vancaillie and D. Flandre, "Advantages of the graded-channel SOI FD MOSFET for application as a quasi-linear resistor," in IEEE Transactions on Electron Devices, vol. 52, no. 5, pp. 967-972, May 2005, doi: 10.1109/TED.2005.846327.

[4.2] Delhougne, R., Arreghini, A., Rosseel, E., Hikavyy, A., Vecchio, E., Zhang, L. Furnemont, A., "First demonstration of monocrystalline silicon macaroni channel for 3-D NAND memory devices", 2018 IEEE Symposium on VLSI Technology. doi:10.1109/vlsit.2018.8510635

[4.3] Marcelo Antonio Pavanello, João Antonio Martino, Denis Flandre, "Graded-channel fully depleted Silicon-On-Insulator nMOSFET for reducing the parasitic bipolar effects", 44(6), 917–922. doi:10.1016/s0038-1101(00)00032-0, 2000

[4.4] Jun Ma, ; Han-Bin Liang, ; Pryor, R.A.; Cheng, S.; Kaneshiro, M.H.; Kyono, C.S.; Papworth, K., "Graded-channel MOSFET (GCMOSFET) for high performance, low voltage DSP applications", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 5(4), 352–359. doi:10.1109/92.645061, 1997

[4.5] A. Goel, S. Rewari, S. Verma, and R.S. Gupta, "Temperature- Dependent Gate-Induced Drain Leakages Assessment of Dual-Metal Nanowire Field-Effect Transistor—Analytical Model", IEEE Trans. Electron Devices. 66, 2437, 2019.

[4.6] T. Y. Chan, J. Chen, P. K. Ko and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," 1987 International Electron Devices Meeting, 1987, pp. 718-721, doi: 10.1109/IEDM.1987.191531.

[4.7] Gautam, Rajni; Saxena, Manoj; Gupta, R.S.; Gupta, Mridula, "Temperature dependent subthreshold model of long channel GAA MOSFET including localized charges to study variations in its temperature sensitivity", Microelectronics Reliability, 54(1), 37–43, 2014 doi:10.1016/j.microrel.2013.09.014

[4.8] Guan, Yunhe; Li, Zunchao; Zhang, Wenhao; Zhang, Yefei; Liang, Feng, "An Analytical Model of Gate-All-Around Heterojunction Tunneling FET", IEEE Transactions on Electron Devices, 65(2), 776–782, 2018, doi:10.1109/TED.2017.2783911

[4.9] Dubey, Sarvesh; Santra, Abirmoya; Saramekala, Gopikrishna; Kumar, Mirgender; Tiwari, Pramod Kumar, “An Analytical Threshold Voltage Model for Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs”, IEEE Transactions on Nanotechnology, 12(5), 766–774, 2013, doi:10.1109/TNANO.2013.2273805

[4.10] Q. Nguyen-Gia, M. Kang, J. Jeon and H. Shin, "Characteristic Length of Macaroni Channel MOSFET," in IEEE Electron Device Letters, vol. 40, no. 11, pp. 1720-1723, Nov. 2019, doi: 10.1109/LED.2019.2942619

[4.11] H.-K. Wang, S. Wu, T.-K. Chiang, and M.-S. Lee, “A new two-dimensional analytical threshold voltage model for short-channel triple material surrounding-gate metal-oxide-semiconductor field-effect transistors,” Jpn. J. Appl. Phys., vol. 51, pp. 054301–054306, Apr. 2012

[4.12] L. Zhang, L. Li, J. He and M. Chan, "Modeling Short-Channel Effect of Elliptical Gate-All-Around MOSFET by Effective Radius," in IEEE Electron Device Letters, vol. 32, no. 9, pp. 1188-1190, Sept. 2011, doi: 10.1109/LED.2011.2159358

[4.13] Z. Ding, G. Hu, J. Gu, R. Liu, L. Wang and T. Tang, "An analytical model for the subthreshold swing of double-gate MOSFETs," 2010 International Workshop on Junction Technology Extended Abstracts, 2010, pp. 1-4, doi: 10.1109/IWJT.2010.5475006

[4.14] E. Goel, S. Kumar, K. Singh, B. Singh, M. Kumar and S. Jit, "2-D Analytical Modeling of Threshold Voltage for Graded-Channel Dual-Material Double-Gate MOSFETs," in IEEE Transactions on Electron Devices, vol. 63, no. 3, pp. 966-973, March 2016, doi: 10.1109/TED.2016.2520096.

[4.15] Rewari, V. Nath, S. Haldar, S. S. Deswal and R. S. Gupta, "Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET," in IEEE Transactions on Electron Devices, vol. 65, no. 1, pp. 3-10, Jan. 2018, doi: 10.1109/TED.2017.2771814

[4.16] A. Farkhanda, “Suppression of gate induced drain leakage current (GIDL) by gate work function engineering: Analysis and model,” J. Electron Devices, vol. 13, pp. 984–996, Mar. 2012.

[4.17] A. Bouhdada, S. Bakkali, and A. Touhami, “Modelling of gate-induced drain leakage in relation to technological parameters and temperature,” Microelectron. Rel., vol. 37, pp. 649–652, Apr. 1997.

[4.18] A. Pal, and A. Sarkar, “Analytical Study of Dual Material Surrounding Gate MOSFET to Suppress Short-Channel Effects (SCEs)”, Int. J. Eng. Sci. Technol. 17, 205, 2014.

[4.19] G. Ghibaudoa, M. Aouadb, M. Casseb, S. Martinieb, T. Poirouxb, and F. Balestraa, "On the Modelling of Temperature Dependence of Subthreshold Swing in MOSFETs down to Cryogenic Temperature", Solid-State Electron., 170, 107820 (2020).

[4.20] A. Biswas, and S. Bhattacherjee, “Temperature dependent model for threshold voltage and subthreshold slope of strained-Si channel MOSFETs with a polysilicon gate”, Microelectron. Reliab. 54, 1527, 2014

[4.21] Gautam Rajni, Saxena Manoj, Gupta RS, Gupta Mridula, “Two dimensional analytical subthreshold model of nanoscale cylindrical surrounding gate MOSFET including impact of localized charges”, J Comput Theoretical Nanosci 2012;9:602–10.

[4.22] Susan C. Vitkavage and Eugene A. Irene, "An investigation of Si-SiO2 interface charges in thermally oxidized (100), (110), (111), and (511) silicon", Journal of Applied Physics 68, 5262 (1990)

[4.23] Nilesh Anand Srivastava, Anjali Priya, Ram Awadh Mishra, “Interface trap charge-based reliability assessment of high-k dielectric-modulated nanoscaled FD SOI MOSFET for low power digital ICs: Modeling and simulation”, Superlattices and Microstructures, Volume 154, 2021, 106871

Chapter 5

Chapter 5: Dual-Material Gate Macaroni Channel MOSFET Biosensor using Dielectric-Modulation Technique: Sensitivity Analysis using Threshold Voltage Shifts

---

5.1. Introduction

The key to the unimpeded evolution of the modern era device manufacturing is undoubtedly the ever-expanding consumer demands for sleeker, cost-effective, faster devices that consume lower power. With the progress in time of the current decade, technology has been pushed to the limits where device dimensions have been aggressively scaled down to few tens of nanometers. Though this is inevitable for the modern semiconductor industry to keep pace with the Moore's law, however, it is equally necessary to overcome the major challenges that crop up in such smaller device dimensions. These challenges, collectively known as the short channel effects, can be diminished through a combination of device scaling and new technology incorporation [5.1-5.3]. However, the associated technologies for short channel effects minimization should be fabrication feasible involving reduced fabrication complexities that would, in turn, catalyze cost-effectiveness of the device.

As already discussed in chapter 1, Multi-gate MOSFETs architectures offer superior gate-channel coupling and in this context, Cylindrical Gate-all-around (GAA) structures have been the foremost choice of the researchers since these devices offer excellent SCE immunization coupled with lower power consumption, higher packaging density, better current driving capability and reduced leakage issues.

However, existing literature reports and the results from chapter 4 exhibit that Macaroni channel GAA MOSFETs have easily excelled conventional CGAA MOSFETs in terms of offering radically improved device performance and are thus excellent replacements of CGAA MOSFETs for real-time applications such as biosensor. Also, Macaroni channels are fabrication feasible and their detailed step-by-step fabrication procedure has been discussed in chapter 4.

Therefore, in the following section an advanced Macaroni channel GAA MOSFET has been considered as the basic geometry to explore the biosensor properties of this device.

5.2. Overview

For effective implementation of an advanced MOSFET device to work as a biosensor, the basic device geometry should be carefully chosen considering important parameters like high sensitivity, improved SCE resistance that leads to low power consumption, enhanced

speed of operation etc. In this context, Cylindrical Gate-All-Around MOSFET biosensors have been the primary choice for their execution as biosensors owing to their higher integration density, excellent immunity to SCEs, high sensitivity characteristics, upgraded threshold voltage features etc. [5.4]. However, recent reports claim that Macaroni-channel configured GAA MOSFETs have outclassed the Cylindrical GAA MOSFETs in terms of offering magnificent device performance [5.5] and it is also evident from the results discussed in chapter 4 where comparative investigation of an advanced configuration of Macaroni channel MOSFET and its Full channel CGAA counterpart demonstrate evidences of reduced threshold voltage roll-off, reduced DIBL, reduced subthreshold swing in the former device compared to the latter. Considering the benefits offered by the Macaroni-structure, it has been chosen as the basic device for biosensing applications execution in the following research. To further elevate the extent of perfection in the device characteristics, GWFE scheme has been amalgamated along with a high-K gate stack incorporation as the gate oxide towards the drain end. The high-K gate stack targets development of the Subthreshold Swing whereas GWFE takes care to weaken major SCEs. Thus the resulting device is a Dual-Material Gate Macaroni Channel MOSFET Biosensor. The same technique of dielectric modulation, as discussed in chapter 2, has been applied here to obtain the threshold voltage based sensitivity analysis of the recommended biosensor.

The fabrication feasibilities of Dual-Material gate formation, High-K gate stack oxide and nanogap formation have been discussed precisely in Chapter 2 which further motivates the conceptualization of the following research.

Motivated by the feasibility of fabrication and benefits of Macaroni channels in MOSFET, the current research exhibits intensive investigation of sensitivity of projected Dual-Material Gate Macaroni Channel MOSFET biosensor and also reveals comparative studies of sensitivity analysis of the proposed biosensor and its Dual-Material Full Channel Cylindrical Counterpart.

5.3. Analytical Modeling

The 3-D schematic diagram of proposed Dual-Material Gate Macaroni Channel MOSFET Biosensor is portrayed in fig.5.1. The channel configuration of the MOSFET device is

Macaroni type with filler radius r_1=10nm and outer radius r_2=20nm. Channel thickness is denoted by $t_{Si}=2(r_2- r_1)$. Channel length L=60nm. Doping concentration in the channel is $N_a=10^{17}cm^{-3}$. The gate is of Dual-Material consisting gate material M_{G1} (work function $\phi_{M_{G1}} = 4.8eV$) of gate length L_1 (=30nm) towards source has higher work function and that towards drain side M_{G2} (work function $\phi_{M_{G2}} = 4.4eV$) of gate length L_2 (=30nm) has lower work function. The region beneath M_{G1} and above the interfacial oxide layer is etched to form a nanogap (thickness t_{bio}=9nm) that acts as the site for biomolecules. The region beneath M_{G2} has a high-k oxide HfO_2 (thickness t_2=9nm) placed above the interfacial layer of SiO_2 which covers the entire surface of the channel. Thickness of the SiO_2 layer is t_1=1nm.

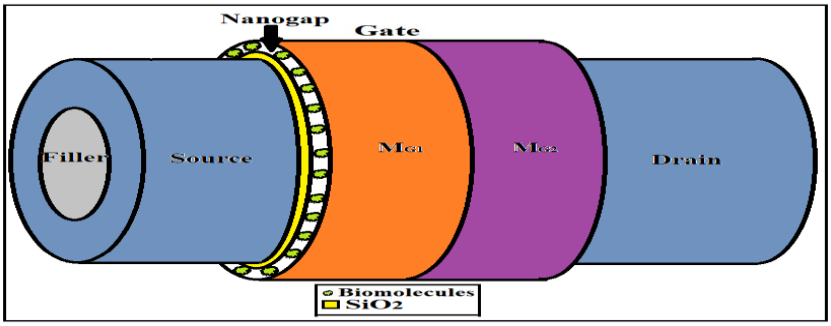


Fig. 5.1. 3-D Schematic Representation of Proposed Dual-Material Gate Macaroni-Channel MOSFET Biosensor

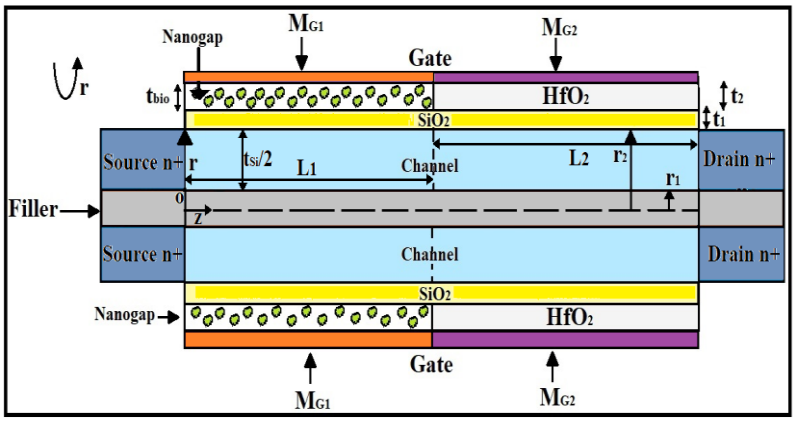


Fig. 5.2. 2-D Cross-sectional Representation of Proposed Dual-Material Gate Macaroni-Channel MOSFET Biosensor

5.3.1. Inner Potential Modeling

In order to investigate the detailed electrical characteristics of the proposed biosensor, the expression for inner potential needs to be obtained which necessitates the solution of the 2-D Poisson's equation which is as follows [5.6]:

$$\frac{\partial^2\Psi_i(r,z)}{\partial r^2}+\frac{1}{r}\frac{\partial\Psi_i(r,z)}{\partial r}+\frac{\partial^2\Psi_i(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{Si}} \tag{5.1}$$

Where i stands for the i[th] region, i=1 for region 1 defined by the boundaries $0\le z\le L_1, r_1\le r\le r_2$ and i=2 for region 2 defined by the boundaries $L_1\le z\le L, r_1\le r\le r_2$. Potential in the i[th] region is denoted as $\Psi_i(r,z)$.

Potential distribution is parabolic along the radial direction and is given as follows [5.7]:

$$\Psi_i(r,z)=a_{1i}(z)+a_{2i}(z)r+a_{3i}(z)r^2 \tag{5.2}$$

In order to find the expression of coefficients related to equation (3.2), the following set of boundary conditions need to be considered as per reference [5.8]:

$$\left.\frac{\partial\Psi_i(r,z)}{\partial r}\right|_{r=r_1}=a_{2i}(z)+2r_1a_{3i}(z)=0 \tag{5.3}$$

$$\left.\frac{\partial\Psi_i(r,z)}{\partial r}\right|_{r=r_2}=\frac{C_{f_i}}{\varepsilon_{Si}}\left[V_{gs_i}-\Psi_i(r_2,z)\right] \tag{5.4}$$

Using the above set of boundary conditions, the following expressions of coefficients have been obtained:

$$a_{2i}(z)=-2r_1a_{3i}(z) \tag{5.5}$$

$$a_{3i}(z)=\frac{4C_{f_i}\left[V_{gs_i}-\psi_{0i}(z)\right]}{\left[C_{f_i}t_{Si}{}^2+4\varepsilon_{Si}t_{Si}\right]} \tag{5.6}$$

Where $\psi_{0i}(z)$ is the inner potential in the i[th] region,

When i=1 for region 1, we get [5.9],

$$C_{f_1}=\frac{\varepsilon_{SiO_2}}{r_2\ln\left(1+\frac{t_{eff_1}}{r_2}\right)},\ t_{eff_1}=t_{SiO_2}+\frac{\varepsilon_{SiO_2}}{\varepsilon_{bio}}t_{bio},$$

$V_{gs_1} = V_{gs} - V_{fb_1}{}'$, effective flat-band voltage in region 1 is $V_{fb_1}{}' = V_{fb_1} - \frac{qN_f}{C_{f_1}}$ [5.10], N_f is the charge density of charged biomolecules.

When i=2 for region 2, we get,

$$C_{f_2} = \frac{\varepsilon_{SiO_2}}{r_2 \ln\left(1 + \frac{t_{eff_2}}{r_2}\right)},\ t_{eff_2} = t_{SiO_2} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} t_{high-k},\ V_{gs_2} = V_{gs} - V_{fb_2}{}', V_{fb_2}{}' = V_{fb_2}$$

Putting the expressions of coefficients with equations (5.5) and (5.6) in equation (5.2) and then in equation (5.1), the following differential equation is obtained at r=r_1:

$$\frac{\partial^2 \psi_{0i}(z)}{\partial z^2} + 2a_{3i}(z) = \frac{qN_a}{\varepsilon_{Si}} \tag{5.7}$$

Solutions to above equation is listed as follows [5.11]:

In Region 1, expression of inner potential is given as:

$$\psi_{01}(z) = M_1 \exp(z/\lambda_1) + N_1 \exp(-z/\lambda_1) + \phi_{01} \tag{5.8}$$

Where $\frac{1}{\lambda_1} = \sqrt{\frac{8C_{f_1}}{\left[C_{f_1} t_{Si}{}^2 + 4\varepsilon_{Si} t_{Si}\right]}}$, $\phi_{01} = V_{gs_1} - \frac{qN_a \lambda_1{}^2}{\varepsilon_{Si}}$

In Region 2, expression of inner potential is given as:

$$\psi_{02}(z) = M_2 \exp\left((z - L_1)/\lambda_2\right) + N_2 \exp\left(-(z - L_1)/\lambda_2\right) + \phi_{02} \tag{5.9}$$

Where $\frac{1}{\lambda_2} = \sqrt{\frac{8C_{f_2}}{\left[C_{f_2} t_{Si}{}^2 + 4\varepsilon_{Si} t_{Si}\right]}}$, $\phi_{02} = V_{gs_2} - \frac{qN_a \lambda_2{}^2}{\varepsilon_{Si}}$

The coefficients' expressions in equation (5.8) and (5.9) can be obtained using the following boundary conditions listed below [5.12]:

$$\psi_{01}(z)\big|_{z=0} = V_{bi} \tag{5.10}$$

$$\psi_{02}(z)\big|_{z=L} = V_{bi} + V_{ds} \tag{5.11}$$

$$\psi_{01}(z)\big|_{z=L_1} = \psi_{02}(z)\big|_{z=L_1} \tag{5.12}$$

$$\left.\frac{\partial \psi_{01}(z)}{\partial z}\right|_{z=L_1} = \left.\frac{\partial \psi_{02}(z)}{\partial z}\right|_{z=L_1} \tag{5.13}$$

Thus, the expressions of coefficients in equation (5.8) and (5.9) thus obtained are:

$$M_1 = \alpha_1 + \beta_1 V_{gs} \tag{5.14}$$

$$N_1 = \alpha_2 + \beta_2 V_{gs} \tag{5.15}$$

$$M_2 = \left(\frac{x_1}{2}\right) M_1 \exp\left(L_1/\lambda_1\right) + \left(\frac{y_1}{2}\right) N_1 \exp\left(-L_1/\lambda_1\right) + \frac{S_{12}}{2} \tag{5.16}$$

$$N_2 = \left(\frac{y_1}{2}\right) M_1 \exp\left(L_1/\lambda_1\right) + \left(\frac{x_1}{2}\right) N_1 \exp\left(-L_1/\lambda_1\right) + \frac{S_{12}}{2} \tag{5.17}$$

Where, $\alpha_2 = \left[\frac{V_{bi}\left(g_1-2\right) - 2V_{ds} + 2S_{12}\cosh\left(L_2/\lambda_2\right) - 2F_2 + g_1F_1}{g_1 - F_1}\right]$, here,

$g_1 = x_1\exp\left(p_1\right) + y_1\exp\left(q_1\right)$, $h_1 = x_1\exp\left(-p_1\right) + y_1\exp\left(-q_1\right)$, $x_1 = 1 + \frac{\lambda_2}{\lambda_1}, y_1 = 1 - \frac{\lambda_2}{\lambda_1}$,

$p_1 = \frac{L_1}{\lambda_1} + \frac{L_2}{\lambda_2}, q_1 = \frac{L_1}{\lambda_1} - \frac{L_2}{\lambda_2}, S_{12} = \phi_{01} - \phi_{02}, F_1 = V_{fb_1}{}' + \frac{qN_a\lambda_1{}^2}{\varepsilon_{Si}}, F_2 = V_{fb_2}{}' + \frac{qN_a\lambda_2{}^2}{\varepsilon_{Si}}, \quad \beta_2 = \frac{2-g_1}{g_1-h_1}$,

$\alpha_1 = V_{bi} + F_1 - \alpha_2$, $\beta_1 = -1 - \beta_2$

5.3.2. Threshold Voltage Modeling

The value of gate voltage at which the inner potential minimum is equal to twice the Fermi Potential is termed as the threshold voltage. It is essential to locate the position of inner potential minimum (that occurs in Region 1) to formulate the threshold voltage. Thus the position of inner potential minimum can be obtained using the following equation:

$$\frac{d\psi_{01}(z)}{dz} = 0 \tag{5.18}$$

The position of minimum inner potential thus obtained is given as:

$$z_{\min} = \frac{\lambda_1}{2}\ln\frac{N_1}{M_1} \tag{5.19}$$

Equating minimum Inner potential to twice the Fermi potential, the expression of threshold voltage thus obtained is:

$$V_{th} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{5.20}$$

Where, $a = 4\beta_1\beta_2 - 1$, $b = 2\left[2\left(\alpha_1\beta_2 + \alpha_2\beta_1\right) + f_1\right]$, $c = 4\alpha_1\alpha_2 - f_1{}^2$, with $f_1 = 2\phi_f + F_1$

- Subthreshold Swing (in mV/dec) [5.13] is given as follows:

$$SS = 2.3V_t\left[\frac{d\psi_{0\min}(z)}{dV_{gs}}\right]^{-1} \tag{5.21}$$

5.3.3. Sensitivity Analysis

Sensitivity analysis of the proposed biosensor can be obtained using the following equations

For neutral biomolecules, sensitivity is given as [5.14]:

$$S_{n,bio} = \left|\frac{V_{th}(K=1) - V_{th}(K>1)}{V_{th}(K=1)}\right| \tag{5.22}$$

For charged biomolecules, sensitivity is given as:

$$S_{c,bio} = \left|\frac{V_{th}(Bio_{neutral}) - V_{th}(Bio_{charged})}{V_{th}(Bio_{neutral})}\right| \tag{5.23}$$

5.3.4. Drain Current Modeling

Drain current analysis can be summed up using the unified model as follows [5.15]:

$$I_{ds} = \begin{bmatrix} I_{sub,}\, 0 \le V_{gs} \le V_{th} \\ I_{lin}, V_{th} \le V_{gs} \le V_{sat} \\ I_{sat}, V_{sat} \le V_{gs} \le 1.0 \end{bmatrix} \tag{5.24}$$

Subthreshold current is within the limit $0 \le V_{gs} \le V_{th}$

In the proposed device, electron current in the channel is given as follows [5.16]:

$$I_{DS}(z) = \int_{r_1}^{r_2} 2\pi R J(r,z)\, dr \tag{5.25}$$

Diffusion current density is expressed as:

$$J(r,z) = \frac{\mu_{eff}}{1+\theta(V_{gs}-V_{th})} q n_i(T) \exp\left(\frac{\psi_{01\min} - V}{V_T}\right)\frac{dV(z)}{dz} \tag{5.26}$$

Where, $V_t = \dfrac{KT}{q}$

Substituting equation (5.26) into (5.25), we get,

$$I_{DS}\int_0^L dz(z) = \frac{\mu_{eff}}{1+\theta(V_{gs}-V_{th})} \pi\left(r_2^2 - r_1^2\right) q n_i(T) \int_0^{V_{ds}} \exp\left(\frac{\psi_{01\min} - V}{V_T}\right) dV(z) \tag{5.27}$$

Thus, the final expression for subthreshold drain current is given as:

$$I_{DS} = \frac{\mu_{eff}}{1+\theta\left(V_{gs}-V_{th}\right)}\pi\frac{\left(r_2^{\,2}-r_1^{\,2}\right)}{L}qn_i\left(T\right)\exp\left(\frac{\psi_{01\min}}{V_T}\right)V_T\left[1-\exp\left(-V_{ds}/V_T\right)\right] \tag{5.28}$$

Here, $\mu_{eff} = \frac{\mu_n}{\sqrt{\left(1+\frac{Na}{N_{ref}+NaS_1}\right)}}$, μ_n being the electron mobility, S_1 and θ are fitting parameters.

Expression for linear drain current is given as:

$$I_{DS,lin} = \frac{2\pi\left(r_2-r_1\right)\mu_{eff}C_{f_1}E_c}{\left(E_cL+V_{ds}\right)}\left[\left(V_{gs}-V_{ths}\right)^{\frac{\alpha}{2}}V_{ds}-\frac{\theta_{short}V_{ds}^{\,2}}{2}\right] \tag{5.29}$$

Where, E_c is the critical electric field, for long channel devices $\alpha = 2$ to $\alpha = 1$ for short channel devices. $\theta_{short} = \frac{0.1}{\left[\frac{d\psi_{0\min}}{dV_{gs}}\right]}$ at $V_{gs} = V_{th}$, $V_{ths} = V_{th}\left(1-\theta_{short}\right)$. To incorporate the SCEs, E_c, θ_{short}, V_{ths} have been incorporated.

Expression of saturation current where V_{ds} is replaced by V_{dsat} is given as:

$$I_{DS,sat} = \frac{2\pi\left(r_2-r_1\right)\mu_{eff}C_{f_2}}{\left(1+\frac{V_{dsat}}{E_c\left(L-L_{sat}\right)}\right)\left(L-L_{sat}\right)}\left[\beta\left(V_{gs}-V_{ths}\right)^{\frac{\alpha}{2}}V_{dsat}-\frac{\theta_{short}V_{dsat}^{\,2}}{2}\right] \tag{5.30}$$

Where, $V_{dsat} = V_{gs}-V_{ths}$, β being a technology dependent empirical fitting parameter

5.4. Results & Discussions

The analytical results of this section have been validated using simulation outcomes from Silvaco Atlas. Several physics based model such as Drift-Diffusion model for carrier transport, CVT (Lombardi) mobility model, Shockley-Read Hall recombination for fixed lifetimes, Parallel electric field dependent FLDMOB model, Auger recombination model, Concentration dependent CONMOB model, INTERFACE statement to define the type and density of localized/fixed charges have been used to obtain the simulation outputs. Filler radius of 10nm and outer radius of 20nm are considered to obtain analytical and simulation results. Fig.5.3 reveals the graphical plot of inner potential distribution along the channel length for proposed biosensor for different K-values of different neutral biomolecules placed

in the nanogap. Firstly, the proposed biosensor has a Dual-Material Gate incorporated in its architecture, this Dual-Material (GWFE scheme enabled) gate results in the formation of a unique step profile in the inner potential distribution along with the formation of a source-shifted minimum. This unique step profile shields the inner potential minimum from getting affected from fluctuating drain voltages. This invariably implies an upgraded immunity of the proposed biosensor from DIBL effect. Now, when the biomolecules (K>1) are absent in the nanogap and the nanogap is filled with air (K=1), the effective oxide thickness (EOT) increases resulting in a weakened gate-channel coupling which inevitably leads to substantially reduced threshold voltage. Hence for the case K=1, the source-channel barrier height is the lowest of all other cases (K>1). Now when a neutral biomolecule (K>1) is present in the nanogap, the gate-channel coupling gets better due to reduced EOT compared to the case for K=1. Thus, the source-channel barrier height increases from the previous case (i.e. for K=1), this, in turn, increases the threshold voltage from the previous case. This shift of threshold voltage from the case when the nanogap is filled with air, offers a metric to detect the biomolecule type. Also, as the K-value increases, EOT reduces leading to higher source-channel barrier height that inexorably causes the threshold voltage to augment significantly. Inner potential distribution along the channel length for different types of charged biomolecules (K=5), having different magnitudes of positive and negative charges, placed in the nanogap, is demonstrated in fig. 5.4. When a positively charged biomolecule of high magnitude such as $5x10^{15}m^{-2}$ is placed in the nanogap, then as per the equation $V_{fb_1}' = V_{fb_1} - \frac{qN_f}{C_{f_1}}$ (also shown in Inner potential modeling section), effective flat-band voltage V_{fb_1}' decreases. Thus, as per equation $V_{gs_1} = V_{gs} - V_{fb_1}'$, for an applied gate voltage, effective gate voltage increases and starts reducing the source-channel barrier height thereby ultimately reducing the threshold voltage. Now, when a negatively charged biomolecule having high magnitude is placed in the nanogap, the effective flat-band voltage increases. Thus for an applied gate voltage, the effective gate voltage decreases and hence a higher gate voltage is necessary to start the conduction. The inevitable result of this is an increased source-channel barrier height that escalates the threshold voltage. This explains the fig.5.4 where the more positive the charge of the biomolecule is, the more diminished is the threshold voltage and

the more negative the charge of biomolecule is, the more enhanced is the threshold voltage. Fig.5.5 exhibits the graphical plot of threshold voltage variation vs. dielectric constant of neutral biomolecules and for two different nanogap thicknesses and two different values of outer radii keeping filler radius fixed at 10nm. Firstly, it can be clearly observed that threshold voltage gradually increases with increase in K-value of the neutral biomolecules as already explained for fig.5.3. Now, threshold voltage increases with outer radius 20nm compared to the case when outer radius is 25nm. This can be attributed to the fact that when the outer radius has lower value, the channel thickness decreases that allows the gate to have an increased control over the channel. Thus the threshold voltage increases thereby reducing the off-state leakages and diminishes the device power consumption. Now, threshold voltage is found to increase when the nanogap thickness is 9nm compared to the case with 11nm. This happens because with 9nm nanogap thickness, the EOT is reduced and gate-channel coupling gets enhanced leading to increased threshold voltage and notable reduction in power consumption. It is important to mention here that when nanogap thickness is considered to be 9nm, t_2 is also 9nm and when nanogap thickness is 11nm, t_2 is also 11nm. Fig.5.6 exhibits the threshold voltage variation vs. charge of biomolecules (K=5) for two different nanogap thicknesses and two different values of outer radii keeping inner radius fixed at 10nm. Firstly, threshold voltage is found to be significantly higher for negatively charged biomolecules having higher magnitudes of charge due to increased source channel barrier height as already discussed in fig.5.4. Threshold voltage gradually decreases with increase in magnitude of positive charge due to reduced source-channel barrier height. Now, for lower outer radius, threshold voltage increases owing to better gate-channel coupling and for lower nanogap thickness, EOT decreases, and gate control over channel increases leading to enhanced threshold voltage as already discussed for fig.5.5. Sensitivity vs. dielectric constant of neutral biomolecules for proposed biosensor and its Dual-Material (DM) Full channel Cylindrical Counterpart is exhibited through the graphical illustration in fig.5.7. The prime reason for selecting the macaroni-configured MOSFET lies in the fact that it offers higher sensitivity compared to its DM Full channel Cylindrical Counterpart (having identical device parameters and biasing conditions). Also, both the biosensors exhibit higher sensitivity for neutral biomolecules having higher K-values, with the proposed biosensor showing higher values of sensitivity. Fig. 5.8 shows the graphical plot of sensitivity vs. charge

of biomolecules for proposed biosensor and its DM Full channel Cylindrical Counterpart. The proposed biosensor exhibits higher values of sensitivity compared to its DM Full channel Cylindrical Counterpart. For both the biosensors, as the magnitude of charge increases, sensitivity also increases, however, both the biosensors are found to be slightly more sensitive to negatively charged biomolecules. Sensitivity analysis for both neutral and charged biomolecules for both type of biosensors exhibit that macaroni-configured MOSFET biosensor offers better sensitivity and is a superior choice compared to the conventional cylindrical biosensors. Fig. 5.9 exhibits Subthreshold Swing variation vs. different channel lengths for two different outer radii (keeping filler radius fixed at 10nm) and for two different oxides placed above SiO_2 in region 2. For an outer radius of 25nm (with HfO_2/SiO_2 gate stack in Region 2), Subthreshold swing is highest which degrades the device performance. While for an outer radius of 20nm offers improved subthreshold swing response with HfO_2/SiO_2 gate stack in Region 2, however, noteworthy upsurge in subthreshold swing is observed when HfO_2 over the SiO_2 layer in the gate stack in region 2 is replaced by only SiO_2. Hence, the gate stack configuration of HfO_2/SiO_2 in region 2 helps to realize better subthreshold characteristics enabling improved performance of the recommended biosensor.

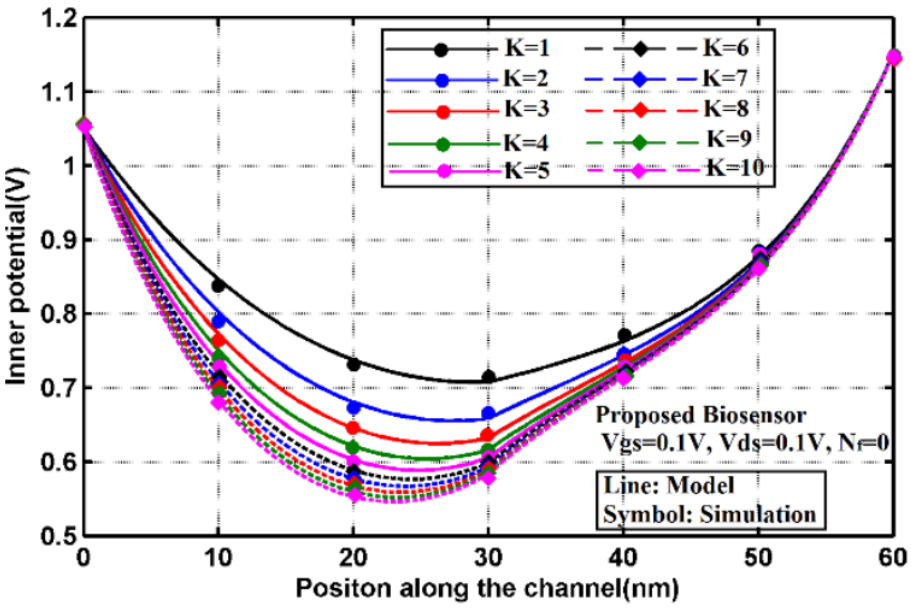


Fig. 5.3. Inner potential distribution along the channel length for proposed biosensor for different K-values of different neutral biomolecules placed in the nanogap

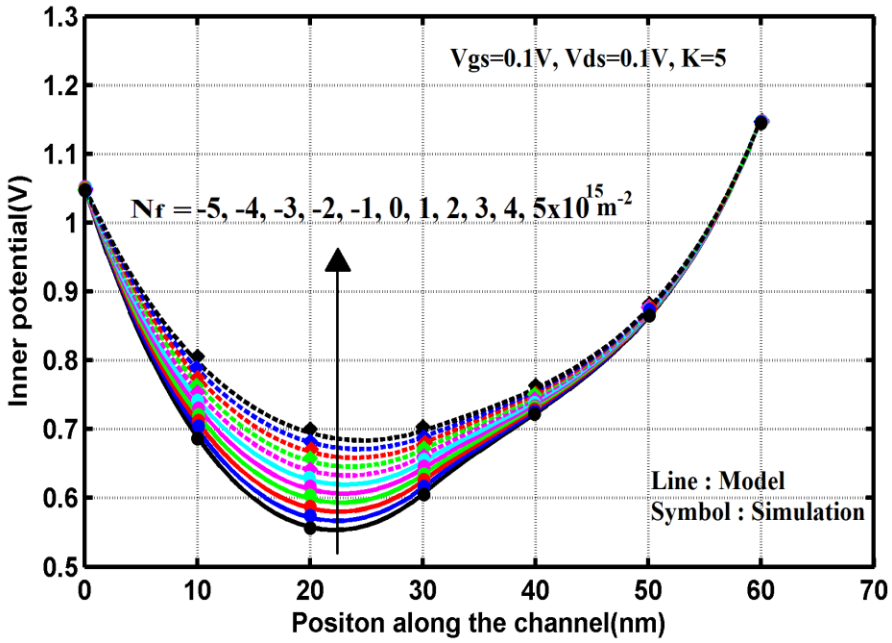


Fig. 5.4. Inner potential distribution along the channel length for proposed biosensor for different charged biomolecules (positive, negative) placed in the nanogap

Fig.5.10 demonstrates the Drain current variation with gate voltage for the proposed biosensor in presence (K>1) and also in absence of biomolecules (K=1). The off-state current is found to substantially change with change in K-value whereas the final On-state current is same for all the cases. In absence of biomolecules in the nanogap (K=1), threshold voltage is the lowest resulting in highest off-state current among all other cases with K>1. For higher values of K, off-state current considerably reduces as seen from the plot. Fig.5.11 demonstrates the Drain current variation with gate voltage for the proposed biosensor in presence of charged biomolecules. For all the cases, the off-state current significantly varies while the final On-state current remains the same. For more positively charged biomolecules, threshold voltage gets largely reduced resulting in high off-state current compared to the neutral biomolecule having same K-value. For more negatively charged biomolecules, threshold voltage gets largely enhanced resulting in reduced off-state current compared to the neutral one. Thus, threshold voltage shifts are responsible in controlling the off-state drain currents. Analytical and simulation results match well validating our projected biosensor's superior performance.

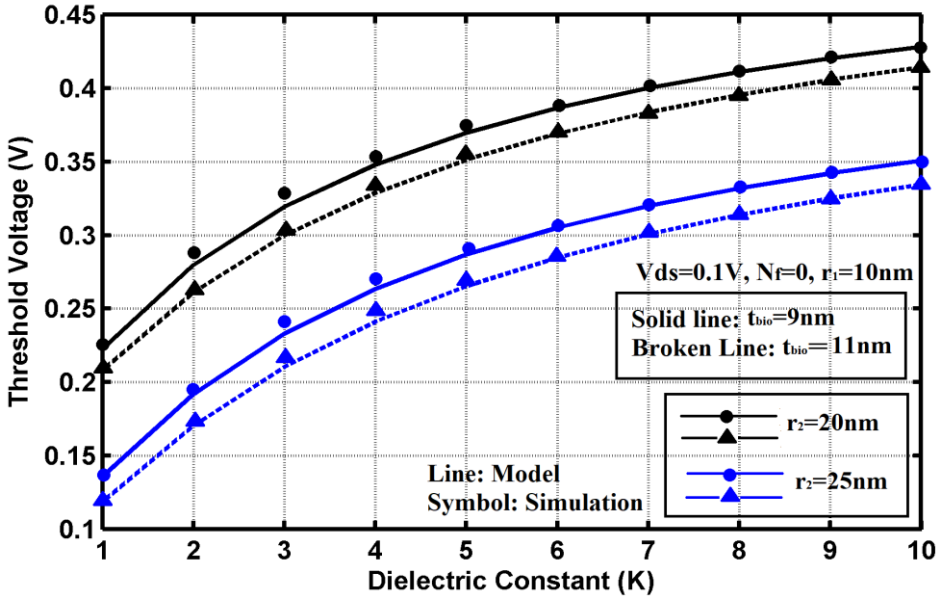


Fig. 5.5 Threshold voltage variation vs. dielectric constant of neutral biomolecules for two different thicknesses of nanogap and for two different outer radii values and fixed filler radius

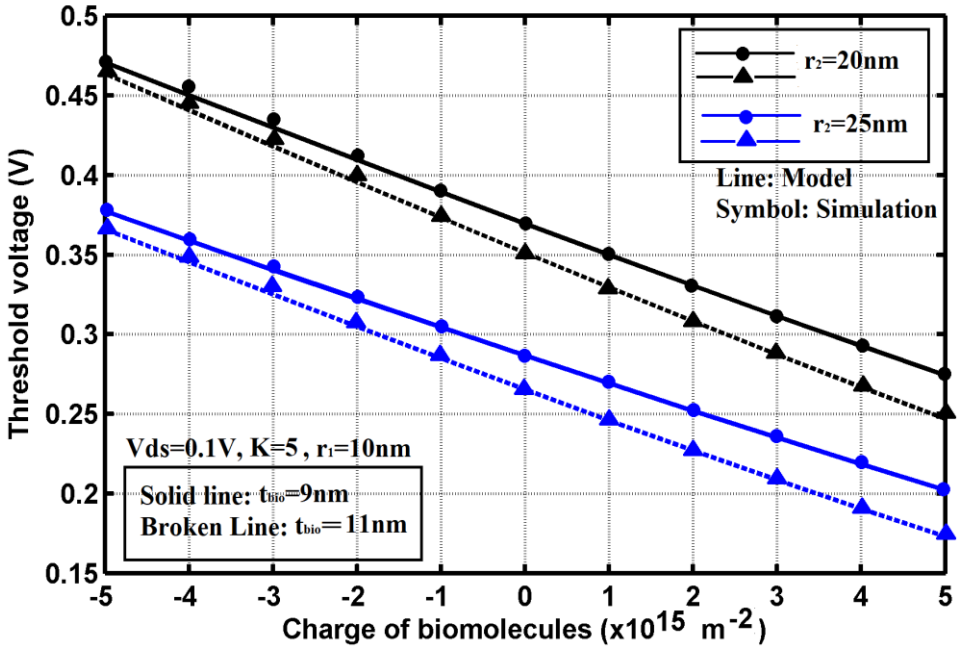


Fig. 5.6 Threshold voltage variation vs. charge of biomolecules (K=5) for two different thicknesses of nanogap and for two different outer radii values and fixed filler radius

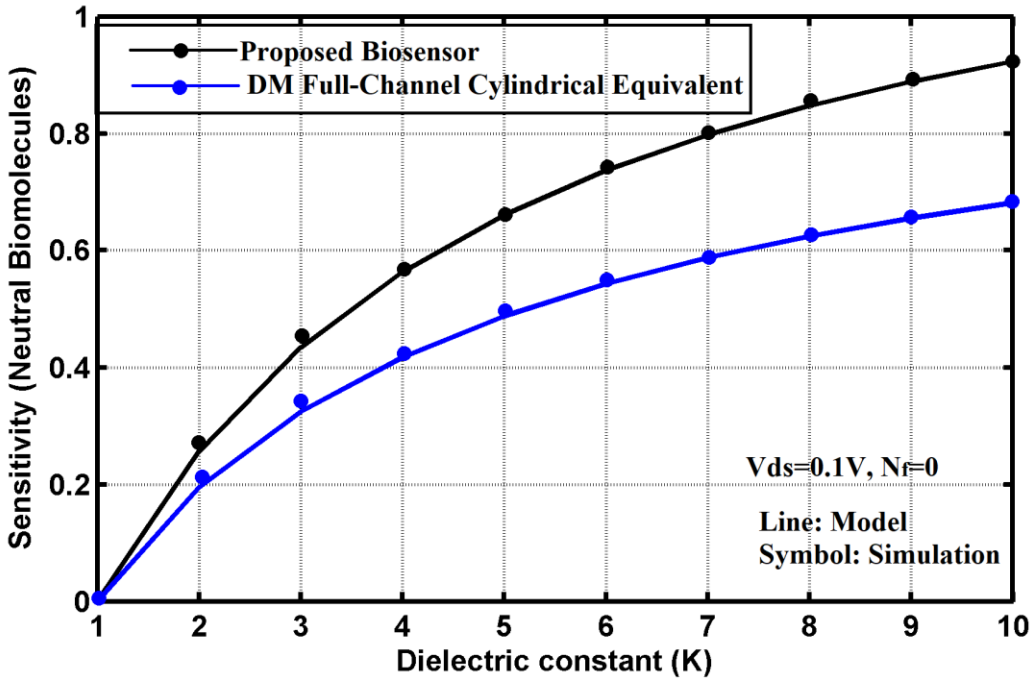


Fig. 5.7 Sensitivity vs. dielectric constant of neutral biomolecules for proposed biosensor and its DM Full Channel Cylindrical Equivalent

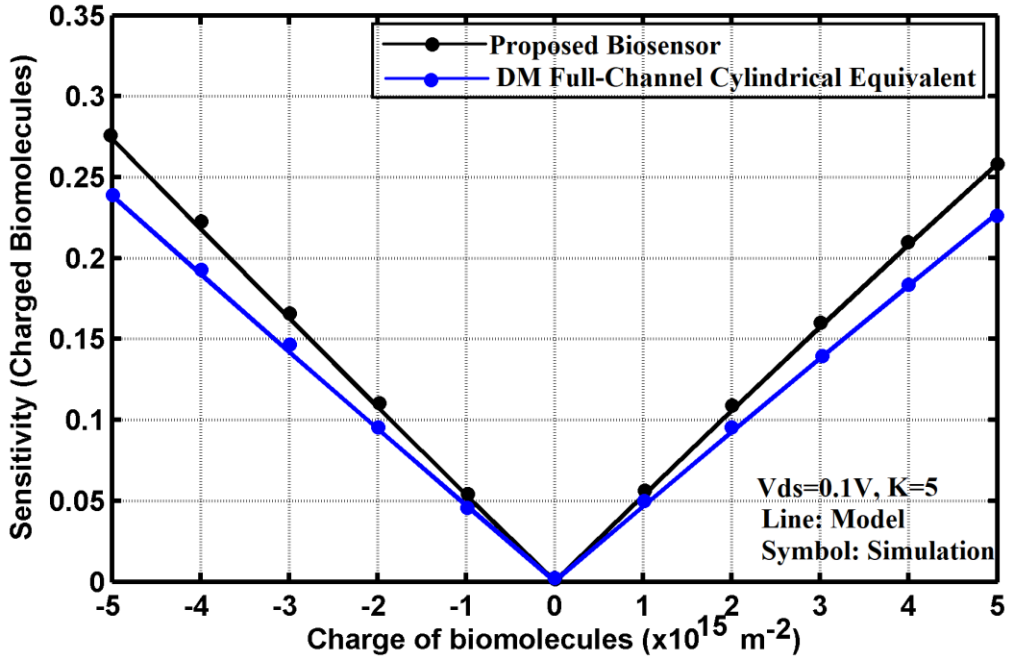


Fig. 5.8 Sensitivity vs. charge of biomolecules for proposed biosensor and its DM Full channel Cylindrical Counterpart

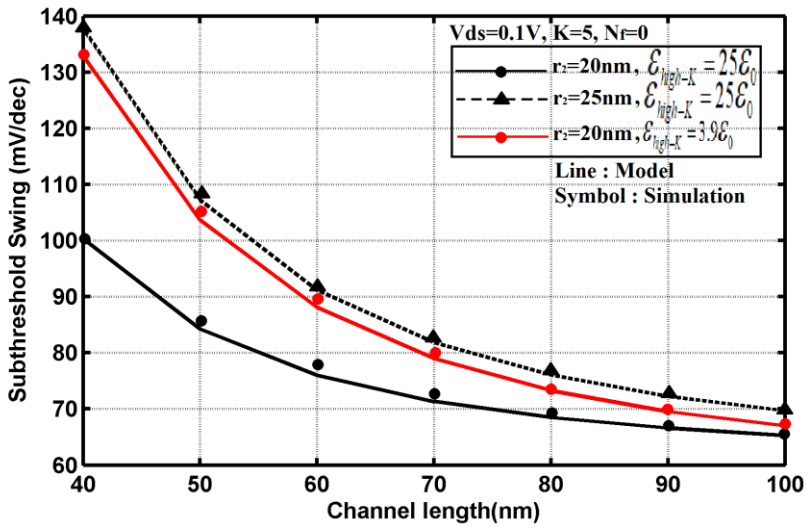


Fig. 5.9 Subthreshold swing variation for different channel lengths for two different outer radii (keeping filler radius fixed at 10nm) and for two different oxides above SiO_2 in region 2

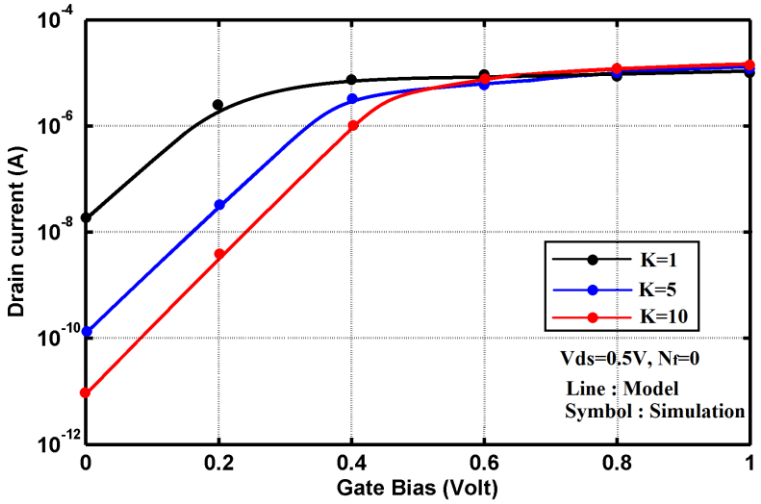


Fig. 5.10 Drain Current vs. Gate voltage for proposed biosensor for neutral biomolecules in the nanogap

5.5. Conclusion

Present investigation explores the performance of a Macaroni channel Dual-Material Gate MOSFET as a biosensor for neutral as well as charged biomolecule detection. Alterations in device characteristics such as inner potential, threshold voltage, drain current are observed due to the presence of neutral/charged biomolecules in the nanogap. A shift in threshold

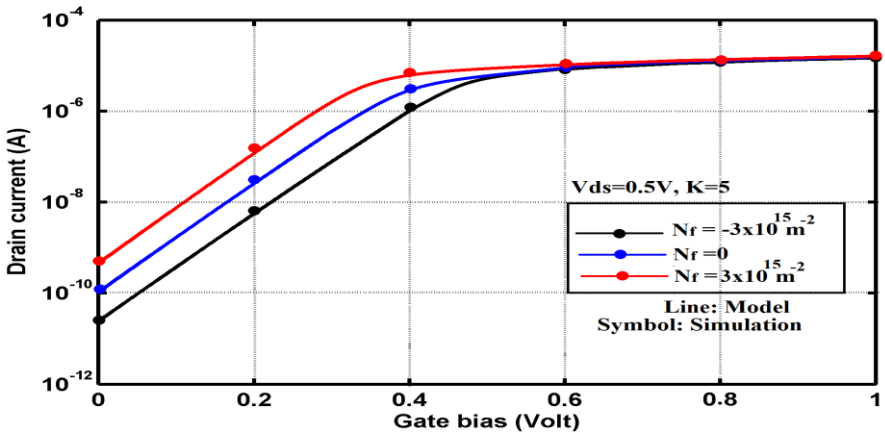


Fig. 5.11 Drain Current vs. Gate voltage for proposed biosensor for charged biomolecules in the nanogap

voltage provides a metric to sense the biomolecule type present in the nanogap and to realize the sensitivity of the recommended biosensor. Device features largely depend on the outer radius selection and short channel effects like threshold voltage reduction, subthreshold swing degradation can be effectively diminished with apposite outer radius selection. Incorporation of HfO_2-SiO_2 gate-stack towards drain end effectively improves subthreshold swing response of the biosensor. Relative threshold voltage alteration based sensitivity analysis exhibits that the projected biosensor offers grander sensitivity performance as compared to its DM Full-channel Cylindrical Equivalent. For all neutral biomolecules, the final on-state current is same with the off-state current only changing with biomolecule type due to a change in threshold voltage with biomolecule type, the same happens for all kinds of charges of charged biomolecule too. Analytical results are in good agreement with simulated results evidencing advanced, potential implementations of the recommended biosensor in future specimen identifying applications.

Relevant Publication

Pritha Banerjee, Jayoti Das, "Analytical Exploration and Simulation of Dual-Material Gate Macaroni Channel MOSFET biosensor using dielectric-modulation technique", **Micro and Nanostructures**, **Elsevier**, Volume 165, 2022, 207196, ISSN 2773-0123, https://doi.org/10.1016/j.micrna.2022.207196. [SCIE, IF: 2.658]

References

[5.1] El Hamid, H.A., Iñiguez, B., Kilchytska, V. et al., "An analytical 3D model for short-channel effects in undoped FinFETs", J Comput Electron 14, 500–505, 2015. https://doi.org/10.1007/s10825-015-0678-0

[5.2] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis and G. Ghibaudo, "Semi-Analytical Modeling of Short-Channel Effects in Si and Ge Symmetrical Double-Gate MOSFETs," in IEEE Transactions on Electron Devices, vol. 54, no. 8, pp. 1943-1952, Aug. 2007, doi: 10.1109/TED.2007.901075

[5.3] Chunsheng Jiang, Renrong Lianga, Jing Wang and Jun Xu, "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs", AIP Advances 5, 057122, 2015, https://doi.org/10.1063/1.4921086

[5.4] A. Goel, S. Rewari, S. Verma and R. S. Gupta, "Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA) for DNA Bio-Molecule Detection," 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 2018, pp. 337-340, doi: 10.1109/EDKCON.2018.8770406

[5.5] Q. Nguyen-Gia, M. Kang, J. Jeon and H. Shin, "Characteristic Length of Macaroni Channel MOSFET," in IEEE Electron Device Letters, vol. 40, no. 11, pp. 1720-1723, Nov. 2019, doi: 10.1109/LED.2019.2942619.

[5.6] Pradhan, K.P.; Kumar, M.R.; Mohapatra, S.K.; Sahu, P.K., "Analytical modeling of threshold voltage for Cylindrical Gate All Around (CGAA) MOSFET using center potential", Ain Shams Engineering Journal, S2090447915000647, 2015, doi:10.1016/j.asej.2015.04.009

[5.7] Reddi Ganapati, Visweswara Rao Samoju, Bhaskara Rao Jammu, "Analytical Modeling of Threshold Voltage for Dual-Metal Double-Gate Gate-All-Around (DM-DG-GAA) MOSFET", Silicon 13, 2869–2880, 2021, https://doi.org/10.1007/s12633-020-00602-2

[5.8] Q. Nguyen-Gia, M. Kang, J. Jeon and H. Shin, "Characteristic Length of Macaroni Channel MOSFET," in IEEE Electron Device Letters, vol. 40, no. 11, pp. 1720-1723, Nov. 2019, doi: 10.1109/LED.2019.2942619.

[5.9] Aniruddh Sharma, Arushi Jain, Yogesh Pratap, R.S. Gupta, "Effect of high-k and vacuum dielectrics as gate stack on a junctionless cylindrical surrounding gate (JL-CSG) MOSFET", Solid-State Electronics 123:26-32, 2016, DOI: 10.1016/j.sse.2016.05.016

[5.10] S K Mohapatra, K P Pradhan, P K Sahu, G S Pati and M R Kumar, "The effect of interface trapped charges in DMG-S-SOI MOSFET: a perspective study", Adv. Nat. Sci.: Nanosci. Nanotechnol. 5 (2014) 045015 (7pp)

[5.11] Yuh-Sheng Jean and Ching-Yuan Wu, "The Threshold–Voltage Model of MOSFET Devices with Localized Interface Charge", IEEE Transactions on Electron Devices, VOL. 44, NO. 3, March 1997

[5.12] Das, R., Chattopadhyay, A., Chanda, M. et al., "Analytical Modeling of Sensitivity Parameters Influenced by Practically Feasible Arrangement of Bio-Molecules in Dielectric Modulated FET Biosensor", Silicon (2022). https://doi.org/10.1007/s12633-021-01617-z

[5.13] Ashok Kumar Raghav, Amit Sharma, Rashmi Gupta and Neeraj Gupta, "Subthreshold modeling of dual-halo dual-dielectric triple-material surrounding-gate (DH-DD-TM-SG) MOSFET for improved leakages", Journal of Engineering Research, Vol 8 No 2, 2020

[5.14] R. Narang, M. Gupta, M. Saxena and R. S. Gupta, "Analytical model for a dielectric modulated double gate FET (DM-DG-FET) biosensor," 2012 International Conference on Emerging Electronics, 2012, pp. 1-4, doi: 10.1109/ICEmElec.2012.6636256.

[5.15]] S. Rewari, V. Nath, S. Haldar, S. S. Deswal and R. S. Gupta, "Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET," in IEEE Transactions on Electron Devices, vol. 65, no. 1, pp. 3-10, Jan. 2018, doi: 10.1109/TED.2017.2771814.

[5.16] Arobinda Pal, Angsuman Sarkar, "Analytical study of Dual Material Surrounding Gate MOSFET to suppress short-channel effects (SCEs)", Engineering Science and Technology, an International Journal, 17, 205-212, 2014

Chapter 6

Chapter 6 : Concluding Remarks and Scope of Future Work

6.1. Concluding Remarks

6.1.1 Brief Outcomes from Each Chapter

6.2. Scope of Future Work

6.1. Concluding Remarks

A conclusive statement is an inherent part of a thesis work and it adds to the inclusiveness of the thesis. The primary objective of the thesis has been to investigate the electrical characteristics of advanced, ultra-thin Nano MOSFET devices with strategically implemented novel technologies of Multi-gate, gate work function engineering, channel and dielectric-engineering. The scheme of dielectric engineering has been implemented using dielectric-modulation technique for employment of advanced Nano MOSFET device to work as an efficient biosensor and demonstrated in chapter 2 and 5. Chapter 2, for the first time, has demonstrated the biosensing capability of an advanced GWFE Trigate MOSFET biosensor. However, Cylindrical Gate-all-around (CGAA) devices are currently the prime choice since the device offers upgraded performance. Hence, it has been selected as the basic device for biosensing implementation in many published researches. Thus, a part of this research encompasses a strategically designed advanced CGAA MOSFET and its properties have been thoroughly investigated to implement the device in future practical applications. Inspite of offering better performance, CGAA MOSFETs have remained in the second position with the first position being replaced by Macaroni channel GAA MOSFETs. These advanced devices offer excellent device performance and thus, owing to the above stated fact, an advanced Macaroni channel GAA MOSFET has been strategically designed and its properties have been investigated thoroughly so as to implement the device as an efficient biosensor. This investigation has been highlighted in chapter 4. Finally chapter 5 deals with the biosensing property of an advanced Macaroni channel MOSFET biosensor, for the first time, using dielectric-modulation technique and the detailed sensitivity analysis has been conducted through proper mathematical modeling and results have been validated using simulation outcomes from proper simulation softwares. The overall interpretation of the research conducted has been summarized through chapters from 2 to 5 with chapter 1 presenting a brief overview of the contemporary literature associated with the topic of research.

6.1.1 Brief Outcomes from Each Chapter:

Chapter 2: For the past few decades, the semiconductor industry has witnessed its remarkable progress and technological resurgence as an outcome of the unquenchable

demands of the present consumer markets for sleeker devices enabled with improved speed, lower power consumption and cost-effectiveness. Device miniaturization, following the trend of Moore's law, has been the prime guiding mechanism to obtain devices with the above said features. However, with aggressive scaling in nanometer dimensions, this fanatic pace of miniaturization of devices has been accompanied by some inevitable short channel effects that tend to severely degrade the device performance. Such SCEs namely threshold voltage roll-off, Drain-induced barrier lowering, increased subthreshold swing, degrading hot carrier effects, impact ionization followed by parasitic BJT effects, increased subthreshold leakage current have cumulatively acted in deteriorating device performance. Thus, device scaling has to be coupled with some innovation in technologies to suppress these detrimental SCEs thereby offering enriched device performance.

One of the several innovative technology is the implementation of Trigate in a MOSFET device as exhibited in chapter 2. Trigate technology falls under the scheme of multi-gate incorporation to mitigate several SCEs thereby boosting device speed initiating lower power consumption. This can be attributed to the fact that the gate can have precise control over the channel since the area increases by three times for the electrons to travel. To further boost the gate-channel coupling, a back/bottom gate has been incorporated in the structure. Gate work function engineering (GWFE) added further enhances SCE immunization. The Dual-material gate employed helps in the formation of surface potential minimum towards source side, a step profile and a reduced slope of surface potential towards drain side compared to the counterpart without GWFE (vide fig. 2.3, 2.4, 2.5). A significant reduction in threshold voltage roll-off can be achieved by selection of gate length ratio of the two gate materials in the dual-material gate (vide fig.2.8). Significant reduction in DIBL is possible with GWFE as evident through fig.2.11 and HCE can be diminished to a large extent as evident in fig.2.15-2.17. Incorporation of high-K gate stack towards drain end causes significant improvement in subthreshold swing (vide fig.2.12). Apart from this, dielectric-modulation technique that has been incorporated in the device helps in efficient biosensing (vide fig.2.3, 2.4, 2.7, 2.9, 2.10). Detailed sensitivity analysis shows the biosensor is more sensitive to neutral biomolecule having higher K value and also sensitivity increases as

channel length increases. For charged biomolecules, the recommended biosensor offers higher sensitivity for negatively charged biomolecule having lower K value. Some of the device parameters also alter device features as illustrated in detail in the chapter.

Chapter 3: Cylindrical Gate-all-around (CGAA) MOSFETs are highly favored as the basic device to implement biosensing applications. This can be attributed to the fact that CGAA MOSFETs offer enriched device performance coupled with high degree of SCE immunization. Thus, an advanced CGAA MOSFET has been skilfully designed in chapter 3 so as to implement the device in future real-time biosensing applications. However, before the planned CGAA device can be implemented to work as an efficient biosensor, the electrical characteristics of the advanced device needs to be investigated in detail and this has been highlighted in chapter 3. Additionally, fixed interface trap charge and temperature induced analytical modeling and simulation of a Dual-material CGAA MOSFET having a Gaussian-doped channel has been considered in this chapter. Temperature has a colossal effect on device characteristics. Within a range of 100K – 500K, the silicon channel features such as bandgap, intrinsic concentration, Fermi level, flat-band voltage etc. show dependence on temperature. Apart from this, the quality of Si-SiO_2 interface plays a major role in determining reliable device performance. This interface tends to get damaged due to several stress, radiation, hot carrier, fabrication related process etc. These damages result in the formation of positive/negative charges at the interface. These charges modulate the flat-band voltage which consequently modulate the source-channel barrier height causing the threshold voltage of the device to undergo significant alterations. These charges also alter the thermal behavior of the device (vide fig.3.3, 3.4, 3.5). The Gaussian-doping parameters like peak doping, projected range straggle have substantial effects on device features (vide fig. 3.4, 3.6, 3.7). GWFE causes DIBL and HCE reduction (vide fig.3.10, 3.11). Temperature also alter subthreshold swing as evident from fig.3.8. Some of the device parameters also alter device features as illustrated in detail in the chapter.

Chapter 4: Owing to the fact that Macaroni GAA MOSFET offer improved device performance even better than conventional CGAA MOSFETs, the mathematical modeling and

simulation of the fixed interface trap charge and temperature induced electrical behavior of a Dual-material Macaroni channel MOSFET having a graded concentration in the channel has been highlighted and demonstrated in chapter 4. Macaroni MOSFET is topologically identical to CGAA with the only exception that there is a hollowed insulating pillar at the center of the Macaroni structure. This causes the channel to become thin thereby enabling higher gate control over the channel which substantially contributes to SCE immunization. Motivated by the above stated fact related to enhanced performance of Macaroni structures, an advanced Macaroni channel CGAA MOSFET has been strategically designed for its suitable implementation as an efficient biosensor. However, the electrical characteristics of the projected device have been investigated in chapter 4 before the projected device can be implemented to work as a biosensor. Additionally, localized trap charge induced thermal behavior of the device has also been considered. Temperature and trap charge induced effects on potential, threshold voltage are exhibited through fig.4.4, 4.5, 4.6, 4.8, and 4.11. Temperature is found to significantly influence the short channel response of the device as evident from fig.4.14, 4.15. Graded channel resists threshold voltage reduction offering the flexibility of suitable selection of threshold voltage of the device through proper selection of the graded doping concentration (vide fig. 4.13). Comparative investigation of the projected device and its Dual-material full channel CGAA exhibits improved SCE resistance in the former compared to the latter (vide fig. 4.12, 4.14, 4.16). A relative research of the projected device with its Single-material gate counterpart offers the evidence of superior SCE immunization in the former over the latter (vide fig.4.14, 4.17, 4.19). The research also includes a study of Gate-induced drain leakage mechanism through modeling of GIDL current that is illustrated in fig.4.18 and 4.19. Finally, the drain current analysis exhibits that due to a change in the threshold voltage for various types of trapped charges, there is a change in the off-state current only. Also, these charges have significant influence on GIDL current (vide fig.4.18). However, fig.4.19 clearly highlights the fact that GWFE can effectively decrease the GIDL current as observed from comparative drain current analysis of the projected device and its Single-material gate counterpart. Also, the projected device supports further scalability without much deterioration in device performance (vide fig. 4.6,

4.11). Some of the device parameters also alter device features as illustrated in detail in the chapter.

Chapter 5: Several existing literature survey reports as well as results obtained from chapter 4 establishes the fact that Macaroni MOSFETs have outclassed Cylindrical Gate-All-Around (CGAA) MOSFETs in terms of device performance. Through the observation of resukts presented in chapter 4, A dual-material gate (GWFE incorporated) Macaroni channel GAA MOSFET has been incorporated that further boosts device performance through formation of source-shifted minimum, step profile and reduced slope of potential (vide fig.5.3, 5.4). The projected biosensor shows shifts in threshold voltage for different types of biomolecules placed in the nanogap. These shifts in threshold voltage have been considered as a metric to detect the biomolecule type. The most important of all that the proposed biosensor shows more sensitivity for neutral/charged biomolecules when compared to their dual-material full channel CGAA MOSFET biosensor. CGAA MOSFET biosensor is one of the foremost choice of researchers due to the fact that CGAA MOSFET has inherent immunity to SCEs, higher current drivability and higher packaging density, etc. The projected biosensor has even excelled CGAA MOSFET biosensor in terms of offering higher sensitivity (vide fig. 5.7, 5.8). Due to change in threshold voltage, there are consequent changes in the off-state drain current for different types of biomolecules, however, the on-state current remains unaffected (vide fig.5.10, 5.11). High-k gate stack towards drain end plays vital role in upgrading subthreshold swing characteristics (vide fig.5.9). Some of the device parameters also alter device features as illustrated in detail in the chapter.

For all the cases, analytical results have been validated using simulation outcomes using proper simulation softwares.

6.2. Scope of Future Work

This doctoral thesis supports several research contributions in the arena of some ultra-thin non-conventional MOSFET structures. However, the evolution of the semiconductor industry keeping pace with further device miniaturization so as to support the thumb rule of Moore's Law governed by stringent requirements that also undergo metamorphosis as per consumer demands, permits further research and development in the field of device innovation.

Some of the scopes of future work as thus listed as follows:

- Macaroni-channel MOSFETs being superior to Cylindrical Gate-all-around MOSFETs, the quantum mechanical analytical modeling can be carried out on these devices for extremely scaled channel lengths and widths.

- To eliminate the fabrication-associated difficulties of doping ultra-shallow source/drain junctions, Schottky barrier Macaroni MOSFETs can be devised, this will cut down the cost and allow higher SCE immunity, lower contact resistances due to metallic source/drain, excellent scalability can be achieved with these devices.

- Junctionless MOSFETs eliminate the necessity of fabricating source/drain regions, allow higher scalability, high SCE immunization etc. Hence Junctionless Macaroni devices can be implemented in research.

- Material property improvement such as incorporation of strain, halo doping etc. in Macaroni MOSFETs can boost carrier mobility, current drivability, offer the flexibility to tune to a preferred threshold voltage value and can cause effective suppression of major SCEs.

- New gate engineering techniques can be explored along with experimenting various type of doping concentration techniques in the channel and differently devised dielectric engineered gate-oxides to support further scalability and SCE resistances.

- Partial or full modification of geometries of existing advanced MOSFET devices can be considered to further upgrade the device performance, for example, Trigate with a bottom gate, Macaroni MOSFET having a hollow pillar of insulating material at channel center that have been already adopted in this thesis work. Such modifications can be further improvised for superior device performance.

******

Reprints of Published Papers Related to This Thesis

Silicon (2022) 14:419–428
https://doi.org/10.1007/s12633-020-00823-5

ORIGINAL PAPER

Gate Work Function Engineered Trigate MOSFET with a Dual-Material Bottom Gate for Biosensing Applications: a Dielectric-Modulation Based Approach

Pritha Banerjee[1] · Jayoti Das[1]

Received: 8 July 2020 / Accepted: 3 November 2020 / Published online: 16 November 2020

Abstract
Mathematical model development of a Dielectric-Modulated Dual Material Trigate MOSFET with a dual material bottom gate has been introduced for application as a biosensor for detection of biomolecules like enzymes, cell, DNA etc. With solution of 3-D Poisson's equation, electrical features of the proposed device have been acquired and corresponding shift in the device features due to change in permittivity, charge etc. by the biomolecules implies the type of biomolecule introduced in the nanogap. Further simulation results from Atlas corroborate the analytical results.

Keywords Dielectric modulation · Biosensor · Short channel effects (SCEs) · Work function engineering · Trigate MOSFETs

1 Introduction

In the contemporary era of technological renaissance, spectacular device features are accredited to the metrics of miniaturization, portability, cost effectiveness and improved speed. Escalated efficiency coupled with reduced power consumption can be achieved through device scaling that adds momentum to unimpeded device performances. However, aggressive downscaling limits the device performances due to severe Short channel effects that tends to weaken the reliability thereby degrading the device characteristics [1, 2]. Subjugating these reliability issues necessitate the incorporation of innovative technologies along with renovation of device architectures. Extensive researches to address the issues include implementation of Double Gate MOSFET to gain an enhanced gate control over the channel [3]. The advanced technology of gate work function engineering has also been considered in DG architectures to further ameliorate the device performances [4, 5]. However, in planar MOSFETs, gate dominance over the channel is constrained by restricted flow of electrons and hence exhibit poor immunity towards SCEs. Aggrandized performance with subdued SCEs can be achieved with Intel introduced trigate MOSFETs having 37% speed enhancement and 50% power reduction compared to planar structures as promulgated in [6]. In the current research, a trigate MOSFET is considered with gate work function engineering paving the way for superlative device features and the device is explored to work as a Biosensor for label free detection of biomolecules.

Bioelectronics has arisen as a nascent field embodying extensive gamut of advanced, prospective applications. FET-based Biosensors, which is one such application, are gaining prominence owing to their magnificent advantages such as direct transduction, miniaturization, higher sensitivity for label free detection of neutral (eg: proteins, enzymes etc.) and charged (such as DNA) biomolecules. Ample research endeavors highlighting the potential application of FET based Biosensors have been encountered where the gate oxide is etched to carve out a nanogap that holds the immobilized biomolecules. An SiO_2 layer beneath the nanogap acts as adhesion layer. Thus a change in gate capacitance due to a change in dielectric property of the biomolecules' type alter the device threshold voltage thereby providing a metric to sense the presence and type of biomolecule [7, 8]. Absence of biomolecule is marked by filling the nanogap with air ($K = 1$) whereas presence of biomolecule implies $K > 1$.

Additionally, the undertaken research venture encompasses the use of high-K TiO_2 over SiO_2 layer towards the drain end that effectively reduces the HCE leading to efficient power practices [9]. Simulation using Atlas provides results that validate the analytical results obtained.

✉ Pritha Banerjee
prithaedu7@gmail.com

Jayoti Das
jayoti.das@gmail.com

[1] Department of Physics, Jadavpur University, Kolkata, India

2 Device Architecture

Figure 1 illustrates the 3-D device structure under consideration. M_S is the gate towards source end with work function $\phi_{M_S} = 5.35eV$ and M_D is the gate towards drain end with work function $\phi_{M_D} = 4.4eV$.

The structure comprises of a Dual Material Trigate along with a bottom Gate plate with same composition. The gate work functions are chosen in such a way so that the surface potential minimum for the chosen range of neutral/charged biomolecules remain in region 1 with the minimum shifted mostly towards the source. This feature is highly desirable since a source-shifted minimum allows high immunity to DIBL, HCE and other prominent SCEs.

For devices without GWFE, the surface potential minimum remains at the middle of the channel and is highly prone to get affected from fluctuating drain voltages. This leads to severe performance degradation due to extreme SCEs. Detection in that case, gets severely hampered. This has been taken care of, in the present work. Hence, along with the procedure of biomolecule detection, the SCE response of the proposed biosensor has also been compared with the Single-Material (SM) gate structure, to prove the superiority of the former over the latter. The nanogap has a thickness $t_{bio} = 11$ nm, TiO_2 thickness $t_2 = 11$ nm, thickness of top SiO_2 layer $t_1 = 1$ nm. Thickness of bottom gate oxide (SiO_2) is $t_b = 2$ nm. P-type Si channel has a thickness $t_{ch} = 10$ nm and doping concentration $N_{ch} = 10^{17}$ cm^{-3}.Width (w) of the trigate device is 5 nm.

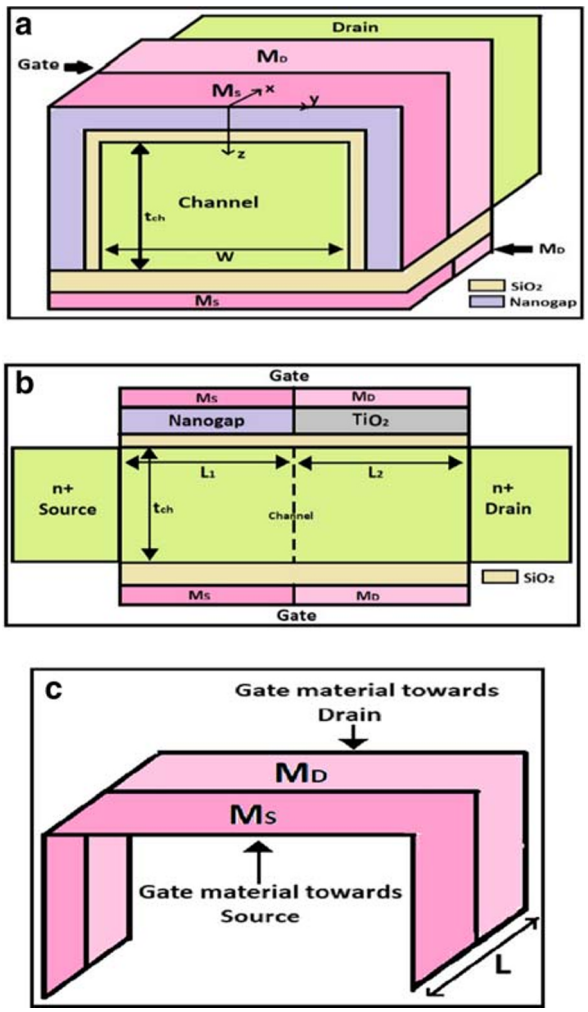


Fig. 1 **a**. 3-D Schematic illustration of the Proposed Biosensor. **b** 2-D Cross-sectional view of the proposed Biosensor. **c** 3-D Schematic illustration of the Dual- Material Trigate Configuration

3 Analytical Modeling

A detailed sensitivity analysis of the recommended biosensor necessitates the surface potential modeling of the device which is carried out by solving the 3-D Poisson's equation as follows:

$$\frac{\partial^2\varphi_i(x,y,z)}{\partial x^2} + \frac{\partial^2\varphi_i(x,y,z)}{\partial y^2} + \frac{\partial^2\varphi_i(x,y,z)}{\partial z^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \tag{1}$$

Here, $\varphi_i(x,y,z)$ is the potential in the ith region, i = 1 for region 1 with boundaries $0 \le x \le L_1, -\frac{w}{2} \le y \le \frac{w}{2}, 0 \le z \le t_{ch}$, i = 2 for region 2 with boundaries $L_1 \le x \le L_1 + L_2 (= L)$ $, -\frac{w}{2} \le y \le \frac{w}{2}, 0 \le z \le t_{ch}$.

The potential distribution between the side-wall gates is assumed to be parabolic [10], therefore,

$$\varphi_i(x,y,z) \approx c_{i0}(x,z) + c_{i1}(x,z)y + c_{i2}(x,z)y^2 \tag{2}$$

Now, at low drain voltages, potential distribution is parabolic in the z-direction [11], at y = 0, the expression obtained is:

$$\varphi_i(x,0,z) = c_{i0}(x,z) \approx \varphi_{spi}(x) + k_{i1}(x)z + k_{i2}(x)z^2 \tag{3}$$

Potential at the front and lateral interfaces, which is actually the surface potential, is given by

$$\varphi_i(x,0,0) = c_{i0}(x,0) = \varphi_{spi}(x) \tag{4}$$

Potential at the back channel-oxide interface is given by:

$$\varphi_i(x,0,t_{ch}) = c_{i0}(x,t_{ch}) \approx \varphi_{spi}(x) + k_{i1}(x)t_{ch} + k_{i2}(x){t_{ch}}^2 = \varphi_{sbi}(x) \tag{5}$$

Symmetry in the y-direction mathematically leads to

$$\varphi_i\left(x,-\frac{w}{2},z\right) = \varphi_i\left(x,+\frac{w}{2},z\right) \tag{6}$$

This mathematically leads to:

$$c_{i1}(x,z) = 0 \tag{7}$$

Substituting Eqs. (2) and (7), the following expression thus obtained is:

$$\varphi_i\left(x,\pm\frac{w}{2},z\right)=c_{i0}(x,z)+c_{i2}(x,z)\frac{w^2}{4}=\varphi_{spi}(x) \tag{8}$$

Hence,

$$c_{i2}(x,z)=\frac{4}{w^2}\left[\varphi_{spi}(x)-c_{i0}(x,z)\right] \tag{9}$$

The boundary conditions [12] required to evaluate the coefficients in Eq. (3) are enumerated as follows:

In Region 1

$$k_{11}(x)=\left.\frac{d\varphi_1}{dz}\right|_{y=0,z=0}=\frac{\varepsilon_{ox_1}}{\varepsilon_{Si}t_{g_{eff}}}\left[\varphi_{sp1}(x)-{V_{gs1}}'\right] \tag{10}$$

$$\left.\frac{d\varphi_1}{dz}\right|_{y=0,z=t_{ch}}=\frac{\varepsilon_b}{\varepsilon_{Si}t_b}\left[{V_{gs1}}''-\varphi_{sb1}(x)\right] \tag{11}$$

Here, $\varepsilon_{ox_1}=\varepsilon_b$

Eq. (11) leads to the expression of $k_{12}(x)$as:

$$k_{12}(x)=\frac{{V_{gs1}}''-\varphi_{sp1}(x)\left(1+\frac{C_{eff}}{C_{Si}}+\frac{C_{eff}}{C_b}\right)+{V_{gs1}}'\left(\frac{C_{eff}}{C_{Si}}+\frac{C_{eff}}{C_b}\right)}{{t_{ch}}^2\left(1+\frac{2C_{Si}}{C_b}\right)} \tag{12}$$

In Region 2

$$k_{21}(x)=\left.\frac{d\varphi_1}{dz}\right|_{y=0,z=0}=\frac{\varepsilon_{ox_1}}{\varepsilon_{Si}t_{eff}}\left[\varphi_{sp2}(x)-{V_{gs2}}'\right] \tag{13}$$

$$\left.\frac{d\varphi_2}{dz}\right|_{y=0,z=t_{ch}}=\frac{\varepsilon_b}{\varepsilon_{Si}t_b}\left[{V_{gs2}}'-\varphi_{sb2}(x)\right] \tag{14}$$

Similarly, Eq. (14) leads to:

$$k_{22}(x)=\frac{\left[{V_{gs2}}'-\varphi_{sp2}(x)\right]\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_b}\right]}{{t_{ch}}^2\left(1+\frac{2C_{Si}}{C_b}\right)} \tag{15}$$

Here, ${V_{gs1}}'=V_{gs}-{V_{FBf_1}}'$, ${V_{FBf_1}}'=V_{FB_1}-\frac{qN_f}{C_{eff}}$, the front channel-oxide flat-band voltage in Region 1 is $V_{FB_1}=\phi_{M_S}-\phi_{Si}$, N_f is the density of charged biomolecule, C_{eff} is the effective oxide capacitance comprising the nanogap dielectric and the interfacial SiO_2 (ε_{ox_1})layer,

$$C_{eff}=\frac{\varepsilon_{ox_1}}{t_{g_{eff}}},t_{g_{eff}}=t_1+t_{bio}\frac{\varepsilon_{ox_1}}{\varepsilon_{bio}},C_b=\frac{\varepsilon_b}{t_b}$$
$$\varepsilon_{ox_1}=\varepsilon_b,C_{ox}=\frac{\varepsilon_{ox_1}}{t_{eff}},t_{eff}=t_1+t_2\frac{\varepsilon_{ox_1}}{\varepsilon_{TiO_2}}$$
$${V_{gs1}}''=V_{gs}-V_{FBb_1},V_{FBb_1}=V_{FB_1}$$
$${V_{gs2}}'=V_{gs}-V_{FB_2},V_{FB_2}=\phi_{M_D}-\phi_{Si}$$

Using the expressions of coefficients of Eq.(3), the total potential thus obtained is:

In Region 1

$$\varphi_1(x,y,z)=A_1\varphi_{sp1}(x)+B_1{V_{gs1}}'+C_1{V_{gs1}}'' \tag{16}$$

Here, $A_1=1+K_1z-K_2z^2-K_3zy^2+K_4z^2y^2$, $B_1=-K_5z+K_6z^2+K_7zy^2-K_8z^2y^2$, $C_1=\frac{z^2}{K}-\frac{4}{w^2}\frac{z^2}{K}y^2$

Expressions of the coefficients in A_1, B_1, C_1, A_2 and B_2 are listed in the Appendix.

In Region 2.

Total potential in Region 2 is

$$\varphi_2(x,y,z)=A_2\varphi_{sp1}(x)+B_2{V_{gs2}}' \tag{17}$$

Here, $A_2=1+{K_1}'z-{K_2}'z^2-{K_3}'zy^2+{K_4}'z^2y^2$, $B_2=-{K_5}'z+{K_6}'z^2+{K_7}'zy^2-{K_8}'z^2y^2$

The differential equations obtained by substituting Eq. (16) in Eqs.(1) and (17) in Eq.(1) are given by:

In Region 1

$$\frac{d^2\varphi_{sp_1}(x)}{dx^2}-\gamma_1\varphi_{sp_1}(x)=\theta_1 \tag{18}$$

Here,

$$\gamma_1=\frac{2K_2+2K_3z-2K_4z^2-2K_4y^2}{A_1},$$

$$\theta_1=\frac{qN_{ch}}{A_1}$$
$$\varepsilon_{Si}+\frac{{V_{gs1}}'\left(-2K_6-2K_7z+2K_8z^2+2K_8y^2\right)}{A_1}+\frac{{V_{gs1}}''}{A_1}\left(\frac{8z^2}{w^2}+\frac{8y^2}{w^2}-2\right),$$

In Region 2

$$\frac{d^2\varphi_{sp_2}(x)}{dx^2}-\gamma_2\varphi_{sp_2}(x)=\theta_2 \tag{19}$$

Here,

$\gamma_2 = \frac{2K_2{}' + 2K_3{}' z - 2K_4{}' z^2 - 2K_4{}' y^2}{A_2}, \theta_2 = \frac{qN_{ch}}{A_2}$

$\varepsilon_{Si} + \frac{V_{gs2}{}'\left(-2K_6{}' - 2K_7{}' z + 2K_8{}' z^2 + 2K_8{}' y^2\right)}{A_2}$.

Solution to Eqs. (18) and (19) are given respectively as:

In Region 1

$$\varphi_{sp_1}(x) = P_I e^{\delta_1 x} + Q_I e^{-\delta_1 x} - \omega_1 \tag{20}$$

Here, $\delta_1 = \sqrt{\gamma_1}$, $\omega_1 = \frac{\theta_1}{\gamma_1}$.

In Region 2

$$\varphi_{sp_2}(x) = P_{II} e^{\delta_2 (x - L_1)} + Q_{II} e^{-\delta_2 (x - L_1)} - \omega_2 \tag{21}$$

Here, $\delta_2 = \sqrt{\gamma_2}$, $\omega_2 = \frac{\theta_2}{\gamma_2}$.

The coefficients P_I,Q_I, P_{II} and Q_{II} are deduced using the following listed boundary conditions [13]:

Continuity of surface potential at the interface of two materials leads to:

$$\varphi_{sp_1}(x)\Big|_{x=L_1} = \varphi_{sp_2}(x)\Big|_{x=L_1} \tag{22}$$

Therefore,

$$\frac{d\varphi_{sp_1}(x)}{dx}\Big|_{x=L_1} = \frac{d\varphi_{sp_2}(x)}{dx}\Big|_{x=L_1} \tag{23}$$

Potential at source-channel end:

$$\varphi_{sp1}(0) = V_{Bi} \tag{24}$$

Potential at drain-channel end:

$$\varphi_{sp2}(L) = V_{Bi} + V_{ds} \tag{25}$$

$V_{Bi}$is the built-in potential.

Hence,

$$Q_{II} = \frac{bP_I e^{\delta_1 L_1} + aQ_I e^{-\delta_1 L_1} - \omega_{12}}{2},$$

$$P_{II} = \frac{aP_I e^{\delta_1 L_1} + bQ_I e^{-\delta_1 L_1} - \omega_{12}}{2},$$

$$Q_I = \frac{(V_{Bi} + \omega_1)(ae^c + be^d) - 2(V_{Bi} + V_{ds} + \omega_2) - 2\omega_{12}\cosh\delta_2 L_2}{2(a\sinh c + b\sinh d)},$$

$$P_I = V_{Bi} + \omega_1 - Q_I$$

Here, $a = 1 + \delta_{12}$, $b = 1 - \delta_{12}$,$c = \delta_1 L_1 + \delta_2 L_2$, $d = \delta_1 L_1 - \delta_2 L_2$.

3.1 Threshold Voltage Modeling

Threshold voltage can be obtained by equating the minimum surface potential to twice the Fermi potential [14]. Since surface potential minimum for all cases (except for the case with $N_f = 0$, $K = 1$) occurs in region 1, hence the position of minimum potential can be obtained as:

$$\frac{\partial\phi_{sp_1}(x)}{\partial x}\Big|_{x=x_{MIN}} = 0 \tag{26a}$$

The position of minimum surface potential thus obtained is:

$$x_{MIN} = \frac{1}{2\delta_1}\ln\frac{Q_I}{P_I} \tag{27a}$$

Hence threshold voltage can be obtained from

$$\varphi_{sp_1}(x_{MIN}) = 2\varphi_F \tag{28a}$$

For the case $N_f = 0$, $K = 1$, surface potential minimum for proposed biosensor is formed in region 2. Hence position of minimum is obtained as

$$\frac{\partial\phi_{sp_2}(x)}{\partial x}\Big|_{x=x_{MIN}} = 0 \tag{26b}$$

The position of minimum thus obtained is

$$x_{MIN} = \frac{1}{2\delta_2}\ln\frac{Q_{II}}{P_{II}} + L_1 \tag{27b}$$

Hence threshold voltage can be obtained from

$$\varphi_{sp_2}(x_{MIN}) = 2\varphi_F \tag{28b}$$

3.2 Short Channel Effect Modeling

DIBL [15] is denoted as:

$$DIBL = V_{thr,lin} - V_{thr,sat}, \tag{29}$$

Here $V_{thr,\ lin}$ and $V_{thr,\ sat}$ are the threshold voltages in linear and saturation regions respectively.

Subthreshold swing [16] is denoted as:

$$SS = 2.3V_t\left[\frac{d\varphi_{sp}(x)}{dV_{gs}}\Big|_{x=x_{MIN}}\right]^{-1} \tag{30}$$

Lateral Electric field is denoted as:

$$E_x = -\frac{d\varphi_{sp}(x)}{dx} \tag{31}$$

3.3 Sensitivity Analysis

Sensitivity is measured as follows:

For neutral biomolecules:

$$S_{N_{Bio}} = \left| \frac{V_{thr}\,(K=1) - V_{thr}\,(K>1)}{V_{thr}(K=1)} \right| \tag{32}$$

For charged biomolecules:

$$S_{C_{Bio}} = \left| \frac{V_{thr}(Bio_{neutral}) - V_{thr}\left(Bio_{charged}\right)}{V_{thr}(Bio_{neutral})} \right| \tag{33}$$

4 Results and Discussions

Validation of mathematical results have been conducted using simulation results from Atlas, Silvaco Fig. 2 portrays the consequence of variation of neutral biomolecules on the surface potential distribution of the proposed biosensor. The surface potential distribution is found to vary in region 1 under the nanogap containing the biomolecule whereas the surface potential in region 2 has remained unaffected due to the fixed TiO_2-SiO_2 gate stack architecture. It is clearly evident that when the nanogap is filled with air, the surface potential minimum attains the highest value (only in this case, minimum gets shifted towards drain and occurs in region 2). When the biomolecules are present in the nanogap, the dielectric value changes (K > 1), the surface potential minimum gradually decreases resulting in increased source-channel barrier height which in turn increases the threshold voltage thereby providing a metric to discern the type of neutral biomolecule present in the nanogap. As the K-value decreases, the effective oxide thickness under gate M_S increases, this leads to a decreased gate control over the channel. Hence, source-channel barrier height decreases with decreasing K leading to decreased threshold voltage and increased SCE. On the other hand, as K-value increases, the effective oxide thickness in region 1 decreases that allows better gate control over the channel in region 1. This leads to increased source-channel barrier height thereby increasing threshold voltage and effectively reducing the SCEs. Figure 3 and 3b are interpretations of the graphical analysis representing the effect of negatively, positively and neutral biomolecule on the surface potential distribution of the suggested biosensor for K = 2.1 and K = 5 respectively. In Fig. 3, for charged biomolecules with K = 2.1, the surface potential value is much higher for a particular value of charge compared to that for K = 5. For K = 2.1, effective oxide thickness under gate M_S is much higher leading to diminished gate control over the channel under region 1. This paves the way for diminished source-channel barrier height, increased surface potential value and augmented SCEs. In Fig. 3b, charged biomolecule for K = 5 in the nanogap leads to reduced effective oxide thickness and enhanced gate control over channel in region 1 thereby resulting in increased source-channel barrier height and improved threshold voltage characteristics. Also, in both the cases, presence of positive biomolecules (1-5x$10^{15}$$m^{-2}$) modulates the surface potential by shifting the surface potential minimum upwards (with increase in positive charge) compared to that of the neutral biomolecule thereby modulating the threshold voltage originating from a change in

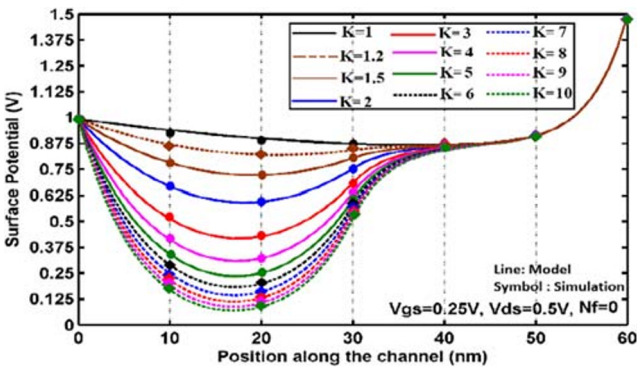


Fig. 2 Effect of variation of neutral biomolecules on the Surface potential distribution of proposed biosensor

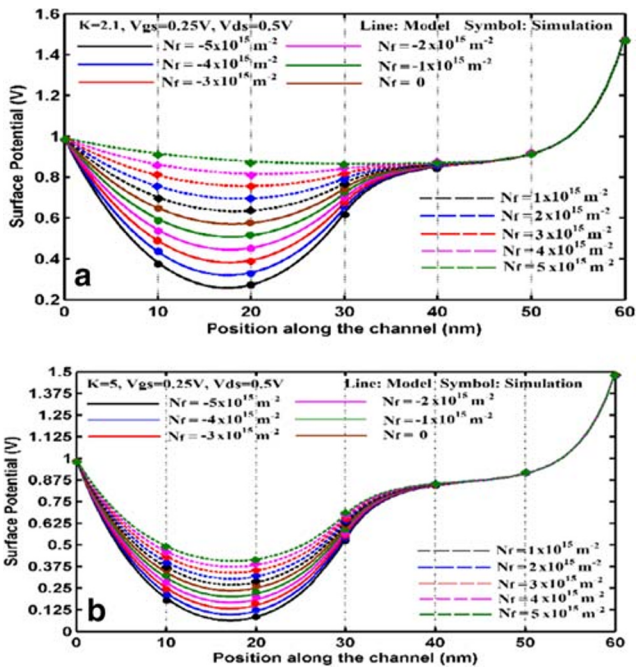


Fig. 3 **a** Effect of variation of charged biomolecules (K = 2.1) on the Surface potential distribution of proposed biosensor. **b** Effect of variation of charged biomolecules (K = 5) on the Surface potential distribution of proposed biosensor. Elucidation of the effect of Gate work function engineering (GWFE) on the surface potential distribution of proposed biosensor and its SM config. in presence of charged/ neutral biomolecule in the nanogap is depicted in Fig. 4**a**, **b** With careful selection of work function of gate materials in the DM architecture, a source-shifted surface potential minimum and a unique step profile towards the drain can be obtained for a chosen range of biomolecule. These features contribute to mitigate SCEs leading to almost accurate biomolecule detection coupled with improved device performances.

the flat-band voltage. Again, presence of negatively charged biomolecules (−1 to -5x10^{15}m^{-2}) causes a downward shift of surface potential minimum (with increase in negative charge) thereby increasing the source-channel barrier height and modulating the threshold voltage of the device contributing to revealing of charged biomolecule type present in the nanogap/cavity.

In the graphical plot of Fig. 4, charged/neutral biomolecule with K = 5 causes the formation of source-shifted surface potential minimum thereby contributing to lessened DIBL. Step profile in GWFE architecture causes reduced HCE. However, SM counterpart suffers from the drawbacks of weakened SCE immunization due to lack of such step profile and a source-shifted minimum. In fact, it is quite hard to predict the position of occurrence of surface potential minimum in case of SM structures. For example, in Fig. 4 for SM structure, for positively charged molecule with K = 5, surface potential minimum occurs in region 2 and such a case is not desired at all since it leads to high DIBL. For neutral biomolecule (K = 5), surface potential minimum occurs in the middle of the channel that leads to aggravated SCEs. For negatively charged molecule (K = 5), the minimum is found to occur in region 1. Same result can be found in Fig. 4 for charged/neutral biomolecule with K = 2.1. Since, the gate work functions in proposed biosensor have been selected carefully, hence, it can be assured that in case of proposed biosensor, the surface potential minimum can be made to get confined in region 1 towards the source to ensure weakened SCEs and almost accurate detection unlike biosensors without GWFE (SM architectures). Figure 5 portrays the graphical analysis of Surface potential distribution along the channel length position for three different ratio of L_{gap}:L_2 for neutral/charged biomolecule in the nanogap. For L_{gap}:L_2 = 2:1, the source-channel barrier height increases whereas surface potential minimum shifts more towards drain, the step profile is also less prominent. A drain-shifted minimum and a less prominent step profile can cause more DIBL. For ratio 1:1, step profile becomes more prominent, minimum gets shifted towards source, source-channel barrier height is preferable. However, for ratio 1:2, though step profile is prominent and minimum is source-shifted but the source-channel barrier height is very much decreased that leads to much increased leakages causing performance degradation. Though the selection of ratio value allows selection of a preferable threshold voltage, however, tuning to an allowable DIBL limit is necessary to minimize performance degradation. The impact of height variation up to which the biomolecules fill the nanogap/cavity is demonstrated in Fig. 6. The nanogap has a fixed height of 11 nm. Threshold voltage is found to decrease when the nanogap is fully filled with neutral biomolecules whereas, when the nanogap is filled up to 9 nm out of 11 nm, with neutral biomolecules, the threshold voltage increases. This nature of threshold voltage continues for both L = 60 nm and 100 nm with only exception that threshold voltage largely increases for L = 100 nm.

Impact of varying nanogap length on the threshold voltage of neutral biomolecules is portrayed in Fig. 7. Increase in nanogap length, that is, for a ratio L_{gap}:L_2 = 2:1, threshold voltage is maximum for both the cases of L = 60 nm and L = 100 nm. The increased source-channel height for

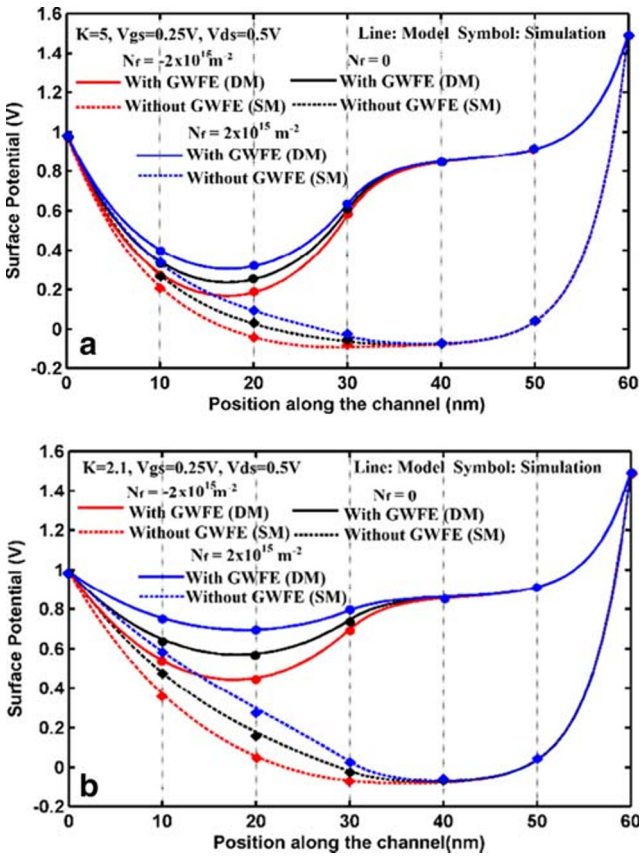


Fig. 4 **a** Effect of variation of charged/neutral biomolecules (K = 5) on the Surface potential distribution of proposed biosensor and its SM conFig. 4b Effect of variation of charged/neutral biomolecules (K = 2.1) on the Surface potential distribution of proposed biosensor and its SM config

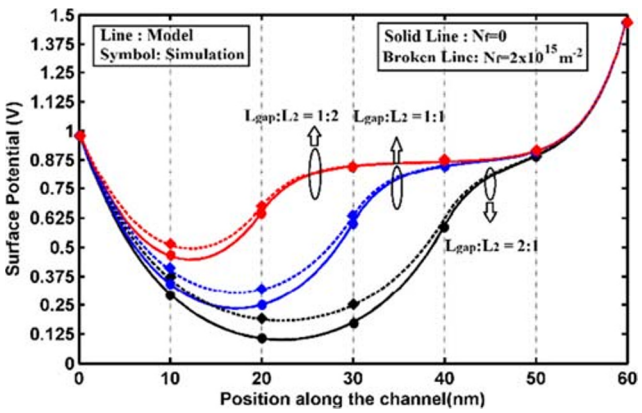


Fig. 5 Effect of variation of L_{gap}:L_2 ratio on the Surface potential distribution of proposed biosensor for neutral/charged biomolecule in the nanogap

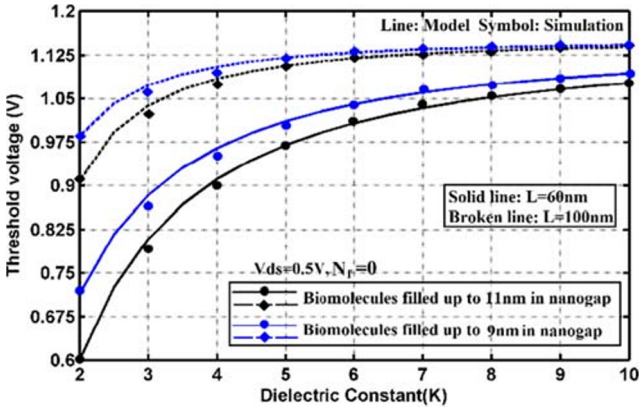


Fig. 6 Effect of height variation of neutral biomolecules on the threshold voltage of the proposed biosensor

L_{gap}:L_2 = 2:1 as portrayed in Fig. 5 leads to an increased threshold voltage and a reduced threshold voltage roll-off. With L_{gap}:L_2 = 1:2, threshold voltage roll-off gets worse and threshold voltage decreases leading to elevated leakages and degrading performance. Also, threshold voltage (both for L = 60 nm and L = 100 nm) increases for neutral biomolecules with higher dielectric constant as evident from increased source-channel barrier height with increased K of neutral biomolecules in Fig. 2. Threshold voltage greatly increases for L = 100 nm compared to L = 60 nm.

With Fig. 7b, the influence of nanogap/cavity length variation containing charged biomolecules on the threshold voltage of the proposed biosensor is illustrated. For L_{gap}:L_2 = 2:1, threshold voltage is highest for both L = 60 nm and L = 100 nm respectively owing to increased source-channel barrier height, whereas threshold voltage decreases for L_{gap}:L_2 = 1:1 and 1:2 respectively. Hence, increase in nanogap length results in corresponding increase in threshold voltage. Moreover, threshold voltage largely increases when L = 100 nm compared to that at L = 60 nm. Also, as per Fig. 3, since the source-channel barrier height increases for more negatively charged biomolecules, threshold voltage peaks for more negatively charged biomolecules and gradually decreases for more positively charged biomolecules. Figure 8 offers the graphical insight into the analysis for threshold voltage variation for charged biomolecules with K = 2.1 and K = 5 respectively. For charged biomolecules with K = 2.1, the effective oxide thickness in region 1 increases. Hence, gate control over the channel in region 1 diminishes. This causes the SCEs such as threshold voltage roll-off to get intensified. Whereas, for charged biomolecules with K = 5, the gate control over the channel in region 1 intensifies resulting in mitigated SCEs like threshold voltage roll-off. Therefore, the variation of threshold voltage with charged biomolecules for K = 5 is much lower compared to the case with K = 2.1. Change of threshold voltage of charged biomolecule (eg: $N_f = -1x10^{15}m^{-2}$, $N_f = 1x10^{15}m^{-2}$) compared to the neutral biomolecule ($N_f = 0$) is much larger for K = 2.1 compared to the case for K = 5. This is reflected in the Sensitivity graph for neutral biomolecules, the sensitivity for charged biomolecule with lower K will be much higher compared to the case for higher K. Evidences of reduced SCEs such as DIBL for the proposed biosensor is clearly illustrated in Fig. 9. For W =

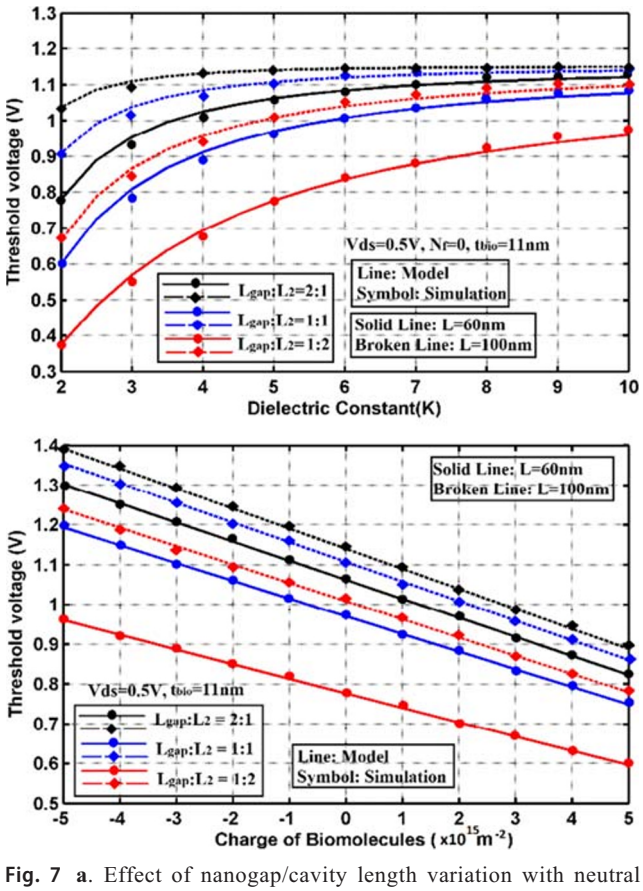


Fig. 7 **a**. Effect of nanogap/cavity length variation with neutral biomolecules on the threshold voltage of the proposed biosensor. **b** Variation of threshold voltage vs. charge of biomolecules (K = 5) for three different L_{gap}:L_2 ratio values for the proposed biosensor

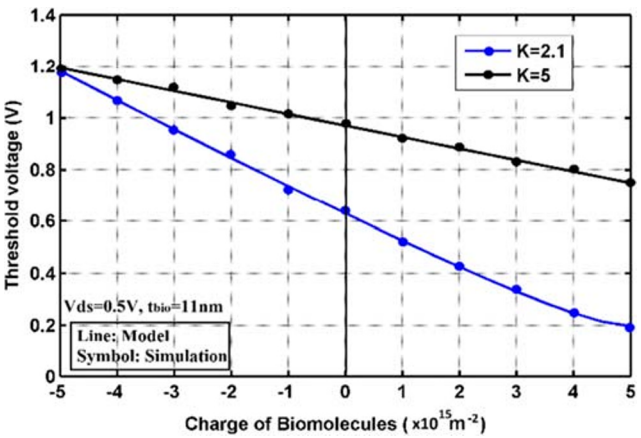


Fig. 8 Variation of threshold voltage vs. charge of biomolecules for K = 2.1 and K = 5 respectively for the proposed biosensor

5 nm, the proposed biosensor offers much lesser DIBL compared to its SM counterpart. This is accredited to the fact that a source-shifted surface potential minimum with a unique step profile allows improved shielding effect to DIBL. These attributes being absent in the SM config., the latter structure (having same width) immensely suffers from DIBL. With W = 7 nm, DIBL is found to greatly enhance in the proposed biosensor owing to reduced gate dominance over the channel thereby leading to strengthened SCEs. Since, with the increase in width, the lateral gates become far apart, hence precise gate control over the channel diminishes initiating elevated DIBL. Justification for selection of the TiO_2-SiO_2 gate-stack under Gate M_D is substantiated through the outcomes obtained in Fig. 10. With w = 5 nm and K_2 = 40 (TiO_2), SS is minimum compared to all other gate-stack configurations with lower K_2 values. Thus careful selection of gate-stack config. Can effectively reduce the SS thereby ensuring lower off-state leakages and diminished power consumption. However, for same gate-stack config. Under Gate M_D, SS increases for w = 7 nm due to reduced gate dominance over the channel. Hence optimization of gate width keeping fabrication compatibility is necessary for enhanced device performances. For neutral biomolecules, the sensitivity for the proposed biosensor is plotted as a function of the dielectric constant of the neutral biomolecules for two different channel lengths in Fig. 11. Sensitivity enhances with increment in dielectric constant of the neutral biomolecules. As per Eq. (32) for Sensitivity calculation of neutral biomolecule, the source-channel barrier height is lowest for air (K = 1) and hence threshold voltage [as per Fig. 3]. With gradual increase in K value, the source-channel barrier height increases leading to increasing threshold voltage. This explains the physics behind the increase in sensitivity of neutral biomolecule as per Eq. (32). Also, for higher channel lengths, the sensitivity parameter radically increases compared to that at L = 60 nm. Figure 11b depicts the Sensitivity analysis of charged biomolecules for K = 5 and K = 2.1 respectively. As per Fig. 7, variation of threshold voltage of

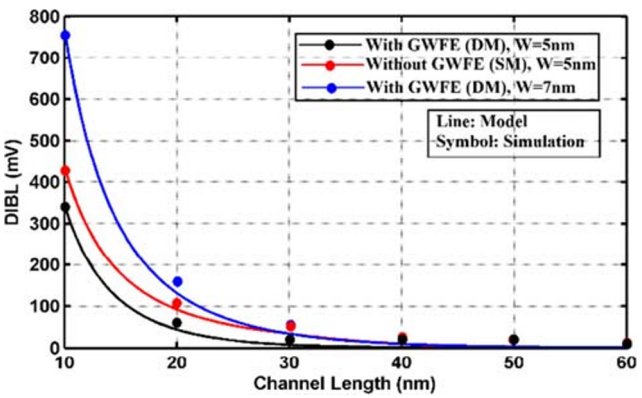


Fig. 9 DIBL variation vs. channel length for proposed biosensor with varying widths and for its SM config. With W = 5 nm

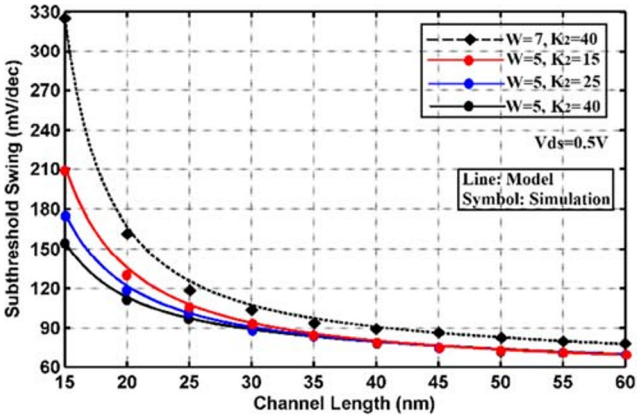


Fig. 10 SS variation vs. channel length for proposed biosensor with varying widths and for different gate-stack config. Under Gate M_D

charged biomolecule with respect to the neutral biomolecule is much higher for K = 2.1 (i.e lower K values). This greater variation leads to a rise in sensitivity. For higher K values, shift of threshold voltage of charged biomolecule with respect to the neutral biomolecule is comparatively lower, hence the sensitivity is lower for charged biomolecules with high K. For charged biomolecule with lower K, the proposed biosensor is

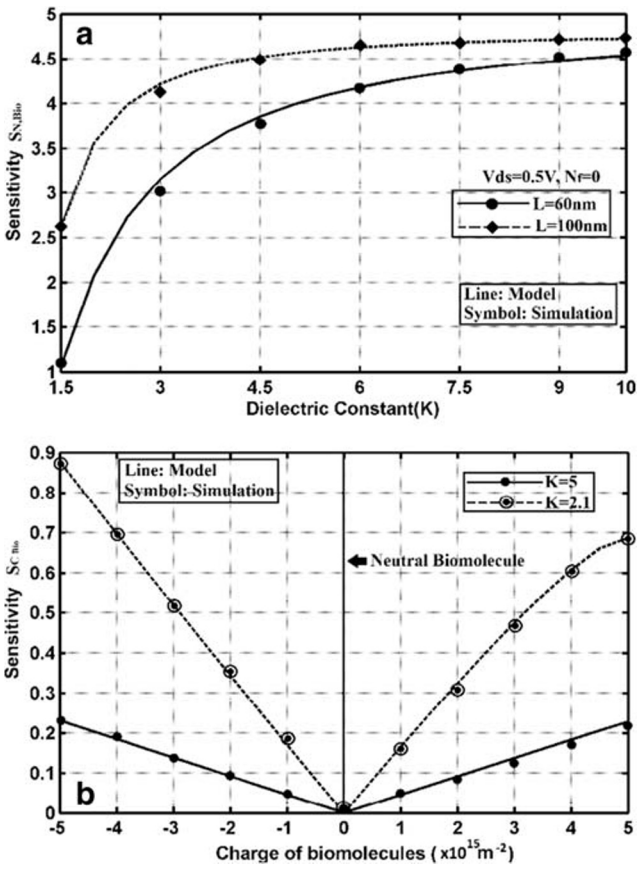


Fig. 11 **a**. Sensitivity vs. dielectric constant for neutral biomolecules of the proposed biosensor. **b** Sensitivity vs. charge of biomolecules (K = 5 and 2.1) of the proposed biosensor

more sensitive to negatively charged biomolecule compared to the positively charged biomolecule. Figure 12, b and c depict the electric field distribution along the channel position for the proposed biosensor comprising of the neutral, negatively charged and positively charged biomolecules respectively. In all the cases, it is quite observable that the proposed biosensor offers reduced electric field at the drain end compared to its SM counterpart. The unique step profile towards the drain end in DM structures lead to weakened HCE. Hence, it can be inferred that the recommended biosensor is largely immune to HCE that consequences in reduced power dissipation in the device. Atlas results match well with the mathematical results thereby authenticating our anticipated device.

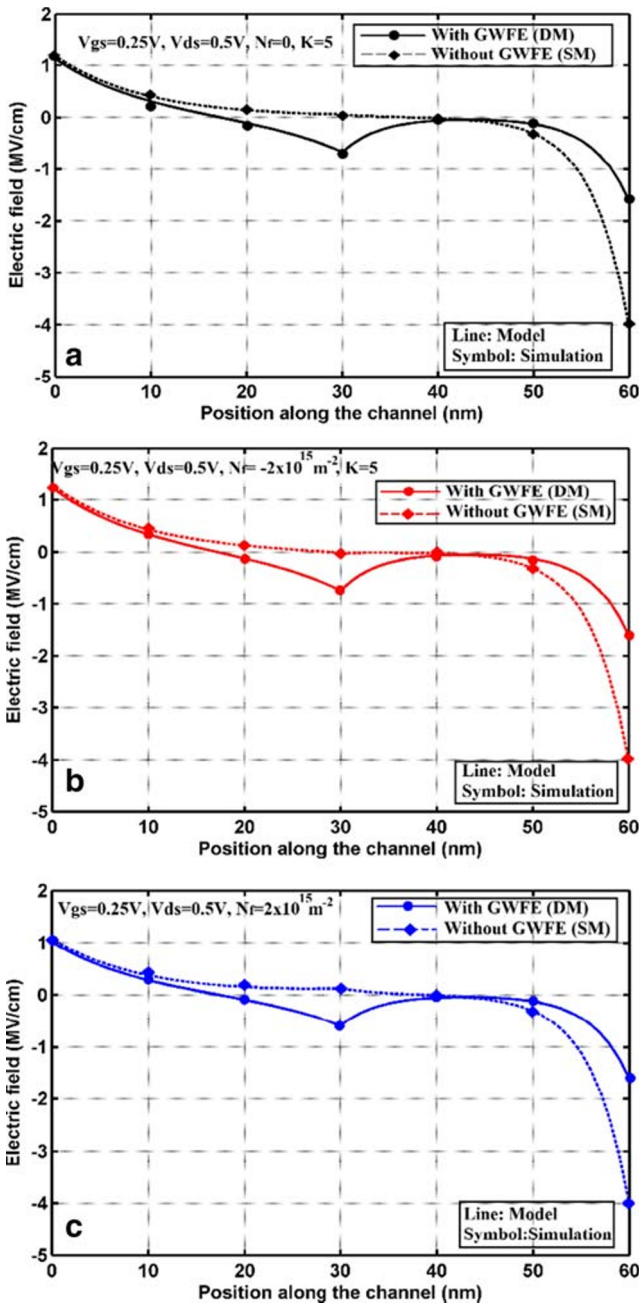


Fig. 12 **a**. Electric Field vs. position along the channel of the proposed biosensor with neutral biomolecule, **b** Electric Field vs. position along the channel of the proposed biosensor with negatively charged biomolecule (K = 5). **c** Electric Field vs. position along the channel of the proposed biosensor with positively charged biomolecule (K = 5)

5 Conclusion

Effective detection of neutral and charged biomolecules using a Dielectric-Modulated DM Trigate MOSFET with a DM bottom gate has been presented in the current research. Shifts in threshold voltage due to source-channel barrier height modulation as a consequence of flat-band voltage changes offer a metric providing potential detection of the biomolecule type. Moreover, the GWFE architecture provides efficient shielding to SCEs like DIBL, SS, HCE thereby offering upgraded device performances. Further, Sensitivity is found to increase for neutral biomolecules with higher k values while for charged biomolecules with low K, sensitivity for negative charges is quite high. These evidences contribute to strengthen the fact that the proposed biosensor is a worthwhile detector offering superior performances and propitious applications for future VLSI generations.

Acknowledgments Pritha Banerjee as the Principal Investigator thankfully acknowledges the financial support obtained from Department of Science and Technology (DST), Ministry of Science and Technology, Government of India to carry out this research work under Women Scientist scheme (WOS-A) vide File No. SR/WOS-A/PM-82/2018.

Appendix

$$K = t_{ch}^2\left(1+\frac{2C_{Si}}{C_b}\right), K, K_1 = \frac{\varepsilon_{ox_1}}{\varepsilon_{Si} t_{g_{eff}}}$$

$$K_2 = \frac{1+\frac{C_{eff}}{C_{Si}}+\frac{C_{eff}}{C_b}}{K}, K_3 = \frac{4}{w^2}K_1$$

$$K_4 = \frac{4}{w^2}K_2,\ K_5 = K_1, K_6 = \frac{\frac{C_{eff}}{C_{Si}}+\frac{C_{eff}}{C_b}}{K}$$

$$K_7 = \frac{4}{w^2}K_1,\ K_8 = \frac{4}{w^2}K_6, K_1^{'} = \frac{\varepsilon_{ox_1}}{\varepsilon_{Si} t_{eff}}$$

$$K_2^{'} = \frac{1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_b}}{K}, K_3^{'} = \frac{4}{w^2}K_1^{'}$$

$$K_4^{'} = \frac{4}{w^2}K_2^{'}, K_5^{'} = K_1^{'}, K_6^{'} = K_2^{'}$$

$$K_7^{'} = \frac{4}{w^2}K_1^{'}, K_8^{'} = \frac{4}{w^2}K_6^{'}$$

References

1. F. D'Agostino and D. Quercia, "Short-channel effects in MOSFETs," In: Proc. Introduction VLSI Design (EECS 467), Dec. 2000, pp. 1–15
2. Mahmud MA, Subrina S (2017) Analytical model of subthreshold swing of a gate and channel engineered double gate MOSFET. Int J Numer Model 30:e2235. https://doi.org/10.1002/jnm.2235
3. Sanjay PB, Vohra A (2020) Metal gate electrode, channel and gate oxide engineering to improve DC and analog/RF performance of double-gate MOSFET for high-speed applications. Appl. Phys. A 126:400. https://doi.org/10.1007/s00339-020-03576-5
4. Gupta N, Chaujar R (2016) Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. Appl Phys A Mater Sci Process 122:717. https://doi.org/10.1007/s00339-016-0239-9
5. Md. Arafat Mahmud and Samia Subrina, "two-dimensional analytical model of threshold voltage and drain current of a double-halo gate-stacked triple-material double-gate MOSFET", J Comput Electron, June 2016, Volume 15, Issue 2, pp. 525–536
6. Cartwright J (2011) Intel enters the third dimension. Nature. https://doi.org/10.1038/news.2011.274 http://www.nature.com/news/2011/110506/full/news.2011.274.html
7. Das R, Chanda M, Sarkar CK (2018) Analytical modeling of charge plasma-based optimized nanogap embedded surrounding gate MOSFET for label-free biosensing. IEEE Trans Electron Devices 65(12)
8. Kiran Kumar R, Shiyamala S (2019) A 2-D analytical modeling of dual work function metal gate MOSFET using high-K gate dielectric with enhanced RF/analog performance for low power applications. Silicon 12:2065–2072. https://doi.org/10.1007/s12633-019-00290-7
9. Padmanaban B, Ramesh R, Nirmal D, Sathiyamoorthy S (2015) Numerical modeling of triple material gate stack gate all-around (TMGSGAA) MOSFET considering quantum mechanical effects. Superlattice Microst 82:40–54
10. Vadthiya N, Tripathi S, Naik RBS (2018) A two-dimensional (2D) analytical modeling and improved Short Channel performance of Graded-Channel gate-stack (GCGS) dual-material double-gate (DMDG) MOSFET. Silicon 10:2399–2407. https://doi.org/10.1007/s12633-017-9683-1
11. H. Ghanatian and S. E. Hosseini, "Analytical modeling of subthreshold swing in undoped trigate SOI MOSFETs," J. Comput. Electron., vol. 15, no. 2, pp. 508–515, Apr. 2016 no. 3, pp. 966–973, Mar. 2016
12. Goel E, Singh B, Kumar S (2017) K Singh and S Jit, "analytical threshold voltage modeling of ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs". Indian J Phys 91(4): 383–390
13. Te-Kuang CHIANG, Mei-Li CHEN (2007) A new two-dimensional analytical model for Short-Channel symmetrical dual-material double-gate metal–oxide–semiconductor field effect transistors. Jpn J Appl Phys 46(6A):3283–3290
14. Gao H-W, Wang Y-H, Chiang T-K (2017) A Quasi-3-D scaling length model for trapezoidal FinFET and its application to subthreshold behavior analysis. IEEE Trans Nanotechn 16(2)
15. Zhang L, Lin L, He J, Chan M (2011) Modeling short-channel effect of elliptical gate-all-around MOSFET by effective radius. IEEE Electron Device Lett 32(9)
16. Chiang TK (2009) A new compact subthreshold behavior model for dual-material surrounding gate (DMSG) MOSFETs. Solid State Electron 53:490–496

Microelectronics Journal 120 (2022) 105354

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Threshold voltage modeling of Gaussian-doped Dual work function Material Cylindrical Gate-all-around (CGAA) MOSFET considering the effect of temperature and fixed interface trapped charges

Pritha Banerjee *, Jayoti Das

Department of Physics, Jadavpur University, India

ARTICLE INFO

Keywords:
Gaussian-doped MOSFET
Projected range
Straggle
Interface trapped charges
Cylindrical Gate-all-around (CGAA) MOSFET
Gate work function engineering (GWFE)
Short channel effects (SCEs)

ABSTRACT

Current research endeavor encompasses comprehensive threshold voltage analysis of a Gaussian-doped Dual work function Material (DM) Cylindrical Gate-all-around (CGAA) MOSFET with temperature variance in presence of fixed interface trap charges. Threshold voltage reliability over a wide range of temperature in presence of trap charges and its Gaussian-parameters such as projected range and straggle based dependencies are exhibited. Short channel response of the device has also been considered. Analytical results are corroborated through simulation outputs from Atlas.

1. Introduction

Incessant evolution in CMOS technology development can be assured with pioneered, scaled devices enabling improved speed, reduced power consumption, high packaging density etc. However, attenuated short channel effects are to be assured concurrently so as to obtain ameliorated device performances. In this context, the avant-garde technology of Cylindrical Gate MOSFETs have always gained prominence owing to their eminent capability of mitigating SCEs due to boosted gate control [1,2]. Other than elevated resistance to SCEs, these devices assure exalted packaging density and strong field confinement [3]. The implementation of another trailblazing technology of GWFE [4] in Cylindrical MOSFETs can further upgrade the device performance by modulating channel-source, channel-drain barrier heights thereby further improving the threshold voltage characteristics along with weakening of SCEs like Drain-induced barrier lowering (DIBL), Hot carrier effect (HCE) etc.

Several researches have been reported on this preferred structure [5,6]. However, the extent of reliability of the device depends largely on the interface quality of Si–SiO_2 which tends to get damaged due to high electric fields, radiation induced damages, fabrication related process parameters and many more [7,8]. These lead to the accumulation of interface trap charges that modulate the flat-band voltages leading to significant changes of the device characteristics [9,10]. This implies the significance of trap charge induced device performance exploration in advanced MOSFET devices.

Realization of the physical phenomena behind the operation of a device is extremely essential. Mathematical analysis and its corresponding corroboration with simulation outcomes offers better comprehensibility, higher level of accuracy encompassing proper insights to these physical phenomena. Hence, established researches exhibit analytical modeling followed by proper simulation of advanced devices with mathematical attributes of the innovative technologies incorporated in those devices. In this context, an intensified focus has been noticed on devising the mathematics of the Gaussian-distributed concentration in the channel region of planar devices such as GWFE Double-gate MOSFETs [11]. It is important to mention here that most researches are based on devices having a uniform channel doping. While, in most practical MOSFETs, the channel doping is Gaussian-type [12] and hence this necessitates to study the Gaussian-doped devices where electrical features of the device vary largely due to the Gaussian distribution parameters. In addition to this, a suitable selection of the Gaussian parameters allow to tune the electrical attributes of the device thereby enabling significant suppression of SCEs.

Cylindrical Gate-all-around structures have always been a prime topic of device selection considering its upgraded device performances as discussed earlier. Extensive analytical and simulative investigation on GWFE CGAA MOSFETs exist in literature [13]. Sahoo Et al [14].

* Corresponding author.
E-mail addresses: prithaedu7@gmail.com (P. Banerjee), jayoti.das@gmail.com (J. Das).

https://doi.org/10.1016/j.mejo.2021.105354
Received 6 May 2021; Received in revised form 28 December 2021; Accepted 28 December 2021
Available online 31 December 2021

reported the electrical characteristics of ideal Si–SiO_2 interface characterized CGAA MOSFET. Whereas, achieving an ideal Si–SiO_2 interface is very rare in fabrication. This necessitates the investigation of trap charge induced i.e damaged interface characterized device performance of CGAA devices and along with its corresponding comparison with the features of the undamaged device to understand the extent of device feature variations due to a damaged interface. Interface trap charge induced behavior of CGAA MOSFETs have been considered by Chiang Et al [15]. However, the research reports are based on the assumption that the channel is of uniform doping density. In real fabrication, the channel doping concentration follows a Gaussian-distribution and this necessitates to undertake the investigation to formulate the mathematics related to a Gaussian-doped channel of fixed trap charge induced GWFE CGAA MOSFET device. Moreover, realization of device performance over an extensive temperature range enables the perception of the thermal reliability of the device [16]. The fixed interface trap charges alter the device features under varying temperature conditions and hence, temperature-based analytical modelling offers an estimation of temperature sensitivity of the projected device so that the device can be optimized accordingly.

Therefore, for the first time, the mathematical formulation of temperature-based, fixed interface trap charge induced Gaussian-doped channel GWFE (Dual work function Material Gate) CGAA MOSFET has been projected in the current research endeavor. No such research that addresses the impact of change of Gaussian parameters such as Projected Range, straggle on the electrical features of a fixed interface trap charge induced GWFE CGAA MOSFET in a temperature varying environment is available in literature (to the best of our knowledge).

This research aims to present the much awaited mathematical devising of a Gaussian-doped DM CGAA MOSFET with incorporated GWFE in presence of the trap charges and also takes into account its thermal characterization to understand its performance reliability over an eclectic range of temperature 100 K–500 K. A parallel in-depth investigation of device features, comprehensive short channel effect immunity study are also provided and validated using simulation outcomes.

Results exhibit radical dependence of device characteristics on Gaussian parameters which, till date, has remained unknown in existing researches for the projected device. Analytical outputs are validated using Atlas outputs.

1.1. Device architecture

Fig. 1 presents a DM CGAA with a Gaussian-doped channel. The Gate material Ms (work function = 4.6eV) is towards the source and M_D (work function = 4.4eV) is towards the drain. The entire channel length is L with gate Ms length being L_1 and that of M_D being L_2, gate oxide is SiO_2 with thickness being t_{ox} (=2 nm).

Till date, only a simulative investigation on Single-Material Cylindrical Gate-all-around MOSFET exists in literature, the expression for Gaussian-doping distribution in the channel region is thus followed as per [17].

$$N_c(r) = \frac{Q}{\sigma_p\sqrt{2\pi}}\exp\left(\frac{-(r-R_p)^2}{2{\sigma_p}^2}\right) \tag{1}$$

Here, Q = implantation dose per unit area with a Projected Range R_p and straggle σ_p.

Fixed interface trapped charges are denoted as N_f and these are present along the interface of Si–SiO_2.

2. Analytical modeling

2.1. Central potential modeling

The temperature dependent parameters are followed using [18].

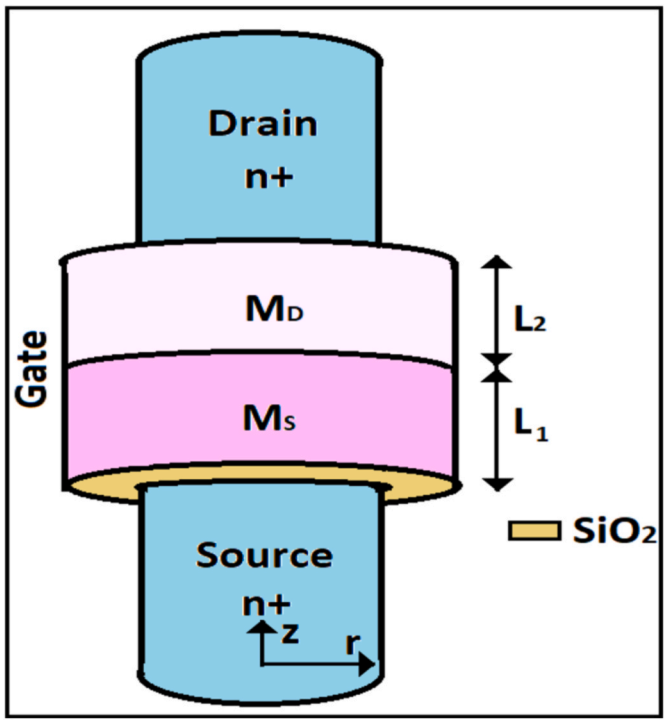


Fig. 1. Schematic 3-D representation of the device under consideration.

Finding an expression of central potential in the two regions defined by boundaries $0 \le z \le L_1, 0 \le r \le R$ (Region 1) and $L_1 \le z \le L, 0 \le r \le R$ (Region 2) respectively necessitates the solution of 2-D Poisson's equation given by [19].

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial(\varphi_j(r,z))}{\partial r}\right)+\frac{\partial^2\varphi_j(r,z)}{\partial z^2}=\frac{qN_c(r)}{\varepsilon_{Si}(T)} \tag{2}$$

where j = 1, 2 for regions 1 and 2 respectively.

$$\varepsilon_{Si}(T) = \left(11.4+\left(1+\left(1.2\times10^{-4}\right)T\right)\right)\varepsilon_0 \tag{3}$$

Following Young's Parabolic Potential Approximation [20], we have

$$\varphi_j(r,z) = C_{0j}(z) + C_{1j}(z)r + C_{2j}(z)r^2 \tag{4}$$

Applying the following boundary conditions we have:

Radial symmetry of the considered structure leads to a zero electric field at the channel center:

$$\left.\frac{\partial\varphi_j(r,z)}{\partial r}\right|_{r=0} = C_{1j} = 0 \tag{5}$$

2.2. Surface potential at r = R is given as

$$\varphi_j(R,z) = \varphi_{sj}(z) \tag{6}$$

Center potential at r = 0 is given as:

$$\varphi_j(0,z) = C_{0j}(z) \tag{7}$$

Electric field is continuous at r = R i.e at Si–SiO_2 interface which mathematically leads to

$$\left.\frac{\partial\varphi_j}{\partial r}\right|_{r=R} = \frac{C_{ox}}{\varepsilon_{Si}(T)}\left[{V_{gs_j}}' - \varphi_{sj}(z)\right] \tag{8}$$

where $C_{ox} = \frac{\varepsilon_{ox}}{R\ln\left(1+\frac{t_{ox}}{R}\right)}$ as per [21], ${V_{gs_j}}' = V_{gs} - {V_{fbj}}'$,

$$V_{fbj}{}' = V_{fbj} - \frac{qN_f}{C_{ox}}, \tag{9}$$

N_f is the fixed interface trap charge density.

$$V_{fbj} = \varphi_{M_{S(j=1)/D(j=2)}} - \varphi_{si}(T)$$

$$\varphi_{si}(T) = \chi + \frac{E_g(T)}{2} + \varphi_{fsi}(T),\ \varphi_{fsi}(T) = \frac{KT}{q}\ln\left(\frac{N_c(r=R)}{n_i(T)}\right)$$

$$n_i\left(T\right) = \left(1.706\times10^{25}\right)\left(\frac{T}{300}\right)^{3/2}.\exp\left(\frac{-qE_g(T)}{2KT}\right)$$ Considering the above cited boundary conditions, the coefficient C_{2j} thus obtained is

$$C_{2j} = \frac{V_{gsj}{}' - C_{0j}(z)}{R^2\left(1+\frac{2\varepsilon_{Si}(T)}{RC_{ox}}\right)} \tag{10}$$

Using the expressions obtained in (5) and (9) in equation (4) and then using equation (2), the differential equation thus obtained is

$$\frac{d^2C_{0j}(z)}{dz^2} - \alpha C_{0j}(z) = \beta_j \tag{11}$$

where $\alpha = \frac{4}{R^2\left(1+\frac{2\varepsilon_{Si}(T)}{RCox}\right)}$,

$$\beta_j = \frac{qN_c(r=0)}{\varepsilon_{Si}(T)} - \alpha V_{gsj}{}'$$

Solution to equation (10) gives the expression of central potential in Region 1 and 2 respectively which are as follows [22]:

$$C_{01}(z) = A_1e^{\eta z} + B_1e^{-\eta z} - \sigma_1 \text{ In Region 1} \tag{12}$$

$$C_{02}(z) = A_2e^{\eta(z-L_1)} + B_2e^{-\eta(z-L_1)} - \sigma_2 \text{ In Region 2} \tag{13}$$

where, $\eta = \sqrt{\alpha}, \sigma_1 = \frac{\beta_1}{\alpha}, \sigma_2 = \frac{\beta_2}{\alpha}$

The coefficients A_1, B_1, A_2, B_2 can be obtained from the following boundary conditions:

Continuity of central potential at the interface of two different materials leads to Ref. [23]:

$$C_{01}(z)|_{z=L_1} = C_{02}(z)|_{z=L_1} \tag{14}$$

$$\left.\frac{dC_{01}(z)}{dz}\right|_{z=L_1} = \left.\frac{dC_{02}(z)}{dz}\right|_{z=L_1} \tag{15}$$

At the source end, Central potential leads to:

$$C_{01}(z=0) = V_{bi}(T) = \frac{KT}{q}\ln\left(\frac{N_c(r=0)N_d}{n_i{}^2(T)}\right) \tag{16}$$

At Drain end, Central potential leads to:

$$C_{02}(L) = V_{bi}(T) + V_{ds} \tag{17}$$

The expressions for the coefficients A_1, B_1, A_2, B_2 are listed in Appendix section.

2.3. Threshold voltage modeling

The value of gate voltage at which the minimum central potential is equal to twice the Fermi potential is called the threshold voltage [24].

Formulation of threshold voltage necessitates finding an expression for the position of minimum central potential, substituting that in the expression of central potential in region 1 and equating it to twice the Fermi potential. Since, metal with higher work function surrounds region 1 so the minimum central potential occurs in Region 1, hence,

$$\left.\frac{dC_{o1}}{dz}\right|_{z=z_{\min}} = 0 \tag{18}$$

This yields $z_{\min} = \frac{1}{2\eta}\ln\left(\frac{B_1}{A_1}\right)$ (19)

$$C_{01}(z_{\min}) = 2\varphi_{fsi}(r=0) \tag{20}$$

The expression of threshold voltage thus obtained is:

$$V_{thr} = \frac{-b \pm \sqrt{b^2-4ac}}{2a} \tag{21}$$

The expressions of a, b and c are listed in the Appendix Section.

Drain-induced barrier lowering (DIBL) in mV is given as [25]:

$$DIBL = V_{thr_{lin}} - V_{thr_{sat}} \tag{22}$$

Subthreshold Swing (SS) in mV/dec is evaluated using the following expression as [26]:

$$SS = 2.3\frac{KT}{q}\left[\frac{dC_{01_{\min}}}{dV_{gs}}\right]^{-1} \tag{23}$$

Lateral electric field is given as:

$$E_z = -\frac{dC_{oj}}{dz} \tag{24}$$

3. Results and discussions

This section involves of mathematical analyses and their corresponding validation using simulated data from Atlas.

Fig. 2 demonstrates the central potential distribution along different positions of the channel which has a vertical Gaussian-doping of implant dose Q = 10^{16}/m^2, Projected range of 2.5 nm and straggle parameter is 2 nm. Radius of the channel is 5 nm. The graphical representation shows data for a low temperature of T = 100 K and for a high temperature of T = 500 K. For both the cases, it can be discerned that with more positive trap charges, the source-channel barrier height decreases that in turn will decrease the threshold voltage of the device. While for negative trap

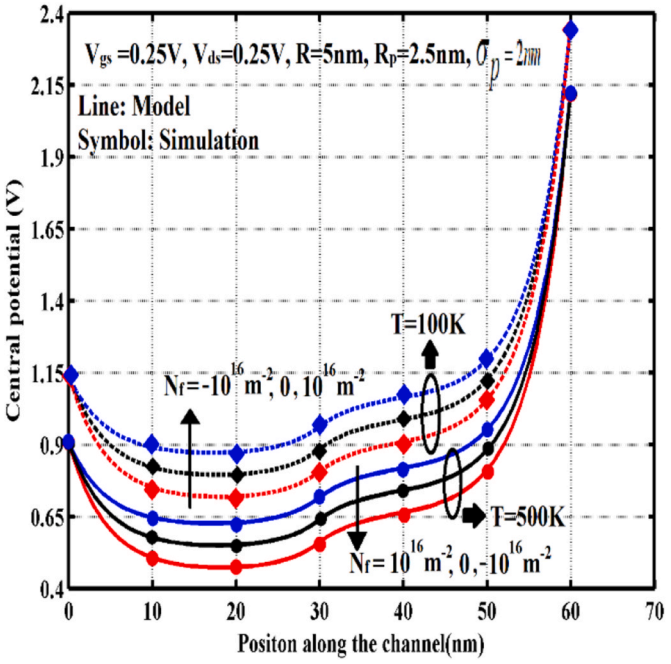


Fig. 2. Central potential along channel length for DM CGAA with implant dose Q = 10^{16}/m^2 with and without interface trapped charges for temperatures T = 500 K and T = 100 K

charges, the source-channel barrier height increases resulting in increased threshold voltage. For reduced temperatures, the central potential increases and for higher temperature, it decreases. However, the consequence of temperature on the device features can be more accurately predicted from the plot of threshold voltage at varying temperatures. Fig. 3 demonstrates the central potential distribution along different positions of the channel for both damaged and undamaged device for two different values of Projected range at R = 5 nm and straggle parameter of 2 nm. Central potential for undamaged and damaged device (with positive/negative trap charges) follows the same trend as reported in Fig. 2. However, in all the cases, when Rp = 0, that is, peak doping is located at the channel centre, source-channel barrier height in central potential increases that will lead to a greater threshold voltage, this justifies the increment of threshold voltage with increase in doping and decrease in Projected range value. When Rp = 5 nm, position of peak doping shifts away from the centre leading to decreased source-channel barrier height in central potential that will lead to a decreased threshold voltage, this justifies the decrease of threshold voltage with decrease in doping and increase of Projected range value. Fig. 4a demonstrates the effect of temperature on threshold voltage of damaged and undamaged device for two sets of Gaussian doping parameters and device radius. For R = 5 nm, Projected range = 2.5 nm and straggle parameter = 2 nm, threshold voltage for both damaged and undamaged device decreases with elevation in temperature. Now, for positive trap charges, the source-channel barrier height being lesser, threshold voltage is also lesser compared to the case for negative trap charges. An enhanced source-channel barrier height leads to an increased threshold voltage for negative trap charges in all the cases. For a radius R = 5 nm, the gate control being resilient, V_{thr} decrease with temperature for both damaged and undamaged device is much stable compared to the case of R = 10 nm. This is more comprehensible if the Roll-off (RO) of V_{thr} in terms of temperature for undamaged device is observed. For R = 10 nm, RO is higher implying more temperature dependent variability of V_{thr} compared to the same for R = 5 nm. This implies that temperature based V_{thr} reliability can be obtained more with smaller device radius due to increased gate control. It is to be noted that in both the cases of R = 5nm/10 nm, Gaussian configuration is so chosen that Projected range is half of the radius for ease of result comparison. Fig. 4b highlights the effect of a lower density of fixed interface trapped charges ($N_f = -5, 5, -1, 1 \times 10^{15} m^{-2}$) on the threshold voltage of the device at different

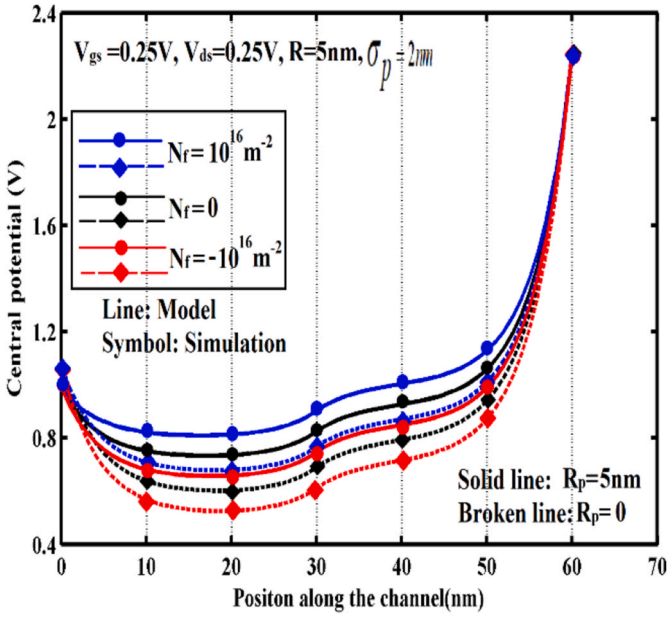


Fig. 3. Central potential along the channel length for both damaged and undamaged device for two different values of Projected range.

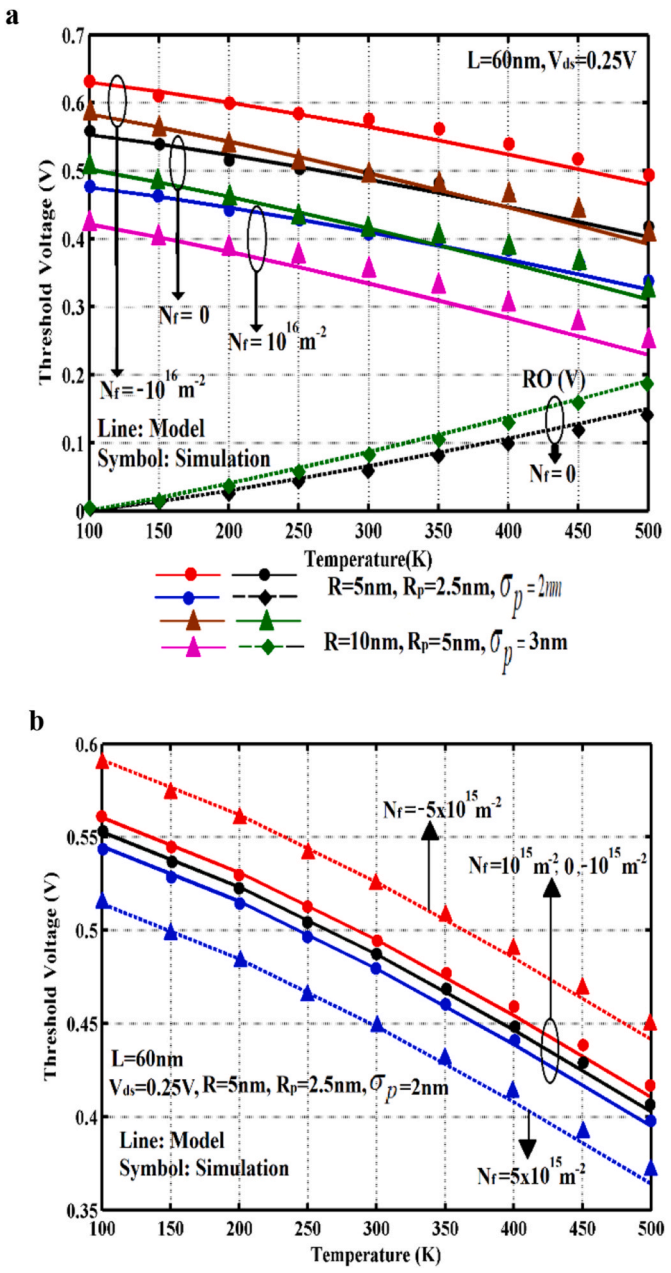


Fig. 4. a Threshold voltage and Roll-Off (Temperature) versus Temperature for two different sets of Gaussian parameters and device radius and for damaged and undamaged device b Threshold voltage versus Temperature for damaged (having lower density of fixed interface trapped charges) and undamaged device.

temperatures. The plot follows the same trend for temperature as observed in Fig. 4a. However, it can be clearly observed that, for a lower density of trapped charges such as $N_f = -1{,}1 \times 10^{15} m^{-2}$, the effect on the flat-band voltage of the device due to fixed trap charges is much lower, however, as the density of fixed interface trap charges increases from $N_f = -1{,}1 \times 10^{15} m^{-2}$ to $N_f = -5{,}5 \times 10^{15} m^{-2}$, the flat-band voltage gets significantly impacted and the higher the flat-band voltage modulation, the greater is the shift of threshold voltage of the damaged device compared to the ideal/undamaged device.

Effect of change in Gaussian parameters on threshold voltage for both damaged and undamaged device and for two sets of straggle parameters is displayed in Fig. 5. V_{thr} for positive, neutral and negative charges follow the same trend as depicted in Fig. 4a. Now, keeping R = 5 nm, V_{thr} is seen to decrease with increase in Projected Range value.

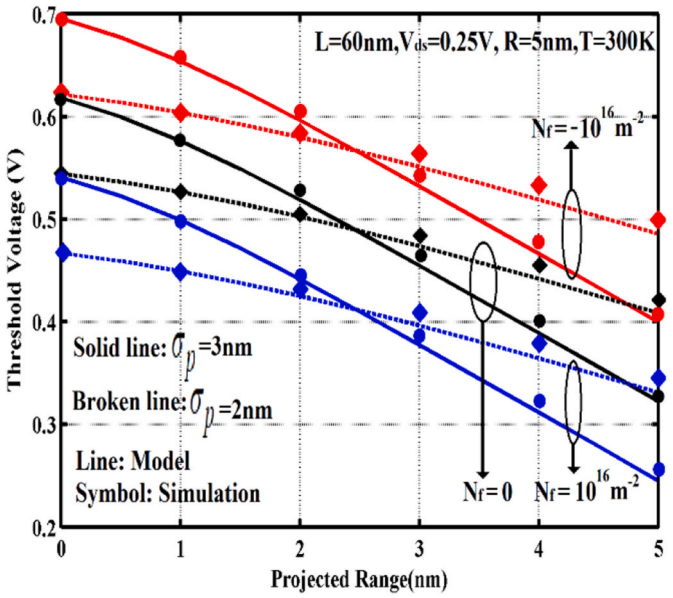


Fig. 5. Threshold voltage versus Projected Range for both damaged and undamaged device for two different straggle parameters.

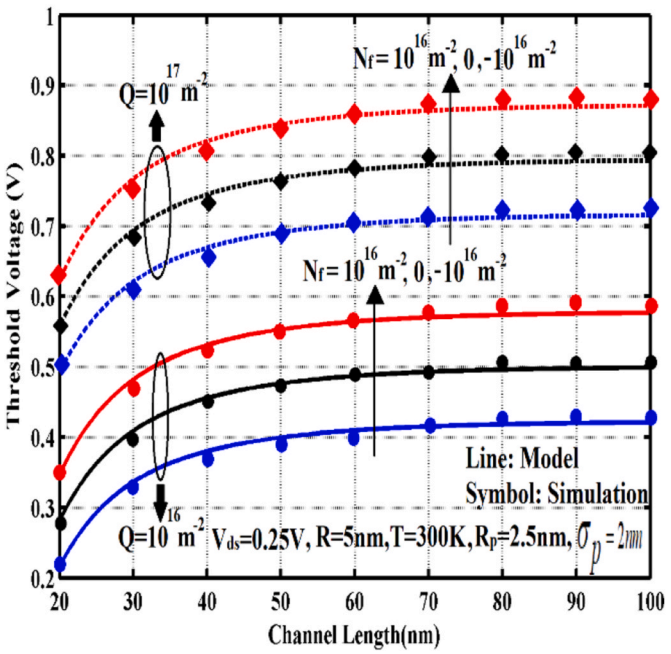


Fig. 6. Threshold voltage versus channel length for both damaged and undamaged device for two different values of implanted dose (Q).

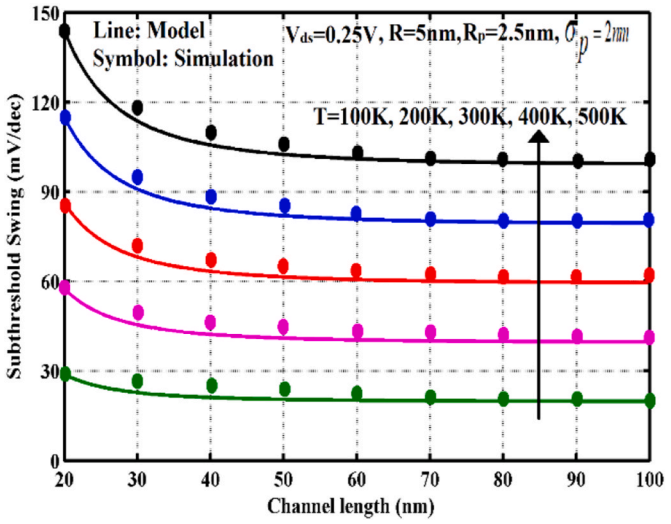


Fig. 7. SS versus channel length for vertical Gaussian doped DM CGAA at different temperatures.

Projected range in Gaussian-doping distribution defines the position of the peak doping in the channel.

When $R_p = 0$, this means the apex doping is positioned at the channel centre. Now, since threshold voltage upsurges with high doping, so at $R_p = 0$, the threshold voltage is maximum since source-channel barrier height in central potential is also maximum. Shifting of peak doping from centre leads to decreased source-channel barrier height in central potential thereby leading to a decreased threshold voltage. This justifies the plot in Fig. 5. Straggle parameter gives a measure of the profile spreading. As the straggle parameter increases, the profile becomes more widely spread and the rate of decrease of threshold voltage with Projected range (RO in terms of Projected range) is much decreased for $\sigma_p = 3nm$ compared to$\sigma_p = 2nm$.

Hence, proper selection of Gaussian parameters can effectively enhance performance consistency of the device thereby offering upgraded device performances. This is also exhibited and can be comprehended in the reported research by Goel et al. [27]. Fig. 6 exhibits the plot of threshold voltage versus channel length for both damaged and undamaged device for two different implant doses. For a higher implant dose, threshold voltage increases. This is also established in other researches as well [28]. Hence apposite choice of implant dose helps reliable tuning of threshold voltage to a preferred value. The variation of Substhreshold Swing (SS) for different channel length at different temperatures for undamaged device is plotted in Fig. 7. The plot clearly exhibits that SS highly increases with temperature. For higher channel lengths, SS is nearly 100mV/dec at T = 500 K whereas it is much reduced, about 20mV/dec for T = 100 K. However, for T = 300 K, SS is about 60mV/dec for channel lengths 40 nm or above. At reduced temperatures, the rate of impact ionization is minor compared to that at heightened temperatures and this leads to improved subthreshold characteristics that in turn improves SS of the device at lower temperatures. Graphical analysis of SS vs. channel length for two different radii value and at two different Projected range values is presented in Fig. 8. Increment of device radius from 5 nm to 7 nm largely increases the SS value for channel lengths below 30 nm. Increase in device radius causes the gate control over the channel to decrease resulting in higher SS. However, in both the cases, a shift of Projected range from Rp = 0 to Rp = 5 nm results in increase of SS. When Rp = 0, the peak doping is located at the channel centre. High doping at the centre, increases the source-channel barrier height in centre potential which leads to higher threshold voltage and lower subthreshold leakages thereby improving the device characteristics. A shift of peak doping from centre results in lower source-channel barrier height in central potential thereby leading to lower threshold voltages leading to increased subthreshold leakages.

A short investigation on the advantages of using a Dual work function Material Gate over the Single Material (SM) one is exhibited from Figs. 9 and 10(c).

Fig. 9 portrays a relative investigation of DIBL of the device under consideration and its Gaussian-doped SM counterpart. Step profile in the central potential distribution of DM device allows lower DIBL compared to the SM device where the latter is generally devoid of any step profile in its central potential distribution. Lateral Electric field distribution along channel position of both damaged and undamaged device and their SM damaged and undamaged counterparts is plotted in Fig. 10a- 10 (c). In all the cases, it can be seen, that the DM config. has a reduced

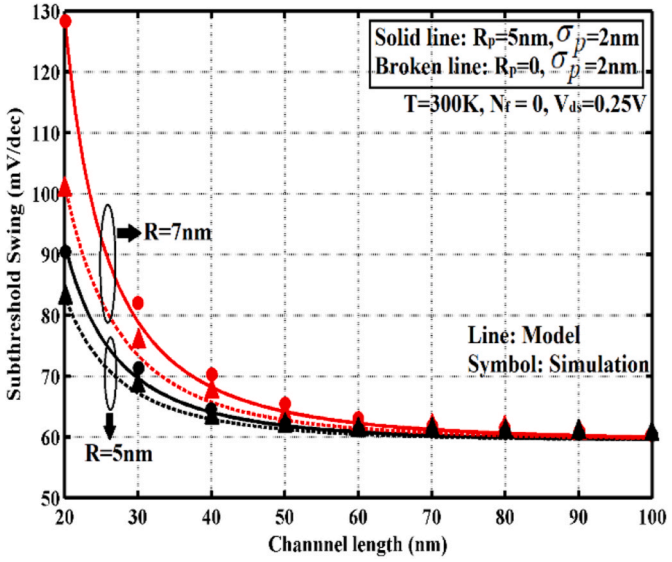


Fig. 8. SS versus channel length for two different Projected Ranges and two values of Device radius.

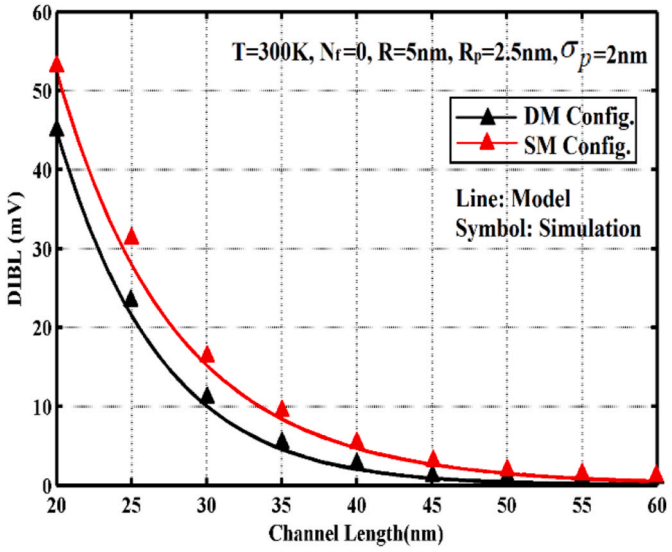


Fig. 9. DIBL versus channel length for vertical.

electric field at drain end and a peak at the interface of two dissimilar materials. Firstly, the step profile in the central potential distribution due to work function engineering leads to reduced slope of potential at drain end leading to reduced HCE in the device.

Secondly, work function engineering leads to a peak at the interface of two dissimilar materials giving the transport efficiency of the DM device a significant boost that upgrades the device characteristics. SM config. being devoid of gate work function engineering suffers from increased electric field at drain end leading to a heightened HCE in the device.

The analytical results are validated through simulation outputs from Atlas.

4. Conclusion

Mathematical emphasis on formulating the threshold voltage in a Gaussian-doping distribution channel of a Dual work function Material Cylindrical Gate-all-around MOSFET in a varying temperature

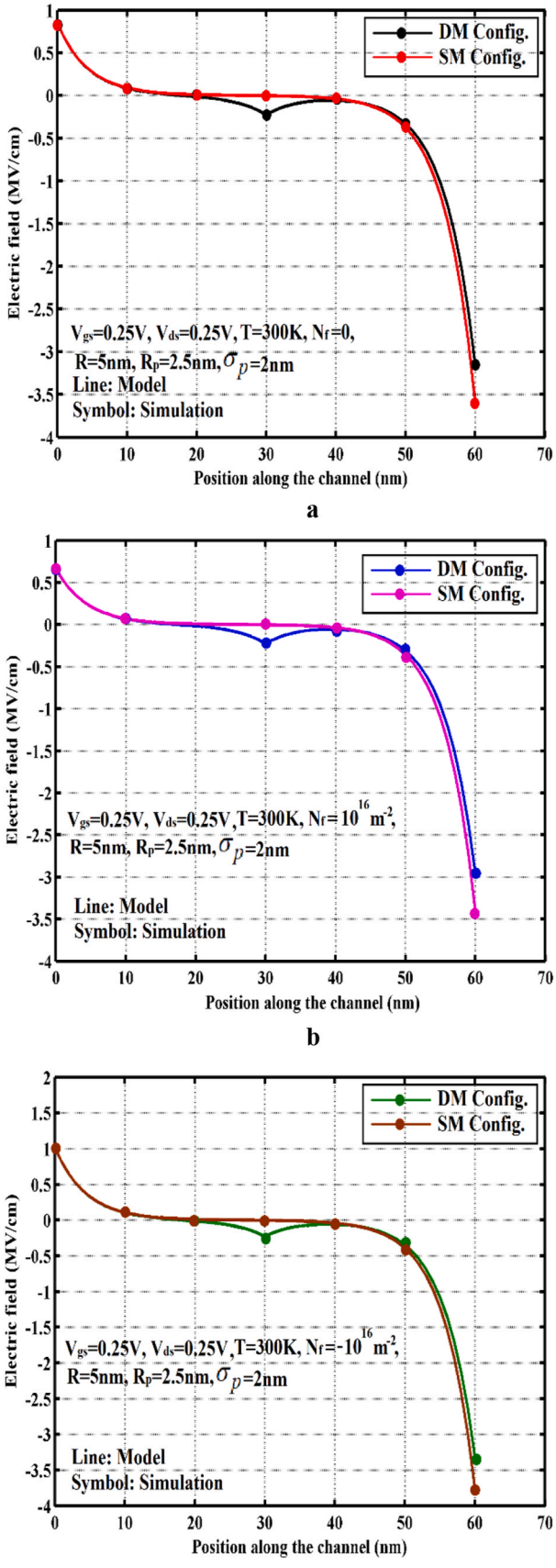


Fig. 10. Lateral Electric Field Distribution along channel position for DM and SM Device Config. for (a) undamaged, (b) positive trap charges and (c) negative trap charges.

environment and in presence/absence of fixed interface trap charges has been illustrated in the current research exertion. Significances of the effect of variation of Gaussian parameters, interface trap charges and temperature on the threshold voltage is clearly revealed in the present research. Gaussian parameter like Projected Range modulates the source-channel barrier heights of central potential thereby impacting the threshold voltage, whereas, proper selection of straggle parameter can effectively control the abrupt threshold voltage roll-off. Interface trap charges, whether positive or negative, inexorably modify the device flat-band voltage which leads to considerable changes in threshold voltage. Further, graphical exertions of device characteristics in a varying temperature environment provides comprehensive details of the temperature dependent device performance reliability. In addition, a brief short channel effect analysis has also been presented that investigates the DIBL, SS and HCE behavior of the Gaussian-doped device. Comparative exploration of features of the device and its Gaussian-doped SM counterpart exhibits the former's improved reliability over the latter. Simulation outputs from Atlas further validate the central-potential based mathematical model.

Declaration

Funding and Acknowledgement

Pritha Banerjee as the Principal Investigator and a DST Woman Scientist (A) thankfully acknowledges the financial support obtained from the Department of Science and Technology (DST), Government of India, to carry out this research work under Women Scientist scheme (WOS-A) vide reference no. SR/WOSA/PM-82/2018.

Author statement

Pritha Banerjee: Conceptualization, Methodology, Software, Writing – original draft preparation, Investigation Jayoti Das: Conceptualization, Supervision, Visualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix

Expressions related to Central potential Modeling section:

The expressions for the coefficients A_1, B_1, A_2, B_2 are listed below:

$$A_1 = \theta_1 + \gamma_1 V_{gs} \tag{i}$$

$$B_1 = \theta_2 + \gamma_2 V_{gs} \tag{ii}$$

$$A_2 = A_1 e^{\eta L_1} - (\sigma_1 - \sigma_2) \tag{iii}$$

$$B_2 = B_1 e^{-\eta L_1} - (\sigma_1 - \sigma_2) \tag{iv}$$

Here,

$$\theta_2 = \frac{V_{bi}(T) + \frac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)}(e^{\eta L} - 1) + V_{fb_1}{}' e^{\eta L} - V_{fb_2}{}' - (V_{bi}(T) + V_{ds}) - (\sigma_1 - \sigma_2)\cosh \eta L_2}{2 \sinh \eta L} \tag{v}$$

$$\gamma_2 = \frac{1 - e^{\eta L}}{2 \sinh \eta L} \tag{vi}$$

$$\theta_1 = V_{bi}(T) + \frac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)} + V_{fb_1}{}' - \theta_2 \tag{vii}$$

$$\gamma_1 = -1 - \gamma_2 \tag{viii}$$

Expressions related to Threshold Voltage Modeling section:

$$a = 4\gamma_1\gamma_2 - 1 \tag{ix}$$

$$b = 2\left[2(\theta_1\gamma_2 + \theta_2\gamma_1) + \left(2\varphi_{f_{Si}}(r=0) + \frac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)} + V_{fb_1}{}'\right)\right] \tag{x}$$

$$c = 4\theta_1\theta_2 - \left(2\varphi_{f_{Si}}(r=0) + \frac{qN_c(r=0)}{\alpha\varepsilon_{Si}(T)} + V_{fb_1}{}'\right)^2 \tag{xi}$$

References

[1] Daniele Quercia FabioD'Agostino, Introduction to VLSI design (EECS 467), Short-Channel Effects in MOSFETs", December 11th (2000) 1–15.

[2] Nitish Kumar, Vaibhav Purwar, Himanshi Awasthi, Rajeev Gupta, Kunal Singh, Sarvesh Dubey, Modeling the threshold voltage of core-and-outer gates of ultra-thin nanotube Junctionless-double gate-all-around (NJL-DGAA) MOSFETs, Microelectron. J. 113 (2021), 105104. ISSN 0026-2692.

[3] M.A. Abdi, F. Djeffal, Z. Dibi, D. Arar, A two dimensional analytical subthreshold behavior analysis including hot-carrier effect for nanoscale Gate Stack Gate All Around (GASGAA) MOSFETs, J. Comput. Electron. 10 (2011) 179–185.

[4] Lü Wei-Feng, Dai Liang, Impact of work-function variation on analog figures-of-merits for high-k/metal-gate junctionless FinFET and gate-all-around nanowire MOSFET, Microelectron. J. 84 (2019) 54–58. ISSN 0026-2692.

[5] K. Nayak, S. Agarwal, M. Bajaj, K.V.R.M. Murali, V.R. Rao, Random dopant fluctuation induced variability in undoped channel Si gate all around nanowire n-MOSFET, IEEE Trans. Electron. Dev. 62 (2) (Feb. 2015) 685–688, https://doi.org/10.1109/TED.2014.2383352.

[6] H. Nam, Y. Lee, J. Park, C. Shin, Study of work-function variation in high- k/metal-gate gate- all-around nanowire MOSFET, IEEE Trans. Electron. Dev. 63 (8) (Aug. 2016) 3338–3341, https://doi.org/10.1109/TED.2016.2574328.
[7] Zhi Chen, et al., On the mechanism for interface trap generation in MOS transistors due to channel hot carrier stressing, IEEE Electron. Device Lett. 21 (1) (Jan. 2000) 24–26, https://doi.org/10.1109/55.817441.
[8] C.D. Liang, et al., Defects and low-frequency noise in irradiated black phosphorus MOSFETs with HfO2 gate dielectrics, IEEE Trans. Nucl. Sci. 65 (6) (June 2018) 1227–1238, https://doi.org/10.1109/TNS.2018.2828080.
[9] Rajni Gautam, Manoj Saxena, R.S. Gupta, Mridula Gupta, Two dimensional analytical subthreshold model of nanoscale cylindrical surrounding gate MOSFET including impact of localised charges, J. Comput. Theor. Nanosci. 9 (4) (April 2012) 602–610.
[10] S.R. Suddapalli, B.R. Nistala, A center-potential-based threshold voltage model for a graded-channel dual-material double-gate strained-Si MOSFET with interface charges, J. Comput. Electron. 18 (2019) 1173–1181, https://doi.org/10.1007/s10825-019-01377-5.
[11] A. Dasgupta, S.K. Lahiri, A two-dimensional analytical model of threshold voltages of short-channel MOSFETs with Gaussian-doped channels, IEEE Trans. Electron. Dev. 35 (3) (March 1988) 390–392, https://doi.org/10.1109/16.2468.
[12] Sarvesh Dubey, Pramod Kumar Tiwari, S. Jit, A two-dimensional model for the subthreshold swing of short-channel double-gate metal–oxide–semiconductor field effect transistors with a vertical Gaussian-like doping profile, J. Appl. Phys. 109 (2011), 054508.
[13] M. Kessi, A. Benfdila, A. Lakhelef, L. Belhimer, M. Djouder, Investigation on body potential in cylindrical gate-all-around MOSFET, in: 2019 IEEE 31st International Conference on Microelectronics, MIEL), 2019, pp. 213–216, https://doi.org/10.1109/MIEL.2019.8889640.
[14] J. Sahoo, R. Mahapatra, Center potential based threshold voltage modelling of TM-CGAA MOSFET, in: 2016 International Conference on Microelectronics, Computing and Communications, MicroCom), 2016, pp. 1–6, https://doi.org/10.1109/MicroCom.2016.7522548.
[15] T. Chiang, A compact model for threshold voltage of surrounding-gate MOSFETs with localized interface trapped charges, IEEE Trans. Electron. Dev. 58 (2) (Feb. 2011) 567–571, https://doi.org/10.1109/TED.2010.2092777.
[16] A. Goel, S. Rewari, S. Verma, R.S. Gupta, Temperature-dependent gate-induced drain leakages assessment of dual-metal nanowire field-effect transistor—analytical model, in: IEEE Transactions on Electron Devices, vol. 66, May 2019, pp. 2437–2445, https://doi.org/10.1109/TED.2019.2898444, 5.
[17] Himangi Sood, Viranjay M. Srivastava, Ghanshyam Singh, Performance analysis of undoped and Gaussian doped cylindrical surrounding-gate MOSFET with it's small signal modeling, Microelectron. J. 57 (2016) 66–75.
[18] Rajni Gautam, Manoj Saxena, R.S. Gupta, Mridula Gupta, Temperature dependent subthreshold model of long channel GAA MOSFET including localized charges to study variations in its temperature sensitivity, Microelectron. Reliab. 54 (2014) 37–43.
[19] B. Yu, Y. Yuan, J. Song, Y. Taur, A two-dimensional analytical solution for short-channel effects in nanowire MOSFETs, IEEE Trans. Electron. Dev. 56 (10) (Oct. 2009) 2357–2362, https://doi.org/10.1109/TED.2009.2028048.
[20] N. Jaiswal, A. Kranti, Modeling short-channel effects in core–shell junctionless MOSFET, IEEE Trans. Electron. Dev. 66 (1) (Jan. 2019) 292–299, https://doi.org/10.1109/TED.2018.2881006.
[21] O. Prakash, S. Beniwal, S. Maheshwaram, A. Bulusu, N. Singh, S.K. Manhas, Compact NBTI reliability modeling in Si nanowire MOSFETs and effect in circuits, IEEE Trans. Device Mater. Reliab. 17 (2) (June 2017) 404–413, https://doi.org/10.1109/TDMR.2017.2694709.
[22] A. Chaudhry, M.J. Kumar, Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review, IEEE Trans. Device Mater. Reliab. 4 (1) (March 2004) 99–109, https://doi.org/10.1109/TDMR.2004.824359.
[23] S.R. Sriram, B. Bindu, Analytical model for RDF-induced threshold voltage fluctuations in double-gate MOSFET, IEEE Trans. Device Mater. Reliab. 19 (2) (June 2019) 370–377, https://doi.org/10.1109/TDMR.2019.2910197.
[24] S. Dubey, A. Santra, G. Saramekala, M. Kumar, P.K. Tiwari, An analytical threshold voltage model for triple-material cylindrical gate-all-around (TM-CGAA) MOSFETs, IEEE Trans. Nanotechnol. 12 (5) (Sept. 2013) 766–774, https://doi.org/10.1109/TNANO.2013.2273805.
[25] L. Zhang, L. Li, J. He, M. Chan, Modeling short-channel effect of elliptical gate-all-around MOSFET by effective radius, IEEE Electron. Device Lett. 32 (9) (Sept. 2011) 1188–1190, https://doi.org/10.1109/LED.2011.2159358.
[26] Hamdam Ghanatian, Seyed Ebrahim Hosseini, Analytical modeling of subthreshold swing in undoped trigate SOI MOSFETs, J. Comput. Electron. 15 (2016) 508–515.
[27] E. Goel, B. Singh, S. Kumar, K. Singh, S. Jit, Analytical threshold voltage modeling of ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs, Indian J Phys (April 91 (4) (2017) 383–390.
[28] Sarvesh Dubey, Pramod Kumar Tiwari, S. Jit, A two-dimensional model for the potential distribution and threshold voltage of short-channel double-gate metal-oxide-semiconductor field-effect transistors with a vertical Gaussian-like doping profile, J. Appl. Phys. 108 (2010), 034518, https://doi.org/10.1063/1.3460796.

Journal of Electronic Materials (2022) 51:1512–1523
https://doi.org/10.1007/s11664-021-09419-0

ORIGINAL RESEARCH ARTICLE

Gate Work Function-Engineered Graded-Channel Macaroni MOSFET: Exploration of Temperature and Localized Trapped Charge-Induced Effects with GIDL Analysis

Pritha Banerjee[1] · **Jayoti Das**[1]

Received: 22 August 2021 / Accepted: 23 December 2021 / Published online: 13 January 2022

Abstract
The current research paper presents the analytical modelling and simulation-based device characteristics of a dual-material (DM) gate-graded Channel (GC) macaroni metal-oxide-semiconductor field-effect transistor (MOSFET) in the presence/absence of localized interface trapped charges within a temperature range of 100–500 K. The device's inner potential and threshold voltage dependence on the inherent macaroni features, such as filler radius and outer radius, of the proposed macaroni MOSFET are exhibited through the current research. Detailed investigation exhibits that the dual-material gate allows suitable suppression of various short-channel effects such as drain-induced barrier lowering (DIBL), hot-carrier effect (HCE) and gate-induced drain leakage (GIDL) current. Graded channel technology has been incorporated to obtain suitable tuning of threshold voltage. Device features such as inner potential, threshold voltage and drain current (including GIDL) for a damaged (presence of localized trapped charges) and undamaged device have been presented to demonstrate the impact of localized trapped charges on device features. Comprehensive temperature-based research exploration exhibits significant thermal influence on the device performance and an estimation of device performance reliability over the 100–500 K temperature range has been provided in the investigation. Comparative research analysis of inner potential, threshold voltage, DIBL and subthreshold swing (SS) of the device with its graded-channel dual-material gate-all-around cylindrical counterpart clearly highlights the advantages offered by the proposed device over other contemporary devices. Analytical results have been verified from simulation outputs using Silvaco TCAD.

Keywords Macaroni metal-oxide-semiconductor field-effect transistor (MOSFET) · short-channel effects · cylindrical MOSFETs · gate-induced drain leakage (GIDL) · analytical modelling · gate work function-engineered (GWFE) MOSFET

Introduction

Unhindered progress followed by a technology renaissance is being witnessed in the current semiconductor era, and it has been a remarkable phenomenon that continues to offer advanced devices meeting the ever-expanding demands of technological requirements of the present-day consumer market. Device portability, increased power efficiency, minimized cost and faster operation are gradually gaining consumer attention, and this drives the inevitability to upgrade device configuration on a frequent basis. This has created noteworthy research avenues, which is evident from a technological literature survey demonstrating the step-by-step upgrade of metal-oxide-semiconductor field-effect transistors (MOSFETs) from conventional planar devices[1] to advanced cylindrical-gate MOSFET devices[2,3] through suitable device scaling. Cylindrical MOSFETs are popular for escalated gate control over the channel allowing better resistance to short-channel effects (SCEs), enabling strong field confinement, higher packaging density etc.[4] To date, existing literature highlights the impact of inherent device parameters of a conventional single-material gate (SMG) conventional macaroni-channel MOSFET on its performance and a comparative study of this device with its full-channel conventional SMG cylindrical counterpart, demonstrating that the macaroni configuration is superior to the cylindrical counterpart.[5] However, gate work function engineering

✉ Pritha Banerjee
prithaedu7@gmail.com

Jayoti Das
jayoti.das@gmail.com

[1] Department of Physics, Jadavpur University, Kolkata, India

(GWFE) has the intrinsic property of suppressing various SCEs, offering improved threshold voltage and drain current characteristics[6].

When device scaling in the nanometer regime is considered, most of the conventional MOSFETs are observed to suffer from major SCEs that result in degraded device performance. The single-material gate conventional macaroni MOSFET is also found to be affected by SCEs; however, the extent of device performance degradation in this MOSFET is much lower than its full-channel cylindrical counterpart. To further boost device performance of the conventional macaroni device and to support further device scaling, the conventional macaroni MOSFET has been radically modernized and equipped with technology such as gate work function engineering followed by channel grading in the current research for the first time. A dual-material gate has been incorporated to effectively suppress major SCEs such as drain-induced barrier lowering (DIBL), hot-carrier effect (HCE), and gate-induced drain leakage (GIDL). Through channel grading, tuning of threshold voltage has been achieved. In addition, response of the proposed device in the presence of localized interface trapped charges has been investigated in detail. The Si-SiO_2 interface is often damaged due to the fabrication process, radiation, HCE etc. This can result in the formation of interface traps causing localized positive/negative trapped charges[7]. These charges considerably modify the flat-band voltage initiating changes in device characteristics. This necessitates the performance investigation of our proposed device in both damaged and undamaged conditions to meticulously observe the extent of device performance reliability. Further, drain current analysis is presented considering gate-induced drain leakage (GIDL) effects[8]. GIDL is a primary leakage mechanism in short-channel MOSFETs. It contributes to significant power dissipation in short-channel devices. When the drain voltage is positive and gate voltage is near zero or negative, the region near the n+ drain is depleted. The depletion region is narrower due to heavy doping of the drain. This causes electric field lines to crowd near the drain causing electron tunneling into it. The holes, on the other hand, move into the channel creating a path for off-state GIDL current.

Finally, the performance of the proposed device has been explored over a wide temperature range of 100–500 K. Temperature is an important parameter which considerably affects device performance. Estimation of temperature sensitivity of both the damaged and undamaged device provides detailed insight for device optimization. To date, to the best of our knowledge, no such research highlighting the performance of a gate work function-engineered macaroni MOSFET with a graded channel exists that also considers the effect of localized interface trapped charges in a temperature-varying environment. However, this research aims to highlight the above stated scientific analyses using mathematical formulation and confirm through proper simulation results from Silvaco TCAD.

Device Architecture

The macaroni MOSFET is a cylindrical device with a hollow pillar along the channel center. Detailed 3-D and 2-D schematic representations of the device under consideration are presented in Fig. 1a–c. The gate consists of two materials, M_S (= 4.6 eV) towards the source and M_D (= 4.4 eV) towards the drain. The channel length is L = 60 nm. The outer radius is r_2 (= 15 nm) and inner radius is r_1(= 10nm).

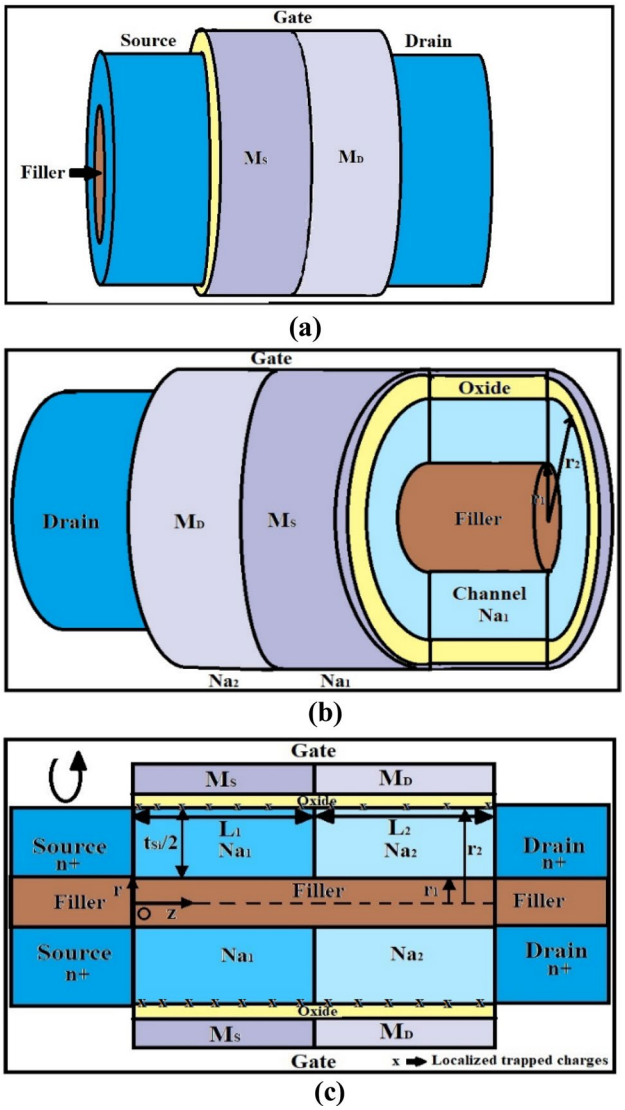


Fig. 1 (a) 3-D schematic representation of the device, (b) 3-D cross-sectional schematic representation of the device, (c) 2-D cross-sectional representation of the device.

The *p*-type channel has a graded concentration, with a higher doping concentration of $Na_1 = 10^{17}cm^{-3}$ towards the source and in the region under gate M_s and a lower doping concentration $Na_2 = 10^{16}\ cm^{-3}$ towards the drain and in region under gate M_D. The channel thickness is t_{Si} $(= 2(r_2 - r_1))$. The oxide thickness is t_{ox}(=2 nm).

Analytical Modelling

The temperature parameters used in this research are listed below[9]:

i) $E_g(T) = E_g(300) + E_{g\alpha}\left(\frac{300^2}{300+E_{g\beta}} - \frac{T^2}{T+E_{g\beta}}\right)$, where $E_g(300) = 1.08eV, E_{g\alpha} = 4.73 \times 10^{-4}eV/K, E_{g\beta} = 636K$

ii) $n_i(T) = (1.706 \times 10^{25}).\left(\frac{T}{300}\right)^{3/2}.\exp\left(\frac{-qE_g(T)}{2K_BT}\right)$

iii) $\varepsilon_{Si}(T) = \left(11.4 + \left(1 + \left(1.2 \times 10^{-4}\right)T\right)\right)\varepsilon_0$

In order to investigate the electrical features of the proposed device, the 2-D Poisson's equation must be solved. The channel potential $\Psi_i(r, \theta, z)$ does not vary along the radial plane. Hence, the 2-D Poisson's equation to be solved is as follows[10]:

$$\frac{\partial^2\Psi_i(r,z)}{\partial r^2} + \frac{1}{r}\frac{\partial\Psi_i(r,z)}{\partial r} + \frac{\partial^2\Psi_i(r,z)}{\partial z^2} = \frac{qNa_i}{\varepsilon_{Si}(T)} \tag{1}$$

where $i = 1, 2$ for regions 1, 2 defined by boundaries as follows:

Region 1 has boundaries $0 \le z \le L_1, r_1 \le r \le r_2$ and doping concentration of $Na_1 = 1$ x $10^{17}cm^{-3}$ and Region 2 has boundaries $L_1 \le z \le L, r_1 \le r \le r_2$ and doping concentration of $Na_2 = 1$ x $10^{16}cm^{-3}$. q is the electronic charge and $\varepsilon_{Si}(T)$ is the temperature-dependent channel permittivity. To solve Eq. 1, Young's parabolic potential approximation must be considered which is as follows :

$$\Psi_i(r,z) = C_{1i}(z) + C_{2i}(z)r + C_{3i}(z)r^2 \tag{2}$$

where $C_{1i}(z)$, $C_{2i}(z)$ and $C_{3i}(z)$ are z-dependent coefficients.

The boundary conditions used to solve Eq. 1 are as follows[11]:

I. $\left.\frac{\partial\Psi_i(r,z)}{\partial r}\right|_{r=r_1} = C_{2i}(z) + 2r_1C_{3i}(z) = 0$ which leads to

$$C_{2i}(z) = -2r_1C_{3i}(z) \tag{3}$$

II. $\left.\frac{\partial\Psi_i(r,z)}{\partial r}\right|_{r=r_2} = C_{2i}(z) + 2r_2C_{3i}(z) = \frac{C_{ox}}{\varepsilon_{Si}(T)}\left[V'_{gs_i} - \Psi_i(r_2,z)\right]$

where $C_{ox} = \frac{\varepsilon_{ox}}{r_2\ln\left(1+\frac{t_{ox}}{r_2}\right)}$, ε_{ox} is the oxide permittivity,

$$V'_{gsi} = V_{gs} - V'_{fb_i} \tag{3.i}$$

$$V'_{fb_i} = V_{fbi} - \frac{qN_f}{C_{ox}} \tag{3.ii}$$

where N_f is the interface localized charge density

$$V_{fbi} = \phi_{M_{S/D}}\left(= \phi_{M_{S_{\text{for Reg.1}}}} or \phi_{M_{D_{\text{for Reg.2}}}}\right) - \phi_{Si_i}(T) \tag{3.iii}$$

$$\phi_{Si_i}(T) = \chi + \frac{E_g(T)}{2} + \phi_{f_i}(T)$$

Boundary condition (II) leads to $C_{3i}(z) = \dfrac{4C_{ox}\left(V'_{gsi} - \psi_{0i}(z)\right)}{4\varepsilon_{Si}(T)t_{Si} + C_{ox}t_{Si}^2}$ (4)

Here $\psi_{0i}(z)$ is the inner potential at the channel/filler interface for the *i*th region.

Putting the expressions of Eqs. 3 and 4 in Eq. 2 and then using Eq. 1, the differential equation thus obtained is as follows:

$$\frac{\partial^2\psi_{0i}}{\partial z^2} + 2C_{3i}(z) = \frac{qNa_i}{\varepsilon_{Si}(T)} \tag{5}$$

General solution to the above differential equations in regions 1 and 2 are as follows:

$$\psi_{01}(z) = A\exp(z/\lambda) + B\exp(-z/\lambda) + \varphi_{01} \quad \text{in region 1} \tag{6}$$

$$\psi_{02}(z) = C\exp((z-L_1)/\lambda) + D\exp(-(z-L_1)/\lambda) + \varphi_{02} \quad \text{in region 2} \tag{7}$$

Here $\varphi_{0i} = V'_{gsi} - \frac{qNa_i\lambda^2}{\varepsilon_{Si}(T)}$, $\lambda = \sqrt{\frac{4\varepsilon_{Si}(T)t_{Si}+C_{ox}t_{Si}^2}{8C_{ox}}}$

To find the expressions of the coefficients A, B, C and D, the boundary conditions to be followed are listed as follows[12]:

III. At the source end, $\psi_{01}(z=0) = V_{bi_1}(T)$

IV. At the drain end, $\psi_{02}(z=L) = V_{bi_2}(T) + V_{ds}$

V. Continuity of potential at the interface of two dissimilar materials leads to $\psi_{01}(z)\big|_{z=L_1} = \psi_{02}(z)\big|_{z=L_1}$

VI. Continuity of electric flux at the interface of two dissimilar materials lead to $\left.\frac{\partial\psi_{01}(z)}{\partial z}\right|_{z=L_1} = \left.\frac{\partial\psi_{02}(z)}{\partial z}\right|_{z=L_1}$

The above stated boundary conditions lead to the following:

$$A = \alpha_1 + \beta_1V_{gs} \tag{8}$$

$$B = \alpha_2 + \beta_2V_{gs} \tag{9}$$

$$C = A\exp(L_1/\lambda) + \left(\frac{\varphi_{01} - \varphi_{02}}{2}\right) \tag{10}$$

$$D = B\exp(-L_1/\lambda) + \left(\frac{\varphi_{01} - \varphi_{02}}{2}\right) \tag{11}$$

Here,$\alpha_1, \beta_1, \alpha_2, \beta_2$ are listed in the Appendix section.

Threshold Voltage Modeling

Threshold voltage of the device can be obtained by equating the minimum inner potential to $2\phi_{f_1}(T) = 2\frac{KT}{q}\ln\left(\frac{Na_1}{n_i(T)}\right)$, that is,

$$\psi_{01\,\min} = 2\frac{KT}{q}\ln\left(\frac{Na_1}{n_i(T)}\right) \tag{12}$$

The expression of threshold voltage obtained from Eq. (10) is as follows:

$$V_{\text{th}} = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \tag{13}$$

Here expressions of a, b, c are listed in Appendix Section.

Short-Channel Response Study

DIBL (mV)[13] response of the device is obtained from the following equation:

$$\text{DIBL} = V_{\text{th}_{\text{linear}}} - V_{\text{th}_{\text{saturation}}} \tag{14}$$

Subthreshold swing[14] (mV/dec) is obtained using the following equation:

$$SS = \frac{KT}{q}\left[\frac{d\psi_{01\,\min}}{dV_{\text{gs}}}\right]^{-1} \tag{15}$$

In order to study the -carrier effect (HCE) response of the device, the electric field response of the device under consideration must be observed.

$$E_{iz} = -\frac{d\psi_{0i}(z)}{dz} \tag{16}$$

Drain Current Modelling

A unified drain current for the device for different regions of operation is as follows[15]:

$$I_{\text{ds}} = \begin{bmatrix} I_{\text{gidl}}, -0.3 \le V_{\text{gs}} \le 0 \\ I_{\text{sub}}, 0 \le V_{\text{gs}} \le V_{\text{th}} \\ I_{\text{lin}}, V_{\text{th}} \le V_{\text{gs}} \le V_{\text{sat}} \\ I_{\text{sat}}, V_{\text{sat}} \le V_{\text{gs}} \le 1.0 \end{bmatrix} \tag{17}$$

GIDL current is given by the following expression:

$$I_{\text{gidl}} = A'E_i^2\left(0.5t_{\text{Si}}, L_1 + L_2\right)\exp\left(\frac{-B'}{E_i\left(0.5t_{\text{Si}}, L_1 + L_2\right)}\right) \tag{18}$$

where A', B' are constants given in[15]

Subthreshold current is given as follows in the limit $0 \le V_{\text{gs}} \le V_{\text{th}}$

Electron current in the channel of the device under consideration is as follows[16]:

$$I_{\text{DS}}(z) = \int_{r_1}^{r_2} 2\pi RJ(r,z)dr \tag{19}$$

Here diffusion current density is given by

$$J(r,z) = \frac{\mu_n'}{1 + \theta\left(V_{\text{gs}} - V_{\text{THR}}\right)}qn_i(T)\exp\left(\frac{\psi_{01\,\min} - V}{V_T}\right)\frac{dV(z)}{dz} \tag{20}$$

Here $V_t = \frac{KT}{q}$

The rest is given in the Appendix section.

Linear drain current within the limit $V_{\text{th}} \le V_{\text{gs}} \le V_{\text{sat}}$ is given as follows:

$$I_{\text{lin}} = \frac{2\pi\left(r_2 - r_1\right)\mu_{\text{eff}}C_{\text{ox}}E_c}{\left(E_cL + V_{\text{ds}}\right)}\left[\left(V_{\text{gs}} - V_{\text{ths}}\right)^{\frac{\alpha}{2}}V_{\text{ds}} - \frac{\theta_{\text{short}}V_{\text{ds}}^2}{2}\right] \tag{21}$$

where E_c is the critical field, for the long-channel device $\alpha = 2$ to $\alpha = 1$ for the short-channel device, $\theta_{\text{short}} = \frac{0.1}{\left[\frac{d\psi_{01\,\min}}{dV_{\text{gs}}}\right]}$ at $V_{\text{gs}} = V_{\text{th}}, V_{\text{ths}} = V_{\text{th}}\left(1 - \theta_{\text{short}}\right)$, short-channel effects have been incorporated in the drain current by using E_c,θ_{short}, V_{ths}.

Saturation current within the limit $V_{\text{th}} \le V_{\text{gs}} \le V_{\text{sat}}$(with V_{ds} replaced by V_{dsat}) given as follows:

$$I_{\text{sat}} = \frac{2\pi\left(r_2 - r_1\right)\mu_{\text{eff}}C_{\text{ox}}}{\left(1 + \frac{V_{\text{dsat}}}{E_cL}\right)\left(L - L_{\text{sat}}\right)}\left[\beta\left(V_{\text{gs}} - V_{\text{ths}}\right)^{\frac{\alpha}{2}}V_{\text{dsat}} - \frac{\theta_{\text{short}}V_{\text{dsat}}^2}{2}\right] \tag{22}$$

where $V_{\text{dsat}} = V_{\text{gs}} - V_{\text{ths}}$, β is a technology-dependent empirical fitting parameter.

Results and Discussion

Several physics-based simulation models in Slivaco TCAD have been used to obtain the simulation outputs and verify the results. These models include band-to-band tunneling (BBT.STD) for considering the tunneling effect of charge carriers, drift-diffusion for carrier transport, CVT (Lombardi) mobility, Shockley-Read-Hall recombination for fixed lifetimes, concentration- and temperature-dependent ANALYTIC, HEI, parallel electric field-dependent FLDMOB, Auger recombination, concentration-dependent CONMOB and IMPACT SELB to consider the impact ionization effect. The INTERFACE statement is used to define the type and density of localized/fixed charges. Figure 2 exhibits the inner potential distribution of the proposed device along the position in the channel in the presence and absence of localized trap charges and also for three different temperatures. For all the cases of temperature variation, the source-channel barrier height of the inner potential minimum increases for negative trap charges compared to the case when there are no trap charges (the Si–SiO_2 interface is an ideal one). This implies a corresponding increase in the threshold voltage in the presence of negative trapped charges compared to the case when the interface is ideal (for no traps). For positive trap charges, the source-channel barrier height decreases compared to the ideal case, hence providing implications of reduced threshold voltage in presence of positive trapped charges. Now, as temperature gradually increases from 100 K to 500 K, the inner potential decreases as a whole. Impacts of such a behavior on threshold voltage of the device can be understood from threshold voltage plots provided in this section. In addition, gate work function engineering in the device resulted in the formation of a unique step profile in the channel at the junction of the dissimilar materials and this acts to reduce major SCEs such as drain-induced barrier lowering (DIBL) and hot-carrier effect (HCE). Figure 3a shows the distribution of inner potential for the proposed device for two different outer radii (keeping the filler radius fixed at 10 nm) in presence and in absence of localized interface trapped charges. The device shows similar behavior for positive, negative and zero trap charges as depicted in Fig. 2. Now, for an outer radius of 15 nm, the step profile is more pronounced compared to case where outer radius is 20 nm. A more prominent step profile allows better shielding effect from drain voltage fluctuations. Also, the inner potential minimum is more shifted towards the source for outer radius of 15 nm compared to the case where outer radius is 20 nm. Hence, the inner potential minimum obtained with an outer

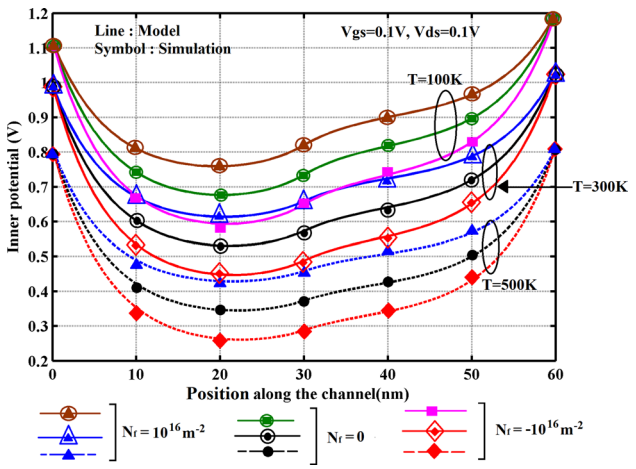


Fig. 2 Distribution of inner potential along channel length of the proposed device in the presence and absence of trap charges at different temperatures.

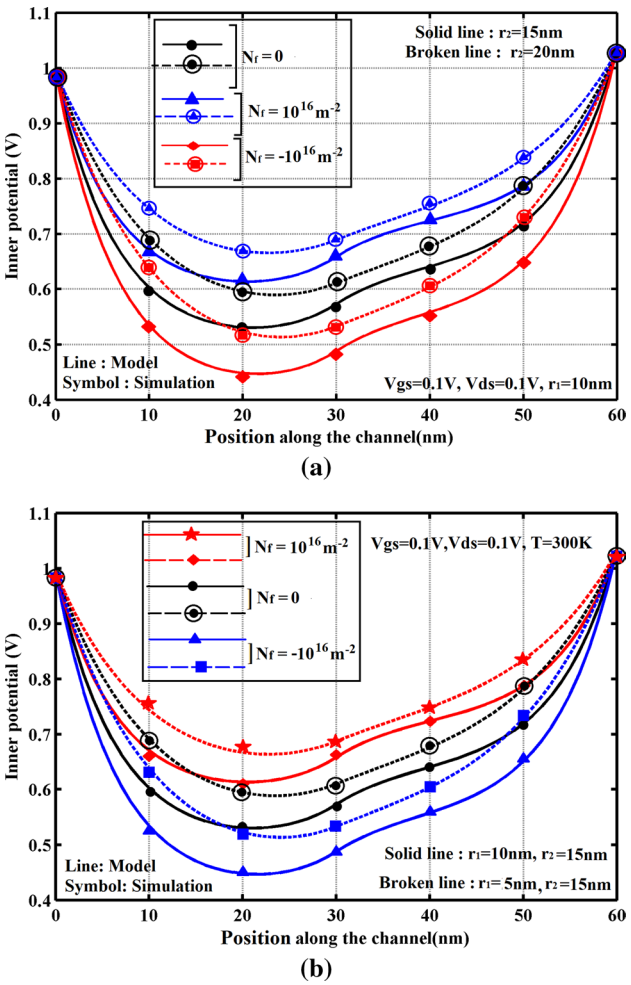


Fig. 3 (a) Distribution of inner potential along the channel position of the proposed device in the presence and absence of trap charges for two different values of outer radius keeping the filler radius fixed at 10 nm ($T = 300$ K), (b) Distribution of inner potential along the channel position of the proposed device in the presence and absence of trap charges for two different values of filler radius keeping the outer radius fixed at 15 nm ($T = 300$ K).

radius of 15 nm is more shielded from drain voltage fluctuations, and this is a highly desirable feature which a device is expected to possess. The reason for this trend is that, with a filler radius of 10 nm and outer radius of 15 nm, the channel thickness is lower and the gate can have more control over the channel, whereas for an outer radius of 20 nm, the channel thickness increases and the gate gradually loses control over the channel leading to increased short channel effects (SCEs). Also, the source-channel barrier height is enhanced for an outer radius of 15 nm (compared to $r_2 = 20$ nm), which implies a higher threshold voltage and diminished power dissipation due to reduced leakages (as a result of increased gate control over the channel). Figure 3b shows the distribution of inner potential of the proposed device for two different values of filler radii (keeping the outer radius fixed at 15 nm) in the presence and absence of localized interface trapped charges. The device shows similar behavior for positive, negative and zero trap charges as depicted in Fig. 2. The step profile of the inner potential distribution is more prominent for filler radius $r_1 = 10$ nm compared to the case with $r_1 = 5$ nm (for a fixed outer radius of r_2=15 nm). For filler radius $r_1 = 10$ nm, outer radius of $r_2 = 15$ nm, the channel thickness is less leading to enhanced gate control over the channel. This also results in higher threshold voltage and reduced off-state leakages. Inner potential distribution of the proposed device for different densities of positive and negative trap charges and also in the absence of trap charge is shown in Fig. 4. The plot is also shown for two different channel lengths, $L = 60$ nm, and for a much lower channel length, L = 40 nm. Inner potential for both channel lengths shows that as the density of positive trap charge increases, the source-channel barrier height significantly decreases that, in turn, lowers the threshold voltage allowing major off-state leakages. This causes degradation of the device performance since this enhances power dissipation. On the other hand, as the density of negative trap charges increases, the source-channel barrier height largely enhances which considerably enhances the threshold voltage leading to deteriorated circuit speed and increased power consumption. Moreover, as the channel length is scaled down to as low as 40 nm, the source-channel barrier height is affected and the height decreases further leading to reduction of threshold voltage.

Inner potential distribution along the channel length of the proposed device and its full channel cylindrical gate-all-around (GAA) counterpart is displayed in Fig. 5. As observed from the graph, the step profile in the proposed device is much more prominent compared to its cylindrical full-channel counterpart. Hence, it is obvious that the shielding effect to fluctuating drain voltages is much higher in the proposed device which leads to fewer SCEs and improved device performance. Also, the source-channel barrier height is greater in the proposed device (compared to the cylindrical contemporary), so threshold voltage is higher in the proposed device leading to reduced leakages and diminished off-state power dissipation.

Figure 6 shows the threshold voltage variation of the proposed device versus temperature in the presence and in absence of trap charges. Threshold voltage increases for negative trap charges compared to the case when no traps are present. For positive trap charges, threshold voltage decreases further compared to the case with no traps. This can be attributed to the fact that for negative charges, source-channel barrier height increases significantly contributing to elevated threshold voltage, while source-channel barrier height is much reduced for positive trap charges causing the

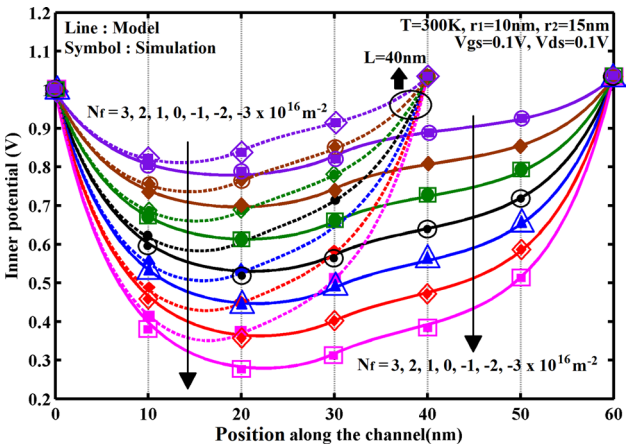


Fig. 4 Distribution of inner potential along the channel position of the proposed device for different densities of positive and negative trap charges, and without trap charges, for two different channel lengths ($T = 300$ K).

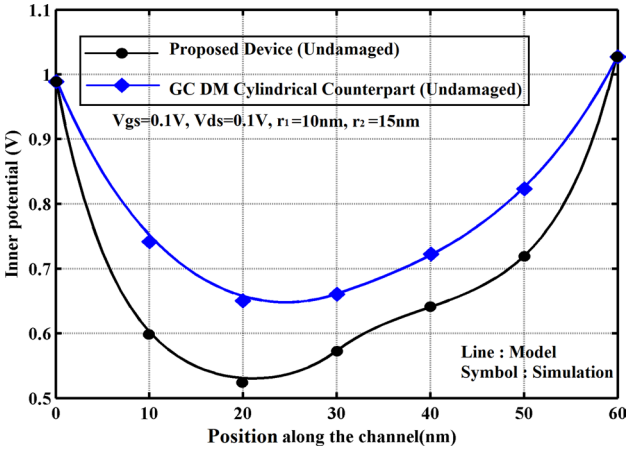


Fig. 5 Distribution of inner potential along the channel length in the absence of trap charges for the proposed device and its cylindrical full-channel GAA counterpart with the same radius as the outer radius of the proposed device ($T = 300$ K, $N_f = 0$).

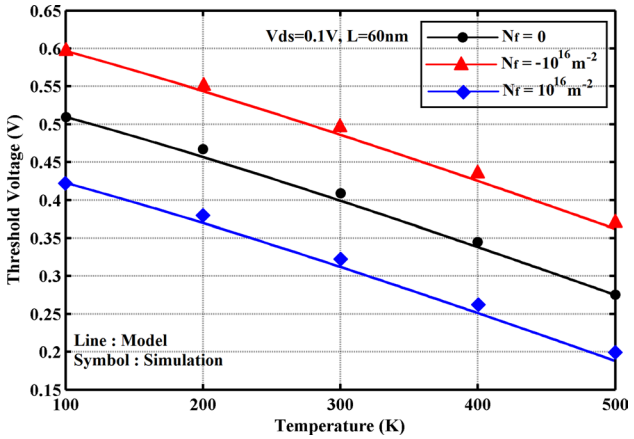


Fig. 6 Threshold voltage variation versus temperature of the proposed device in the presence and absence of trap charges.

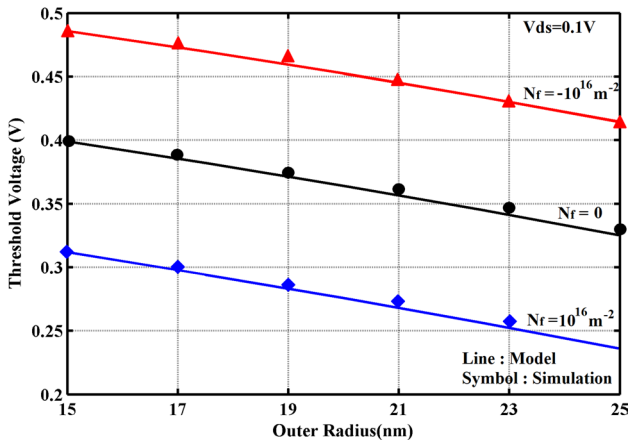


Fig. 7 Threshold voltage variation versus values of outer radius of the proposed device in the presence and absence of trap charges (filler radius = 10 nm, $L = 60$ nm, $T = 300$ K).

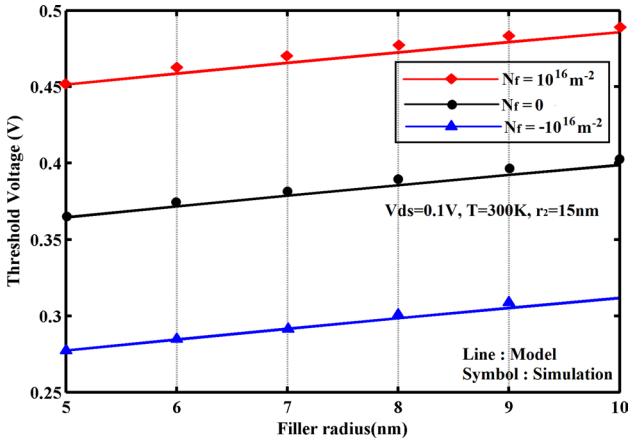


Fig. 8 Threshold voltage variation versus values of filler radius of the proposed device in the presence and absence of trap charges (outer radius = 15 nm, $L = 60$ nm, $T = 300$ K).

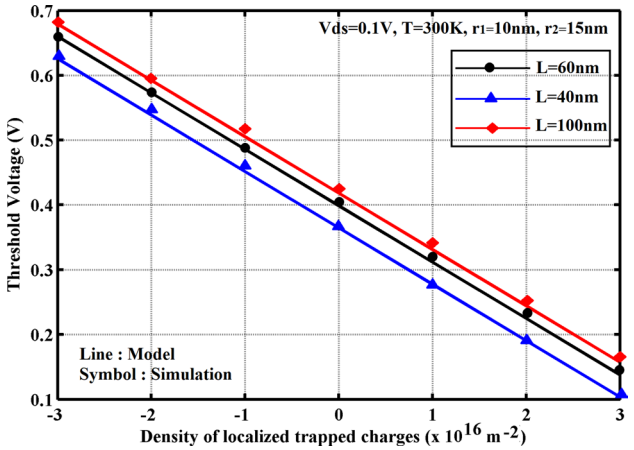


Fig. 9 Threshold voltage variation versus density of positive and negative trap charges in the proposed device for three different channel lengths.

threshold voltage to decrease as described in Fig. 2. As temperature increases, threshold voltage in all cases gradually decreases. This can be attributed to the fact that at increased temperatures, carrier generation is higher, and hence a very low gate voltage is required to turn on the device. Figure 7 displays the graphical illustration of the threshold voltage variation versus values of outer radius keeping the filler radius fixed at 10 nm and at $T = 300$ K (in the presence and absence of trap charges). As the outer radius increases gradually keeping filler radius fixed at 10 nm, the threshold voltage gradually decreases causing increased leakages and deteriorated device performance. With an enhanced outer radius, channel thickness increases resulting in weakened gate control over the channel. This feature has been apparently observed in Fig. 3a. Figure 8 illustrates the graphical extraction of threshold voltage vs. different values of filler radius keeping the outer radius fixed at 15 nm. It can be observed that as the filler radius increases, keeping the outer radius fixed at 15 nm, the channel thickness gradually decreases leading to enhanced gate control of the channel. This, in turn, escalates the threshold voltage, thereby diminishing the off-state leakages. This feature has already been observed in Fig. 3b. In short, keeping the filler radius fixed, threshold voltage decreases as the outer radius increases, and for a fixed outer radius, threshold voltage increases when the filler radius increases. Figure 9 exhibits the graphical analysis of threshold voltage variation for different densities of positive and negative trap charges and for three different channel lengths of the proposed device. As observed from Fig. 4, when the channel length is scaled down to 40 nm, the source-channel barrier height decreases (since SCEs

increase at short-channel lengths) causing the threshold voltage to decrease as compared to the case when $L = 60$ nm. Hence, threshold voltage is highest for L=100 nm, moderate for $L = 60$ nm and lowest for $L = 40$ nm for any density of positive/negative trap charges and also for the ideal case ($N_f = 0$). Now, as observed from Fig. 4, as the density of negative trap charge increases, threshold voltage also increases due to elevated source-channel barrier height and is the highest for the density – $3x10^{16}$ m^{-2}, and with increasing density of positive charges, source-channel barrier height decreases, thereby reducing the threshold voltage which has the lowest value for density of 3 x $10^{16}m^{-2}$.

Figure 10 demonstrates the threshold voltage variation of the proposed device and its full channel cylindrical gate-all-around (GAA) counterpart for zero traps. As previously discussed in Fig. 5, threshold voltage for the proposed device is higher compared to its cylindrical counterpart due to increased source-channel barrier height in the inner potential distribution. Also, a source-shifted minimum and prominent step profile in the proposed device results in lower threshold voltage roll-off which is considerably high in its full-channel cylindrical contemporary due to the absence of the above-mentioned properties in its inner potential distribution.

Figure 11 illustrates the graphical analysis of threshold voltage vs. channel length for graded and non-graded channels of the proposed device in the presence and absence of interface trap charges. For positive, negative and zero trap charges, threshold voltage follows the same trend as depicted before. Now, for an ungraded channel device, threshold voltage is the lowest, and when the channel is graded with high doping near the source, threshold voltage increases ensuring gradual reduction of leakages. Hence, the graded channel architecture with appropriate doping value selection allows suitable tuning of threshold voltage, thereby allowing the effective control of SCEs and leakages.

A major advantage of using a dual-material gate over single material is clearly highlighted in Fig. 12 which illustrates the DIBL variation for the above two device configurations for different temperatures. Step profiles are absent in the potential distribution of devices without GWFE, whereas prominent step profiles in DM devices allow a high shielding effect to DIBL. This unique potential step profile shields the inner potential minimum from being affected by drain voltage fluctuations, thereby resulting in higher immunity to DIBL in the proposed GWFE device compared to its single-material gate counterpart. Also, the DIBL variation at different temperatures for the GC DM full-channel cylindrical

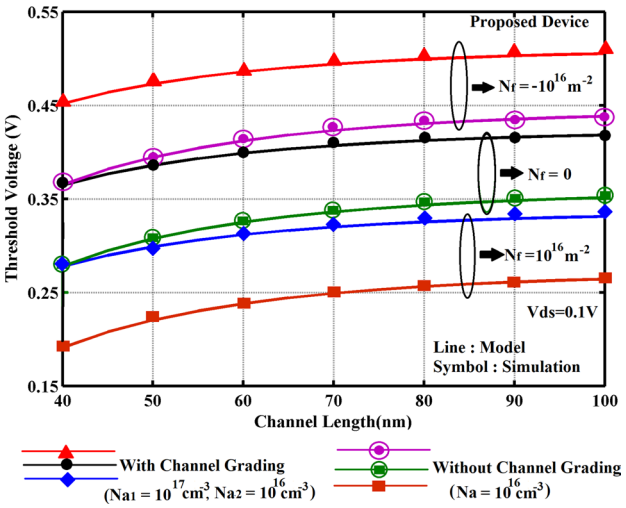


Fig. 11 Threshold voltage variation versus channel length of the graded and non-graded channel of the proposed device in the presence and absence of trap charges.

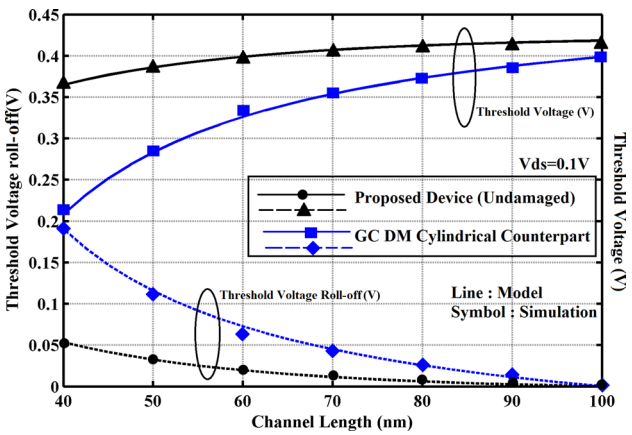


Fig. 10 Threshold voltage roll-up and threshold voltage variation vs. channel length for the proposed device and its GC DM cylindrical counterpart with the same radius as the outer radius of the proposed device.

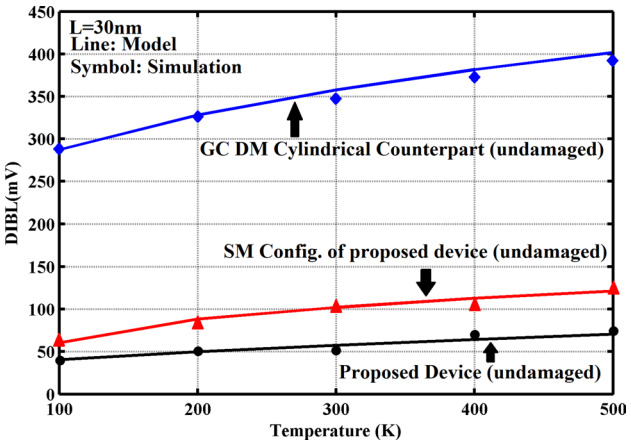


Fig. 12 DIBL variation for different temperatures in the absence of trap charges for the proposed device, its SM counterpart and GC DM full-channel cylindrical counterpart with a radius similar to the outer radius of the proposed device ($T = 300$ K).

counterpart of the proposed device is exhibited in the same graphical plot. Figure 10 clearly exhibits that, with the reduction in channel length, the threshold voltage for the GC DM full-channel cylindrical MOSFET greatly decreases compared to that in the proposed device. The roll-off is higher in the GC DM full-channel cylindrical MOSFET, and for a channel length as high as 100 nm, the threshold voltage for the above device is still lower than the proposed device at 100-nm channel length. This reduced threshold voltage implies an increased DIBL in the GC DM cylindrical device, which becomes aggressive when the channel length is scaled down to as low as 40 nm. This is shown in Fig. 12 where the DIBL values for a temperature range of 100–500 K for the GC DM cylindrical device (with the same radius as the outer radius of the proposed device) is significantly higher than both the proposed device and its SM counterpart at a scaled channel length of 30 nm. Hence, among the three devices, the proposed device, which shows the least DIBL, has excellent immunity against major SCEs such as DIBL.

Reduced temperatures lead to a lower impact ionization rate compared to that at heightened temperatures which leads to upgraded subthreshold swing characteristics in the proposed device as observed in Fig. 13. Many researchers have reported on short-channel MOSFETs revealing the subthreshold swing characteristics at low temperatures of 100 K and 200 K. Ghibaudoa et al.[17] reported subthreshold swing values of as low as about 20 mV/dec at 10 0K and about 40 mV/dec at 200 K. Biswas et al.[18] reported subthreshold swing values as low as 20 mV/dec at 100 mV and about 40mV/dec at 200 K for both strained and unstrained channel MOSFETs. The trend of subthreshold swing as obtained in the case of the proposed device closely matches the trend of SS shown by MOSFET devices at low temperatures of 100 K and 200 K. Hence, subthreshold swing largely depends on temperature and decreases (increases) with a decrease (increase) in temperature. A comparative subthreshold swing investigation of the proposed device and its GC DM full-channel cylindrical counterpart is presented through a graphical analysis in Fig. 14. The figure clearly exhibits that SS in proposed device for channel lengths as low as 40 nm, is about 70 mV/dec, whereas, for the GC DM full-channel cylindrical MOSFET, SS at 40-nm channel length is as high as about 110 mV/dec. Also, as channel length gradually increases to 100 nm, SS for the proposed device saturates to 60 mV/dec (the ideal value of SS for short-channel MOSFETs), while that for the GC DM full-channel cylindrical counterpart, the SS value saturates to as high as about 65 mV/dec at 100-nm channel length.

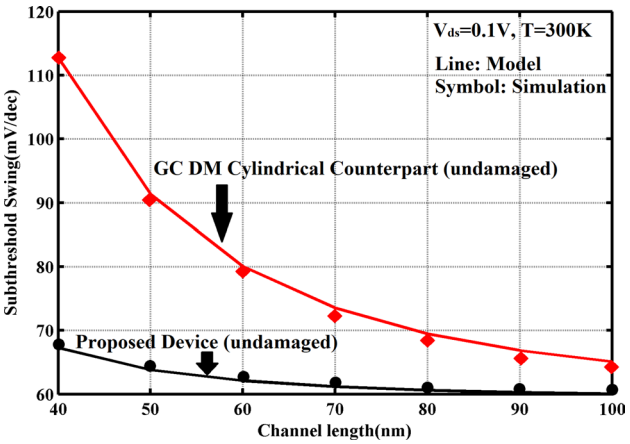


Fig. 14 Subthreshold swing variation versus channel length in the absence of trap charges for the proposed device and its GC DM full-channel cylindrical counterpart.

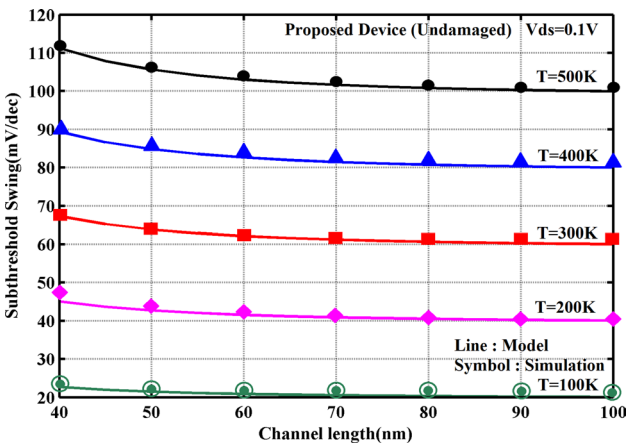


Fig. 13 Subthreshold swing variation versus channel length in the absence of trap charges for the proposed device at different temperatures.

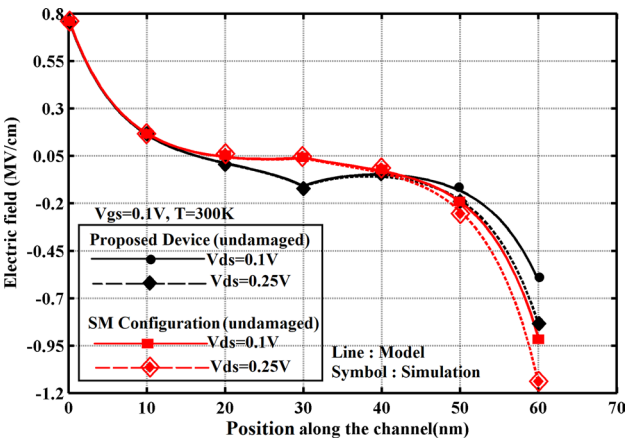


Fig. 15 Lateral electric field variation along channel position for different drain voltages in the absence of trap charges for the proposed device and its SM counterpart with the same radius as the outer radius of the proposed device ($T = 300$ K, $N_f = 0$).

Another advantage of gate work function engineering (GWFE) can be observed from Fig. 15 where the electric field at the drain end is reduced in the case of the proposed device compared to its SM counterpart. This results in a reduced hot-carrier effect (HCE)[19,20] in the device. Also, in both cases, lateral electric field increases at the drain end with an increase in V_{ds}. In the proposed device, the electric field peaks at the interface of two dissimilar materials, thereby boosting the transport efficiency. This feature is absent in SM devices due to the absence of a step profile in their inner potential distribution. Figure 16 presents the drain current analysis of the proposed device versus gate bias for different densities of positive and negative trapped charges. Since the threshold voltage for negative trapped charges is higher among the three cases, lower off-state leakages occur which cause the subthreshold current to decrease, whereas the gate-induced drain leakage (GIDL) current increases. For no trap charges, threshold voltage decreases compared to the previous case, hence subthreshold current increases compared to the previous case. However, GIDL decreases. For positive trapped charges, threshold voltage is lowest among the three cases, hence the subthreshold current highly increases, whereas GIDL current largely decreases. Further, as the density of negative trapped charges increases, threshold voltage highly increases. For a density value of $3x10^{16}$ m^{-2}, subthreshold current is significantly suppressed reducing off-state leakages while the reverse case occurs for the highest density of positive trapped charges.

Use of a gate material with lower work function (compared to the work function of a gate material at the source side) contributes to a decrease the electric field at the drain end thereby diminishing the speed of electrons at the drain end, and this, in turn, decreases the minority carrier tunneling from the drain. Since the flat-band voltage is directly proportional to the gate material work function, it can be said that a lower flat-band voltage at the drain side causes the suppression of minority carriers from the drain, hence improving the GIDL effect and reducing the GIDL current. As per the equation, $V'_{fb_i} = V_{fbi} - \frac{qN_f 7}{C_{ox}}$ (keeping a gate material with a lower work function towards the drain) the presence of positively charged traps decrease the flat-band voltage further at drain end thereby largely decreasing GIDL current. For negative trapped charges, flat-band voltage at the drain increases allowing significant minority carrier tunneling and worsening device performance by increasing the GIDL current which clearly demonstrates the physics governing the graphical illustration in Fig. 16.

In Fig. 17, GIDL current is very high in the single-material (SM) gate device compared to the proposed device due to high flat-band voltage at the drain end in the SM device, which induces a high electric field thereby allowing more minority carriers to tunnel from the drain into the channel. Also, the SM device suffers from high DIBL which increases the subthreshold leakage current in the device compared to the proposed GWFE device. These graphical illustrations confirm the superiority of the proposed device and creates remarkable avenues for it to be implemented in the forthcoming generation VLSI circuital applications.

Results of this section are verified using simulation outputs from Silvaco TCAD, and the results exhibit the superiority of the proposed device over the existing contemporary devices.

Conclusion

The current research effort presents the localized trap charge induced analytical modelling and simulation of a graded-channel dual-material gate macaroni MOSFET.

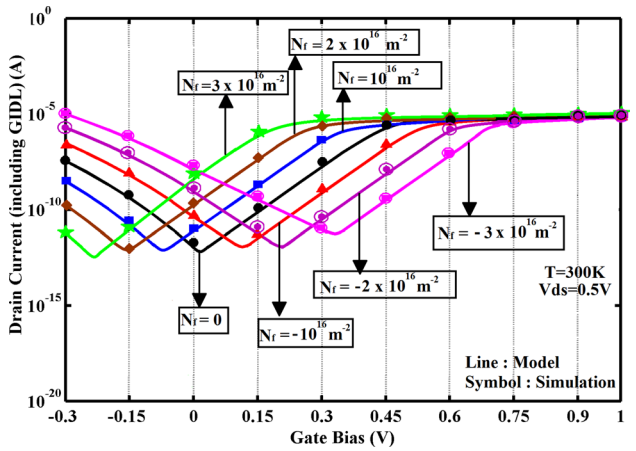


Fig. 16 Drain current variation versus gate for different densities of positive and negative trap charges for the proposed device (L = 60 nm).

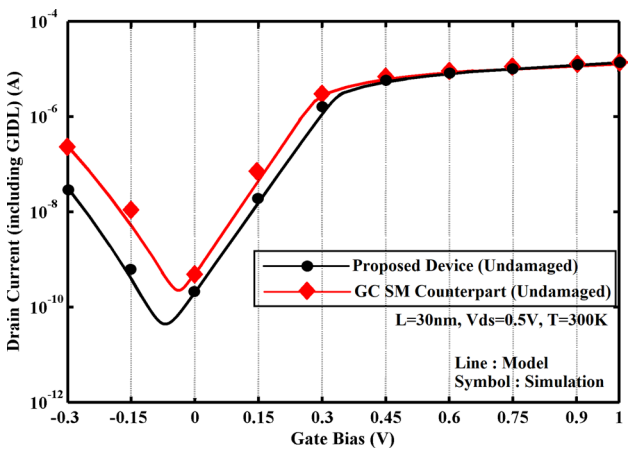


Fig. 17 Drain current variation versus gate voltage in absence of trap charges for proposed device and its SM counterpart.

Temperature-dependent performance reliability of the proposed device (both damaged and undamaged) has been meticulously analyzed from the inner potential distribution, threshold voltage and short-channel effect response. Trap charges significantly modulate device flat-band voltage which consequently affects device features. Drain current analysis including the gate-induced drain leakage (GIDL) effect has been presented for both the damaged and undamaged device and results exhibit significant drain current alterations in the presence of trap charges. This reflects the importance of investigating damaged device features along with the undamaged one. The proposed device exhibits upgraded short channel performance compared to its full-channel gate-all-around (GAA) cylindrical counterpart in terms of threshold voltage, threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold swing (SS) that highlights the advantages of macaroni configuration, making it a prospective replacement for full-channel GAA cylindrical MOSFFETs. Further, comparative study of short-channel effects (SCEs), gate-induced drain leakage (GIDL) analysis between the proposed device and its single-material counterpart (even at a scaled length of 30 nm) clearly exhibits the advantages of gate work function engineering (GWFE) in the former device over the latter. Further, results demonstrate that proper selection of channel grading concentrations can suitably tune the threshold voltage in the proposed graded-channel device. Simulation outputs match well with analytical results thereby validating the proposed device as a potential contender for future generation VLSI applications.

Appendix

Expressions of $\alpha_1, \beta_1, \alpha_2, \beta_2$ in Eqs. 6, 7 are listed as follows:

$$\alpha_2 = \left[\frac{\left\{\left(V_{\mathrm{bi}_1}(T)\exp(L/\lambda)\right)-\left(V_{\mathrm{bi}_2}(T)+V_{\mathrm{ds}}\right)\right\}+S_{12}\cosh\left(L_2/\lambda\right)+\left(V'_{\mathrm{fb}_1}+\frac{qNa_1\lambda^2}{\varepsilon_{\mathrm{Si}}(T)}\right)\exp(L/\lambda)-\left(V'_{\mathrm{fb}_2}+\frac{qNa_2\lambda^2}{\varepsilon_{\mathrm{Si}}(T)}\right)}{2\sinh(L/\lambda)}\right],$$

$$\beta_2 = \left(\frac{1-\exp(L/\lambda)}{2\sinh(L/\lambda)}\right), \qquad \alpha_1 = \left(V_{\mathrm{bi}_1} - \alpha_2 + V'_{\mathrm{fb}_1} + \frac{qNa_1\lambda^2}{\varepsilon_{\mathrm{Si}}(T)}\right),$$

$\beta_1 = -1 - \beta_2, S_{12} = \varphi_{01} - \varphi_{02}$

Expressions of a, b and c in Eq. 11 are listed as follows:

$$a = 4\beta_1\beta_2 - 1,$$

$$b = 2\left[\left\{2\left(\alpha_1\beta_2 + \alpha_2\beta_1\right) + \left(2\phi_{f_1}(T) + V'_{\mathrm{fb}_1} + \frac{q\mathrm{Na}_1\lambda^2}{\varepsilon_{\mathrm{Si}}(T)}\right)\right\}\right],$$

$$c = \left[4\left(\alpha_1\alpha_2\right) - \left(2\phi_{f_1}(T) + V'_{\mathrm{fb}_1} + \frac{q\mathrm{Na}_1\lambda^2}{\varepsilon_{\mathrm{Si}}(T)}\right)^2\right]$$

Subthreshold Drain Current Modelling (Contd.)

Substituting Eq. 18 into Eq. 17, the equation thus obtained is as follows:

$$I_{\mathrm{DS}}\int_0^L dz(z) = \frac{\mu'_n}{1+\theta\left(V_{\mathrm{gs}}-V_{\mathrm{THR}}\right)}\pi\left(r_2^2-r_1^2\right)qn_i(T)\int_0^{V_{\mathrm{ds}}}\exp\left(\frac{\psi_{01\,\min}-V}{V_T}\right)dV(z) \tag{23}$$

The final expression for the drain current of the device is:

$$I_{DS} = \frac{\mu'_n}{1+\theta\left(V_{gs}-V_{THR}\right)}\pi\frac{\left(r_2^2-r_1^2\right)}{L}qn_i(T)\exp\left(\frac{\psi_{01\,\min}}{V_T}\right)V_T\left[1-\exp\left(-V_{ds}/V_T\right)\right] \tag{24}$$

Here, $\mu'_n = \frac{\mu_n}{\sqrt{\left(1+\frac{\mathrm{Na}_1}{N_{\mathrm{ref}}+\mathrm{Na}_1 S_1}\right)}}$, μ_n is the electron mobility, S_1 and θ are fitting parameters.

Authors' contributions All the authors have significant contributions and have given final approval of this version to be published.

Funding Pritha Banerjee as the Principal Investigator and a DST Woman Scientist (A) thankfully acknowledges the financial support obtained from the **Department of Science and Technology (DST)**, Ministry of Science and Technology, Government of India, to carry out this research work under **Women Scientist Scheme (WOS-A)** vide File No. SR/WOSA/PM-82/2018.

Conflicts of interest The authors declare that there is no Conflicts of interest/Competing interests.

Consent for Publication The authors declare their consent for publication upon acceptance of paper.

Ethical approval The authors declare that all procedures followed were in accordance with the ethical standards.

References

1. A. Tsormpatzoglou, C.A. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, Threshold Voltage Model for Short-Channel Undoped Symmetrical Double-Gate MOSFETs. *IEEE Trans. Electron Devices.* 55, 2512 (2008).
2. T.K. Chiang, A New Compact Subthreshold Behavior Model for Dual-Material Surrounding Gate (DMSG) MOSFETs. *Solid-State Electron.* 53, 490 (2009).
3. R. Das, M. Chanda, and C.K. Sarkar, Analytical Modeling of Charge Plasma-Based Optimized Nanogap Embedded Surrounding Gate MOSFET for Label-Free Biosensing. *IEEE Trans. Electron Devices.* 65, 5487 (2018).
4. M.A. Abdi, F. Djeffal, Z. Dibi, and D. Arar, A Two Dimensional Analytical Subthreshold Behavior Analysis Including Hot-Carrier Effect for Nanoscale Gate Stack Gate all Around (GASGAA) MOSFETs. *J. Comput. Electron.* 10, 179 (2011).
5. Q. Nguyen-Gia, M. Kang, J. Jeon, and H. Shin, Characteristic Length of Macaroni Channel MOSFET. *IEEE Electron Device Lett.* 40, 1720 (2019).

6. G.M. Paolucci, A.S. Spinelli, C.M. Compagnoni, and P. Tessariol, A Semi-Analytical Model for Macaroni MOSFETs With Application to Vertical Flash Memories. *IEEE Trans. Electron Devices.* 63, 1871 (2016).
7. T.K. Chiang, A Compact Model for Threshold Voltage of Surrounding-Gate MOSFETs with Localized Interface Trapped Charges. *IEEE Trans. Electron Devices.* 58, 567 (2011).
8. A. Goel, S. Rewari, S. Verma, and R.S. Gupta, Temperature-Dependent Gate-Induced Drain Leakages Assessment of Dual-Metal Nanowire Field-Effect Transistor—Analytical Model. *IEEE Trans. Electron Devices.* 66, 2437 (2019).
9. R. Gautam, M. Saxena, R.S. Gupta, and M. Gupta, Temperature Dependent Subthreshold Model of Long Channel GAA MOSFET Including Localized Charges to Study Variations in its Temperature Sensitivity. *Microelectron. Reliab.* 54, 37 (2014).
10. S. Dubey, A. Santra, G. Saramekala, M. Kumar, and P.K. Tiwari, An Analytical Threshold Voltage Model for Triple-Material Cylindrical Gate-All Around (TM-CGAA) MOSFETs. *IEEE Trans Nanotechnol.* 12, 766 (2013).
11. Q. Nguyen-Gia, M. Kang, J. Jeon, and H. Shin, Models of Threshold Voltage and Subthreshold Slope for Macaroni Channel MOSFET. *IEEE Electron Device Lett.* 41, 973 (2020).
12. P. Banerjee, and J. Das, Gate Work Function Engineered Trigate MOSFET with a Dual-Material Bottom Gate for Biosensing Applications: a Dielectric-Modulation Based Approach. *SILICON* (2020). https://doi.org/10.1007/s12633-020-00823-5.
13. L. Zhang, L. Li, J. He, and M. Chan, Modeling Short-Channel Effect of Elliptical Gate-All-Around MOSFET by Effective Radius. *IEEE Electron Device Lett.* 32, 1188 (2011).
14. H. Ghanatian, and S.E. Hosseini, Analytical Modeling of Subthreshold Swing in Undoped Trigate SOI MOSFETs. *J. Comput. Electron.* 15, 508 (2016).
15. S. Rewari, V. Nath, S. Haldar, S.S. Deswal, and R.S. Gupta, Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET. *IEEE Trans. Electron Devices.* 65, 3 (2018).
16. A. Pal, and A. Sarkar, Analytical Study of Dual Material Surrounding Gate MOSFET to Suppress Short-Channel Effects (SCEs). *Int. J. Eng. Sci. Technol.* 17, 205 (2014).
17. G. Ghibaudoa, M. Aouadb, M. Casseb, S. Martinieb, T. Poirouxb, and F. Balestraa, On the Modelling of Temperature Dependence of Subthreshold Swing in MOSFETs down to Cryogenic Temperature. *Solid-State Electron.* 170, 107820 (2020).
18. A. Biswas, and S. Bhattacherjee, Temperature dependent model for threshold voltage and subthreshold slope of strained-Si channel MOSFETs with a polysilicon gate. *Microelectron. Reliab.* 54, 1527 (2014).
19. R. Bouchakour, L. Hardy and M. Jourdain, An Analytical Model for Hot-Carrier-Induced Degradation of Submicron N-MOSFET in ESSDERC '96: Proceedings of the 26th European Solid State Device Research Conference (1996), p. 271
20. S.R. Sriram, and B. Bindu, Analytical Model of Hot Carrier Degradation in Uniaxial Strained Triple-Gate FinFET for Circuit Simulation. *J. Comput. Electron.* 17, 163 (2018).

165 (2022) 207196

Contents lists available at ScienceDirect

Micro and Nanostructures

journal homepage: www.journals.elsevier.com/micro-and-nanostructures

Analytical Exploration and Simulation of Dual-Material Gate Macaroni Channel MOSFET biosensor using dielectric-modulation technique

Pritha Banerjee *, Jayoti Das

Department of Physics Jadavpur University, Kolkata, India

ARTICLE INFO

Keywords:
Biosensor
Macaroni-channel MOSFET
Sensitivity
Short channel effects (SCEs)

ABSTRACT

The paper presents extensive analytical modeling and simulation of a novel Dual-Material Gate Macaroni-Channel MOSFET to act as a biosensor for detection of neutral as well as charged biomolecules using dielectric modulation approach. Dielectric modulation in a MOSFET device is the alteration in the dielectric constant in the gate dielectric region of the device. Presence of biomolecules (in a nanogap etched under the gate of the projected device) having different dielectric constants impact the gate capacitance that in turn affects the device features such as potential, threshold voltage, drain current which undergo considerable shift in presence of biomolecules. Detailed Sensitivity analysis based on threshold voltage shift for different types of biomolecule allows suitable detection of biomolecule type. Suitable selection of device outer radius allows significant suppression of some major Short channel effects such as threshold voltage reduction, reduced subthreshold swing enabling superior device performance. Finally, comparative sensitivity analysis of the proposed device with its full channel Cylindrical Gate-all-around counterpart having same channel thickness exhibits better sensitivity capability of the proposed device for both neutral and charged biomolecule. Analytical results are substantiated using Atlas simulation outputs.

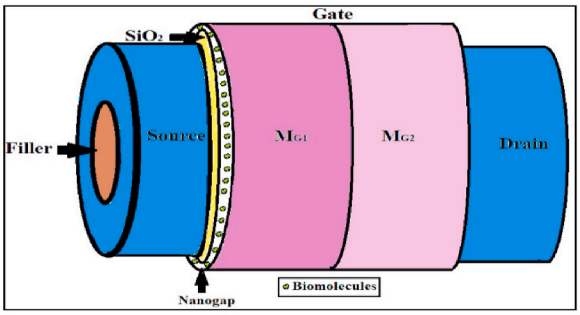
1. Introduction

Bioelectronics has received foremost consideration in the ongoing era of electronics industrial resurgence. This indispensable branch of electronics has observed striking, noteworthy developments in the recent decades which contributed significantly to ease critical medical treatments in less time. While the lives of entire human population is solely dependent on healthcare protocols, hence this drives the necessity for technical up gradation of existing ways of medical treatments to help the civilization fight major healthcare related crisis. The recent pandemic of Covid-19 has made this truth more prominent. While scientists all over the world are trying to bring up effective vaccines, it is equally important to detect the harm causing virus at an early stage to stop mass infection and death preventions. Biosensors can work wonders in this context. Nowadays, FET based biosensors are receiving significant attention where the easy method of detection through dielectric-modulation approach has been made possible [1,2]. However, the MOSFET geometry used in devising the biosensor should be wisely selected to provide better performance. In nano-meter regime, the planar MOSFETs have been found to suffer highly from SCEs that degrade the device performance and hinder the effective action of the biosensor.

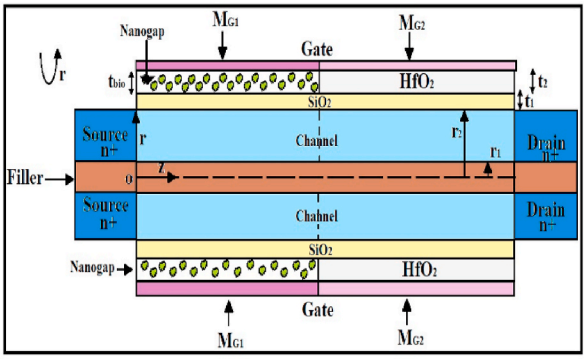
* Corresponding author.
E-mail address: prithaedu7@gmail.com (P. Banerjee).

https://doi.org/10.1016/j.micrna.2022.207196
Received 13 September 2021; Received in revised form 21 February 2022; Accepted 6 March 2022
Available online 28 March 2022

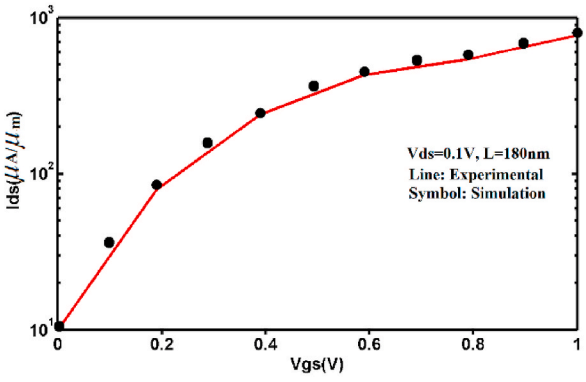
Cylindrical MOSFETs are very popular for their upgraded SCE performances [3,4]. However recent study shows Macaroni channel MOSFETs excel cylindrical ones in terms of offering superior device performances. Hence, the basic structure for implementation of the biosensor has been considered to be a Macaroni-channel MOSFET, where the geometry is like a cylindrical MOSFET with a filler present at the channel center. The Macaroni structures are also fabrication feasible as observed from the researches exhibited by Delhougne et al. [5] where the authors, for the first time, demonstrated the step by step fabrication process of macaroni channel device having a channel made of monocrystalline silicon. Congedo et al. [6] also described detailed fabrication procedures for Macaroni channels. This fabrication compatible Macaroni structure has been found to perform better than cylindrical structures. Hence, new device formulation is necessary for the Macaroni Sensor. Further, a dual-Material gate has been introduced so as to weaken the major SCEs like Drain-induced barrier lowering (DIBL), Hot carrier effects (HCE), etc. Further, suitable selection of the outer radius can help suppress the SCEs that are also substantiated through the threshold voltage and subthreshold swing results. In the proposed structure,



a



b



c

Fig. 1. a 3-D Schematic Representation of Proposed Dual-Material Gate Macaroni-Channel MOSFET Biosensor, b 2-D Cross-sectional Representation of Proposed Dual-Material Gate Macaroni-Channel MOSFET Biosensor, cCalibration of simulated data with experimental data following [19].

the gate oxide is composed of an interfacial SiO_2 layer. Towards the source side, the region beneath the gate material and interfacial oxide layer is etched to form a nanogap for the biomolecules. A number of research papers demonstrated the fabrication process regarding the formation of nanogap (that act as the site for biomolecules) in FET devices. Following the procedure described by Kim et al. [7], firstly the Macaroni channel, source and drain extensions are grown using photolithography and ion-implantation after a device-isolation step, for the projected device. HfO_2 (under gate material M_{G2}), SiO_2, Cr (under gate material M_{G1}) and gate materials are to be subsequently grown and deposited using the thin film processes. Cr is the sacrificial layer that leaves the nanogap after selective wet etching. After the above three layers are deposited, they are patterned by photolithography and subsequent etching processes. The nanogap is now formed by lateral wet etching of Cr. The interfacial layer of SiO_2 is used for biomolecule immobilization [8]. When the nanogap is filled with air, the condition is considered as absence of biomolecule. When it is filled with biomolecule such as streptavidin (K = 2.1), protein (K = 2.50), biotin (K = 2.63), APTES (K = 3.57), etc. the gate capacitance changes causing the threshold voltage to change. Towards the drain side, hafnium oxide is placed over interfacial oxide layer to allow improvement of subthreshold slope characteristics [9]. A high gate work function material towards source side allows confinement of the potential minimum towards source side, which is absent in case of single material gate structures. A low work function gate material towards drain side causes the potential towards drain to rise compared to minimum potential towards source side. Thus the source-shifted potential minimum gets shielded from drain voltage fluctuations and remains unaltered thereby offering better SCE performances. Mathematical outputs are validated using simulation outputs from Atlas.

2. Device architecture

The proposed biosensor is shown in Fig. 1a. The MOSFET has a Macaroni channel with filler radius $r_1 = 10$ nm and outer radius $r_2 = 20$ nm, channel thickness $t_{Si} = 2$ (r_2-r_1). The channel has a doping concentration $N_a = 10^{17}cm^{-3}$. The gate oxide consists of an interfacial SiO_2 layer (thickness $t_1 = 1$ nm). The gate is of Dual-Material, gate material M_{G1} (Work function = 4.8eV) towards source has higher work function and that towards drain side M_{G2} (Work function = 4.4eV) has lower work function. Gate length (L_1) of M_{G1} is 30 nm, and that under M_{G2} is (L_2) 30 nm. The region beneath M_{G1} and above the interfacial oxide layer is etched to form a nanogap (thickness $t_{bio} = 9$ nm) to act as site for the biomolecules. The region beneath M_{G2} has a high-k oxide HfO_2 placed above the interfacial layer of SiO_2.

The proposed device has a great similarity in topology with Cylindrical Surrounding Gate MOSFET Following the parameters specified in Ref. [19] for Cylindrical Surrounding Gate MOSFET, the experimental outputs are used to verify the simulated outputs as shown in Fig. 1c.

3. Analytical modeling

3.1. a. Inner potential modeling

The first step to explore the detailed sensitivity analysis of the proposed biosensor is to obtain the expression of inner potential, which can be obtained by solving the 2-D Poisson's equation which is as follows [10].

$$\frac{\partial^2 \Psi_i(r,z)}{\partial r^2} + \frac{1}{r}\frac{\partial \Psi_i(r,z)}{\partial r} + \frac{\partial^2 \Psi_i(r,z)}{\partial z^2} = \frac{qN_a}{\varepsilon_{Si}} \tag{1}$$

Where i = 1, 2 for Region 1 and 2 respectively. Region 1 is confined by the boundaries $0 \le z \le L_1, r_1 \le r \le r_2$ and Region 2 has boundaries $L_1 \le z \le L, r_1 \le r \le r_2$. $\Psi_i(r,z)$ is the potential distribution in the ith region. ε_{Si} is the permittivity of the silicon channel.

The potential distribution is parabolic along the radial direction. It is expressed as:

$$\Psi_i(r,z) = a_{1i}(z) + a_{2i}(z)r + a_{3i}(z)r^2 \tag{2}$$

The coefficients in the above equation can be obtained using the following boundary conditions [11].

$$\left.\frac{\partial \Psi_i(r,z)}{\partial r}\right|_{r=r_1} = a_{2i}(z) + 2r_1 a_{3i}(z) = 0 \tag{3}$$

$$\left.\frac{\partial \Psi_i(r,z)}{\partial r}\right|_{r=r_2} = \frac{C_{fi}}{\varepsilon_{Si}}\left[V_{gs_i} - \Psi_i(r_2,z)\right] \tag{4}$$

Using equations (3) and (4), the coefficients' expressions thus obtained are

$$a_{2i}(z) = -2r_1 a_{3i}(z) \tag{5}$$

$$a_{3i}(z) = \frac{4C_{fi}\left[V_{gs_i} - \psi_{0i}(z)\right]}{\left[C_{fi}t_{Si}^2 + 4\varepsilon_{Si}t_{Si}\right]} \tag{6}$$

Here, $\psi_{0i}(z)$ is the inner potential in Region i, $C_{f_1} = \frac{\varepsilon_{SiO_2}}{r_2 \ln\left(1+\frac{t_{eff_1}}{r_2}\right)}$, $t_{eff_1} = t_{SiO_2} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{bio}}t_{bio}$, $V_{gs_i} = V_{gs} - V_{fb_i}{}'$,

$$V_{fb_1}{}' = V_{fb_1} - \frac{qN_f}{C_{f_1}}, \tag{7}$$

N_f is the charge density of biomolecules in the nanogap.

$$C_{f_2} = \frac{\varepsilon_{SiO_2}}{r_2 \ln\left(1 + \frac{t_{eff_2}}{r_2}\right)},\ t_{eff_2} = t_{SiO_2} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} t_{high-k}$$

Putting expressions (5) and (6) in equation (2) and then in equation (1), the final differential equation obtained for Region (1) at $r = r_1$ is as follows:

$$\frac{\partial^2 \psi_{0i}(z)}{\partial z^2} + 2a_{3i}(z) = \frac{qN_a}{\varepsilon_{Si}} \tag{8}$$

Solution to the above differential equation is given as follows:

3.2. Expression of Inner potential in region 1

$$\psi_{01}(z) = M_1 \exp(z/\lambda_1) + N_1 \exp(-z/\lambda_1) + \varphi_{01} \tag{9}$$

Here, $\frac{1}{\lambda_1} = \sqrt{\frac{8C_{f_1}}{[C_{f_1} t_{si}{}^2 + 4\varepsilon_{si} t_{si}]}}$, $\varphi_{01} = V_{gs_1} - \frac{qN_a \lambda_1{}^2}{\varepsilon_{si}}$

3.2.1. Expression of inner potential in region 2

$$\psi_{02}(z) = M_2 \exp((z - L_1)/\lambda_2) + N_2 \exp(-(z - L_1)/\lambda_2) + \varphi_{02} \tag{10}$$

Here, $\frac{1}{\lambda_2} = \sqrt{\frac{8C_{f_2}}{[C_{f_2} t_{si}{}^2 + 4\varepsilon_{si} t_{si}]}}$, $\varphi_{02} = V_{gs_2} - \frac{qN_a \lambda_2{}^2}{\varepsilon_{si}}$

The coefficients M_1, N_1, M_2, N_2 can be obtained following the below listed boundary conditions [12]:

$$\psi_{01}(z)|_{z=0} = V_{bi} \tag{11}$$

$$\psi_{02}(z)|_{z=L} = V_{bi} + V_{ds} \tag{12}$$

$$\psi_{01}(z)|_{z=L_1} = \psi_{02}(z)|_{z=L_1} \tag{13}$$

$$\left.\frac{\partial \psi_{01}(z)}{\partial z}\right|_{z=L_1} = \left.\frac{\partial \psi_{02}(z)}{\partial z}\right|_{z=L_1} \tag{14}$$

The expressions of the coefficients M_1, N_1, M_2, N_2 are shown in appendix.

3.3. b. threshold voltage modeling

The value of V_{gs} at which the minimum inner potential can be equated to twice the Fermi Potential can be termed as the threshold voltage V_{th} [13]. The inner potential minimum is found to occur in Region 1 so determination of position of minimum inner potential is necessary for threshold voltage formulation.

The position of minimum inner potential can be obtained using the following equation:

$$\frac{d\psi_{01}(z)}{dz} = 0 \tag{15}$$

Hence, the position of minimum potential is. $z_{\min} = \frac{\lambda_1}{2} \ln \frac{N_1}{M_1}$

Equating minimum Inner potential to twice the Fermi potential, the expression of threshold voltage thus obtained is

$$V_{th} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{16}$$

where a, b and c expressions are shown in Appendix section.

DIBL (mV) [14] is modeled using the following equation as follows:

$$DIBL = V_{th,lin} - V_{th,sat} \tag{17}$$

Subthreshold Swing (mV/dec) [15] is modeled as follows:

$$SS = 2.3V_t\left[\frac{d\psi_{0\min}(z)}{dV_{gs}}\right]^{-1} \tag{18}$$

c. Sensitivity Analysis of the Proposed Biosensor.

For neutral biomolecules, Sensitivity is defined by the following equation [16]:

$$S_{n,bio} = \left|\frac{V_{th}(K=1) - V_{th}(K>1)}{V_{th}(K=1)}\right| \tag{19}$$

For charged biomolecules, Sensitivity is defined by the following equation:

$$S_{c,bio} = \left|\frac{V_{th}(Bio_{neutral}) - V_{th}(Bio_{charged})}{V_{th}(Bio_{neutral})}\right| \tag{20}$$

d. Drain Current Modeling.

A unified model for the drain current analysis of the proposed biosensor is shown below [17]:

$$I_{ds} = \begin{bmatrix} I_{sub}, 0 \le V_{gs} \le V_{th} \\ I_{lin}, V_{th} \le V_{gs} \le V_{sat} \\ I_{sat}, V_{sat} \le V_{gs} \le 1.0 \end{bmatrix} \tag{21}$$

3.4. *Subthreshold current is in the limit* $0 \le V_{gs} \le V_{th}$

Electron current in the channel of the device under consideration is as follows [18]:

$$I_{DS}(z) = \int_{r_1}^{r_2} 2\pi R J(r,z)dr \tag{22}$$

Here diffusion current density is given by

$$J(r,z) = \frac{\mu_{eff}}{1+\theta(V_{gs}-V_{th})} qn_i(T)\exp\left(\frac{\psi_{01\min} - V}{V_T}\right)\frac{dV(z)}{dz} \tag{23}$$

Here. $V_t = \frac{KT}{q}$

The rest part is given in Appendix Section.

Linear drain current is given as follows:

$$I_{DS,lin} = \frac{2\pi(r_2 - r_1)\mu_{eff}C_{fi}E_c}{(E_cL + V_{ds})}\left[(V_{gs} - V_{ths})^{\frac{a}{z}}V_{ds} - \frac{\theta_{short}V_{ds}^{\ 2}}{2}\right] \tag{24}$$

Where E_c is the critical field, for long-channel device $\alpha = 2$ to $\alpha = 1$ for short channel device, $\theta_{short} = \frac{0.1}{\left[\frac{d\psi_{0\min}}{dV_{gs}}\right]}$ at $V_{gs} = V_{th}$ $V_{ths} = V_{th}(1 - \theta_{short})$, short channel effects have been incorporated in the drain current by using E_c θ_{short}, V_{ths}.

Saturation current (with V_{ds} replaced by V_{dsat}) is given as follows:

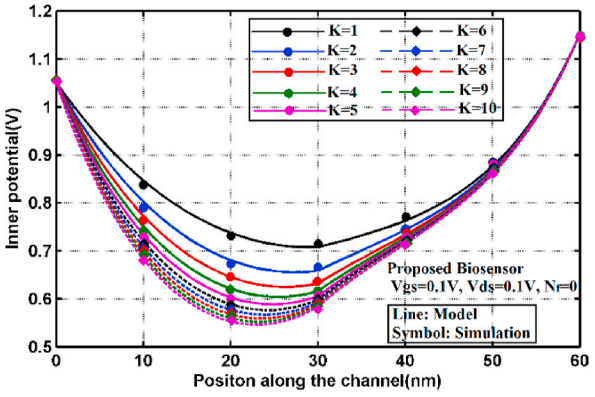


Fig. 2. Variation of Inner potential of proposed biosensor along the channel position for different neutral biomolecules and in absence of biomolecule (that is, in presence of air) in the nanogap.

$$I_{DS,sat} = \frac{2\pi(r_2 - r_1)\mu_{eff}C_{f_2}}{\left(1 + \frac{V_{dsat}}{E_c(L - L_{sat})}\right)(L - L_{sat})}\left[\beta\left(V_{gs} - V_{ths}\right)^{\frac{q}{2}}V_{dsat} - \frac{\theta_{short}V_{dsat}^{\ 2}}{2}\right] \quad (25)$$

Where $V_{dsat} = V_{gs} - V_{ths}$, β is a technology dependent empirical fitting parameter.

3.5. Results and discussions

Analytical results of this section has been verified using simulation outputs from Atlas. Several physics based model such as Drift-Diffusion model for carrier transport, CVT (Lombardi) mobility model, Shockley-Read Hall recombination for fixed lifetimes, Parallel electric field dependent FLDMOB model, Auger recombination model, Concentration dependent CONMOB model, INTERFACE statement to define the type and density of localized/fixed charges have been used to obtain the simulation outputs. Filler radius of 10 nm and outer radius of 20 nm is considered to obtain analytical and simulation results. Fig. 2 displays the graphical analysis of the effects of variation of inner potential along channel position due to different types of neutral biomolecule (and also in absence of biomolecule) in the nanogap. The work function combination of gate material is so chosen so as to confine the minimum (for every K in the nanogap) in region 1 towards the source to effectively suppress the SCEs to offer upgraded device performance. In absence of biomolecule, that is, when the nanogap is filled with air (K = 1), the inner potential minimum is highest with source-channel barrier height being minimum among all the other cases. This imply that the case with air in nanogap will reflect lowest threshold voltage. With gradual increase in K-value in the nanogap, the source-channel barrier height gradually increases which will increase the threshold voltage thereby providing a metric to detect the type of biomolecule used. Also, as the K-value increases, the effective oxide thickness decreases which, in turn, increases the gate control over the channel leading to weakening SCEs for high-K neutral biomolecules. Fig. 3 exhibits analytical graphical portrayal of inner potential variation along channel position for charged biomolecules with K = 5. As the charge of the biomolecule is more and more positive, the inner potential minimum value increases causing a decrease in source-channel barrier height which, in turn, will decrease the threshold voltage. Again, as the charge becomes more and more negative, source-channel barrier height increases thereby increasing the threshold voltage. This change in threshold voltage acts as a metric to detect type of charged biomolecule. As per the expression $V_{fb_1}{}' = V_{fb_1} - \frac{qN_f}{C_{f_1}}$, presence of positive/negative charges modify the flat-band voltage that in turn impacts the threshold voltage.

Fig. 4 displays the variation of threshold voltage for different neutral biomolecules and for two different outer radius and two different nanogap heights. Firstly, for lower outer radius of 20 nm, threshold voltage is higher compared to the case for higher outer radius of 25 nm. For the case with outer radius 20 nm, channel thickness decreases thereby increasing the gate control over the channel. Thus, threshold voltage is higher which results in lower leakages and diminished power dissipation. Now, for both the cases of outer radius 20 nm and 25 nm, as the nanogap height increases, threshold voltage is found to reduce owing to reduced gate control. Finally, with increase in K-value of the neutral biomolecules, threshold voltage also increases as a direct effect of elevated source-channel barrier with increased K as also observed from Fig. 2.

Fig. 5 presents graphical analysis of threshold voltage variation for different charged biomolecules for two different outer radius and two different nanogap heights. For a lower outer radius, the channel thickness decreases thereby enhancing gate control and increased threshold voltage. Thus, device offers lower leakages. Threshold voltage decreases with increased nanogap height owing to reduced gate control. Finally threshold voltage is higher for negatively charged biomolecules due to increased source-channel barrier height. For more positively charged biomolecules, threshold voltage gradually lessens due to reduced source-channel barrier height as

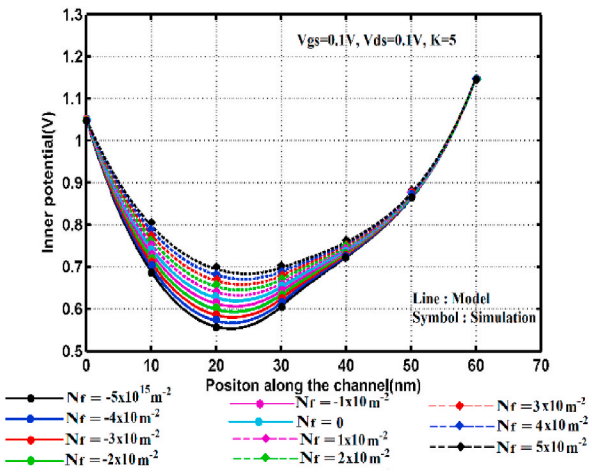


Fig. 3. Variation of Inner potential of proposed biosensor along the channel position for different charged biomolecules and in absence of charged biomolecule in the nanogap.

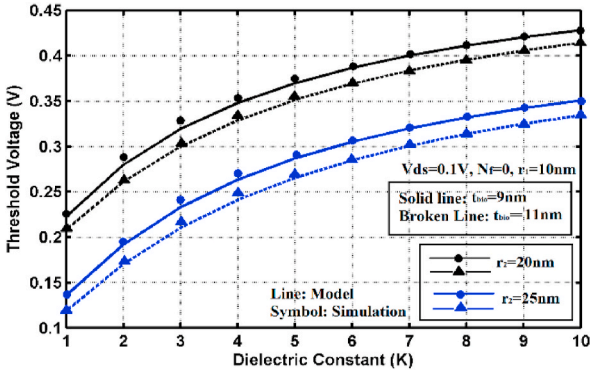


Fig. 4. Variation of threshold voltage for different neutral biomolecules for two different values of outer radius (filler radius fixed at 10 nm) and two different nanogap heights.

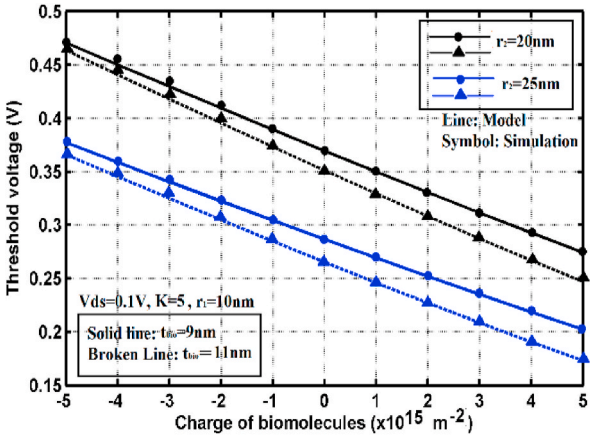


Fig. 5. Variation of threshold voltage vs. charge of biomolecules for two different values of outer radius keeping (filler radius fixed at 10 nm) and two different nanogap heights.

observed in Fig. 3. Thus, suitable selection of outer radius can effectively boost device performance.

Fig. 6 exhibits graphical analysis of Sensitivity of neutral biomolecules of proposed biosensor and its DM Full-channel Cylindrical counterpart with same channel thickness. The main reason of selecting a Macaroni channel configured MOSFET over Full-channel cylindrical one (having identical device parameters and biasing conditions) lies in the fact that the proposed biosensor shows higher sensitivity (for a fixed K-value) compared to the cylindrical counterpart, thus implying that the proposed biosensor offers superior sensing compared to its full-channel cylindrical counterpart. Also with increase in K-value of neutral biomolecules, sensitivity

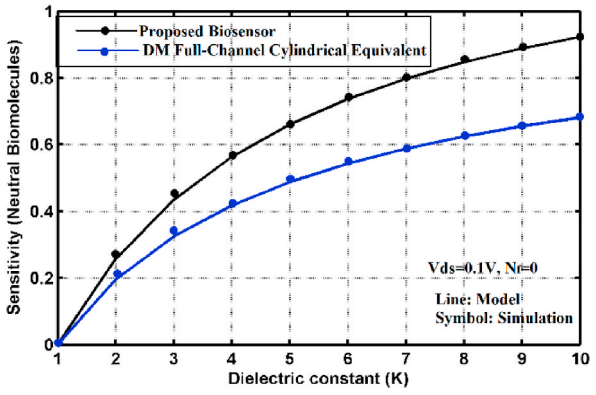


Fig. 6. Variation of threshold voltage vs. K-value of neutral biomolecules for proposed biosensor and its DM Full-channel Cylindrical Equivalent.

highly increases hence revealing the fact that both biosensors are more sensitive for high-k biomolecules, with the proposed biosensor showing higher values of sensitivity.

The sensitivity analysis of the biosensor for charged biomolecules is presented in Fig. 7. The analysis is conducted for the proposed biosensor and its DM Full-channel Cylindrical Equivalent with same channel thickness. The proposed biosensor offers higher sensitivity compared to its Cylindrical equivalent which makes Macaroni configuration, a better choice for biosensor over conventional cylindrical biosensors. For both biosensors, as the charge of biomolecules increases more and more, the sensitivity values increase. Both the biosensors are found to be slightly more sensitive to negatively charged biomolecules compared to the positive ones. Through Subthreshold Swing variation displayed in Fig. 8, it is observed, that for outer radius 25 nm (with HfO_2/SiO_2 gate stack in Region 2), Subthreshold swing is highest which intimidates the achievement of superior device performance. Configuration with Outer radius of 20 nm offers better subthreshold swing response with HfO_2/SiO_2 gate stack in Region 2, however, significant increase in subthreshold swing is noted when HfO_2/SiO_2 gate stack in region 2 is replaced by only SiO_2. Hence, the gate stack configuration of HfO_2/SiO_2 in region 2 helps to achieve better subthreshold characteristics enabling improved performance of the biosensor. Drain current analysis vs. gate voltage for the proposed biosensor for different neutral biomolecules in the nanogap (and also in absence of any biomolecule, $K = 1$) is shown in Fig. 9. The Off-state current is found to considerably change for different types of biomolecule, however, no change is observed in final On-current.

For the case, $K = 1$, threshold voltage is lowest as observed from Fig. 2, hence the off-state current largely increases. As the K-value elevates, threshold voltage largely increases leading to lower off-state current. Shifts in threshold voltage also causes shifts in off-state currents as observed in Fig. 9. Fig. 10 exhibits shift in off-state current for charged biomolecules while the final On-state current remains unaltered. As the biomolecule is more and more positively charged, the threshold voltage largely reduces which increases the off-state drain current compared to the case with neutral biomolecule in the nanogap. Also, as the biomolecule is more and more negatively charged, threshold voltage largely enhances which reduces the off-state current in the device. Shifts in threshold voltage shifts the off-state current as evident from Fig. 10. Analytical and simulation results match well hence validating our proposed biosensor's superior performance.

4. Conclusion

Current research exploration highlights the performance of a Macaroni channel Dual-Material Gate MOSFET as a biosensor for detection of neutral as well as charged biomolecule. Shifts in device features such as inner potential, threshold voltage, drain current are noted as a result of presence of neutral/charged biomolecules in the nanogap. A shift in threshold voltage is explored as a metric to sense the type of biomolecule present in the nanogap and to realize the sensitivity performance of the proposed biosensor. Device features largely depend on the outer radius selection and various short channel effects can be effectively suppressed with suitable outer radius selection. Comparative threshold voltage shift based sensitivity analysis reveals that the proposed biosensor offers superior sensitivity performance as compared to its DM Full-channel Cylindrical Equivalent with same channel thickness. Analytical results are in good agreement with simulated results entailing advanced, prospective applications of the recommended biosensor in future specimen identifying applications.

Declaration

Funding and acknowledgement

Pritha Banerjee as the Principal Investigator and a DST Woman Scientist thankfully acknowledges the financial support obtained from Department of Science and Technology (DST), Ministry of Science and Technology, Government of India, to carry out this research work under Women Scientist scheme (WOS-A) vide File No. SR/WOSA/PM-82/2018.

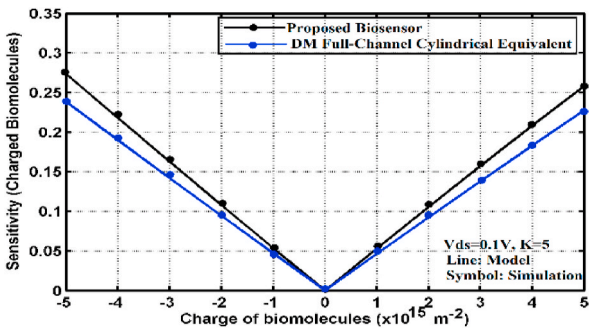


Fig. 7. Variation of Sensitivity vs. charge of biomolecules for proposed biosensor and its DM Full-channel Cylindrical Equivalent.

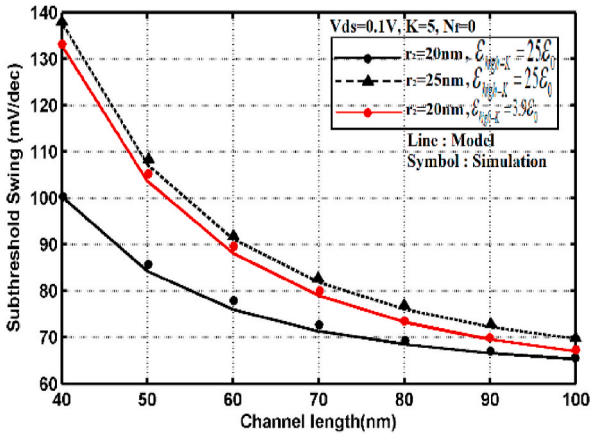


Fig. 8. Variation of Subthreshold swing vs. different channel lengths for two different values of outer radius keeping filler radius fixed at 10 nm and for two different gate oxide-stack configuration in region 2.

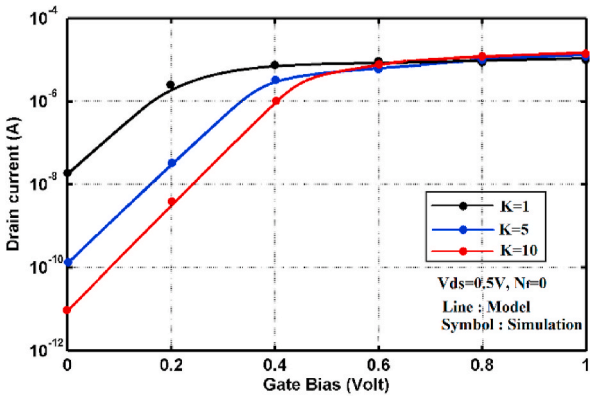


Fig. 9. Drain Current vs. Gate voltage for proposed biosensor for neutral biomolecules in the nanogap.

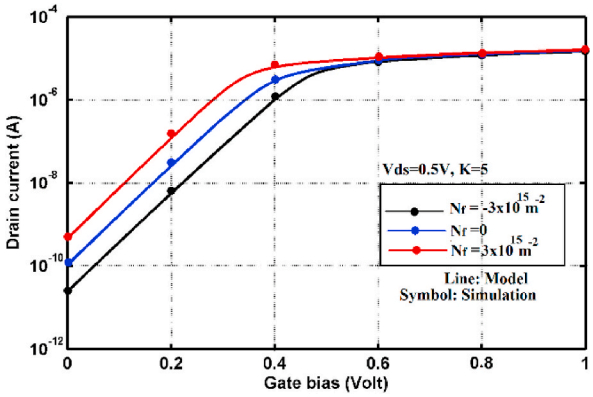


Fig. 10. Drain Current vs. Gate voltage for proposed biosensor for charged biomolecules in the nanogap.

Conflicts of interest/Competing interests

The authors declare that there is no Conflicts of interest/Competing interests.

Consent for publication

The authors declare their consent for publication upon acceptance of paper.

Ethics declarations

The authors declare that all procedures followed were in accordance with the ethical standards.

Authors' contributions

All the authors have significant contributions and have given final approval of this version to be published.

Declaration of competing interest

The authors of the manuscript entitled "Analytical Exploration and Simulation of Dual-Material Gate Macaroni Channel MOSFET Biosensor using Dielectric-Modulation Technique" declare that they have no conflict of interest.

Appendix. Inner potential modeling (contd.)

The coefficients M_1, N_1, M_2, N_2 in equations (9) and (10) are listed as follows:

$$M_1 = \alpha_1 + \beta_1 V_{gs} \tag{A.i}$$

$$N_1 = \alpha_2 + \beta_2 V_{gs} \tag{A.ii}$$

$$M_2 = \left(\frac{x_1}{2}\right) M_1 \exp(L_1 / \lambda_1) + \left(\frac{y_1}{2}\right) N_1 \exp(-L_1 / \lambda_1) + \frac{S_{12}}{2} \tag{A.iii}$$

$$N_2 = \left(\frac{y_1}{2}\right) M_1 \exp(L_1 / \lambda_1) + \left(\frac{x_1}{2}\right) N_1 \exp(-L_1 / \lambda_1) + \frac{S_{12}}{2} \tag{A.iv}$$

Where, $\alpha_2 = \left[\frac{V_{bi}(g_1-2)-2V_{ds}+2S_{12}\cosh(L_2/\lambda_2)-2F_2+g_1F_1}{g_1-F_1}\right]$, here, $g_1 = x_1 \exp(p_1) + y_1 \exp(q_1), h_1 = x_1 \exp(-p_1) + y_1 \exp(-q_1)\, x_1 = 1 + \frac{\lambda_2}{\lambda_1}, y_1 = 1 - \frac{\lambda_2}{\lambda_1}$,

$$p_1 = \frac{L_1}{\lambda_1} + \frac{L_2}{\lambda_2}, q_1 = \frac{L_1}{\lambda_1} - \frac{L_2}{\lambda_2}, S_{12} = \varphi_{01} - \varphi_{02}, F_1 = {V_{fb_1}}' + \frac{qN_a{\lambda_1}^2}{\varepsilon_{Si}}, F_2 = {V_{fb_2}}' + \frac{qN_a{\lambda_2}^2}{\varepsilon_{Si}},$$

$$\beta_2 = \frac{2-g_1}{g_1-h_1},\ \alpha_1 = V_{bi} + F_1 - \alpha_2,\ \beta_1 = -1 - \beta_2,$$

Threshold voltage modeling (Contd.)

a, b and c expressions from equation (16) are listed as follows:

$$a = 4\beta_1\beta_2 - 1 \tag{A.v}$$

$$b = 2[2(\alpha_1\beta_2 + \alpha_2\beta_1) + f_1] \tag{A.vi}$$

$$c = 4\alpha_1\alpha_2 - {f_1}^2 \tag{A.vii}$$

Where. $f_1 = 2\varphi_f + F_1$

Subthreshold drain current modeling (Contd.)

Substituting eq. (23) in eq. (22), the equation thus obtained is as follows:

$$I_{DS}\int_0^L dz(z) = \frac{\mu_{eff}}{1+\theta\left(V_{gs}-V_{th}\right)}\pi\left(r_2{}^2 - r_1{}^2\right)qn_i(T)\int_0^{V_{ds}} \exp\left(\frac{\psi_{01\min}-V}{V_T}\right)dV(z) \quad \text{(A.viii)}$$

The final expression for drain current of the device is:

$$I_{DS} = \frac{\mu_{eff}}{1+\theta\left(V_{gs}-V_{th}\right)}\pi\frac{\left(r_2{}^2 - r_1{}^2\right)}{L}qn_i(T)\exp\left(\frac{\psi_{01\min}}{V_T}\right)V_T[1-\exp(-V_{ds}/V_T)] \quad \text{(A.ix)}$$

Here, $\mu_{eff} = \frac{\mu_n}{\sqrt{\left(1+\frac{Na}{N_{ref}+NaS_1}\right)}}$, μ_n is the electron mobility, S_1 and θ are fitting parameters.

References

[1] Rakhi Narang Ajay, Manoj Saxena, Mridula Gupta, Modeling of gate underlap junctionless double gate MOSFET as bio-sensor, Mater. Sci. Semicond. Process. 71 (2017) 240–251, https://doi.org/10.1016/j.mssp.2017.08.008. ISSN 1369-8001.

[2] S.K. Parija, S.K. Swain, S. Adak, et al., Comparison study of DG-MOSFET with and without gate stack configuration for biosensor applications, Silicon (2021), https://doi.org/10.1007/s12633-021-01118-z.

[3] B. Cousin, M. Reyboz, O. Rozeau, M.A. Jaud, T. Ernst, J. Jomaah, A unified short channel compact model for cylindrical surrounding-gate MOSFET, Solid State Electron 56 (2011) 40–46.

[4] Sarvesh Dubey, Abirmoya Santra, Gopikrishna Saramekala, Mirgender Kumar, Pramod Kumar Tiwari, An analytical threshold voltage model for triple-material cylindrical gate-all-around (TM-CGAA) MOSFETs, IEEE Trans. Nanotechnol. 12 (NO. 5) (2013).

[5] R. Delhougne, A. Arreghini, E. Rosseel, A. Hikavyy, E. Vecchio, L. Zhang, A. Furnemont, First demonstration of monocrystalline silicon macaroni channel for 3-D NAND memory devices, IEEE Symposium on VLSI Technology (2018), https://doi.org/10.1109/vlsit.2018.8510635.

[6] G. Congedo, A. Arreghini, L. Liu, E. Capogreco, J.G. Lisoni, K. Huet, J. Van Houdt, Analysis of Performance/variability Trade-Off in Macaroni-type 3-D NAND Memory, IEEE 6th International Memory Workshop (IMW), 2014, https://doi.org/10.1109/imw.2014.6849381.

[7] Chang-Hoon Kim, Cheulhee Jung, Park Hyun Gyu, Choi Yang-Kyu, Novel dielectric-modulated field-effect transistor for label-free DNA detection, BIOCHIP JOURNAL 2 (No. 2) (2008) 127–134.

[8] Rakhi Narang Ajay, Manoj Saxena, Mridula Gupta, Investigation of dielectric modulated (DM) double gate (DG) junctionless MOSFETs for application as a biosensors, Superlattice. Microst. 85 (2015) 557–572.

[9] Kamalaksha Baral, Prince Kumar Singh, Gautam Kumar, Ashish Kumar Singh, Manas Ranjan Tripathy, Sanjay Kumar, Satyabrata Jit, "Impact of ion implantation on stacked oxide cylindrical gate junctionless accumulation mode MOSFET: an electrical and circuit level analysis, Mater. Sci. Semicond. Process. 133 (2021), 105966, https://doi.org/10.1016/j.mssp.2021.105966. ISSN 1369-8001.

[10] Muktasha Maji, Gaurav Saini, Modeling of dual material surrounding split gate junctionless transistor as biosensor, Superlattice. Microst. 135 (2019) 106–290.

[11] Quan Nguyen-Gia, Myounggon Kang, Jongwook Jeon and Hyungcheol Shin, "Characteristic length of macaroni channel MOSFET", DOI 10.1109/LED.2019.2942619, IEEE Electron. Device Lett.

[12] Ekta Goel, Sanjay Kumar, Kunal Singh, Balraj Singh, Mirgender kumar and satyabrata jit, "2-D analytical modeling of threshold voltage for graded-channel Dual-material double-gate MOSFETs, IEEE Trans. Electron. Dev. 63 (NO. 3) (2016).

[13] Quan Nguyen-Gia, Myounggon Kang, Jongwook Jeon and Hyungcheol Shin, "Models of threshold voltage and subthreshold slope for macaroni channel MOSFET", DOI 10.1109/LED.2020.2995642, IEEE Electron. Device Lett.

[14] Lining Zhang, Li Lin, He Jin, Mansun Chan, Modeling short-channel effect of elliptical gate-all-around MOSFET by effective radius, IEEE Electron. Device Lett. 32 (NO. 9) (2011).

[15] H. Ghanatian, S.E. Hosseini, Analytical modeling of subthreshold swing in undoped trigate SOI MOSFETs, J. Comput. Electron. 15 (2) (2016) 508–515. Mar. 2016.

[16] Pritha Banerjee, Jayoti Das, Gate work function engineered trigate MOSFET with a dual-material bottom gate for biosensing applications: a dielectric-modulation based approach, Silicon 14 (2020) 1–10, https://doi.org/10.1007/s12633-020-00823-5. November.

[17] S. Rewari, V. Nath, S. Haldar, S.S. Deswal, R.S. Gupta, Gate induced drain leakage reduction in cylindrical dual-metal hetero-dielectric gate all around MOSFET, IEEE Trans. Electron. Dev. 65 (2018) 3.

[18] A. Pal, A. Sarkar, Analytical study of dual material surrounding gate MOSFET to suppress short-channel effects (SCEs), Int. J. Eng. Sci. Technol. 17 (2014) 205.

[19] N. Singh, A. Agarwal, L.K. Bera, T.Y. Liow, R. Yang, S.C. Rustagi, D.L. Kwong, High-performance fully depleted silicon nanowire (diameter_5 nm) gate all-around CMOS devices, IEEE Electron. Device Lett. 27 (2006) 383–386.