Design and Development of Improved Topologies for Microgrid Connected Bidirectional Converter with Energy Storage

Thesis submitted by

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I. JOURNAL PUBLICATIONS:

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[J2] **S. B. Santra**, D. Chatterjee, and T. J (Peter). Liang, "High Gain and High Efficiency Bidirectional DC-DC Converter with Current Sharing Characteristics Using Coupled Inductor", **IEEE Transactions on Power Electronics**, Vol. 36, no. 11, pp. 12819-12833, Nov. 2021.

[J3] **S. B. Santra**, A. Roy, T. R. Choudhury, D. Chatterjee and B. Nayak, "Performance Improvement of DC-DC Converter using L-D based modified GaN-FET driver", **International Journal of Circuit Theory and Applications**, Vol. 48, no. 6, pp. 860-873, April. 2020.

[J4] **S. B. Santra**, M. Ramana and D. Chatterjee, "Performance Analysis of Novel Bidirectional DC-DC Converter with LD based Modified GaN-FET Driver", **IEEE Transactions on Industry Applications**, Vol. 57, no. 5, pp. 5199-5214, Sept.-Oct. 2021.

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[J6] **S. B. Santra**, D. Chatterjee, K. Kumar, M. Bertoluzzo, A. Sangwongwanich and F. Blaabjerg, "Capacitor selection Method in PV Interfaced Converter Suitable for Maximum Power Point Tracking", **IEEE Journal of Emerging and Selected Topics in Power Electronics**, Vol. 9. No. 2, pp. 2136-2146, April 2021.

II. CONFERENCE PUBLICATIONS:

[C1] **S. B. Santra**, K. Bhattacharya, T. R. Choudhury and D. Chatterjee, "Generation of PWM Schemes for Power Electronic Converters", **Proceedings of 2018 20th National Power System Conference (NPSC)**, NIT Tiruchirappalli, India, 2018.

[C2] **S. B. Santra**, D. Chatterjee, S. Banerjee, K. Kumar and M. Bertoluzzo, "Selection of capacitor in PV system for Maximum Power Point Tracking**, Proceedings of 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)**, IIT Madras, India, 2018.

[C3] **S. B. Santra**, A. Roy and D. Chatterjee, "Design of Bootstrap Capacitor Based GaN-FET Driver for Improvement in Transient Performance of DC-DC Converter", **Proceedings of 2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE 2020)**, Cochin, India, 2020.

Statement of Originality

I **Subhendu Bikash Santra** registered on **12. 06. 2019** do hereby declare that this thesis entitled "**Design and Development of Improved Topologies for Microgrid Connected Bidirectional Converter with Energy Storage**" contains literature survey and original research work done by the undersigned candidate as a part of Doctoral studies.

All information in this thesis have been obtained and presented in accordance with existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I have fully cited and referred all materials and results that are not original to this work.

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Date

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Certificate from the Supervisor

This is to certify that the thesis entitled "**Design and Development of Improved Topologies for Microgrid Connected Bidirectional Converter with Energy Storage",** submitted by Sri Subhendu Bikash Santra, who got his name registered on 12th June 2019, for the award of Ph. D. (Engg.) degree of Jadavpur University, is absolutely based upon his own work under the supervision of Prof. (Dr.) Debashis Chatterjee and that neither his thesis nor any part of the thesis has been submitted for any degree/diploma or any other academic award anywhere before.

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Signature of the supervisor with date & seal

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Dedicated to

--Maa Saraswati and Lord Krishna

"*Ghora Roope Maharave, Sarva Shathru Bhayankari,*
Bhaktebhyo Varade Devi Thrahi Maam Saranagatam.
Om Surasurarchithe Devi, Sidha Gandharva Sevite,
Jadya Papa Hare Devi, Trahi Maam Saranagatam."

Preface

Fossil fuel is the primary source of energy in power generating units of thermal power plant. More such units to meet increased load demand is harmful for the environment because of its induced effect on pollution and global warming. In last decade, there is a major shift towards generating green power using renewable energy sources across globe as per different SDGs of UN. Photovoltaic (PV) and wind turbine-based power generation hold majority of percentage of renewable energy adaptation. However, intermittent nature of PV, wind power which depends sun irradiation and wind speed respectively makes the power extraction from these sources difficult. Storage units are essential for these systems especially with PV. Storage units are of low voltage and high current type. Series connection of multi storage units are not possible due to charge imbalance problem. Generally, storage units (low-cost lead acid battery) are of 24V-48V DC system. PV panel also inherently generate low DC voltage which can't be converted to single phase RMS 230V AC voltage. Thus, high gain single stage boost converter is essential which can increase PV panel voltage to 300V-380V DC voltage so that by using inverter single phase line voltage 230V RMS can be generated. The similar system is required for three phase AC system. Therefore, storage unit should be interfaced to 300V-380V constant DC link voltage. The storage unit can maintain the intermittent nature of PV generated power. The interfacing converter between storage and common DC link voltage should have sufficient voltage gain and capability to flow power in both ways i.e., from battery to DC link or vice versa. Thus, single stage high gain bidirectional DC-DC converter is essential to interface low voltage storage to 300V-380V DC common link. The same circuit is also useful in EV to supply momentary power from ultracapacitor during acceleration and can store during deceleration. In this thesis a single switch generalized high voltage gain non-isolated boost converter using coupled inductor is proposed which has less switch current and voltage stress. The converter also offers high operating efficiency. The proposed circuit solves the common problem of excessive high switch current stress in high voltage gain non-isolated boost converters. The boost circuit is then modified to have buck stage in the same circuit to derive a novel non-isolated bidirectional DC-DC converter (BDC). The proposed BDC has high voltage gain/conversion factors in both direction of power flow. Single coupled inductor turn is used while developing the power circuit. The proposed BDC has inherent soft switching i.e., zero voltage switching turn ON feature

which further reduce the converter loss. Therefore, proposed circuit has high efficiency of operation >94% for both mode of operation. The efficiency improvement of proposed BDC can be further enhanced by 1-1.5% margin by replacing MOSFET to GaN-FET. The testing of GaN-FET based BDC using reliable gate driver is also tested in this current work. Another common problem of BDC while interfacing with storage is large ripple current. This ripple current can be filtered by using large filter capacitor at low voltage side. But this makes system bulky and any fault in the capacitor degrade battery life as battery has to supply the ripple current. Thus, modification in the BDC circuit topologies is essential to achieve less ripple current (ideally zero) especially at low voltage without any filter. In this work a new coupled inductor based non-isolated BDC circuit is proposed which has flat input ripple current of very low magnitude at LV side for wide variation of duty ratio. This circuit can also replace the necessity of interleaved structure of high voltage gain BDC circuit for interfacing storage. The proposed circuit has less component usage and inherent soft switching (ZVS turn ON) of all active switches which enhances operating efficiency. This proposed circuit is a good alternative of interleaved non-isolated BDC for achieving low ripple current, high efficiency and voltage gain.

The application of BDC converter connected to microgrid is very important. BDC should operate instantaneously during any power mismatch between sources to load. The mismatch problem is critical when source is PV panel due to its intermittent power generation. Therefore, for maintaining constant DC link voltage is necessary for stable microgrid operation and it is a major challenge. The BDC should operate instantaneously but power converter cannot alone make the system fast and reliable. The system components are also source of delay during transition event. The large delay make system unstable even though BDC's are highly efficient and fast acting. Thus, proper selection of system components especially passive components like capacitor, inductor is very critical. In this work the passive components selection procedure for BDC connected microgrid is discussed.

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Contents

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[2] T. R. Choudhury, B. Nayak and **S. B. Santra**, "A Novel Switch Current Stress Reduction Technique for Single Switch Boost-Flyback Integrated High Step Up DC–DC Converter," in ***IEEE Transactions on Industrial Electronics***, vol. 66, no. 9, pp. 6876-6886, Sept. 2019.

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List of Symbols and Abbreviations

Symbols

$V_1, V_2, ...V_n$	Voltages
θ	Phase angle of AC voltage
φ	Phase angle difference
$L_{Leakage}$	Leakage inductance
n	Turns ratio
V_{LV}	Low voltage
V_{HV}	High Voltage
i_{Lk}	Leakage Current
$S_1, S_2,....S_n$	Active Switches
$.i_1, i_2, ...i_n$	Loop currents
ΔQ	Change of charge
T_s	Switching time
$.t_1, t_2,...t_n$	timings
D	Duty Ratio
$D_1, D_2, \ D_n$	Diodes
I_o	Load Current
M	Voltage Gain
R_L	Load Resistance
.fsw.	Switching frequency
$C_1, C_2, \ C_n.$	Capacitors
$L_1, L_2, \ L_n$	Inductor
Lm	Magnetizing inductance
Lin	Input inductor
N_1/N_p	Primary winding turns
N_2/Ns	Secondary winding turns
N_3/NT	Tertiary winding turns
M	Mutual inductance
$\Delta i_L.$	Inductor current ripple
dT_s/DT_S	switching ON time.
$\omega_{r.}$	Resonant Frequency

$.i_{switchpeak}$	Peak switch current
$.t_r$	Half cycle resonating current
V_{in}	input voltage
$I_{in.}$	Input current
$I_{m.}$	Magnetising current
I_{sec}	Secondary winding current
I_{pri}	primary winding current
V_{c1}, V_{c2}, V_{cn}	Capacitor voltages
$\zeta_{Lm.}$	Normalized time constant
r_{switch}	switch resistance
$r_{d.}$	Diode resistance
$.r_{sec.}$	Secondary resistance
V_{sw}	Switch voltage stress
C_{eq}	Equivalent capacitor
Δi_{Lm}	Magnetizing ripple current
V_{GS}	Gate to source voltage
V_{GSTH}	Threshold voltage
Z_{pull_down}	Gate drive loop impedance
C_{gd}	Capacitance between gate to drain
C_{boot}	Bootstrap capacitance
R_{boot}	Damping bootstrap resistance
$R_{SR/CS}$	Series path resistance of gate path
L_b	Series gate inductance
M_{CCM}	Voltage gain in continuous conduction mode
C_f	PV panel connected capacitance
P_{input}	Input power
P_{output}	Output power
Z_{in}	Input impedance looking from output ports
Q_2	Switch
V_{sense}	Senseed PV voltage
I_{sense}	Sensed PV output current
$\Delta T_{Control}$	Sensing and processing delay

ΔT_G	Irradiation change
V_{cf}	PV capacitor voltage
ΔG	Irradiation change
P_k	Reference power
P_{ka}	Actual power
ΔT_{PV}	PV panel time constant
V_t	Thermal voltage
R_{se}	Series resistance
R_{sh}	Shunt resistance
I_{ph}	PV generated current
ω.	Grid angular frequency

Abbreviations

BDC	Bidirectional DC-DC Converter
PV	Photovoltaic panel
RES	Renewable energy sources
LVDC	Low voltage DC Microgrid
DAB	Dual active bridge
RCD	Resistive capacitive snubber circuit
ZVS	Zero voltage switching
RMS	Root mean square
SEPIC	Single ended primary inductor converter
LV and HV	Low voltage and High voltage side
EV	Electric vehicle
CIBDC	Coupled inductor based bidirectional DC-DC converter
MOSFET	Metal oxide field effect transistor
GaN-FET	Gallium nitride field effect transistor
FPGA	Field programmable gate array
PWM	Pulse width modulation
RIRC	Reduced input ripple current
MPPT	Maximum power point tracking
PEC	Power electronic converter

***Abbreviations/Symbols appearing in this thesis other than the mentioned ones are defined in the respective contexts.**

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Chapter-1

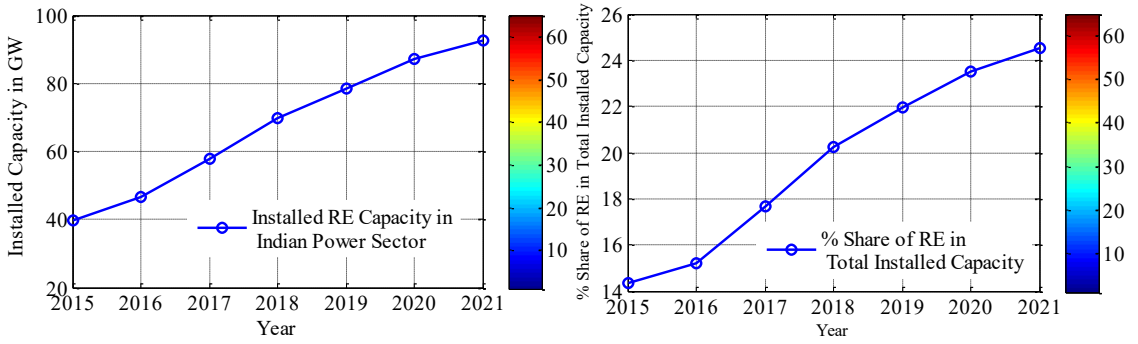
Introduction

Motivation, necessity and applications of the current work is discussed in this chapter. Microgrid and EV system arrangement with requirements of bidirectional DC-DC converter is highlighted. Specifications with required standards for the application area is also mentioned in this chapter. The objective and research questions to be addressed in this work are mentioned. Finally outline of the thesis work is mentioned in this chapter.

1. Introduction

1.1. Introduction

Environmental concerns like increased global warming, pollution and limited capacity of fossil fuel encouraged the scientific community throughout the globe to find alternative solutions to meet the energy demand. United Nations has designed seventeen sustainable developmental goals (SDGs) are designed to meet the prolonged sustainable growth. Renewable energy resources (RES) like photovoltaic (PV) panel, wind turbine-based power plant [1] are the best possible solutions for energy sustainability. Over the last decade, India is also aggressively investing on renewable power generation based on Paris agreement. There is a national goal to install renewable power generation capacity of 40% cumulatively by 2030 out of 100 GW should be installed by the end of 2022. Cumulative 92.54 GW RES is installed by the end of Jan 2021. By the last seven years the installed capacity of RES has increased by 66% where capacity of PV energy is increased to 15 times [2]. The increment of using RES in India is shown in Fig. 1.1 (a) and Fig. 1.1 (b).



(a) (b)

Fig. 1.1. RES capacity in India (a) Installed capacity in GW (b) Share (%) of RES in total installed capacity.

There are many ON grid and OFF grid PV power projects like community hall microgrid, government offices, schools and multi-farming cooperative society microgrid are currently under installation stage in India where storage is an integral part which requires power electronics interface circuit at different voltage levels. Intermittent behaviour of PV power sources requires a storage unit where there is a need of bidirectional DC-DC converter [3] for charging and discharging the storage unit based on availability of PV power and load requirements. Similarly, to reduce direct pollution there has been a tremendous emphasis given on the usage of electric vehicle (EV) in India. The great ambition of Govt. of India is to make compulsory 100% usage of EV by the end of 2030

[2]. In the EV also, there is a requirement of storage and bidirectional DC-DC converter (BDC) for storing or dissipating energy based on acceleration and decelaration [4].

1.1.1. Microgrid Structure and Voltage Levels

Microgrid is a cluster of connected loads along with renewable energy resources defined through a clear boundary, can work independently or in grid connected mode. The microgrid is connected locally to the consumer or distribution side making power flow in either top to bottom or bottom to top which is a major feature of future smart grid where consumer can contribute to the power generation [5]. The microgrid can be of DC, AC or hybrid architecture [6] based on RES i.e. PV and wind system which is shown in Fig. 1.2.

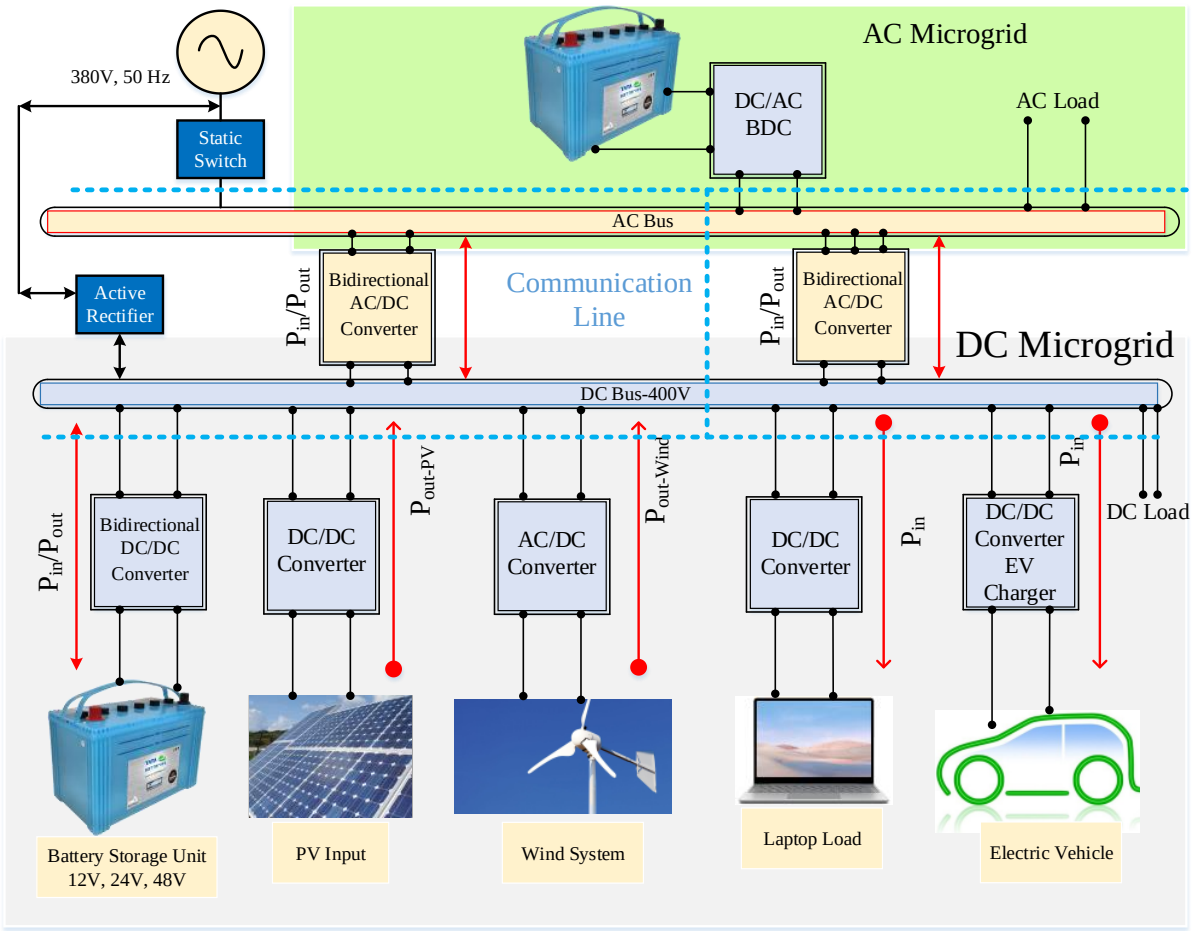


Fig. 1.2. General architecture of AC , DC and hybrid microgrid.

In DC microgrid, all the RES generations are converted to common DC link voltage using DC/DC converter for PV systems and AC/DC converter for permanent magnet synchronous generator (PMSG) based wind system [1]. In DC microgrid different common DC link voltages exists, such as 12V-48V for extra low voltage DC microgrid (ELVDC) and 380V-400V for low voltage DC microgrid (LVDC) [7]. Energy storage is an integral part of DC or AC microgrid where unavailability of power from RES is

supported by the storage units. Similarly, for AC microgrid the common bus voltage is AC where voltage level is generally of 380V to 400V. In AC microgrid, unlike DC microgrid, PV interfaced converter is DC/AC type and for PMSG it is AC-DC-AC type. For storage interfacing DC/AC converter is required for AC microgrid whereas for DC microgrid DC/DC converter is essential. DC loads can be directly connected to DC microgrid through interfacing DC/DC converter. Electric vehicle (EV) charging can be achieved from DC microgrid where necessary common DC link voltage is above 400V.

1.1.2. Storage Unit for Microgrid

Integration of RES in microgrid creates intermittency in power generation which is uncontrolled and dependent on environmental conditions unlike conventional alternator-based generator system. Therefore, storage unit is an integral part of the microgrid system [8] to maintain continuity of power supply. There are different storage technologies exist using electrical, mechanical or electrochemical methods as shown in Fig. 1.3, which are still in development for future applications. Out of these, lead acid battery and flywheel are low cost solutions [9]. However, these energy storage systems have different dynamic response time as well as space requirements. The faster response time of storage units is essential to maintain voltage stability in DC microgrid and frequency stability [10] in AC microgrid.

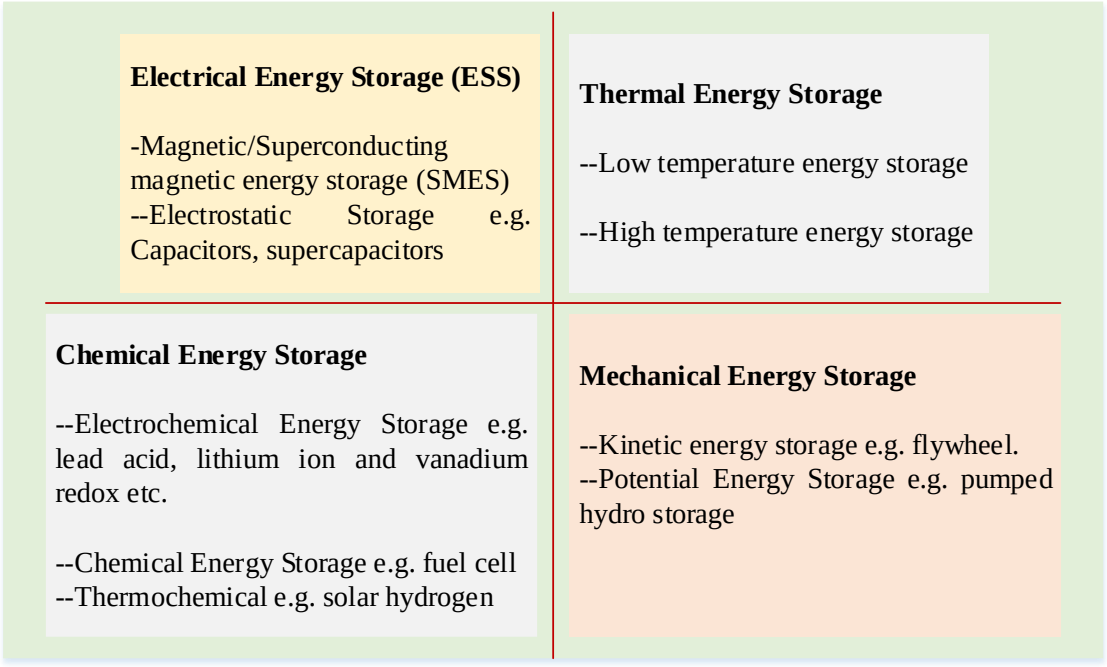


Fig. 1.3. Different energy storage techniques.

These storage unit possess important electrical characteristics i.e. peak current, ripple current, minimum state of charge (SoC), terminal voltage regulation etc. which are

essential for interfacing and designing bidirectional DC-DC converter. The important electrical characteristics of storage systems [11] are shown in Table -1.1

Table-1.1

Response time and characteristics of storage elements

Storage Technologies	Discharging/ Charging rate (MW)	Discharging Duration	Dynamics	
			Response Time	Ramp rate
Battery Energy Storage [BES]	0-40	ms.-hrs.	ms.	MW/Sec
Capacitor [Supercapacitor]	0.0099-0.049	ms.-1 hr.	ms.	MW/Sec
Flywheel Energy Storage [FES]	0.0009-0.26	ms.-15 min	Instantaneous	MW/Sec
Fuel Cell	0.001-50	Sec-24+ hr	ms.	MW/Sec

The battery energy storage response time is in the range of mili-seconds and of low voltage type. Typically, the voltage is in the range of 12V-48V. Series connected storage cell can be adopted to increase the voltage level but it has huge disadvantage of charge imbalance [11]. Therefore, series connection of storage units are not possible for practical applications. In contrary, parallel connected energy storage can provide high current at low voltage level and has no charge balance problem. Therefore, the storage unit used in microgrid is of low voltage and high current type. Lead acid battery is commonly adopted due to its low cost and moderate response time which is in the range of 20-25 ms.

1.1.3. Storage Unit for Electric Vehicle (EV)

Due to the charge imbalance problem, series connection of individual storage units are not possible even for EV application. Therefore, the storage units in EV are of low voltage and high current type. There are two types of storage units present in EV i.e. main storage unit (Li-ion battery) for motor drive train and another storage mainly used for auxiliary power supply [12]. It helps to store inertial energy during braking and provides momentary power at acceleration. These storage units are fast responsive like ultracapacitors. The storage units used for EV is shown in Fig. 1.4. Fuel cell sources are the primary energy source to drive the powertrain of EV and the voltage level is generally 48V. However, the DC link voltage for driving the inverter fed motor is 380V-400V DC. Auxiliary storage [12] units are generally of ultra-capacitor type and the voltage level

ranges from 24V-48V. Similarly, like microgrid storage, the response time of main storage unit of EV is also slower compared to ultracapacitor based auxiliary storage units.

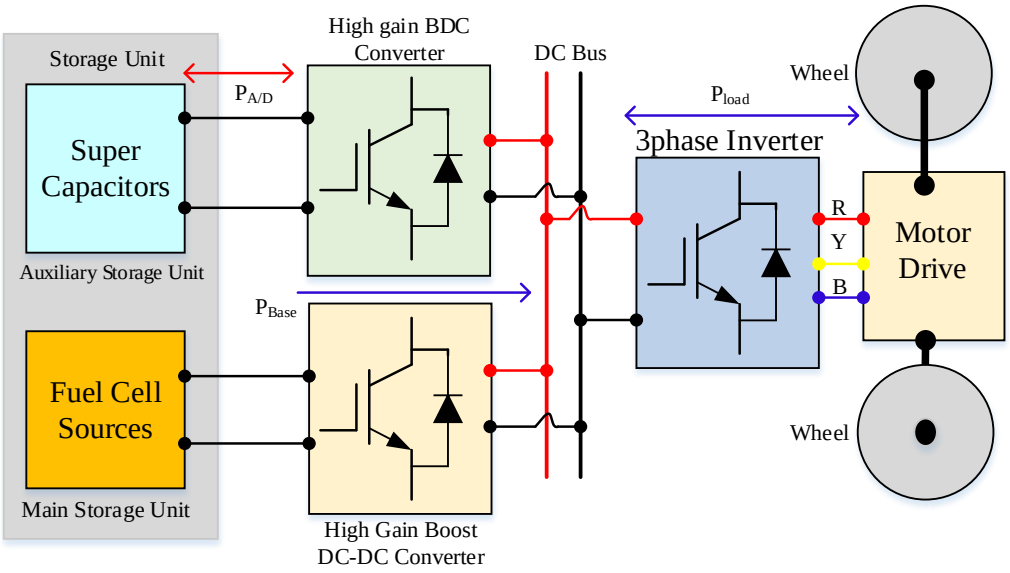


Fig. 1.4. Storage units in EV powertrain.

1.2. Storage Interface using Power Electronic Converters in Microgrid/EV

The storage units which are used for microgrid as well as for EV are of low voltage type whereas the common DC link voltage is much higher compared to source voltage. Therefore, high voltage gain and high efficiency bidirectional DC-DC power converter is necessary for interfacing low voltage source to high voltage DC bus to counter the intermittent nature of PV and wind power. The general single unit scheme of microgrid system is shown in Fig. 1.5. The important characteristics requirements of interfacing power electronics converter with storage units are discussed in the next section.

1.2.1. Characteristic Requirements of BDC

The voltage level of storage unit varies from 12V-48V. However, the common DC link voltage is 380V-400V for driving inverter fed EV [1] or converting single phase AC from DC supply. Therefore, the required power converter should be capable of converting 48V to 380V i.e. high voltage conversion factor is necessary while boosting the input voltage. Similarly, during charging time, the converter should be capable of converting 380V-400V to 48V directly using duty ratio control. Generally, voltage conversion factor >10 for boosting operation and <0.1 for buck operation at a duty ratio range 0.4 to 0.6 is essential [12] for complying gain as well as efficiency. For conventional two switch

synchronous BDC, efficiency drastically falls below 70% for both above 0.6 duty ratio during boost mode and below 0.3 duty ratio at buck mode.

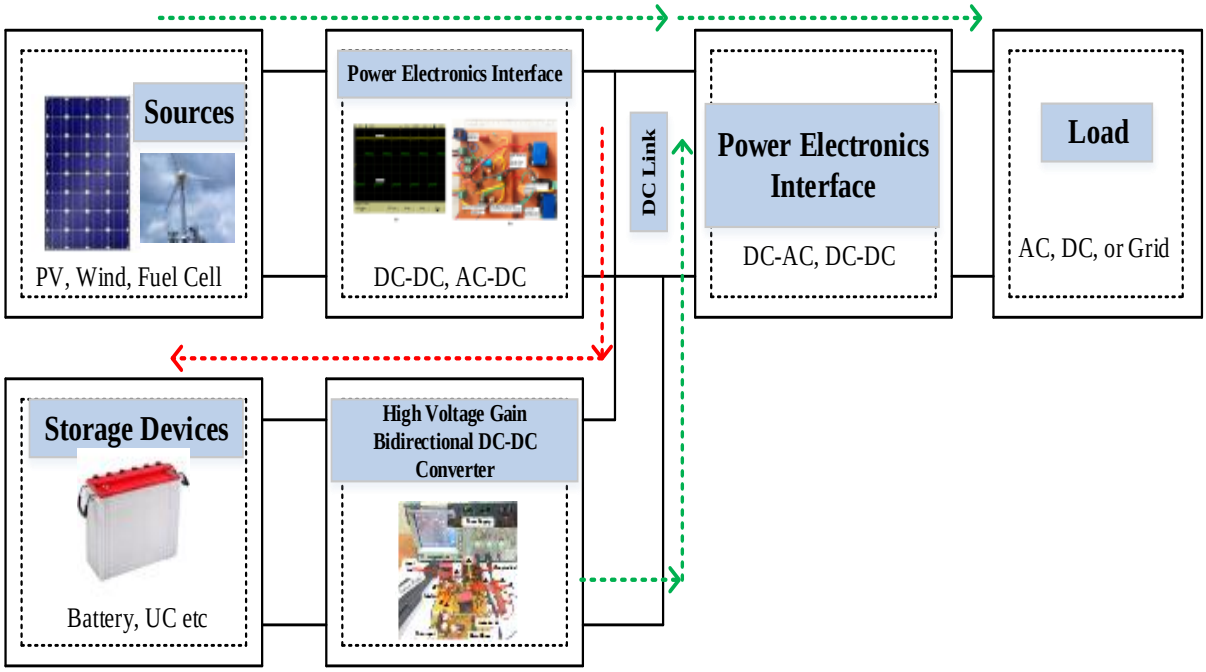


Fig. 1.5. Single unit of microgrid system and interfacing power converter.

To comply with the high gain requirements, cascading of converters are not appreciable as it degrades the overall conversion efficiency. Thus, the major characteristic requirement is to attain a single unit power converter interface capable of providing buck as well as boost operation with sufficient conversion factor and efficiency greater than 90%. The storage unit has limited peak current and ripple current providing capability. The ripple current from storage should be zero ideally so that the battery life does not degrade at a faster rate. Thus, power electronic interfacing BDC input current ripple should be very low or ideally zero. These are the system generated requirements based on the application especially in microgrid.

1.2.2 Specifications and Standards

There are several important standards available and some are currently under development stage especially for storage interface system connected to microgrid. Electromagnetic compatibility is another important parameter which should be checked before using any power electronics converter in use. The relevant standards [13] of microgrid system is shown in Table-1.2.

Table-1.2

Important standard and requirements

Standard	Importance
IEEE 1547	Voltage level and THD requirements for energy storage system connected to power grid.
VDE0126-1-1	Leakage current level for PV connected system and safety requirements.
IEC 61727	Voltage level and connection of DC and AC microgrid.
IEEE 2020.2-2015	Interoperability of battery energy storage unit with electric grid at the distribution level. It also states about the overcurrent protection, short circuit protection, undervoltage and overvoltage protection, etc.
IEEE 2020.3-2016	Testing procedure of battery energy storage unit and connected converter. Charge test, charging response time, discharging response time is also specified in this standard.
VDE-AR-N 4105	This is recently developed standard discussed about requirements of connection in LV distribution network using microgrid.
IEC 61000-4-11:2004	Short interruption and voltage variation immunity test
IEC 6100-6-3:2011	Recommendations for emission in domestic and commercial converter applications.

Similarly, the requirement of BDC converter for storage interface is mentioned in Table-1.3.

Table-1.3

Recommended Properties of Converter (BDC) [Low/Medium Power Application]

Parameter	Value
Low voltage/battery storage voltage	24V-48V
Operating frequency	f_{min}=50kHz for MOSFET and f_{min}>100kHz for GaN-FET
DC Bus voltage	380V-400V
Output Power	<1 kW
Battery ripple current	<5%
Efficiency	>95%
Voltage regulation	≤10%
Other Requirements	• Duty ratio control of bidirectional power flow. • Voltage and current control. • Connection requirement as per storage unit specifications.

1.3. Motivation

As discussed in the previous sections, it is clear that there is a requirement of bidirectional DC-DC converter (BDC) for microgrid storage interface and for EV. The dependency on power electronic converters is very essential for moving towards clean power and energy sustainability. Especially, for Indian context the converter should be of higher operating efficiency and faster response time. High power density is also an important requirement of these converters to attain better portability. This motivates to find topological solutions of bidirectional DC-DC converter for application in microgrid and EV.

1.4. Objective

As discussed earlier in the section 1.1.1 and 1.1.2, it is evident that there is a requirement of high voltage gain, high efficiency, and single unit bidirectional DC-DC converter for integrating storage unit in microgrid. Therefore, the main research interest of this work is to propose and design suitable topologies of BDC connected to microgrid. In chapter-2 an extensive review is performed in terms of topological requirements and existing problems especially with non-isolated BDC. From the detailed review of non-isolated BDC and its application requirements, the specific objectives in the form of research question (RQ) are derived as

RQ-1 *Is it possible to formulate a generalized circuit that can reduce peak current of the main switch during boost operation without sacrificing voltage conversion factor and efficiency with lesser component usage*?

RQ-2 *Is it possible to design single stage high efficiency, high gain bidirectional DC-DC converter which has current sharing characteristics at low voltage side? The circuit should be derived from generalized boost stage circuit (RQ-1) which has inherent less peak current at main switch.*

RQ-3 *Is it possible to design BDC form RQ-2 for further efficiency enhancement and achieving high power density using GaN-FET switch*?

RQ-4 *Is it possible to formulate a circuit which can replace the interleaved structure of DC-DC converter to reduce the input current ripple at low voltage side as well as improves voltage conversion factor from RQ-2 without using extra switches*?

RQ-5 *Is it possible to improve transient performance and power extraction efficiency of PV panel used in the microgrid through proper system parameter design with BDC*?

1.5. Outline of the Thesis

The current work is organized serially to comply with the objective and research questions through different chapters.

Chapter-1: Motivation, necessity and applications of the current work is discussed in this chapter. Microgrid and EV system arrangement with bidirectional DC-DC converter requirement is highlighted. Specifications with required standards for the application area is also mentioned in this chapter. Finally, the objective and research questions to be addressed in this work are mentioned.

Chapter-2: A detailed topological review of non-isolated BDC is performed in this chapter. Small discussion on isolated BDC with advantages and disadvantages are mentioned to establish the necessity of non-isolated BDC. Different circuit topologies like SEPIC, switched capacitor, switched inductor, coupled inductor and hybrid structures are discussed which helps to achieve high conversion factor. Several critical problems in designing non-isolated BDCs are also discussed in this chapter which forms a background to establish research problems and topological requirements for the application in microgrid.

Chapter-3: The main switch of non-isolated BDC at low voltage side suffers from high peak current or current stress during turn off time. The current stress is problematic as it requires high rating switch with larger heat sink. Therefore, it is also a major problem for reliable continuous circuit operation both in transient as well as steady state. This chapter discusses the current stress reduction solutions of coupled inductor based high gain BDC. A half cycle resonating branch is proposed which can successfully generalized to reduce the peak switch current as well as RMS current for designing boost stage of BDC. The proposed solution cited in this chapter helps in achieving less peak switch current without sacrificing voltage conversion factor and efficiency.

Chapter-4: The generalized boost circuit which is established in chapter-3 to achieve less current stress is adopted in this chapter to design a high efficiency, high gain BDC with current sharing characteristics at low voltage side using three winding coupled inductor. The circuit derivation, operation in continuous conduction mode (CCM) in both the operating modes, soft switching operation, voltage mode control using small signal analysis is discussed in this chapter.

Chapter-5: In this chapter gate driver of GaN-FET switch is discussed with the objective to apply GaN-FET switch in designed BDC to achieve further enhancement in operating efficiency and transient performance. In this chapter design issues of BDC with GaN-FET switch are also discussed.

Chapter-6: Low voltage side of BDC are interfaced with storage units which can't offer large ripple current. Therefore, designing BDC with zero input ripple current at low voltage side is essential. This chapter deals with circuit topology derivation to replace interleaved structure to achieve reduced low voltage side input current ripple without using extra active switch. The circuit using coupled inductor discussed in this chapter have large conversion factor with less current ripple at low voltage side.

Chapter-7: Performance improvement of BDC is not the only factor for enhancing microgrid operation. The system parameters used in the structure of microgrid is equally important for the betterment of system response. The selection of passive components which are used in microgrid where solar PV is the primary source has great importance for extracting maximum power under dynamic environmental conditions. This chapter shows the procedure to select passive components in microgrid structure for enhancing power extraction efficiency and dynamic performance.

Chapter-8: This chapter concludes the research findings and proposes the scope of future work in the relevant area.

The work flow of the current thesis including the outcome as journal and conference paper is shown in Fig. 1.6.

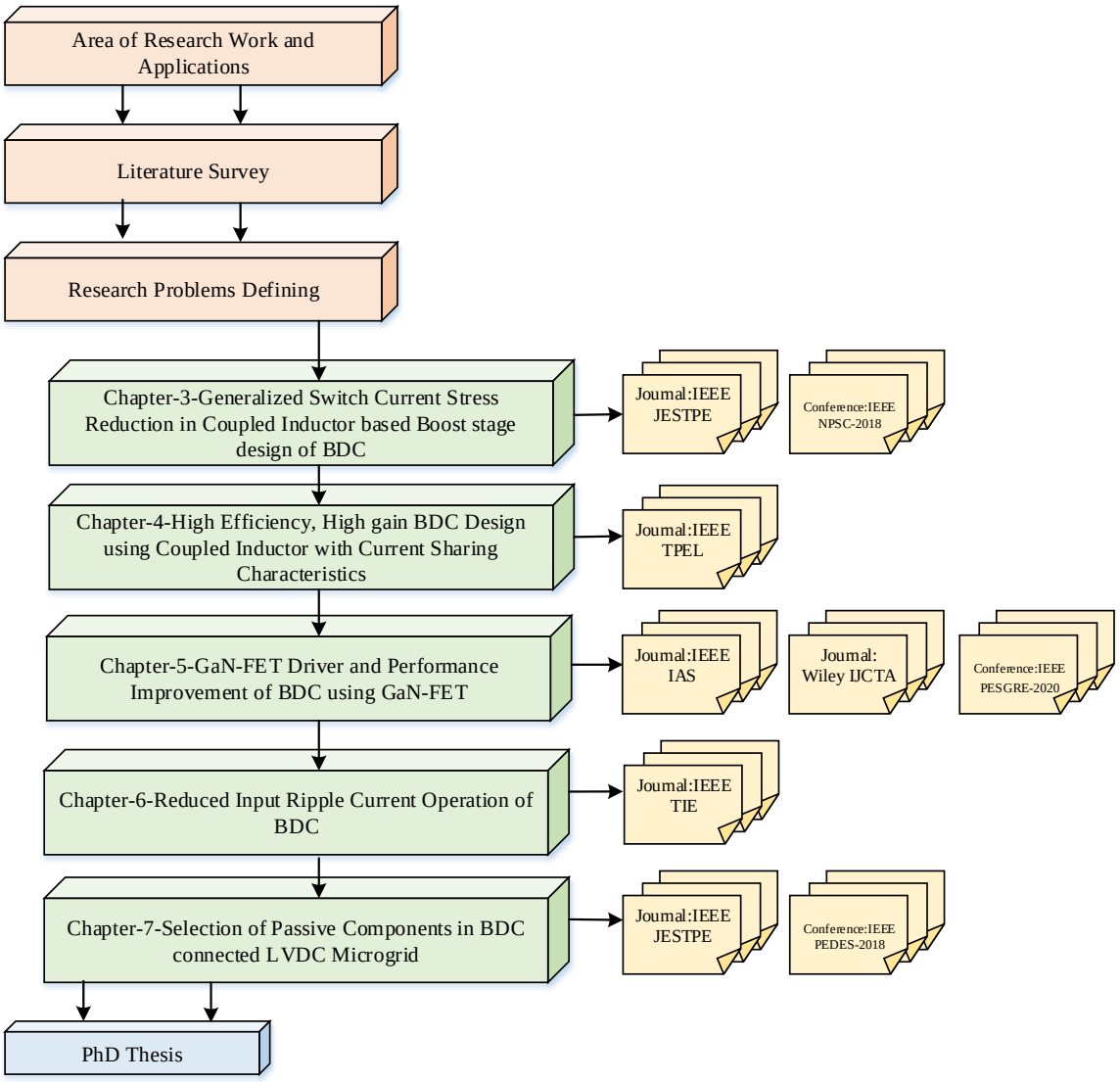


Fig. 1.6. Thesis work flow and overview.

1.6. References:

[1] Teodorescu, R., Liserre, M. and Rodriguez, “Grid converters for photovoltaic and wind power systems”, John Wiley & Sons, Feb-2011.

[2] “Annual technical Report”, Ministry of New and Renewable Energy, Government of India, 2020-21.

[3] F. A. Silva, "Modern Electric, Hybrid Electric, and Fuel Cell Vehicles, Third Edition [Book News]," in *IEEE Industrial Electronics Magazine*, vol. 12, no. 4, pp. 46-48, Dec. 2018, doi: 10.1109/MIE.2018.2874371.

[4] A. Wangsupphaphol and N. R. N. Idris, "Acceleration-based design of electric vehicle auxiliary energy source," in *IEEE Aerospace and Electronic Systems Magazine*, vol. 31, no. 1, pp. 32-35, January 2016, doi: 10.1109/MAES.2016.140011.

[5] Clark W. Gellings, "Smart Grid Planning and Implementation," in Smart Grid Planning and Implementation, River Publishers, 2015, pp.i-viii.

[6] N. Eghtedarpour and E. Farjah, "Power Control and Management in a Hybrid AC/DC Microgrid," in *IEEE Transactions on Smart Grid*, vol. 5, no. 3, pp. 1494-1505, May 2014, doi: 10.1109/TSG.2013.2294275.

[7] N. Eghtedarpour and E. Farjah, "Power Control and Management in a Hybrid AC/DC Microgrid," in *IEEE Transactions on Smart Grid*, vol. 5, no. 3, pp. 1494-1505, May 2014, doi: 10.1109/TSG.2013.2294275.

[8] T. Dragicevic, J. C. Vasquez, J. M. Guerrero and D. Skrlec, "Advanced LVDC Electrical Power Architectures and Microgrids: A step toward a new generation of power distribution networks.," in *IEEE Electrification Magazine*, vol. 2, no. 1, pp. 54-65, March 2014, doi: 10.1109/MELE.2013.2297033.

[9] Kai Sun; Yunhe Hou; Wei Sun; Junjian Qi, "Renewable and Energy Storage in System Restoration," in Power System Control Under Cascading Failures: Understanding, Mitigation, and System Restoration, IEEE, 2019, pp.295-356, doi: 10.1002/9781119282075.ch8.

[10] M. M. Morcos, N. G. Dillman and C. R. Mersman, "Battery chargers for electric vehicles," in *IEEE Power Engineering Review*, vol. 20, no. 11, pp. 8-11, Nov. 2000, doi: 10.1109/39.883280.

[11] J. W. Dixon and M. E. Ortuzar, "Ultracapacitors + DC-DC converters in regenerative braking system," in *IEEE Aerospace and Electronic Systems Magazine*, vol. 17, no. 8, pp. 16-21, Aug. 2002, doi: 10.1109/MAES.2002.1028079.

[12] D. Bourner, "Bidirectional DC-DC Converter Systems: Sustaining Power Component Design Methodology to Achieve Critical Power Conditioning," in *IEEE Power Electronics Magazine*, vol. 5, no. 2, pp. 66-71, June 2018, doi: 10.1109/MPEL.2018.2821939.

[13] Anuradha M. Annaswamy; Massoud Amin, "IEEE Vision for Smart Grid Controls: 2030 and Beyond," in *IEEE Vision for Smart Grid Controls: 2030 and Beyond*, vol., no., pp.1-168, 20 June 2013, doi: 10.1109/IEEESTD.2013.6577608.

Chapter-2

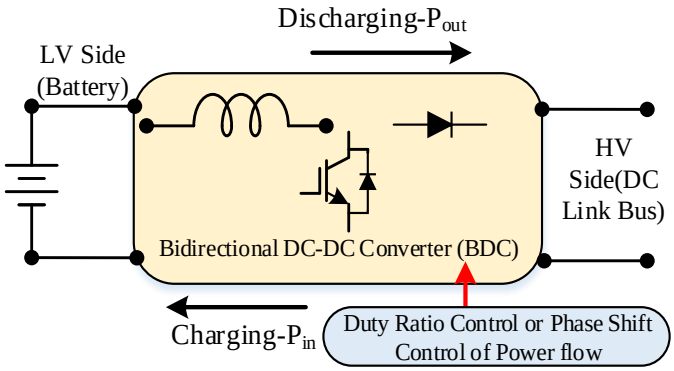
Review of Bidirectional DC-DC Converter

A detailed topological review of non-isolated BDC is performed in this chapter. Small discussion on isolated BDC with advantages and disadvantages are mentioned to establish the necessity of non-isolated BDC. Different circuit topologies like SEPIC, switched capacitor, switched inductor, coupled inductor and hybrid structures are discussed which helps to achieve high conversion factor. Several critical problems in designing non-isolated BDCs are also discussed in this chapter which forms a background to establish research problems and topological requirements for the application in microgrid.

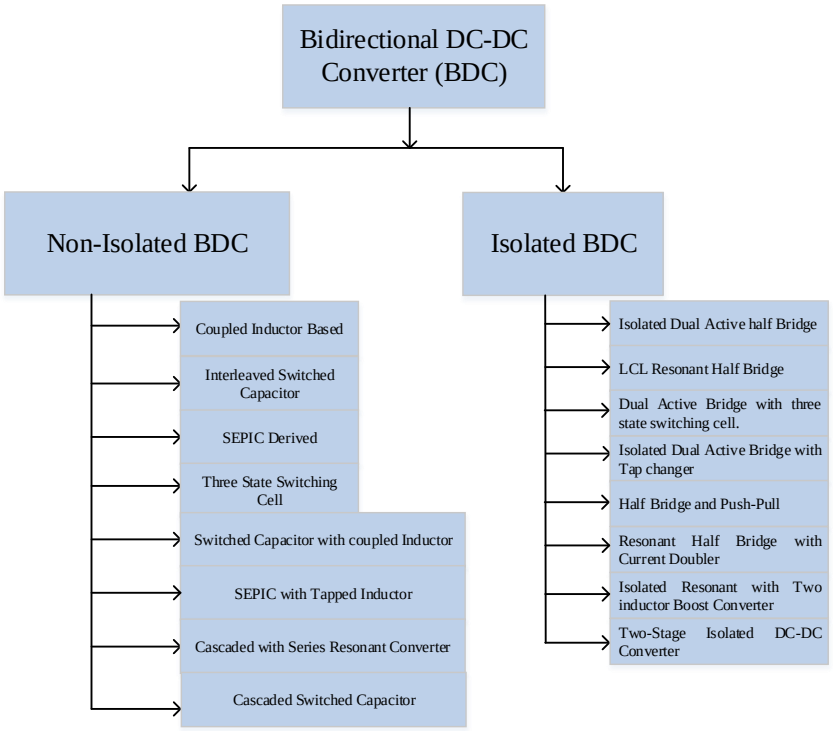
2. Review of Bidirectional DC-DC Converter

2.1. Introduction

Bidirectional DC-DC Converter (BDC) is a power electronic circuit which is capable to control the power flow in two ways i.e., from battery to DC bus or vice versa. The BDC not only controls the power flow but also acts as an interfacing circuit between two different DC voltage levels. It can boost the input voltage while discharging the battery and can step down high voltage (HV) DC bus to charge the low voltage (LV) battery side [1]. The power flow can be controlled through switching sequence commonly applied for non-isolated BDC or through phase shift for isolated BDC [2]. The generalized structure of BDC is shown in Fig. 2.1 (a).



(a)



(b)

Fig. 2.1. General structure of (a) bidirectional converter and power flow (b) different topologies of BDC

For non-isolated BDC, the ground path is common between input ports to output ports whereas for isolated BDC, high frequency ferrite core transformer is used between two ports. Isolated BDC uses AC power flow concept using high frequency transformer which acts as AC link between two different DC voltage levels. For non-isolated DC-DC converter, power flow is maintained by duty ratio-based voltage mode control [2]. These types of converters depend on DC bus voltage for controlling the power flow whereas for isolated DC-DC converter phase shift between primary to secondary AC link voltage controls the power flow. The major topological division in BDC design is mentioned in Fig. 2.1 (b).

2.2. Isolated Bidirectional DC-DC Converter

Isolated BDC provides bidirectional power flow by just controlling the phase difference between intermediate AC voltages between transformer primary to secondary winding [2]. The power flow control can be easily explained through a simple network of two alternating sources (V_1 and V_2) with different phase connected through a line inductance as shown in Fig. 2.2. The phase angle of reference voltage V_1 can be considered as zero. Therefore, the phase difference between V_1 and V_2 is θ.

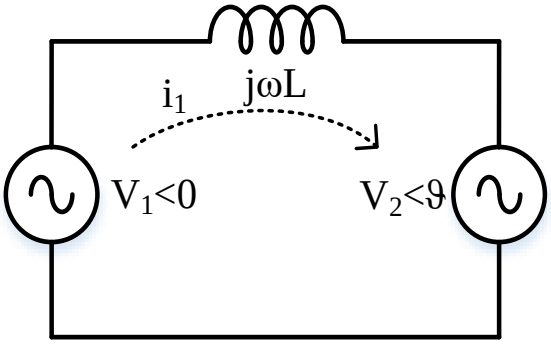


Fig. 2.2. AC active power flow between two sources with line inductance.

The current (i_1) flowing through the network is

$$i_1 = \frac{v_1 < 0 - v_2 < \vartheta}{j\omega L} \text{ i.e. } i_1(t) = \frac{1}{\omega L}\left[v_1 \sin \omega t + v_2 \sin(\omega t - \vartheta)\right] \tag{2.1}$$

The real part of the voltage V_2 is $v_2(t) = v_2 \cos(\omega t - \vartheta)$

Thus, the average power absorbed by the voltage source V_2 is

$$\langle P(t) \rangle = \frac{1}{T}\int_0^T \left[\left(\frac{v_1}{\omega L}\sin \omega t + \frac{v_2}{\omega L}\sin(\omega t - \vartheta)\right) v_2 \cos(\omega t - \vartheta) \right] dt = \frac{v_2 v_1}{\omega L}\sin \vartheta \tag{2.2}$$

The absorption or dissipation of active power depends on the phase angle difference between two ac voltage sources. If the phase difference ϑ is positive then voltage source V_2 is consuming active power and for negative value it signifies that it is delivering active power. Therefore, bidirectional power flow is possible just by altering the phase difference as per equation 2.2. Similar concept is used in isolated BDC to control the active power flow. The high frequency isolated transformer leakage inductance ($L_{leakage}$) can be acted as line inductance [3-4] just like the inductance shown in Fig. 2.2. Transformer primary to secondary turns ratio (n) can be used for achieving the voltage gain improvement. As the input is DC therefore inverter unit is required before primary of the transformer and in the secondary side active rectifier is essential for converting AC voltage to DC load. The reverse configuration is essential if power flow changes in opposite direction. Hence inverter/rectifier unit is essential in both sides of isolating high frequency transformer. This is the main reason for defining isolated BDC as dual active bridge (DAB). The general architecture of DAB is shown in Fig. 2.3.

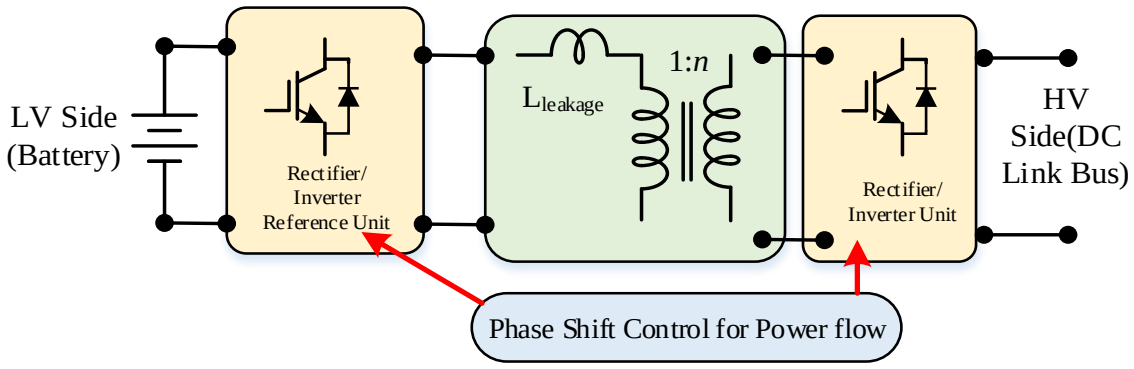


Fig. 2.3. General structure of isolated BDC (DAB).

2.2.1. Isolated Voltage Source Based Bidirectional DC-DC Converter

Isolated voltage source based bidirectional converter is popularly known as dual active bridge (DAB) converter [3] which is shown in Fig. 2.4. This converter has utilized the phase shift of AC voltages between input bridge and output bridge to control the power flow. Power flow equation can be derived from finding voltage across leakage inductance (V_L) and current through it (i_L). The primary bridge is considered as the reference bridge. Based on the switching state between both the bridges, the phase difference between AC voltages can be determined. The operating modes and key operating waveforms are shown in Fig. 2.5. The primary ac link voltage $V_{ab}=V_{LV}$, when switch S_1 and S_2 are turned ON. Similarly, the reflected primary winding voltage from output across c-d node is V_{HV}/n. By turning ON, S_a and S_b , positive voltage can be generated between c-d point

and V_L becomes V_{LV}-V_{HV}/n. However, when S_c and S_d are ON then the leakage inductor voltage becomes $V_{LV}+V_{HV}/n$. During this time, leakage inductor current (i_L) rises with a slope of $\frac{V_{LV}+\frac{V_{HV}}{n}}{L}$. If V_{LV} becomes equal to V_{HV}/n then the difference which is inductor voltage becomes zero and current through leakage inductance is constant either positive or negative based on previous state current. This is known as extreme condition of DAB as shown in Fig. 2.5.

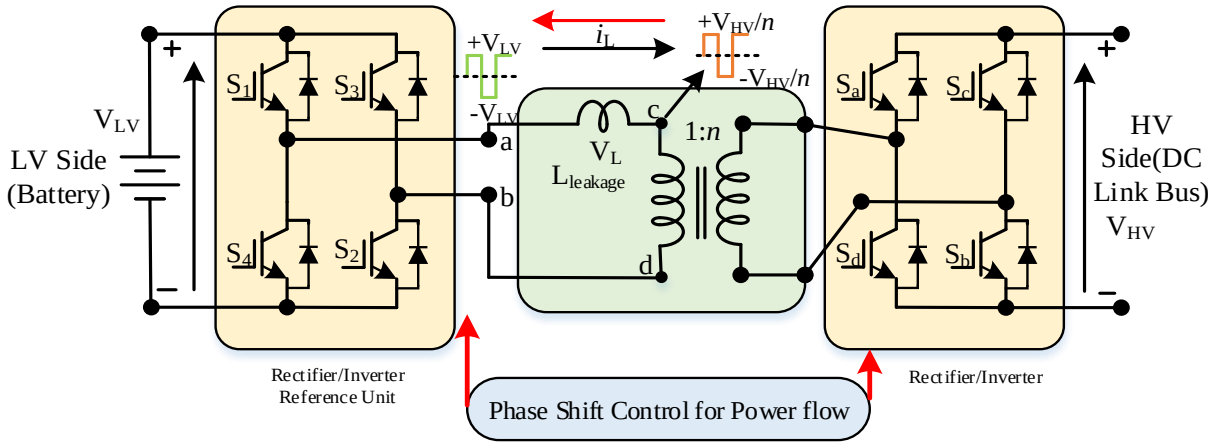


Fig. 2.4. Voltage source based DAB.

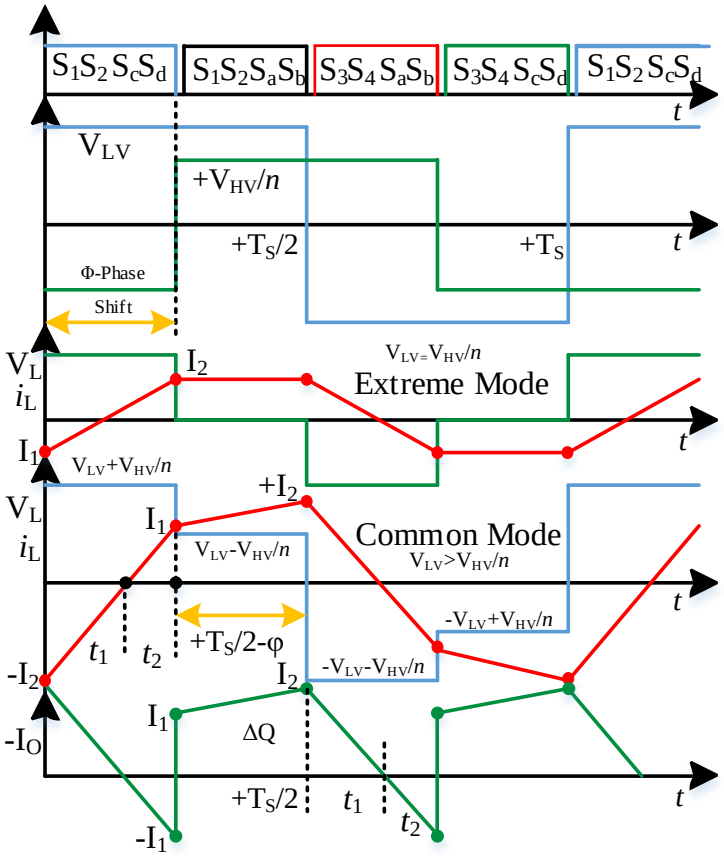


Fig. 2.5. Key operating waveform.

This boundary condition is very crucial as it helps to determine required leakage inductance and output capacitor values. This mode also guides to find the range of duty for achieving soft switching operation i.e., zero voltage switching (ZVS) range. In DAB operation generally, $V_{LV} > V_{HV}/n$ condition prevail which is known as common mode of operation where leakage inductance voltage never becomes zero. Therefore, inductor current waveform never becomes trapezoidal shape which is a good characteristic in extreme operating mode. Trapezoidal shape current ensures less switch peak current as well as has less RMS current. However, there are several clever ways recently developed using advanced PWM technique which guarantees less RMS and peak switch current. The current slopes in common modes of DAB operations are, $\frac{V_{LV}+\frac{V_{HV}}{n}}{L}$, $\frac{V_{LV}-\frac{V_{HV}}{n}}{L}$, $\frac{-V_{LV}-\frac{V_{HV}}{n}}{L}$ and $\frac{-V_{LV}+\frac{V_{HV}}{n}}{L}$ as shown in Fig. 2.5. The peak value of leakage inductor symmetrical current is I_2 where current slope is $\frac{V_{LV}-\frac{V_{HV}}{n}}{L}$. When voltages across V_L is maximum i.e., $V_{LV}+V_{HV}/n$ then the current slope is maximum and corner current is I_1. Current I_1 and I_2 are symmetrical as shown in Fig. 2.5. The phase shift φ can be determined graphically by adding two timing i.e., $t_1$and t_2. The phase shift φ is (t_1+ t_2). The inductor current value of I_1 and I_2 are

$$I_2 = t_1 \frac{V_{LV}+\frac{V_{HV}}{n}}{L} \text{ and } I_1 = t_2 \frac{V_{LV}+\frac{V_{HV}}{n}}{L} \tag{2.3}$$

Again, the difference (I_2-I_1) and addition (I_2+I_1) of two currents are

$$I_2 - I_1 = \left[\frac{T_s}{2}-\varphi\right]\frac{V_{LV}-\frac{V_{HV}}{n}}{L} \text{ and } I_2 + I_1 = [\varphi]\frac{V_{LV}+\frac{V_{HV}}{n}}{L} \tag{2.4}$$

The average value of the output current is very crucial to find out the charge which indirectly determine the voltage gain equation for DAB.

$$\Delta Q = [I_1+I_2]\left[\frac{T_s}{2}-\varphi\right] + \frac{1}{2}I_2t_1 - \frac{1}{2}I_1t_2 = [\varphi]\left[\frac{T_s}{2}-\varphi\right]\frac{V_{LV}+\frac{V_{HV}}{n}}{L} + \frac{1}{2}I_2t_1 - \frac{1}{2}I_1t_2 \tag{2.5}$$

By replacing all the values of t_1 and t_2, the charge can be derived which is

$$\Delta Q = [\varphi]\left[\frac{T_s}{2} - \varphi\right]\frac{V_{LV}}{L} \tag{2.6}$$

Therefore, the average load current Io is

$$I_o = \frac{\Delta Q}{n\frac{T_s}{2}} = [\varphi]\left[1 - \frac{\varphi}{\frac{T_s}{2}}\right]\frac{V_{LV}}{nL} \tag{2.7}$$

When $D=2\varphi/T_s$, then the average value of the load current can be derived as

$$I_o = \left[\frac{D(1-D)T_s}{2}\right]\frac{V_{LV}}{nL} = \left[\frac{D(1-D)}{2}\right]\frac{V_{LV}}{f_{sw}nL} \tag{2.8}$$

From this equation the voltage gain is

$$M = \frac{V_{HV}}{V_{LV}} = \left[\frac{D(1-D)}{2}\right]\frac{R_L}{f_{sw}nL} \tag{2.9}$$

The voltage gain of DAB [3] is load dependent and the maximum power depends on D value which depends on duty cycle. Load power is proportional to

$$P_L = K_1[D(1-D)]^2 \tag{2.10}$$

For both directional power flow at 0.5 duty ratio the power flow is maximum which can be derived from equation (2.10) and shown in Fig. 2.6.

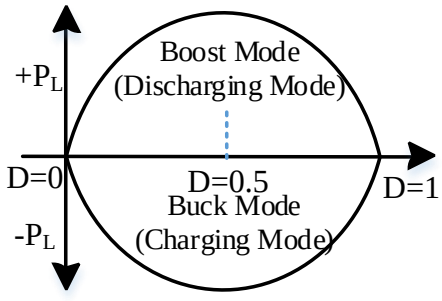


Fig. 2.6. DAB power flow in boost and buck mode with variation of D values.

The power flow control of DAB is performed through phase shift. However, single phase shift-based DAB control has major problem of circulating current as shown in Fig. 2.7 (a). This technique has higher conduction loss especially in the primary bridge [4] and has limited duty ratio range for achieving soft switching i.e., ZVS. By modifying the

PWM pattern between primary and secondary bridge, the circulating current problem of DAB can be eliminated. By making primary bridge AC link voltage to three level voltage or adding a zero state the freewheeling time of primary bridge is reduced and circulating current loss can be effectively minimized [5-6]. This PWM technique is known as extended phase shift control (ESP).

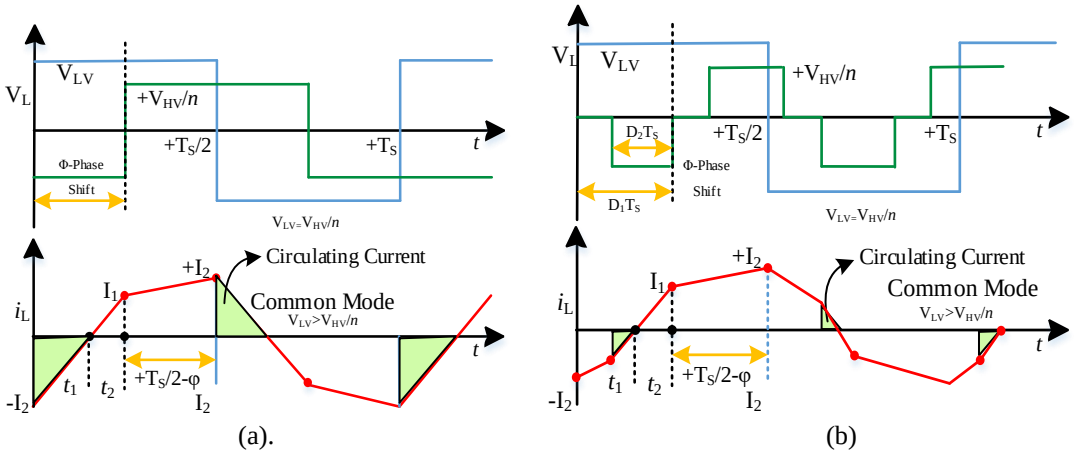


Fig. 2.7. PWM pattern of DAB (a) single phase shift (SPS) (b) extended phase shift (ESP).

This technique has internal phase shift in either in the primary or in secondary active bridge. Though the phase shift is same, but there is a net reduction of effective phase shift between two bridges. This technique comes with disadvantages of complex control as well as net reduction of active power flow in either direction. This technique is shown in Fig. 2.7 (b). Apart from EPS technique there are two other PWM techniques i.e. double phase shift (DPS) and triple phase shift (TPS) are popular in DAB power flow control which provides better efficiency and extended ZVS operating range [6]. However, the control algorithm is complex for achieving ZVS as well as has larger transient time in power flow reversal.

Soft switching operation of DAB can be achieved utilizing MOSFET junction capacitance (C_a, C_b) and antiparallel diode (D_a, D_b) utilizing synchronous rectification concept. The dead time between a transition state should be intelligently selected to achieve the ZVS turn-ON operation of all active switches. The general convention of achieving ZVS turn-ON is shown in Fig. 2.8. The dead time between two PWM pulses must be sufficient so that complementary switch voltage become zero before applying PWM pulse to achieve ZVS turn-ON. The junction capacitor charging and discharging time denoted by t_a which guides the dead time value. Dead time (t_d) should be greater than t_a for successful ZVS turn-ON operation. The t_a value is dependent on load current

(I_L) and leakage inductance (L) which limits the duty ratio range (D) of ZVS turn-ON operation in DAB.

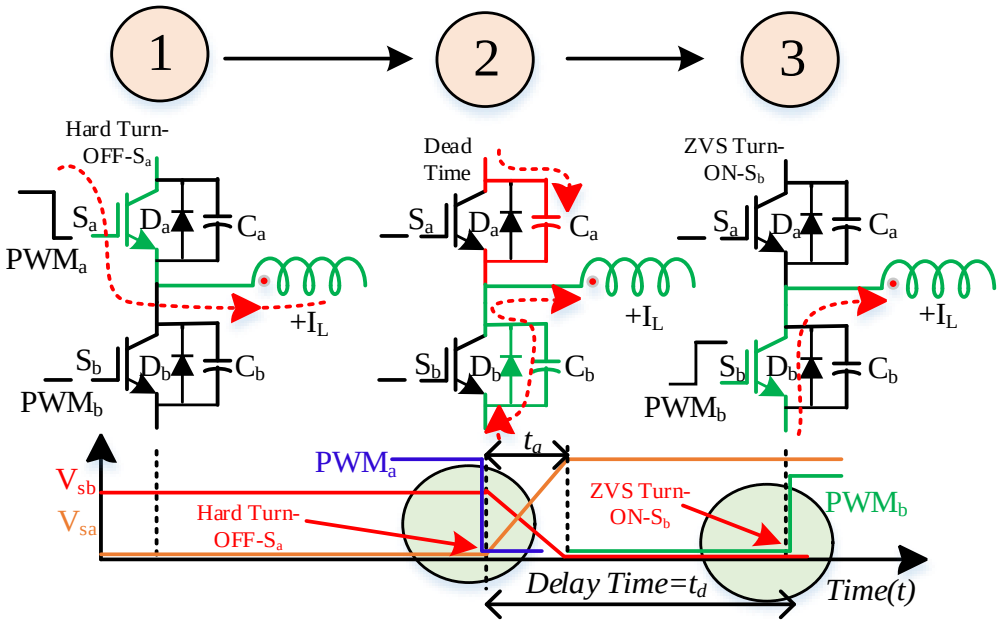


Fig. 2.8. Soft Switching Operation i.e., ZVS turn-ON of DAB in one half bridge

Therefore, in summary voltage source based isolated BDC i.e., voltage fed BDC has many advantages [7] like easy power flow control in both the directions with flexible gain which can be adjusted by two degrees' of freedom i.e., either by controlling transformer turns ratio or by adjusting duty ratio. But the major disadvantages are:

- Power transfer depends on leakage inductance with maximum power flow possible at D=0.5 for both the operating mode as shown in Fig. 2.6.
- The number of active switches is generally eight for DAB which requires eight separate gate driver circuit as well as control circuit which makes system more complex.
- The voltage gain depends on load resistance and soft switching range i.e., ZVS operation is dependent on load current. This makes limited range of adequate gain with soft switching operation. This problem worsens for lightly loaded condition and input voltage variation.
- The leakage inductance current waveform is generally non-trapezoidal shape for boost as well as buck mode which makes increased RMS and peak current of all active switches. It also incurs large circulating current loss.
- Different phase shift i.e., internal or external or both phase shift can reduce the circulating current. However, it limits the power transfer capability. Moreover, operation becomes more complex with ZVS turn-ON feature.

Half bridge-based proposals are also found in literature but it has more complex operation than conventional voltage source-based DAB especially in achieving soft switching operation [8-9]. Thus, easy control with extended soft switching range with minimum RMS current operation using half bridge BDC [8] is still an area which is unexplored.

The mentioned problem in voltage source-based DAB also include large input current ripple and it creates practical difficulties when interfacing with battery storage units. Voltage source based BDC has considerable large ripple current except the inductance value is very high. Large leakage inductance value incurs duty cycle loss in DAB. Therefore, it is not a recommended design criterion for achieving higher efficiency. Ideally, battery input current ripple should be zero with all the required features for BDC explained earlier in this section encourages researchers to check for isolated current fed BDC which is discussed in the next section.

2.2.2. Isolated Current Source Based Bidirectional DC-DC Converter

Current fed isolated BDC have better soft switching range in both the bridges as well as having less input current ripple at low voltage side [4], [10] compared to voltage fed DAB. The general structure of current fed DAB is shown in Fig. 2.9.

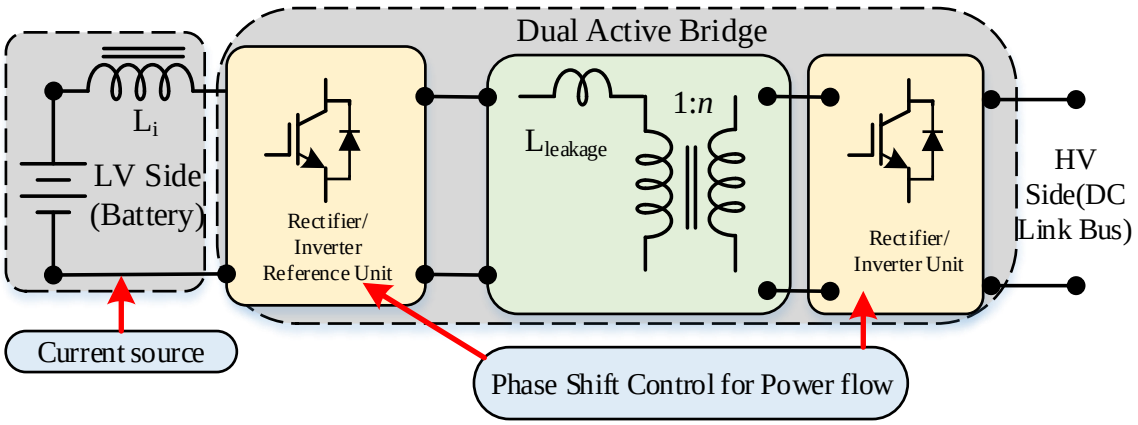


Fig.2.9. Current source based dual active bridge.

The operation is similar to voltage source-based DAB with phase shift control discussed in the previous section. The major advantage of having less duty cycle loss with extended ZVS range. However, this converter is having large voltage stress at the primary bridge switches. To minimize the voltage stress problem, there are many techniques found in the literature which broadly divided into two categories [11-12] i.e. (a) passive RCD based snubber network (b) active clamp-based snubber network. The active clamp-based solution is widely popular due to less power loss and easy control. Flyback snubber, flyback and parallel capacitor snubber and snubber-less naturally clamped DAB falls

under active clamp-based solution to achieve less voltage stress. The snubber circuit-based solutions in current fed DAB is shown in Fig. 2.10. RCD based snubber circuit has problem [11] of higher circulation conduction loss when snubber capacitor discharges through resistance. The increased conduction loss of using passive RCD snubber can be eliminated using active clamp snubber circuit. The conduction loss is less in active clamp snubber circuit compared to passive snubber. However due to resonance, the current spikes are more using active clamp circuit. Flyback based active snubber circuit eliminate the current spikes problem as well as increased conduction loss. The clamped capacitor voltage is maintained by recycling the stored energy. However, flyback-based snubber circuit [12] has limitation of large inrush current. Therefore, in flyback-based snubber circuit [12], recharging circuit is necessary for limiting the inrush current.

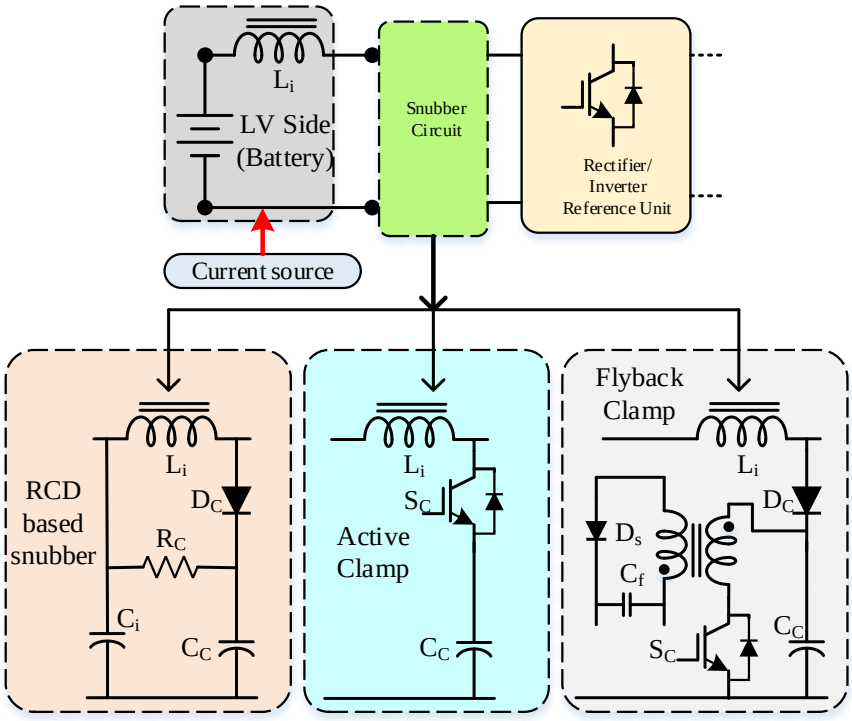


Fig. 2.10. Current source based dual active bridge.

All the mentioned current fed DAB with snubber circuit has major problem of large current ripple similar to voltage fed DAB in low voltage side. Therefore, integrating these types of converter in storage interface is not robust and reliable. Over last decade many researches have been carried out to find the circuit-based solutions to minimize the low voltage side current ripple [13-14]. Interleaved current fed DAB is the major development in the bidirectional converter especially for interfacing low voltage, low current ripple source [4], [15].

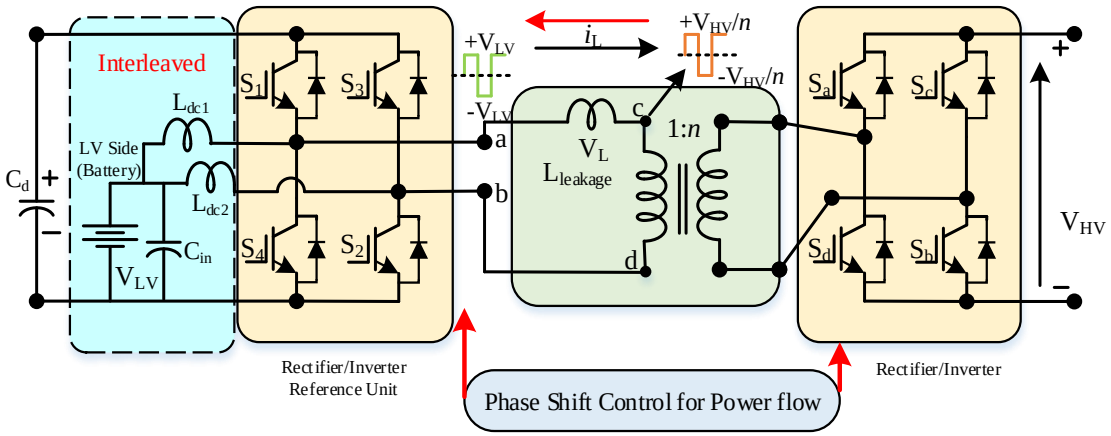


Fig. 2.11. Current source based interleaved dual active bridge.

The general circuit structure of interleaved current fed DAB is shown in Fig. 2.11. Based on the phase difference between input to output bridges, the operating modes of current fed interleaved BDC are divided into four operating modes [4] i.e., Mode-I, Mode-II, Mode-III and Mode-IV. Out of these modes, mode-I and mode-II are used due to the fact that converter operates within 0.25 to 0.75 duty ratio range where the phase shift should be within $\frac{\pi}{6}$.

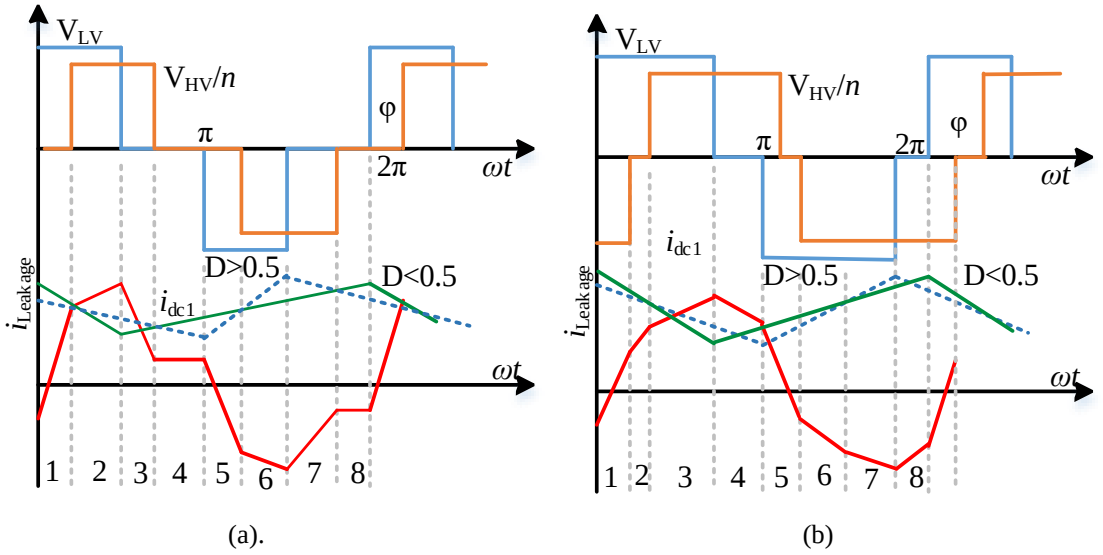


Fig. 2.12. Important operating modes within 0.25 to 0.75 duty ratio, (a) Mode-I (b) Mode-II

The active power flow equation is similar to voltage fed DAB. Due to interleaved structure with the ZVS condition [4] in low voltage side bridge is different compared to voltage fed DAB. The ZVS turn-ON condition is

$$\frac{P_2}{2V_{LV}}+\frac{V_{LV}(1\text{-}D)\pi}{m\omega L_{Leakage}}+\frac{V_d\left[d\phi+(1\text{-}d)(1\text{-}D)\pi\right]}{\omega L_{Leakage}}>0 \text{ for } S_1 \text{ and } S_3 \qquad (2.11)$$

$$\frac{P_2}{2V_{LV}}+\frac{V_{LV}(1-D)\pi}{m\omega L_{Leakage}}+\frac{V_d[d[\phi-\pi]+(1+d)(1-D)\pi]}{\omega L_{Leakage}}<0 \text{ for } S_2 \text{ and } S_4 \qquad (2.12)$$

Where, $d=\frac{V_{HV}}{nV_d}$, $m=\frac{L_{dc1}}{L_{Leakage}}$, D=Duty ratio and φ=Phase shift.

The soft switching range of S_2 and S_4 depends on the value of d. For lower value of d, the ZVS range of these two switches are extended which is also shown in Fig. 2.13 (a) and Fig. 2.13 (b). Thus, when d<1 and D<0.5 ZVS operation of the primary bridge switches are not load dependent and guaranteed [16]. However, during same condition the secondary side bridge is hard switched.

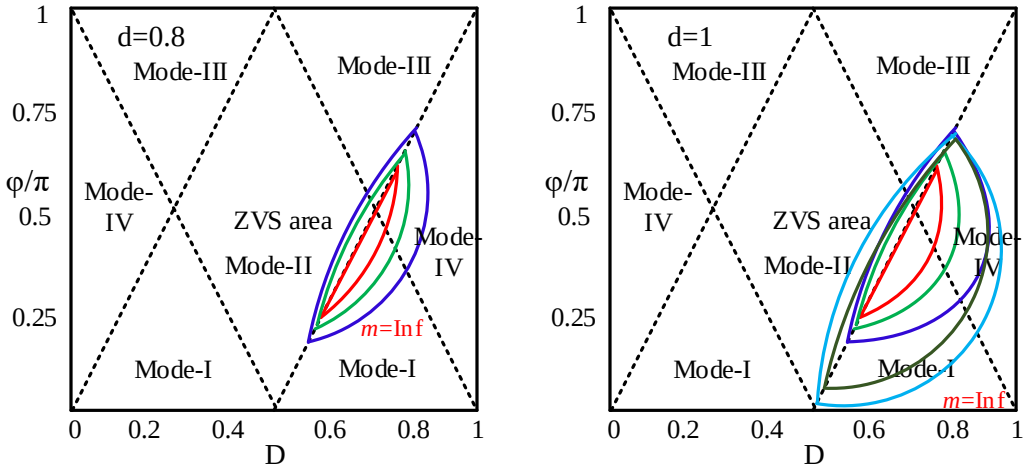


Fig. 2.13. ZVS boundaries of bottom switches (S_2 and S_4) of LV side bridge for (a) d=0.8 (b) d=1

In summary the current source based dual active bridge have many advantages [17-18] over voltage source-based converter of similar ratings and discussed in details. However, both these isolated converters have some critical disadvantages especially at low to medium power level i.e., upto 1-1.5kW and they are as follows:

(a) Load dependent soft switching conditions for active switches.

(b) Complexity in achieving soft switching in both bridges simultaneously for a wider load range.

(c) Complexity in implementing control architecture. Eight active switches require extra driver circuit which leads to extra loss.

(d) Current source based isolated dual active bridge has less input ripple current at low voltage side but requires complex snubber circuit to minimize voltage spikes. Also, the current ripple performance is not constant for wider duty cycle variation.

(e) Isolated transformer leakage inductance controlling is difficult which indirectly control the power flow.

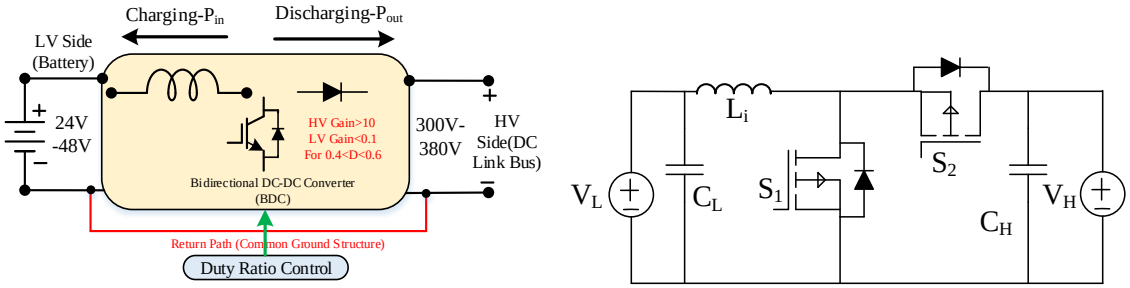
(f) Duty cycle loss is another major problem of these isolated types of converters.

(g) Designing dead time is very critical as improper selection leads to loss of soft switching operation.

These issues left a research gap to investigate on non-isolated version of bidirectional DC-DC converter using different circuit topologies. These types of BDCs are discussed in the next section in details.

2.3. Non-Isolated Bidirectional DC-DC Converter

Non-isolated bidirectional DC-DC converters are simple in structure [19-20] and has less control complexity. Duty ratio-based control taking bus voltage information as feedback can be easily implemented to control the power flow. There is no isolation stage in these types of converters and has common ground structure as shown in Fig. 2. 14 (a).



(a) (b)

Fig. 2.14. General structure of (a) non-isolated BDC and (b) conventional BDC.

By changing the switching pattern, a synchronous boost converter can be operated as buck converter and it is the most primitive non-isolated BDC. The structure of conventional BDC is shown in Fig. 2. 14 (b). Although the controlling power flow is simple but this converter has several operating disadvantages [21] like it has (a) less efficiency i.e., below 60% above 0.5 duty ratio in both buck as well as boost operating modes, (b) less voltage conversion factor in both the operating modes, (c) large voltage stress in all active switches and (d) large switching losses. These limitations encourage researchers to find alternative circuit topologies to achieve higher efficiency as well as large voltage conversion factors with reduced stress at all active switches. New circuit design concepts with limitations are discussed in details which forms research background in this current work.

2.3.1. SEPIC Derived BDC

Single ended primary inductor converter (SEPIC) was first introduced by bell laboratory in 1978 with unidirectional feature using a switch and one diode. The diode can be replaced by a switch to form SEPIC BDC [22-26] as shown in Fig. 2. 15 (a).

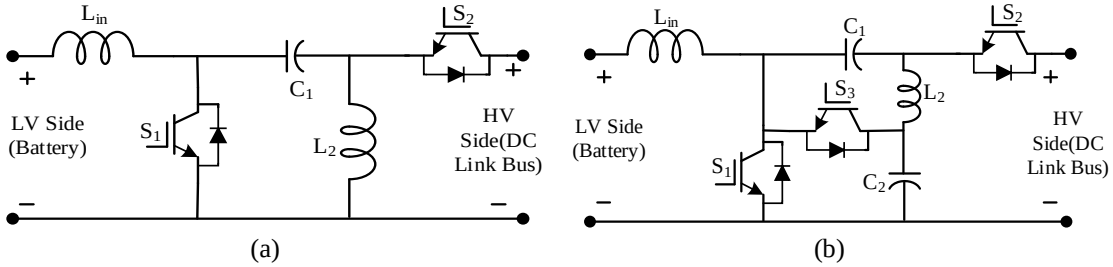


Fig. 2.15. General structure of (a) SEPIC BDC and (b) modified SEPIC BDC.

It has capability to control the power flow in either direction i.e. buck or boost mode. The major problems of this primitive circuit are less voltage conversion factor, discontinuous output current, large switch voltage stress i.e. (V_{in}+V_o). This circuit has voltage gain of D/(1-D) which is less for 48V-380V BDC system. The output voltage can be appropriate if multiple SEPIC BDC output are connected in series and input side is connected in parallel. This configuration is not applicable as it has more losses which reduces the conversion efficiency. Another way to improve the voltage gain conversion factor of SEPIC derived BDC is to use capacitor diode network just like high gain boost converter. This diode capacitor network can improve voltage gain in one directional power flow. But for bidirectional power flow the diodes can be replaced by switch [25-26] as shown in Fig. 2.16. This circuit has continuous current in both input and output ports.

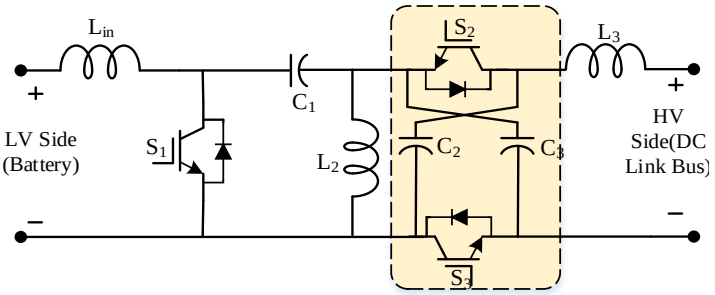
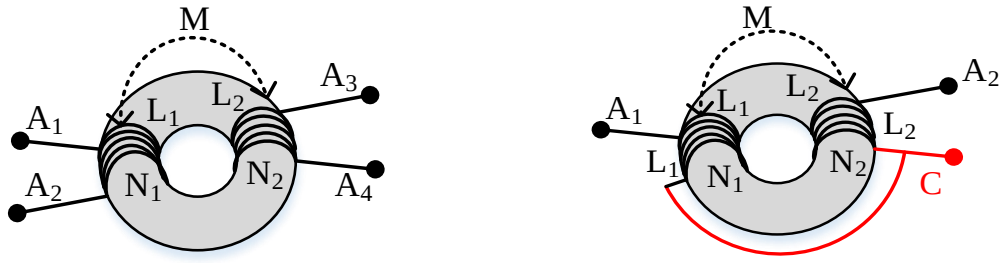


Fig. 2.16. Modified high gain SEPIC BDC.

However, even after improving voltage conversion factor these types of non-isolated BDC have many problems like (a) high switch voltage stress as well as current stress (b) lower efficiency (c) hard switching operation of active switches (d) large size inductor to minimize current ripple. These limitations encourage researchers to find the alternative topological solution.

2.3.2. SEPIC with Coupled Inductor BDC

Application of coupled inductor can improve the voltage gain of existing SEPIC circuits [27]. Ring core-based two winding transformer is shown in Fig. 2.17 (a) where turns ratio is N_1/N_2 and inductance ratio primary to secondary is L_1/L_2. The mutual inductance is M. The same transformer can be acted as coupled inductor as shown in Fig. 2.17 (b). The main benefit of coupled inductor is it can enhance voltage gain due to incorporation of turns ratio and has common point to connect in a suitable position while designing new topologies.



(a). (b)

Fig. 2.17. Ring core based two winding (a) transformer (b) coupled inductor.

The primitive SEPIC based circuit is modified using coupled inductor [22], [27] as shown in Fig. 2.18. This circuit improves the voltage conversion factor and has less component addition. This also has two degree of freedom like the isolated converters i.e. duty ratio and turns ratio.

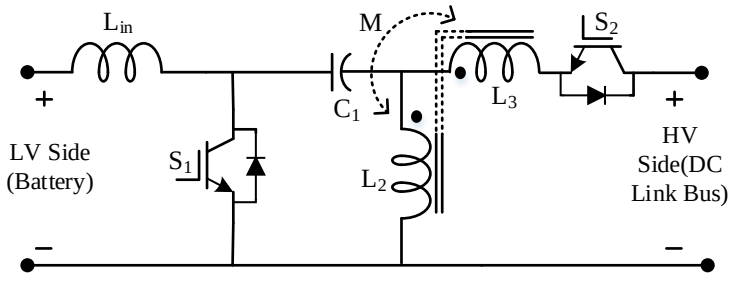


Fig. 2.18. Coupled inductor based modified SEPIC BDC.

Steady state voltage gain of SEPIC can further be enhanced by using active voltage multiplier cell and coupled inductor [27] as shown in Fig. 2.19. The circuit performs well in both directions of power flow and suitable for 48V-380V conversion system. However, poor efficiency and large current stress at the main switch (S_1) limits the application. The operating duty ratio range is also limited. The input current ripple is also large in this type of solution. The SEPIC [22] circuit is modified using coupled inductor to achieve soft switching feature of active switches as shown in Fig. 2. 20. This helps to achieve high efficiency operation. This circuit is having higher voltage gain factor compared to earlier modifications in the literature. Switch voltage stress is also less in this solution.

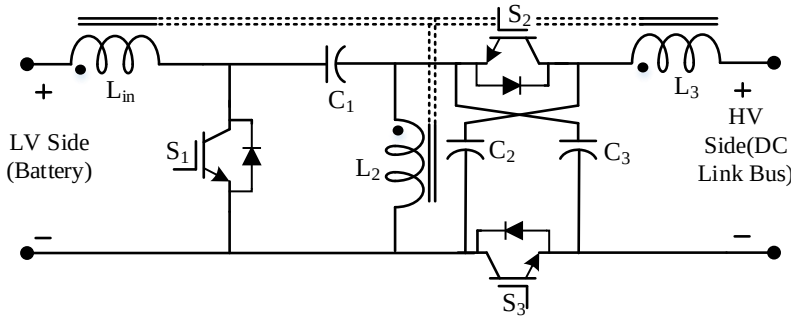


Fig. 2.19. Coupled inductor based modified SEPIC BDC with voltage multiplier cell.

The major drawbacks of this topological solution are (a) large switch current stress, (b) large input current ripple and (c) large efficiency variations for wider load range.

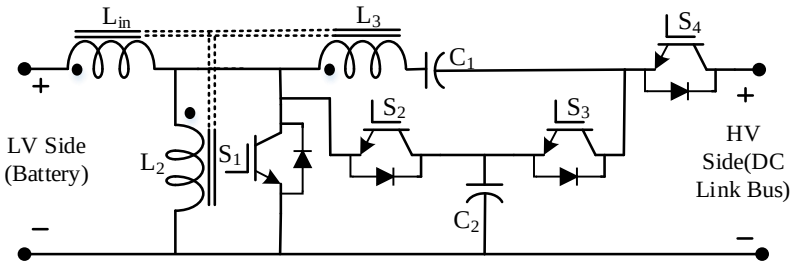
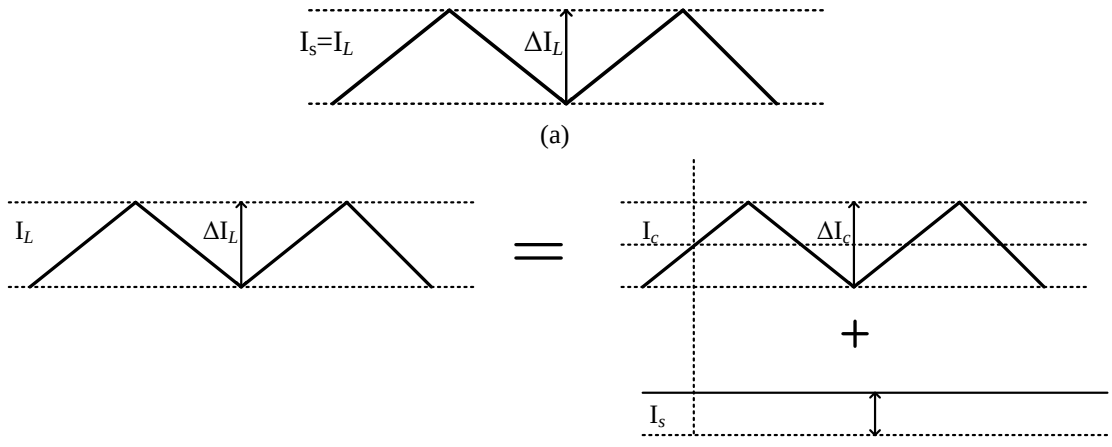
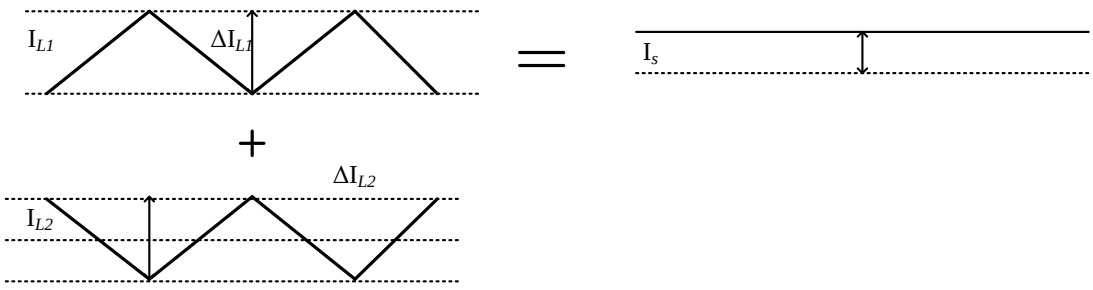


Fig. 2.20. Higher efficiency coupled inductor based modified SEPIC BDC with soft switching features.

2.3.3. Interleaved Switched Capacitor based BDC

The topological solutions discussed in the previous section has common problem of large input current ripple as shown in Fig. 2.21 (a). This requires large input inductor as well as filter capacitor to minimize input ripple current. Filter capacitor provides the ripple current required by the inductor as shown in Fig. 2.21 (b). The input ripple current problem can be effectively solved by the interleaved BDC structure where two inductor current waveforms are complementary as shown in Fig. 2.21 (c). The switching of two parallel input inductor helps to reduce the ripple current due to asymmetry in inductor current slopes. For duty ratio exactly at 0.5 there will be a zero-input current ripple as resultant inductor current ripple cancels each other.





(c)

Fig. 2.21. (a) Inductor current ripple (b) ripple free source current using large filter capacitor (c) ripple free source current using interleaved structure.

This solution is good as inductor size as well as filter capacitor size can be reduced. The conventional interleaved BDC [28-29] is shown in Fig. 2.22.

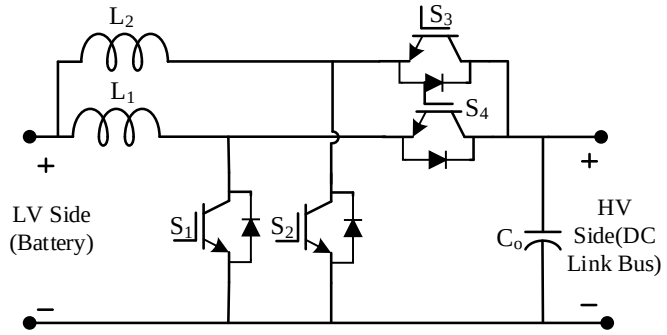
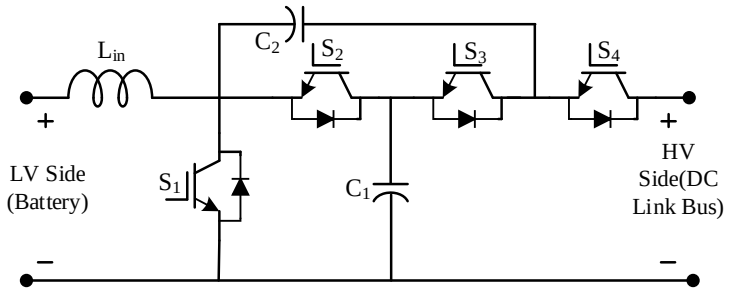
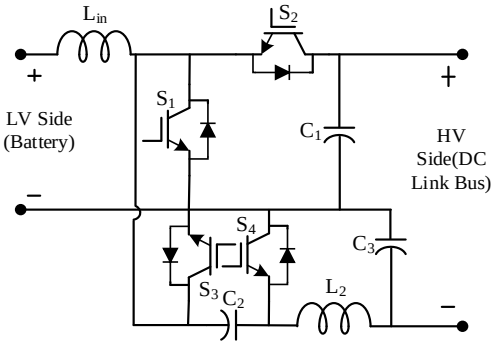


Fig. 2.22. Conventional interleaved BDC structure

Though the input current ripple is very less but this structure is having same voltage gain like conventional synchronous boost converter i.e. 1/(1-D) and similar voltage stress across main switches. To increase the voltage gain with interleaved structure, switched capacitor network is adopted. Switched capacitor network has very simple working principle and capable of voltage boosting. A voltage doubler circuit is an example of switched capacitor network. Similarly, voltage multiplier cell can be added with interleaved structure to increase the voltage gain. A switched capacitor based BDC [30] is shown in Fig. 2.23 (a) which has superior gain and less ripple current. But these types of circuit have excessive large switch current due to direct capacitor voltage switching.



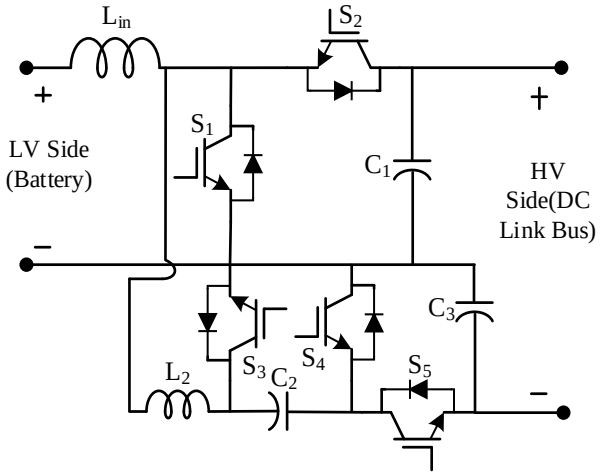
(a)



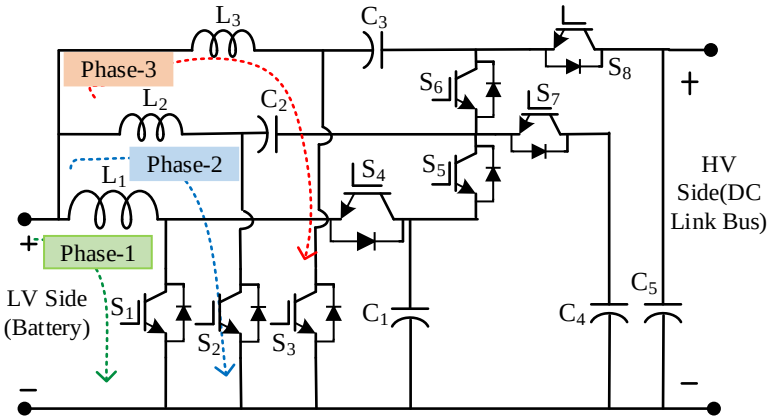
(b)

Fig. 2.23. (a) Switched capacitor BDC and (b) interleaved with switched capacitor

Switched capacitor network has inherent capability of increasing voltage gain and this technique is combined with interleaved structure can be applied to achieve high voltage gain with very less input current ripple. Fig. 2.23 (b) shows the hybridization of interleaved with switched capacitor network. Later the same circuit is modified [32] to increase the voltage gain further which is shown in Fig. 2.24 (a).



(a)



(b)

Fig. 2.24. (a) Modified interleaved with switched capacitor and (b) three-phase interleaved with switched capacitor BDC.

However, the modified circuit has one more active switch compared to earlier. By increasing number of active switches in BDC the circuit complexity increases and more switch requires separate driver circuit with associated extra loss. Thus, the overall system loss increases. Hard switching of these switches further enhances the loss. Interleaved structure is reutilized in three phase parallel structure at the LV side of the BDC [33] as shown in Fig. 2.24(b) to reduce the input ripple current to a very negligible value whereas switched capacitor network in the HV side enhances the voltage gain. This structure has soft switching capabilities of LV switches. The circuit can provide superior voltage gain, less ripple current with the sacrifice of large switch current stress especially at LV side. The numbers of active switches are eight which requires extra driver circuits. The DAB is also having eight number of switches with isolation. Thus, applicability of interleaved high gain non-isolated converter is questionable especially beyond 1.5 kW.

2.3.4. Cascaded Switched Capacitor

Switched capacitor BDCs are simple in structure and can be cascaded to increase the voltage level. Capacitor and active switch combination makes it possible. The basic switched capacitor cell can be cascaded to make large conversion factor. A voltage multiplier based switched capacitor BDC [34] cell is shown in Fig. 2.25(a). The same cell can be extended to achieve three times voltage multiplier output [34] in boost mode as shown in Fig. 2.25 (b).

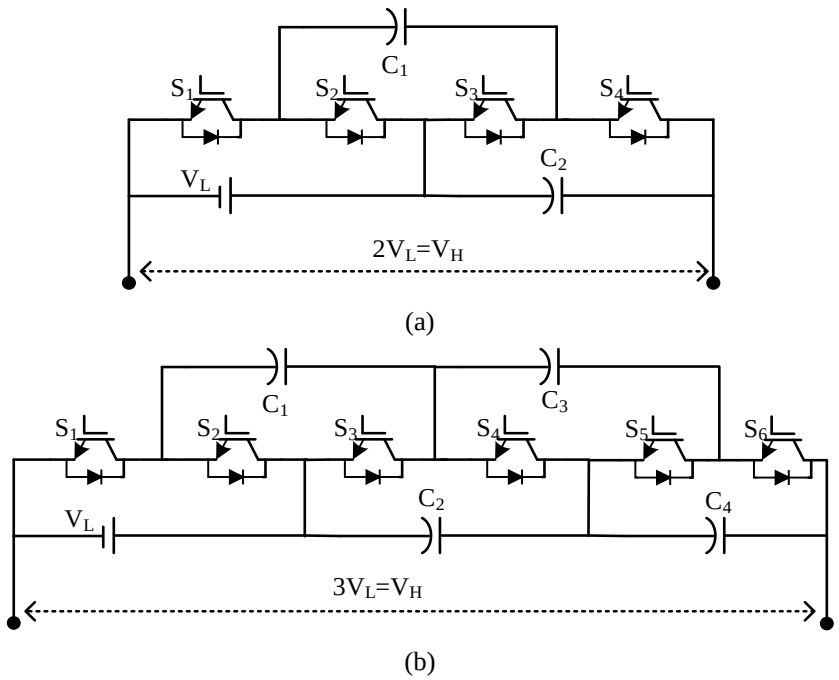


Fig. 2.25. Basic switched capacitor based (a) basic BDC cell (b) cascaded BDC cell

Similarly switched capacitor cell can be cascaded including inductor in the path as proposed by L. Sun *et.al.* [35] and it is an alternative solution to increase the voltage conversion factor further. This extension methodology is shown in Fig. 2.26.

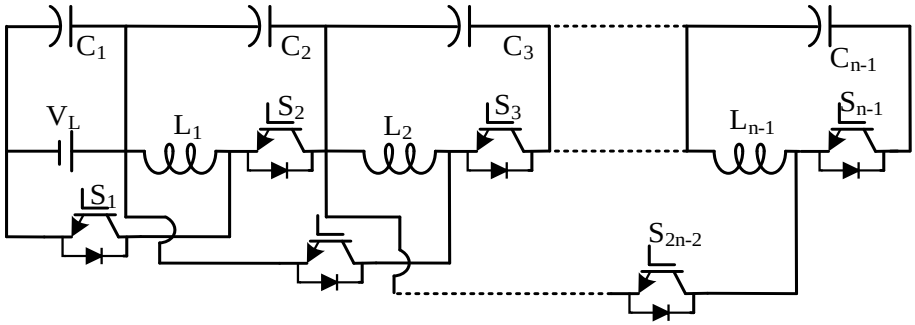


Fig. 2.26. Modified switched capacitor BDC proposed by L. Sun *et.al.* [35].

These types of BDCs have simple topological structure and less control complexity. However, the major issues of these types of converters are (a) large switch peak current (b) high inrush current (c) large voltage ripple (d) large number of active switches. Although, these types of converters have very simple operating principle but never adopted due to other disadvantages mentioned.

2.3.5. Hybrid Structure based BDC

Z-source network is very important for increasing the voltage gain. This network is first introduced in Z-source inverter by F.Z. Peng [36]. Thereafter this network is extensively used for unidirectional high gain boost converter design for PV integrated converter. The same concept is used for designing BDC and the basic unit for Z-source based BDC [37] is shown in Fig. 2.27.

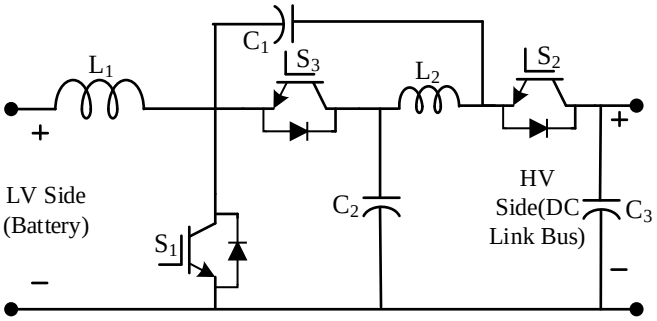


Fig. 2.27. Z-source inverter based basic BDC unit.

There is further achievement in this direction of BDC design. Switched capacitor-based network is integrated successfully for improving the voltage conversion factor further. Thus, hybrid structure of z-source based BDC is a good design technique of non-isolated BDC. The basic hybrid BDC structure is shown in Fig. 2.28.

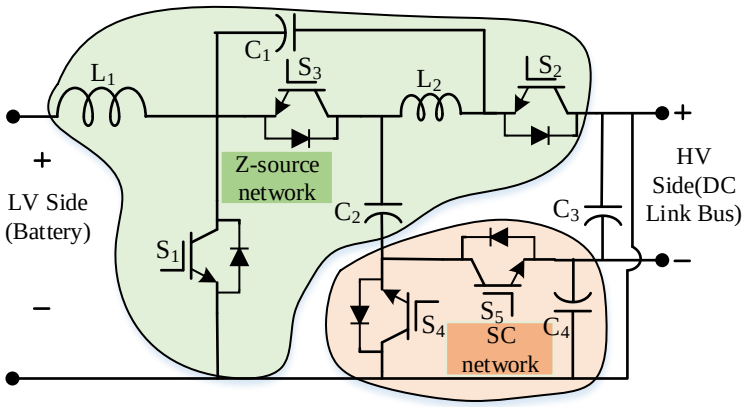


Fig. 2.28. Z-source inverter and switched capacitor (SC) based hybrid BDC unit.

Similarly, recent development in hybrid structure [38] is proposed by Y.Zhang *et.al*. and shown in Fig. 2.29. This structure is capable of providing sufficient voltage conversion factor and less voltage stress. However, high current stress, less efficiency, more component count and large input current ripple continues to be major problems of these type of converters.

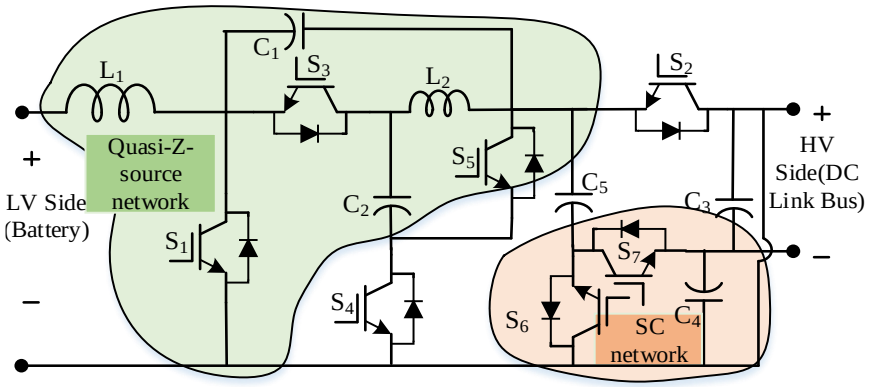
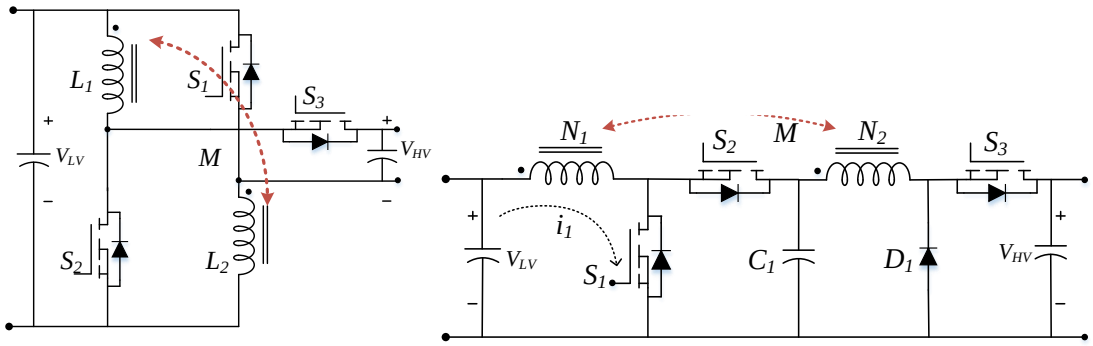


Fig. 2.28. Z-source inverter and switched capacitor (SC) based modified hybrid BDC unit.

2.3.6. Coupled Inductor based BDC

Coupled inductor-based circuits are useful for voltage lifting application. The winding turns ratio can be adjusted like transformer mutually coupled two windings can be used in combination with capacitor to achieve superior voltage lift. Coupled inductor based BDC circuits have two degree of freedom i.e., duty ratio and winding turn ratio like isolated converters. The basic coupled inductor based BDC circuit is proposed by [39] as shown in Fig. 2.29 (a). The circuit shown in Fig. 2.29(a) has two current paths but the switchings are not complementary thus this circuit have same input current ripple as inductors. However, current rating of the coupled inductor is smaller compared to circuit shown in Fig. 2.29(b). The voltage gain in both the operating modes are similar in these circuits. These circuits also have large voltage stress as well as current stress at the main

switches. The turns ratio can't be increased to four, it increases the core size as well as core, and copper loss of coupled inductor. This reduces the operating efficiency.



(a). (b)

Fig. 2.29. Z-source inverter and switched capacitor (SC) based modified hybrid BDC unit.

Therefore, to achieve sufficient voltage gain in both the operating modes of BDC using coupled inductor with less turns ratio is a major challenge. In last decade there are many coupled based bidirectional DC-DC converter topologies are proposed in this direction. Intermediate capacitor is used [40] to modify the base BDC circuit as shown in Fig. 2.29(b) which helps to increase the voltage gain. The circuit do not have parallel inductor paths which has the capability to share currents. The voltage gains as well as efficiency limitation of coupled inductor-based circuit is first modified by R. Y. Duan *et. al.* [41] where leakage energy is recovered through a clamped capacitor as shown in Fig. 2.30. This topology has inherently higher conversion ratios i.e. (n+2)/(1-d) and (d/n+2) in boost and buck mode respectively. This topology also has the capability to achieve soft switching.

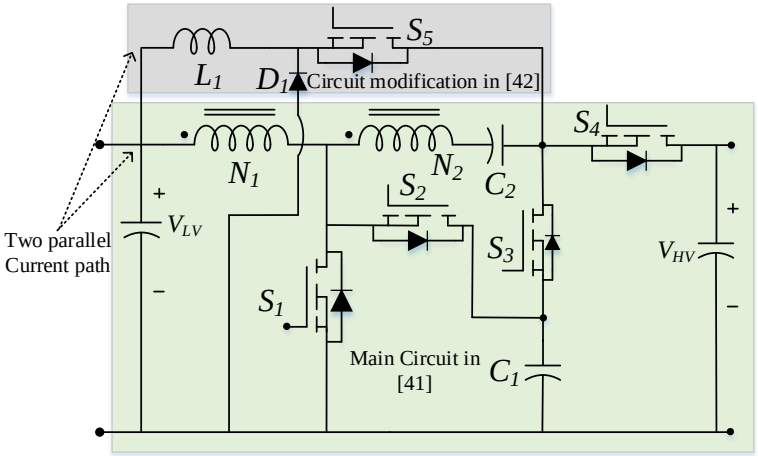


Fig. 2.30. Coupled inductor based high gain factor BDC.

The current sharing in buck mode is not achieved in this topology which was rectified by the same authors in [42]; where extra inductor is used in parallel to the coupled inductor

as shown in Fig. 2.30. This extra inductor is used in buck operation and remained unused in boost operation which left a research gap. Exactly same circuit like in [42] with one extra capacitor is proposed in [43] which provides same performance like original circuit. Circuit proposed by W. Hassan *et al*. [44] utilized the same structure [42] with a small modification by branching coupled inductor but reached to the same conversion factor as in the original circuit. M. Amir *et al*. [45] proposed same coupled inductor based BDC as previously proposed in [46]. Quasi resonant operation of same [42] BDC structure where coupled inductor is replaced by simple inductor is proposed [47] which is further generalized to make the topology suitable for high power application. But the basic circuit structure remains the same. H. Liu *et al*. [48] utilized the same structure but branching coupled inductor path leads to reduced voltage gain compared to the original circuit [42]. Reduction in input current ripple and current sharing is possible by using parallel structure as shown in Fig. 2.29 (b). Voltage gain can be improved using cascading structure [40] as shown in Fig. 3.30. However, the hard-switched cascading structure has less efficiency and do not have current sharing benefit. To achieve high conversion factor and soft switching using synchronous rectifier concept, secondary coupled inductor branch is used primarily in [42] as shown in Fig.2.31 (b). Later modification of the secondary coupled inductor branch position is adopted in [21] as shown in Fig. 2.31 (a) to achieve current sharing and higher gain, but fails to achieve it. Similarly, modification in coupled inductor branch position is mentioned in [44] as shown in Fig. 2.31 (b) to achieve same objectives but the performance parameter remains same as [42]. The BDC circuits proposed in [42], [21], [44] utilized n=2 turns ratio for achieving the required gain. Four active switches are used in [21], [44] for designing BDC and proposal [44] has better gain factor i.e. (n+2)/(1-D) and (D/n+2) compared to [21]. Therefore, utilizing only four switch and n=1 to achieve the same or better conversion factor is a design challenge of coupled inductor based non-isolated BDC. The BDC circuit proposed by Y. Yao *et.al* [49] used five active switches and a coupled inductor with four number of turns ratio. This circuit can be easily interfaced between 48V to 380V system. The soft switching of active switches enhances the average operating efficiency i.e. above 94% for all loading conditions. However, the operation of the circuit is quite complex.

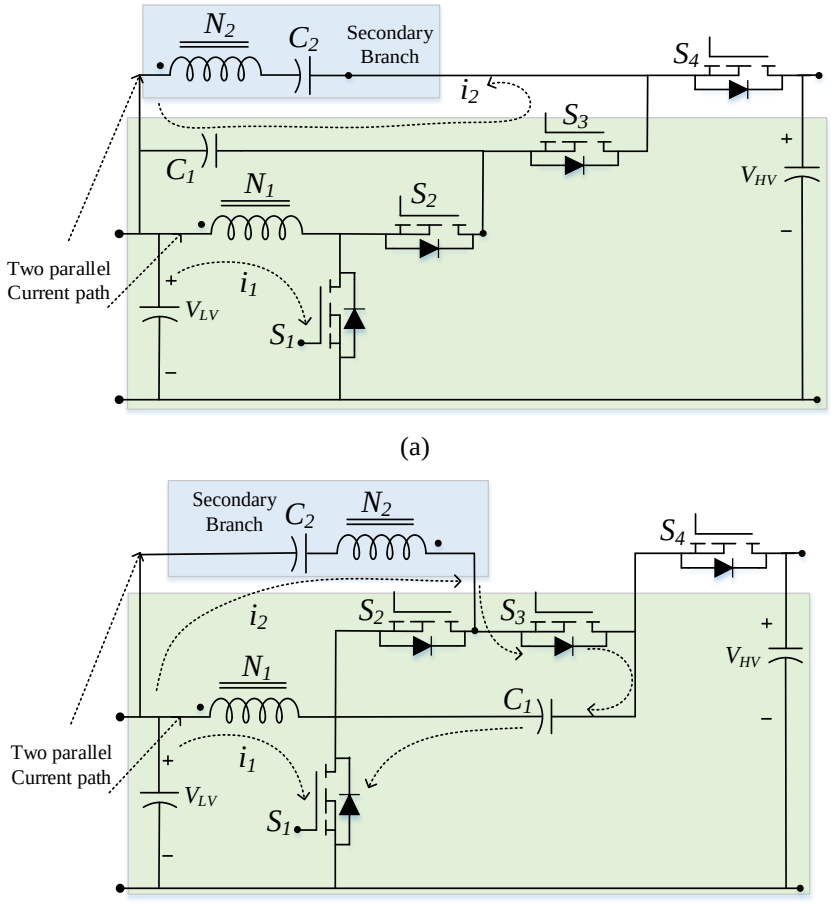


Fig. 2.30. BDC configurations using coupled inductor (a) Position changing secondary branch [21] of coupled inductor (b) Rearrangement of secondary branch [44] of coupled inductor.

2.3.6. Coupled Inductor and Switched Capacitor based BDC

The voltage conversion factor of non-isolated BDC can be improved within the operating duty ratio (0.4-0.6) and with a less number of winding turns ratio using a cascade hybrid structure of where coupled inductor circuit is cascaded with switched capacitor network [50]. The general circuit block diagram of these types of network is shown in Fig. 2.32.

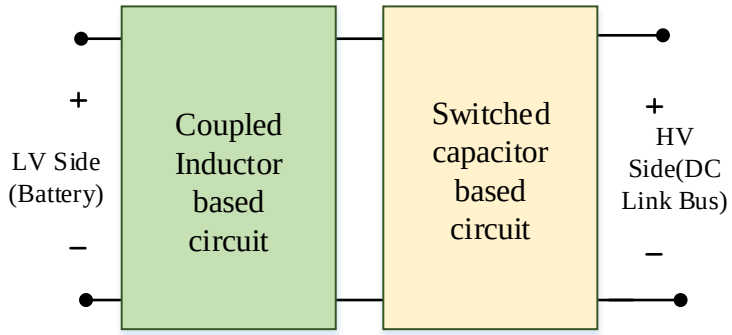


Fig. 2.32. High gain BDC configurations using cascaded coupled inductor and switched capacitor network.

LV side coupled inductor network can even be a combination of interleaved structure with coupled inductor. Similar design philosophy is adopted in [51] which provides good voltage conversion factor in both operation modes. The major problems of these network are (a) high component count, (b) increased control complexity and (c) difficulty in achieving soft switching operation of main and auxiliary switches. The current stress of LV side main switch is also large.

2.4. Common Issues with Non-Isolated BDCs for Interfacing Storage

In last decade, there has been many topological developments of non-isolated BDC found in the literature which has superior voltage conversion factors and less voltage stress in both operating modes. However, there are research opportunity based on the unsolved problems exists in non-isolated BDC for interfacing storage. These common issues are,

(a) To attain high voltage conversion factor, researchers have used many passive circuit components with auxiliary switches. This increases the peak current value of low voltage (LV) side main switch and creates large current stress especially at switch turn off time. To limit current stress of high gain non-isolated BDC circuits there is a requirement of less energy storing elements in circuit design. However, this reduces the voltage gain factors. Therefore, limiting current stress of LV side main switch with no compromise on voltage gain factor i.e., >10 for boost mode and <0.1 for buck mode within operating duty ratio range (0.4-0.6) is a major circuit development challenge.

(b) High efficiency operation is an important requirement of designed prototype. Switching loss is a considerable loss which needs to be eliminated or minimized to attain efficiency range greater than 90%. Generally auxiliary active clamp-based network is adopted to attain soft switching of main switches. But this creates control complexity and hard switching of auxiliary switches continues to be a major problem. Therefore, achieving soft switching of main and auxiliary switches are very essential. The main challenge is to design high gain BDC where all switches will be soft switched without using any auxiliary network.

(c) The high gain BDC has another major problem of large input current ripple because input current is same as inductor current ripple. Coupled inductor circuit has even more inductor ripple current and hence input current ripple. This large ripple current can’t be supplied by the storage and hence requires large input side filter capacitor. Interleaved circuit has promising solutions of having less input current ripple. There are two major

problems with interleaved high gain BDC, (i) large component count and (ii) narrow range of input ripple current reduction.

(d) Coupled inductor-based circuits are very useful in achieving large voltage gain within operating duty ratio. The number of winding turns of coupled inductor is large generally greater than two. This increases the core size as well as core loss. Therefore, designing high gain BDC for n=1 using coupled inductor is a topological development challenge.

2.5. Topological Requirements for Non-Isolated BDC for Storage Interface

There are some important characteristics requirements of BDC converter which are necessary for successful storage interface both for microgrid and EV. The characteristics are:

(a) High Efficiency operation in both boost and buck mode. (>91%)

(b) High voltage conversion factor in both operating modes and parallel path structure during buck operation.

(c) Less number of power electronics switches.

(d) Low voltage and current stress of main as well as auxiliary switches.

(e) Continuous and low input current ripple at LV side for wide duty ratio range.

(f) Low switching and conduction loss.

(g) High power density using GaN-FET based wide bandgap devices.

2.6. Summary

In this chapter several topologies of BDC are discussed with individual advantage and shortcomings. Isolated BDCs are highly efficient but has control complexity and soft switching of active switches are load dependent. Non-isolated BDC, on the other hand has simple control structure (voltage mode or current mode control) and large conversion factors. The operating efficiency is comparable with isolated counterpart. Coupled inductor based non-isolated circuits are capable to provide high conversion factor and performance is even better compared to isolated converter. The operating efficiency of the non-isolated BDCs can be enhanced utilizing GaN-FET based wide bandgap devices in place of Si-MOSFET. This also enables the designer to achieve high power density BDC.

2.7. References

[1] Sha D, Xu G. High-Frequency Isolated Bidirectional Dual Active Bridge DC–DC Converters with Wide Voltage Gain. Springer; 2018 May 17

[2] Martins LF. Modelling and Analysis of DC-DC Converters for Bidirectional EV Charging Applications (Doctoral dissertation, University of Sheffield) 2019.

[3] Stojadinović M. Bidirectional DC-DC Converters for MVDC Applications (Doctoral dissertation, ETH Zurich) 2020.

[4] Zhang J. Bidirectional DC-DC power converter design optimization, modeling and control (Doctoral dissertation, Virginia Tech). 2008.

[5] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen and J. W. Kolar, "Switching control strategy for full ZVS soft-switching operation of a Dual Active Bridge AC/DC converter," 2012 Twenty-Seventh Annual *IEEE Applied Power Electronics Conference and Exposition (APEC*), 2012, pp. 1048-1055, doi: 10.1109/APEC.2012.6165948.

[6] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063-8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.

[7] van Hoek, Hauke, Jan Abraham Ferreira, and Rik W. de Doncker. Design and operation considerations of three-phase dual active bridge converters for low-power applications with wide voltage ranges. No. RWTH-2017-02955. Institut für Stromrichtertechnik und Elektrische Antriebe, 2017.

[8] P. He and A. Khaligh, "Comprehensive Analyses and Comparison of 1 kW Isolated DC–DC Converters for Bidirectional EV Charging Systems," in *IEEE Transactions on Transportation Electrification*, vol. 3, no. 1, pp. 147-156, March 2017, doi: 10.1109/TTE.2016.2630927.

[9] Bo Yang, “Topology investigation of front-end DC/DC converter for distributed power system,” Ph.D. dissertation, Dept. Elect. Eng., Virginia Tech, Blacksburg, VA, USA, 2003.

[10] S. Chakraborty and S. Chattopadhyay, "Analysis and comparison of voltage-source and current-source asymmetric dual-active half-bridge converters," *2014 IEEE Energy Conversion Congress and Exposition* (ECCE), 2014, pp. 2072-2079, doi: 10.1109/ECCE.2014.6953676.

[11] Bhatt, Kunalkumar, Ram Avtar Gupta, and Nitin Gupta. "Design and development of isolated snubber based bidirectional DC–DC converter for electric vehicle applications." *IET Power Electronics* 12, no. 13 (2019): 3378-3388.

[12] T. Wu, Y. Chen, J. Yang and C. Kuo, "Isolated Bidirectional Full-Bridge DC–DC Converter With a Flyback Snubber," in *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1915-1922, July 2010, doi: 10.1109/TPEL.2010.2043542.

[13] X. Sun, X. Wu, Y. Shen, X. Li and Z. Lu, "A Current-Fed Isolated Bidirectional DC–DC Converter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6882-6895, Sept. 2017, doi: 10.1109/TPEL.2016.2623306.

[14] Ha, Sung Pil, Jung Hyo Lee, Jung Pill Hwang, Jun Hyuk Choi, and Chung Yuen Won. "Two phase interleaved bidirectional DC-DC converter for electric vehicle using variable DC-link voltage." In *2012 IEEE Vehicle Power and Propulsion Conference*, pp. 748-752. IEEE, 2012.

[15] C. Lai, Y. Cheng, M. Hsieh and Y. Lin, "Development of a Bidirectional DC/DC Converter With Dual-Battery Energy Storage for Hybrid Electric Vehicle System," in *IEEE Transactions on Vehicular Technology*, vol. 67, no. 2, pp. 1036-1052, Feb. 2018, doi: 10.1109/TVT.2017.2763157.

[16] Z. Zhang, Z. Wu, S. Xie, X. Ma, J. Xu and M. Liu, "A soft-switching current-fed isolated bidirectional dc-dc converter with low circulating power and easy-implemented control strategy," 2019 *IEEE Energy Conversion Congress and Exposition* (ECCE), 2019, pp. 1310-1314, doi: 10.1109/ECCE.2019.8912905.

[17] P. Xuewei and A. K. Rathore, "Current-Fed Soft-Switching Push–Pull Front-End Converter-Based Bidirectional Inverter for Residential Photovoltaic Power System," in *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 6041-6051, Nov. 2014, doi: 10.1109/TPEL.2014.2301495.

[18] A. K. Rathore, D. R. Patil and D. Srinivasan, "Non-isolated Bidirectional Soft-Switching Current-Fed LCL Resonant DC/DC Converter to Interface Energy Storage in DC Microgrid," in *IEEE Transactions on Industry Applications*, vol. 52, no. 2, pp. 1711-1722, March-April 2016, doi: 10.1109/TIA.2015.2498127.

[19] K. Tytelmaier, O. Husev, O. Veligorskyi and R. Yershov, "A review of non-isolated bidirectional dc-dc converters for energy storage systems," 2016 II International Young Scientists Forum on Applied Physics and Engineering (YSF), 2016, pp. 22-28, doi: 10.1109/YSF.2016.7753752.

[20] Y. Du, X. Zhou, S. Bai, S. Lukic and A. Huang, "Review of non-isolated bi-directional DC-DC converters for plug-in hybrid electric vehicle charge station application at municipal parking decks," 2010 *Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition* (APEC), 2010, pp. 1145-1151, doi: 10.1109/APEC.2010.5433359.

[21] M. Das and V. Agarwal, "Design and Analysis of a High-Efficiency DC–DC Converter With Soft Switching Capability for Renewable Energy Applications Requiring High Voltage Gain," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2936-2944, May 2016, doi: 10.1109/TIE.2016.2515565.

[22] E. H. Ismail, "Bridgeless SEPIC Rectifier With Unity Power Factor and Reduced Conduction Losses," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 4, pp. 1147-1157, April 2009, doi: 10.1109/TIE.2008.2007552.

[23] Zhang, Hailong, Yafei Chen, Sung-Jun Park, and Dong-Hee Kim, "A Family of Bidirectional DC–DC Converters for Battery Storage System with High Voltage Gain" *Energies* vol. 12, no. 7: pp. 1289-1299, Feb. 2019. https://doi.org/10.3390/en12071289

[24] I. Kim, S. Paeng, J. Ahn, E. Nho and J. Ko, "New Bidirectional ZVS PWM Sepic/Zeta DC-DC Converter," *2007 IEEE International Symposium on Industrial Electronics*, 2007, pp. 555-560, doi: 10.1109/ISIE.2007.4374656.

[25] Fardoun, A. A., Ismail, E. H., Sabzali, A. J., & Al-Saffar, M. A, "Bidirectional converter for high-efficiency fuel cell powertrain" *Journal of Power Sources*, Vol. 249, no. pp. 470-482. March 2014.

[26] M. P. Hirth, R. Gules and C. H. Illa Font, "A Wide Conversion Ratio Bidirectional Modified SEPIC Converter With Nondissipative Current Snubber," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1350-1360, April 2021, doi: 10.1109/JESTPE.2020.2966410.

[27] Abramovitz, Alexander; Yao, Jia; Smedley, Keyue: 'Derivation of a family of high step-up tapped inductor SEPIC converters', *Electronics Letters*, vol. 50, no. 22, pp. 1626-1628, March 2014. DOI: 10.1049/el.2014.2190.

[28] Wang, Feng, Yutao Luo, Hongluo Li, and Xiaotong Xu. "Switching characteristics optimization of two-phase interleaved bidirectional DC/DC for electric vehicles." Energies 12, no. 3 (2019): 378.

[29] Banaei, M. R., Zoleikhaei, A., & Sani, S. G. (2019). Design and implementation of an interleaved switched-capacitor dc-dc converter for energy storage systems. Journal of Power Technologies, 99(1), 1.

[30] Y. Zhang, Y. Gao, L. Zhou and M. Sumner, "A Switched-Capacitor Bidirectional DC–DC Converter With Wide Voltage Gain Range for Electric Vehicles With Hybrid Energy Sources," in *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9459-9469, Nov. 2018, doi: 10.1109/TPEL.2017.2788436.

[31] H. Zhang, Y. Chen, C. -S. Shin, S. -J. Park and D. -H. Kim, "Transformer less Bidirectional DC-DC Converter for Battery Storage System with High Voltage Gain," 2019 *10th International Conference on Power Electronics and ECCE Asia* (ICPE 2019 - ECCE Asia), 2019, pp. 2376-2381, doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8796887.

[32] Y. Zhang, Y. Gao, J. Li and M. Sumner, "Interleaved Switched-Capacitor Bidirectional DC-DC Converter With Wide Voltage-Gain Range for Energy Storage Systems," in *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3852-3869, May 2018, doi: 10.1109/TPEL.2017.2719402.

[33] Y. Zhang, W. Zhang, F. Gao, S. Gao and D. J. Rogers, "A Switched-Capacitor Interleaved Bidirectional Converter With Wide Voltage-Gain Range for Super Capacitors in EVs," in *IEEE*

Transactions on Power Electronics, vol. 35, no. 2, pp. 1536-1547, Feb. 2020, doi: 10.1109/TPEL.2019.2921585.

[34] S. Xiong and S. Tan, "Cascaded High-Voltage-Gain Bidirectional Switched-Capacitor DC–DC Converters for Distributed Energy Resources Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1220-1231, Feb. 2017, doi: 10.1109/TPEL.2016.2552380.

[35] L. Sun, F. Zhuo, F. Wang and T. Zhu, "A novel topology of high voltage and high power bidirectional ZCS DC-DC converter based on serial capacitors," *2016 IEEE Applied Power Electronics Conference and Exposition* (APEC), 2016, pp. 810-815, doi: 10.1109/APEC.2016.7467964.

[36] Fang Zheng Peng, "Z-source inverter," in IEEE Transactions on Industry Applications, vol. 39, no. 2, pp. 504-510, March-April 2003, doi: 10.1109/TIA.2003.808920.

[37] Y. Zhang, Q. Liu, J. Li, and M. Sumner, "A common ground switched quasi-Z-source bidirectional dc-dc converter with wide-voltage-gain range for EVs with hybrid energy sources," *IEEE Trans. Ind. Electron*., vol. 65, no. 6, pp. 5188–5200, Jun. 2018.

[38] Y. Zhang, Q. Liu, Y. Gao, J. Li and M. Sumner, "Hybrid Switched-Capacitor/Switched-Quasi-Z-Source Bidirectional DC–DC Converter With a Wide Voltage Gain Range for Hybrid Energy Sources EVs," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2680-2690, April 2019, doi: 10.1109/TIE.2018.2850020.

[39] L. Yang, and T. Liang, "Analysis and implementation of a novel bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 422–434, Jan. 2012

[40] T. Liang, H. Liang, S. Chen, J. Chen, and L. Yang, "Analysis, design and implementation of a bidirectional double-boost DC-DC converter," *IEEE Trans. Ind. Appl*., vol. 50, no. 6, pp. 3955–3962, Nov./Dec. 2014.

[41] R. Duan, and J. Lee, "High-efficiency bidirectional DC-DC converter with coupled inductor," *IET Power Electron*, vol. 5, no. 1, pp. 115–123, Jan. 2012.

[42] R. Wai, R. Duan, and K. Jheng, "High-efficiency bidirectional dc-dc converter with high-voltage gain," *IET Power Electron*, vol. 5, no. 2, pp. 173–184, Feb. 2012.

[43] Y. Zhang, H. Liu, J. Li, and M. Sumner, "A low-current ripple and wide voltage-gain range bidirectional DC–DC converter with coupled inductor," *IEEE Trans. Power Electron*., vol. 35, no. 2, pp. 1525–1535, Feb. 2020.

[44] W. Hassan, J. L. Soon, D. D. Lu, and W. Xiao, "A high conversion ratio and high-efficiency bidirectional DC-DC converter with reduced voltage stress," *IEEE Trans. Power Electron*., vol. 35, no. 11, pp. 11827–11842, Nov. 2020

[45] M. Aamir, S. Mekhilef, and H. Kim, "High-Gain zero-voltage switching bidirectional converter with a reduced number of switches," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 62, no. 8, pp. 816–820, Aug. 2015

[46] R. Wai, R. Duan, and K. Jheng, “High-efficiency bidirectional dc-dc converter with high-voltage gain,” *IET Power Electron*, vol. 5, no. 2, pp. 173–184, Feb. 2012

[47] H. Moradisizkoohi, N. Elsayad, and O. A. Mohammed, “Experimental demonstration of a modular, quasi-resonant bidirectional DC–DC converter using GaN switches for electric vehicles,” *IEEE Trans. Ind. Appl*., vol. 55, no. 6, pp. 7787–7803, Nov./Dec. 2019.

[48] H. Liu, L. Wang, Y. Ji, and F. Li, “A novel reversal coupled inductor high-conversion-ratio bidirectional DC–DC converter, ”*IEEE Trans. Power Electron*., vol. 33, no. 6, pp. 4968–4979, Jun. 2018.

[49] J. Yao, A. Abramovitz and K. Ma Smedley, "Steep-Gain Bidirectional Converter With a Regenerative Snubber," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6845-6856, Dec. 2015, doi: 10.1109/TPEL.2015.2395455.

[50] Y. Zhang, H. Liu, J. Li and M. Sumner, "A Low-Current Ripple and Wide Voltage-Gain Range Bidirectional DC–DC Converter With Coupled Inductor," in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1525-1535, Feb. 2020, doi: 10.1109/TPEL.2019.2921570.

[51] H. Bahrami, S. Farhangi, H. Iman-Eini, and E. Adib, “A new interleaved coupled-inductor nonisolated soft-switching bidirectional DC–DC converter with high voltage gain ratio,” *IEEE Trans. Ind. Electron*., vol. 65, no. 7, pp. 5529–5538, Jul. 2018.

Chapter-3

Generalized Switch Current Stress Reduction Technique for Non-Isolated BDC

Coupled inductor based high gain non-isolated bidirectional converter suffers from high switch current stress especially at low voltage side main switch. This phenomenon is also true for other non-coupled inductor based high gain non-isolated BDC converters. In this chapter low voltage side main switch current stress reduction technique is discussed. This circuit design technique can be generalized and applied to existing topologies after modification. This technique ensures low current stress al low voltage side. In this chapter boost stage design of BDC using the proposed circuit technique is discussed in details.

3. Generalized Switch Current Stress Reduction Technique for Non-Isolated BDC

3.1. Introduction

Topology derivation for boost stage of BDC is very important because the voltage gain in this stage should be sufficient (>10) to interface low voltage (LV) energy storage [1]-[3] to high voltage DC link within operating duty ratio range from 0.4 to 0.6. Conventional boost converters are not suitable in these applications as extreme high duty-ratio is required [4] to meet the high gain, which increases the conduction loss. Again, at high duty ratio, the problem of diode reverse recovery and electromagnetic interference (EMI) increases significantly [5]. Therefore, to achieve high step-up ratio and efficiency at low duty cycle, there are many boosting techniques like switched capacitor, voltage multiplier cell, and interleaved structures available in literature [6-7]. However, all these voltage lifting techniques suffer from large number of capacitors and power diode usage, which increases the loss and degrades efficiency. Coupled inductor based boosting technique [8-9] has emerged utilizing magnetic coupling and has promising two-degree solution of voltage lifting. But the leakage inductance creates voltage spikes and increases the switch voltage stress. Active and passive clamp based coupled inductor boost converter circuit eliminates voltage spikes due to leakage inductance [10-11]. The application of voltage multiplier cell and switched capacitor cell in coupled inductor-based boost converter are also found in literature to minimize the leakage inductance effect with further enhancement in voltage gain [12-13]. Interleaving technique in coupled inductor-based boost converter minimize the input current ripple [14]. Therefore, various high step-up coupled inductor-based boost converter topologies evolved which ensures high efficiency operation with low input current ripple [15-21]. However, these converters suffer from high switch voltage stress as well as current stress. The peak current as well as turn off current of LV main switch is very large. This restricts practical application to storage interface in microgrid or in EV.

3.2. Proposed Switch Current Stress Reduction Network

Achieving high voltage gain in boost stage using coupled inductor-based circuit requires minimum two parallel current paths during main LV switch ON operation. This allows to store sufficient energy during switch ON time and helps to achieve high voltage gain. For

example, the coupled inductor-based boost DC-DC converter proposed by Yifei Zheng *et.al* [22] as shown in Fig. 3.1 has two parallel paths during LV main switch S_1 ON time. During ON time of S_1 large energy is stored in primary inductor which is later used by secondary coupled inductor circuit to lift the output voltage.

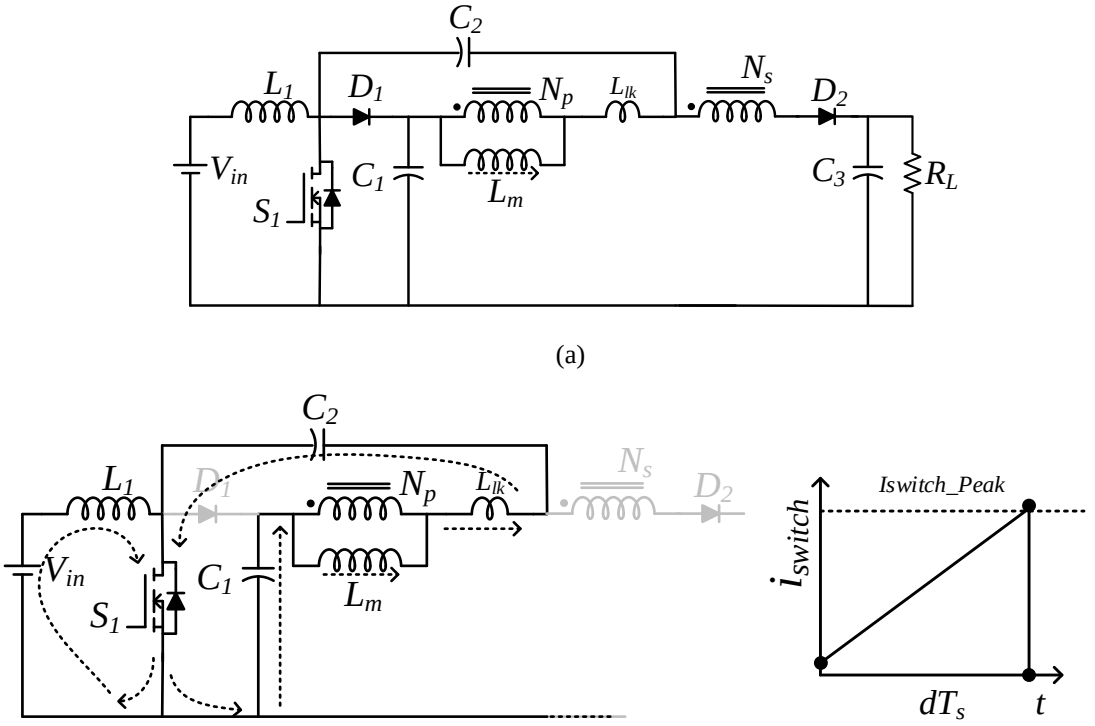


Fig. 3.1. (a) The coupled inductor boost circuit topology [22]. (b) Circuit at switch ON time (c) Switch current waveform.

Again, another example of implementation of the proposed method in a coupled inductor boost DC-DC converter proposed by Y. Hsieh *et.al* [21] is presented here, which uses extra capacitors to lift the input dc voltage. During switch S_1 ON time, two loop current paths are used similar to [22] as shown in Fig. 3.2 to achieve the high voltage gain.

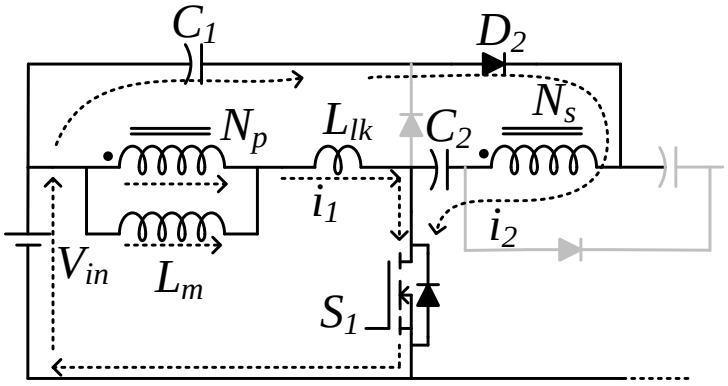
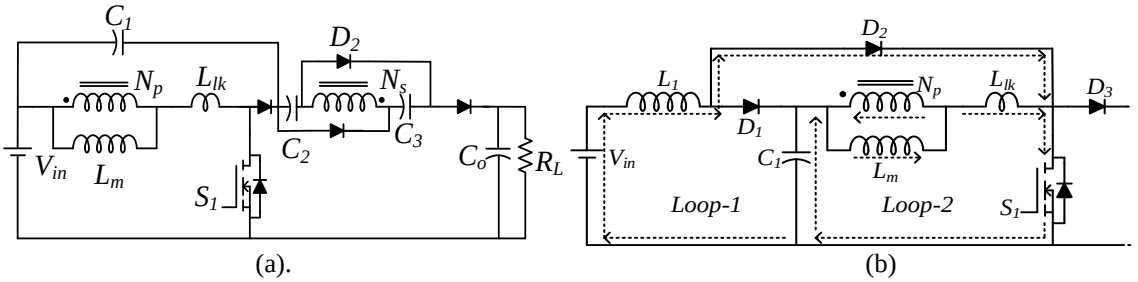


Fig. 3.2. Switch "ON" time circuit proposed by Y. Hsieh *et.al* [21].

Converter proposed by Yi-Ping Hsieh *et al* [15] and S.-M. Chen *et al.* [19] also have two current paths which is shown in Fig. 3.3 (a) and Fig. 3.3 (b)



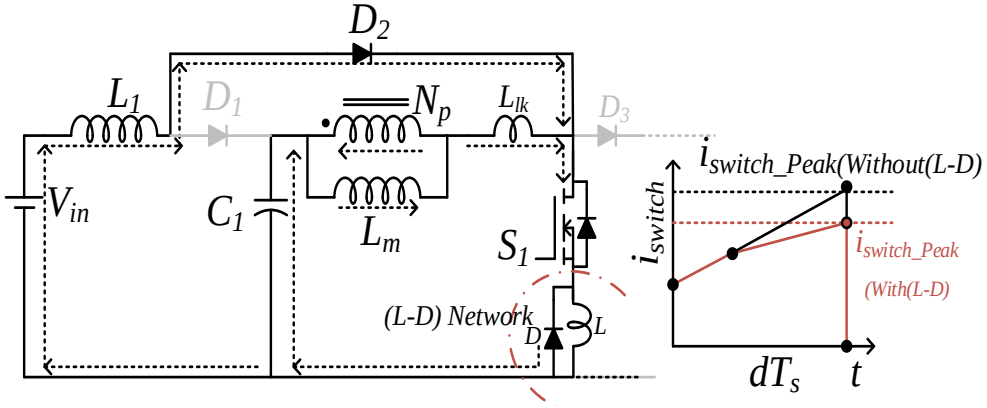
(a). (b)

Fig. 3.3. (a) Coupled inductor boost circuit topology [15] (b) Converter configuration of (a) switch '*ON*' time circuit by S.-M. Chen *et al.* [19]

Similarly, there are other examples [16], [17], [19] and [25] where usage of number of current loops at LV side to achieve high voltage gain is greater than one. All these topologies use two current paths during switch ON time to store energy either in inductor or in capacitor or both. Even though the rms current is small, the cumulative current through the switch creates extremely high peak current at the beginning or at the end of the turn ON time of the switch. This creates large switch current stress at the end of switch ON time as shown in Fig. 3.1 (c). Such high current stress is a common problem to all high step-up coupled inductor boost converters [22]. This is one of the major reasons of non-reliable converter operation and fault. In addition, this requires an expensive high current rating device.

3.2.1. Proposed L-D Based Network

Considering the problem of large current stress of LV side main switch, an extra L-D network proposed by T.R. Choudhury *et.al* [24] is connected in series with main switch as shown in Fig. 3.4 (a). The peak switch current at the end of the switch ON time reduces significantly, as shown in Fig. 3.4 (b).



(a). (b)

Fig. 3.4. Circuit modification by (a) L-D based network by TR Choudhury *et al.* [24] (b) LV main switch current.

Multiple current loop paths are required during main LV switch ON time in coupled inductor based high gain boost converter to achieve sufficient voltage gain. There is no technical problem with multiple loop current paths during ON time except high magnitude peak current at LV side main switch. Converter proposed in [19] utilizes two current loop paths as shown in Fig. 3.4 (b) to achieve high voltage gain. But during ON time, the switch current is the summation of two individual loop current as shown in Fig. 3.5 and peak switch current is large.

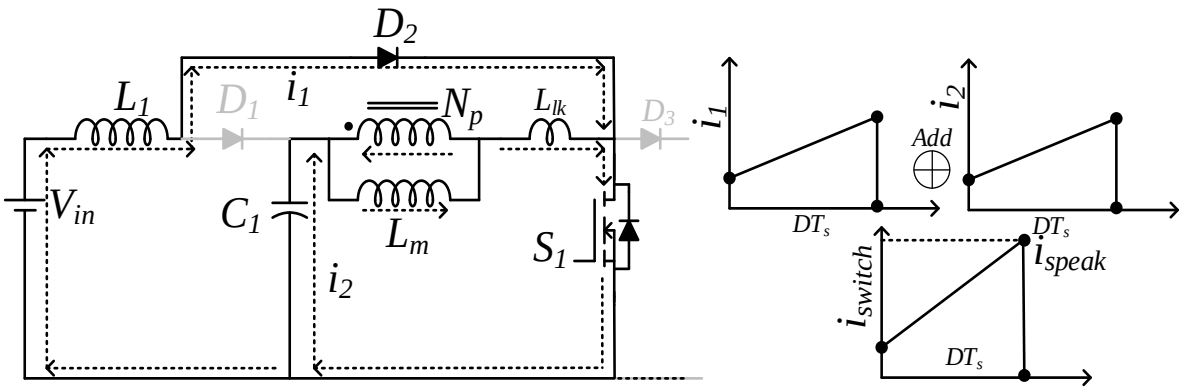
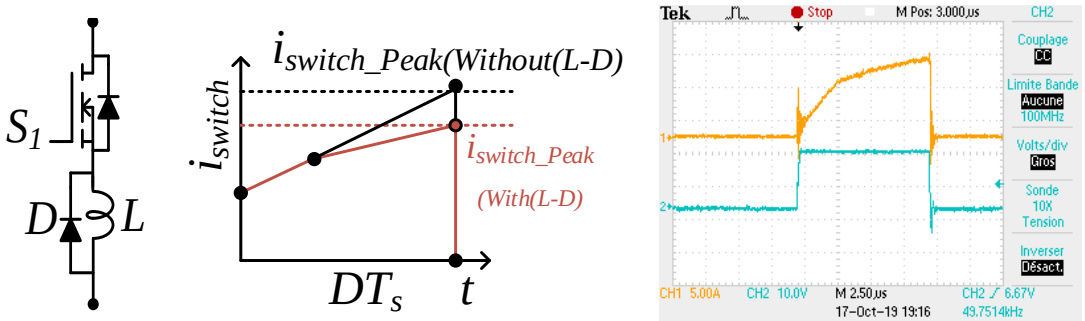


Fig. 3.5. Switch "ON" time circuit proposed by S.M. Chen *et.al* [19] and current paths

Increasing the resultant loop inductance by increasing magnetizing inductance value the fast rise of current slope can be restricted, but this requires bulky coupled inductor. This increases coupled inductor size with associated core and copper loss. Inductor diode (L-D) branch can be connected in series with main switch as shown in Fig. 3.6 (a) for restricting the current slope.



(a) (b) (c)

Fig. 3.6. (a) main switch with L-D network (b) switch current with and without L-D network (c) Typical switch current waveform using L-D based network.

The modified inductor current slope using L-D network is less as mentioned in equation (3.1).

$$\frac{di_{switch}}{dt} = \frac{v_{in}}{L_m} > \frac{v_{in}}{L_m + L_d} = \frac{di_{switch\_LD}}{dt} \tag{3.1}$$

This less slope value reduces LV side main switch current stress as shown in Fig. 3.6 (b) and 3.6(c). The extra inductance required in the L-D branch is very small [24] and it is feasible solution which can be applied to all high gain boost converter. The major concern of this solution is that the energy stored in the extra inductor is dissipated as heat due to conduction of antiparallel diode of L-D branch during main switch OFF time. Thus, voltage gain as well as efficiency of the converter reduces. This creates a research gap to reduce the LV side main swich current stress without sacrificing on voltage gain and efficiency. In this thesis a generalized half cycle resonating branch utilizing coupled inductor is proposed to minimize switch current stress. No extra components are used in modifying the coupled inductor circuit topology. This technique requires modification in existing topologies in literature.

3.2.2. Proposed Half Cycle Resonating Branch

Conceptually the LV side main switch current stress can be reduced by modifying the loop current shapes. For example, the ON time current loop shapes of [19] can be modified as shown in Fig. 3.7.

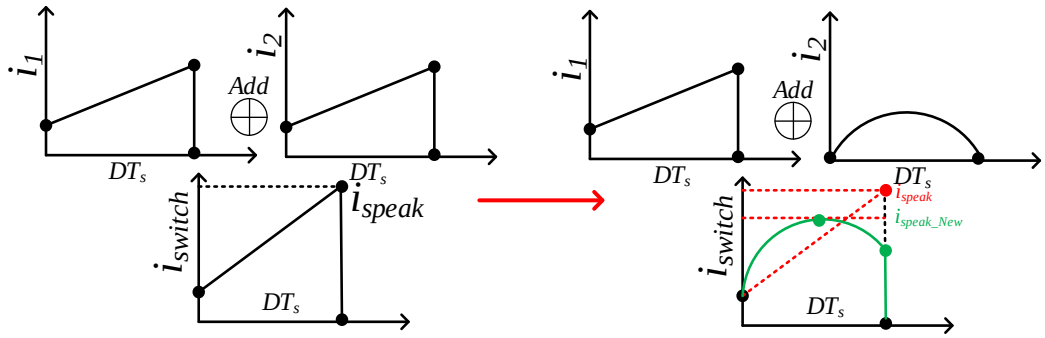


Fig. 3.7. Reshaping of loop currents of converter to reduce the resultant current stress

Bending of second loop current can be ahieved by half cycle resonating branch as shown in Fig. 3.8 (a).

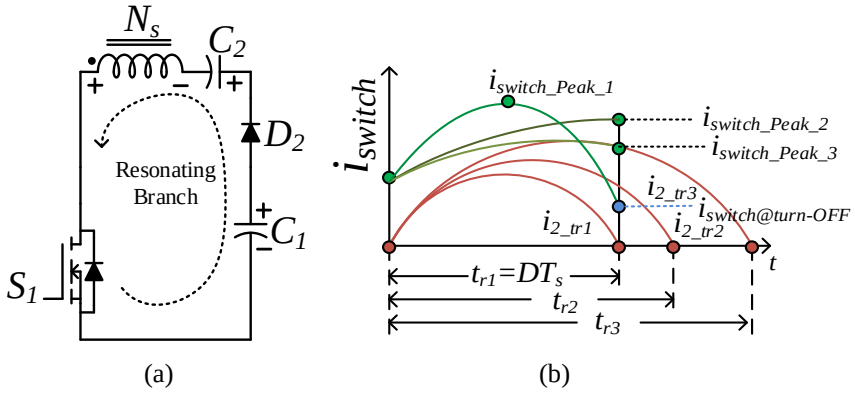


Fig. 3.8. (a) half cycle resonating branch (b) resultant LV side main switch current

The half cycle resonating branch can be effectively applied to shape the second loop current, so that the peak switch current can be minimized as shown in Fig. 3.8 (b). For this capacitor used in second loop can be utilized. Half cycle resonating branch is used to store energy during ON time. In this approach, the second loop current follow sinusoidal pattern and its maximum value depends on the values of loop elements. Two capacitors (C_1, C_2), diode (D_2), switch (S_1) and coupled inductor secondary inductance (L_2) during ON time forms a resonating branch. Capacitor C_1 make diode D_2 forward biased assisted by secondary inductance (L_2) and capacitor C_2 stores energy. This branch continues to circulate current through the main switch till diode D_2 is forward biased or main switch is ON. The current equation i_2 can be derived as,

$$i_2 = v_{C_1}\sqrt{\frac{C_{eq}}{L_2}}\sin(\omega_r t) \text{ where } C_{eq} = \frac{C_1 C_2}{C_1 + C_2}, \tag{3.2}$$

$$T_r = \frac{1}{\omega_r} = 2\pi\sqrt{L_2 C_{eq}} \text{ and } t_r = \pi\sqrt{L_2 C_{eq}}$$

3.3. Topology Derivation of the Boost Stage using Proposed Half Cycle Resonating Branch

Half cycle resonating branch can be used effectively to modify the existing topologies. From this modification, one unified new circuit can be derived. As an example, the coupled inductor-based boost DC-DC converter proposed by Yifei Zheng *et.al* [22] as shown in Fig. 3.9 is taken here to demonstrate the application of the technique. The converter [22] have advantages like high voltage gain, low switching stress, and higher efficiency but it has large switch peak current. During ON time of S_1, large energy is stored in primary inductor which is later used by secondary of coupled inductor circuit to lift the output voltage.

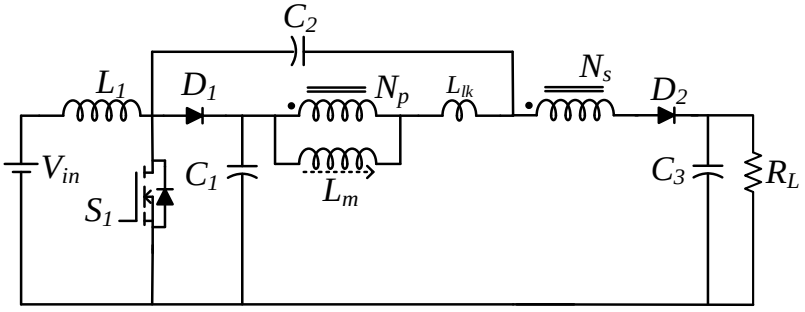


Fig. 3.9. The coupled inductor boost circuit topology [22].

Capacitor (C_1) in Fig. 3.9 is just holding the first stage lifted voltage i.e. (V_{in}/(1-D)) which is later used by coupled inductor circuit to lift the voltage at C_3. Capacitor C_2 is used to add more voltage gain by taking the energy from input inductor L_1 at switch OFF time of

S_1. Instead of using this circuit, modification of topology using the proposed method is possible as shown in Fig. 3.10 to reduce peak current of switch S_1 without sacrificing voltage gain.

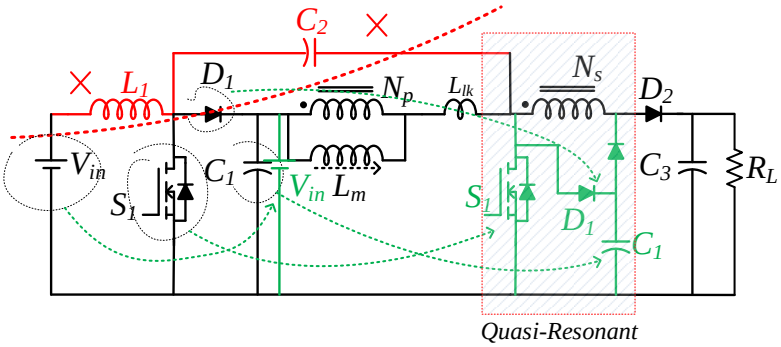
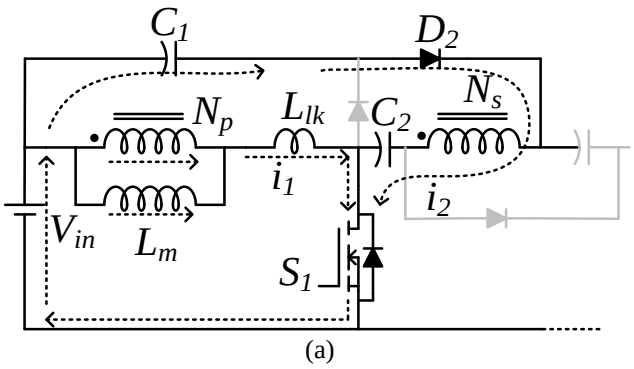
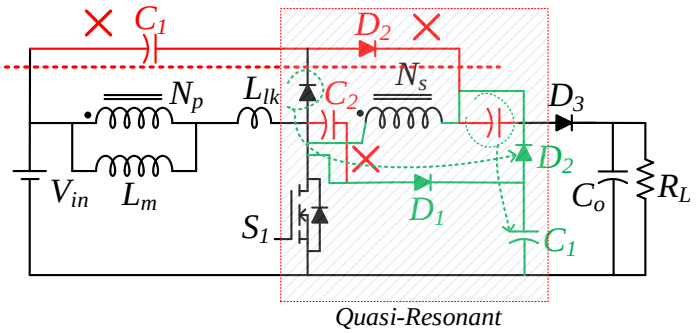


Fig. 3.10. Circuit modification using proposed technique.

Similarly, another example of implementation of the proposed method in a coupled inductor-based boost DC-DC converter proposed by Y. Hsieh *et.al* [21] is presented here, which uses extra capacitors to lift the input dc voltage. During switch ON time of S_1 two loop current paths are used similar to [22] as shown in Fig. 3.11(a) to achieve the high voltage gain. The proposed technique can also be applied to the converter just by rearranging the circuit elements as shown in Fig. 3.11 (b). The modified circuit is also able to lift the input voltage just like the existing one but switch current reduction is possible using half cycle resonating branch.



(a)



(b)

Fig. 3.11. (a) Switch ON time circuit proposed by Y. Hsieh *et.al* [21] (b) Circuit modification using proposed technique.

Converter proposed by Yi-Ping Hsieh *et al* [15] can also be modified and proposed technique can be applied as shown in Fig. 3.12 (a) and Fig. 3.12 (b) respectively.

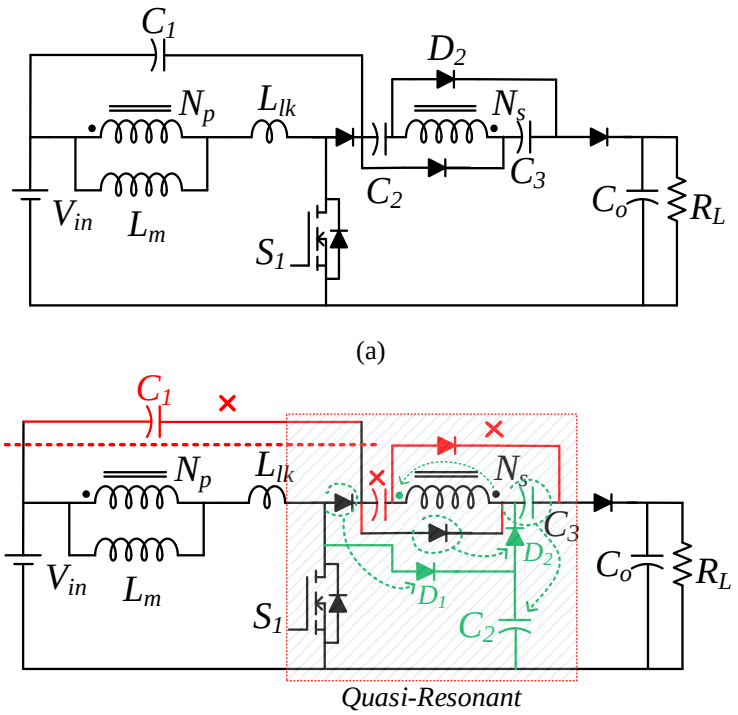


Fig. 3.12. (a) Coupled inductor boost circuit topology [15] (b) Circuit modification using proposed technique.

Similarly, converters proposed in [16], [17], [19] and [25] can be topologically modified and same operation can be adopted to minimize switch current stress of LV side main switch S_1.

3.4. Proposed Generalized Boost Topology

After applying half cycle resonating branch in existing topologies as explained in the previous section a generalized novel boost stage is derived which is shown in Fig. 3.13 (b) whereas LV side main switch S_1 ON time circuit is shown in Fig. 3.13(a).

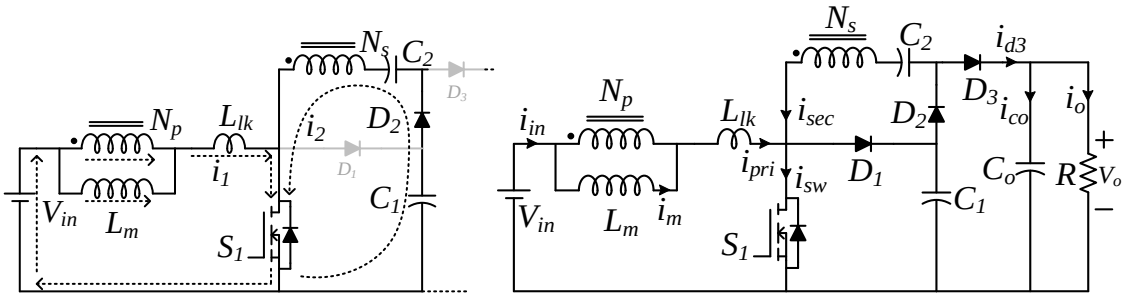


Fig. 3.13. (a) LV side main switch ON circuit (b) Proposed coupled-inductor based boost (PCB) converter using half cycle resonating branch.

3.4.1. Operating Principle in Continuous Conduction Mode

The proposed converter as shown in Fig. 3.13 (b) comprises of one coupled inductor, three diodes, three capacitors and a power electronic switch. The coupled inductor is modelled as ideal transformer with magnetizing inductance L_m and leakage inductance L_{lk}. In order to simplify the analysis, the following conditions are assumed.

(a) The capacitor voltage ripple is considered to be small and negligible.

(b) All power electronics switches are considered to be ideal.

(c) The coefficient of coupling (k) of coupled inductor is considered as $\frac{L_m}{L_m + L_{lk}}$ and the turns ratio is $n = \frac{N_s}{N_p}$

The analysis of the converter is done in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are discussed below.

CCM Operation

The operating principle of the proposed converter is divided into four modes as per power flow in CCM. Fig. 3.14 shows the key waveforms of the proposed converter and Fig. 3.15 indicates the circuit diagram of each mode.

Mode 1 [t_0-t_1]: In this mode the main switch (S_1) is ON and capacitor C_1 is discharging through D_2, C_2, and S_1. The discharging current is i_{sec} as shown in Fig. 3.15 (a). The current will circulate till D_2 is in forward biased. The leakage inductance is negligible compared to magnetizing inductance. The constant load current is supplied by the output capacitor C_0. The magnetizing current (i_m) increases gradually. The switch current is the summation of discharging current (i_{d2}) and primary current (i_{pri}) as shown in Fig. 3.15 (a). In this mode the voltage and current equations can be written as,

$$v_{in} = v_{Lm} + v_{lk} \tag{3.3}$$

$$v_{c_2} = n v_{Lm} + v_{c_1} \tag{3.4}$$

$$-i_{c_1} = i_{c_2} = i_{sec} = v_{c_1}\sqrt{\frac{C_{eq}}{L_2}}\sin(\omega_r t) \tag{3.5}$$

Where, $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$, $T_r = \frac{1}{\omega_r} = 2\pi\sqrt{L_2 C_{eq}}$ and $t_r = \pi\sqrt{L_2 C_{eq}}$

$$i_{in} = i_{primary}\,,\ -i_{c_0} = i_0 \tag{3.6}$$

$$i_{sw} = i_{pri} + i_{sec} = i_m + (n+1)i_{sec} \tag{3.7}$$

Mode 2 [t_1-t_2]: At t_1, the main switch (S_1) is OFF. The polarity of V_{lk} changes which make D_1 forward bias and energy stored in the leakage inductance (L_{lk}) is transferred to capacitor C_1 in this mode which is shown in Fig. 3.15(b). The load current is supplied by the output capacitor C_0. In this mode the voltage across C_2 is constant.

$$v_{in} + v_{Lm} + v_{lk} = v_{c_1} \tag{3.8}$$

The time of released energy [2] $t_{c1}=t_3-t_1=2(1-D)/(n+1)$ (3.9)

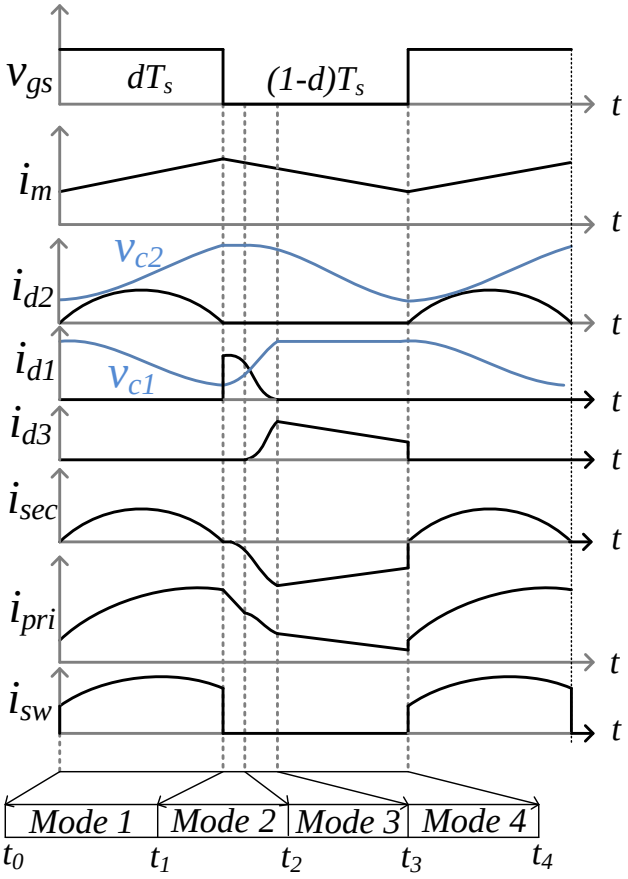


Fig. 3.14. Key waveform of proposed converter in CCM.

Mode 3 [t_2-t_3]: This mode starts after t_2. The current through diode D_1 starts decreasing and D_3 is forward biased in this mode. The output capacitor C_0 is in charging mode. Magnetizing current starts decreasing, D_2 is reversed biased and Capacitor C_2 starts discharging through D_3 to the load. Voltage across capacitor C_1 is rising till D_1 is forward biased. The voltage and current equations in this mode which is shown in Fig. 3.15 (c) are

$$v_{in} + v_{Lm} + v_{lk} = v_{c_1} \tag{3.10}$$

$$v_{c_1} + nv_{Lm} + v_{c_2} = v_0 \tag{3.11}$$

$$i_{d_3} = i_{sec} = i_{c_0} + i_0 \tag{3.12}$$

$$i_{pri} = i_{sec} + i_{c_1} \tag{3.13}$$

Mode 4 [t_3-t_4]: This mode starts after t_3 as shown in Fig. 3.15(d). In this mode diode D_1 is reverse biased. Capacitor (C_0) is in charging condition. Magnetizing current (i_m) falls at a constant rate. The diode D_3 current is same as coupled inductor secondary current (i_{sec}). The diode D_3 current (i_{d3}) is the summation of capacitor current and load current. In this mode voltage and current equations are,

$$v_{c_1} + nv_{Lm} + v_{c_2} = v_0 \tag{3.14}$$

$$i_{d_3} = i_{sec} = i_{c_0} + i_0 \tag{3.15}$$

$$i_m - ni_{sec} = i_{pri} \tag{3.16}$$

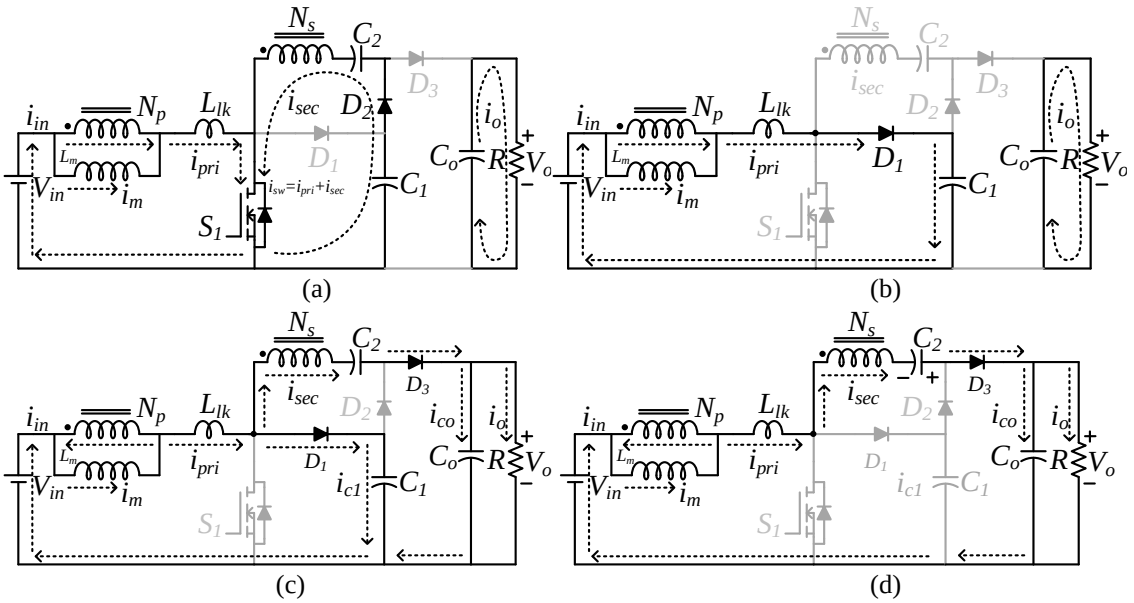


Fig. 3.15. Operation of proposed converter in CCM: (a) Mode 1 [t_0-t_1] (b) Mode 2 [t_1-t_2] (c) Mode 3 [t_2-t_3] (d) Mode 4 [t_3-t_4].

3.4.2. Operating Principle in Discontinuous Conduction Mode

DCM Operation

The operating mode of the converter in discontinuous mode in a switching cycle is shown in Fig. 3.16 through key waveforms. There are five modes in a switching period (T_s).

Mode 1 [t_0-t_1]:

This mode starts, when main switch S_1 is ON as shown in Fig. 3.15 (a). The magnetizing current (i_m) is increasing linearly. The discharging current (i_{d2}) flows from C_1, C_2, D_2 and S_1.This current charges the capacitor C_2 and flows till diode D_2 is forward biased.

Mode 2 [t_1-t_2]:

This mode starts when main switch S_1 is turned OFF, diode D_2, and D_3 are reverse biased.

The stored energy in leakage inductance is transferred to capacitor C_1 through diode D_1. This mode ends when D_3 starts conducting and current through C_1 starts decreasing. Magnetizing current (i_m) decreases linearly.

Mode 3 [t_2-t_3]:

In this mode current through capacitor C_1 starts falling and diode D_3 is in conduction. Diode D_2 is reverse biased as shown in Fig. 3.15 (c). Capacitor C_2 starts discharging through D_3 to load.

Mode 4 [t_3-t_4]:

In this mode capacitor C_2 is fully discharged and magnetizing current (i_m) falls to zero value as shown in Fig. 3.16.

Mode 5 [t_4-t_5]:

In this mode the load current is supplied by the output capacitor C_0. The primary current as well as magnetizing current is zero. All diodes are turned OFF in this mode.

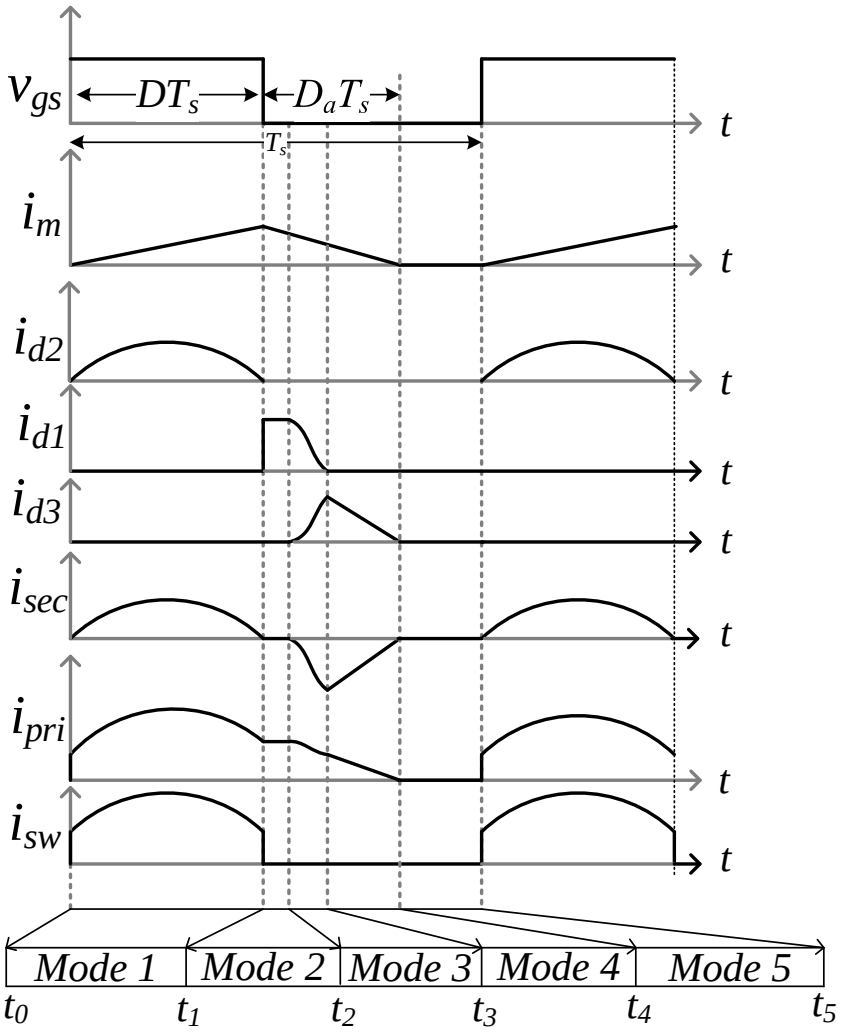


Fig. 3.16. Key waveforms of proposed converter in DCM.

3.4.3. Voltage Gain and Boundary Condition

From mode-1 operation which is shown in Fig. 3.15(a) the following voltage equations are obtained where V_{Lm}, V_{Lk}, V_{L2} are primary voltage, leakage inductance voltage and secondary voltage respectively.

$$v_{\mathrm{Lm}} = v_{\mathrm{L1}} = \frac{L_{\mathrm{m}}}{L_{\mathrm{m}}+L_{\mathrm{lk}}} v_{\mathrm{in}} = k v_{\mathrm{in}} \tag{3.17}$$

$$v_{\mathrm{Lk}} = \frac{L_{\mathrm{lk}}}{L_{\mathrm{m}}+L_{\mathrm{lk}}} v_{\mathrm{in}} = (1-k) v_{\mathrm{in}} \tag{3.18}$$

$$v_{\mathrm{L2}} = nk v_{\mathrm{in}} \tag{3.19}$$

Applying volt-sec balance in coupled inductor primary and secondary inductance the output voltage and capacitor voltage equations are derived in CCM. The detailed derivation is mentioned in Appendix-A.

$$v_{\mathrm{C_1}} = \frac{2\mathrm{D}(k-1)+(2-k)}{1-\mathrm{D}} v_{\mathrm{in}} \tag{3.20}$$

$$v_{\mathrm{C_2}} = \left(nk + \frac{2\mathrm{D}(k-1)+(2-k)}{1-\mathrm{D}} \right) v_{\mathrm{in}} \tag{3.21}$$

$$v_{\mathrm{C0}} = v_0 = \frac{nk+4\mathrm{D}(k-1)+2(2-k)}{1-\mathrm{D}} v_{\mathrm{in}} \tag{3.22}$$

Taking coefficient of coupling k=1, the voltage gain of the proposed converter in CCM is derived from equation. (3.22).

$$\mathrm{M_{CCM}} = \frac{v_{\mathrm{o}}}{v_{\mathrm{in}}} = \frac{n+2}{1-\mathrm{D}} \tag{3.23}$$

$$v_{\mathrm{C_1}} = \frac{v_{\mathrm{in}}}{1-\mathrm{D}}, \; v_{\mathrm{C_2}} = \left(n + \frac{1}{1-\mathrm{D}} \right) v_{\mathrm{in}} \tag{3.24}$$

The converter voltage gain (M_{CCM}) is shown in Fig. 3.17 for different coefficient of coupling (k).

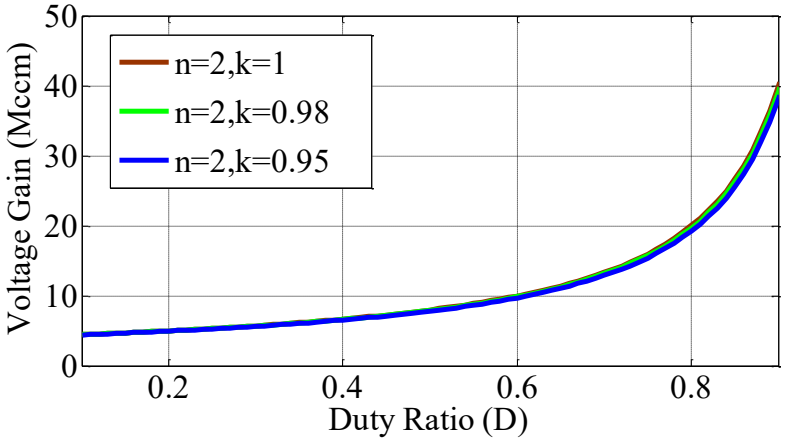


Fig. 3.17. Voltage gain of proposed converter in CCM for different coefficient of coupling (k)

The voltage gain (M_{CCM}) in CCM is compared with other existing topologies in literature as shown in Fig. 3.18.

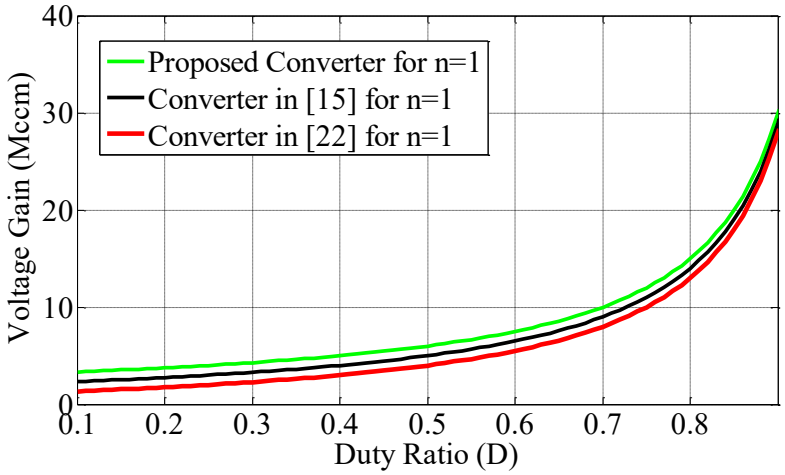


Fig. 3.18. Voltage gain comparison of converter in CCM @k=1 and n=1

Similarly, the voltage gain in DCM mode can be derived for k=1,

$$\mathrm{M_{DCM}} = \frac{(n+2)(\mathrm{D}+D_a)}{D_a} \tag{3.25}$$

From (3.25) the duty cycle $\mathrm{D_a}$ can be derived which is,

$$D_a = \frac{v_{\mathrm{in}}(n+2)\mathrm{D}}{v_{\mathrm{in}}(n+2)-v_{\mathrm{o}}} \tag{3.26}$$

From the voltage gain in DCM, the boundary condition between CCM and DCM can be derived which is shown in Fig. 3.19. The voltage gain (3.25) in DCM can be rewritten as,

$$\mathrm{M_{DCM}} = \frac{n+2}{2} + \sqrt{\frac{(n+2)^2}{4} + \frac{\mathrm{D}^2}{2\tau_{Lm}}} \tag{3.27}$$

$\tau_{Lm} = \dfrac{L_{\mathrm{m}}}{\mathrm{R}_L \mathrm{T}_{\mathrm{s}}}$ is the magnetizing inductor normalized time constant.

Therefore, the time constant at boundary condition ($\mathrm{D_a}$=1-D) is,

$$\tau_{Lmb} = \frac{\mathrm{D}(1-\mathrm{D})^2}{2(n+2)^2} \tag{3.28}$$

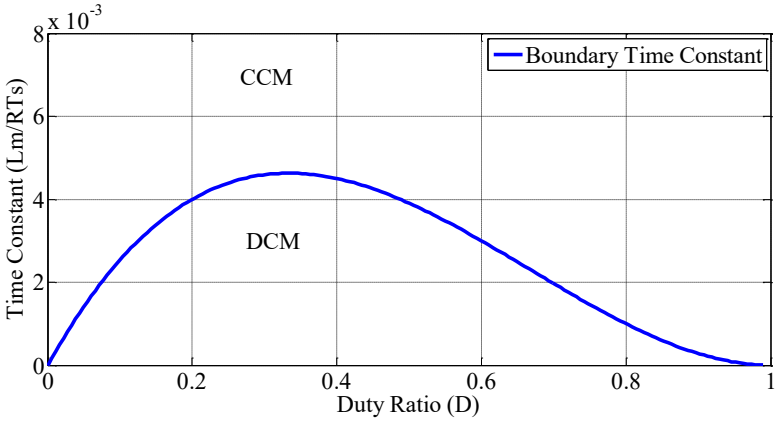


Fig. 3.19. Boundary condition of the converter at n=2

3.4.4. Effect of ESR on Voltage Gain

The voltage gain of the proposed DC-DC converter changes from ideal gain due to parasitic elements. The voltage gain (3.29) of the converter taking parasitic elements is,

$$\frac{v_o}{v_{in}} = \frac{\frac{2+n}{1\text{-D}} - \frac{2v_d}{v_{in}}}{1+\frac{1}{1\text{-D}}\left(A\frac{r_{pri}}{R_L}+B\frac{r_{sec}}{R_L}+C\frac{r_{sw}}{R_L}+D\frac{r_{d1}}{R_L}+E\frac{r_{d2}}{R_L}+F\frac{r_{d3}}{R_L}\right)} \tag{3.29}$$

Where, the parasitic parameters of the converter are: r_{pri}=18mΩ, r_{sec}=24mΩ, r_{sw}=35mΩ, r_{d1}, r_{d2}, r_{d3}=12mΩ, V_{in}=12V, V_d=0.61V, n=2, R_L=51.84Ω @ 100W and R_L=86.4Ω @ 60W.

The coefficients of voltage gain are:

$A=\frac{2(2+n)}{1-\text{D}}$, $B=n^3(1-\text{D})+\frac{n^2(2+n)}{1-\text{D}}$, $\text{D}=\frac{2+n}{1-\text{D}}$, $F=\frac{2+n}{1-\text{D}}$, $E=n$, and $C=n(1-\text{D})+\frac{\text{D}(2+n)}{1-\text{D}}$.

The voltage gain of the proposed converter is plotted ideally (22) as well as by taking the parasitic elements (3.29) as mentioned and shown in Fig. 3.20.

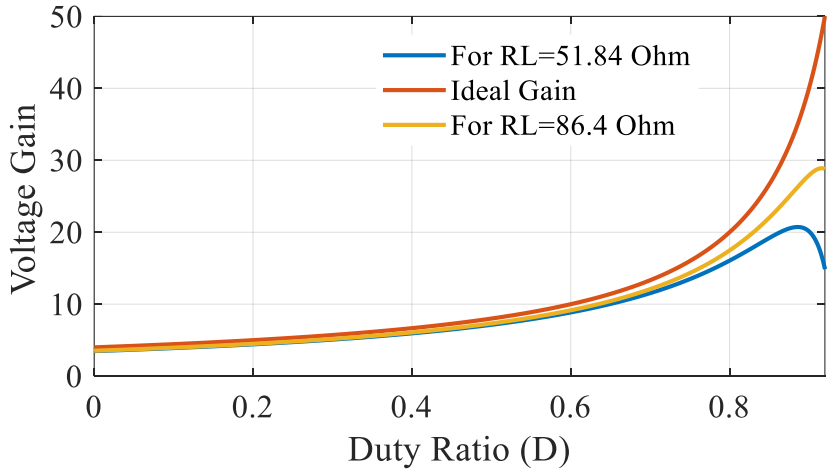


Fig. 3.20. Proposed DC-DC converter voltage gain taking parasitic elements with different load condition

3.4.5. Voltage and Current Stress of Proposed Topology and Comparison

3.4.5.1. Voltage Stress

The switch voltage stress (V_{sw}) of the converter is

$$v_{\text{Sw}} = \frac{v_{\text{in}}}{1\text{-D}} = \frac{v_0}{n+2} \tag{3.30}$$

Similarly, the diode voltage stress of the converter is

$$v_{\text{D1}} = \frac{v_0}{n+2} \text{ and } v_{\text{D2}} = v_{\text{D3}} = \frac{n+1}{n+2}v_0 \tag{3.31}$$

The comparison of voltage stress is listed in Table-3.1.

TABLE-3.1
COMPARISON OF VOLTAGE STRESS

	Proposed	[15]	[22]	[25]
Switch Voltage	$\frac{v_0}{n+2}$	$\frac{n+\mathrm{M}}{(1+2n)\mathrm{M}}v_0$	$\frac{n+1+\mathrm{M}}{(n+2)\mathrm{M}}v_0$	$\frac{n+\mathrm{M}}{(n+1)\mathrm{M}}v_0$
Diode voltage	$\frac{n+1}{n+2}v_0$	$\frac{n(n+\mathrm{M})}{(1+2n)\mathrm{M}}v_0$	$\frac{(n+1)(n+1+\mathrm{M})}{(n+2)\mathrm{M}}v_0$	$\frac{n(n+\mathrm{M})}{(n+1)\mathrm{M}}v_0$

Therefore, low voltage switch rating can be selected, which has low on state resistance and conduction loss can be minimized. The comparison of normalized switch voltage stress is shown in Fig. 3.21. The switch voltage stress of the converter is less.

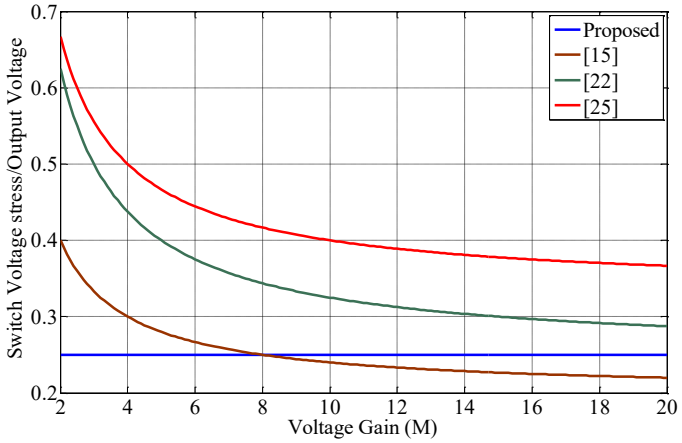


Fig. 3.21. Switch voltage stress comparison of converter in CCM @k=1 and n=2

3.4.5.2. Current Stress in CCM

By applying the charge balance for the output capacitor (C_o) and the average magnetizing current can be derived in CCM.

$$i_{\mathrm{m}} = \frac{v_o(n+1)}{(1\text{-}\mathrm{D})\mathrm{R}_L} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}\mathrm{D})^2\mathrm{R}_L} \tag{3.32}$$

The peak value of the magnetizing current (i_{Lm}) is

$$i_{\mathrm{m\_Peak}} = i_{\mathrm{m}} + \frac{\Delta i_{\mathrm{m}}}{2} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}\mathrm{D})^2\mathrm{R}_L} + \frac{v_{in}\mathrm{DT}_s}{2\mathrm{L}_{\mathrm{m}}} \tag{3.33}$$

Therefore, the average switch current (i_{sw}) during ON time is

$$i_{sw} = i_{\mathrm{m}} + (n+1)i_{\mathrm{sec}} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}\mathrm{D})^2\mathrm{R}_L} + (n+1)i_{\mathrm{sec}} \tag{3.34}$$

Where $i_{\mathrm{sec}} = i_2 = \frac{v_{\mathrm{in}}}{1-\mathrm{D}}\sqrt{\frac{\mathrm{C}_{\mathrm{eq}}}{\mathrm{L}_2}}\sin\left(\frac{1}{\sqrt{\mathrm{L}_2\mathrm{C}_{\mathrm{eq}}}}\mathrm{t}\right)$

As discussed earlier, if the resonating current (i_{sec}) value is maintained zero at the end of ON time i.e., $\mathrm{DT}_s = \pi\sqrt{\mathrm{L}_2\mathrm{C}_{\mathrm{eq}}} = t_r$, then the switch current (i_{sw}) value is minimum at turn

OFF instant and switch current stress reduction range starts. The switch current at turn-OFF transition will be same as peak current of magnetizing current (i_{Lm}) as shown in Fig. 3.22.

$$i_{sw}\big|_{t=DT_s} = \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R_L} + \frac{v_{in} DT_s}{2L_m} \tag{3.35}$$

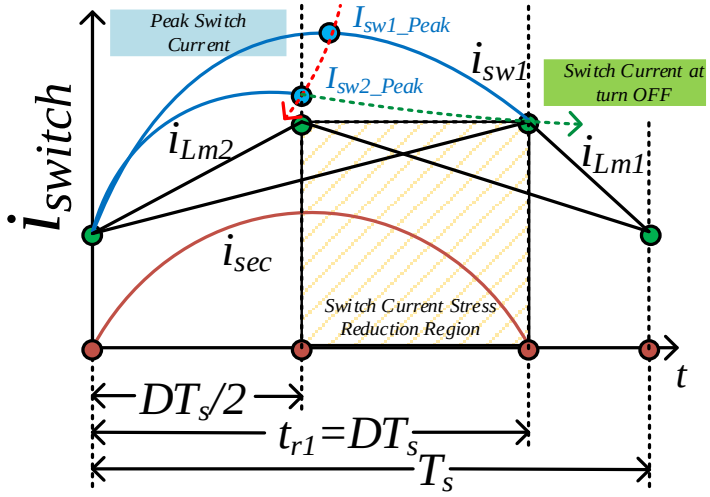


Fig. 3.22. Switch current stress reduction region of the converter in CCM

From the Fig. 3.22, it is clear that switch current value at turn OFF time is minimum when $t_{r1}=DT_s$ as i_{sec} is zero and the peak switch current can be minimized within $DT_s/2 \leq t \leq DT_s$. This is the operating region where switch current stress can be effectively minimized. As discussed in Section-3.2, in this technique no extra circuit element is used and it do not reduce voltage gain and efficiency of the converter.

Applying analytical method in the equivalent circuit shown in Fig. 3.15 (a) the switch current of the proposed converter can be derived. The switch current (i_{sw}) is

$$i_{sw}(t) = \frac{v_{in}}{L_m + L_{lk}} t + \frac{L_m}{L_m + L_{lk}} i_m(t) + \frac{v_{in}}{1-D}\sqrt{\frac{C_{eq}}{L_2}} \sin\left(\frac{1}{\sqrt{L_2 C_{eq}}} t\right) \text{ for } t>0 \tag{3.36}$$

The value of the switch current is minimum at $t_r = DT_s$. For duty ratio of 0.7, $t_r = 0.7T_s$ is the point where the switch current value at turn-off instant is minimum. The effective peak switch current minimization starts from $0.25T_s$ to $0.7T_s$ as shown in Fig. 3.23. This region is the effective switch current stress reduction region using secondary half cycle resonating branch. This technique is compared with L-D based solution [24] in p.u. From the Fig. 3.23, it is clear that switch current stress can be minimized effectively using proposed technique.

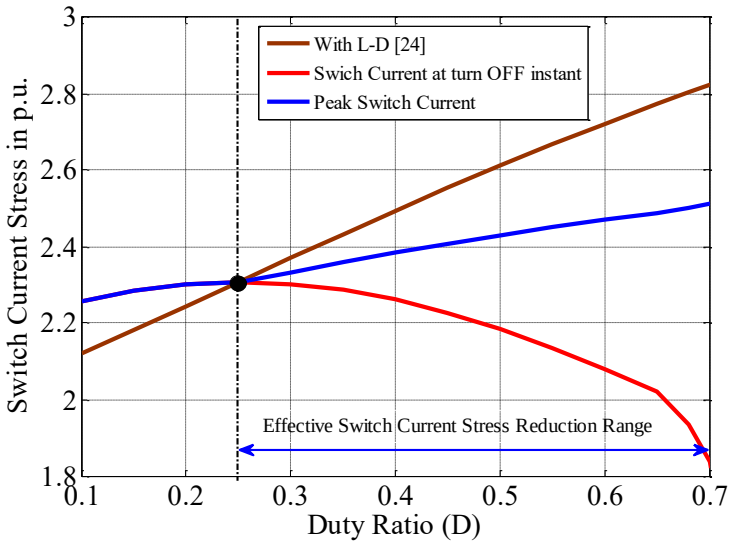


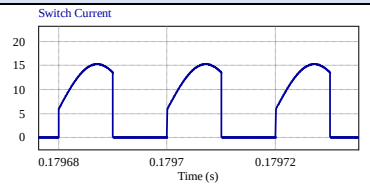
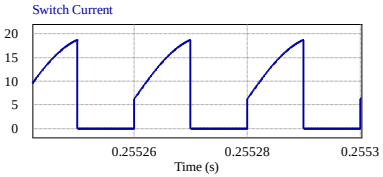
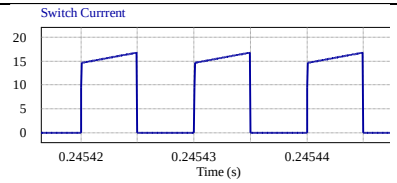
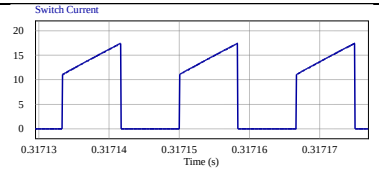
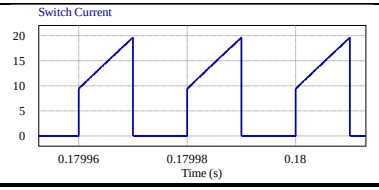
Fig. 3.23. Switch current stress comparison with L-D based solution [24].

The advantages of the proposed technique over L-D based solution are (a) Switch current reduction in the higher duty-ratio operating region, (b) no extra circuit element, (c) no adverse effect on the voltage gain and efficiency. Switch current stress comparison of single switch coupled inductor-based boost converter is shown in Table-3.2.

The comparison of other coupled inductor-based converter with current proposal is performed at 200W. The base current for normalizing process is considered as 6 A. The peak switch current without L-D circuit [19] at 0.5 duty ratio and 200 W condition is 19.6 A. The same peak switch current is decreased to 15.6A using L-D based circuit where L value is 12µH and converter operated at 50 kHz. The magnetizing inductance is 75µH.

The operating condition of the proposed converter should be $t_r > DT_s$ to minimize switch current stress effectively as shown in Fig. 3.23. Therefore, to meet the switch current stress reduction range up to 0.7 duty ratio, the critical condition is $0.7Ts=t_r$. For switching frequency of 50 kHz, the half cycle resonating time (t_r) is 14µSec. The secondary side inductance (L_r) is 1.78µH and therefore the C_r value can be derived from $t_r=\pi\sqrt{L_2C_{eq}}$ which is 11µF. The capacitor values of C_1, C_2 are selected to be 25µF and 20µF to meet $C_{eq}=\frac{C_1C_2}{C_1+C_2}$. With these values, simulation study is performed to verify switch current stress reduction range and compare with L-D based solution are mentioned in Fig. 3.23 and Table-3.2.

TABLE 3.2
COMPARISON OF SWITCH CURRENT STRESS

Topology	Peak Switch Current	Switch RMS Current	Current Waveform	Switch Selection @ 200W	SCSR
Proposed	$\cong \frac{v_{in}(n+1)(2+n)}{(1\text{-}D)^2 R_L} + \frac{v_{in}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}$	$\cong \frac{(n+2)\sqrt{D}}{(1\text{-}D)} i_o \sqrt{1+\frac{1}{12}\left(\frac{\Delta i_m}{i_o}\right)^2 \left(\frac{1-D}{n+3}\right)^2}$		FQP34N20 V_{ds}=200V, R_{ds}=0.075Ω I_d=31A.	YES
[15]	$\frac{v_{in}(n+1+nD)^2}{(1\text{-}D)^2 R_L} + \frac{v_{in} DT_s}{2L_m}$	$\approx \frac{(1+n+nD)\sqrt{D}}{(1\text{-}D)} i_o \sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2 \left(\frac{1-D}{1+n+nD}\right)^2}$		IRFB4410ZPBF V_{ds}=100V, R_{ds}=0.072Ω I_d=97A	NO
[22]	$\frac{v_{in}(1+(n+1)D)^2}{(1\text{-}D)^2 R_L} + \frac{v_{in}(n+1)(1+(n+1)D)}{(1\text{-}D) R_L} + \frac{v_{in} DT_s}{2L_m} + \frac{v_{in} DT_s}{2L_1}$	$\approx \frac{(n+2)\sqrt{D}}{(1\text{-}D)} i_o$		IPA075N15N3 V_{ds}=150V, R_{ds}=0.0075 Ω I_d=43A.	NO
[25]	$\frac{v_{in}(1+nD)^2}{(1\text{-}D)^2 R_L} + \frac{v_{in} n(1+nD)}{(1\text{-}D) R_L} + \frac{v_{in} DT_s}{2L_m} + \frac{v_{in} DT_s}{2L_1}$	$\cong \frac{(n+1)\sqrt{D}}{(1\text{-}D)} i_o \sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2}$		FQP34N20 V_{ds}=200V, R_{ds}=0.075Ω I_d=31A.	NO
[24]	$\frac{v_{in}(1+nD)}{(1\text{-}D)^4 R_L} + \frac{v_{in}(n+1)(1+nD)}{(1\text{-}D)^3 R_L} + \frac{v_{in} DT_s}{2(1-D)L_m} + \frac{v_{in} DT_s}{2L_1}$	$\approx \frac{(nD+n+2)\sqrt{D}}{(1\text{-}D)} i_o \sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2}$		IRF640 V_{ds}=200V, R_{ds}=0.18Ω I_d=18A.	YES

3.4.5.3. RMS Current Comparison

The proposed half cycle resonating branch utilizing coupled inductor does not increase the RMS value of the switch current. This can be theoretically demonstrated through graphical as well as mathematical formulation from switch current waveform as shown in Fig. 3.24.

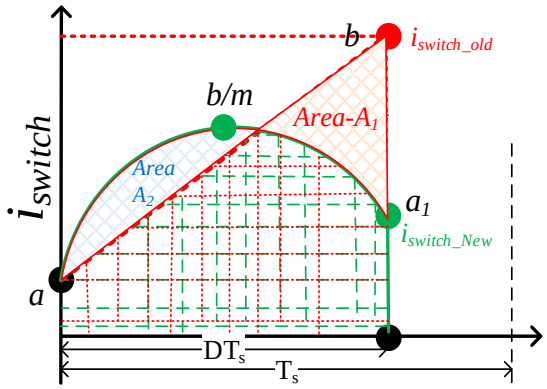


Fig. 3.24. Switch current waveform of conventional [19] and proposed converter during turn- 'ON' time.

In Fig.3.24, the modified current waveform can be approximated as shifted sinusoidal waveform compared to trapezoidal shape for conventional converter [19], [15], and [22] as shown in Fig. 3.24. The area A_1 in Fig. 3.24 is the reduction whereas area A_2 is the additional area. Assuming the peak current is reduced by factor 'm' where 'a' and 'a_1' are approximately same, the expression for RMS current for the modified waveform is given by,

$$I_{1rms}=\sqrt{D\left(a^2+\frac{1}{2}\left(\frac{b}{m}-a\right)^2+\frac{4a}{\pi}\left(\frac{b}{m}-a\right)\right)} \tag{3.37}$$

And for the existing trapezoidal wave the RMS current is

$$I_{2rms}=\frac{1}{\sqrt{3}}\sqrt{D\left(a^2+ab+b^2\right)} \tag{3.38}$$

Therefore, for lower value of RMS current in the proposed waveform,

$$I_{2rms}\geq I_{1rms} \tag{3.39}$$

From, the inequality criterion of (3.39) the peak current scaling factor (m) value can be mathematically derived which is 1.22. Therefore, 19 % reduction in peak current confirms equal RMS current or less as per Fig. 3.24. However, the starting point of switch current value 'a' is usually more in existing schemes compared to current proposal as shown in Table-3.2, which can be more advantageous. On the other hand, if ending point 'a_1' is higher than 'a' the reduction factor may increase from 1.22 value. Thus, it can be inferred

that the RMS value of current for the existing scheme can be definitely reduced as the peak current is usually reduced by more than 20% from the existing schemes.

3.4.5.4. Diode, Capacitor and Coupled Inductor Winding Current

Diode average, RMS currents can be calculated from Fig. 3.14 in CCM. The average value (3.40) of the diode D_3 is same as average load current (I_o).

$$i_{d3}=i_o \tag{3.40}$$

The RMS value of diode D_3 is

$$i_{d3}=i_{sec}\sqrt{1\text{-}D\text{-}D_b} \tag{3.41}$$

Where D_b is derived from charge balance equation of simplified capacitor current waveforms shown in Fig. 3.25.

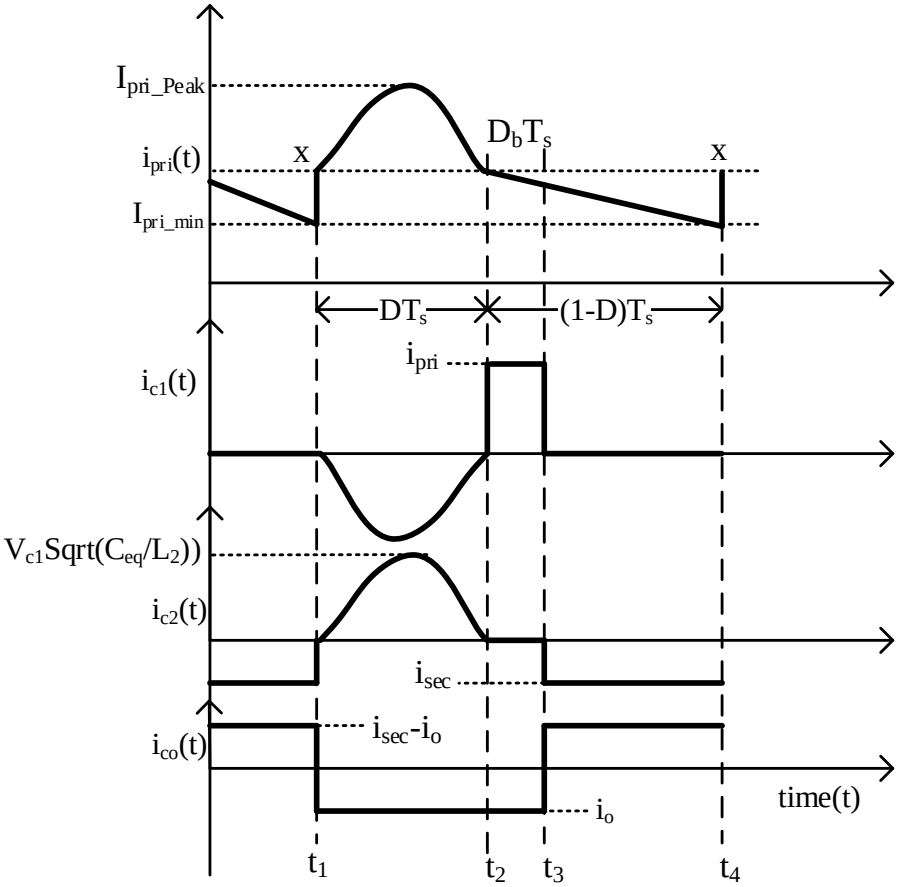


Fig. 3.25. Simplified capacitor current and primary winding current of coupled inductor waveforms.

$$D_b=\frac{v_{c1}D}{2\pi i_o}\sqrt{\frac{C_{eq}}{L_2}}\left(1\text{-}\cos\left(2\pi D\right)\right)\times\left(\frac{1\text{-}D}{n+2}\right) \tag{3.42}$$

The average and RMS current of diode D_2 is derived as shown in equation (3.43) and (3.44) respectively.

$$i_{d2(avg)} = \frac{v_{c1}}{\pi}\sqrt{\frac{C_{eq}}{L_2}} \tag{3.43}$$

$$i_{d2(RMS)} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(v_{c1}\sqrt{\frac{C_{eq}}{L_2}}\sin\left(\frac{2\pi}{T_s}t\right)\right)^2 dt} \tag{3.44}$$

The average and RMS current of diode D_1 is derived as shown in equation (3.45) and (3.46) respectively.

$$i_{d1(avg)} \cong \frac{n+2}{1\text{-}D} i_0 D_b \tag{3.45}$$

$$i_{d1(RMS)} \cong \frac{n+2}{1\text{-}D} i_0 \sqrt{D_b} \tag{3.46}$$

The RMS current (3.47) of the primary winding of the coupled inductor is given by

$$i_{pri(RMS)} = \sqrt{\left[(x^2 + x(x\text{-}I_{pri\_min})(1\text{-}D) + \frac{(x\text{-}I_{pri\_min})^2}{3}(1\text{-}D) + \frac{v_{c1}}{\pi}\sqrt{\frac{C_{eq}}{L_2}}(1\text{-}\cos(2\pi D)) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi})\right]} \tag{3.47}$$

Where, $x \cong \frac{n+2}{1\text{-}D} i_0$

Similarly, RMS current (3.48) of the secondary winding of the coupled inductor is given by

$$i_{sec(RMS)} = \sqrt{i_{sec}^2 \times (1\text{-}D\text{-}D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{3.48}$$

The RMS current of capacitors C_2, C_1 and C_0 are mentioned in equation (3.49), (3.50) and (3.51) respectively.

$$i_{c_2(RMS)} = \sqrt{i_{sec}^2 \times (1\text{-}D\text{-}D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{3.49}$$

$$i_{c_1(RMS)} = \sqrt{I_{pri\_min}^2 \times (D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{3.50}$$

$$i_{c_o(RMS)} = \sqrt{i_o^2 \times (D+D_b) + (i_{sec}\text{-}i_o)^2(1\text{-}D\text{-}D_b)} \tag{3.51}$$

3.4.6. Results and Discussion

The proposed converter is simulated in PSIM 9.1.1 and tested to check the performance using parameters of 100 W prototype hardware as mentioned in Table-3.3. Duty cycle is from 0.4-0.6 to verify different switch current stress reduction which is the inherent feature of this converter. The half cycle resonating branch current timing is main

important so that for almost entire operating region the switch current reduction is possible without sacrificing the voltage gain and efficiency.

TABLE-3.3
SIMULATION AND HARDWARE PARAMETERS

Converter Specification		
Input Voltage = 12 V	Power Output = 100 W	Output Voltage = 72 V
Duty Ratio = 0.5	Switching Frequency=50 kHz	Load Resistance = 50 Ω
Design Parameters	**Value**	**Part Number**
Coupled Inductor	L_m = 44 µH, Turns Ratio 25:25 (n = 1), $L_{leakage}$ = 8.26 µH	Ferrite Core PQ 32/30
Switch (S_1)	FQP34N20 (V_{ds} = 200 V, R_{ds} = 0.075 Ω, I_d=31 A.) @ 200W	FQP34N20
Diodes (D_1, D_2, D_3)	FRD	IN5401
Capacitor C_1	10 uF	
Capacitor C_2	Simulation: 1.3 uF, Hardware: 10 uF	
Capacitor C_o	100 uF	

As discussed in previous section, the converter operation is divided into two main sections i.e., CCM and DCM. The Switch current reduction is tested in CCM as well as in DCM. In CCM the switch current reduction is again divided into three subsections which are (a) $DT_S < t_r$ (b) $DT_S = t_r$ (c) $DT_S > t_r$. In all three modes, the switch current reduction is effectively achieved in (a) $DT_S < t_r$ (b) $DT_S = t_r$ as shown in simulation result in Fig. 3.26. Simulation was carried out taking switching time is 20µs. At D = 0.5 and $DT_s = t_r$ the switch current value is minimum at turn OFF instant as shown in Fig. 3.26 (a).

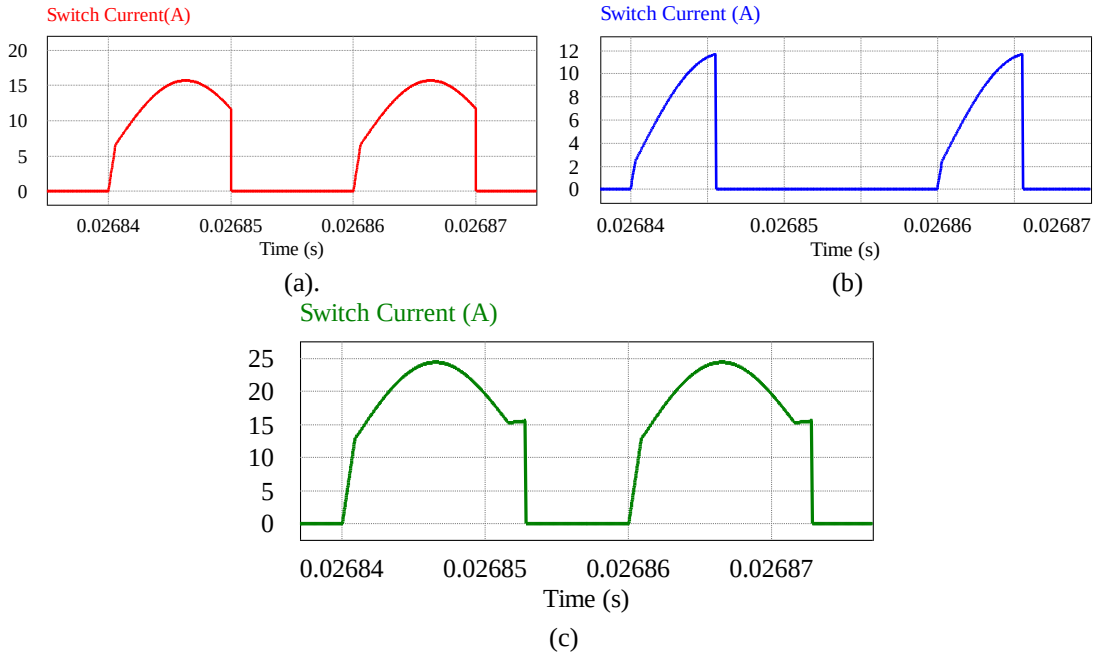


Fig. 3.26. Switch Current in CCM (a) for [$DT_S = t_r$] (b) for [$DT_S < t_r$] (c) for [$DT_S > t_r$].

For $DT_S<t_r$ the switch current stress is low as shown in Fig. 3.26 (b) but for $DT_S>t_r$ the switch current stress is almost same with other topologies which is shown in Fig. 3.26 (c). Therefore, selection of t_r should be such that in the operating duty ratio range i.e., 0.4-

0.7 the converter ON time is exactly same as t_r or less than t_r. As the switching time is 20µSec, for 0.5 duty ratio at $DT_s = t_r$, the half cycle resonating time is 10 µs. Therefore, from equation, $t_r = \pi\sqrt{L_2 C_{eq}}$ the equivalent capacitor is determined. By increasing the capacitance (C_{eq}) value t_r can be increased. Taking C_1, C_2 10 µF the resonating time is increased to check the switch current during $DT_s < t_r$. condition. Prototype of 100 W converter is designed and tested at 0.5 duty ratio. For 12 V input the switch voltage stress is around 24 V as shown in Fig. 3.27 (d) for D = 0.5, n = 1 and $DT_s < t_r$. The input current, and switch current under this condition is shown in Fig. 3.27 (a) which shows a good match with the simulation. The capacitor voltages V_{C1}, V_{C2} are shown in Figs 3.27 (b) and Fig. 3.27 (c) respectively which matches with calculated value as per equation (3.24) and simulation.

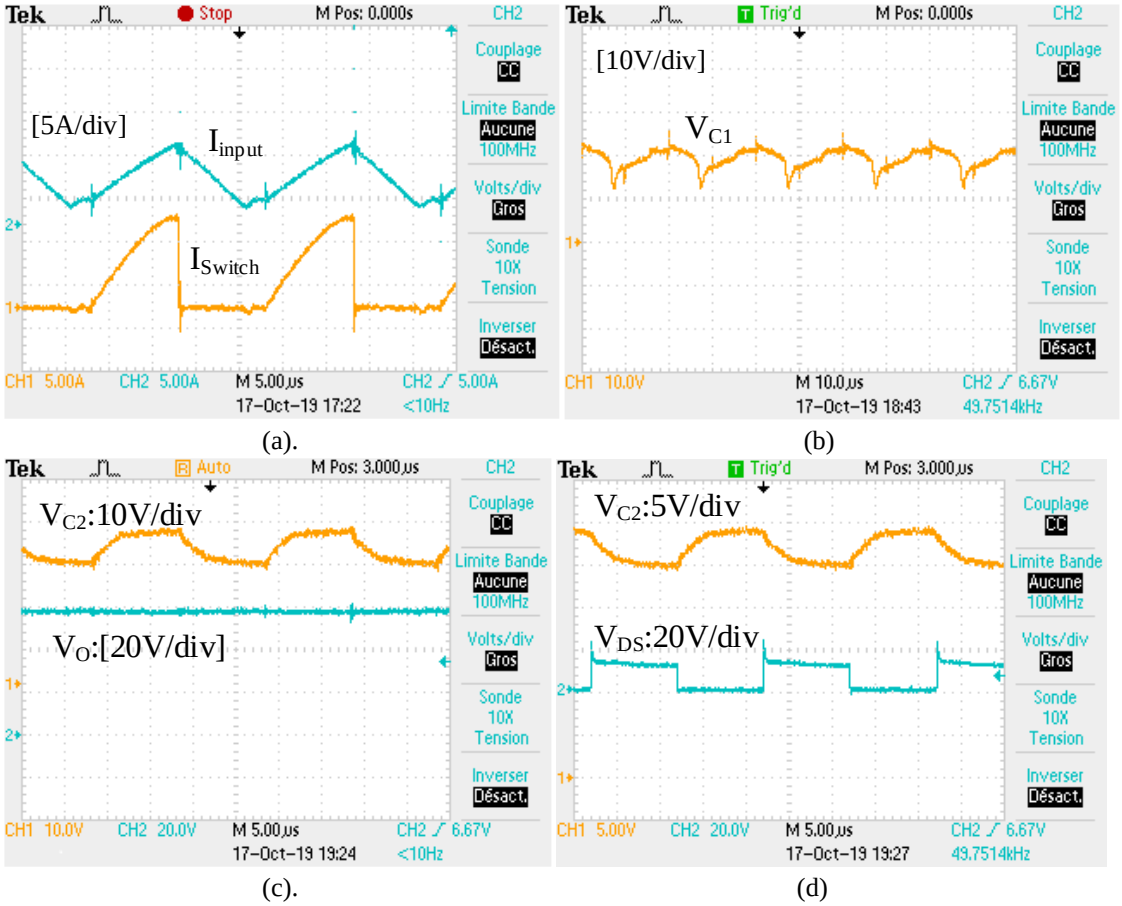


Fig. 3.27. Proposed Converter operation in CCM at ($DT_S<t_r$) (a) Input current and Switch current (b) Capacitor Voltage V_{c1} (c) Capacitor Voltage V_{c2} and output voltage V_o.(d) Switch voltage V_D.

Again, at C_1 10µF and C_2 at 1.3µF the resonating time t_r can be made exactly same as 10µsec. Therefore, $DT_s=t_r$ can be achieved at 0.5 duty ratio at 50 kHz. At this condition the switch current value at turn OFF instant is minimum but stress is greater than $DTs<t_r$ condition as shown in Fig. 3.28 (a).

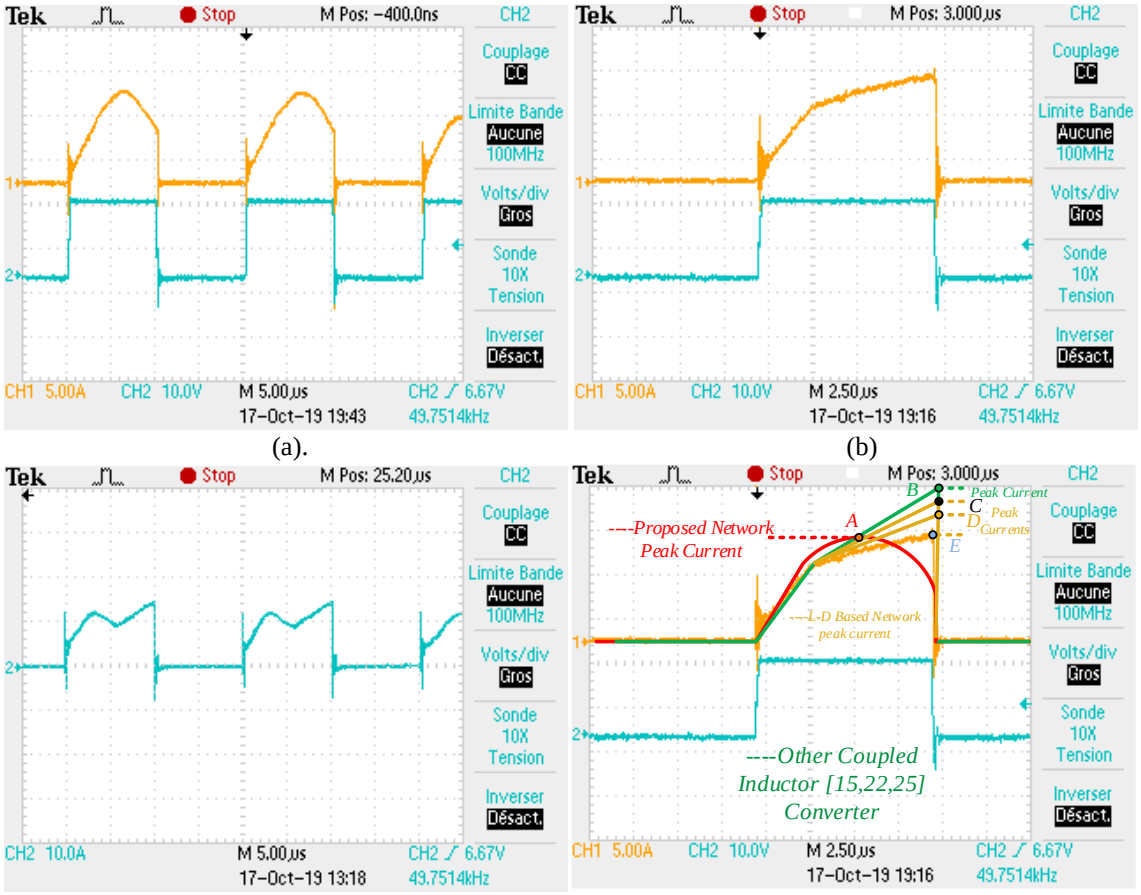


Fig. 3.28. Switch current waveform of (a) proposed converter (5A/div) in CCM at $DT_S=t_r$ (b) L-D network (5A/div) solution [24] (c) proposed converter (10A/div) in CCM at $DT_S>t_r$, and (d) comparison of switch current stress [A-Proposed technique peak, B-Peak current of coupled inductor boost, C, D, E-Peak current (5A/div) with increasing inductance value using L-D network-based solution.

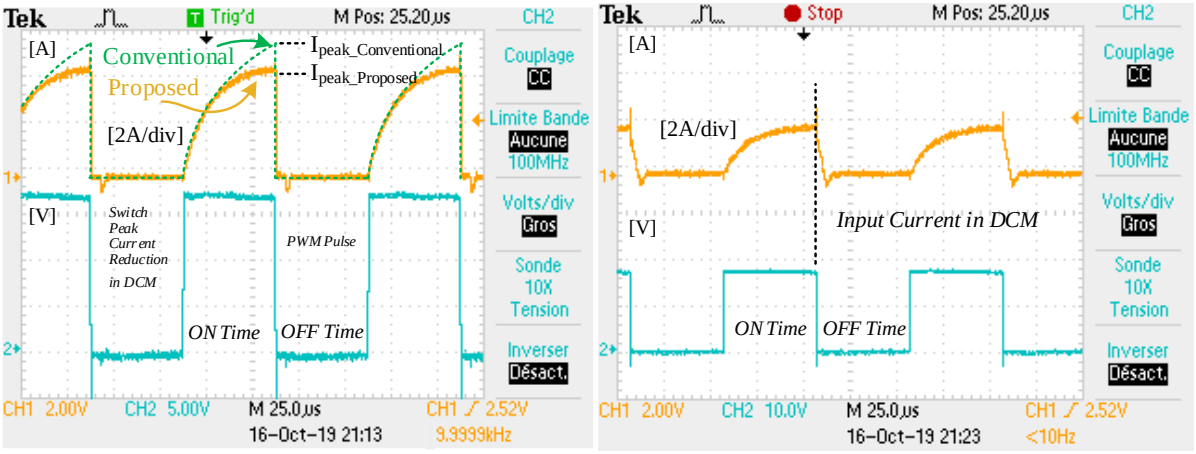
For L-D based solution of switch current stress reduction depends on value of inductance. For larger inductance switch current stress is less and same as current proposal as shown (point A, E) in Fig. 3.28 (d). But for low inductance value the peak switch current is more (Point C, D) than current proposal as shown in Fig. 3.28 (d). The switch current at turn OFF transient is more compared to current proposal. The prototype converter is designed for 100W. The input voltage is 12V and in the ideal condition, the average input current is 100/12=8.33 A. Therefore, the base value of current is considered as 8.5 A for calculation and comparison of peak current. The base inductor value is L_m=44µH as mentioned in Table-3.3. For comparison with L-D based solution, the converter proposed in [24] is operated at 100W and in same input voltage, duty ratio (D=0.5) where the initial L value is 10.5µH at 50 kHz is mentioned in Table-3.4. But in the current topology if $DT_s>t_r$ then the current stress reduction fails as shown in Fig. 3.28 (c). Therefore, designing circuit element of C_1 and C_2 with coupled inductor secondary inductance is very important to achieve true switch current reduction with the operating duty ratio range

i.e., 0.4-0.7. In the current proposal no extra element is used as well as voltage gain and efficiency are not hampered.

TABLE-3.4
COMPARISON OF SWICH CURRENT REDUCTION METHOD

L-D Based Solution	Peak Switch Current @ Duty (D)= 0.5	Voltage gain and Efficiency (η) Decrement
For L = 0.24 p.u.	1.5 p.u.	Gain= 5-6%, η=4-5%
For L = 0.14 p.u.	1.8 p.u.	Gain=3-5%, η=3%
For L = 0.10 p.u.	≈2.6 p.u.	Gain= 2-3%, η=2.5%
Current Proposal	Peak Switch Current @ Duty (D)= 0.5	Voltage gain and Efficiency (η) Decrement
At $DT_s=t_r$	1.54 p.u.	No Decrement
At $DT_s<t_r$	1.37 p.u.	No Decrement
At $DT_s>t_r$	2.81 p.u.	Switch current reduction fails

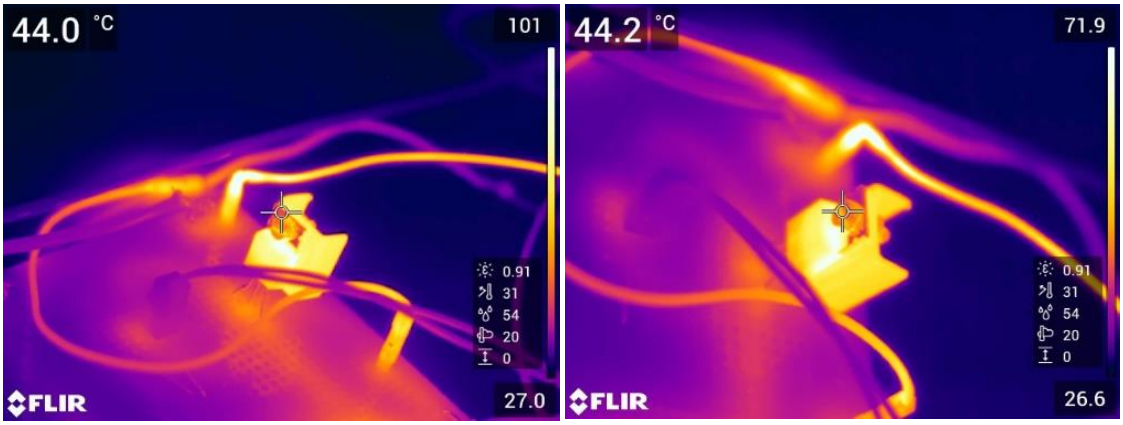
From Fig. 3.23 theoretically it is derived that from 0.25 to 0.7 duty ratio the switch current stress reduction is possible without wasting extra energy like using L-D network and voltage gain loss. The switch current reduction is also valid for DCM operation of the converter. Converter proposed in [19] is considered as conventional for comparison with current proposal at DCM. From Fig. 3.29 it is clear that in the DCM the switch current peak value is less.



(a). (b)

Fig. 3.29. Converter operation in DCM at ($DT_S<t_r$) (a) switch current (b) input Current. @ 10 kHz.

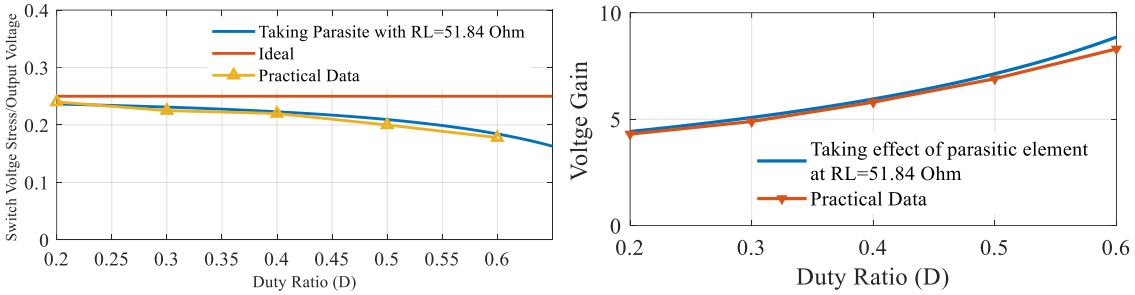
RMS current is the dominating factor while determining loss and efficiency for any converter. The RMS current of the current proposal is comparable with L-D based solution [24] and other topologies. Thermal image of the main switch is captured using thermal imager to show the closeness of RMS current between current proposal and L-D based solution [24] at rated 100W condition as shown in Fig. 3.30 (a) and Fig. 3.30 (b).



(a). (b)

Fig. 3.30. Thermal image of switch in (a) L-D based switch current stress reduction proposed in [24] (b) proposed DC-DC converter.

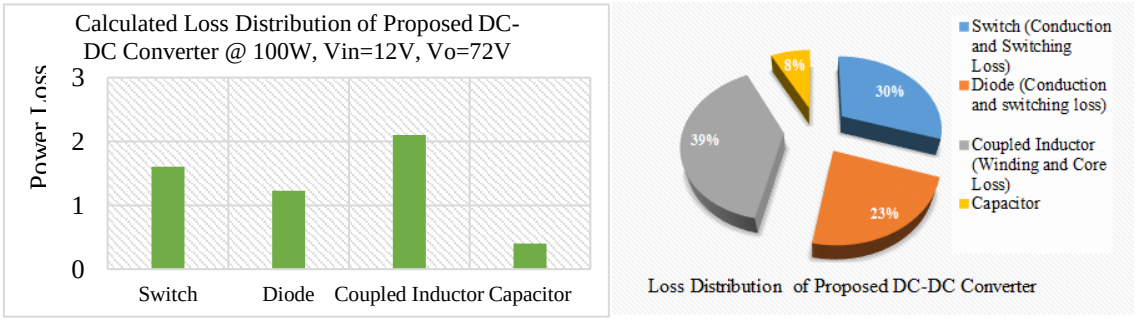
The voltage gain variation between non-ideal and practical gain is marginal. Switch voltage stress is compared using parasitic values as well as practical values as shown in Fig. 3.31 (a). The practical reading of output voltage is matched with the voltage gain taking parasitic elements as shown in Fig. 3.31 (b).



(a) (b)

Fig. 3.31. (a) Ideal and practical switch voltage stress. (b) Voltage gain comparison with parasitic elements and practical data.

Theoretical loss calculation is performed on proposed DC-DC converter at 100W, based on selected components summarized in Table-3.3 to estimate losses, efficiency and shown in Fig. 3.32(a) and Fig. 3.32(b). Losses in coupled inductor and diode is more in the loss distribution.



(a). (b)

Fig. 3.32. Loss distribution of the proposed DC-DC boost converter.

Based on the theoretical calculation [26] taking hardware components as mentioned in

Table-3.3, estimated efficiency is compared to measured efficiency at different power points through power quality analyser APLAB-PQA2100E as shown in Fig. 3.33(a). The difference between theoretical estimated efficiency and practical measurement is due to ignorance of different circuital parameters like skin effect, proximity effect, exact transient time for switching events etc. Current waveforms are also considered as ideal for theoretical calculation which create differences in measured and calculated efficiency. The calculation for finding theoretical efficiency is added in the appendix section A.

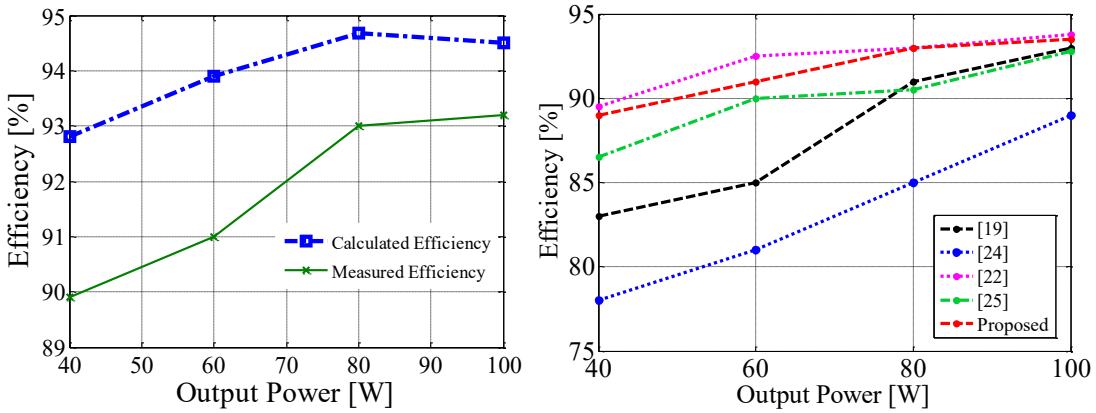


Fig. 3.33. (a) Estimated and measured efficiency of the proposed DC-DC converter and (b) Efficiency comparison of the proposed converter.

At 100W, the measured efficiency is 93.2%. Better-graded wires can be used in the inductor to further improve the efficiency. The discrepancy is caused by ignoring the leakage inductance, small-ripple assumption and measurement error. Efficiency comparison with other converter as shown in Fig. 3.33 (b) is also performed to show that there is no sacrifice on efficiency especially when compared with proposal [24]. The converter in [22] has better efficiency i.e., ≈1% by margin compared to current proposal. However, this difference is marginal and current proposal is better in terms of voltage gain, switch current stress minimization.

3.5. Summary

Generally, in a single switch type high step-up coupled inductor-based boost converter, multi loop current paths are used to lift the voltage gain particularly at a duty ratio less than 0.5. This increases the switch current stress due to low inductance of the coupled inductor. Considering this, a half cycle resonating branch is introduced to utilize the inductance of the coupled inductor without increasing the circuit component and complexity. This improves the current stress on the main switch of the coupled inductor based single switch high step-up boost converter. This technique can be used to modify all the existing circuit topologies, resulting in the better performance in terms of voltage

gain, efficiency and current stress. The measured efficiency of designed boost DC-DC converter is 93.2% at 100W, which is close to the proposal [22]. Additionally, the proposed technique performs superior than [24] as it can reduce the current stress up to 22% without sacrificing the voltage gain and efficiency. Moreover, this technique does not increase the RMS current, which improves the converter life span and reliability.

3.6. Publication and References

Publication:

[1] **S. B. Santra**, D. Chatterjee, Y. P. Siwakoti and F. Blaabjerg, "Generalized Switch Current Reduction Technique for Coupled-Inductor Based Single Switch High Step-Up Boost Converter", **IEEE Journal of Emerging and Selected Topics in Power Electronics**, Vol. 9. No. 2, pp. 1863-1875, April 2021.

[2] T. R. Choudhury, B. Nayak and **S. B. Santra**, "A Novel Switch Current Stress Reduction Technique for Single Switch Boost-Flyback Integrated High Step Up DC–DC Converter," in **IEEE Transactions on Industrial Electronics**, vol. 66, no. 9, pp. 6876-6886, Sept. 2019.

References:

[1] F. Blaabjerg, Zhe Chen and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184-1194, Sep. 2004.

[2] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc–dc converters," *IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 65–73, Jan. 2003.

[3] Z. Jiang and R. A. Dougal, "A compact digitally controlled fuel cell/battery hybrid power source," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1094–1104, Aug. 2006.

[4] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformer-less dc–dc converter with high voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.

[5] R. J. Wai, C. Y. Lin, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High efficiency power conversion system for kilowatt-level stand-alone generation unit with low input voltage," *IEEE Trans. Ind. Electron*., vol. 55, no. 10, pp. 3702–3714, Oct. 2008.

[6] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg and B. Lehman,"Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," in *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143-9178, Dec.2017.

[7] Y. Zheng, W. Xie and K. M. Smedley, "A Family of Interleaved High Step-Up Converters with Diode-Capacitor Technique," in *IEEE Journal of Emerging and Selected Topics in Power Electronics* (Early Access-2019).

[8] R. J. Wai and R. Y. Duan, “High-efficiency dc/dc converter with high voltage gain,” *Proc. IEE—Elect. Power Appl*., vol. 152, no. 4, pp. 793–802, Jul. 2005.

[9] S. Chen et al., "Research on Topology of the High Step-up Boost Converter with Coupled Inductor," in *IEEE Trans. Power Electron.,* (Early Access-2019).

[10] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," in *Proc. IEE – Elec. Power Appl*., vol. 151, no. 2, pp.182-190, 9 March 2004.

[11] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, “Boost converter with coupled inductors and buck–boost type of active clamp,” *IEEE Trans. Ind. Electron*., vol. 55, no. 1, pp. 154–162, Jan. 2008.

[12] Y. P. Hsieh, J. F. Chen, T. J. Liang and L. S. Yang, "A Novel High Step-Up DC–DC Converter for a Microgrid System," in *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1127-1136, April 2011.

[13] A. Ajami, H. Ardi and A. Farakhor, "A Novel High Step-up DC/DC Converter Based on Integrating Coupled Inductor and Switched-Capacitor Techniques for Renewable Energy Applications," in *IEEE Trans. on Power Electron.,* vol. 30, no. 8, pp. 4255-4263, Aug. 2015.

[14] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti and F. Blaabjerg,"High-Efficiency High Step-Up DC–DC Converter with Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," in *IEEE Trans. on Power Electron.*, vol. 33, no. 7, pp. 5967-5982, July 2018.

[15] Y. Hsieh, J. Chen, T. J. Liang and L. Yang, "Novel High Step-Up DC–DC Converter for Distributed Generation System," *in IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1473-1482, April 2013

[16] S. Chen, T.J.Liang, L. Yang and J. Chen, "A Boost Converter With Capacitor Multiplier and Coupled Inductor for AC Module Applications," in *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1503-1511, April 2013.

[17] Y. Siwakoti and F. Blaabjerg, “A single switch non-isolated ultra step-Up DC-DC converter with integrated coupled inductor for high boost applications,” *IEEE Trans. Power Electron*., vol. 32, no. 11, pp. 8544–8558, Nov. 2017.

[18] E. Babaei and Z. Saadatizadeh, “High voltage gain dc–dc converters based on coupled inductors,” *IET Power Electron*., vol. 11, no. 3, pp. 434–452, 2018.

[19] S.-M. Chen, T.-J. Liang, L.-S. Yang, and J.-F. Chen, “A cascaded high step-up DC–DC converter with single switch for micro source applications,” *IEEE Trans. Power Electron*., vol. 26, no. 4, pp. 1146–1153, Apr. 2011.

[20] B. P. R. Baddipadiga, V. A. Prabhala, and M. Ferdowsi, “A family of high-voltage-gain DC-DC converters based on a generalized structure,” *IEEE Trans. Power Electron*., vol. 33, no. 10, pp. 8399–8411, Oct. 2018.

[21] Y.Hsieh, J.Chen, T. J. Liang and L.Yang, "Analysis and implementation of a novel single-switch high step-up DC-DC converter," in *IET Power Electron.*, vol. 5, no. 1, pp. 11-21, January 2012.

[22] Y. Zheng and K. M. Smedley, "Analysis and Design of a Single-Switch High Step-Up Coupled-Inductor Boost Converter," in *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 535-545, Jan. 2020.

[23] A. M. S. S. Andrade and M. L. d. S. Martins, "Study and Analysis of Pulsating and Nonpulsating Input and Output Current of Ultrahigh-Voltage Gain Hybrid DC–DC Converters," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3776-3787, May 2020.

[24] T. R. Choudhury, B. Nayak and S. B. Santra, "A Novel Switch Current Stress Reduction Technique for Single Switch Boost-Flyback Integrated High Step Up DC–DC Converter," in *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6876-6886, Sept. 2019.

[25] K. B. Park, G. W. Moon, and M. J. Youn, “Non-isolated high step-up boost converter integrated with SEPIC converter,” *IEEE Trans. Power Electron*., vol. 25, no. 9, pp. 1791–1801, Sep. 2010.

[26] R.W.Erickson and D.Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA, Kluwer, 2001.

Chapter-4

High Voltage Gain and High Efficiency Coupled Inductor Based Non-Isolated BDC

The boost stage of BDC using coupled inductor which has superior voltage gain and less voltage stress, current stress is already discussed in chapter-3. By adopting the same boost circuit, a coupled inductor based novel high gain, high efficiency non-isolated bidirectional converter is proposed in this chapter. The proposed BDC has less voltage and current stress especially at low voltage side main switch. The steady state operation of the proposed BDC is discussed in details along with proper controller design. Comparison with other topologies is also discussed in this chapter.

4. High Voltage Gain and High Efficiency Coupled Inductor Based Non-Isolated BDC

4.1. Introduction

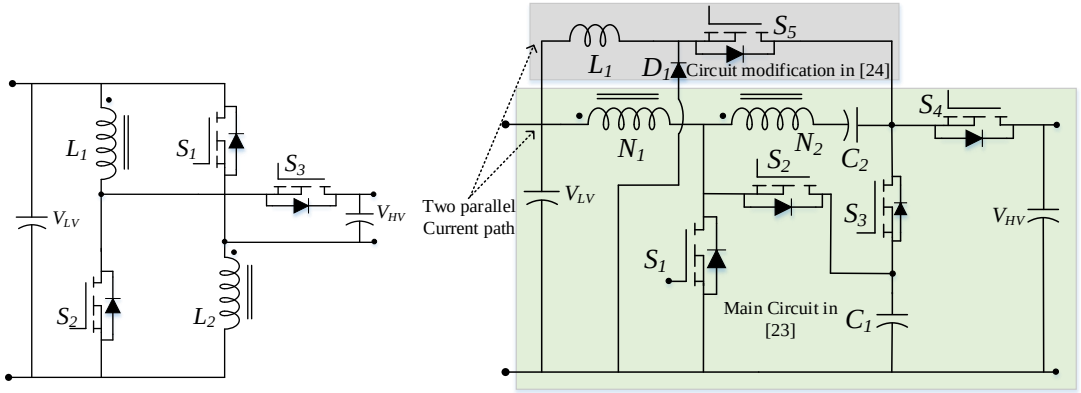
The boost converter proposed in the previous chapter is adopted to develop bidirectional DC-DC converter topology by incorporating buck stage in the same circuit. Some modification in circuit topology of boost mode is performed compared to circuit proposed in earlier chapter which ensures high conversion factor in both buck and boost operation modes. Three winding coupled inductor is used in designing the boost/buck stage. All the circuit components are operational in both the operating modes which confirms best utilization of components. The half cycle resonating branch in the proposed BDC confirms low current stress at LV main switch. The coupled inductor three windings are used in topology derivation to achieve current sharing property in the LV side for both the operating modes.

4.2. Topological Survey and Limitations of Existing Coupled Inductor Based BDC

Bidirectional DC-DC converters (BDC) are indispensable as buffer stage which is widely used in the applications like storage interface [1], electric vehicle (EV) [2]. Traditional two switch non-isolated BDC [3-4] is not suitable for these applications as it requires extreme duty ratios to attain voltage gain (≥10) in boost mode and (≤1/10) in buck mode to interface low voltage battery i.e., 12V-48V source to high voltage side i.e., 150V-400V bus [1-2]. The efficiency and the voltage stress performance are also poor for the conventional BDC. To solve the difficulty in attaining required conversion ratio in both buck and boost mode of operation BDCs are classified into two broad categories i.e., isolated BDC and non-isolated BDC. Isolated BDC uses transformer as an isolating element which offers flexibility in varying turns ratio and helps in attaining high conversion ratios. However, the number of active switches is generally greater than eight or more in full bridge isolated BDC [5-7]. Clamped capacitor circuits [8] are used in these topologies to overcome voltage stress due to leakage inductance, which further increases control complexity of these isolated BDC. Half bridge topologies [9] are alternative choice in these categories to reduce number of active switches. However, achieving soft switching (ZVS) [10] and control complexity is a major problem of these converters. Non-isolated BDCs uses different circuit concepts like SEPIC, voltage multiplier cell, switched capacitor, coupled inductor to achieve high conversion ratio. The efficiency of SEPIC derived BDCs [11] is low because

of its cascaded structure. Voltage multiplier cell can be used in designing BDCs, but it creates large voltage stress across switches. Switched capacitor based BDCs [12-14] are inherently perform better because of its simple structure and less control complexity. However, the switching loss and large switch current stress in these types of converter continues to be the major problem. Hybrid structures, like SEPIC with switched capacitor and quasi-Z source with switched capacitor [15] are capable of achieving high conversion factor. But large component count and inability to achieve soft switching limits conversion efficiency. In contrary coupled inductor based BDCs are well suited for achieving wide range voltage gain with low stress voltage [16]. The efficiency of these converters is also comparable to the isolated BDCs. By proper circuit arrangement; switch current [17] and voltage stress can also be minimized. The leakage inductance energy can be stored in clamped capacitor which can be utilized in power flow. Zero voltage switching (ZVS) turn on of active switches in these converters can be attained using auxiliary circuit [18-20], but has limited gain and control complexity. However, soft switching of these converters can be achieved using synchronous rectification concept which do not require extra circuit elements.

In last decade, there are many coupled based bidirectional DC-DC converter topologies are proposed in this direction. The fundamental topology with interleaved structure is proposed by L. S. Yang *et.al* [21] as shown in Fig. 4.1 (a). Intermediate capacitor-based topology is proposed [22] in modification of initial topology to increase the voltage gain but lost parallel inductor structure which is helpful in current sharing during buck mode. The main topology which recovers the leakage energy in a clamped capacitor and use it in circuit operation is originally proposed by R. Y. Duan *et. al* [23] as shown in Fig. 4.1 (b).



(a). (b)

Fig. 4. 1. BDC configurations using coupled inductor (a) Interleaved structure by L.-S. Yang *et al.* [21] (b) Clamped capacitor-based high gain circuit [23] and modified circuit [24].

This topology has inherently higher conversion ratios i.e. (n+2)/(1-D) and (D/n+2) in boost and buck mode respectively. This topology also has the capability to achieve soft switching. The current sharing in buck mode is not achieved in this topology which was rectified by the same authors in [24]; where extra inductor is used in parallel to the coupled inductor as shown in Fig. 4.1 (b). This extra inductor is used in buck operation and remained unused in boost operation which left a research gap. Topology proposed by M. Das *et al*. [25] can achieve soft switching like [23] but conversion ratio is inferior. Exactly same circuit like in [23], with one extra capacitor is proposed in [26] which provides same performance like original circuit. Circuit proposed by W. Hassan *et al*. [27] utilized the same structure [23] with a small modification by branching coupled inductor, but reached to the same conversion factor as in the original circuit. M. Amir *et al*. [28] proposed same coupled inductor based BDC as previously proposed in [24]. Quasi resonant operation of same [23] BDC structure where coupled inductor is replaced by simple inductor is proposed [29] which is further generalized to make the topology suitable for high power application. But the basic circuit structure remains the same. H. Liu *et al*. [30] utilized the same structure, but branching coupled inductor path leads to reduced voltage gain compared to the original circuit [23]. Interleaved structure using two extra inductors is utilized by the proposal [31] to achieve current sharing whereas coupled inductor increases the voltage conversion factor. Interleaved structure with switched capacitor network [32-33] is also promising solution in non-isolated BDC circuit design. Though topology [31] performs better in terms of gain, stress level and efficiency compared to [25], [27] but circuit operation is complex with additional parallel inductors. However, the limitation of [31] can be eliminated by effectively utilizing coupled inductor voltage conversion factor without increasing complexity of the circuit.

Reduction in input current ripple and current sharing is possible by using parallel structure as shown in Fig. 4.1 (a). Voltage gain can be improved using cascading structure [35] as shown in Fig. 4.2 (a). However, the hard-switched cascading structure has less efficiency and do not have current sharing benefit. To achieve high conversion factor and soft switching using synchronous rectifier concept secondary coupled inductor branch is used primarily in [23] as shown in Fig. 4.1 (b). Later modification of the secondary coupled inductor branch position is adopted in [25] as shown in Fig. 4.2 (b) to achieve current sharing and higher gain but fails to achieve it. Similarly, modification in coupled inductor branch position is mentioned in [27] as shown in Fig. 4.2 (c) to achieve same objectives but the performance parameter remains same as [23].

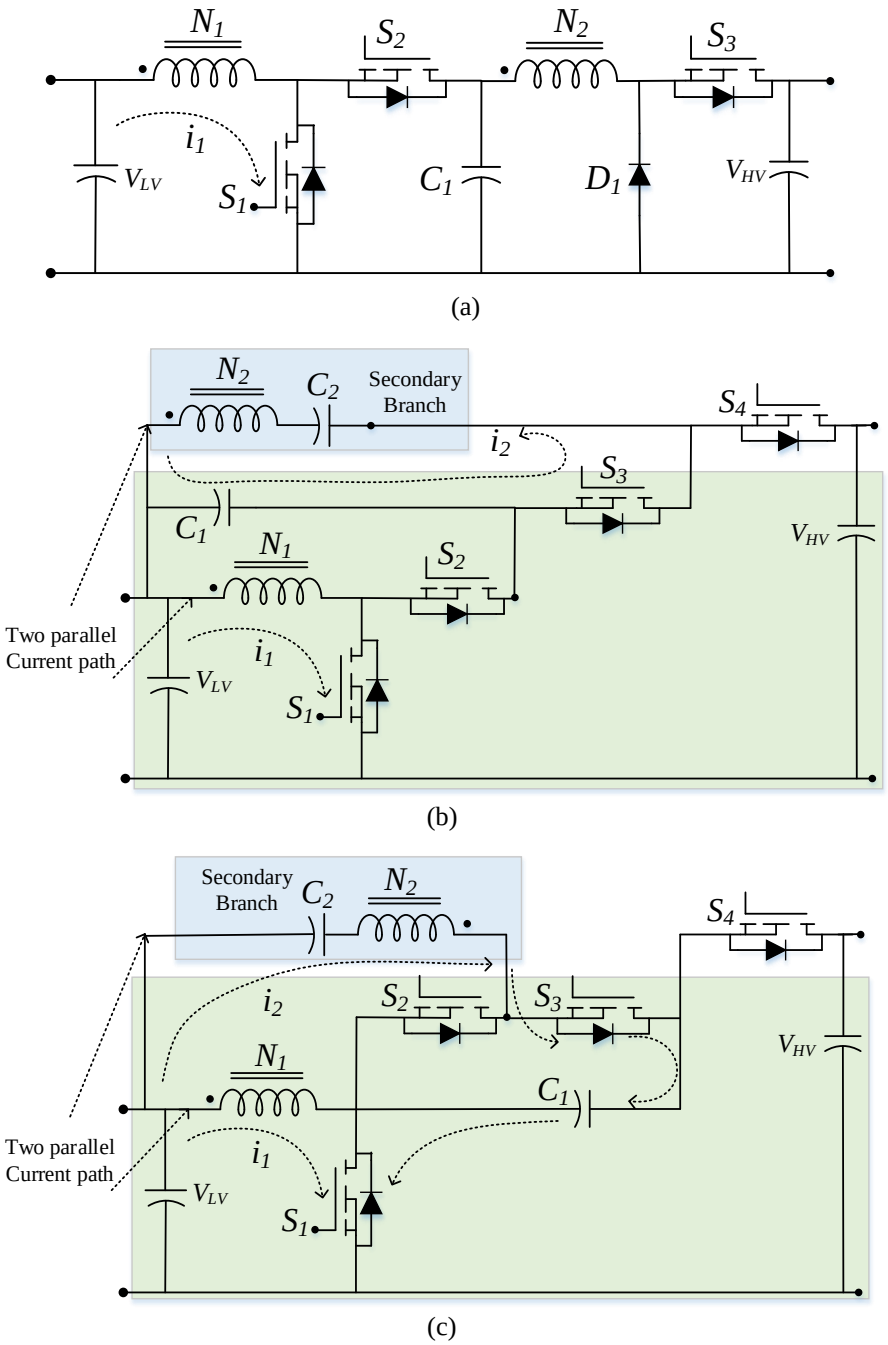


Fig. 4.2. BDC configurations using coupled inductor (a) Cascade structure by T. J. Liang *et al.* [35] (b) Position changing secondary branch [25] of coupled inductor (c) Rearrangement of secondary branch [27] of coupled inductor.

In this chapter a coupled inductor based bidirectional DC-DC (CIBDC) is proposed which is capable of achieving

(a) High conversion ratio both in buck and boost mode compared to proposals [23], [25], [27] and [31] for less winding turns ratio (*n=1*).

(b) Sharing current in either mode of operation due to parallel path structure utilizing coupled inductor and it do not need extra inductors [31]. This proposal has major advantage compared to the initial work [24] that coupled inductor winding is used to

create parallel path which shares current in both operating modes and helps in increasing conversion ratio, reducing coil size unlike an extra inductor path [24] which is unused during boosting operation.

(c) Clamped capacitor helps to recover leakage energy which helps in increasing efficiency.

(d) All switches are soft switched (ZVS) utilizing synchronous rectification concept which further improves efficiency.

(e) Low main switch current and voltage stress.

4.3. Current Sharing Characteristics

Current sharing structure means creating parallel paths for splitting large current into different parallel paths. This technique is particularly suitable at low voltage side of BDC where average magnitude and ripple content of current are also large. Thus, creating parallel paths not only helps to use lower rating coils and has flexibility in designing high voltage gain. If properly designed these parallel path structure also helps to reduce the ripple current magnitude which is established in consecutive chapter. In this chapter this technique is used to achieve high efficiency, high conversion factor (voltage gain) bidirectional DC-DC converter.

4.4. Proposed Topology of BDC using coupled inductor

In the proposed coupled inductor based bidirectional DC-DC converter (CIBDC), two secondary coupled inductor branches are used to achieve high voltage conversion factor, current sharing characteristics along with ZVS turn on of all active switches using synchronous rectification concept as shown in Fig. 4.3. The current topology uses six active MOSFET switches, four capacitors and coupled inductor to design CIBDC. To simplify the analysis, coupled inductor is modelled as ideal transformer with two secondary winding and magnetizing inductance L_m. Leakage inductance L_{lk} is also considered in the model. Circuit performance parameter like ripple voltage across capacitors are taken very small and ignored for simplifying analysis. The active MOSFET switches are considered as ideal switches. The ratio of magnetizing inductance (L_m) to (L_m+L_{lk}) i.e. $\frac{L_m}{L_m + L_{lk}}$ is considered as coupling coefficient (k) whereas $n = \frac{N_2}{N_1}$ is winding turns ratio. The steady state operating principle of proposed CIBDC is discussed using two operating modes i.e., boost and buck mode in continuous conduction (CCM).

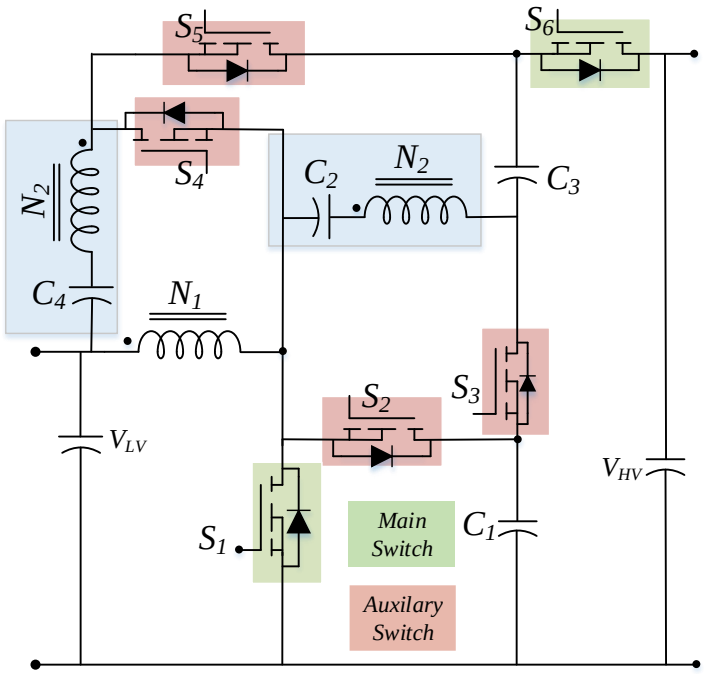


Fig.4.3. Proposed coupled-inductor based bidirectional converter (CIBDC) using two secondary branches.

4.4.1. Operating Principle of Boost Stage

In the boost mode of operation, power flows from low voltage source (V_{LV}) to the high voltage bus (V_{HV}). This mode of proposed CIBDC is divided into six subintervals based on switching states as shown in Fig. 4.4. The circuit operation of six subintervals is shown in Fig. 4.5 indicates each mode of operation. The high voltage side (V_{HV}) circuit model is considered to be a combination of output capacitor and resistance for verifying the boosting operation.

Mode 1 [t_0-t_1]: This mode starts from t_0 when S_4 and S_6 are turned off under ZVS condition as shown in Fig. 4.4. The current is diverted through antiparallel body diode of switch S_4 and S_6. Switch S_1 current flows through its body diode which makes S_1 voltage to be zero. The equivalent circuit of the mode is shown in Fig. 4.5 (a). At t_1 this mode ends when switch S_1 is turned ON.

Mode 2 [t_1-t_2]: Body diode of S_1 is conducting before starting of the mode and switch voltage is zero. Therefore, ZVS switch ON operation is achieved when switch S_1 is turned ON at beginning of this mode. The coupled inductor magnetizing current (i_{Lm}) starts rising. The polarity of coupled inductor secondary and tertiary winding makes the antiparallel body diode of switch S_3 and S_5 forward biased as shown in Fig. 4.5 (b). The capacitor C_1 and C_4 along with coupled inductor secondary, tertiary winding release its energy to capacitor C_2 and C_3. The load current is supplied by the output high voltage side capacitor (C_{HV}). In this mode soft switching operation of S_1, is achieved during turn ON similarly

like synchronous rectifier. The magnetizing and switch current equation in this mode are,

$$\frac{di_{Lm}}{dt}=\frac{di_{S1}}{dt}=\frac{v_{LV}}{L_m},\frac{di_{S3}}{dt}=\frac{v_{C2}-v_{C1}}{n^2L_1},\frac{di_{S5}}{dt}=\frac{v_{C3}+v_{C1}-v_{C4}-v_{LV}}{n^2L_1} \quad (4.1)$$

Mode 3 [t_2-t_3]: Switch S_3 and S_5 is turned ON at ZVS condition similar to S_1 in this mode. The magnetizing current (i_{Lm}) continues rising. The capacitor C_1 and C_4 along with coupled inductor secondary, tertiary winding continue to release its energy to capacitor C_2 and C_3 in this mode as shown in Fig. 4.5 (c). The load current is supplied by high voltage side capacitor similar to mode 2. By selecting the proper capacitance values of C_1 and C_2 along with coupled inductor secondary winding inductance (L_{sec}) half cycle quasi resonant current (t_r) operation is possible during DT_s interval (DT_s=t_r) which makes switch S_1 current stress lower [17]. Similarly, like synchronous rectifier, soft switching operation of S_3 and S_5 is achieved in this mode.

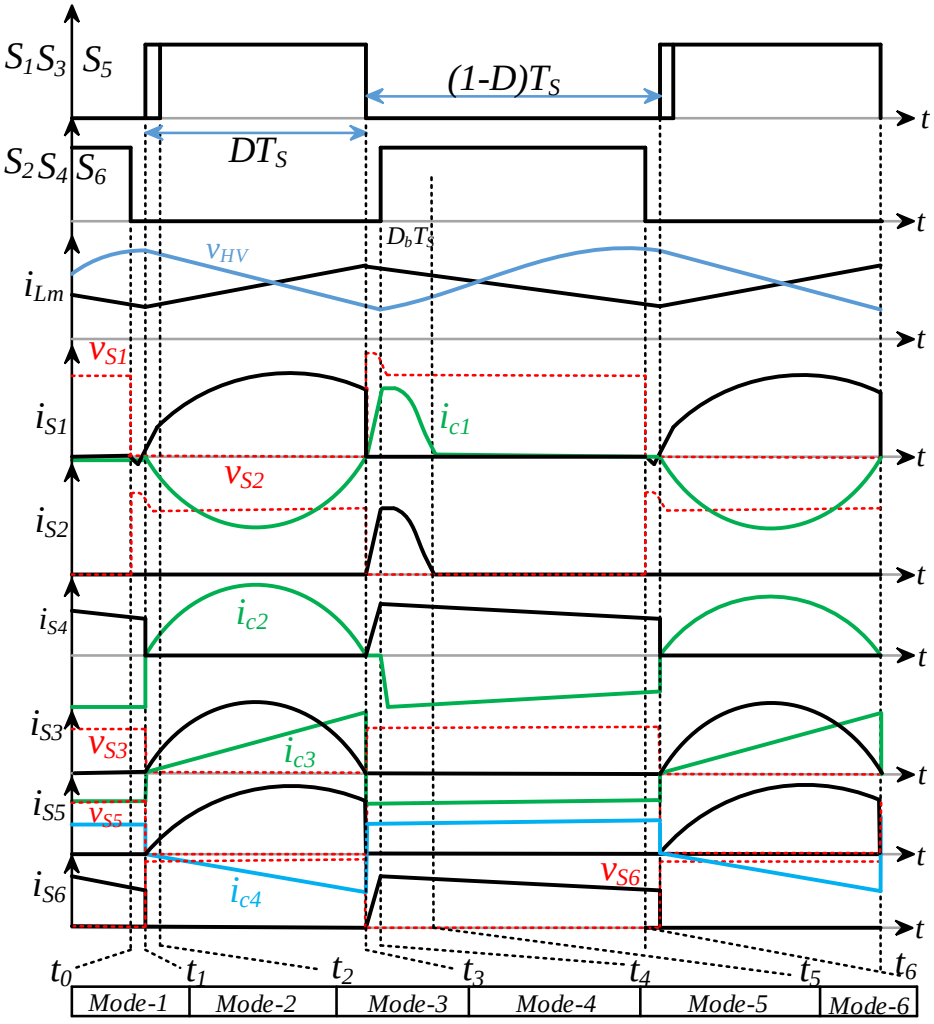


Fig. 4.4. Key waveforms of proposed CIBDC in boost mode

Mode 4 [t_3-t_4]: Switch S_1, S_3 and S_5 are turned OFF at the starting of this mode. The polarity of the coupled inductor primary winding as well as leakage inductance is reversed which

naturally turn ON the body diode of switch S_2, S_4 and high voltage side switch S_6 as shown in Fig. 4.5 (d). This makes these switch voltages to zero during this mode. The magnetizing energy stored in leakage inductance is transferred through body diode of switch S_2 to the capacitor C_1. During this mode capacitor C_4 is in charging mode which stores energy from tertiary winding of coupled inductor. The stored energy of the capacitor C_2, C_3 and coupled inductor secondary winding is discharged to the high voltage side capacitor and to the load. The magnetizing current starts falling during this mode.

Mode 5 [t_4-t_5]: This mode starts with S_2, S_4 and S_6 are turned ON at ZVS condition. The magnetizing current (i_{Lm}) continue to fall at this mode. The stored energy of capacitor C_2, C_3 and coupled inductor secondary winding is discharged to the high voltage side capacitor and load as shown in Fig. 4.5 (e). This mode ends when S_2 stops conduction as stored leakage energy is transferred to C_1.

$$\frac{di_{Lm}}{dt} = \frac{di_{S2}}{dt} = \frac{v_{C1} - v_{LV}}{L_m}, \frac{di_{S4}}{dt} = \frac{v_{LV} + v_{C4} - v_{C1}}{n^2 L_1} \frac{di_{S6}}{dt} = \frac{v_{HV} - v_{C3} - v_{C1}}{n^2 L_1} \quad (4.2)$$

Mode 6 [t_5-t_6]: This mode is same as mode 5 only switch S_2 will not carry any charging current to capacitor C_1 as shown in Fig. 4.5 (f).

4.4.2. Operating Principle of Buck Stage

In the buck mode operation power flows from high voltage (V_{HV}) source to low voltage (V_{LV}). The buck mode operation is divided into seven subintervals based on switching states as shown in Fig. 4.6. The circuit operation of seven subintervals are shown in Fig.4.7 which indicates each mode of operation. The low voltage side (V_{LV}) circuit model is considered to be a combination of output capacitor and resistance for verifying the buck operation. There are seven operating modes of buck operation within an operating cycle (T_s).

Mode 1 [t_0-t_1]:

This mode starts from t_0 when S_1, S_3 and S_5 are turned OFF as shown in Fig. 4.7 (a). Due to the polarity of coupled inductor windings the body diode of switch S_1, S_5 and S_6 become forward biased. In this mode coupled inductor secondary and tertiary winding current goes to high voltage side using body diode of switch S_6. This makes possible to turn ON S_6 under ZVS condition which is at the end of the mode at t_1. Switch S_1 and S_5 current decreases to zero value at the end of this mode. S_1 and S_5 is turned OFF at ZVS condition due to conduction of body diodes.

Mode 2 [t_1-t_2]:

Mode 2 starts from t_1 when S_6 is turned ON at ZVS condition as shown in Fig. 4.7 (b). During this mode the reverse current which is flowing into high voltage side decreased to zero value as shown in Fig. 4.6. At the end of this mode freewheeling stage of buck operation stops.

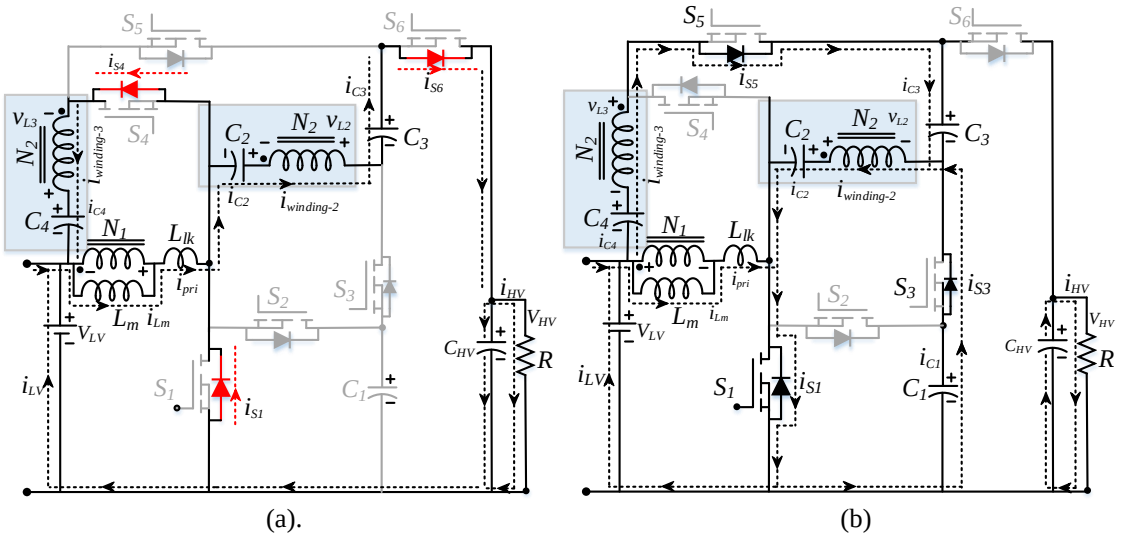
Mode 3 [t_2-t_3]:

As S_1 is already ON before the starting of this mode, it makes easier to flow power from high voltage side to low voltage side through coupled inductor and capacitor C_3, C_2. This mode is the active mode in buck operation. The body diode of switch S_2 and S_4 are turned ON based on coupled inductor polarity as shown in Fig. 4.7 (a). The magnetizing current (i_m) is rising in opposite direction if compared with boost mode of operation as shown in Fig. 4.6. Capacitor C_1 and C_4 charges in this mode through body diode of switch S_2 and S_4 respectively. The operation of this mode is mentioned in Fig. 4.7 (c). As body diode of S_2 and S_4 are in conduction therefore it is possible to turn ON these switches under ZVS condition. This mode ends at t_3 when S_2 and S_4 are turned ON. During this mode low voltage side capacitor and load current is supplied directly by high voltage side. The magnetizing and switch current equation are,

$$\frac{di_{Lm}}{dt}=\frac{di_{S2}}{dt}=\frac{v_{C1}-v_{LV}}{L_m},\ \frac{di_{S6}}{dt}=\frac{v_{HV}-v_{C2}-v_{C3}-v_{C1}}{n^2L_1},\ \frac{di_{S4}}{dt}=\frac{v_{C4}+v_{LV}-v_{C1}}{n^2L_1} \quad (4.3)$$

Mode 4 [t_3-t_4]:

In this mode switch S_2 and S_4 are turned ON at ZVS condition. The charging current path is same as mode 3. This mode ends when current through S_2 becomes zero and capacitor C_1 is fully charged. The circuit operation of this mode is shown in Fig. 4.7 (d).



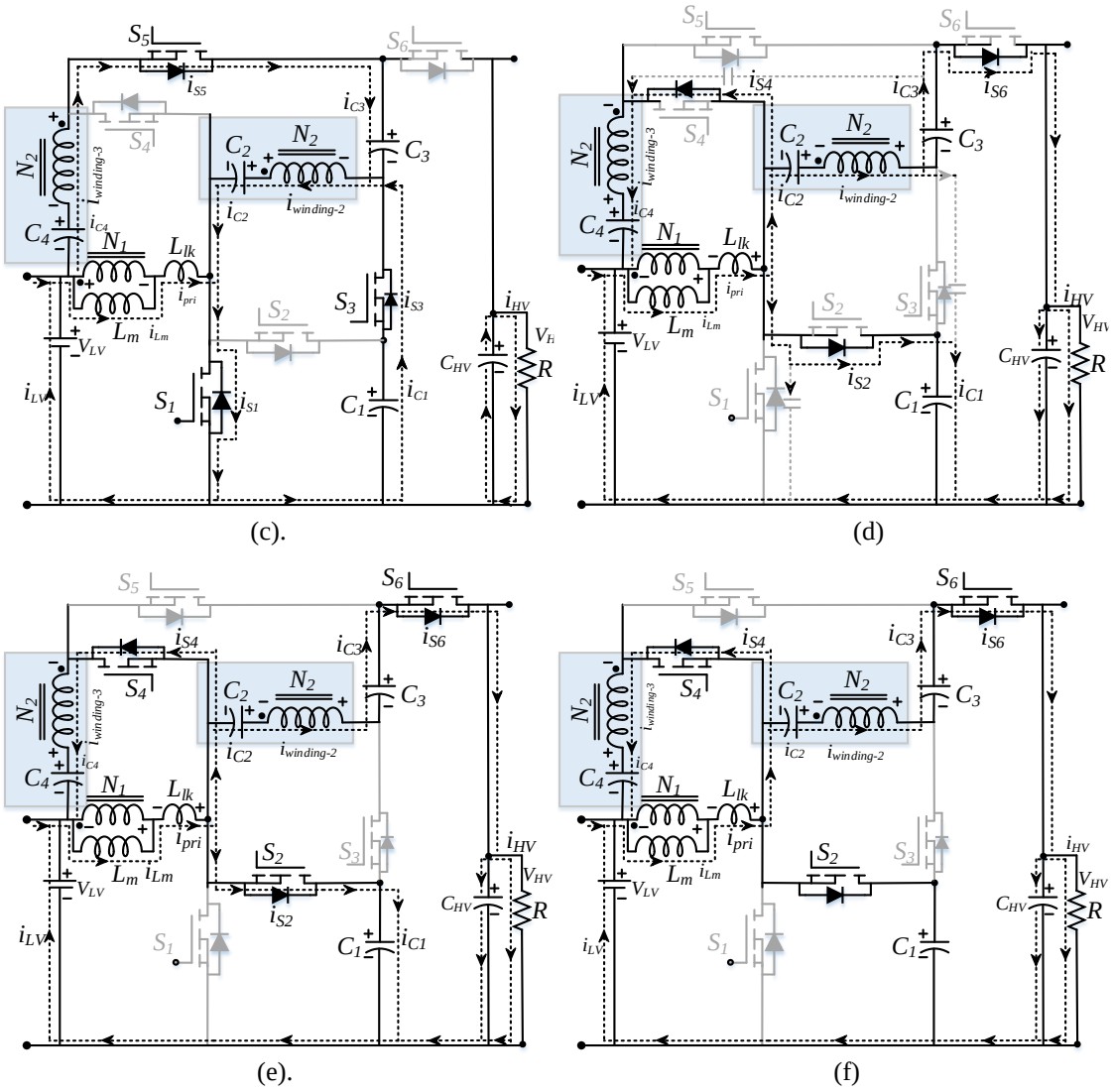


Fig. 4.5. Operation of proposed converter in boost mode: (a) Mode 1 [t_0-t_1] (b) Mode 2 [t_1-t_2] (c) Mode 3 [t_2-t_3] (d) Mode 4 [t_3-t_4]. (e) Mode 5 [t_4-t_5] (f) Mode 6 [t_5-t_6]

Mode 5 [t_4-t_5]:

As switch S_2 is ON and capacitor C_1 starts discharging in this mode as shown in Fig. 4.7 (e). The other branch current path remains same as mode 4. From mode 3 to mode 5 is the active stage of buck operation. This mode ends when witch S_6 is turned OFF at t_5.

Mode 6 [t_5-t_6]:

At the starting of this mode S_6 switch is turned OFF. The polarity of coupled inductor changes to maintain continuity of inductor current which makes body diode of switches S_1, S_3 and S_5 forward biased and starts conduction from the beginning of this mode. This state is similar to freewheeling state of conventional buck converter. In this mode capacitor C_1 discharges and capacitor C_2 and C_3 charges as shown in Fig. 4.7 (f). The magnetizing current starts decreasing in this mode as mentioned in Fig. 4.6. The switch voltages of S_1, S_3 and S_5 are zero as body diodes are in conduction. This makes possible

to achieve ZVS turn ON of corresponding switches in next mode. The magnetizing and switch current equation in this mode are,

$$\frac{di_{Lm}}{dt} = \frac{v_{LV}}{L_m}, \frac{di_{S3}}{dt} = \frac{v_{C2} - v_{C1}}{n^2 L_1}, \frac{di_{S5}}{dt} = \frac{v_{C3} + v_{C1} - v_{C4} - v_{LV}}{n^2 L_1} \quad (4.4)$$

Mode 7 [t_6-t_7]:

This mode starts with turning ON of switches S_1, S_3 and S_5 under ZVS condition. The same operation like mode 6 continues in this mode. This is also like a freewheeling mode of conventional buck converter. This mode ends when switches S_3, S_5 and S_1 are turned OFF and mode-1 repeats the cycle by turning ON body diode of switches S_5 and S_6. The circuit of this mode is shown in Fig. 4.7(g).

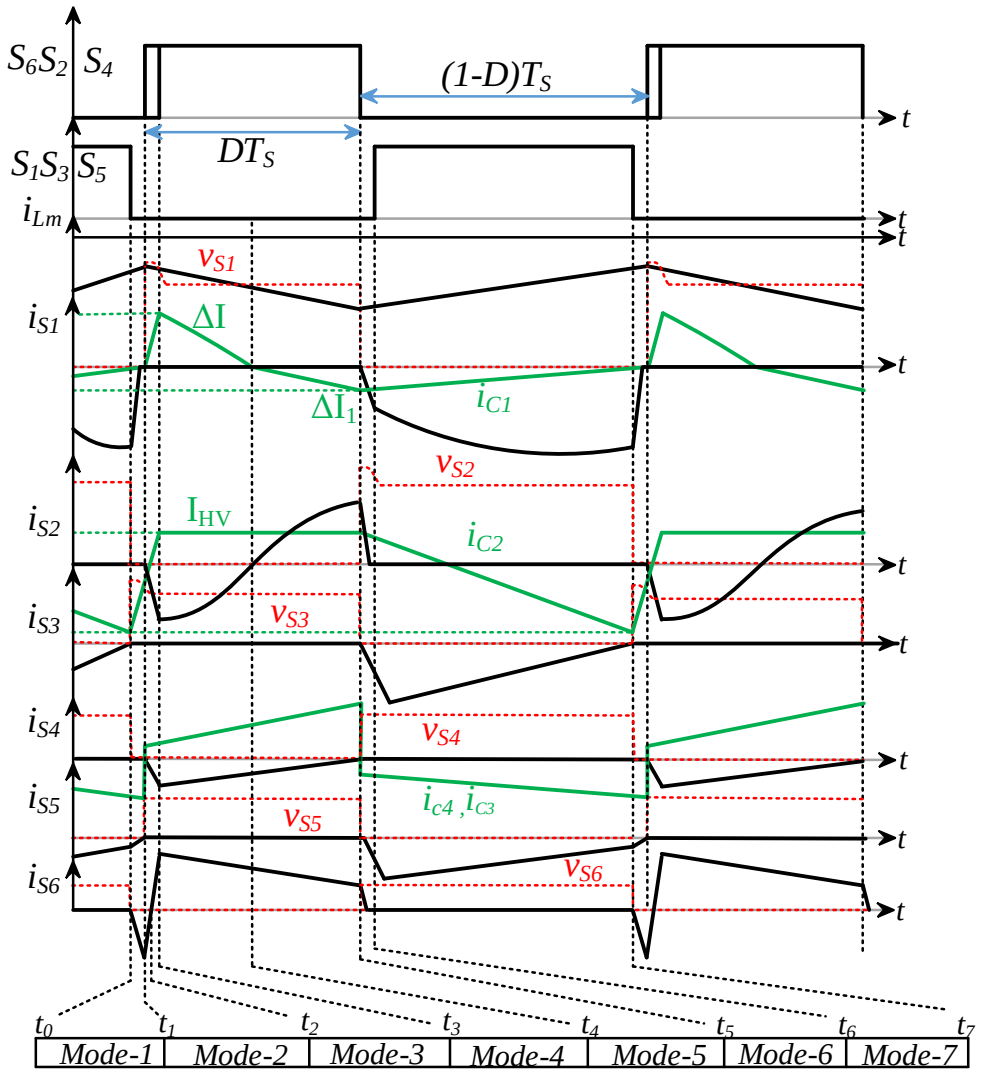
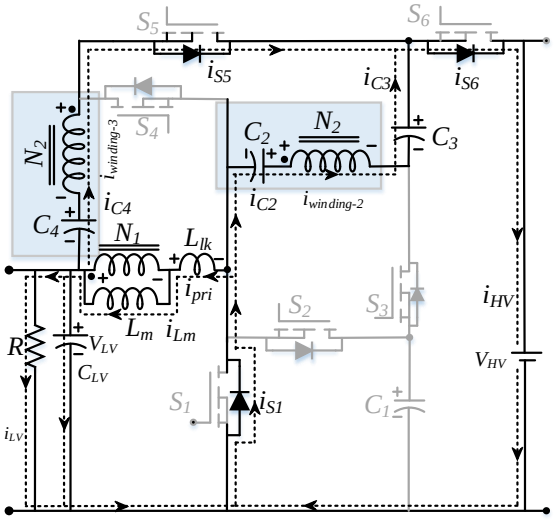
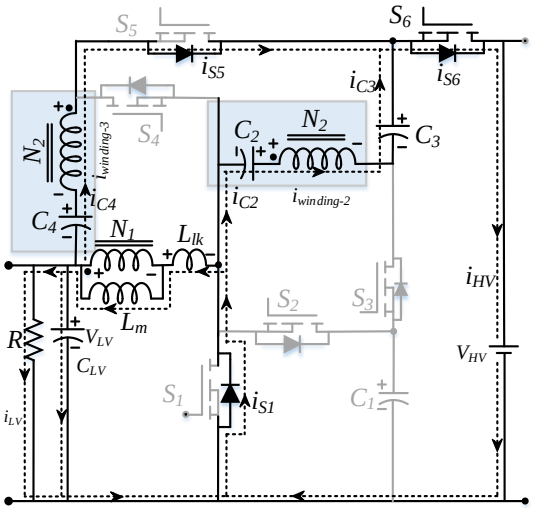


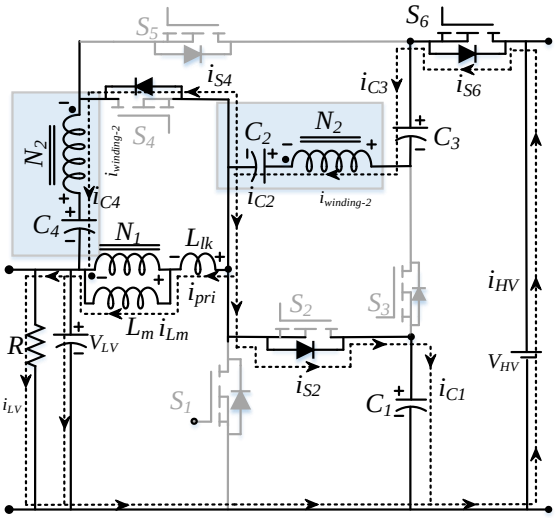
Fig. 4.6. Key waveforms of proposed CIBDC in buck mode


S5
S6
iS5
iC3
iS6
S4
C2
N2
C3
iwinding-3
iC4
iC2
iwinding-2
C4
N1
Llk
ipri
Lm
iLm
S2
S3
iHV
R
VLV
CLV
VHV
S1
iS1
C1
iLV

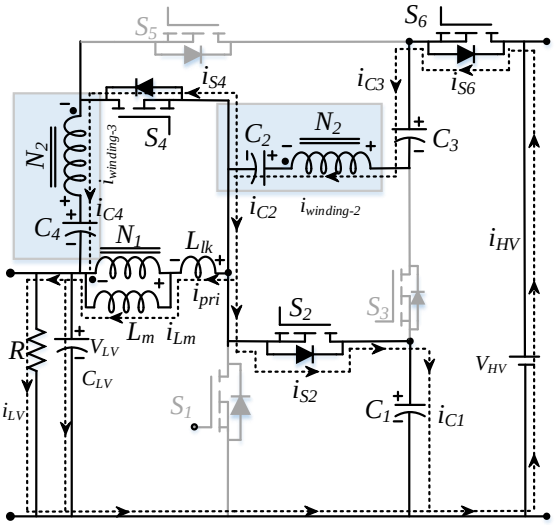
(a).


S5
S6
iS5
iC3
iS6
S4
C2
N2
C3
iwinding-3
iC4
iC2
iwinding-2
C4
N1
Llk
Lm
S2
S3
iHV
R
VLV
CLV
VHV
S1
iS1
C1
iLV

(b)


S5
S6
iS4
iC3
iS6
S4
C2
N2
C3
iwinding-2
iC4
iC2
iwinding-2
C4
N1
Llk
ipri
Lm
iLm
S2
S3
iHV
R
VLV
VHV
S1
iS2
C1
iC1
iLV

(c)


S5
S6
iS4
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C2
N2
C3
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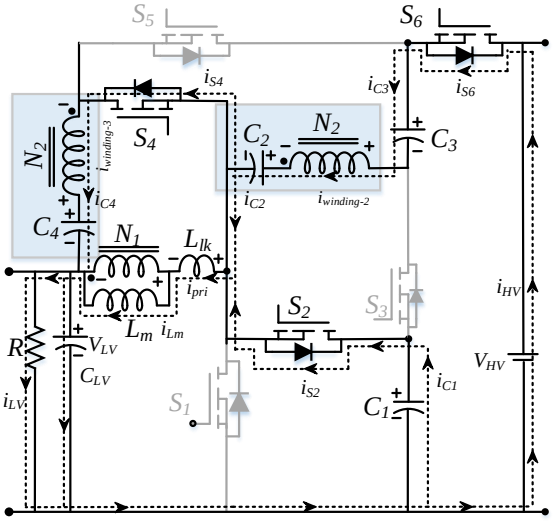
iwinding-2
C4
N1
Llk
ipri
Lm
iLm
S2
S3
iHV
R
VLV
CLV
VHV
S1
iS2
C1
iC1
iLV

(d)


S5
S6
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C4
N1
Llk
ipri
Lm
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VLV
CLV
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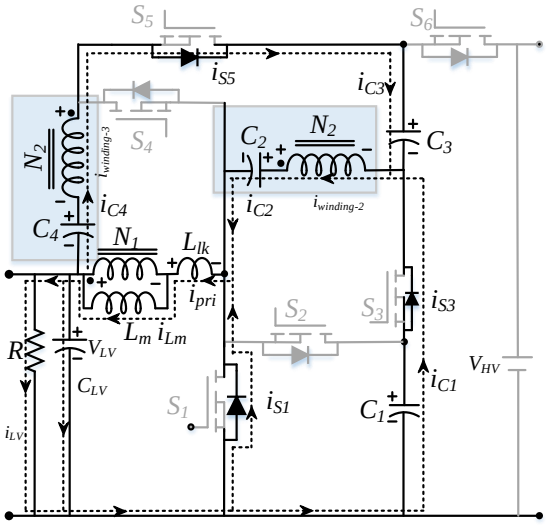
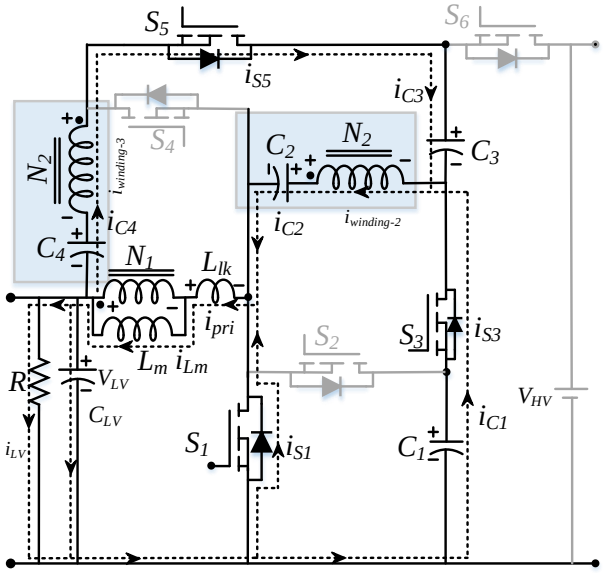
iS2
C1
iC1
iLV

(e).


S5
S6
iS5
iC3
S4
C2
N2
C3
iwinding-3
iC4
iC2
iwinding-2
C4
N1
Llk
ipri
Lm
iLm
S2
S3
iS3
R
VLV
CLV
VHV
S1
iS1
C1
iC1
iLV

(f)



(g)

Fig. 4.7. Operation of proposed converter in buck mode: (a) Mode 1 [t_0-t_1] (b) Mode 2 [t_1-t_2] (c) Mode 3 [t_2-t_3] (d) Mode 4 [t_3-t_4]. (e) Mode 5 [t_4-t_5] (f) Mode 6 [t_5-t_6] (g) Mode 7 [t_6-t_7]

4.4.3. Voltage Gain, Boundary condition and Comparison

4.4.3.1 Gain in Boost Mode

The boost mode operation of the proposed CIBDC is shown in Fig. 4.5. Form Fig. 4.5 (b) which is same as switch ON operation of conventional boost converter, the voltage equations are derived where V_{Lm}, V_{L2}, V_{L3}, V_{Lk}, are main winding voltage, secondary winding voltage, tertiary winding voltage and leakage inductance voltage respectively.

$$v_{\mathrm{Lm}} = v_{\mathrm{L1}} = \frac{L_{\mathrm{m}}}{L_{\mathrm{m}} + L_{\mathrm{lk}}} v_{\mathrm{LV}} = k v_{\mathrm{LV}} \tag{4.5}$$

$$v_{\mathrm{Lk}} = \frac{L_{\mathrm{lk}}}{L_{\mathrm{m}} + L_{\mathrm{lk}}} v_{\mathrm{LV}} = (1-k) v_{\mathrm{LV}} \tag{4.6}$$

$$v_{\mathrm{L2}} = v_{\mathrm{L3}} = nk v_{\mathrm{LV}} \tag{4.7}$$

Switch ON and OFF time voltage equations of secondary loop as well as third loop are required to apply volt-second balance in coupled inductor primary winding from which C_1 and C_4 voltages can be derived.

$$v_{\mathrm{C_1}} = \frac{2\mathrm{D}(k-1)+(2-k)}{1-\mathrm{D}} v_{\mathrm{LV}} \tag{4.8}$$

$$v_{\mathrm{C_4}} = \frac{k\mathrm{D}(n+1)}{1-\mathrm{D}} v_{\mathrm{LV}} \tag{4.9}$$

Similarly, from coupled inductor secondary, tertiary winding volt-sec balance, capacitor C_2, C_3 and high voltage side capacitor voltage can be derived.

$$v_{C_2} = \left(nk + \frac{2\mathrm{D}(k\text{-}1)+(2\text{-}k)}{1\text{-}\mathrm{D}} \right) v_{\mathrm{LV}} \tag{4.10}$$

$$v_{C_3} = \left(\frac{\mathrm{D}k(n\text{-}2)+k(\mathrm{D}+1)+(\mathrm{D}\text{-}1)}{\mathrm{D}(1\text{-}\mathrm{D})} \right) v_{\mathrm{LV}} \tag{4.11}$$

For ideal coupling coefficient k=1, the boosting voltage gain of CIBDC can be derived which is mentioned in equation. (4.13).

$$v_{\mathrm{HV}} = v_0 = \frac{2nk+4\mathrm{D}(k-1)+2(2-k)}{1\text{-}\mathrm{D}} v_{\mathrm{LV}}$$

(4.12)

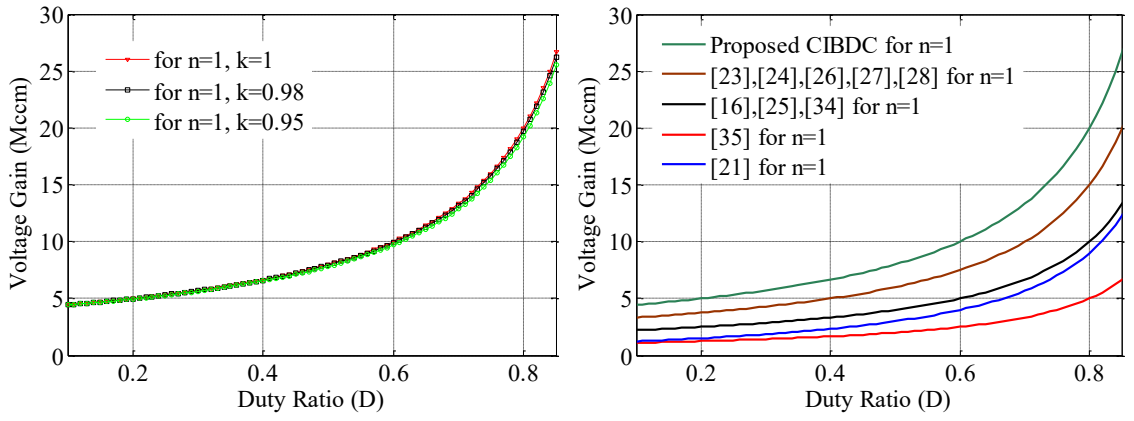
$$\mathrm{M}_{\mathrm{CCM}} = \frac{v_{\mathrm{HV}}}{v_{\mathrm{LV}}} = \frac{2n+2}{1\text{-}\mathrm{D}} \tag{4.13}$$

$$v_{C_1} = \frac{v_{\mathrm{LV}}}{1\text{-}\mathrm{D}} \tag{4.14}$$

$$v_{C_2} = \left(n + \frac{1}{1\text{-}\mathrm{D}} \right) v_{\mathrm{LV}} \tag{4.15}$$

$$v_{C_4} = \left(\frac{\mathrm{D}(n+1)}{1\text{-}\mathrm{D}} \right) v_{\mathrm{LV}} \tag{4.16}$$

For different coupling coefficient k value, the boosting voltage gain of proposed CIBDC is shown in Fig. 4.8 (a). The boosting gain ($\mathrm{M_{CCM}}$) of proposed CIBDC is compared to other topologies for *n=1* as shown in Fig. 4.8 (b). The voltage gain ($\mathrm{M_{CCM}}$) is derived (4.17) in terms of normalized time constant from CCM and DCM voltage gain and output capacitor charge balance equation.



(a). (b)

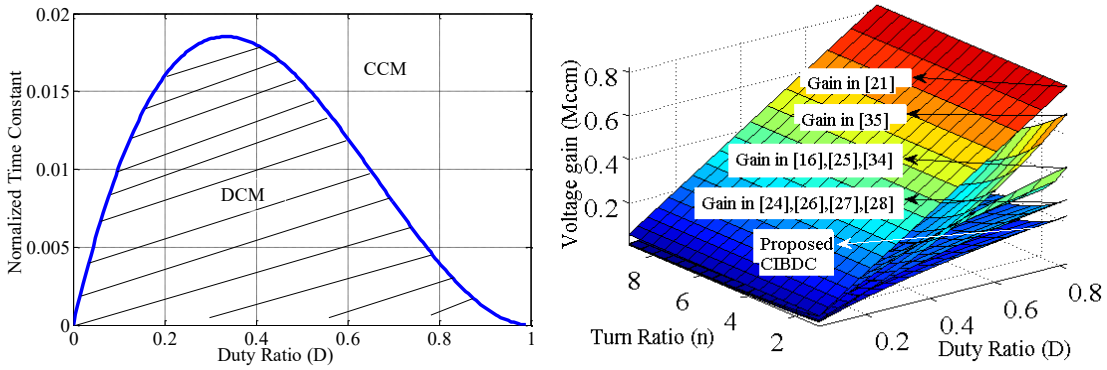
Fig.4.8. $\mathrm{M_{CCM}}$ (a) for different coupling coefficient (k), (b) Comparison of $\mathrm{M_{CCM}}$ of CIBDC and existing topologies @k=1 and n=1

$$\mathrm{M}_{CCM} = (n+1) \pm \sqrt{(n+1)^2 + \frac{\mathrm{D}^2}{2\tau_{\mathrm{Lm}}}} \tag{4.17}$$

From the boundary condition of CCM and DCM mode the normalized time constant at boundary (τ_{Lmb}) is derived.

$$\tau_{Lmb} = \frac{(1-D)^2 D}{2(n+1)^2} \tag{4.18}$$

Thus, correct selection of normalized time constant $\frac{L_m}{R_L T_s} = \tau_{Lm} > \tau_{Lmb}$, which depends on magnetising inductance (L_m), switching frequency (f_{sw}) and load resistance (R) is essential for ensuring CCM operation of CIBDC as shown in Fig. 4.9 (a).



(a) (b)

Fig. 4.9. (a) Normalized time constant at boundary condition in boost mode when *k=1*. (b)Voltage gain comparison of CIBDC in buck mode.

4.4.3.2 Gain in Buck Mode

The buck mode operation of the proposed CIBDC is shown in Fig. 4.7. Form Fig. 4.7 (b) which is same as switch ON operation of conventional buck converter, the voltage equations are derived from volt-sec balance of primary, secondary winding like in boost mode. Loop voltage equations are essential for both switch ON and OFF time. The capacitor voltage equations are.

$$v_{C_4} = \frac{k(1-D)(n+1)}{D} v_{LV} \tag{4.19}$$

$$v_{C_1} = \frac{k + 2D(1-k)}{D} v_{LV} \tag{4.20}$$

$$v_{LV} = v_0 = \frac{D}{2nk + 4D(k-1) + 2(2-k)} v_{HV} \tag{4.21}$$

Taking coupling coefficient *k*=1, the voltage gain in buck mode is derived from equation. (4.21) and gain is compared with other topologies as shown in Fig. 4.9 (b).

$$M_{CCM} = \frac{v_{LV}}{v_{HV}} = \frac{D}{2n+2} \tag{4.22}$$

$$v_{C_1} = \frac{v_{LV}}{D} \tag{4.23}$$

$$v_{C_4} = \left(\frac{(n+1)(1-D)}{D} \right) v_{LV} \tag{4.24}$$

4.4.4. Voltage Stress, current stress and comparison

4.4.4.1. Switch voltage stress

There are six switches in the proposed CIBDC. Switch voltage stress (V_{sw}) of S_1 the converter is

$$v_{S1} = \frac{v_{LV}}{1-D} = \frac{v_{HV}}{2n+2} \tag{4.25}$$

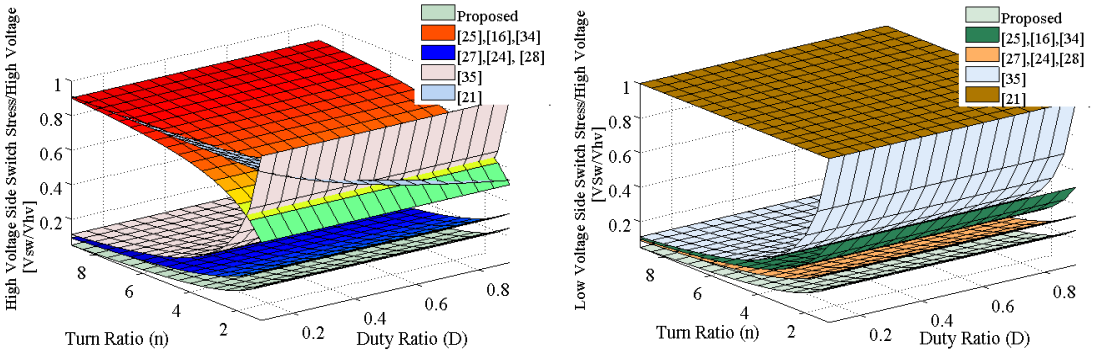
Similarly, switch voltage stress for S_2, S_3, S_4, S_5 and S_6 are respectively

$$v_{S2} = v_{S6} = \frac{v_{HV}}{2n+2},\ v_{S3} = v_{S4} = \frac{v_{HV}}{2}\ ,\ v_{S5} = \frac{2n+1}{2n+2} v_{HV} \tag{4.26}$$

The switch voltage stress comparison is mentioned in Table-4.1 and represented graphically in Fig. 4.10(a) and Fig. 4.10(b).

TABLE -4.1
COMPARISON OF VOLTAGE STRESS

	Proposed	[25], [16], [34]	[24], [26],[27], [28]	[35]	[21]
High Voltage Side (S_6) Switch Stress	$\frac{v_{HV}}{2n+2}$	$\frac{n}{n+1} v_{HV}$	$\frac{v_{HV}}{n+2}$	$\frac{v_{HV}}{n}$	$\frac{v_{HV}}{1+D}$
Low Voltage Side (S_1) Switch Stress	$\frac{v_{HV}}{2n+2}$	$\frac{v_{HV}}{n+1}$	$\frac{v_{HV}}{n+2}$	$\frac{v_{HV}}{n}$	v_{HV}



(a) (b)

Fig. 4.10. Switch voltage stress comparison of (a) high voltage side (S_6) (b) low voltage side (S_1) of CIBDC in CCM.

4.4.4.2. Switch Current Stress

Boost Mode

The magnetizing current (i_{Lm}) value can be calculated from of high voltage side capacitor (C_{HV}) charge balance in CCM. The magnetizing current value is

$$i_{\mathrm{Lm}} = \frac{v_{\mathrm{HV}}(n+1)}{(1\text{-}\mathrm{D})\mathrm{R}_L} = \frac{2v_{\mathrm{LV}}(n+1)^2}{(1\text{-}\mathrm{D})^2\mathrm{R}_L} \tag{4.27}$$

The maximum of magnetizing current (i_{Lm}) value is

$$i_{\mathrm{Lm\_Peak}} = i_{\mathrm{Lm}} + \frac{\Delta i_{\mathrm{Lm}}}{2} = \frac{2v_{\mathrm{LV}}(n+1)^2}{(1\text{-}\mathrm{D})^2\mathrm{R}_L} + \frac{v_{\mathrm{LV}}\mathrm{DT_s}}{2\mathrm{L_m}} \tag{4.28}$$

Coupled inductor winding-2 current is necessary to find peak switch current (i_{S1}) during ON time

$$i_{S1\_Peak} = i_{\mathrm{Lm\_Peak}} + (n+1)i_{winding2\_Peak} \tag{4.29}$$

The proposed CIBDC is capable of achieving low switch current stress like proposed in [17] by properly selecting C_1, C_2 values and half cycle resonating time. RMS current of switch S_1 can also be minimized.

Thus, the peak current of low voltage switch S_1 is

$$i_{\mathrm{S1\_Peak}} \cong \frac{2v_{\mathrm{LV}}(n+1)^2}{(1\text{-}\mathrm{D})^2\mathrm{R}_L} + \frac{v_{\mathrm{LV}}}{1-\mathrm{D}}\sqrt{\frac{\mathrm{C}_{eq}}{\mathrm{L}_2}} + \frac{2v_{\mathrm{LV}}(1+n)}{\mathrm{DR}_L} \tag{4.30}$$

Similarly, the peak current for high voltage side switch S_6 is

$$i_{\mathrm{S6\_Peak}} = \frac{2v_{\mathrm{LV}}(n+1)^2}{n(1\text{-}\mathrm{D})^2\mathrm{R}_L} + \frac{v_{\mathrm{LV}}\mathrm{DT_s}}{2n\mathrm{L_m}} \tag{4.31}$$

The peak switch currents of S_3, S_2 and S_4 are respectively,

$$i_{\mathrm{S2\_Peak}} = i_{\mathrm{S4\_Peak}} = i_{\mathrm{Lm\_Peak}}$$

$$i_{\mathrm{S3\_Peak}} \cong \frac{v_{\mathrm{LV}}}{1-\mathrm{D}}\sqrt{\frac{\mathrm{C}_{eq}}{\mathrm{L}_2}} \tag{4.32}$$

The RMS values of switch currents during boost mode are derived from current waveform as shown in Fig. 4.4

$$i_{\mathrm{S1\text{-}RMS}} \cong \frac{1+n}{1-\mathrm{D}} i_{\mathrm{Lm}}\sqrt{\mathrm{D}}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{\mathrm{Lm}}}{i_{\mathrm{HV}}}\right)^2\left(\frac{1-\mathrm{D}}{n+3}\right)^2} \tag{4.33}$$

$$i_{\mathrm{S3\text{-}RMS}} = \sqrt{\frac{1}{\mathrm{T}_s}\int_0^{\mathrm{DT_s}}\left(v_{ceq}\sqrt{\frac{\mathrm{C_{eq}}}{\mathrm{L}_2}}\sin\frac{2\pi}{\mathrm{T_s}}\mathrm{t}\right)^2 dt} \tag{4.34}$$

$$i_{\text{S2-RMS}} = \frac{2+2n}{1-D}\sqrt{\text{D}_\text{b}}\, i_{\text{HV}} \tag{4.35}$$

$$i_{\text{S4-RMS}} = \frac{i_{\text{Lm}}}{n}\sqrt{1-\text{D}} \tag{4.36}$$

$$i_{\text{S5-RMS}} = \sqrt{\frac{1}{\text{T}_s}\int_0^{\text{DT}_s}\left(v_{ceq}\sqrt{\frac{\text{C}_{\text{eq1}}}{\text{L}_{\text{eq}}}}\sin\frac{2\pi}{\text{T}_\text{s}}\text{t}\right)^2 dt} \tag{4.37}$$

$$i_{S6-\text{RMS}} = i_{\text{Lm-min}}\sqrt{(1-\text{D})\left[1+\frac{1}{3}\left(\frac{\Delta i_{\text{Lm}}}{i_{\text{Lm-min}}}\right)^2\right]} \tag{4.38}$$

Buck Mode

In the buck mode operation of proposed CIBDC, the switch current stress of S_1 is same as peak magnetising current as it only conducts during freewheeling time like conventional buck converter.

$$i_{\text{S1\_Peak}} = i_{\text{S2\_Peak}} = i_{\text{Lm\_Peak}} \tag{4.39}$$

Similarly, the peak current of high voltage side switch S_6 is

$$i_{\text{S6\_Peak}} \cong \frac{\text{D}nv_{\text{LV}}}{(1-\text{D})\text{L}_2}(t_3 - t_2) \tag{4.40}$$

Where, t_3-t_2 =D_cT_s

The average magnetizing current during buck mode of operation is

$$i_{\text{Lm}} = \frac{n+1-n\text{D}}{n+1}i_{\text{LV}} \text{ and } \Delta i_{\text{Lm}} = \frac{v_{\text{LV}}(1\text{-D})\text{T}_s}{\text{L}_m} \tag{4.41}$$

The RMS values of switch currents during buck mode are derived from current waveform as shown in Fig. 4.6.

$$i_{S1-\text{RMS}} = i_{\text{Lm-min}}\sqrt{1-\text{D}+\frac{2}{i_{\text{Lm-min}}}+\left(\frac{\Delta i_{\text{Lm}}}{i_{\text{Lm-min}}}\right)^2} \tag{4.42}$$

$$i_{\text{S2-RMS}} = \frac{\text{D}}{6(n+1)}\sqrt{\frac{5\text{D}}{3}}i_{\text{LV}} \tag{4.43}$$

$$i_{\text{S3-RMS}} = \frac{\text{D}\sqrt{1-\text{D}}}{6\sqrt{3}(n+1)}i_{\text{LV}} \tag{4.44}$$

$$i_{\text{S4-RMS}} = \frac{n\text{D}\sqrt{\text{D}}}{2\sqrt{3}(n+1)}i_{\text{LV}} \tag{4.45}$$

$$i_{\text{S5-RMS}} = \frac{n\text{D}\sqrt{1\text{-D}}}{2\sqrt{3}(n+1)}i_{\text{LV}} \tag{4.46}$$

$$i_{\text{S6-RMS}} = \frac{i_{\text{Lm-min}}}{n}\sqrt{\text{D} + \frac{\text{D}}{3}\left(\frac{\Delta i_{\text{Lm}}}{i_{\text{Lm-min}}}\right)} \tag{4.47}$$

4.4.5. Winding current and theoretical loss calculation

The RMS currents of capacitor C_1, C_2, C_3 and C_4 are calculated from ideal capacitor current waveforms in both buck and boost mode. Similarly, winding RMS currents are also derived in both the operating modes. The capacitors RMS current in boost mode are given by

$$i_{\text{c}_1(\text{RMS})} = \sqrt{\text{i}^2_{\text{pri\_min}} \times (\text{D}_\text{b}) + \frac{v^2_{\text{c1}}}{2\pi^2}\frac{\text{c}_{\text{eq}}}{\text{L}_2}\text{D-}\frac{\sin 4\pi\text{D}}{4\pi}} \tag{4.48}$$

$$i_{\text{c}_2(\text{RMS})} = i_{\text{winding-2 (RMS)}} = \sqrt{i^2_{\text{HV}} \times (\text{1-D-D}_\text{b}) + \frac{v^2_{\text{c1}}}{2\pi^2}\frac{\text{c}_{\text{eq}}}{\text{L}_2}\text{D-}\frac{\sin 4\pi\text{D}}{4\pi}} \tag{4.49}$$

$$i_{\text{c}_3(\text{RMS})} = i_{\text{c}_4(\text{RMS})} = i_{\text{winding-3(RMS)}} = \sqrt{i^2_{\text{HV}}\frac{1-\text{D}}{3D}(\text{4-D})} \tag{4.50}$$

Where, $\text{D}_\text{b} = \frac{v_{\text{c1}}\text{D}}{4\pi\text{i}_{\text{HV}}}\sqrt{\frac{\text{c}_{\text{eq}}}{\text{L}_2}}\left(\text{1-cos}\left(2\pi\text{D}\right)\right)\times\left(\frac{\text{1-D}}{n+1}\right)$

The RMS current of primary winding of proposed CIBDC is given by

$$i_{\text{pri(RMS)}} = \sqrt{\left[(\text{x}^2 + \text{x}\left(\text{x-I}_{\text{pri\_min}}\right)(\text{1-D}) + \frac{\left(\text{x-I}_{\text{pri\_min}}\right)^2}{3}(\text{1-D}) + \frac{v_{\text{c1}}}{\pi}\sqrt{\frac{\text{c}_{\text{eq}}}{\text{L}_2}}\left(\text{1-cos}\left(2\pi\text{D}\right)\right) + \frac{v^2_{\text{c1}}}{2\pi^2}\frac{\text{c}_{\text{eq}}}{\text{L}_2}\text{D-}\frac{\sin 4\pi\text{D}}{4\pi})\right]}$$

Where, $x \cong \frac{2n+2}{\text{1-D}} i_{\text{HV}}$ (4.51)

Again, during the buck mode of operation, the capacitors RMS currents are given by

$$i_{\text{c}_1(\text{RMS})} = \sqrt{\frac{\Delta i^2\text{D}}{2} + \Delta i_1^2\left(1-\frac{\text{D}}{2}\right)} \tag{4.52}$$

Where, $\Delta i = \frac{n+1}{2\text{L}_2}\text{T}_\text{s}$, and $\Delta i_1 = \frac{n+1}{4\text{L}_2}\text{T}_\text{s}\frac{\text{D}}{1-0.5\text{D}}$

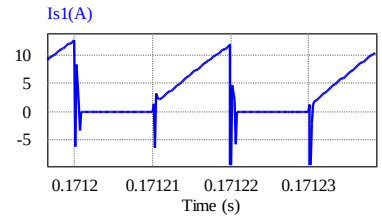
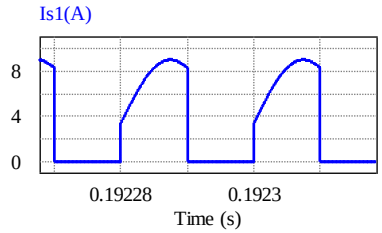
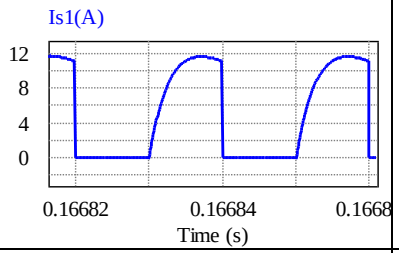
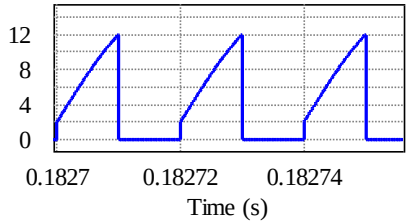
$$i_{\text{c}_2(\text{RMS})} = i_{\text{winding-2 (RMS)}} \cong i_{\text{c}_3(\text{RMS})} = i_{\text{HV}}\sqrt{\text{D}+\frac{4\text{D}^2}{\text{1-D}}} \tag{4.53}$$

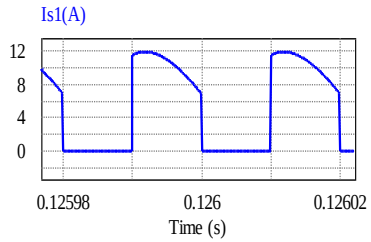
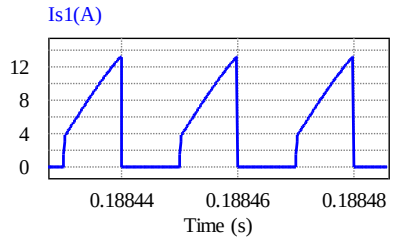
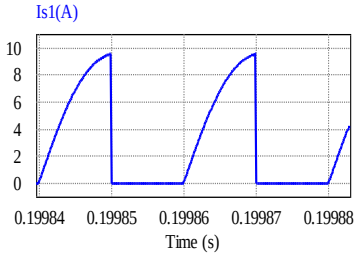
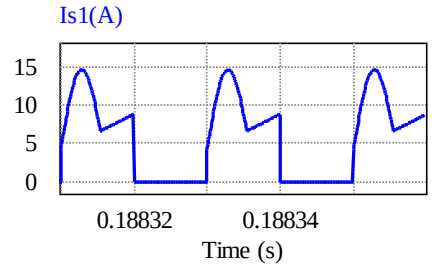
$$i_{\text{c}_4(\text{RMS})} = i_{\text{winding-3 (RMS)}} = 2i_{\text{HV}}\text{D}\left(\frac{2}{\text{1-D}}+n\right)\sqrt{1+\frac{1}{\text{D}}} \tag{4.54}$$

Switch current stress of different topologies is performed and shown in Table-4.2

TABLE-4.2

Comparison of Switch Current Stress, Gain, Switches and Efficiency @ 200W

Topology	Main Switch Peak Current at LV side		Main Switch RMS Current at LV side, no of components, Gain and Efficiency		Switch Selection @ 200W Converter Specification	Stress
	Buck	Boost	Buck	Boost		
Proposed	$\frac{n+1-n\mathrm{D}}{n+1} i_{\mathrm{LV}} + \frac{v_{\mathrm{LV}}(1\text{-}\mathrm{D})\mathrm{T}_s}{2\mathrm{L}_m}$ ***Current Waveform***: 	$\frac{2v_{\mathrm{LV}}(n+1)^2}{(1\text{-}\mathrm{D})^2\mathrm{R}} + \frac{v_{\mathrm{LV}}}{1-\mathrm{D}}\sqrt{\frac{C_{eq}}{\mathrm{L}_2}} + \frac{2v_{\mathrm{LV}}(1+n)}{\mathrm{DR}}$ ***Current Waveform***: 	$i_{\text{Lm-min}}\sqrt{1-\mathrm{D}+\frac{2}{i_{\text{Lm-min}}}+\left(\frac{\Delta i_{\mathrm{Lm}}}{i_{\text{Lm-min}}}\right)^2}$ ***Capacitor***:4 ***Switches***:6, ***Efficiency***: 95.6% ***Buck gain***: $=\frac{\mathrm{D}}{(2+2n)}$	$\frac{1+n}{1-D}\sqrt{D}i_{\mathrm{Lm}}\sqrt{1+\frac{1}{12}\left(\frac{\Delta i_{\mathrm{Lm}}}{i_{\mathrm{HV}}}\right)^2\left(\frac{1-D}{n+3}\right)^2}$ or $\approx\frac{2+n+\mathrm{D}}{(2+2n)\sqrt{\mathrm{D}}} i_{\mathrm{LV}}$ ***Boost gain***: $=\frac{2+2n}{(1-\mathrm{D})}$ ***Efficiency:*** 96.13%	FQP34N20 V_{ds}=200V, R_{ds}=0.075 Ω I_d=31A. f_{sw}=50kHz *n=1* V_{in}=48V V_o=384V	Low
[27]	$\frac{v_{\mathrm{LV}}(n+1)(2+n)}{(1\text{-}\mathrm{D})^2\mathrm{R}} + \frac{v_{\mathrm{LV}}(1\text{-}\mathrm{D})\mathrm{T}_s}{2\mathrm{L}_m}$ ***Current Waveform***: 	$\cong\frac{v_{\mathrm{LV}}(n+1)(2+n)}{(1\text{-}\mathrm{D})^2\mathrm{R}} + \frac{v_{\mathrm{LV}}}{1-\mathrm{D}}\sqrt{\frac{C_{eq}}{L_2}}$ ***Current Waveform***: Is1(A) 	$\frac{2+n-\mathrm{D}}{(2+n)\sqrt{1-\mathrm{D}}} i_{\mathrm{LV}}$ ***Capacitor***:2 ***Switches***:4, ***Efficiency***: 95.61% ***Buck gain***: $=\frac{\mathrm{D}}{(2+n)}$	$\frac{1+n+\mathrm{D}}{(2+n)\sqrt{\mathrm{D}}} i_{\mathrm{LV}}$ ***Boost gain***: $=\frac{2+n}{(1-\mathrm{D})}$ ***Efficiency:*** 96.38%	IPB027N10N5 V_{ds}=100V, R_{ds}=2.7m Ω I_d=120A *n=4.5* f_{sw}=50kHz V_{in}=30V V_o=380V	High

[25]	$\approx \frac{i_{HV}(n+1)}{D} + \frac{v_{LV} DT_s}{2L_m}$ ***Current Waveform***: 	$\approx \frac{i_{HV}(n+1)}{(1\text{-}D)} + \frac{v_{LV} DT_s}{2L_m}$ ***Current Waveform***: 	$\approx \frac{nT_s(1\text{-}D)\sqrt{1\text{-}D}}{L_m\sqrt{3}} v_{LV}$ ***Capacitor***:2 ***Switches***:4, ***Efficiency***: 90% ***Buck gain***: $= \frac{D}{(1+n)}$	$\frac{nT_s D\sqrt{D}}{L_m\sqrt{3}} v_{LV}$ ***Boost gain***: $= \frac{1+n}{(1-D)}$ ***Efficiency:*** 88%	IPA075N15N3 V_{ds}=150V, R_{ds}=0.0075 Ω I_d=172A. *n=4* f_{sw}=50kHz V_{in}=40V V_o=400V	High
[16]	$\frac{2P}{V_{LV}} + \frac{V_{HV}}{nR}$ ***Current Waveform***: 	$\frac{P}{V_{LV}} + \frac{(1\text{-}D)V_{LV}}{2f_{sw}}\left(\frac{1}{L_1} + \frac{1}{L_m}\right) + i_{pri\_max}$ ***Current Waveform***: 	$\simeq \frac{1+n-D}{(1+n)\sqrt{1-D}} i_{LV}$ ***Capacitor***:2 ***Switches***:4, ***Efficiency***: 96.4% ***Buck gain***: $= \frac{D}{(1+n)}$	$\cong \frac{1+n}{1-D} i_{Lm}\sqrt{D}$ ***Boost gain***: $= \frac{1+n}{(1-D)}$ ***Efficiency:*** 95%	IRFB4332 V_{ds}=250V, R_{ds}=0.033 Ω I_d=60A. *n=3.4* f_{sw}=50kHz V_{in}=48V V_o=380V	High

4.4.6. Design equation and soft switching condition

Coupled inductor number of turn (n) is derived from voltage gain equation of boost mode of CIBDC which is

$$n \geq \frac{v_{HV}(1\text{-}D)\text{-}2v_{LV}}{2v_{LV}} \tag{4.55}$$

The magnetizing inductance is derived from the normalized time constant at boundary as mentioned in equation (4.56). Therefore, to ensure the CCM operation in proposed CIBDC $\frac{L_m}{R_L T_s} = \tau_{Lm} > \tau_{Lmb}$

$$L_m \geq \frac{R_L D(1\text{-}D)^2}{2f_{sw}(n+1)^2} \tag{4.56}$$

High voltage side capacitance (C_{HV}) is derived from change in capacitor charge based on change in capacitor ripple voltage (ΔV).

$$C_{HV} \geq \frac{i_{HV} D}{f_{sw} \Delta v_{HV}} \tag{4.57}$$

Low voltage side capacitance is designed from buck operation using capacitor charge and voltage ripple

$$C_{LV} \geq \frac{v_{HV}(1\text{-}D)}{16(n+1)L_m f_{sw}^2 \Delta v_{LV}} \tag{4.58}$$

Similarly, the values of the intermediate capacitor C_1, C_2, C_3 and C_4 are derived based on the ripple voltage and charge

$$C_1 \geq \frac{i_{LV} D}{n f_{sw} \Delta v_{C1}} \text{ and } C_2 \geq \frac{2 i_{LV} D}{n f_{sw} \Delta v_{C2}} \tag{4.59}$$

$$C_3 \geq \frac{i_{LV} D}{2(n+1) f_{sw} \Delta v_{C3}} \text{ and } C_4 \geq \frac{i_{LV} D}{(n+1) f_{sw} \Delta v_{C4}} \tag{4.60}$$

Soft switching condition of auxiliary switches i.e., S_2, S_3, S_4 and S_5 are dependent on leakage inductance and fall in the stored electrostatic energy due to switch parasitic capacitance. During switch transition the capacitor stored energy should be dissipated before gaining magnetizing energy due to leakage inductance to achieve ZVS condition

4.4.7. Small signal analysis using average state space model

Small signal analysis of proposed CIBDC is performed to derive the transfer function. There are five energy storing elements in form of a coupled inductor and four capacitors.

The voltage across intermediate capacitors C_1, C_2, C_3 are constant and depending on input or output voltages. Therefore, they are not considered [27] as state variable in the small signal analysis. The state variables are coupled inductor current and output capacitor voltage. Hence, the resultant transfer function model is reduced to second order model. In boost mode the state variables are coupled inductor current (i_L) and output capacitor voltage (V_{HV}). Similarly, in buck mode the state variables are coupled inductor current (i_L) and output capacitor voltage (V_{LV}).

4.4.7.1 Boost Mode:

In boost mode, S_1 is the main switch. At switch ON time (S_1=1) the circuit equations are,

$$L_1 \frac{di_L(t)}{dt} = V_{LV} \tag{4.61}$$

$$C_{HV} \frac{dV_{HV}(t)}{dt} = \frac{-V_{HV}}{R_L} \tag{4.62}$$

At switch OFF time (S_1=0) the circuit equations are,

$$(n+1) L_1 \frac{di_L(t)}{dt} = V_{LV} + V_{C2} + V_{C3} - V_{HV} = V_{LV}\left[\frac{2+2n\text{-}D\text{-}nD}{1\text{-}D}\right] - V_{HV}(t) \tag{4.63}$$

$$C_{HV} \frac{dV_{HV}(t)}{dt} = \frac{-V_{HV}(t)}{R_L} + \frac{i_L(t)}{n} \tag{4.64}$$

For ON time the state space matrix equations are,

$$\frac{d}{dt}[X] = [A_1]X + [B_1]u \tag{4.65}$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ V_{HV} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{C_{HV}R_L} \end{bmatrix}\begin{bmatrix} i_L \\ V_{HV} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} V_{LV} \tag{4.66}$$

For OFF time the state space matrix equations are,

$$\frac{d}{dt}[X] = [A_2]X + [B_2]u \tag{4.67}$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ V_{HV} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1(n+1)} \\ \frac{1}{nC_{HV}} & \frac{-1}{C_{HV}R_L} \end{bmatrix}\begin{bmatrix} i_L \\ V_{HV} \end{bmatrix} + \begin{bmatrix} \frac{2}{L_1(1\text{-}D)} - \frac{D}{L_1} \\ 0 \end{bmatrix} V_{LV} \tag{4.68}$$

State space averaging technique is applied and after linearizing the small signal model is developed for boost mode.

$$\frac{d}{dt}\left[\tilde{x}\right]=[a]\tilde{x}+[b]\tilde{u}+\left[[A_1-A_2]X+[B_1-B_2]u\right]\tilde{d} \tag{4.69}$$

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_L\\ \tilde{v}_{HV}\end{bmatrix}=\begin{bmatrix}0 & \frac{-1+D}{L_1(n+1)}\\ \frac{1-D}{nC_{HV}} & \frac{-1}{C_{HV}R_L}\end{bmatrix}\begin{bmatrix}\tilde{i}_L\\ \tilde{v}_{HV}\end{bmatrix}+\begin{bmatrix}\frac{2+D^2}{L_1}\\ 0\end{bmatrix}\tilde{v}_{LV}+\begin{bmatrix}\frac{V_{HV}}{L_1(n+1)}-\frac{1+D^2}{L_1(1-D)}V_{LV}\\ \frac{-I_L}{nC_{HV}}\end{bmatrix}\tilde{d} \tag{4.70}$$

Small change in input voltage is zero i.e., $V_{LV}=0$. Thus, from equation (4.70) the transfer function of output voltage to duty ratio is derived i.e.

$$\frac{\tilde{v}_{HV}(s)}{\tilde{d}(s)}=\frac{k(-\beta s+1)}{s^2+2\xi\omega_n s+\omega_n^2} \tag{4.71}$$

Where,

$$k=\frac{V_{HV}(1-D)-V_{LV}(n+1)(1+D^2)}{n(n+1)C_{HV}L_1},\quad \beta=\frac{L_1(n+1)I_L}{V_{HV}(1-D)-\left[(n+1)(1+D^2)V_{LV}\right]}$$

$$2\xi\omega_n=\frac{1}{R_L C_{HV}}\ \text{and}\ \ \omega_n=\frac{(1-D)^2}{nC_{HV}L_1(n+1)}$$

4.4.7.2 Buck Mode:

In buck mode S_6 is the main switch. At switch ON time (S_6=1) the circuit equations are

$$L_1\frac{di_L(t)}{dt}=\frac{V_{HV}}{2+2n}-V_{LV}(t) \tag{4.72}$$

$$C_{LV}\frac{dV_{LV}(t)}{dt}=\frac{-V_{LV}}{R_L}+i_L(t) \tag{4.73}$$

At switch OFF time (S_1=0) the circuit equations are,

$$L_1\frac{di_L(t)}{dt}=-V_{LV}(t) \tag{4.74}$$

$$C_{LV}\frac{dV_{LV}(t)}{dt}=i_L(t)-\frac{V_{LV}(t)}{R_L} \tag{4.75}$$

For ‘ON’ time the state space matrix equations are,

$$\frac{d}{dt}\begin{bmatrix}i_L\\ V_{LV}\end{bmatrix}=\begin{bmatrix}0 & \frac{-1}{L_1}\\ \frac{1}{C_{LV}} & \frac{-1}{C_{LV}R_L}\end{bmatrix}\begin{bmatrix}i_L\\ V_{LV}\end{bmatrix}+\begin{bmatrix}\frac{1}{2+2n}\\ 0\end{bmatrix}V_{HV} \tag{4.76}$$

For ‘OFF’ time the state space matrix equations are,

$$\frac{d}{dt}\begin{bmatrix} i_L \\ V_{LV} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_{LV}} & \frac{-1}{C_{LV}R_L} \end{bmatrix}\begin{bmatrix} i_L \\ V_{HV} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{HV} \tag{4.77}$$

State space averaging technique is applied and after linearizing the small signal model is developed for boost mode

$$\frac{d}{dt}\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{LV} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} \\ \frac{1}{C_{LV}} & \frac{-1}{C_{LV}R_L} \end{bmatrix}\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{LV} \end{bmatrix} + \begin{bmatrix} \frac{V_{HV}}{(2n+2)} \\ 0 \end{bmatrix}\tilde{d} \tag{4.78}$$

Thus, from equation (4.78) the transfer function of output voltage to duty ratio is derived i.e.

$$\frac{\tilde{v}_{LV}(s)}{\tilde{d}(s)} = \frac{k_1}{s^2+2\xi\omega_n s+\omega_n^2} \tag{4.79}$$

Where, $k_1 = \frac{V_{HV}}{(2n+2)C_{LV}L_1}$, $2\xi\omega_n = \frac{1}{R_L C_{LV}}$ and $\omega_n = \frac{1}{C_{LV}L_1}$

4.4.8. Controller Design

The controller C(s) is designed based on desired closed loop performance by specifying the closed loop natural undamped frequency (ω_{cl}) and damping ratio (ζ_{cl}). The controller is in PID format [27] which can be represented by

$$C(s) = \frac{s^2+2\xi\omega_n s+\omega_n^2}{k_2 s\,(\alpha_2 s+\alpha_1)} \tag{4.80}$$

Where, $\alpha_2 = \frac{1}{\omega_{cl}^2}$ and $\alpha_1 = \frac{2\xi}{\omega_{cl}}$. Using the controller, bode diagram of closed loop system for both modes are shown in Fig. 4.11 which shows a good phase margin of 63° and 62.9° for boost and buck mode respectively.

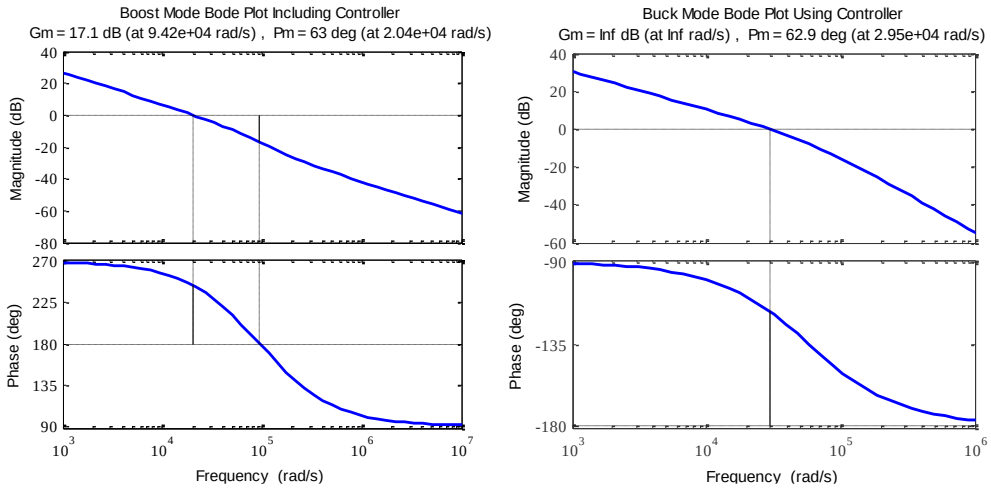


Fig. 4.11. Frequency response of the proposed CIBDC using compensator (a) boost mode (b) buck mode.

Mode transfer of proposed CIBDC from buck to boost mode or vice versa can be done easily using the switching function of main switches i.e., $S_1 = \mathrm{M}v$ and $S_6 = \bar{\mathrm{M}}\,v$

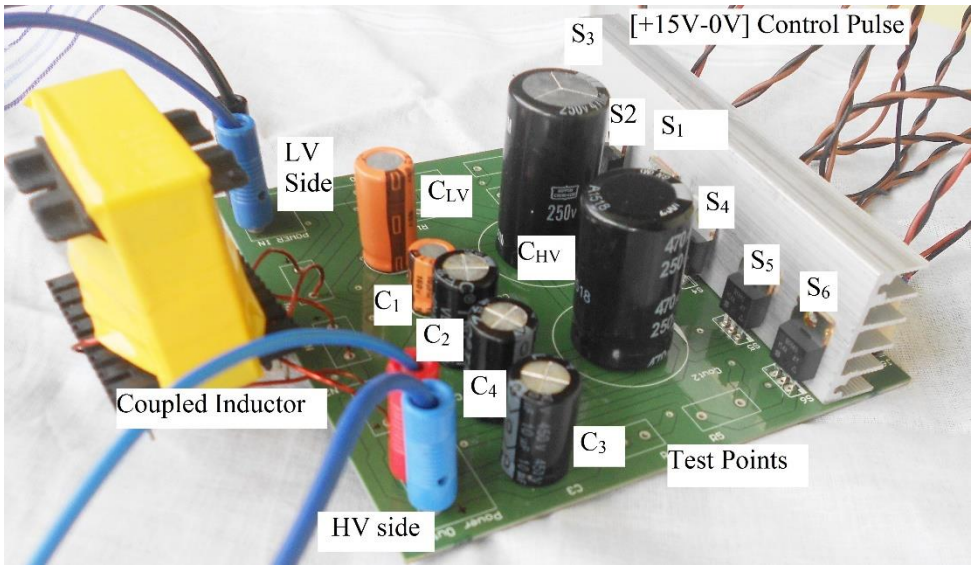
Where, v is the switching function and M is for mode selection

$$v = \begin{cases} 1 & 0<t<DT_s \\ 0 & DT_s<t<T_s \end{cases} \qquad \mathrm{M} = \begin{cases} 1 & \text{Boost} \\ 0 & \text{Buck} \end{cases} \tag{4.81}$$

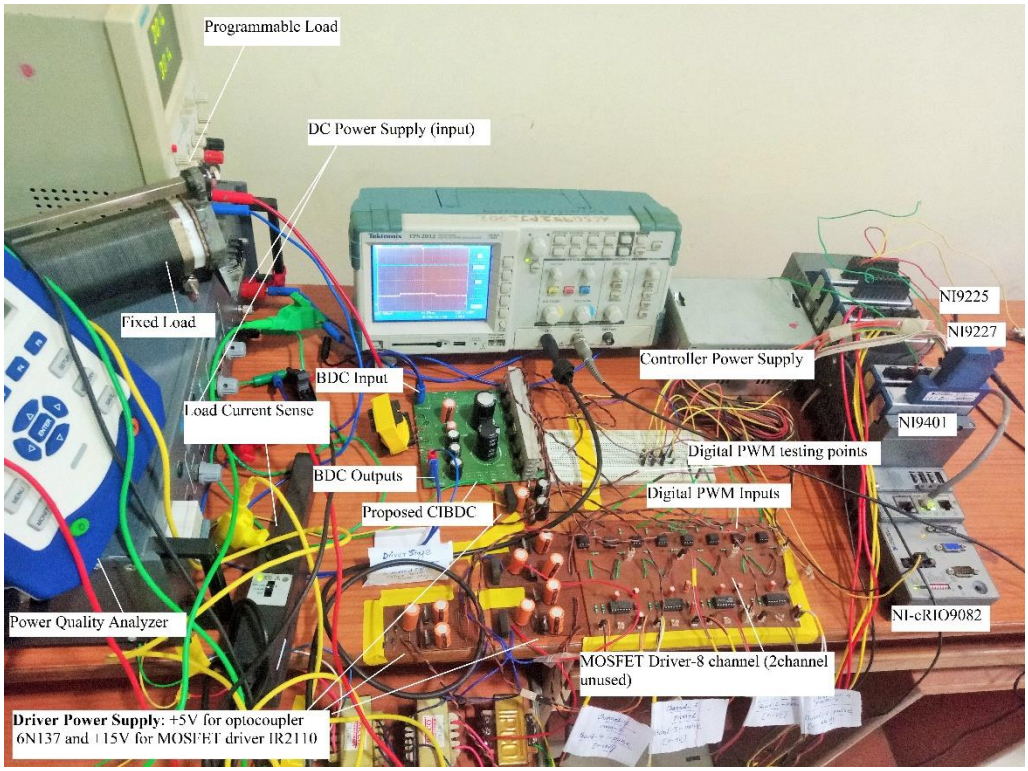
Voltage mode control is implemented in NI-cRIO 9082 using Lab-VIEW programming. NI-9225 is the voltage sensor module is used to sense the output voltage of the converter directly. After the control operation the digital PWM pulses for S_1 to S_6 is generated through NI-9401 digital input/output module. The total control function is developed in scan interface of NI-cRIO9082. The PWM pulses are sent to optocoupler stage (6N137) for isolation from control to the power stage. IR2110 driver is used to drive the six MOSFET switches. The total hardware set-up and controller for testing the proposed CIBDC are shown in Fig. 4.12 (b) and Fig. 4.12(c) respectively.

4.4.9. Results and Discussion

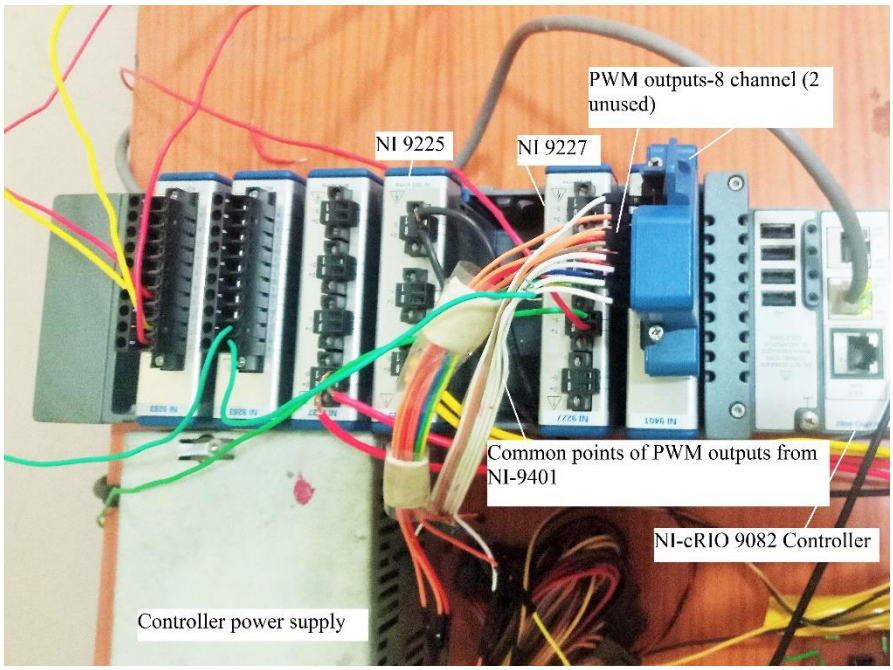
The performance of proposed CIBDC circuit in buck and boost mode is tested on a 250 W prototype converter as shown in Fig. 4.12 (a). The low voltage input is 48V where 384V is the output voltage designed at 50 kHz switching frequency. The optimum duty ratio of 0.5 is selected for testing prototype CIBDC. Unity turns ratio (*n=1*) is selected for coupled inductor which is derived from equation (4.55).



(a)



(b)



(c)

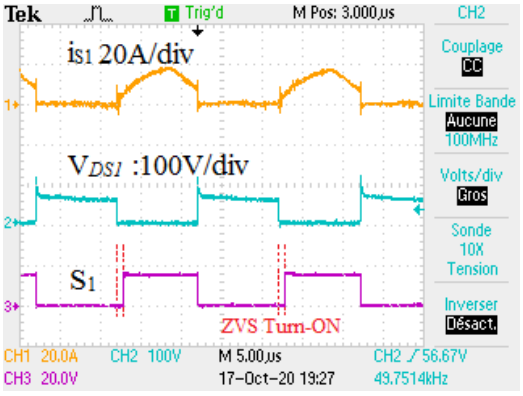
Fig.4.12. Proposed Prototype of CIBDC @ 250W (a) Power circuit of CIBDC (b) controller circuit including the driver stage (c) NI-cRIO 9082 controller with NI9225 (voltage sense module) and NI9401 (digital PWM module)

The designed parameters for proposed BDC are mentioned in Table-4.3. The performance of the proposed BDC is tested and demonstrated which shows a good match with theoretical results.

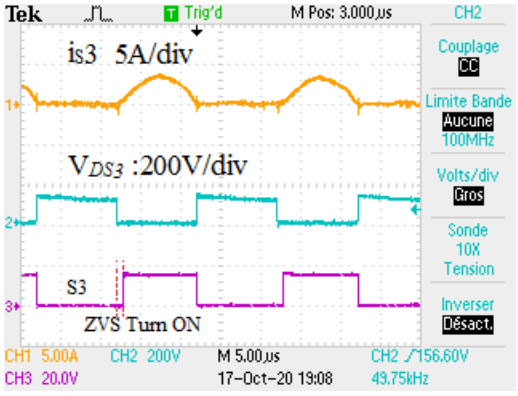
TABLE-4.3
SIMULATION AND HARDWARE PARAMETERS

CIBDC Specification		
Input Voltage = 48 V	Power Output = 250 W	Output Voltage = 384 V
	Switching Frequency=50 kHz	
Design Parameters	**Value**	**Part Number**
Coupled Inductor	L_m = 45 µH, Turns Ratio 25:25 (*n = 1*), $L_{leakage}$ = 7.15 µH	Ferrite Core PQ 32/30
Switch (S_1, S_2, S_3, S_4)	FQP34N20 (V_{ds} = 200 V, R_{ds} = 0.075 Ω, I_d=31 A.) @ 250W	FQP34N20
Switch (S_6)	FQP17N40 (V_{ds} = 400 V, R_{ds} = 0.27 Ω, I_d=16 A.) @ 250W	FQP17N40
Capacitor C_1, C_2, C_3	Simulated:12 µF hardware: 10µF	
Capacitor C_4	Simulated:15 µF hardware: 10µF	
Capacitor C_{LV}	100 µF	
Capacitor C_{HV}	470 µF	

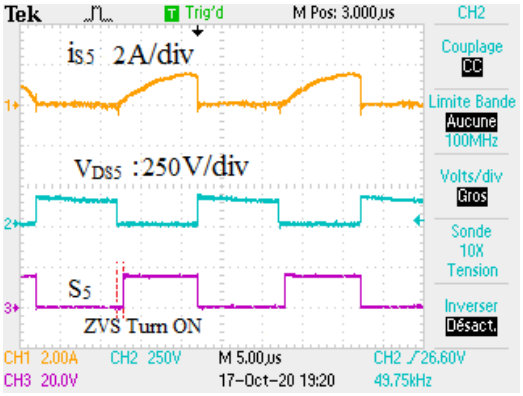
The recorded waveforms of boost mode of operation are mentioned in Fig. 4.13. ZVS turn on is achieved in all the active MOSFET switches as shown in Fig. 4.13 (a)-(f). In S_4, S_6 switches ZVS turn ON and turn OFF is achieved where in S_2 ZVS turn ON and ZCS turn OFF is recorded as shown in Fig. 4.13 (e), Fig. 4.13 (f) and Fig. 4.13 (d) respectively



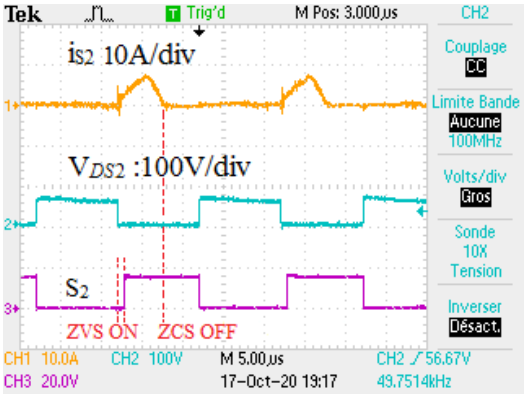
(a).



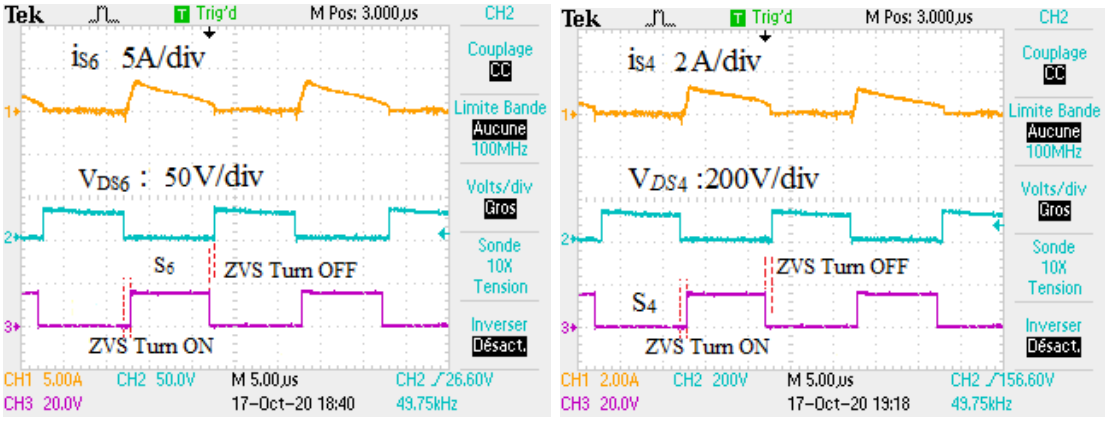
(b)



(c)



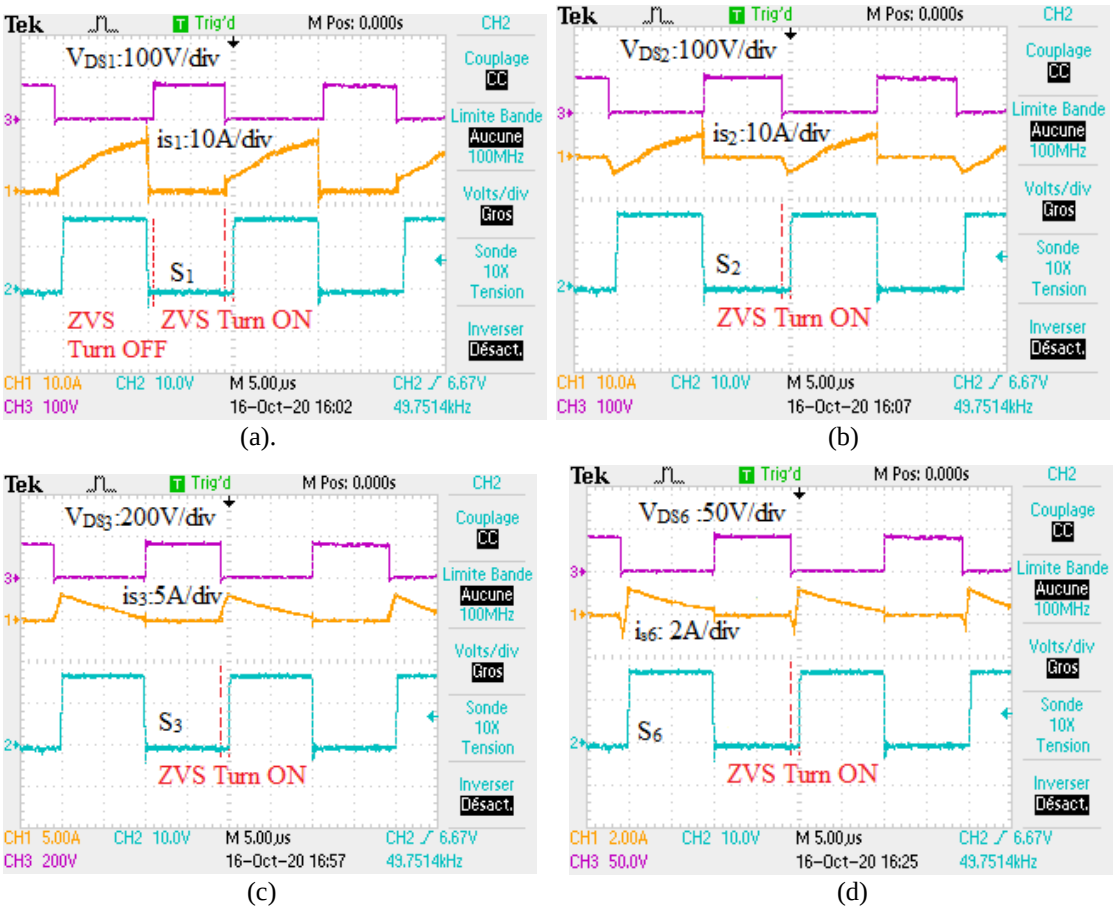
(d)



(e). (f)

Fig. 4. 13. (a)- (f) Experimental results of switch voltage and current in boost mode.

Similarly, the performance of buck mode is reported in Fig. 4.14. All switches are inherently soft switched like in boost mode.

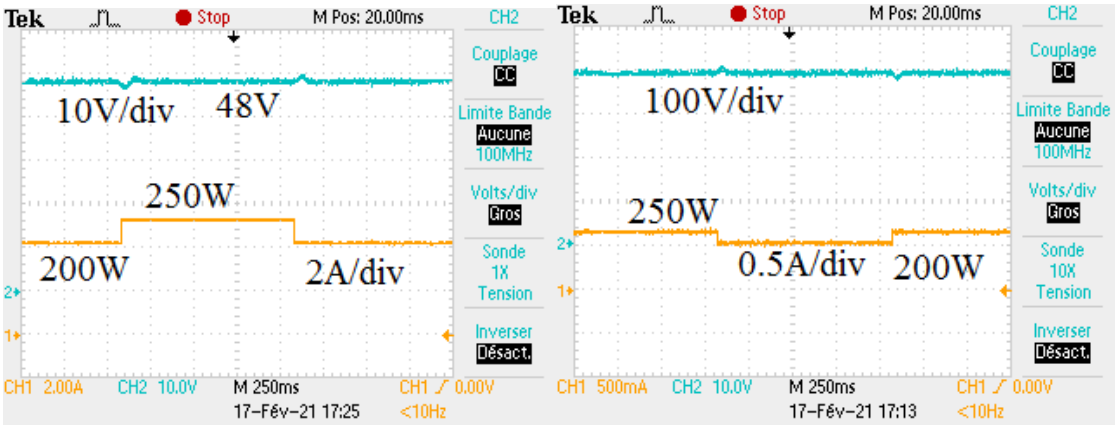


(a). (b)

(c) (d)

Fig. 4.14. (a)- (d) Experimental results of switch voltage and current in buck mode.

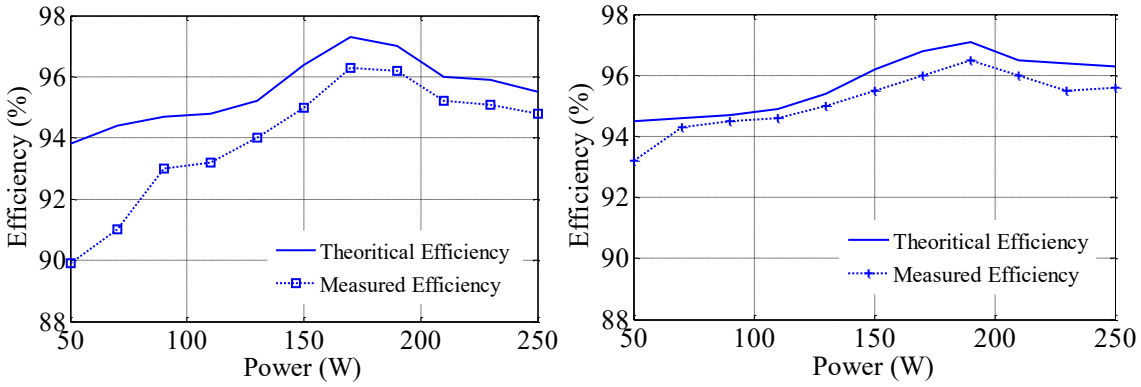
Dynamic performance of CIBDC is tested during step load change both in buck mode and boost mode as shown in Fig. 4.15 (a) and Fig. 4.15(b) which shows stable converter operation.



(a). (b)

Fig. 4.15. Voltage response for a load change from (a) 200W-250W-200W in buck mode, (b) 250W-200W-250W in boost mode.

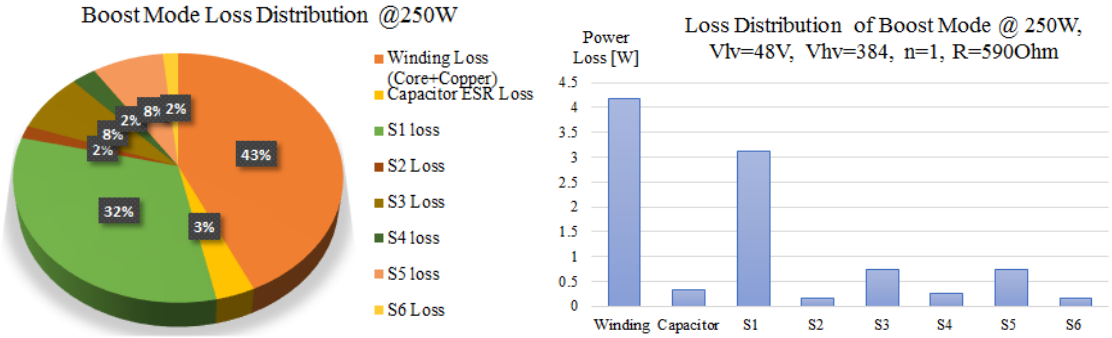
The theoretical and experimental efficiency of proposed BDC in both buck and boost mode is shown in Fig. 4.16. The efficiency calculation is mentioned in Appendix-B. The difference of the theoretical and measured efficiency is due to the fact that RMS and average current for switches, capacitors and inductor coil are calculated using ideal waveforms. However, the efficiency pattern is same throughout the entire operating range. The maximum measured efficiencies for buck and boost mode of operation are 96.12% and 96.63% respectively. The loss distribution of CIBDC at 250W is shown in Fig. 4.17 (a) and Fig. 4.17 (b). The proposed converter is designed with taking less coupled inductor winding turns ($n=1$) taking topological advantage to meet same voltage gain whereas in existing literatures the number of turns [25], [27] is generally greater than four ($n\geq4$). The proposed CIBDC has lesser switch current stress by 15-20% and RMS values compared to the topologies like [25], [27] and [16].



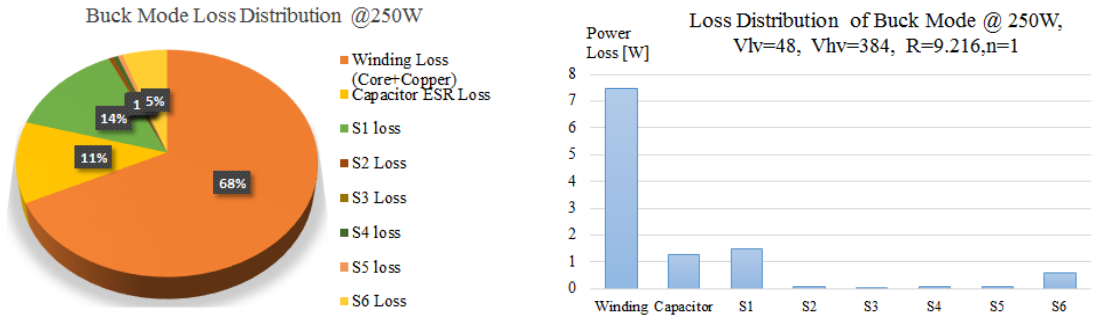
(a) (b)

Fig. 4.16. Efficiency of proposed CIBDC in (a) buck mode (b) boost mode.

The voltage stress performance of proposed converter is almost similar to existing topologies. The boosting voltage gain factor of CIBDC for 0.4 duty ratio at *n=1* is 6.66 where as in [25], [16] the same factor is 3.33 and in [27], [23-24] the value is 5. At the same condition the conversion factor is 3.21 in [31].



(a)



(b)

Fig. 4.17. Loss distribution of CIBDC @250W (a) boost mode (b) buck mode

4.5. Summary

In this chapter a novel coupled inductor based bidirectional DC-DC converter is proposed which is capable of delivering high voltage conversion ratio in both buck and boost mode of operation. In this CIBDC topology higher conversion factor i.e. ≥10 in boost and ≤1/10 in buck mode are obtained with unity turns ratio (*n=1*). Current and voltage stress is less in main MOSFET switches in both the operating modes which enables to select low voltage, low ON state resistance of MOSFET. This helps to reduce conduction loss. Again, all the active switches are soft switched i.e. ZVS. Therefore, switching loss is negligible which further improves the conversion efficiency. The proposed converter utilized two parallel inductor current paths to share input currents during boost as well as in buck mode which reduces current rating of individual coils and helps in reducing input current ripple. Due to topological advantage, the leakage inductance energy is directly

transferred to load. The detailed analysis of topological derivation, current and voltage stress along with efficiency calculation in steady state is discussed in details. The maximum measured efficiency is 96.12% in buck mode at 170W and 96.63% in boost mode at 190W.

4.6. Publication and References

Publication:

S. B. Santra, D. Chatterjee, and T. J (Peter). Liang, “High Gain and High Efficiency Bidirectional DC-DC Converter with Current Sharing Characteristics Using Coupled Inductor”, **IEEE Transactions on Power Electronics**, Vol. 36, no. 11, pp. 12819-12833, Nov. 2021.

References:

[1] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron*., vol. 31, no. 5, pp. 3528-3549, May 2016.

[2] H. J. Chiu and L. W. Lin, "A bidirectional dc-dc converter for fuel cell electric vehicle driving system," *IEEE Trans. Power Electron*., vol. 21, DOI 10.1109/TPEL.2006.876863, no. 4, pp. 950-958, July 2006.

[3] D. M. Sable, F. C. Lee, and B. H. Cho, “A zero-voltage-switching bidirectional battery charger/discharger for the NASA EOS satellite,” in *Proc 7th IEEE Appl. Power Electron. Conf. Expo*., Boston, MA, Feb. 1992, pp. 614–621.

[4] A. Nasiri, Z. Nie, S. B. Bekiarov, and A. Emadi, “An on-line UPS system with power factor correction and electric isolation using BIFRED converter,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 722–730, Feb.2008.

[5] P. Xuewei and A. K. Rathore, "Novel Bidirectional Snubberless Naturally Commutated Soft-Switching Current-Fed Full-Bridge Isolated DC/DC Converter for Fuel Cell Vehicles," *IEEE Trans.Ind. Electron*., vol. 61, no. 5, pp. 2307-2315, May 2014.

[6] D. Aggeler, J. Biela, S. Inoue, H. Akagi, J.W. Kolar, “Bi-directional isolated dc-dc converter for next-generation power distribution-comparison of converters using Si and SiC devices,” in *Proceedings of Power Conversion Conference*, pp. 510-517, 2007.

[7] T. Mishima, H. Mizutani, and M. Nakaoka, "A sensitivity-improved PFM LLC resonant full-bridge DC–DC converter with LC antiresonant circuitry," *IEEE Trans. Power Electron*., vol. 32, no. 1, pp. 310-324, Jan. 2017.

[8] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, “Isolated bidirectional full-bridge dc-dc converter with a flyback snubber,” *IEEE Trans. Power Electron*., vol. 25, no. 7, pp. 1915-1922, Jul. 2010.

[9] J.-B. Lee, K.-B. Park, J.-K. Kim, H.-S. Youn, and G.-W. Moon, "A new center-tapped half-bridge zeta converter with small transformer dc-offset current and low voltage stress," *IEEE Trans. Power Electron*., vol. 30, no. 12, pp. 6593-6603, Dec. 2015.

[10] T.-F. Wu, J.-G. Yang, C.-L. Kuo, and Y.-C. Wu, "Soft-switching bidirectional isolated full-bridge converter with active and passive snubbers," *IEEE Trans. Ind. Electron*., vol. 61, no. 3, pp. 1368-1376, March 2014.

[11] H. Ardi, A. Ajami, F. Kardan, and S. N. Avilagh, "Analysis and implementation of a nonisolated bidirectional DC–DC converter with high voltage gain," *IEEE Trans. Ind. Electron*., vol. 63, no. 8, pp. 4878-4888, Aug. 2016.

[12] H. S. H. Chung, W. C. Chow, S. Y. R. Hui and S. T. S. Lee, "Development of a switched-capacitor DC-DC converter with bidirectional power flow," in *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 9, pp. 1383-1389, Sept. 2000, doi: 10.1109/81.883334.

[13] Y. Zhang, W. Zhang, F. Gao, S. Gao and D. J. Rogers, "A Switched-Capacitor Interleaved Bidirectional Converter With Wide Voltage-Gain Range for Super Capacitors in EVs," in *IEEE Trans. on Power Electron*., vol. 35, no. 2, pp. 1536-1547, Feb. 2020, doi: 10.1109/TPEL.2019.2921585.

[14] Y. Zhang, Y. Gao, L. Zhou and M. Sumner, "A Switched-Capacitor Bidirectional DC–DC Converter With Wide Voltage Gain Range for Electric Vehicles With Hybrid Energy Sources," in *IEEE Trans. on Power Electron*., vol. 33, no. 11, pp. 9459-9469, Nov. 2018, doi: 10.1109/TPEL.2017.2788436.

[15] Y. Zhang, Q. Liu, Y. Gao, J. Li and M. Sumner, "Hybrid Switched-Capacitor/Switched-Quasi-Z-Source Bidirectional DC–DC Converter With a Wide Voltage Gain Range for Hybrid Energy Sources EVs," in *IEEE Trans. on Ind. Electron*., vol. 66, no. 4, pp. 2680-2690, April 2019.doi: 10.1109/TIE.2018.2850020.

[16] J. Yao, A. Abramovitz and K. Ma Smedley, "Steep-Gain Bidirectional Converter With a Regenerative Snubber," in *IEEE Trans. on Power Electron*., vol. 30, no. 12, pp. 6845-6856, Dec. 2015, doi: 10.1109/TPEL.2015.2395455.

[17] S. B. Santra, D. Chatterjee, Y. P. Siwakoti and F. Blaabjerg, "Generalized Switch Current Stress Reduction Technique for Coupled- Inductor based Single Switch High Step-Up Boost

Converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, May 2020 (early access).doi: 10.1109/JESTPE.2020.2998487.

[18] M. R. Mohammadi and H. Farzanehfard, "Family of Soft-Switching Bidirectional Converters With Extended ZVS Range," in *IEEE Trans. on Ind. Electron*., vol. 64, no. 9, pp. 7000-7008, Sept. 2017, doi: 10.1109/TIE.2017.2686308.

[19] P. Das, S. A. Mousavi and G. Moschopoulos, "Analysis and Design of a Nonisolated Bidirectional ZVS-PWM DC–DC Converter With Coupled Inductors," in *IEEE Trans. on Power Electron*., vol. 25, no. 10, pp. 2630-2641, Oct. 2010, doi: 10.1109/TPEL.2010.2049863.

[20] G. Chen et al., "A Family of Zero-Voltage-Switching Magnetic Coupling Nonisolated Bidirectional DC–DC Converters," in *IEEE Trans. on Ind. Electron*., vol. 64, no. 8, pp. 6223-6233, Aug. 2017, doi: 10.1109/TIE.2017.2682007.

[21] L. Yang and T. Liang, "Analysis and Implementation of a Novel Bidirectional DC–DC Converter," in *IEEE Trans. on Ind. Electron*., vol. 59, no. 1, pp. 422-434, Jan. 2012.doi: 10.1109/TIE.2011.2134060.

[22] Y. P. Hsieh, J. F. Chen, L. S. Yang, C. Y. Wu and W. S. Liu, "High conversion-ratio bidirectional dc–dc converter with coupled inductor," *IEEE Trans. on Ind. Electron*., vol. 61, DOI 10.1109/TIE.2013.2244541, no.1, pp. 210-222, Jan. 2014.

[23] R. -. Duan and J. -. Lee, "High-efficiency bidirectional DC-DC converter with coupled inductor," in *IET Power Electron*., vol. 5, no. 1, pp. 115-123, Jan. 2012, doi: 10.1049/iet-pel.2010.0401.

[24] R. -. Wai, R. -. Duan and K. -. Jheng, "High-efficiency bidirectional dc-dc converter with high-voltage gain," in *IET Power Electron*., vol. 5, no. 2, pp. 173-184, Feb. 2012, doi: 10.1049/iet-pel.2011.0194.

[25] S. M. P., M. Das and V. Agarwal, "Design and Development of a Novel High Voltage Gain, High-Efficiency Bidirectional DC–DC Converter for Storage Interface," in *IEEE Trans. on Ind. Electron*., vol. 66, no. 6, pp. 4490-4501, June 2019, doi: 10.1109/TIE.2018.2860539.

[26] Y. Zhang, H. Liu, J. Li and M. Sumner, "A Low-Current Ripple and Wide Voltage-Gain Range Bidirectional DC–DC Converter With Coupled Inductor," in *IEEE Trans. on Power Electron*., vol. 35, no. 2, pp. 1525-1535, Feb. 2020, doi: 10.1109/TPEL.2019.2921570.

[27] W. Hassan, J. L. Soon, D. D. Lu and W. Xiao, "A High Conversion Ratio and High-Efficiency Bidirectional DC-DC Converter with Reduced Voltage Stress," in *IEEE Trans. on Power Electron*., doi: 10.1109/TPEL.2020.2987083. 2020 early access.

[28] M. Aamir, S. Mekhilef and H. Kim, "High-Gain Zero-Voltage Switching Bidirectional Converter With a Reduced Number of Switches," in *IEEE Trans. on Circuits and Systems II: Express Brief*s, vol. 62, no. 8, pp. 816-820, Aug. 2015, doi: 10.1109/TCSII.2015.2433351.

[29] H. Moradisizkoohi, N. Elsayad and O. A. Mohammed, "Experimental Demonstration of a Modular, Quasi-Resonant Bidirectional DC–DC Converter Using GaN Switches for Electric Vehicles," in *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7787-7803, Nov.-Dec. 2019, doi: 10.1109/TIA.2019.2914648.

[30] H. Liu, L. Wang, Y. Ji and F. Li, "A Novel Reversal Coupled Inductor High-Conversion-Ratio Bidirectional DC–DC Converter," in *IEEE Trans. on Power Electron*., vol. 33, no. 6, pp. 4968-4979, June 2018, doi: 10.1109/TPEL.2017.2725358.

[31] H. Bahrami, S. Farhangi, H. Iman-Eini and E. Adib, "A New Interleaved Coupled-Inductor Nonisolated Soft-Switching Bidirectional DC–DC Converter With High Voltage Gain Ratio," in *IEEE Trans. on Ind. Electron*., vol. 65, no. 7, pp. 5529-5538, July 2018, doi: 10.1109/TIE.2017.2782221.

[32] H. Moradisizkoohi, N. Elsayad and O. Mohammed, "A Voltage-Quadrupler Interleaved Bidirectional DC-DC Converter With Intrinsic Equal Current Sharing Characteristic For Electric Vehicles," in *IEEE Trans. on Ind. Electron*., doi: 10.1109/TIE.2020.2998757.2020 early access.

[33] Y. Zhang, Y. Gao, J. Li and M. Sumner, "Interleaved Switched-Capacitor Bidirectional DC-DC Converter With Wide Voltage-Gain Range for Energy Storage Systems," in *IEEE Trans. on Power Electron*., vol. 33, no. 5, pp. 3852-3869, May 2018, doi: 10.1109/TPEL.2017.2719402.

[34] H. Wu, K. Sun, L. Chen, L. Zhu, Y. Xing, "High Step-Up/Step-Down Soft-Switching Bidirectional DC-DC Converter with Coupled-Inductor and Voltage Matching Control for Energy Storage Systems", *IEEE Trans. on ind. Electron*., vol. 63, no. 5, pp. 2892-2903, May 2016.

[35] T. Liang, H. Liang, S. Chen, J. Chen and L. Yang, "Analysis, Design and Implementation of a Bidirectional Double-Boost DC-DC Converter", in *IEEE Transactions on Industry Application*, vol. 50, no. 6, pp. 3955-3962, Nov.-Dec. 2014.

[36] R.W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 3rd edition. Springer, USA, Aug. 2020.

Chapter-5

GaN-FET Driver and Performance Improvement of BDC using GaN-FET

In previous chapter high gain, high efficiency BDC is designed using coupled inductor which has superior voltage gain and less voltage stress, current stress. The efficiency and power density of the BDC can be further enhanced by using GaN-FET devices. In this chapter reliable gate driver for GaN-FET is proposed and the performance is tested in synchronous buck converter as well as in proposed BDC circuit. The GaN-FET switch in the proposed BDC enhances efficiency by 1-1.5%.

5. GaN-FET Driver and Performance Improvement of BDC using GaN-FET

5.1. Introduction

Coupled Inductor based high gain, high efficiency bidirectional DC-DC converter is proposed in the previous chapter where switch current and voltage stress are also less. The efficiency and power density of the converter can be enhanced further using wide bandgap semiconductor devices. The wide bandgap (3.00-3.2 eV) FET devices are having important electrical characteristics which enable designer to use it in high power application. There are two major wide bandgap FET devices (a) GaN-FET (b) SiC-FET. The GaN-FET is suitable for low power application upto 1kW and can provide better performance compared to HEXFET MOSFET. But for high power application IGBT and SiC-FET devices are better in terms of thermal, and switching behaviour. In this work the bidirectional converter is designed for less than 1kW rating for microgrid [1] and auxiliary power supply of EV. Thus based on the characteristics, GaN-FET is selected. In comparison with the Silicon (Si) semiconductor devices, the wide band gap devices like Gallium nitride devices have many properties like wider band gap, higher breakdown electric field, faster electron mobility and velocity, allowing the GaN-FET devices to have faster transition and lower switching loss [2-3]. Fig. 5.1 highlights some key material properties of gallium nitride (GaN) semiconductor devices as compared to traditional silicon devices.

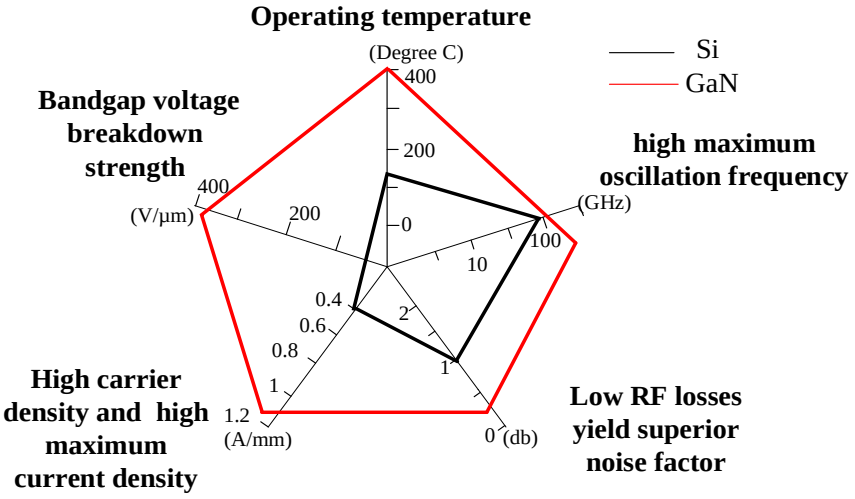


Fig. 5.1 Summary of silicon (Si) and gallium nitride (GaN) relevant material properties

The Advantages of GaN-FET devices compared to Si-MOSFET are listed in Table-5.1.

Table- 5.1
Comparison between Si-MOSFET and GaN-FET electrical parameter-typical values.

Parameters	**Si-MOSFET**	**GaN-FET**
Bandgap, Eg (eV)	1.12	3.44
Electric Breakdown field, Ec (MV/cm)	0.3	3.8
Electron mobility, μn (cm^2/V-s)	1500	1000-2000
Saturated electron drift velocity, vs(x 10^7 cm/s)	1.0	2.5
Dielectric Constant, Ɛr	11.8	9.5
Thermal conductivity, (W/cm-K)	1.5	1.3

From the table-5.1 it is clear that **electrical characteristics of GaN-FET devices are better over HEXFET MOSFET. Some important advantages are**

(a) Large thermal breakdown voltage as well as high reverse blocking voltage.

(b) Very low switching loss (Junction capacitance are 10 times lesser than MOSEFT)

(c) Very low ON-state resistance which enables low conduction loss.

(d) Good thermal conductivity

These important characteristics helps designer to achieve

(a) Higher efficiency from the converter of similar prototype while using MOSFET or IGBT.

(b) Less form factor increases the power density.

(c) Easy cooling requirement due to less switching loss and higher thermal conductivity.

(d) Light weight converter with fewer components.

5.2. GaN-FET Driver

PWM signals generated from microcontroller or FPGA board are required to control power switches in BDC converter. However, the microcontroller can able to generate control signal within 0-5V. This voltage is not sufficient to bias power FETS both MOSFET as well as GaN-FET for switching operation. Therefore proper biasing circuit arrangement should be made [4], [6] with the help form microcontroller PWM pulses to generate

required PWM signal for switching as well as isolation between control circuit and power circuit. This extra circuit between microcontroller and power circuit is known as driver circuit. The basic two operation required form a driver circuit is reliable switching operation and isolation between controls to power circuit. The basic block diagram of driver stage for MOSFET is shown in Fig. 5.2.

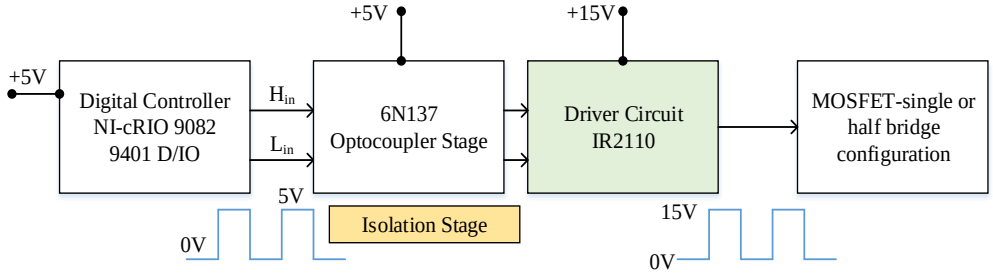


Fig. 5.2. Block diagram of IR2110 based MOSFET driver circuit using optocoupler.

Similarly, for GaN-FET separate driver circuit is required for reliable switching operation.

5.2.1. GaN-FET driver and biasing requirements

For MOSFET +15V-20V is +Vgs is enough to fully turn ON the device. However, for GaN-FET it is not the same. Thus, the circuit arrangement as shown in Fig. 5.2 is not suitable for GaN-FET [10]. The biasing requirement for switching operation of GaN-FET is mentioned in Table-5.2.

Table-5. 2

Typical Si-MOSFET and GaN-FET Parameters

Parameters	**Si-MOSFET**	**GaN-FET**
V_{GSTH}(min)	2V	0.7V
V_{GSTH}(typ)	3V	1.4V
V_{GS}(max)	20V	6-10V
V_{SD}	<1V	1.8V

The modified circuit configuration for GaN-FET is shown in Fig. 5.3.

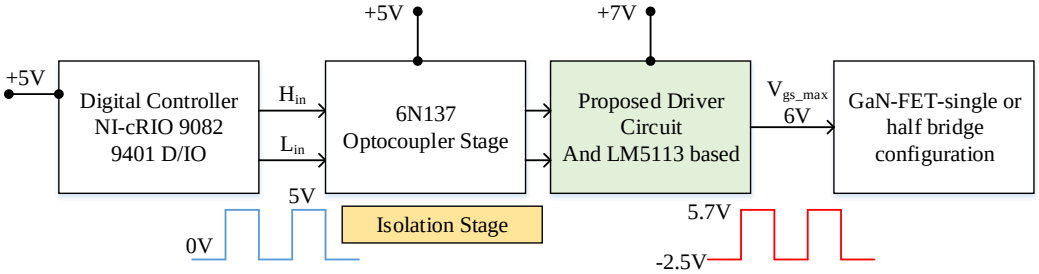


Fig. 5.3. Block diagram of GaN-FET driver

Texas Instruments (TI) make LM5113 can be used as driver for GaN-FET. This circuit is

derived from bootstrapping principle for switching high side and low side switches in half bridge configuration. This LM5113 based circuit can be modified which is discussed later in this chapter.

5.2.2. IR2110 based MOSFET driver

The bootstrap capacitor is used in gate driver circuit to supply bias to the top or high side switch (FET) in the half bridge configured power module. This configuration is used for driving synchronous buck and boost converter. Fig. 5.4 shows the charging and discharging path of the bootstrap capacitor while driving IR2110 based MOSFET.

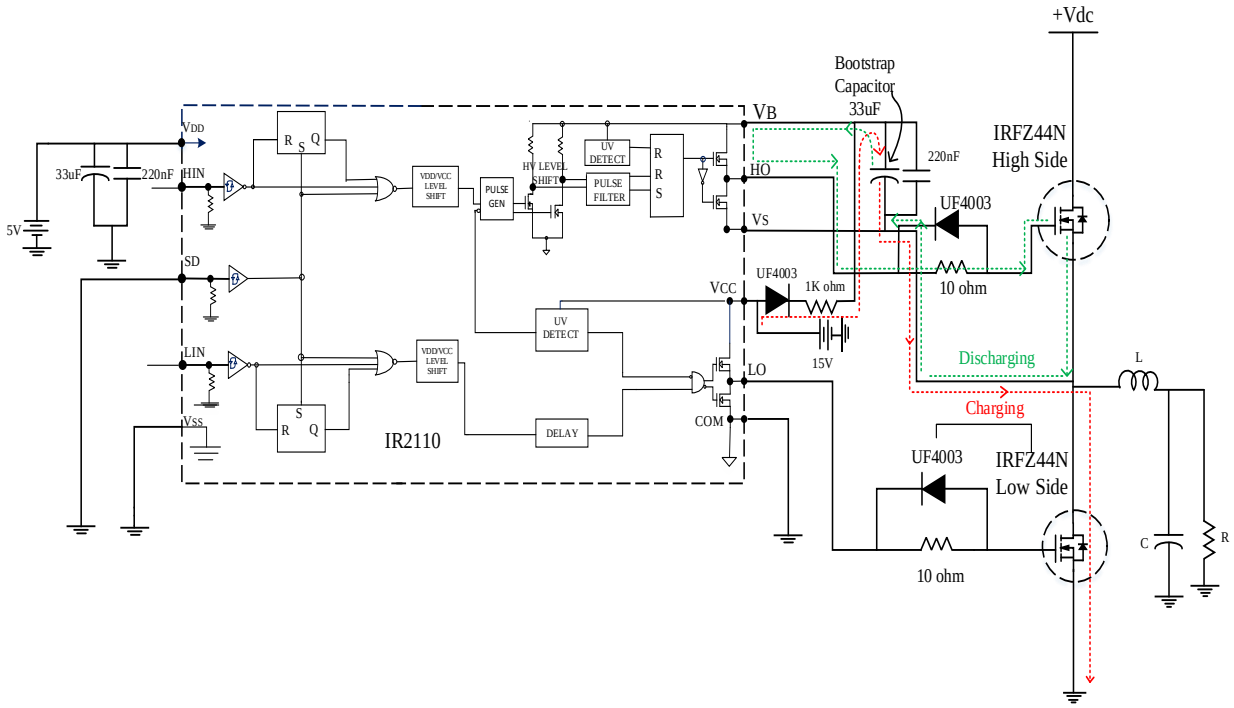


Fig. 5.4. IR2110 based MOSFET driver circuit diagram.

5.2.3. Issues with GaN-FET driver

Similar bootstrapping technique can also be applied for designing GaN-FET driver and developed by Texas Instruments LM5113 as shown in Fig. 5.5. The charging and discharging paths of bootstrap capacitor is also shown and the performance is similar to IR2110 based MOSFET driver. The major challenges of GaN-FETs are (a) lower threshold voltage (b) larger drain to source voltage during a dead time free-wheeling event [5], [7]. As the threshold voltage of GaN FET (V_{Th}) is 0.7V, so to fully turn ON a GaN FET, it needs a minimum gate voltage of 3-4V. Due to low $V_{Th,}$ the major concern is false triggering at high $\frac{dv}{dt}$ which is common during switch turn-OFF process. Therefore, $\frac{dv}{dt}$ immunity is a major concern for the GaN-FET devices especially in high load current and larger dead time. The maximum $\frac{dv}{dt}$ value [8] can be determined by

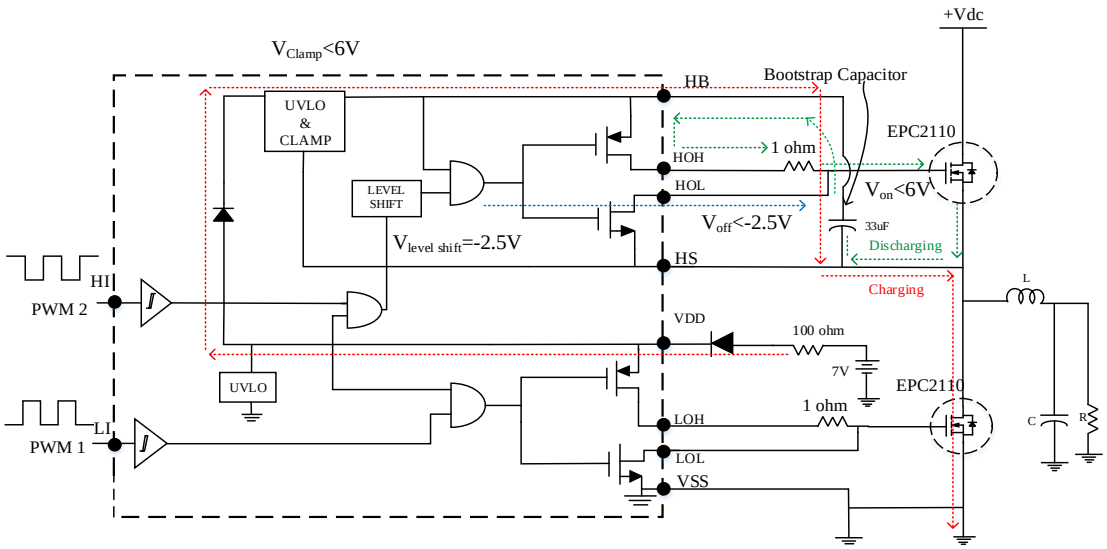


Fig. 5.5. LM5113 based GaN-FET driver circuit diagram.

$$\frac{dV_{max}}{dt} = \frac{V_{Th}}{Z_{Pull\_Down} \times C_{gd}} \tag{5.1}$$

By minimizing Z_{pull_down}, the $\frac{dv}{dt}$ immunity can be limited. This also limits the transient performance expected from the GaN-FET based DC-DC converter. There are two approaches found in the literature to address these issues, (a) using a negative biased gate driver [9] (b) using an inductor based driver circuit [11].

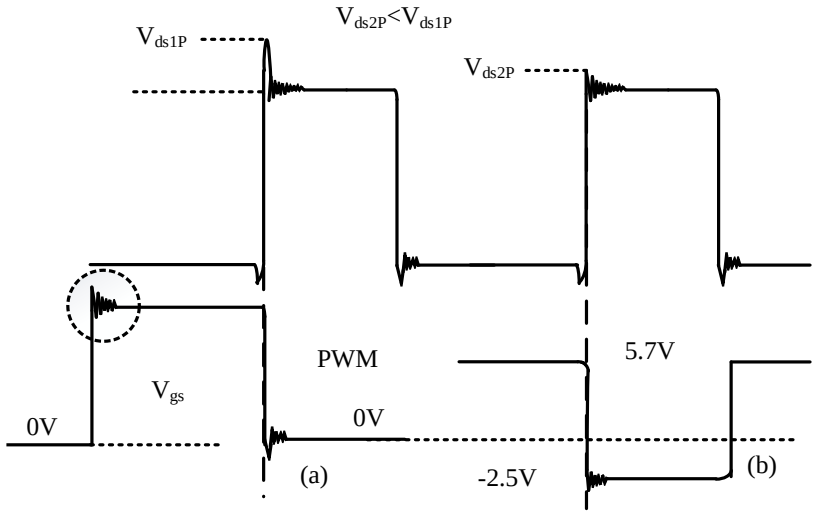


Fig. 5.6. (a) Zero bias turn OFF event of GaN-FET (b) Negative bias turn OFF event of GaN-FET.

By using a negative biased gate driver [11] during turn-OFF, the $\frac{dv}{dt}$ immunity can be achieved with low drain current and limited dead time as shown in Fig. 5.6. For a negative biased gate driver, negative voltage i.e. $-V_a$ is applied during switch turn-OFF time. At this time, $V_{SD} > V_{TH} + V_a$ where V_{SD} (@V_{gs}=-V_a)=V_{SD} (@ V_{gs}=0)+V_a. At turn-OFF operation, conduction loss is represented by

$$P_C = V_{SD} I_{SD} = \left\{ V_{SD} \left(@V_{gs} = 0 \right) + V_a \right\} I_{SD} \quad (5.2)$$

Negative bias is an effective technique to prevent false turn-ON, but the trade-off is higher gate conduction loss. With an inductive load, when a GaN-FET transistor is turned OFF, a circulating current flow via low side transistor from source to drain. The second approach is to use a small inductor in the bootstrap path with a schottky diode which ensures good $\frac{dv}{dt}$ immunity and a better transient response with increased load current. But, this technique increases the gate loss and creates V_{gs} spikes or ringing during turn-ON as shown in Fig. 5.7. This technique creates extra heat at the gate junction during GaN-FET turn-ON time as well as increases gate voltage ringing.

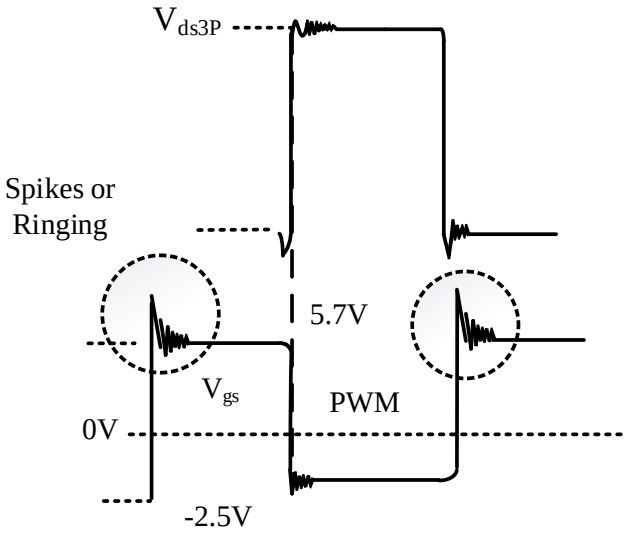
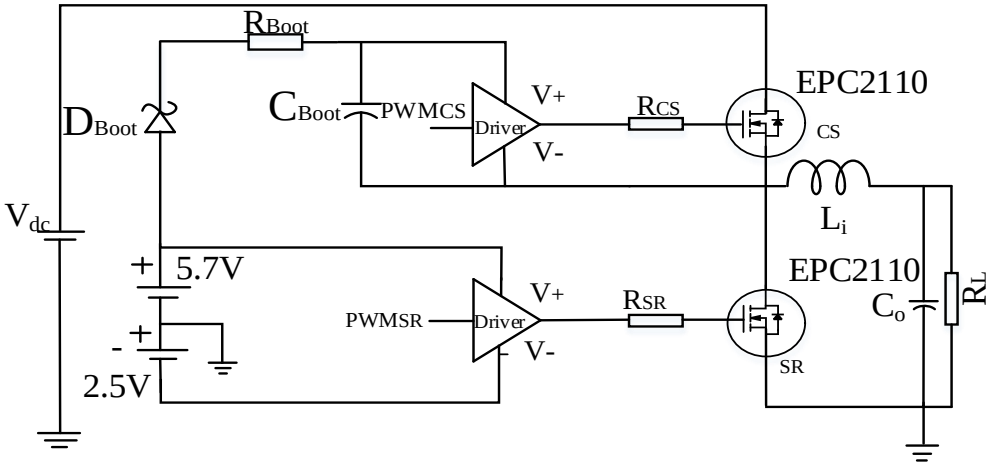


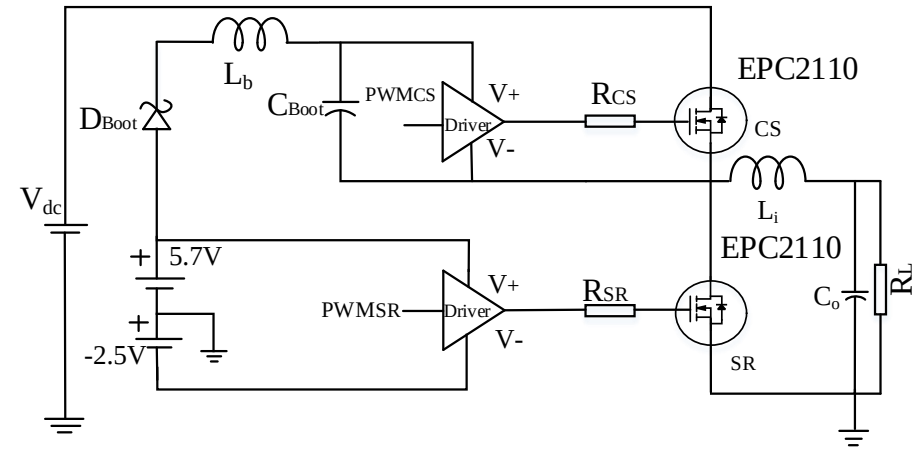
Fig. 5.7. Negative bias turn OFF operation of GaN-EFT

5.3. Proposed GaN-FET driver

The conventional bootstrap capacitor based i.e. LM5113, GaN-FET driver is shown in Fig. 5.8 (a). This is conventional bootstrapping technique which was used in LM5113 chip.



(a)



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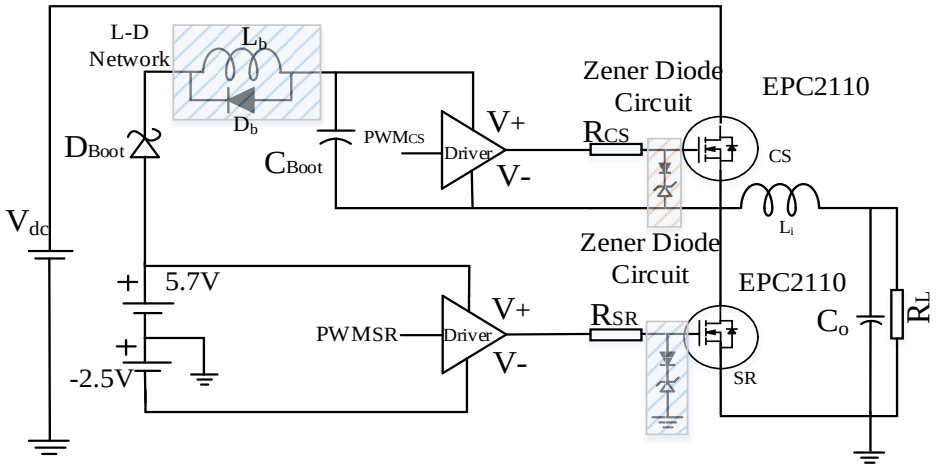


(c)

Fig.5.8. Synchronous buck converter (a) negative bias turn 'OFF' GaN-FET driver (b) inductor based negative biased turn 'OFF' GaN-FET driver (c) proposed GaN-FET driver.

As LM5113 based driver has major problem of false triggering especially with larger drain current and dead time. This false triggering of LM5113 based driver can be eliminated using inductor based negative bias turn OFF driver circuit which is shown in Fig. 5.8 (b). This circuit effectively eliminates the false triggering of GaN-FET. However, this circuit has large drain to source voltage ringing problem during switching events. This ringing problem as well as false triggering problem of GaN-FET driver can be eliminated by inductor diode (L-D) combination-based circuit as shown in Fig. 5.8 (c). Zener diode-based circuit is also there for preventing voltage rise above 5.7 volt during run off event to eliminate false triggering effectively. In the next section the driver component parameter selection is discussed.

5.3.1. Parameter selection and design of proposed driver

The driver design problem mainly involves in designing three major components i.e. (a) bootstrap capacitor (C_{boot}) (b) series resistance (R_{se}) (c) series inductor (L_b). C_{boot} can be

designed in two ways (i) from GaN-FET device characteristics or (ii) from circuit equation. The bootstrap capacitor is used in gate driver circuit to supply bias to the top or high side switch (FET) in half bridge configuration. This configuration is used for driving synchronous buck and boost converter. Fig. 5.5 shows the charging and discharging path for high side GaN driver.

But the design criteria of bootstrap capacitor for GaN-FET Driver is different from MOSFET as junction capacitance of these two devices are different. For FET devices, the minimum value of bootstrap capacitance is 10 times of FET gate to source junction capacitance (C_g) [5]. This capacitance can be derived from the FET gate junction charge (Q_g) which is mentioned in the datasheet. The gate voltage (V_g) is

$$V_g = V_{cc} - V_{diode} \text{ and } C_g = \frac{Q_g}{V_g} \tag{5.3}$$

Roughly the bootstrap capacitor (C_{boot}) value is $10C_g$. Again, from the switching characteristics C_{boot} can be derived. The total charge (Q_{boot}) of bootstrap capacitor is used during switching operation.

$$Q_{boot} = Q_g + Q_{switching} \tag{5.4}$$

From the FET datasheet Q_g is determined. $Q_{switching}$ can be determined using 'ON' time energy loss [12].

$$E_{on} = \frac{1}{6} V_{max} I_{min} t_{on} \tag{5.5}$$

This can be made equivalent to,

$$\Delta E = \frac{1}{2} C_{boot} V_g^2 - \frac{1}{2} C_g V_g^2 \tag{5.6}$$

From equation (5.5) and (5.6) the value of C_{boot} is derived which is

$$C_{boot} = \frac{V_{max} I_{min} t_{on}}{3V_g^2} + C_g = \frac{V_{max} I_{min} D_{max}}{3f_{switching} V_g^2} + C_g \tag{5.7}$$

The gate to source capacitance (C_g) value is less for GaN-FET devices compared to MOSFET. Therefore, rise time is less and suitable for high frequency operation. The design criteria for C_{boot} for GaN-FET driver depends on gate charge characteristics as shown in Fig. 5.9.

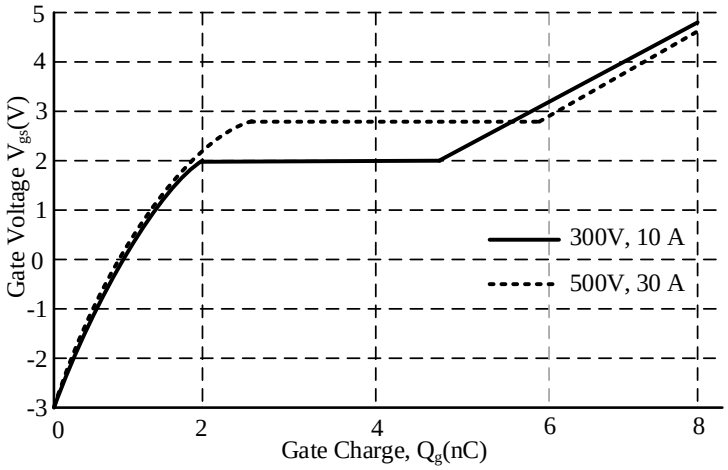


Fig. 5.9. Gate charge characteristics for a GaN-FET @ 25°C.

The gate charge (Q_g) for GaN-FET devices can be derived by using equation (5.8) and from the respective datasheet graph as shown in Fig. 5.9.

$$Q_g = \begin{cases} \int_{V_s}^{V_{gs}} C_g(V_{gs})dv, V_{gs} < V_{Miller} \\ Q_{gs,miller} + Q_{gd} + \int_{V_s}^{V_{gs}} \left(C_g(V_{gs}) + C_{rss}(0)\right)dv, V_{gs} \geq V_{Miller} \end{cases} \quad (5.8)$$

For zero biasing turn OFF event the gate voltage is zero (V_g=0) and for negative biasing turn OFF the gate voltage is negative i.e. V_g<0. The maximum negative voltage can be applied is limited to 10V. Thus, the gate capacitance (C_g) can be derived from equation (5.8) which is,

$$C_g = \frac{Q_g}{V_{cc} - V_{diode}} \quad (5.9)$$

The equivalent circuit during switch ON time is shown in Fig. 5.10 (a). The energy loss during this time in GaN-FET device is,

$$E_{on} = \left\{ \int_{V_s}^{V_{gs}} C_g(V_{gs})[V_{cc} - V_{diode}]dv \right. \quad (5.10)$$

Again, from the ON time energy loss as mentioned in equation (5.10) the bootstrap capacitor (C_{boot}) is derived which is

$$C_{boot} = \frac{2}{V_g^2}\left\{ \int_{V_s}^{V_{gs}} C_g(V_{gs})[V_{cc} - V_{diode}]dv + C_g V_g^2 \right\} \quad (5.11)$$

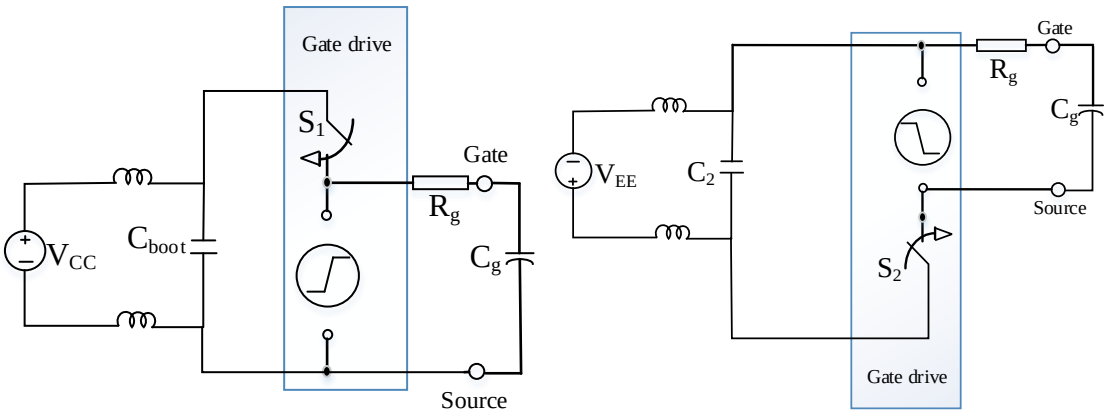


Fig. 5.10. Driver circuit for GaN-FET (a) Turn ON circuit (b) Turn OFF Circuit.

To ensure reliable switching the capacitor (C_{boot}) value should be higher than the value derived from equation (5.11). V_{CC} is ON time and V_{EE} is OFF time gate voltage. Again,

$$C_{boot} > \frac{Q_g}{\Delta V_{cc}} = \frac{Q_g}{k_{cc} V_{cc}} \tag{5.12}$$

Usually, k_{cc} is the coefficient to indicate the voltage variations. It is considered as 1-5% of V_{cc} [5] where Q_g is calculated from equation (5.8). Practically maximum value of equation (5.11) & (5.12) is selected for determining bootstrap capacitor value for GaN-FET driver. The circuit parameters of the proposed driver include series resistance (R_{se}), inductor (L_b), and capacitor (C_{boot}). The bootstrap capacitor voltage is limited to 6 V during the charging time, that is, when lower switch is turned ON. The change of gate current is limited by GaN-FET $(di/dt)_{max.}$ Therefore, the inductor voltage can be written approximately as

$$L_b \cong \frac{V_{boot}}{\left|\frac{di}{dt}\right|_{max}} \tag{5.13}$$

During the same time, from the voltage drop in switch resistance (R_{ds}), $\left|\frac{dv}{dt}\right|$ is derived as in (5.14),

$$\left|\frac{dv}{dt}\right| = R_{ds} \left|\frac{di}{dt}\right|_{max} \tag{5.14}$$

The series resistance (R_{se}) is determined by the maximum allowable gate current. For under damped system, $\zeta < 1$,

$$R_{ds} = 2\xi \sqrt{\frac{L_b}{C_{boot}}} \tag{5.15}$$

Therefore,

$$C_{boot} \geq \left(\frac{2\xi}{R_{ds}}\right)^2 L_b \tag{5.16}$$

Small series resistance (R_{se}) can be calculated [14] using the inequality equation i.e.

$$R_{Se} \geq \sqrt{\frac{4L_b}{C_{GS}}} \tag{5.17}$$

Now the design steps need to be verified by two ways:

Process-1: **A**. Calculate C_{boot} from equation (5.11) & (5.12)

B. Take $\zeta<1$, as series path resistance (R_{se})<<R_{ds} calculate , L_b from equation (5.13) i.e. $C_{boot}\left(\frac{R_{ds}}{2\xi}\right)^2 \geq L_b$

C. Calculate $\left|\frac{di}{dt}\right|$ and check that $\left|\frac{di}{dt}\right| < \left|\frac{di}{dt}\right|_{max}$

Process-2: **A**. Calculate L_b from equation (5.13)

B. Take $\zeta<1$, as series path resistance (R_{se})<<R_{ds} calculate, C_{boot} from equation (5.16) i.e., $C_{boot} \geq \left(\frac{2\xi}{R_{ds}}\right)^2 L_b$

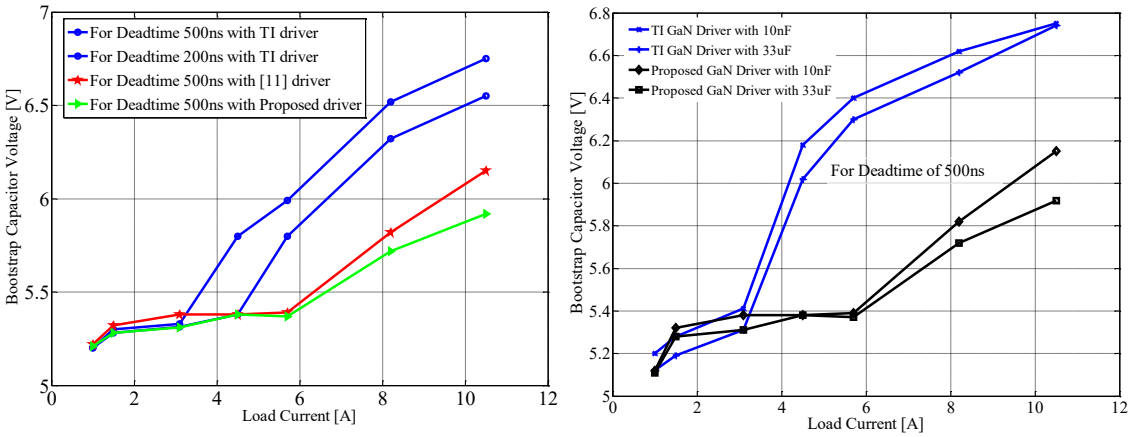
C. Calculate C_{boot} from equation from (5.11) and (5.12) and verify the value derived from equation (5.16) before finalizing driver circuit parameter.

5.3.2. Proposed GaN-FET driver in half bridge DC-DC configuration

The L-D based negative bias turn OFF GaN-FET driver circuit is shown in Fig. 5.8 (c). This configuration is applied in synchronous buck DC-DC converter for steady state and transient performance verification. Simulation study is performed in Multisim 14 version circuit simulation software before hardware implementation.

5.3.3. Performance verification

Applying a negative gate voltage increases $\frac{dv}{dt}$ immunity of the top switch in a synchronous buck DC-DC converter. But it increases V_{SD} value considerably during dead time conduction. A short dip of V_{ds} creates an extra voltage at bootstrap capacitor which in turn exceeds the maximum allowable gate voltage. Therefore, the limitation of bootstrap voltage is important for the reliable switching operation of GaN-FET driver. With the increment of effective dead time, the bootstrap capacitor voltage is recorded for all the three driver circuits as shown in Figs. 5.11 (a) and Fig. 5.11(b) for different load currents. The increment of bootstrap capacitor voltage is found minimum in proposed GaN-FET driver with L-D and zener diode arrangement as shown in Fig. 5.11 (b).



(a). (b)

Fig.5.11. Bootstrap voltage (V_{boot}) for different drivers with load current variations at different (a) dead time (b) C_{boot}.

The bootstrap capacitor voltage not only depends on the load current and driver circuit arrangement but also it depends on capacitor value. For higher capacitance value, the bootstrap capacitor voltage can be limited but it increases the time constant of the driver turn-OFF circuit path. Hence the transient performance becomes poor though it has a better $\frac{dv}{dt}$ immunity. Again, for a fixed dead time, the bootstrap capacitor voltage changes with respect to load current. In this driver design 0.1µH-SMD inductor is used which is also mentioned in the simulation and experimental result section in this chapter. The design value of bootstrap capacitor (C_{boot}) for Si-MOSFET and GaN-FET are shown in Table-5.3.

Table-5.3
Design Value of Bootstrap Capacitor in Si-MOSFET and GaN-FET

	Si-MOSFET@IRF640	GaN-FET@EPC2110
Gate Voltage	ON Time: Vg=12-15V OFF Voltage: Vg=0V	ON Time: Vg<6V OFF Time: Vg<0 i.e. -2.5V
Bootstrap Capacitance	47µF	33uF
Bootstrap Capacitor Voltage rating	63V	15V
'ON' Time Energy Loss	≈6670µJ	≈92µJ
'OFF' Time Energy Loss	≈1240µJ	≈23µJ
Tested Switching Frequency ($f_{switching}$)	156kHz	156kHz
Maximum Duty (D_{max})	90%	90%

It is important to find the bootstrap capacitor voltage for a load current with different capacitance values and dead time so that the turn OFF voltage can be limited to below 6V.

In the proposed GaN-FET driver, the bootstrap voltage is always under 6V and reliable turn-OFF is possible. The performance of the proposed GaN-FET driver is compared with other drivers with respect to bootstrap capacitor voltage at a constant load current as mentioned in Table-5.4. The bootstrap capacitor voltage is least i.e.,5.4V in the proposed driver at 6A load current. A comparison of proposed driver with the existing drivers for different capacitance values are shown in Fig. 5.11 (b). From Fig. 5.11 it is evident that the proposed GaN-FET driver has better $\frac{dv}{dt}$ immunity.

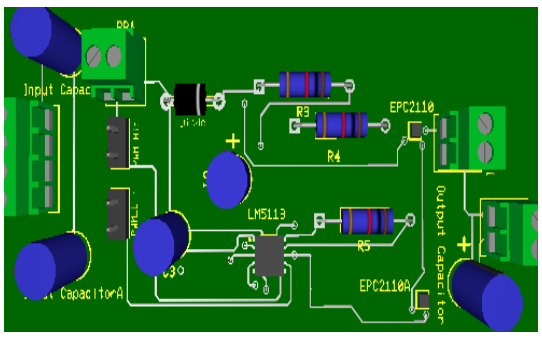
Table-5.4

Comparison of bootstrap capacitor voltage in GaN-FET drivers at constant load current @ 6A

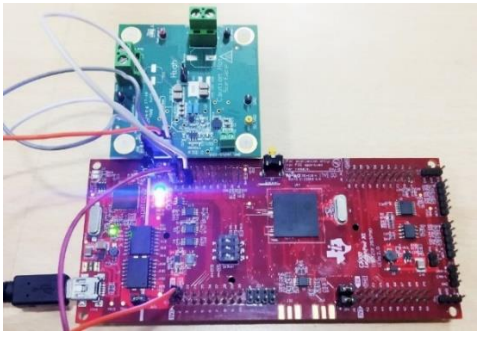
Different Gate Drivers	Bootstrap Capacitor Value	Bootstrap Capacitor Voltage	
		With Dead Time @500ns	Without Dead Time
TI driver [9] with negative biasing turn OFF	33µF	6.3V	6.25V
Driver proposed by P. M. Roschatt *et. al*. [11]	22µF	5.48V	5.41V
Proposed driver	10µF	5.44V	5.40V

5.3.3.1. Steady state performance

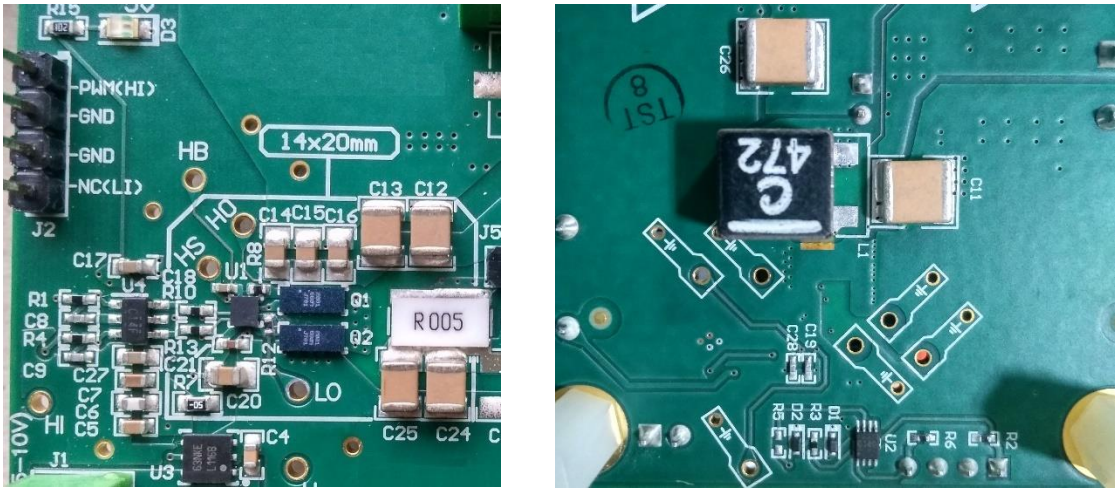
Spice based Multisim model as shown in Fig.5.12 (a) is developed for circuit simulation and for the performance analysis of proposed driver. The hardware prototype is tested and results are compared with texas-LM5113 based GaN-FET driver fed synchronous buck DC-DC converter in open loop and closed loop (voltage mode control) to show the performance improvement. The hardware PCB and prototype model are shown in Fig. 5.12 (b) and Fig. 5.12 (c) and Fig. 5.12 (d).



(a).



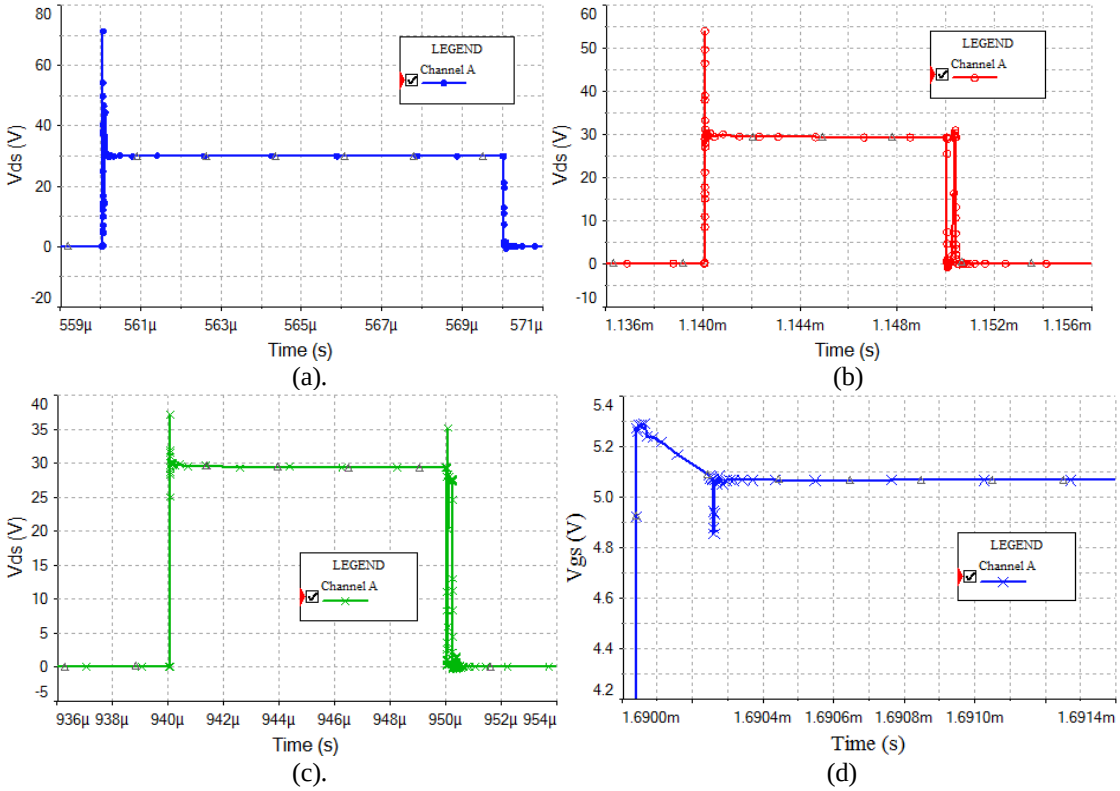
(b)



(c). (d)

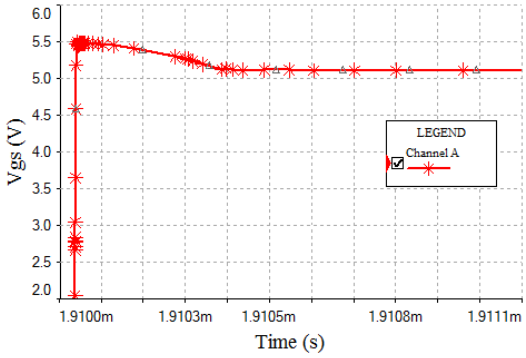
Fig. 5.12. LM5113 based GaN-FET driver fed synchronous buck converter (a) PCB prototype 3D view (Simulated) (b) TMS320F28379D DSP development board. (c) top layer of prototype (d) bottom layer of prototype.

A 0.1µH-SMD inductor is used in the charging path of bootstrap circuit to limit the rise in bootstrap capacitor voltage. The energy stored in inductor is freewheeled through antiparallel diode connected to inductor. This improves $\frac{dv}{dt}$ robustness of GaN-FET switch especially the top switch. The zener diode connected anti-parallel to EPC2110 limits any sudden change in gate voltage during turn-OFF time. Low gate charge of the GaN-FET increases sensitivity to peak gate current. Therefore, bootstrap capacitor voltage should be limited to 6V.

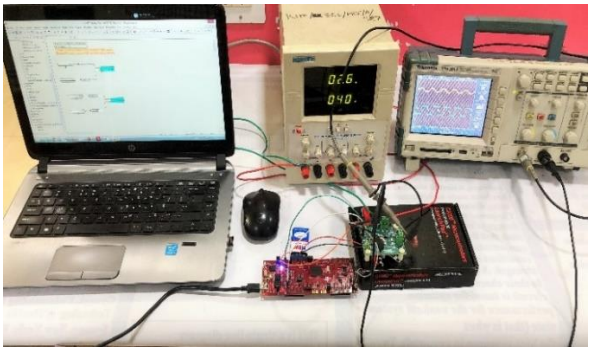


(a). (b)

(c). (d)



(e).

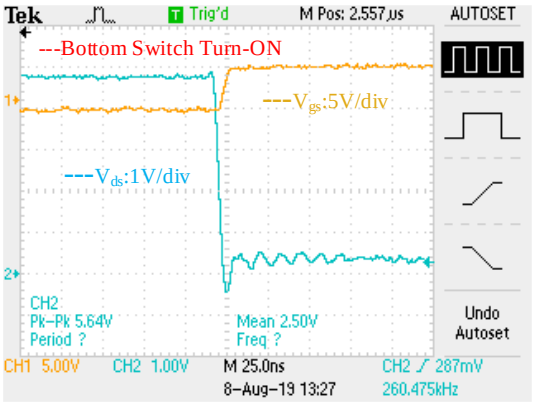


(f)

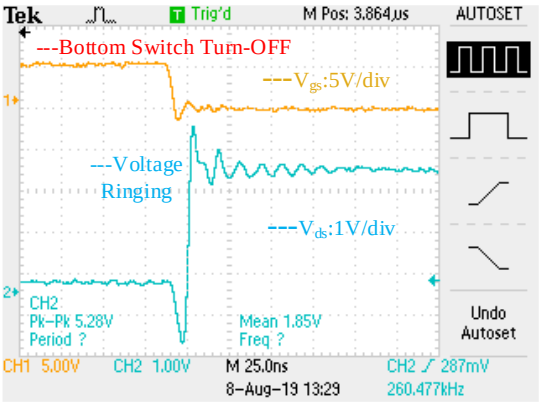
Fig. 5.13. EPC2110 GaN FET drain to source voltage using (a) TI driver (b) driver proposed by P. M. Roschatt *et al*. [11] (c) using proposed driver. EPC2110 GaN FET gate to source voltage using (d) proposed GaN driver (e) driver proposed by P. M. Roschatt *et al*. [11] (f) GaN based synchronous buck converter with DSP board TMS320F28379D.

From the simulation study, it is found that during switch OFF time, the voltage across drain to source will rise at top switch of GaN-FET based synchronous buck converter. Now from Figs. 5.13 (a), 5.13 (b) and Fig. 5.13 (c), it is clear that $\frac{dv}{dt}$ immunity of top switch at turn-OFF time is more in proposed GaN-FET driver compared to others like P. M. Roschatt *et al*. [11] and TI based GaN-FET driver. Therefore, the possibility of false turn ON during turn OFF time can be effectively eliminated by L-D based GaN-FET driver with negative bias.

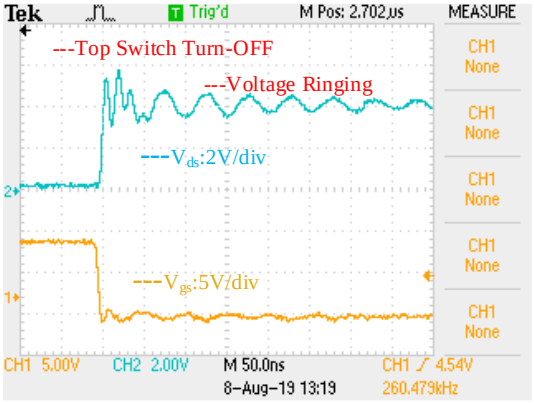
Another advantage of the proposed GaN-FET driver is low gate to source voltage ringing with maximum V_{GS} which is limited to 5.2-5.3V (below 6V) whereas the maximum V_{GS} found in GaN-FET driver proposed by P. M. Roschatt *et al*. [11] is 5.5V-6.1V for L value of 0.1uH. The maximum V_{GS} is shown in Fig. 5.13 (d) and Fig. 5.13 (e) for both the GaN-FET driver circuits. The laboratory based GaN-FET synchronous buck converter prototype is shown in Fig. 5.13 (f). The hardware result of proposed GaN-FET driver fed synchronous buck converter is tested at different frequencies to measure the response time, voltage ringing, and recovery time of the V_{gs} and V_{ds} especially the top switch or high side switch which sometimes mal-operate at high value of load current and larger dead time. The prototype GaN-FET synchronous buck converter is tested at different frequencies to show the switching and gate triggering performance. The ringing in gate pulse using L-D based driver is limited to 5.4V-5.2V and it also reduces the gate conduction loss. The switching behavior of GaN-FET in synchronous buck is shown in Fig. 5.14 at 260 kHz. It is clearly visible from Fig. 5.14 (c) the ringing voltage of top switch V_{ds} is more but it is within limit (<6V) for reliable turn-OFF operation. Also, it is clear that the recovery time is less.



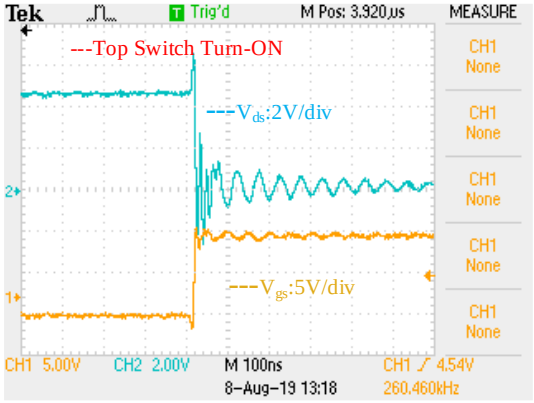
(a).



(b)



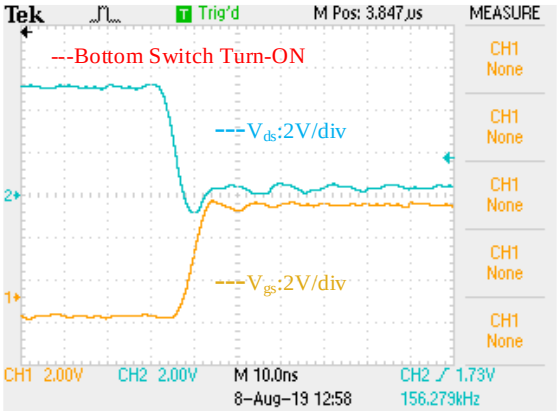
(c).



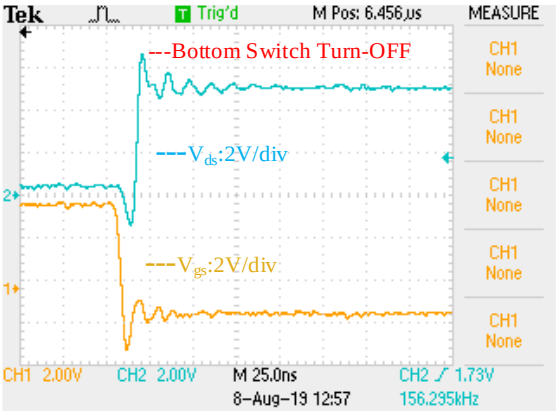
(d)

Fig.5.14. Synchronous buck DC-DC Converter @ 260kHz (a) bottom switch turn 'ON' (b) bottom switch turn 'OFF' (c) top switch turn 'OFF' (d) top switch turn 'ON'.[Yellow-Gate Pulse]

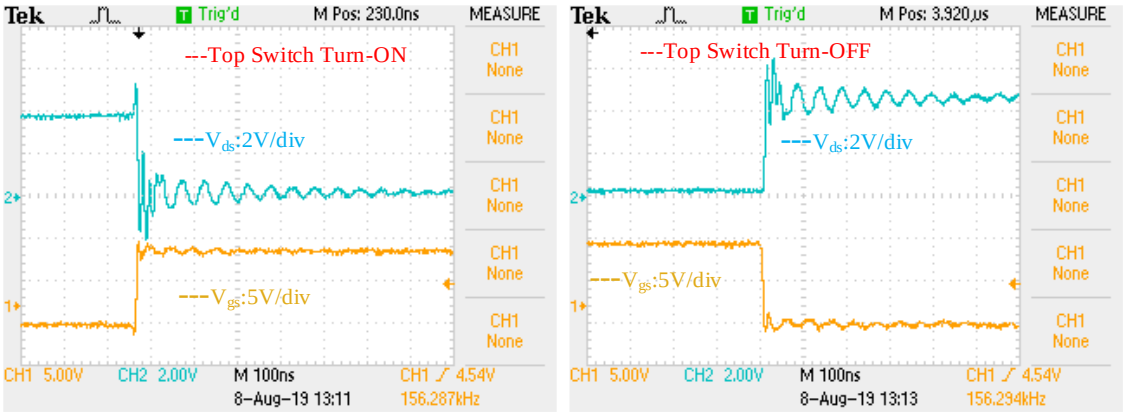
As the bootstrap capacitor voltage is within limit (<6V), the switching operation is fast and reliable. The switching loss is also less compared to Si-MOSFET [IRF640] at same frequency. The same switching test is performed at 156 kHz to verify the operation of GaN-FET devices as shown in Figs.5.15 (a), Fig. 5.15(b), Fig. 5.15 (c) and Fig. 5.15(d).



(a).



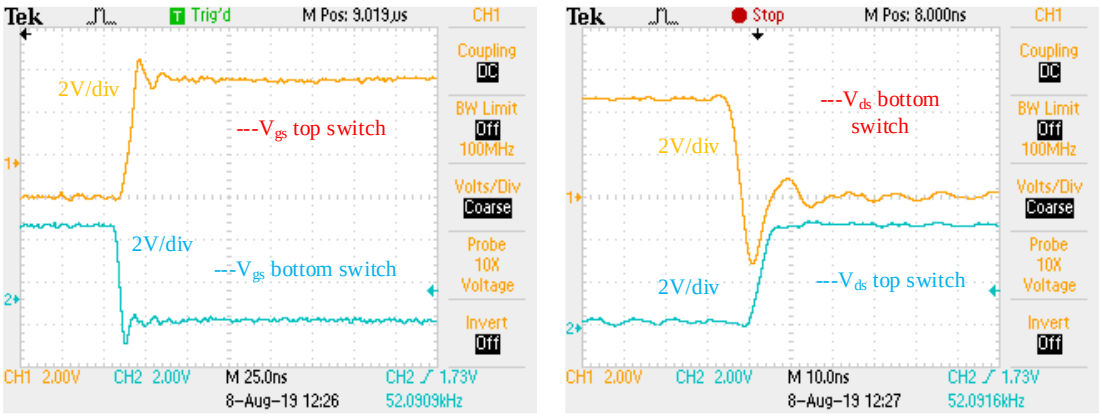
(b)



(c) (d)

Fig.5.15. Synchronous buck @ 156 kHz (a) bottom switch 'ON' (b) bottom switch 'OFF' (c) top switch 'ON' (d) top switch 'OFF'. [Yellow-Gate Pulse]

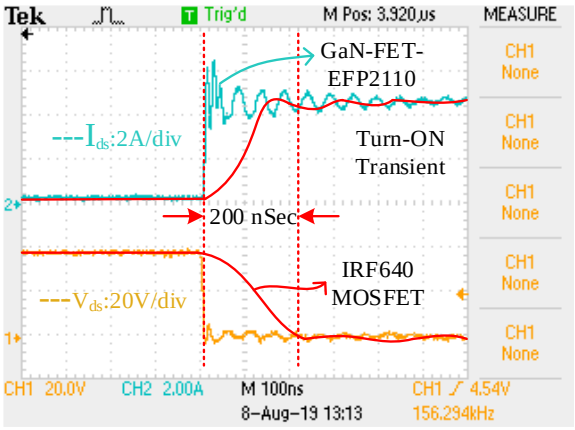
To verify the V_{gs} ringing and switching operation with L-D combination, the same synchronous buck DC-DC converter is tested at low frequency range i.e. at 52 kHz which is shown in Figs. 5.16 (a) and Fig. 5.16 (b).



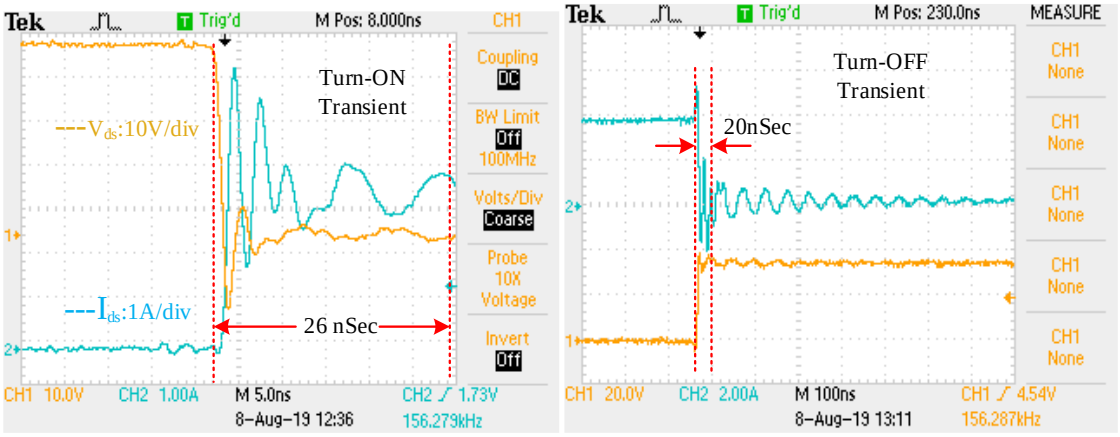
(a). (b).

Fig. 5.16. (a) Gate voltage (V_{GS}) of top [Yellow] and bottom switch [blue] (b) GaN-FET V_{DS} bottom [Yellow] and top switch [blue].

The switching performance of GaN-FET synchronous buck DC-DC converter using proposed driver is compared with IR2110, LM5113 based driver. The turn-ON time for Si-MOSFET based synchronous buck converter is more i.e. 200 ns compared to GaN-FET based converter as shown in Fig. 5.16 (a). The proposed gate driver performs better in terms of faster switching performance as well as in limiting voltage ringing (V_{ds}). The turn-ON and turn-OFF transient time is less compared to LM5113 based drive to GaN-FET (EPC 2110) as shown in Fig. 5.17 and Fig. 5.18.

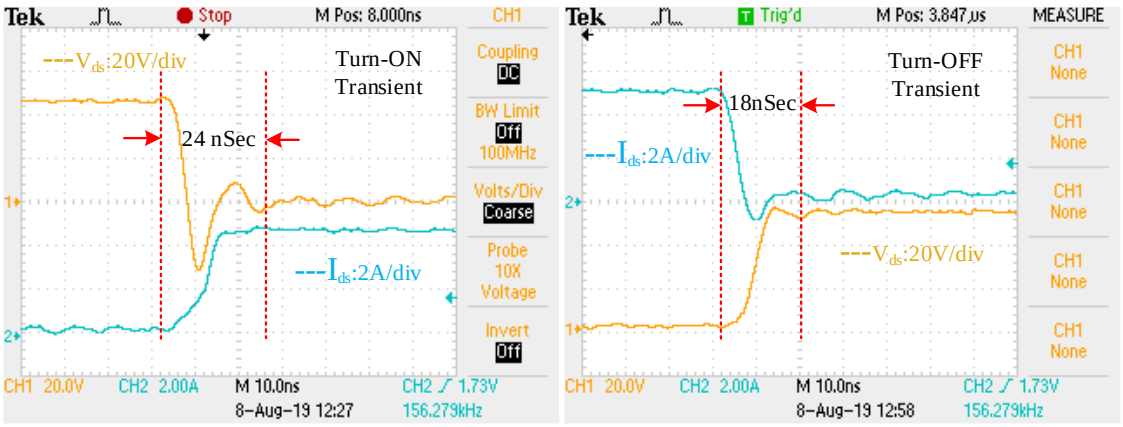


(a)



(b). (c)

Fig. 5.17. (a) Switch voltage (V_{ds}) [Yellow] and current (I_{ds}) [blue] of top Switch (b) LM5113 based GaN-FET V_{ds} [Yellow] and current (I_{ds}) [blue] @ turn-ON (c) LM5113 based GaN-FET V_{ds} [Yellow] and current (I_{ds}) [blue] @ turn-OFF.



(a). (b)

Fig. 5.18. (a) Switch voltage (V_{ds}) [Yellow] and current (I_{ds}) [blue] of top Switch at (a) turn-ON (b) turn-OFF.

The energy loss during switch-ON time is more compared to switch-OFF time for MOSFET. This energy loss increases with higher switching frequency but for GaN-FET this loss is very less. Loss comparison for different configuration is mentioned in Table-5.5.

Table-5.5
Switching and conduction loss comparison @ 156 kHz

GaN-FET@ Proposed driver for EPC2110		Si-MOSFET@IRF640	GaN-FET@ LM5113 driver for EPC2110
Gate Conduction Loss	Low	Medium	Medium
Energy Loss On Time	85µJ	6670µJ	92µJ
Voltage Ringing	Less (≈20 nsec)	Less (≈30-50nsec)	More (≈200nsec)

5.3.3.2. Transient performance using voltage mode control

The closed loop performance is tested in proposed GaN-FET driver fed synchronous buck converter. Simple voltage mode control [13] is implemented to check tracking performance for step reference voltage change. Reference voltage is changed from 5V to 10V.

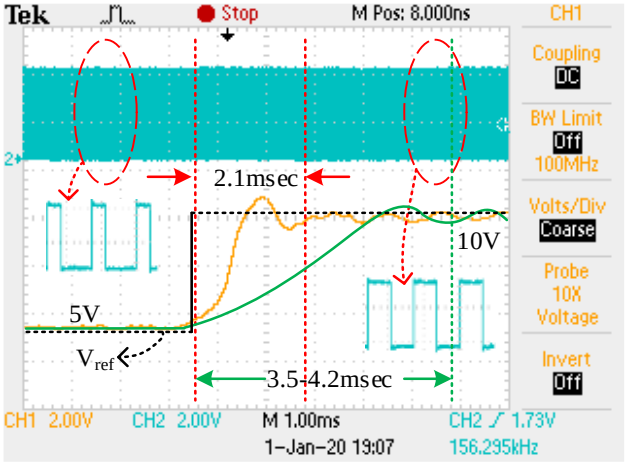


Fig.5.19. Closed loop voltage mode control of GaN-FET synchronous buck converter tracking performance using PI controller.

A faster transient response is observed in the GaN-FET converter compared to Si-MOSFET based circuit as shown in Fig. 5.19. Different performance parameters are listed in Table-5.6 to show the performance improvement.

Table-5.6
Transient performance comparison @ 156 kHz

GaN-FET@ Proposed driver for EPC2110		Si-MOSFET@IRF640	GaN-FET@ LM5113 driver for EPC2110
Settling Time	2.1 msec	≈3.5-4.2 msec	≈2.1msec
False Triggering	Yes	Limited higher frequency	NO

Protection		Operation.	
Voltage Ringing	Less	No ringing.	Medium
Peak Gate Voltage	5.2V-5.3V	12V-15.4V	5.6V-6.5V

This chapter conveys the performance improvement of GaN-FET (EPC2110) based synchronous buck converter using L-D based new FET driver with negative bias. The proposed driver provides false triggering protection of DC-DC converter under loaded condition. The V_{ds} ringing is low at higher switching frequency compared to other driver found in literature. The switching loss of GaN-FET (EPC2110) is low compared to Si-MOSFET (IRF640) and the transient response is also faster. The proposed driver is also capable to limit bootstrap voltage below 6V for load current above 5A which ensures reliable switching operation of DC-DC converter. It performs better than LM5113 based driver and small inductor-based driver in terms of $\frac{dv}{dt}$ robustness.

5.4. Performance Improvement of BDC using Proposed GaN-FET Driver

The proposed L-D based GaN-FET driver is used for designing GaN-FET based implementation of CIBDC as shown in Fig. 5.20.

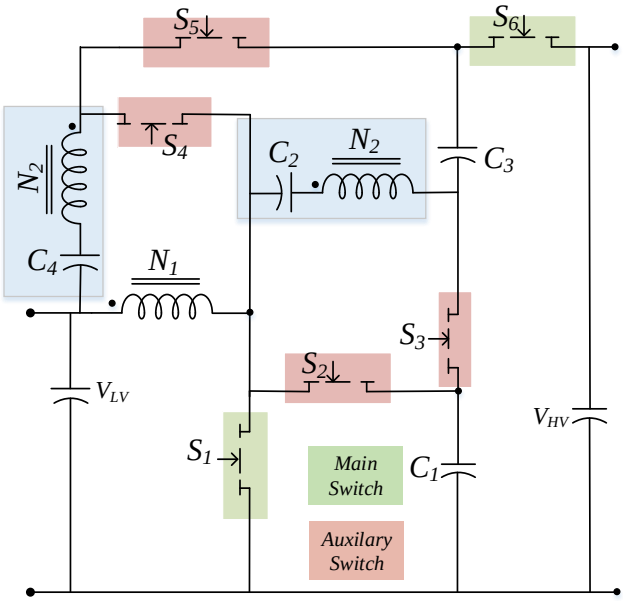


Fig. 5.20. Proposed coupled-inductor based bidirectional converter (CIBDC) using two secondary branches.

The operation and MOSFET based implementation of CIBDC are discussed in the previous chapter in details. Therefore, the major achievement using GaN-FET based implementation of CIBDC is discussed here. Using TO-220 package of GaN-FET the size of 250W

converter is reduced and other benefits like soft switching of all switches are still valid. Due to reduction in the conduction loss the efficiency of the CIBDC is increased. The component details for the prototype is mentioned in Table-5.7.

Table-5.7
GaN-FET Based CIBDC Circuit Parameter

CIBDC Specification		
Input Voltage = 48 V	Power Output = 250 W	Output Voltage = 384 V
	Switching Frequency=50 kHz	
Design Parameters	**Value**	**Part Number**
Coupled Inductor	L_m = 45 µH, Turns Ratio 25:25 (*n = 1*), $L_{leakage}$ = 7.15 µH	Ferrite Core PQ 32/30
GaN Switches (S_1, S_2, S_3, S_4, S_5, S_6)	TPH3212PS (V_{ds} = 650 V, R_{ds} = 0.085 Ω, I_d=31 A.) @ 250W	TPH3212PS
Capacitor C_1, C_2, C_3	Simulated:12 µF, hardware: 10µF	
Capacitor C_4	Simulated:15 µF, hardware: 10µF	
Capacitor C_{LV}	100 µF	
Capacitor C_{HV}	470 µF	

The designed bidirectional DC-DC converter is capable of delivering high voltage conversion ratio in both buck and boost mode of operation. In this CIBDC topology higher conversion factor i.e. ≥10 in boost and ≤1/10 in buck mode are obtained with unity turns ratio (*n=1*). Voltage stress is less in GaN-FET switches in both the operating modes which enables to select low voltage, low ON state resistance of GaN-FET devices.

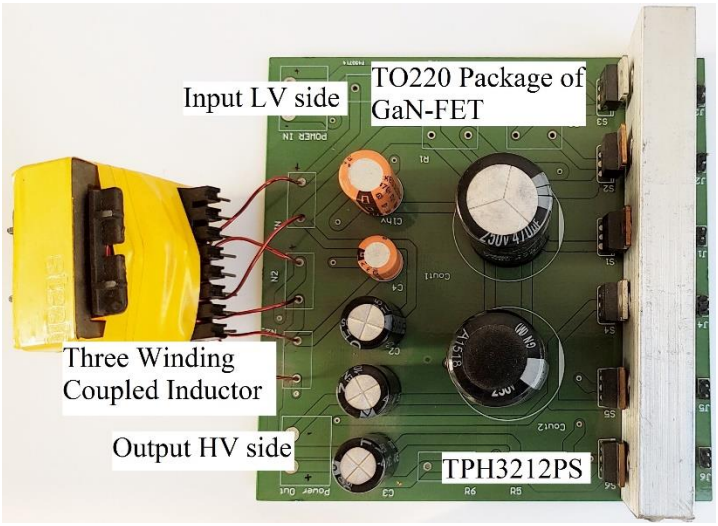


Fig. 5.21. Hardware prototype of 250W GaN-FET based CIBDC

This helps to reduce conduction loss. Again, all the active switches are soft switched i.e., ZVS. Therefore, switching loss is negligible which further improves the conversion efficiency. The proposed converter as shown in Fig. 5.21 utilized two parallel inductor current paths to share input currents during boost as well as in buck mode which reduces

current rating of individual coils and helps in reducing input current ripple. Due to topological advantage the leakage inductance energy is directly transferred to load. The detailed analysis of topological derivation, current and voltage stress along with efficiency calculation in steady state is discussed in the previous chapter. The maximum measured efficiency is 96.12% in buck mode at 170W and 96.63% in boost mode at 190W. Further, 1-1.5% efficiency improvement of CIBDC is possible by selecting switching frequency greater than 100 kHz which minimizes reverse conduction loss of GaN-FET switches to a negligible value. The benefits and one major disadvantage of using GaN-FET in place of MOSFET is mentioned in Table 5.8.

Table-5.8
Advantages of GaN-FET implementation over MOSFET

Loss Component	Advantages
Conduction Loss	Less than MOSFET
Switching Loss	Less than MOSFET
Transient response	Betterment in approximately 10-15% in transient behaviour
Loss Component	Disadvantages
Reverse diode conduction to achieve soft switching	3rd quadrant operation of GaN-FET has increased conduction loss compared to MOSFET
SMD assembly	SMD assembly is difficult in case of GaN-FET

5.5. Summary

The main objective of this chapter is to design proposed CIBDC using GaN-FET. The operation of the CIBDC is already explained in chapter 4, therefore this part is not repeated in this chapter. However, the difficulties especially reliable gate driver for GaN-FET is discussed in details in this chapter. L-D based reliable GaN-FET driver is also proposed which performs well in synchronous buck converter. The same driver circuit is adopted while implementing GaN-FET based CIBDC. Due to application of GaN-FET based switch the peak efficiency of the CIBDC is enhanced by 1-1.5%. Physical antiparallel diode is not present in GaN-FET, but third quadrant operation is possible by adjusting the gate voltage. However, reverse conduction or third quadrant operation to achieve soft switching operation of GaN-FET increases the reverse conduction loss. This extra conduction loss restricts to achieve more efficiency from the CIBDC. The peak efficiency of 250W CIBDC using GaN-FET switch is 96.12% in buck mode and 96.63% in boost mode.

5.6. Publications and References

Publications

Journals:

[1] **S. B. Santra**, A. Roy, T. R. Choudhury, D. Chatterjee and B. Nayak, "Performance Improvement of DC-DC Converter using L-D based modified GaN-FET driver", **International Journal of Circuit Theory and Applications**, Vol. 48, no. 6, pp. 860-873, April. 2020.

[2] **S. B. Santra**, M. Ramana and D. Chatterjee, "Performance Analysis of Novel Bidirectional DC-DC Converter with LD based Modified GaN-FET Driver", **IEEE Transactions on Industry Applications**, Vol. 57, no. 5, pp. 5199-5214, Sept.-Oct. 2021.

Conferences:

[1] **S. B. Santra**, A. Roy and D. Chatterjee, "Design of Bootstrap Capacitor Based GaN-FET Driver for Improvement in Transient Performance of DC-DC Converter", **Proceedings of 2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE 2020)**, Cochin, India, 2020.

[2] **S. B. Santra**, K. Bhattacharya, T. R. Choudhury and D. Chatterjee, "Generation of PWM Schemes for Power Electronic Converters", **Proceedings of 2018 20th National Power System Conference (NPSC)**, NIT Tiruchirappalli, India, 2018.

References

[1] Yongheng Yang, Katherine A., Kim Frede Blaabjerg, Ariya Sangwongwanich "*Advances in Grid-Connected Photovoltaic Power Conversion Systems*", 1st edition, Woodhead Publ*ishing*, Aug. 2018.

[2] W. Zhang et al., "Wide bandgap power devices based high efficiency power converters for data center application," *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, Knoxville, TN, 2014, pp. 121-126.

[3] K. Kumar and S. B. Santra, "Performance Analysis of a Three-Phase Propulsion Inverter for Electric Vehicles Using GaN Semiconductor Devices," in *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 6247-6257, Nov.-Dec. 2018.

[4] A. M. S. Al-bayati, S. S. Alharbi, S. S. Alharbi and M. Matin, "A comparative design and performance study of a non-isolated DC-DC buck converter based on Si-MOSFET/Si-Diode, SiC-JFET/SiC-schottky diode, and GaN-transistor/SiC-Schottky diode power devices," *2017 North American Power Symposium (NAPS), Morgantown*, WV, 2017, pp. 1-6.

[5] Fei Wang, Zheyu Zhang and Edward A. Jones “Characterization of Wide Bandgap Power Semiconductor Devices” 1st Edition, *IET Energy Engineering Series*, IET Publishers, Feb. 2018.

[6] K. Kruse, M. Elbo and Z. Zhang, "GaN-based high efficiency bidirectional DC-DC converter with 10 MHz switching frequency," 2017 *IEEE Applied Power Electronics Conference and Exposition* (APEC), Tampa, FL, 2017, pp. 273-278.

[7] E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, Sept. 2016.

[8] A. Lidow and J. Strydom, “eGaN FET drivers and layout considerations”, *Efficient Power Conversion Corp*. Dec 2012. [Online] El Segundo, CA, USA. Available: http://epc-co.com/epc/DesignSupport.aspx

[9] Chellappan, Salil. "Design considerations of GaN devices for improving power-converter efficiency and density." *Texas Instruments* Inc., April-2017.

[10] Z. Zhang, L. M. Tolbert, D. Costinett, F. Wang and B. J. Blalock, "A New Hands-On Course in Characterization of Wide-Bandgap Devices," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9392-9403, Oct. 2019.

[11] P. M. Roschatt, S. Pickering and R. A. McMahon, "Bootstrap Voltage and Dead Time Behavior in GaN DC–DC Buck Converter with a Negative Gate Voltage," in *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7161-7170, Oct. 2016.

[12] T. Nag, S.B. Santra, A. Chatterjee, D. Chatterjee and A.K. Ganguli, “Fuzzy logic-based loss minimization scheme for brushless DC motor drive system,” *IET Power Electronics*., vol. 9, no. 8, pp. 1581-1589, June.2016.

[13] R.W.Erickson and D.Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA, Kluwer, 2001.

[14] GaN-Tr Application Note (PGA26E07BA) Panasonic.

https://industrial.panasonic.com/content/data/SC/ds/ds8/c2/APN_PGA26E07BA_EN.pdf.

Chapter-6

Reduced Input Ripple Current (RIRC) Operation of BDC

The efficiency, voltage gain, less voltage and current stress can be achieved using coupled inductor based BDC with GaN-FET switch. However, the application to energy storage in microgrid of EV will not be successful due to large inductor ripple current at low voltage which is essentially for the battery side. This ripple current needs large input filter capacitor at LV side so that capacitor can supply ripple current. Otherwise, battery needs to supply the ripple current which means less battery life and regular maintenance. The large ripple current at LV side of BDC can be eliminated by choosing proper topology or circuit arrangement. Interleaved structure based high gain non-isolated BDC can solve the input ripple current problem. However, due to large component count the efficiency of the interleaved high gain non-isolated BDC is less. In this chapter an alternate way to reduce input ripple current without sacrificing on component count and efficiency is proposed. This proposed circuit structure helps to achieve higher efficiency, large voltage gain, less input ripple current. Thus, necessary of connecting large filter capacitor at LV side is eliminated by this proposal.

6. Input Current Ripple Reduction of BDC

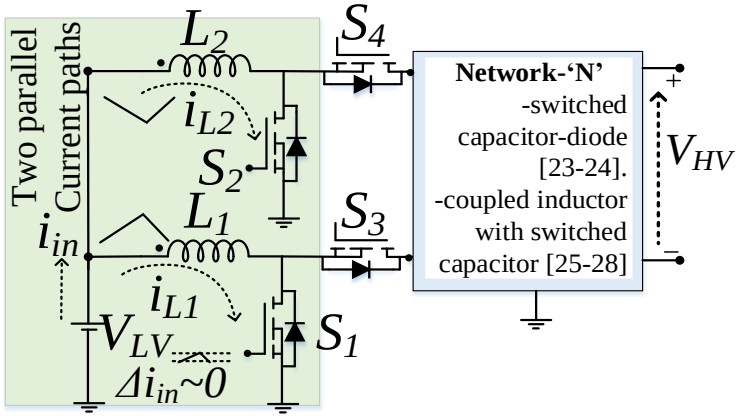
6.1. Introduction

In the previous chapters, it is discussed that the efficiency, voltage gain, less voltage and current stress can be achieved using coupled inductor based BDC with GaN-FET switch. However, the application to energy storage in microgrid of EV will not be successful due to large inductor ripple current at low voltage side which is essentially the battery side. This ripple current needs large input filter capacitor at LV side so that capacitor can supply ripple current. Otherwise, battery needs to supply the ripple current which means less battery life and regular maintenance. The large ripple current at LV side of BDC can be eliminated by choosing proper topology or circuit arrangement. Interleaved structure based high gain non-isolated BDC can solve the input ripple current problem. However, due to large component count the efficiency of the interleaved high gain non-isolated BDC is less. In this chapter an alternate way to reduce input ripple current without sacrificing on component count and efficiency is proposed. This proposed circuit structure helps to achieve higher efficiency, large voltage gain, less input ripple current. Thus, necessary of connecting large filter capacitor at LV side is eliminated by this proposal.

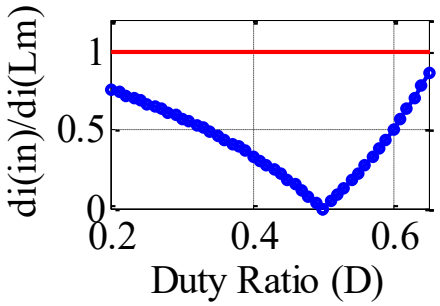
6.2. Interleaved structure at low voltage side

Bidirectional DC-DC converters (BDC) are an integral part of applications like energy storage interface in DC microgrid [1], and electric vehicle (EV) [2] etc. Generally, energy storage is of low voltage (LV) type i.e., 12V-48V and high voltage (HV) side is at 300 V-400 V. Two-switch topologies of non-isolated BDC [3-4] are not capable to provide such high gain requirements in both buck and boost modes due to extreme duty ratio requirement. The voltage gain requirement [1-2] of BDC in some application ranges from 5-10 times in step-up and similarly in the step-down mode. To meet the gain requirement, BDCs uses various techniques which can be isolated and non-isolated in nature. Isolated BDC can provide gain requirement using transformer winding and duty ratio adjustment. The number of active switches is generally greater than eight or more in full bridge isolated BDC [5-6]. Half bridge topologies [7] are good choice for BDC, however, the complexity in soft switching and control [8] of these types of BDC left a good scope of non-isolated BDC. There are different circuit principles used to achieve high gain in these types of BDCs like SEPIC derived [9], switched capacitor based [10-11], coupled inductor based [12]-[16] etc. Voltage gain of non-isolated BDC can be further enhanced by using hybrid structures

like, SEPIC with switched capacitor, quasi-Z source with switched capacitor [17] etc. These converters also provide good dynamic response. However, large component count is inevitable using hybrid structure, which limits the operating efficiency. All high gain non-isolated BDC circuits have common problem of large ripple current at low voltage (LV) side. This is a major concern of BDC applications for energy storage interface. Large ripple current degrades the performance and life of the battery. Large capacitor can manage the input ripple current [18], but this is not desirable as it increase the size and cost of the system. The conventional interleaved BDC circuit [19-20] is capable to significantly reduce the input ripple current at LV side and ideally at D=0.5 ripple current value can be zero. However, it does not improve the voltage gain factors i.e., 1/(1-D) in boost mode and D in buck mode [20], [21]. Zero voltage transition (ZVT) network based BDC is also found in literature where auxiliary switch is used to achieve ZVZCS operation [22] in the main switch. However, limited voltage gain restricts its application in 48V-400V system. Fig. 6.1 (a) shows generalized topology of interleaved BDC [10], [23]-[28] with higher voltage gain using two parallel inductor-switch combination at LV side.



(a)



(b)

Fig. 6.1. Interleaved two phase BDC with high voltage gain and less input current ripple (a) general structure (b) input ripple current at LV side in p.u.

The structure mentioned in Fig. 6.1(a) has many advantages including less input current ripple and common ground that has less EMI problem. The complementary operation of

two switches (S_1 and S_2) with input inductors confirms opposite slope inductor currents which reduces the input current ripple.

6.3. Limitations of Interleaved structure in BDC design

The basic BDC operation can be achieved using synchronous boost converter where switching sequence controls the mode of operation. The basic BDC is shown in Fig. 6.2.

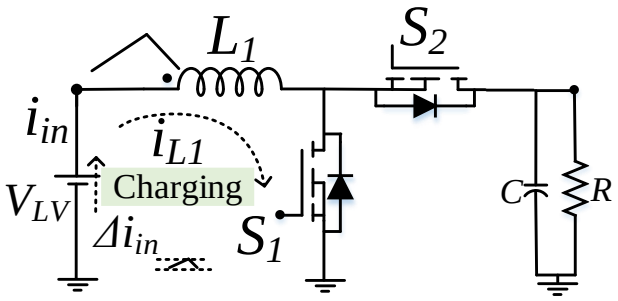


Fig. 6.2. Conventional synchronous BDC

The input LV current ripple without using filter is same as inductor current ripple. To reduce ripple current large size inductor is required. The voltage conversion factor for boost mode is 1/ (1-D) and in buck mode it is D. However, LV ripple current can be reduced without increasing inductor size. To eliminate the input LV ripple current interleaved structure based basic BDC can be used as shown in Fig. 6.3. The ripple current is less and in 0.5 duty it becomes zero. However, voltage conversion factor is same in this BDC circuit. Two slopes of the loop currents i.e. i_{l1} and i_{l2} are opposite as shown in Fig. 6.3.

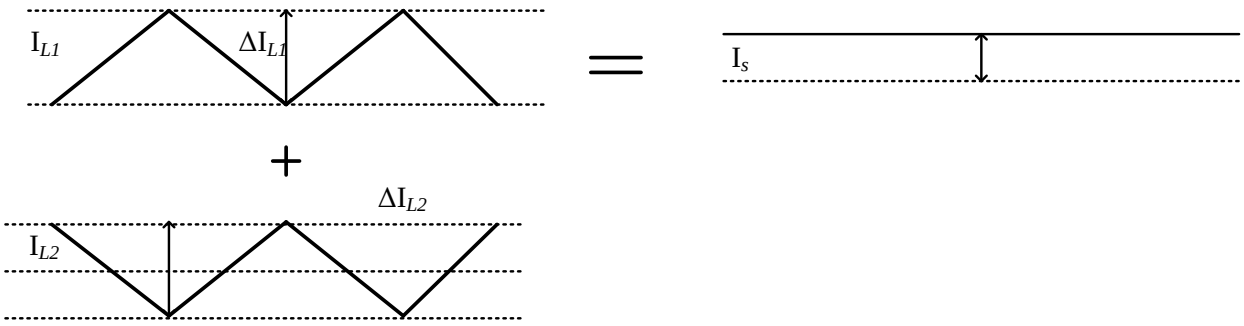


Fig. 6.3. Ideal interleaved structure loop current and input current at D=0.5.

The variation of input ripple current with changes in duty ratio is shown in Fig. 6.1(b). However, the voltage lifting of these interleaved BDC solely depend on the network 'N', as shown in Fig. 6.1(a) which may be switched capacitor or coupled inductor network etc. The major problems of these voltage lifting networks are: (a) larger energy storing elements (L and C) to pump enough energy to the network 'N' ($0.5Li^2$ or $0.5CV^2$); (b) elevated current stress on switches especially at main switch of LV side (c) additional switch compared to single switch coupled inductor based BDCs. The above problems left a

research gap to find an alternative BDC circuit using only one main switch at LV side which performs similar to interleaved high gain BDC with a feature to reduce input ripple current (RIRC) at LV side and reasonable voltage transfer ratio. A zero-input ripple current based high gain boost converter is proposed in [29], however, a large input inductor is used and still it does not guarantee RIRC operation throughout wide duty ratio range. Recently parallel coupled inductor based high gain interleaved BDC is proposed [34] whose current ripple performance is similar to Fig.6.1 (b) and has high conversion factors. This is a promising solution of non-isolated BDC circuit. In the proposed approach, the BDCs ensure less component count and better voltage gain compared to the method shown in Fig. 6.1. Additionally, all semiconductor switches operate at ZVS-turn ON in both operating modes, resulting in a higher efficiency. The proposed method also utilizes parallel path structure to achieve current sharing in both operating modes resulting in RIRC at LV side.

6.4. Proposed interleaved circuit arrangement using single switch

The RIRC operation at LV side can be achieved topologically using two methods i.e., either using (a) already existed two main switch based interleaved structure, where switching of two inductors are complementary (Fig. 6. 4(a)), or Fig. 6. 4(b) using capacitor branch parallel to the inductor (Fig. 6.4(b)) using one main switch.

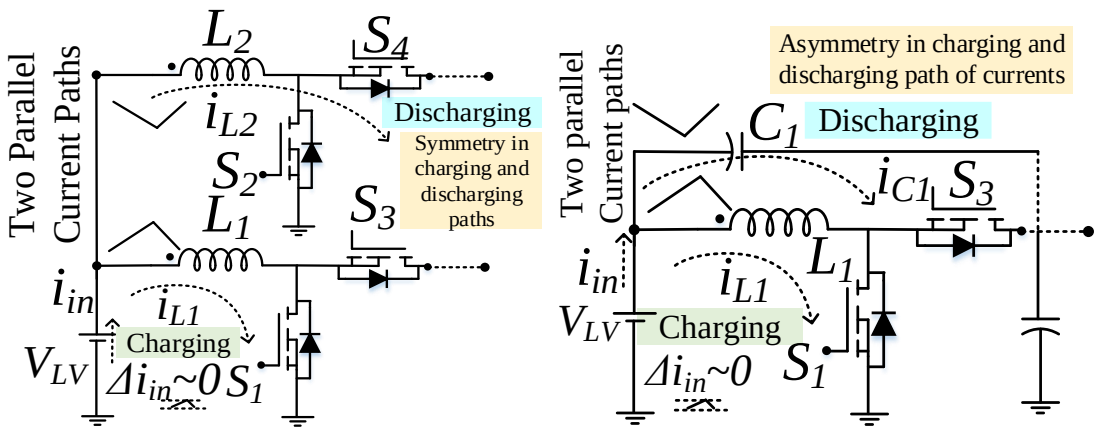


Fig. 6.4. Interleaving with (a) two inductor two switch (symmetric network) (b) one inductor and one capacitor with one switch (asymmetric network).

The proposed solution uses one main switch at LV side with input inductor and a parallel capacitor. To ensure a reduced ripple current, the inductor and capacitor should charge and discharge in a complementary fashion completing their individual loop current paths through V_{LV} and S_1. The proposed LV side structure has asymmetry in inductor charging and

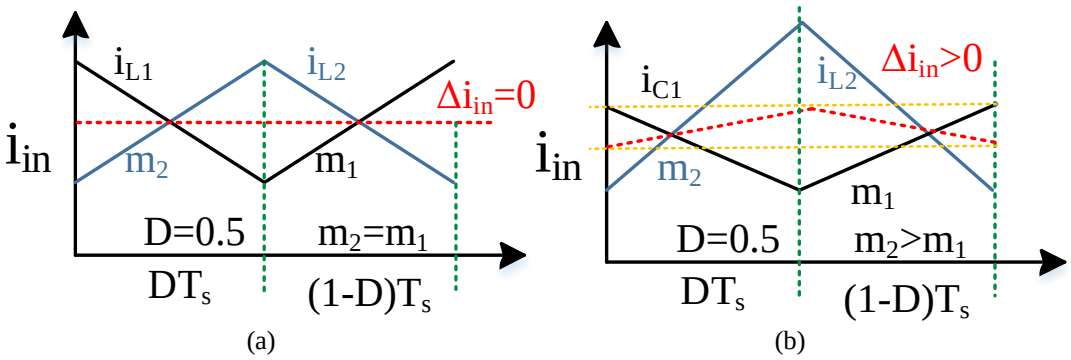


Fig. 6.5. Input current ripple at D=0.5: (a) ideal interleaved (symmetric network) and (b) proposed single switch asymmetric network.

discharging with capacitor charging and discharging as their paths are different, but slope is opposite with respect to input current. This asymmetry eliminates one extra switch requirement and also helps to improve the voltage gain. But due the asymmetry in the charging and discharging path, the magnitude of capacitor and inductor current slopes are different. It is possible to achieve ideal zero ripple current at D=0.5 as shown in Fig. 6.5(a) in interleaved BDC due to equal and opposite current slopes ($m_1=m_2$). In proposed solution, ripple current is not zero at D=0.5 due to asymmetry in current slopes ($m_1 \neq m_2$) as shown in Fig. 6.5(b). However, the proposed solution has advantage of uniform p.u. ripple current as illustrated in Fig. 6.8(d) over a wide duty ratio range. The comparison details are presented in next section.

6.5. Topology derivation using proposed interleaved structure at LV side

The circuit structure at LV side as shown in Fig. 6.4(b) is utilized to design the BDC circuit. During boost stage design of proposed BDC half cycle resonating branch [36] is adopted with coupled inductor where capacitor is connected in parallel to primary inductor to achieve high voltage gain and ripple current reduction simultaneously.

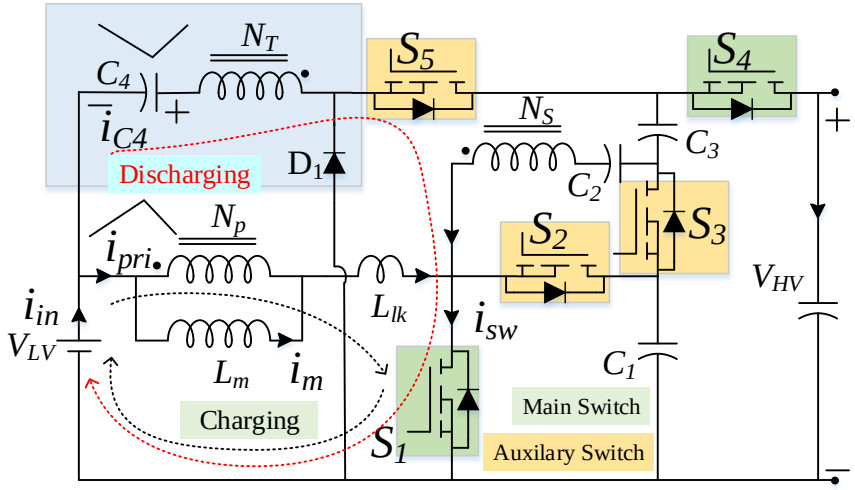


Fig. 6.6. Proposed coupled inductor based BDC for achieving RIRC operation.

By incorporating parallel capacitor branch and modifying the boost stage circuit [36], a new soft switched BDC circuit is derived which has very less LV side input current ripple and has superior conversion factor in both operating modes. The diodes [36] are simply replaced by switches and tertiary winding is used in coupled inductor to achieve BDC stage, which ensures RIRC operation. The schematics of the proposed BDC incorporating parallel capacitor branch with coupled inductor primary is shown in Fig. 6.6. The proposed BDC utilized two main switches and three auxiliary switches with less winding turn ratio (n = 1) to achieve higher voltage transformation factor and RIRC operation. Synchronous rectification-based operation ensures ZVS turn ON of all active switches in both operating modes, which improves conversion efficiency.

6.5.1. Input current ripple performance at LV side

The complete input current equation during the main switch (S_1) ON time is vital to know the input ripple current. There are two loops of the input current during the main Switch S_1 turn-ON in the boost mode.

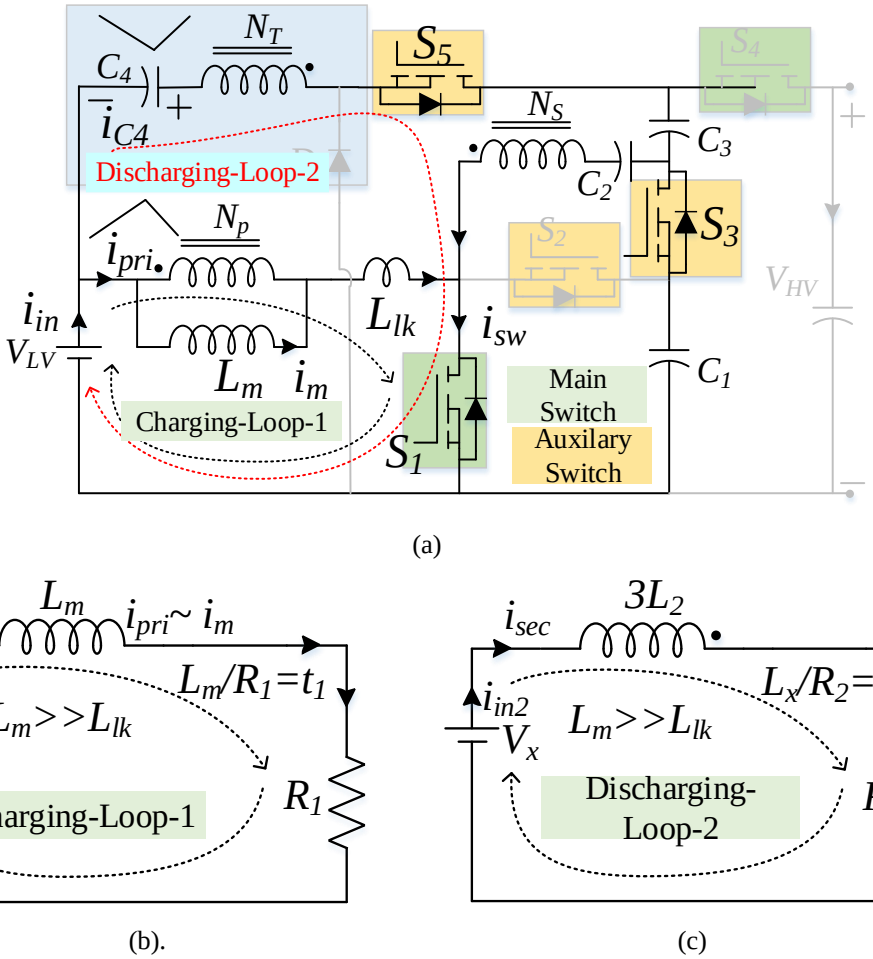


Fig. 6.7. Proposed BDC at S_1 ON in boost mode (a) main circuit with two input current loops (b) equivalent circuit for loop-1 (c) equivalent circuit for loop-2.

The two loops current, i.e., one through the coupled inductor primary winding and another through the capacitor and coupled inductor secondary windings passes through the main Switch S_1 as shown in Fig. 6.7 (a).

The KVL equation (1) for the loop-1 circuit as shown in Fig. 6.7 (b) at $0<t<T_{on}$ can be written as

$$v_{LV} = L_m \frac{di_{Lm}(t)}{dt} + R_1 i_{Lm}(t) \tag{6.1}$$

Where L_m is the magnetizing inductance, R_1 is the equivalent resistance by combining switch S_1 ON state resistance and winding N_T resistance. Leakage inductance L_{lk} is neglected as it has very less value compared to L_m. During S_1 ON time, the input current (I_{in1}) is approximately same as magnetizing current. Considering the minimum value of the I_{in1} to I_{Lmin}, the time domain solution of equation (6.1) can be derived as:

$$i_{in1}(t) = \frac{v_{LV}}{R_1}\left(1 - e^{\frac{-R_1}{L_m}t}\right) + i_{L\min} e^{\frac{-R_1}{L_m}t} \tag{6.2}$$

Similarly, for loop-2 as shown in Fig. 6.7 (c) the KVL equation is

$$v_x = L_x \frac{di_{sec}(t)}{dt} + R_2 i_{sec}(t) \tag{6.3}$$

Where V_x is the effective voltage = $(V_{c2}+V_{c3})-(V_{LV}+V_{c4})$, L_x is the effective inductance ≈ $3L_2$ (L_2 is secondary winding inductance), R_2 is the effective resistance including switch (S_1) ON state resistance. The current in this loop is in the falling slope. Considering the maximum value of the I_{sec} to I_{secmax} ,the time domain solution of equation (6.3) can be derived which is

$$i_{in2}(t) = \frac{-v_x}{R_2}\left(1 - e^{\frac{-R_2}{L_x}t}\right) + i_{secmax} e^{\frac{-R_2}{L_x}t} \tag{6.4}$$

The resultant input current can be derived by adding individual loop current for $0<t<T_{on}$ i.e.

$$i_{in}(t) = i_{in1}(t) + i_{in2}(t) \tag{6.5}$$

$$i_{in}(t) = \frac{v_{LV}}{R_1}\left(1 - e^{\frac{-R_1}{L_m}t}\right) + i_{L\min} e^{\frac{-R_1}{L_m}t} - \frac{v_x}{R_2}\left(1 - e^{\frac{-R_2}{L_x}t}\right) + i_{secmax} e^{\frac{-R_2}{L_x}t} \tag{6.6}$$

The maximum value of the input current condition is derived by putting d/dt ($I_{in}(t)$) =0 which is

$$\left(\frac{v_{LV}}{L_m} - \frac{R_1 i_{L\min}}{L_m}\right) = \left(\frac{v_x}{L_x} + \frac{R_2 i_{secmax}}{L_x}\right) e^{-t\left(\frac{R_2}{L_x} - \frac{R_1}{L_m}\right)} \tag{6.7}$$

Equation (6.7) can be written as

$$A = Be^{-Ct} \tag{6.8}$$

The time for maximum value can be derived from (6.8) and using this time value, the maximum input current value is also derived which is mentioned in equation (6.9) and (6.10) respectively.

$$t = \frac{1}{C}\ln\left(\frac{B}{A}\right) \tag{6.9}$$

$$i_{inmax} = \frac{v_{LV}}{R_1}\left(1-\left(\frac{A}{B}\right)^{\frac{R_1}{CL_m}}\right)-\frac{v_x}{R_2}\left(1-\left(\frac{A}{B}\right)^{\frac{R_2}{CL_x}}\right)+i_{Lmin}\left(\frac{A}{B}\right)^{\frac{R_1}{CL_m}}+i_{secmax}\left(\frac{A}{B}\right)^{\frac{R_2}{CL_x}} \tag{6.10}$$

Where, $A = \left(\frac{v_{LV}}{L_m}-\frac{R_1 i_{Lmin}}{L_m}\right)$ $B = \left(\frac{v_x}{L_x}+\frac{R_2 i_{secmax}}{L_x}\right)$, $C = \frac{R_2}{L_x}-\frac{R_1}{L_m}$, $t_1 = \frac{L_m}{R_1}$ and $t_2 = \frac{L_x}{R_2}$

As in (6.6) it is clear that the minimum current can be found at the end of ON time i.e., $t=DT_s$. By putting this timing value, the minimum input current value is derived. Thus, the input ripple current is

$$\Delta i_{in} = i_{inmax} - i_{inmin} \tag{6.11}$$

$$\Delta i_{in} = \left(\frac{v_{LV}}{R_1}-i_{Lmin}\right)\left(e^{\frac{-DT_s}{t_1}}-\left(\frac{A}{B}\right)^{\frac{1}{Ct_1}}\right)+\left(\frac{v_x}{R_2}+i_{secmax}\right)\left(\left(\frac{A}{B}\right)^{\frac{1}{Ct_2}}-e^{\frac{-DT_s}{t_2}}\right) \tag{6.12}$$

The magnetizing inductor (L_m) current ripple is

$$\Delta i_{Lm} = \frac{v_{LV} DT_s}{L_m} \tag{6.13}$$

Therefore, p.u. ripple current at LV side, which is a function of duty ratio can be calculated from the ratio $\frac{\Delta i_{in}}{\Delta i_{Lm}}$ for the proposed BDC as shown in Fig. 6.8(d). For conventional single switch BDC with coupled inductor of hybrid structure

$$\Delta i_{in} = \Delta i_{Lm} \tag{6.14}$$

For interleaved structure BDC, the p.u. input current ripple ratio is found approximately [20] as

$$\frac{\Delta i_{in}}{\Delta i_{Lm}} = \frac{1-2D}{1-D} \;\forall D<0.5 \text{ and } \frac{\Delta i_{in}}{\Delta i_{Lm}} = \frac{2D-1}{1-D} \;\forall D>0.5 \tag{6.15}$$

6.5.2. Performance comparison with conventional interleaved structure

This non-ideality as per equation (6.15) of ripple current in interleaved structure is due to

the dead time requirement between two complementary switches. In the proposed BDC OFF time ripple current is not derived as converter in steady state the ON-time ripple is same as OFF time ripple and there is no range of duty as single switch is used unlike interleaved structure. The RIRC operation of the proposed BDC for different duty ratio i.e., D = 0.5, D < 0.5 and D > 0.5 region is shown in Fig. 6.8(a), Fig. 6.8 (b) and Fig. 6.8 (c) respectively. The p.u. input current ripple compared to other methodologies is shown in Fig. 6.8(d). From the theoretical results, it is clear that the input current ripple is almost constant throughout wide duty ratio change unlike interleaved structure. Input current ripple is less in interleaved structure as compared to current proposal in the duty ratio range between D=0.44 to D=0.55. However, in other regions the proposed solution performs better as also shown in Fig. 6.8 (d).

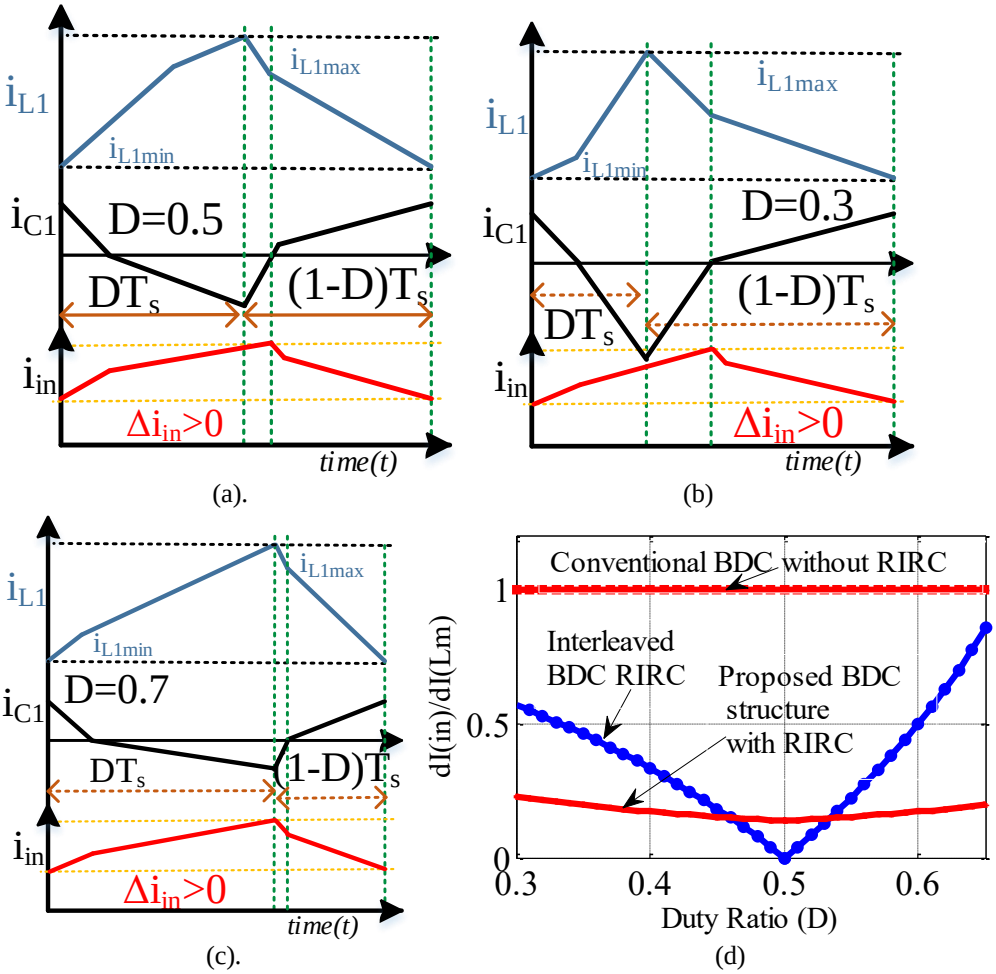


Fig. 6.8. Input current ripple of proposed BDC at (a) D = 0.5 (b) D < 0.5 (c) D > 0.5 and (d) comparison of input current ripple with conventional as well as interleaved BDC.

6.5.3. Operating principle of boost stage

To achieve RIRC and high conversion factor, five MOSFET switches, one diode, coupled inductor and four capacitors are used in designing the proposed BDC. Simplified coupled

inductor modelling with leakage inductance L_{lk} is applied for the steady state analysis. Capacitor voltage ripples are neglected to derive gain factors. Coupling coefficient (k) = $\frac{L_m}{L_m + L_{lk}} \approx 1$ whereas n is winding turns ratio ($N_s = N_T$ & $n = N_s/N_p$). Boost and buck mode of proposed BDC in continuous conduction (CCM) is discussed below. In CCM, the boost operation of BDC is divided into five modes as shown in Fig. 6.9. Circuit diagrams for each operating mode are shown in Fig. 6.11.

Mode 1 [t_0-t_1]: In the beginning (t_0) of this mode, S_4 is switched OFF at ZVS condition as shown in Fig. 6.9. The current flows through D_1 and body diodes of Switch S_4. Switch voltage of S_1 is zero due to body diode conduction. The equivalent circuit of the mode is shown in Fig. 6.11 (a).

Mode 2 [t_1-t_2]: This mode starts with ZVS ON of S_1 at time t_1. The magnetizing current (i_{Lm}) starts rising. Coupled inductor secondary and tertiary winding polarity turned on the body diodes of Switch S_3 and S_5 as shown in Fig. 6.11 (b). It ensures discharge characteristics of capacitor C_4. The loop current equations in this mode are

$$\frac{di_{Lm}}{dt} = \frac{di_{S1}}{dt} = \frac{v_{LV}}{L_m} \tag{6.16}$$

$$\frac{di_{S3}}{dt} = \frac{v_{C2} - v_{C1}}{n^2 L_1} \tag{6.17}$$

$$\frac{di_{S5}}{dt} = \frac{v_{C3} + v_{C1} - v_{C4} - v_{LV}}{n^2 L_1} \tag{6.18}$$

Mode 3 [t_2-t_3]: Similar to previous mode, S_3 and S_5 are turned ON at ZVS condition. The capacitor C_4 continue to discharge and magnetizing current (i_{Lm}) continues rise as shown in Fig. 6.11 (c). By selecting the proper capacitance values of C_1 and C_2 along with coupled inductor secondary winding inductance (L_{sec}) half cycle quasi resonant current ($0.5t_r$) operation is possible during DT_s interval ($DT_s = 0.5t_r$) which makes Switch S_1 current stress lower [36].

Mode 4 [t_3-t_4]: It starts with turn OFF operation of switch S_1, S_3 and S_5. The polarity of leakage inductance naturally makes body diodes of S_2 and S_4 in conduction as shown in Fig. 6.11 (d). This ensures zero voltage of corresponding switches. Leakage inductance energy is transferred to the capacitor C_1. Capacitor C_4 is in now charging through diode D_1. The electrostatic energy stored in capacitor C_2, C_3 and magnetic energy of coupled inductor winding is transferred to HV side. i_{Lm} starts releasing energy at this mode.

Mode 5 [t_4-t_5]: S_2 and S_4 are turned ON at ZVS condition at t_4 where i_{Lm} continues in falling slope. The stored energy of capacitor C_2, C_3 and coupled inductor is transferred to the HV side as shown in Fig. 6.11 (e). Stored leakage inductance energy is fully transferred to C_1 before end of this mode which ensures natural ZCS OFF of S_2. The current equations in this mode are

$$\frac{di_{Lm}}{dt} = \frac{di_{S2}}{dt} = \frac{v_{C1} - v_{LV}}{L_m} \tag{6.19}$$

$$\frac{di_{S4}}{dt} = \frac{v_{HV} - v_{C3} - v_{C1}}{n^2 L_1} \tag{6.20}$$

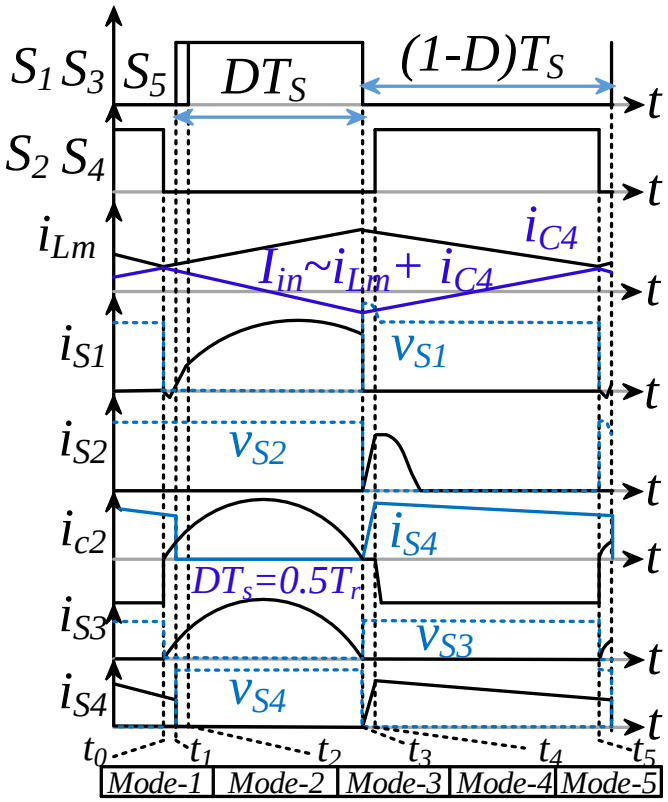


Fig. 6.9. Key waveforms of proposed BDC in boost mode.

6.5.4. Operating principle of buck stage

There are seven sub-modes in buck operation of proposed BDC as shown in Fig. 6.10. The circuit diagrams for each mode are shown in Fig. 6.12. The switching time of one cycle is T_s.

Mode 1 [t_0-t_1]:

Switches S_1, S_3 and S_5 are turned OFF as shown in Fig. 6.12 (a). Body diode of switches S_1, S_5 and S_4 become forward biased due to the winding polarity. It helps to achieve ZVS ON of Switch S_4 at time t_1. ZVS turn OFF operation is also possible for S_1 and S_5 due to body diode conduction.

Mode 2 [t_1-t_2]:

This mode is shown in Fig. 6.12 (b) where Switch S_4 is turned ON under ZVS. The reverse current which is flowing into HV side becomes zero as shown in Fig. 6.12 (b).

Mode 3 [t_2-t_3]:

In this active mode like buck converter, energy is transferred from the HV side to the LV side through capacitor C_3, C_2 and coupled inductor. Inductor polarity helps to turn ON body diode of the Switch S_2 as shown in Fig. 6.12 (c). The loop current equations in this mode are

$$\frac{di_{Lm}}{dt} = \frac{di_{S2}}{dt} = \frac{v_{C1} - v_{LV}}{L_m} \tag{6.21}$$

$$\frac{di_{S4}}{dt} = \frac{v_{HV} - v_{C2} - v_{C3} - v_{C1}}{n^2 L_1} \tag{6.22}$$

As shown in Fig. 6.10, the magnetizing current (i_m) is rising in this mode. But the direction of increment is in negative region which signifies opposite power flow.

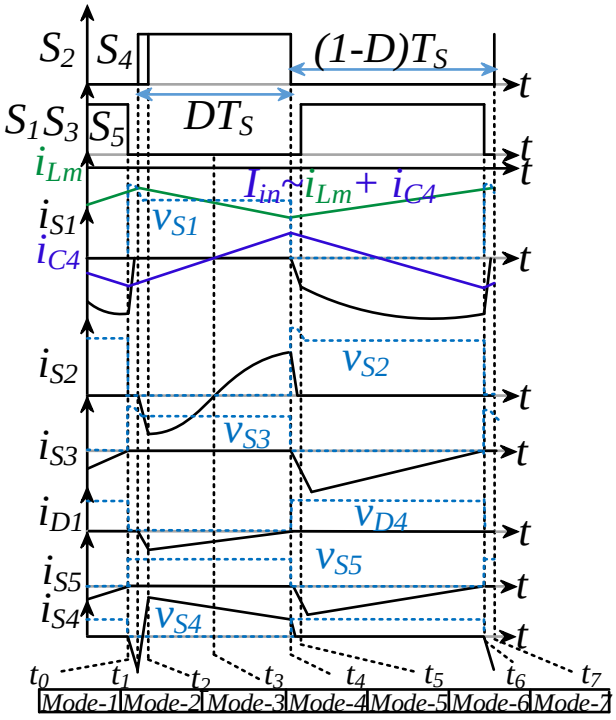


Fig. 6.10. Key waveforms of proposed BDC in boost mode

Capacitor C_1 charges through the body diode of Switch S_2 and C_4 charges through D_1. ZVS ON operation is possible due to the body diode conduction.

Mode 4 [t_3-t_4]:

Mode 3 ensures zero voltage of Switch S_2 which enables ZVS ON operation of S_2 in this mode. This mode stops when C_1 is fully charged. The circuit operation is similar to previous mode as shown in Fig. 6.12 (d).

Mode 5 [t_4-t_5]:

The circuit operation is similar to previous mode as shown in Fig. 6.12 (e). In this mode capacitor C_1 is discharging. The operation of proposed BDC from mode 3 to 5 is like active state of buck converter.

Mode 6 [t_5-t_6]:

In this mode, the main Switch S_4 is turned OFF and the body diode of switches S_1, S_3 and S_5 become forward biased. This mode is same as freewheeling state of the buck converter. Capacitor C_2, C_3 charges and C_1 discharges as shown in Fig. 6.12 (f). I_{Lm} starts falling as inductor is releasing energy. The switch voltages of S_1, S_3 and S_5 are zero as body diodes are in full conduction. This enables possible ZVS turn ON in next mode.

Mode 7 [t_6-t_7]:

In this mode, Switches S_1, S_3 and S_5 are turned ON under ZVS condition. The current paths are similar to Mode 6 as shown in Fig. 6.12 (g).

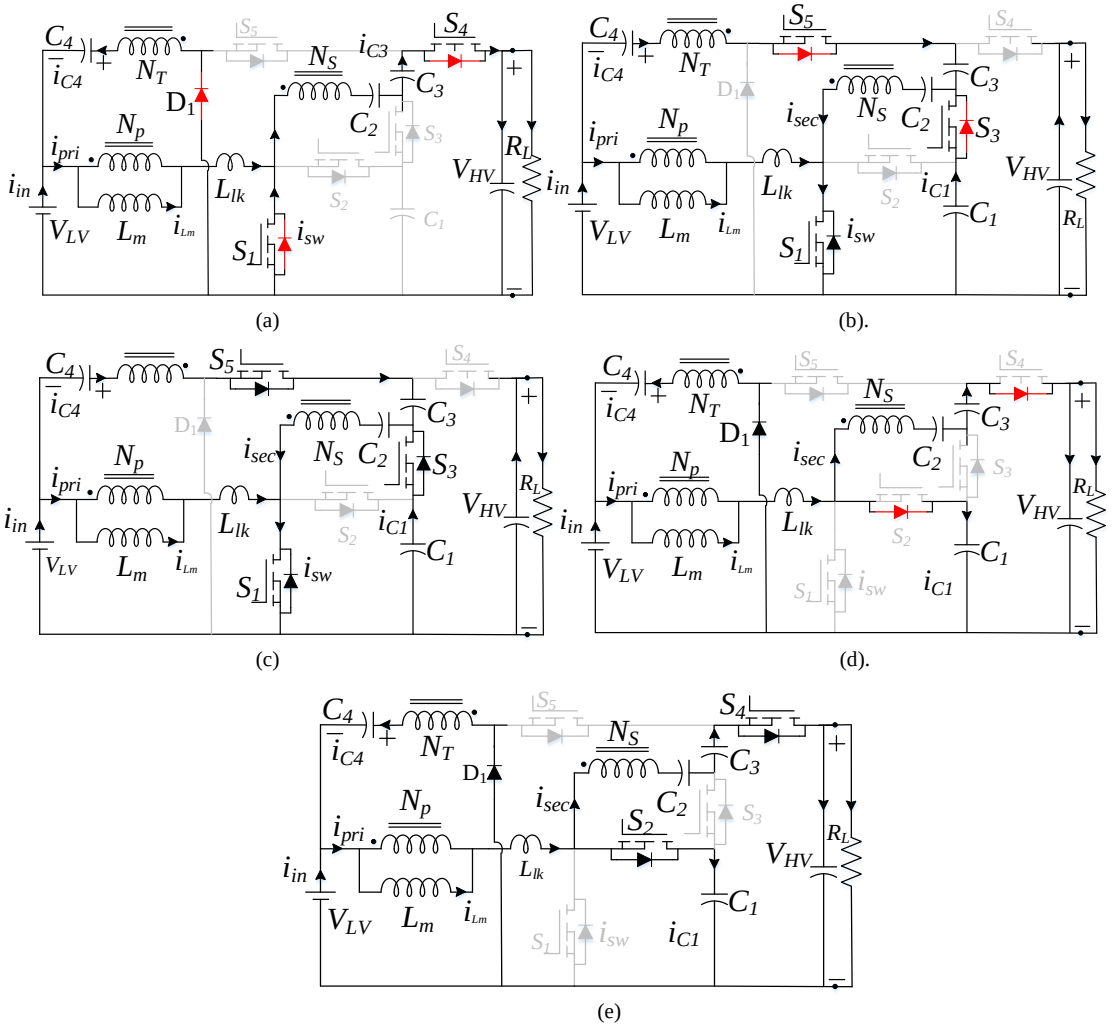


Fig. 6.11. Boost Mode of proposed BDC in CCM: (a) Mode 1 [t_0-t_1] (b) Mode 2 [t_1-t_2] (c) Mode 3 [t_2-t_3] (d) Mode 4 [t_3-t_4] (e) Mode 5 [t_4-t_5].

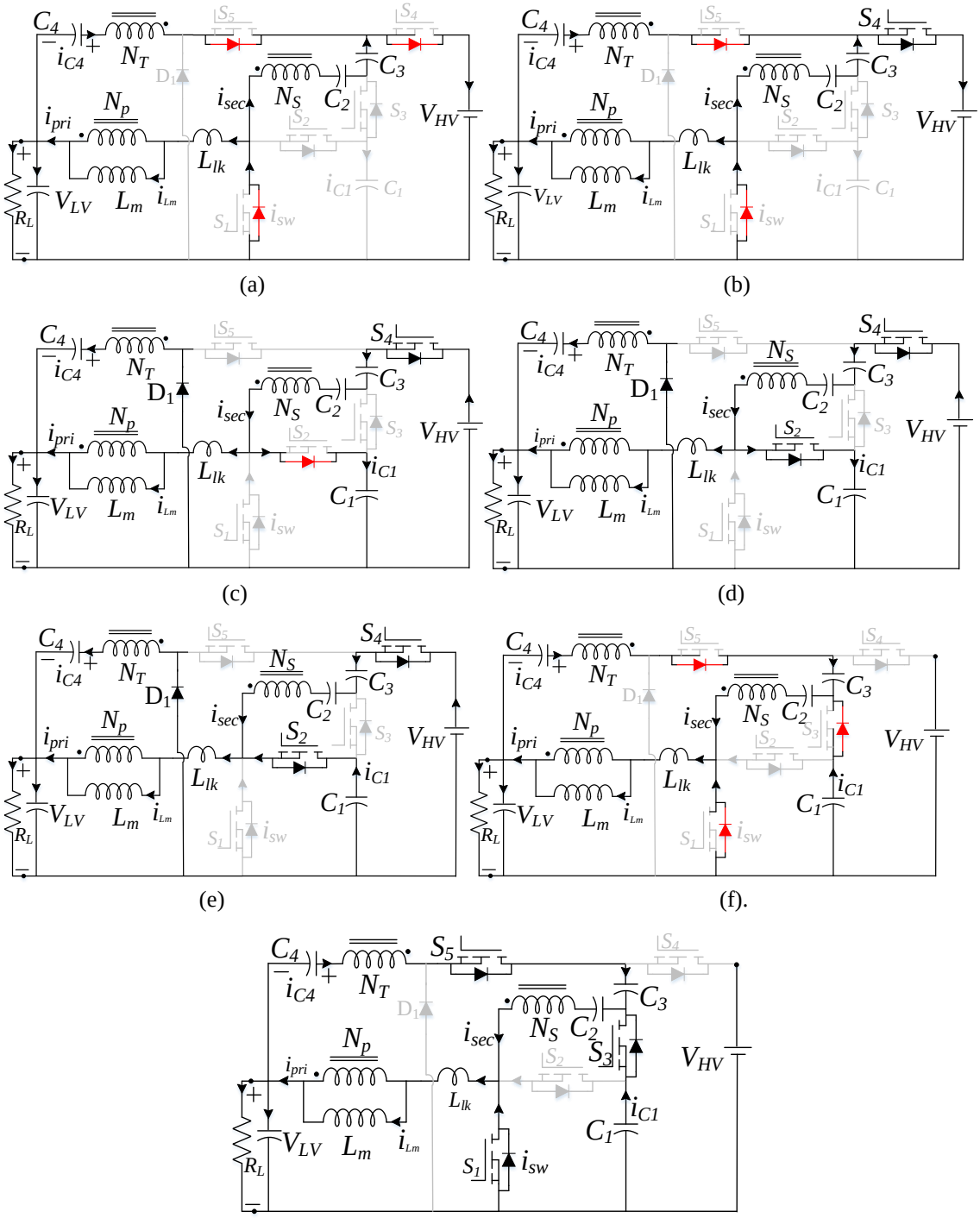


Fig. 6.12. Buck Mode of proposed BDC in CCM: (a) Mode 1 [t_0-t_1] (b) Mode 2 [t_1-t_2] (c) Mode 3 [t_2-t_3] (d) Mode 4 [t_3-t_4] (e) Mode 5 [t_4-t_5] (f) Mode 6 [t_5-t_6] (g) Mode 7 [t_6-t_7].

6.5.5. Voltage gain and boundary condition

A. Boost Mode Voltage Gain:

The voltage gain of the proposed BDC to achieve RIRC operation can be derived from volt sec balance equation of coupled inductor primary (V_{Lm}), secondary (V_{Lsec}) and tertiary windings (V_{LT}). The active boost state of BDC is shown in Fig. 6.11 (c). Leakage inductance voltage is denoted by V_{Lk}. These voltages are related to input low voltage

through coupling coefficient (*k*). In this article for simplicity in analysis *k=1* is considered. Therefore $V_{Lm}=V_{Lv}$, $V_{Lk}=0$, $V_{Lsec}=V_{LT}=nV_{Lv}$. C_1 and C_4 voltages can be derived from volt sec balance from secondary and tertiary winding voltage loop.

$$v_{C_1}=\frac{v_{LV}}{1\text{-}D} \text{ and } v_{C_4}=\frac{D(n+1)}{1\text{-}D}v_{LV} \tag{6.23}$$

Similarly, using volt-sec balance, capacitor C_2, C_3 and output voltage can be derived.

$$v_{C_2}=\left(n+\frac{v_{LV}}{1\text{-}D}\right) v_{C_3}=\frac{nv_{LV}}{(1\text{-}D)} \tag{6.24}$$

The voltage gain in boost mode including effect of coefficient of coupling (k) is

$$v_{HV}=v_o=\left(\frac{2nk+4D(k\text{-}1)+2(2\text{-}k)v_{LV}}{1\text{-}D}\right)v_{LV} \tag{6.25}$$

The voltage gain (6.25) variation for different coupling coefficient is shown in Fig. 6.13.

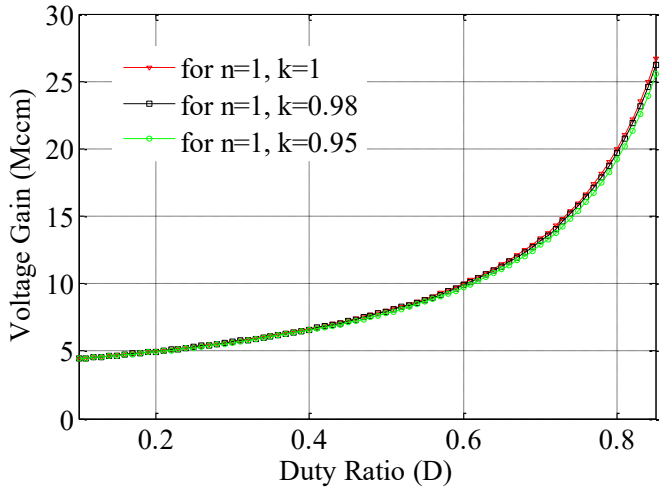


Fig. 6.13. Static voltage gain in boost mode for different coupling coefficient.

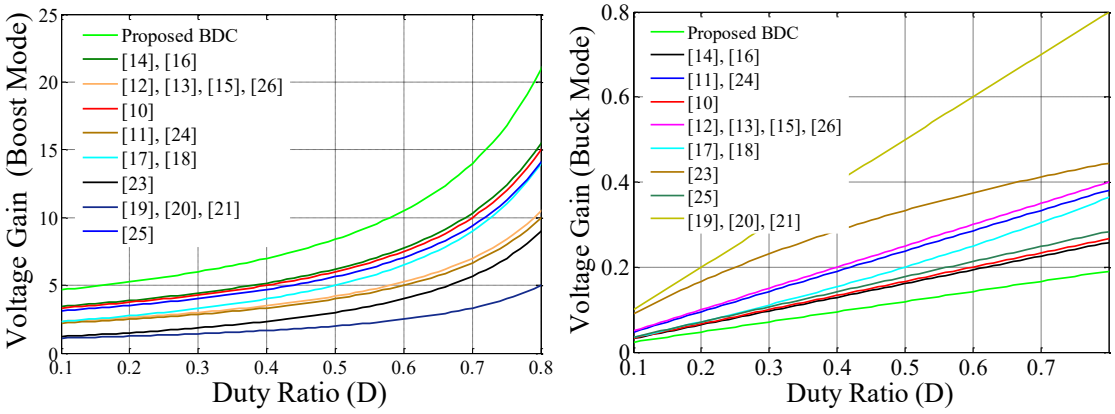
The output voltage can also be derived and boosting factor in CCM is

$$v_{HV}=v_0=\frac{2n+2}{1\text{-}D}v_{LV} \qquad M_{CCM}=\frac{v_{HV}}{v_{LV}}=\frac{2n+2}{1\text{-}D} \tag{6.26}$$

The comparison of voltage gain factor (M_{CCM}) during boosting mode for *n=1* is shown in Fig. 6.14 (a). The boundary conduction mode condition is also derived from CCM and DCM voltage gain and output capacitor charge balance equation in terms of normalized time constant.

From the boundary condition critical conduction mode is derived in terms of normalized time constant (τ_{Lmb}) which is.

$$\tau_{Lmb}=\frac{(1-D)^2 D}{2(n+1)^2} \tag{6.27}$$



(a). (b)

Fig. 6.14. Voltage gain comparison for *k*=1 and *n*=1 in (a) boost (b) buck mode.

$$\frac{L_m}{R_L T_s} = \tau_{Lm} > \tau_{Lmb} \tag{6.28}$$

B. Buck Mode Voltage Gain:

Applying similar approach, the voltage gain in buck mode operation of the proposed BDC is derived. For coupling coefficient *k = 1* the capacitor voltage equations are.

$$v_{C_1} = \frac{v_{LV}}{D} \qquad v_{C_4} = \left(\frac{(n+1)(1\text{-}D)}{D}\right) v_{LV} \tag{6.29}$$

Voltage gain in buck mode is.

$$M_{CCM} = \frac{v_{LV}}{v_{HV}} = \frac{D}{2n+2} \tag{6.30}$$

Comparative result of buck stage gain at *k*=1 between current proposal and existing solutions is shown in Fig. 6.14 (b).

C. Voltage stress, current stress and comparison

The steady state voltage stress of main Switches (S_1, S_4) and auxiliary Switches (S_2, S_3, S_5) are important for selecting correct voltage rating of MOSFET. Voltage stress (V_{sw}) of main switches i.e., S_1 and S_4 of proposed BDC are,

$$v_{S1} = \frac{v_{LV}}{1\text{-}D} = \frac{v_{HV}}{2n+2} \text{ and } v_{S4} = \frac{v_{HV}}{2} \tag{6.31}$$

Similarly, auxiliary switch voltage stress for S_2, S_3, and S_5 are respectively

$$v_{S2} = \frac{v_{HV}}{2n+2},\ v_{S3} = \frac{v_{HV}}{2} \text{ and } v_{S5} = \frac{2n+1}{2n+2} v_{HV} \tag{6.32}$$

The normalized voltage stress for HV (S_4) and LV (S_1) switch is compared with other topologies as shown in Table-6.1. Voltage stress is comparatively less than other solutions found in literature. This enables to select low rating MOSFET switches which has lower

ON state resistance.

Table 6.1
Switch Voltage Stress Comparison Of Main Switch

	Proposed	[12], [13], [15, [26]]	[14], [16],	[10]	[17], [18]	[11]	[19], [20], [21]
HV Side (S_4)	$\frac{v_{HV}}{2n+2}$	$\frac{n}{n+1}v_{HV}$	$\frac{v_{HV}}{n+2}$	$\frac{v_{HV}}{3}$	$\frac{v_{HV}}{2+D}$	$\frac{v_{HV}}{2}$	v_{HV}
LV Side (S_1)	$\frac{v_{HV}}{2n+2}$	$\frac{v_{HV}}{n+1}$	$\frac{v_{HV}}{n+2}$	$\frac{v_{HV}}{3}$	$\frac{v_{HV}}{3-D}$	$\frac{v_{HV}}{2}$	$\frac{v_{HV}}{1-D}$

D. Switch Current Stress:

The average, RMS and peak current of Switches $S_{1\text{-}5}$ is derived from the operating principle of proposed BDC as shown in Fig. 6.11 and Fig. 6.12 for both the operating modes. The low voltage side input average current (I_{in}) is derived from power equivalence of input to output. The tertiary winding branch capacitor C_4 average current is zero from charge balance. Similarly, the magnetizing current (i_{Lm}) is derived from charge balance of high voltage side capacitor.

$$i_{Lm} = \frac{v_{HV}[(n+1)]}{(1\text{-}D)R_L} \tag{6.33}$$

The magnetizing current (i_{Lm}) ripple value is

$$\Delta i_{Lm} = \frac{v_{LV} D T_s}{2L_m} \tag{6.34}$$

By proper selection of capacitor values of C_1 and C_2, main switch current (S_1) peak value can be reduced by maintaining half cycle resonating time equal to switch ON time as mentioned in [36]. The peak value of Switch S_1 is

$$i_{S1\_Peak} = i_{in\_Peak} + i_{winding2\_Peak} \tag{6.35}$$

$$i_{S1\_Peak} \cong \frac{2v_{HV}(n+1)}{(1\text{-}D)R_L} + \frac{v_{LV}}{1-D}\sqrt{\frac{C_{eq}}{L_2}} \tag{6.36}$$

Similarly, the peak current for high voltage side Switch S_4 is

$$i_{S4\_Peak} = \frac{2v_{HV}(n+1)}{n(1\text{-}D)R_L} + \frac{v_{HV} D(1\text{-}D)T_s}{4n(n+1)L_m} \tag{6.37}$$

The peak switch currents of S_2 and S_3 are respectively,

$$i_{S2\_Peak} = i_{Lm\_Peak} \quad \text{and} \quad i_{S3\_Peak} \cong \frac{v_{LV}}{1-D}\sqrt{\frac{C_{eq}}{L_2}} \tag{6.38}$$

From the operating waveform as shown in Fig. 6.9 the RMS values of S_1 to S_5 is derived.

$$i_{\text{S1-RMS}} \approx \frac{2+n+\text{D}}{(2+2n)\sqrt{\text{D}}} i_{\text{LV}} \text{ and } i_{\text{S3-RMS}} \approx \frac{v_{\text{LV}}}{2(1-\text{D})} \sqrt{\frac{\text{C}_{eq}}{\text{L}_2}} \tag{6.39}$$

$$i_{\text{S2-RMS}} = \frac{2(1+n)}{1-D} \sqrt{\text{D}_\text{b}} i_{\text{HV}} \quad \text{and } i_{\text{S5-RMS}} = \sqrt{\frac{1}{\text{T}_\text{s}} \int_0^{\text{DT}_\text{s}} \left(\text{v}_{ceq} \sqrt{\frac{\text{C}_{\text{eq1}}}{\text{L}_{\text{eq1}}}} \sin \frac{2\pi}{\text{T}_\text{s}} \text{t} \right)^2 dt} \tag{6.40}$$

$$i_{S4-\text{RMS}} \approx i_{\text{Lm-min}} \sqrt{(1-\text{D})} \tag{6.41}$$

Where, $\text{D}_\text{b} = \frac{v_{\text{c1}}\text{D}}{4\pi \text{i}_{\text{HV}}} \sqrt{\frac{\text{C}_{\text{eq}}}{\text{L}_2}} \left(1\text{-}\cos\left(2\pi\text{D}\right)\right) \times \left(\frac{1\text{-D}}{n+1}\right)$

Similarly, current equations for buck mode are derived. The RMS values of switch currents are essential to calculate theoretical conduction loss of the proposed BDC. The RIRC operation and main Switch S_1 (LV side) current stress is compared to other topologies as mentioned in Table-6.2.

6.5.6. LV side input current ripple comparison

The low voltage side current ripple comparison is mentioned in Table-6.2. Due to topological advantages the current ripple performance is constant throughout all duty ratio operation.

6.5.7. Theoretical loss calculation

The RMS values of switch currents can be calculated in both the buck and boost mode of CIBDC which is explained in previous section. These RMS current values are essential for calculating theoretical conduction loss of active switches. Thus, total conduction loss in buck mode is

$$\text{P}_{\text{Cu-buck}} = \sum_{i=1}^{5} i_{\text{i}_{\text{RMS\_Buck}}}^2 R_{\text{i}_{\text{DS-ON}}} \tag{6.42}$$

Similarly, total conduction loss for boost mode is,

$$\text{P}_{\text{Cu-boost}} = \sum_{i=1}^{6} i_{\text{i}_{\text{RMS\_Boost}}}^2 R_{\text{i}_{\text{DS-ON}}} \tag{6.43}$$

Parasitic resistance value of coupled inductor windings and capacitor create extra ESR conduction loss in both the operating modes. The ESR loss of boost mode is

$$\text{P}_{\text{ESR-boost}} = i_{\text{i}_{\text{RMS\_pri}}}^2 R_{\text{ESR}} + i_{\text{i}_{\text{RMS\_winding2}}}^2 R_{\text{ESR}} + i_{\text{i}_{\text{RMS\_winding3}}}^2 R_{\text{ESR}} + \sum_{i=1}^{4} i_{C_{\text{i\_RMS}}}^2 R_{\text{i}_{\text{ESR}}} \tag{6.44}$$

Similarly, the ESR loss in buck mode is

$$P_{ESR\text{-}buck} = i^2_{i_{RMS\_pri}} R_{ESR} + i^2_{i_{RMS\_winding2}} R_{ESR} + i^2_{i_{RMS\_winding3}} R_{ESR} + \sum_{i=1}^{4} i^2_{C_{i\_RMS}} R_{i_{ESR}} \quad (6.45)$$

Due to soft switching operation of all active switches, the switching loss is neglected in both the operating modes. Ferrite core is used for designing the coupled inductor and core losses are derived from the data sheet, loss density curve [47] with respect to flux density change for a given frequency. Based on the converter operation the change in the flux density is

$$\Delta B = \frac{v_{HV} D(1\text{-}D)}{2A_c N_1 f_{sw} (n+1)} \quad (6.46)$$

Where, primary side turns ratio is N_1, core area is A_c. Thus, core loss can be easily theoretically derived as

$$P_{core} = \left[W/cm^3 \right] \times Volume \quad (6.47)$$

Therefore, considering all losses of CIBDC, the efficiency (6.48) is derived for both operating modes.

$$\eta = \frac{P_0}{P_0 + P_{cu\_buck/boost} + P_{core} + P_{ESR\_buck/boost}} \quad (6.48)$$

6.5.8. Parameter design and soft switching condition

Coupled inductor number of turns (n) is derived from voltage gain equation of boost mode of BDC which is

$$n \geq \frac{v_{HV}(1\text{-}D) - 2v_{LV}}{2v_{LV}} \quad (6.49)$$

The magnetizing inductance is derived from the normalized time constant at boundary as mentioned in equation 6.50. Therefore, to ensure the CCM operation in proposed BDC

$$\frac{L_m}{R_L T_s} = \tau_{Lm} > \tau_{Lmb} \quad (6.50)$$

$$L_m \geq \frac{R_L D(1\text{-}D)^2}{2f_{sw}(n+1)^2} \quad (6.51)$$

High voltage side capacitance (C_{HV}) is derived from change in capacitor charge based on change in capacitor ripple voltage (ΔV).

TABLE 6.2
COMPARISON OF LV SIDE MAIN SWITCH CURRENT STRESS AND INPUT CURRENT RIPPLE AT BOOST MODE@200W

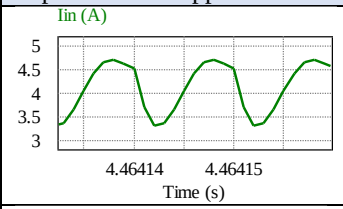
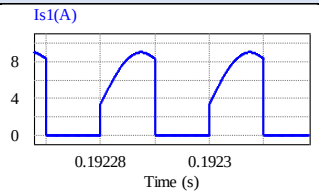
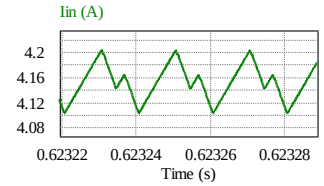
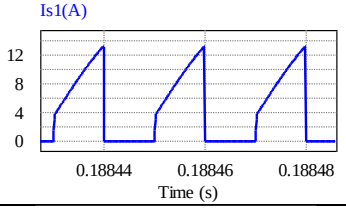
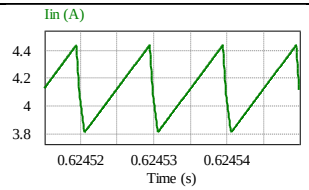
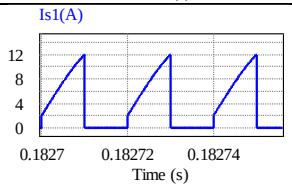
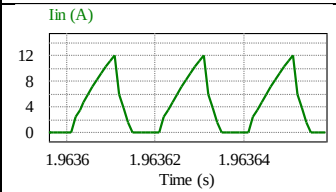
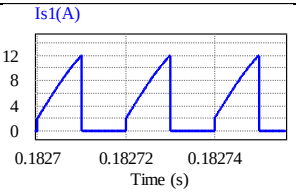
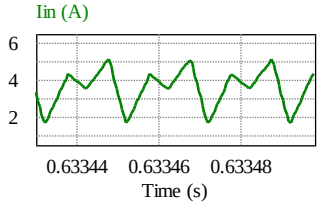
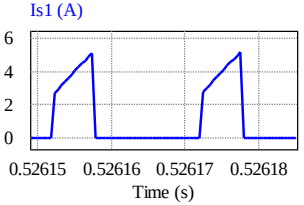
Topology	Input Current Ripple Waveform	Switch RMS Current	Main Switch Current Waveform	Peak Switch Current	RIRC
Proposed		$i_{S1\text{-}RMS} \approx \frac{2+n+D}{(2+2n)\sqrt{D}} i_{LV}$		$\cong \frac{2v_{HV}(n+1)}{(1\text{-}D)R_L} + \frac{v_{LV}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}$	**YES** [Better than Interleaved]
[25]		$= i_{LV}\sqrt{D\left(1+\frac{\Delta I_L}{I_{Lmin}}\left(1+\frac{1}{3}\frac{\Delta I_L}{I_{Lmin}}\right)\right)}$		$= \frac{v_{LV}(n+2)^2}{n^2(1\text{-}D)^2R_L} + \frac{v_{LV}DT_s}{2L_1}$	YES [Interleaved Structure]
[26]		$\cong I_{LV}\sqrt{D} + \frac{v_{LV}DT_s}{L_m}\sqrt{\frac{D}{3}}$		$\cong \frac{v_{LV}(n+1)^2}{(1\text{-}D)^2R_L} + \frac{v_{LV}DT_s}{L_m}.$	YES [Interleaved Structure]
[14]		$i_{S1\text{-}RMS} = \frac{1+n+D}{(2+n)\sqrt{D}} i_{LV}$		$\cong \frac{v_{LV}(n+1)(2+n)}{(1\text{-}D)^2R_L} + \frac{v_{LV}}{1-D}\sqrt{\frac{C_{eq}}{L_2}}$.	NO
[21]		$= i_{LV}\sqrt{D\left(1+\frac{\Delta I_L}{I_{Lmin}}\left(1+\frac{1}{3}\frac{\Delta I_L}{I_{Lmin}}\right)\right)}$		$= \frac{v_{LV}D}{(1\text{-}D)^2R_L} + \frac{v_{LV}DT_s}{L_i}$	YES [Interleaved Structure] D=0.4

TABLE-6.3
COMPARATIVE ANALYSIS OF DIFFERENT NON-ISOLATED BDC

Topology	No of Passive Components	No of Switches and Diodes	Power Flow	Suitable for 350-400 Volt interface with 48 volts	Voltage Gain		Power Level	Measured Efficiency		RIRC
					Boost	Buck		Boost	Buck	
Proposed	Coupled Inductor -1 Capacitors-6	Switch-5 Diodes-1	Bidirectional	Yes, and less no of winding turn (n=1)	$\frac{2n+2}{1-D}$	$\frac{D}{2n+2}$	250W	95.5%	94.6%	**YES** [Better than Interleaved]
[25]	Inductor -2 Coupled Inductor-1 Capacitors-5	Switch-8	Bidirectional	Yes (for n>2)	$\frac{n+2}{n(1-D)}$	$\frac{nD}{n+2}$	1kW	96%	96%	YES [Interleaved Structure]
[26]	Coupled Inductor -2 Capacitors-4	Switch-8	Bidirectional	Yes (for n>2)	$\frac{n+1}{1-D}$	$\frac{D}{n+1}$	1kW	94%	94%	YES [Interleaved Structure]
[14]	Coupled Inductor -1 Capacitors-4	Switch-4	Bidirectional	Yes, and less no of winding turn (n=2)	$\frac{n+2}{1-D}$	$\frac{D}{n+2}$	300W	95% .	94.1%	NO
[21]	Inductor -3 Capacitors-3	Switch-4	Bidirectional	Not suitable (Insufficient Gain)	$\frac{1}{1-D}$	D	200W	96.1%	95%	YES [Interleaved Structure]
[31]	Inductor -2 Capacitors-6	Switch-6	Bidirectional	Yes	$\frac{4}{1-D}$	$\frac{D}{4}$	480W	94.3%	95%	YES [Interleaved Structure]
[32]	Coupled Inductor -1 Capacitors-5	Switch-5	Bidirectional	Yes	$\frac{n+1}{1-D}+n$	$\frac{D}{n+1+nD}$	200W	96%	93%	No
[34]	Coupled Inductor -2 Capacitors-5 (circuit-3,	Switch-4	Bidirectional	Yes	$\frac{2n+2}{1-D}$	$\frac{D}{2n+2}$	400W	95.6%	95.9%	YES [Interleaved Structure]

	I/O-2)									
[35]	Inductor -2 Capacitors-6	Switch-6	Bidirectional	Yes	$\frac{4}{1-D}$	$\frac{D}{4}$	2kW	97%	96%	YES [Interleaved Structure]
[17]	Inductor -2 Capacitors-7	Switch-5	Bidirectional	Yes	$\frac{D+2}{1-D}$	$\frac{D}{3-D}$	400W	90%	92%	NO
[10]	Inductor -3 Capacitors-6	Switch-8	Bidirectional	Yes	$\frac{3}{1-D}$	$\frac{D}{3}$	800W	93.5%	93%	NO
[12]	Inductor -1 Coupled Inductor-1 Capacitors-5	Switch-4	Bidirectional	Yes	$\frac{n+1}{1-D}$	$\frac{D}{n+1}$	400W	95%	94%	NO
[13]	Coupled Inductor -1 Capacitors-4	Switch-4	Bidirectional	Yes	$\frac{n+1}{1-D}$	$\frac{D}{n+1}$	300W	94%	94.5%	NO
[15]	Coupled Inductor -1 Capacitors-5	Switch-4	Bidirectional	Yes	$\frac{n+1}{1-D}$	$\frac{D}{n+1}$	500W	96%	96%	NO

$$C_{HV} \geq \frac{i_{HV}D}{f_{sw}\Delta v_{HV}} \tag{6.52}$$

Low voltage side capacitance is designed from buck operation using capacitor charge and voltage ripple.

$$C_{LV} \geq \frac{v_{HV}(1\text{-}D)}{16(n+1)L_m f_{sw}^2 \Delta v_{LV}} \tag{6.53}$$

Similarly, the values of the intermediate capacitor C_1, C_2, C_3 and C_4 are derived based on the ripple voltage and charge.

$$C_1 \geq \frac{i_{LV}D}{nf_{sw}\Delta v_{C1}} \text{ and } C_2 \geq \frac{2i_{LV}D}{nf_{sw}\Delta v_{C2}} \tag{6.54}$$

$$C_3 \geq \frac{i_{LV}D}{2(n+1)f_{sw}\Delta v_{C3}} \text{ and } C_4 \geq \frac{i_{LV}D}{(n+1)f_{sw}\Delta v_{C4}} \tag{6.55}$$

6.5.9. Results and Discussion

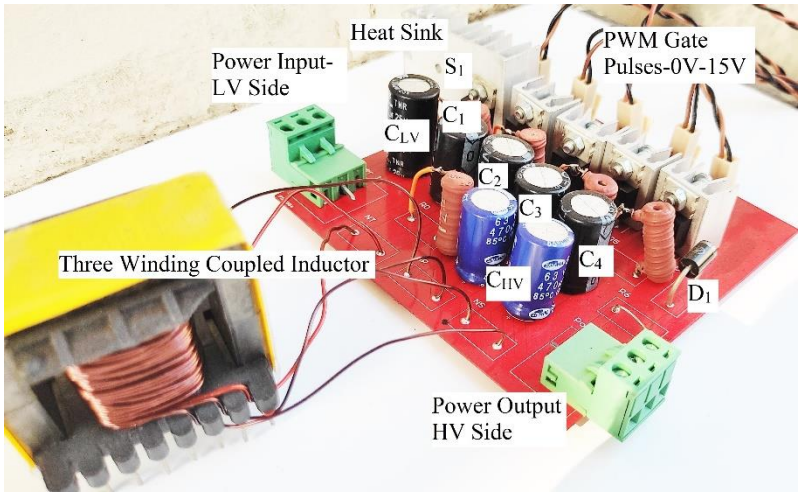
The simulation study of proposed BDC is performed using PSIM 9.1.1. A scaled down 250 W prototype converter is designed as shown in Fig. 6.15 (a) to test the steady and transient state performance in real time microgrid energy storage interface. Performances like input current ripple in LV side is measured to validate the theoretical findings. Other steady state performances like soft switching of all active switches for both operating modes are also tested. The switching frequency is 50 kHz of the proposed converter. The designed parameters for the prototype are mentioned in Table-6.4.

TABLE-6.4
HARDWARE PARAMETERS

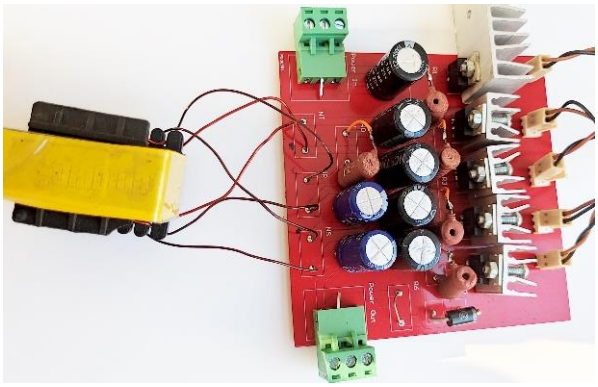
Converter Specification		
V_{LV} = 48 V	V_{HV} = 380V	P_o = 250W
	f_{sw}=50 kHz	
Design Parameters	**Value**	**Part Number**
Coupled Inductor	L_m = 44 µH, Turns Ratio 25:25 (n = 1), $L_{leakage}$ = 8.26 µH	Ferrite Core PQ 32/30
Switch (S_1, S_2, S_3, S_5)	FQP34N20 (V_{ds} = 200 V, R_{ds} = 0.075 Ω I_d=31 A.)	FQP34N20
Diodes (D_1)	FRD	IN5401
Switch (S_4)	FQP17N40 (V_{ds} = 400 V, R_{ds} = 0.27 Ω, I_d=16 A.)	FQP17N40
Capacitor C_1-C_4	10µF	
C_{HV}	220µF	
C_{LV}	100µF	

Overall control system is implemented using NI-cRIO 9082 FPGA interface. The voltage sensor module i.e. NI-9225 is used to sense HV side voltage from common DC bus link.

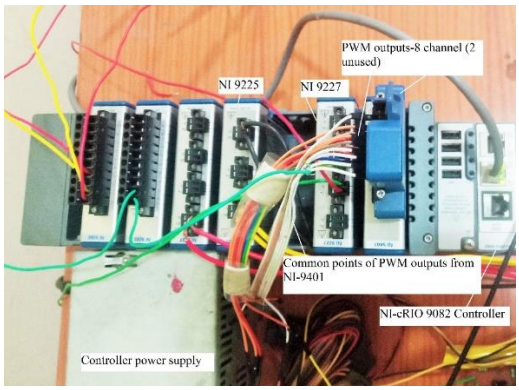
Digital PWM signals for S_1 to S_5 is generated using D/IO module NI-9401 as shown in Fig. 6.15(c). For isolation stage optocoupler (6N137) is used from NI-cRIO 9082 controller to MOSFET driver i.e. IR2110. The total system for hardware for verification is shown in Fig. 6.15 (a), Fig. 6.15 (b) and Fig. 6.15(f).



(a)



(b).



(c)

Fig. 6.15. 250W BDC converter with RIRC operation (a) Power Circuit (b) Top view of Power Circuit (c) LabVIEW based NI-cRIO 9082 Controller.

The input current from LV side is summation of capacitor current (i_{c4}) and coupled inductor primary current (I_{pri}). For duty ratio D = 0.5 and D = 0.3, the two branch currents are measured as shown in Fig. 6.16 (a) and Fig. 6.16 (b) respectively. The LV side input current ripple for D=0.5 and D=0.3 is measured without using any LV side filter capacitor to show performance improvement of ripple current using proposed technique as shown in Fig. 6.16 (c) and Fig. 6.16 (d). These two branch currents are controlled through one main switch (S_1) and possess opposite slopes during ON time as well as OFF time. These opposite slope characteristics helps to reduce the input current ripple similar to the interleaved structure, but with only one main switch. The current proposal provides minimum input ripple current throughout the duty ratio range unlike interleaved structure as discussed in section-6.4.

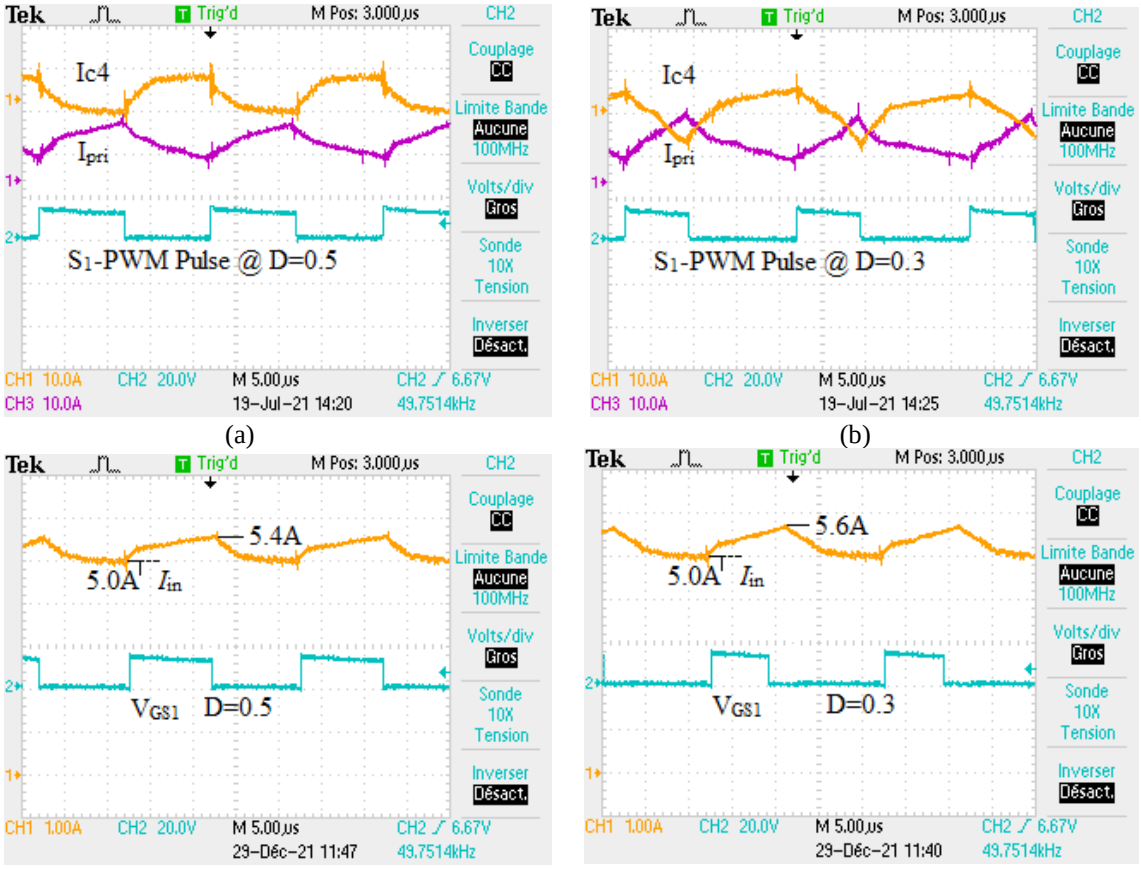


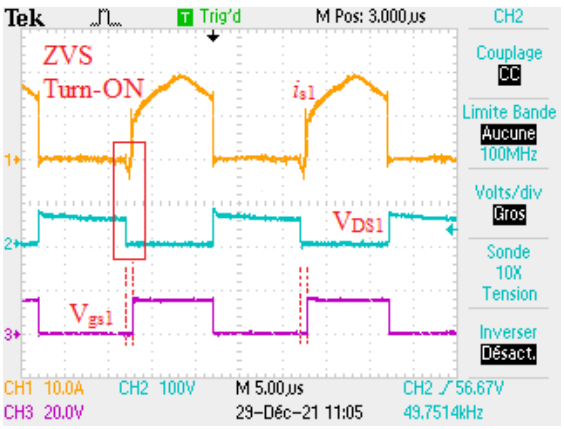
Fig. 6.16. Two individual loop currents i.e. i_{c4} and I_{pri} at LV side for (a) D = 0.5, (b) D = 0.3 and input ripple current without C_{LV} for (c) D=0.5 (d) D=0.3.

Comparative study is performed for different duty ratios to verify the input current ripple performance of different topologies, i.e. (a) interleaved based (b) without interleaved based structure and (c) proposed technique. The RIRC performance is mentioned in Table-6.5.

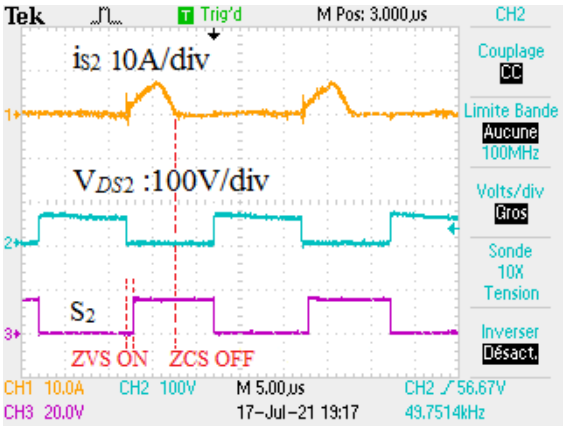
TABLE-6.5
Comparison of RIRC between interleaved and proposed method

Interleaved	Ripple Current and RIRC	Voltage gain
For D = 0.5	Ripple=0, RIRC=Yes	Do not help in improving voltage gain
For D=0.3	Ripple=0.44p.u. RIRC=No	Do not help in improving voltage gain
For D=0.6.	Ripple=0.51 p.u. RIRC=No	Do not help in improving voltage gain
Current Proposal ($DT_s=t_r$, & $DT_s<t_r$) [29]	Ripple Current Reduction (RIRC)	Voltage gain
For D = 0.5	Ripple=0.17 p.u. RIRC=Yes	Helps in increasing voltage gain
For D = 0.3	Ripple=0.27 p.u. RIRC=Yes	Helps in improving voltage gain
Other BDCs	Ripple Current and RIRC	Voltage gain
0.1<D<0.9	Same as inductor ripple current, RIRC=NO	Helps in improving voltage gain

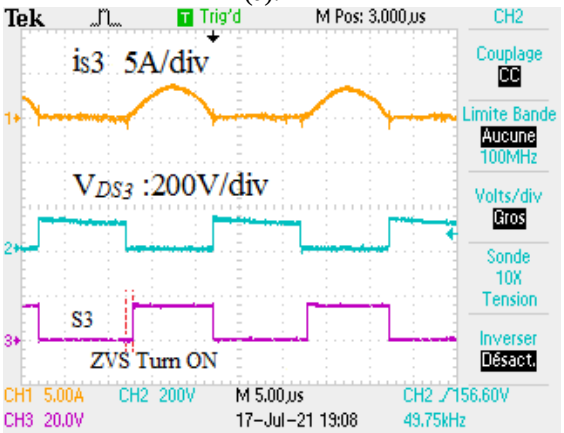
Interleaved structure provides very good RIRC operation and ideally zero input ripple current at D = 0.5. However, for other duty ratios especially D < 0.44 and D > 0.55, the RIRC operation is not maintained. The interleaved structure performance better compared to conventional BDCs, where no current sharing at LV side is reported. The input current ripple is same as of the inductor or magnetizing inductance ripple content in the conventional BDCs, which forces to choose a large inductor size compared to its interleaved counterpart. Current BDC performs well in terms of RIRC for wide duty ratio range. Another benefit of the current proposal is achievement of similar characteristics as of the interleaved structure using reduced switch count. Additionally, the current proposal not only reduces the current ripple but also helps to improve the voltage gain unlike interleaved structure. As described in the previous section, the soft switching of all active switches is also important to achieve higher efficiency operation from the proposed converter



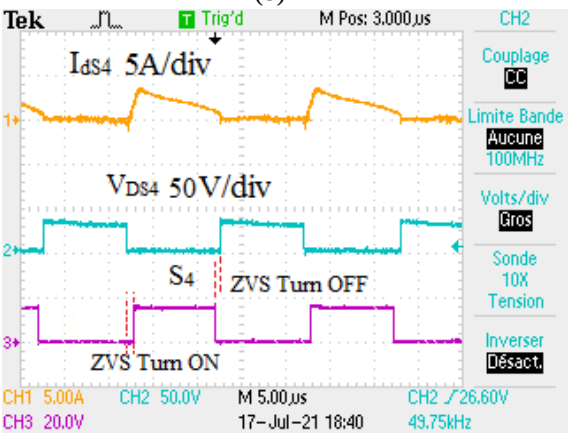
(a).



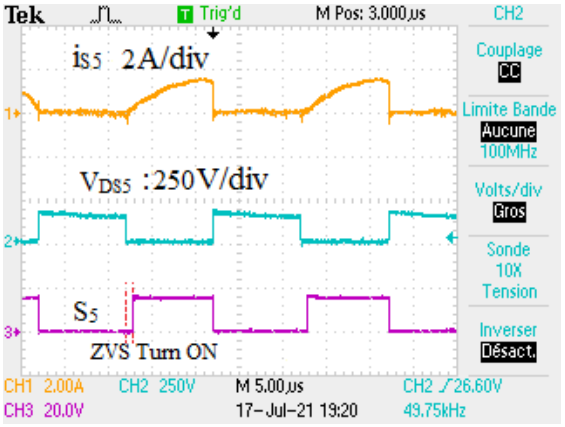
(b)



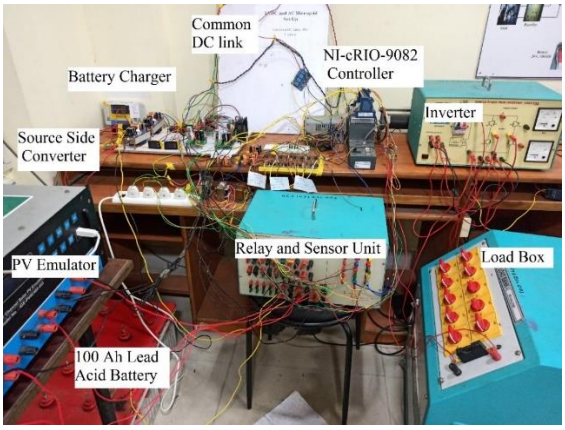
(c).



(d)



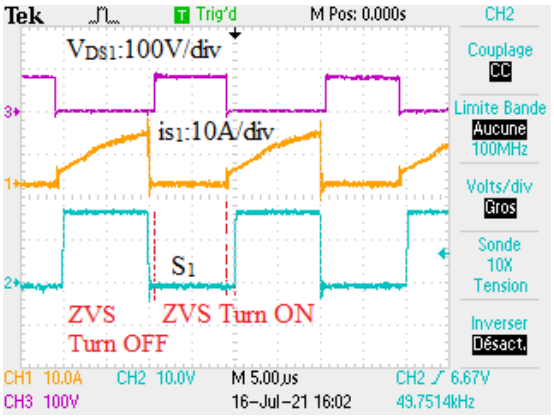
(e).



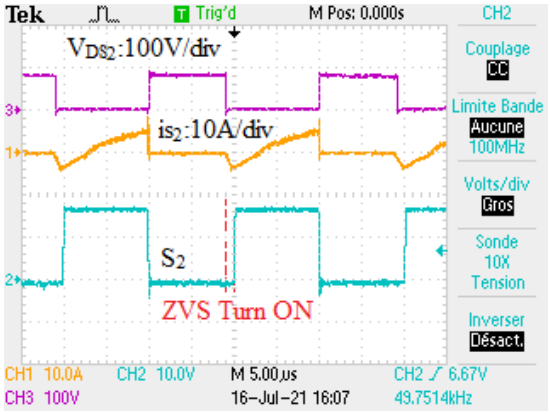
(f)

Fig. 6.17. Soft switching, i.e. ZVS operation of S_1 to S_5 of the proposed BDC in boost mode (a-e), (f) 1kW DC microgrid test bed.

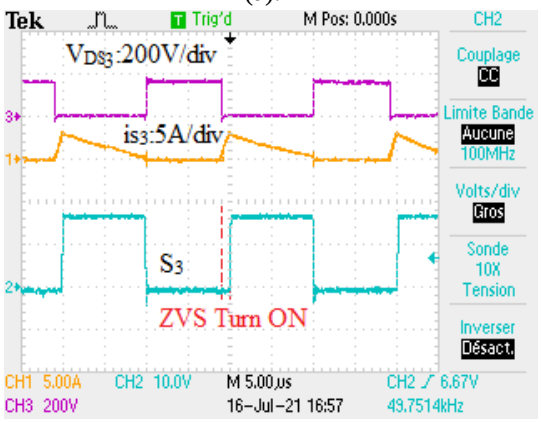
Using inherent synchronous rectification operation ZVS is achieved for switches S_1 to S_5 in both buck as well as boost modes. The soft switching operation of the switches used in proposed BDC are shown in Fig. 6.17. Similarly, during buck mode of operation, the soft switching performance is also tested as mentioned in Fig. 6.18.



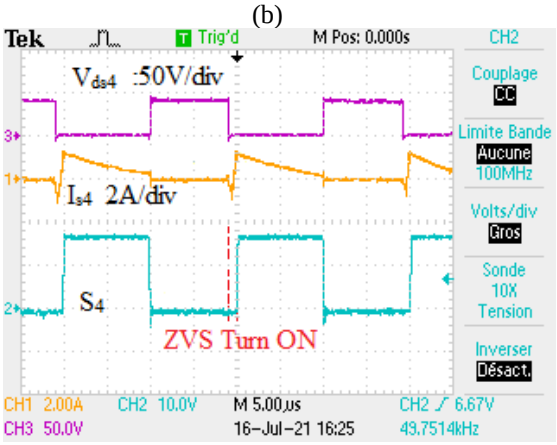
(a).



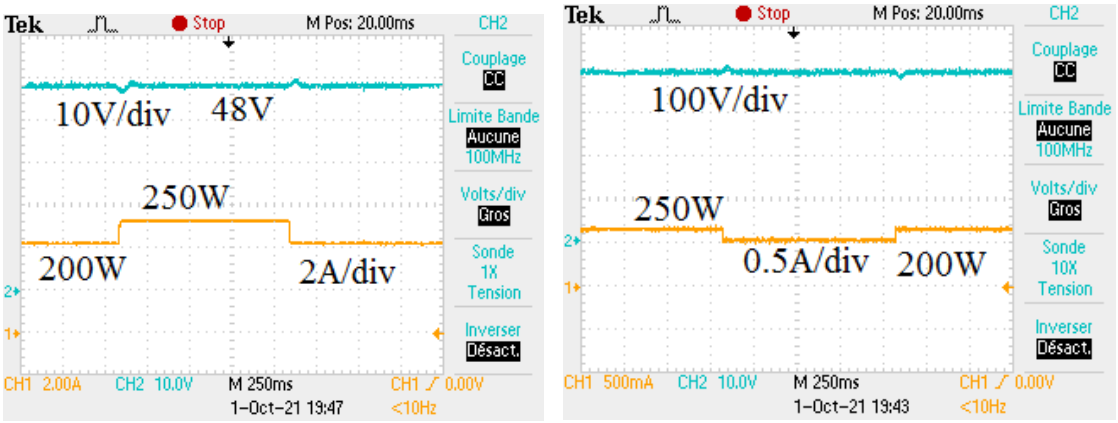
(b)



(c)



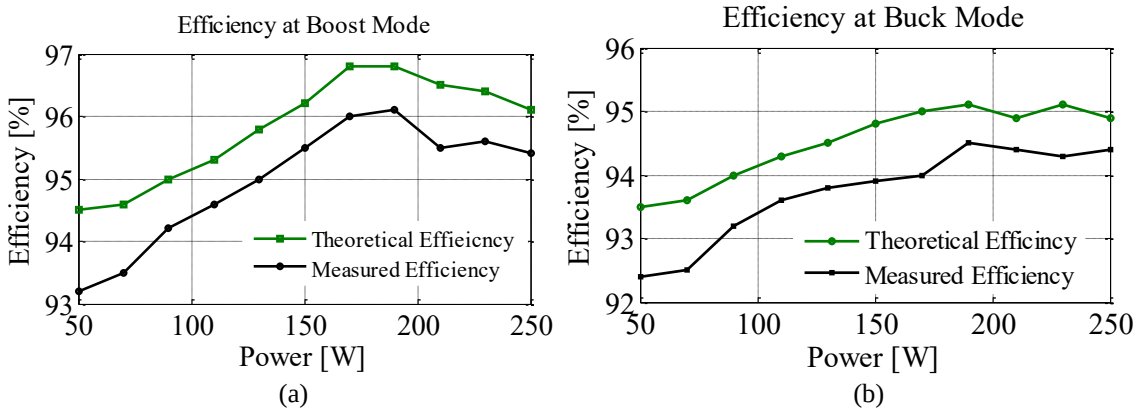
(d)



(e) (f)

Fig. 6.18. Soft switching i.e., ZVS operation of S_1 to S_5 of the proposed BDC (a)-(d) in buck mode and response during load change from (d) 200W-250W-200W in buck mode, (e) 250W-200W-250W in boost mode.

Small signal average model [37] is adopted for controller design for proposed BDC and output voltage is stable during load change as shown in Fig. 6.18 (e) & Fig. 6.18(f). From all theoretical average and RMS currents of winding, switches, and capacitors different loss components are determined theoretically to determine the efficiency at different loading points in buck as well as boost mode. The proposed BDC structure utilized single turn (n = 1) compared to other solutions where (n > 2) is generally used. Thus, the core and copper loss in the coupled inductor are less compared to other proposals [14], [25-26], [12]. Winding currents during charging as well as discharging are also less as parallel paths are formed. The practical efficiency is measured using a power quality analyzer APLAB-PQA2100E. The theoretical and practical efficiency for both operating modes is shown in Fig. 6.19. The theoretical efficiency is higher as ideal current waveforms are considered for calculating loss. The Skin effect and other parasitic effects of loss are neglected while calculating the converter losses under different loading conditions.



(a) (b)

Fig. 6.19. Efficiency determination of the proposed BDC at different loading: (a) boost mode, and (b) buck mode at V_{LV}=48V.

Current BDC has lesser current stress at main switches i.e., 15-20% less peak current value and has less input ripple current for wider duty ratio range compared to other alternatives like interleaved based BDC [25-26] and conventional high voltage lift BDCs [14,], [12], [13] etc. A detailed comparison with other proposal is mentioned in Table-6.3. The loss distribution of proposed BDC in boost and buck mode at 250W are shown in Fig. 6.20 and Fig. 6.21 respectively.

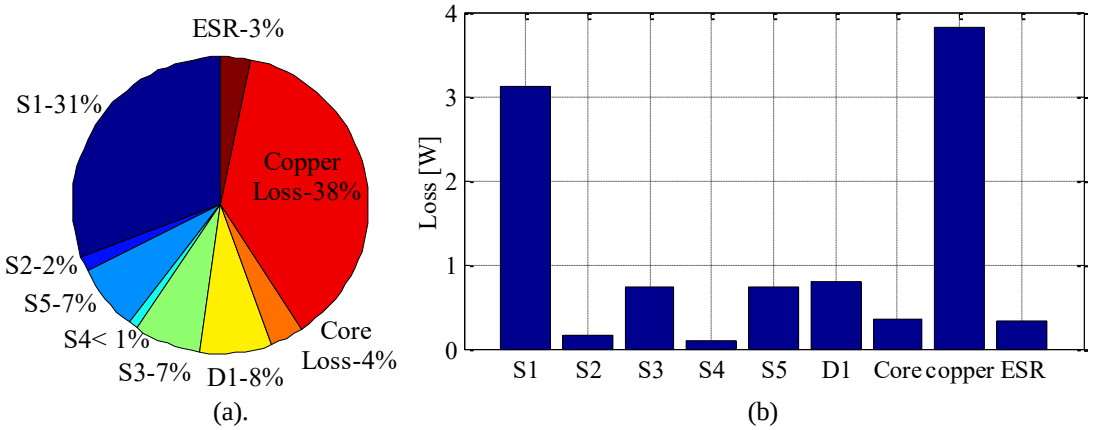


Fig. 6.20. Loss distribution of proposed BDC in boost mode (a) % share of loss (b) individual component wise loss.

The loss in coupled inductor is more due to coil resistance and higher loss in diode D_1 limits further efficiency improvement of proposed BDC in both the operating modes.

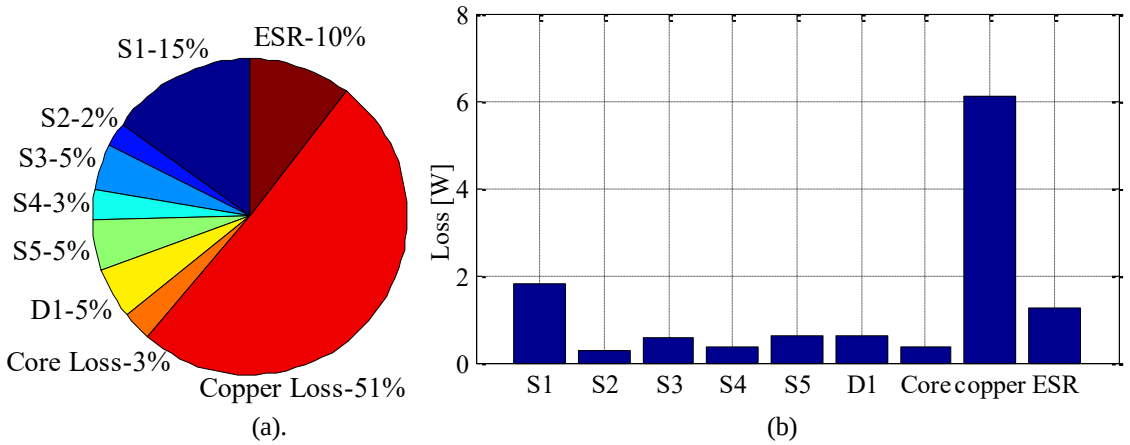


Fig. 6.21. Loss distribution of proposed BDC in buck mode (a) % share of loss (b) individual component wise loss.

6.6. Summary

In this chapter, a new circuit is proposed to reduce the LV side input current ripple, attain high voltage gain, better current sharing and RIRC operation. The circuit has potential to replace high gain network to design interleaved structure-based dc-dc converter. The current proposal reduces the number of switches and provide parallel paths for the current at LV side to achieve high conversion gain and efficiency to makes it suitable for 48V to

400V system. The proposed BDC has 15-20% less peak current at main switches and uniform low input current ripple over a wider duty ratio variation compared to the interleaved structure. The LV side input ripple current in interleaved structure is 0.44 p.u. for D=0.3; whereas 0.27 p.u. in the presented concept for same duty ratio. This means up to 17% reduction of the ripple current is possible. All the active switches in the proposed BDC topology are soft switched utilizing synchronous rectification, which guarantees reduction in the switching loss and helps to achieve higher efficiency. The coupled inductor winding core loss as well as copper loss are also reduced due to smaller number of turns (n=1 in the proposed case) compared to [14], [25-26]. The measured peak efficiency of proposed BDC is 96% in the boost mode and 94.5% in the buck mode of operation. For wider load range, the average efficiency is above 94% for all operating modes which makes it suitable for integrating storage interface for microgrid.

6.7. Publications and References

Publications

S. B. Santra, D. Chatterjee, Y. P. Siwakoti, "Coupled Inductor Based Soft Switched High Gain Bidirectional DC-DC Converter with Reduced Input Current Ripple", **IEEE Transactions on Industrial Electronics**, Vol. 70, no. 2, pp. 1431-1443, Feb-2023**.**

References

[1] F. Blaabjerg, 'Control of Power Electronic Converters and Systems', vol. 2. San Francisco, CA, USA: Academic, 2018.

[2] Hui Li, Fang Zheng Peng and J. S. Lawler, "A natural ZVS medium-power bidirectional DC-DC converter with minimum number of devices," in *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 525-535, March-April 2003.

[3] K. Wang, C. Y. Lin, L. Zhu, D. Qu, F. C. Lee and J. S. Lai, "Bi-directional DC to DC converters for fuel cell systems," *Power Electronics in Transportation* (Cat. No.98TH8349), 1998, pp. 47-51, doi: 10.1109/PET.1998.731056.

[4] F. Z. Peng and Fan Zhang, "A Novel compact DC/DC converter for 42 V systems," *Power Electronics in Transportation*, 2002, 2002, pp. 143-148, doi: 10.1109/PET.2002.1185562.

[5] D. Aggeler, J. Biela, S. Inoue, H. Akagi, J.W. Kolar, "Bi-directional isolated dc-dc converter for next-generation power distribution-comparison of converters using Si and SiC devices," in *Proceedings of Power Conversion Conference*, pp. 510-517, 2007.

[6] T. Mishima, H. Mizutani, and M. Nakaoka, "A sensitivity-improved PFM LLC resonant full-bridge DC–DC converter with LC antiresonant circuitry," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 310-324, Jan. 2017.

[7] J.-B. Lee, K.-B. Park, J.-K. Kim, H.-S. Youn, and G.-W. Moon, "A new center-tapped half-bridge zeta converter with small transformer dc-offset current and low voltage stress," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6593-6603, Dec. 2015.

[8] T.-F. Wu, J.-G. Yang, C.-L. Kuo, and Y.-C. Wu, "Soft-switching bidirectional isolated full-bridge converter with active and passive snubbers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1368-1376, March 2014.

[9] H. Ardi, A. Ajami, F. Kardan, and S. N. Avilagh, "Analysis and implementation of a nonisolated bidirectional DC–DC converter with high voltage gain," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4878-4888, Aug. 2016.

[10] Y. Zhang, W. Zhang, F. Gao, S. Gao and D. J. Rogers, "A Switched-Capacitor Interleaved Bidirectional Converter With Wide Voltage-Gain Range for Super Capacitors in EVs," in *IEEE Trans. on Power Electron.*, vol. 35, no. 2, pp. 1536-1547, Feb. 2020.

[11] Y. Zhang, Y. Gao, L. Zhou and M. Sumner, "A Switched-Capacitor Bidirectional DC–DC Converter With Wide Voltage Gain Range for Electric Vehicles With Hybrid Energy Sources," in *IEEE Trans. on Power Electron.*, vol. 33, no. 11, pp. 9459-9469, Nov. 2018.

[12] J. Yao, A. Abramovitz and K. Ma Smedley, "Steep-Gain Bidirectional Converter With a Regenerative Snubber," in *IEEE Trans. on Power Electron.*, vol. 30, no. 12, pp. 6845-6856, Dec. 2015.

[13] S. M. P., M. Das and V. Agarwal, "Design and Development of a Novel High Voltage Gain, High-Efficiency Bidirectional DC–DC Converter for Storage Interface," in *IEEE Trans. on Ind. Electron.*, vol. 66, no. 6, pp. 4490-4501, June 2019.

[14] W. Hassan, J. L. Soon, D. D. Lu and W. Xiao, "A High Conversion Ratio and High-Efficiency Bidirectional DC-DC Converter with Reduced Voltage Stress," in *IEEE Trans. on Power Electron.*,Vol. 35, no. 11, pp. 11827-11842, Nov.2020.

[15] H. Wu, K. Sun, L. Chen, L. Zhu, Y. Xing, “High Step-Up/Step-Down Soft-Switching Bidirectional DC-DC Converter with Coupled-Inductor and Voltage Matching Control for Energy Storage Systems”, *IEEE Trans. on ind. Electron.*, vol. 63, no. 5, pp. 2892-2903, May 2016.

[16] Y. Zhang, H. Liu, J. Li and M. Sumner, "A Low-Current Ripple and Wide Voltage-Gain Range Bidirectional DC–DC Converter With Coupled Inductor," in *IEEE Trans. on Power Electron.*, vol. 35, no. 2, pp. 1525-1535, Feb. 2020.

[17] Y. Zhang, Q. Liu, Y. Gao, J. Li and M. Sumner, "Hybrid Switched-Capacitor/Switched-Quasi-Z-Source Bidirectional DC–DC Converter With a Wide Voltage Gain Range for Hybrid Energy Sources EVs," in *IEEE Trans. on Ind. Electron.*, vol. 66, no. 4, pp. 2680-2690, April 2019.

[18] Z. Wang, P. Wang, B. Li, X. Ma and P. Wang, "A Bidirectional DC–DC Converter With High Voltage Conversion Ratio and Zero Ripple Current for Battery Energy Storage System," in *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 8012-8027, July 2021.

[19] C. A. Soriano-Rangel, J. C. Rosas-Caro and F. Mancilla-David, "An Optimized Switching Strategy for a Ripple-Canceling Boost Converter," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4226-4230, July 2015.

[20] N. Nupur and S. Nath, "Maximizing Ripple Cancellation in Input Current for SIDO Boost Converter by Design of Coupled Inductors," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, 2021 (early access).

[21] P. Prabhakaran and V. Agarwal, "Novel Boost-SEPIC Type Interleaved DC–DC Converter for Mitigation of Voltage Imbalance in a Low-Voltage Bipolar DC Microgrid," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 8, pp. 6494-6504, Aug. 2020.

[22] M. Packnezhad and H. Farzanehfard, "Soft-Switching High Step-Up/Down Converter Using Coupled Inductors With Minimum Number of Components," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 7938-7945, Sept. 2021.

[23] Q. Li et al., "An Improved Floating Interleaved Boost Converter With the Zero-Ripple Input Current for Fuel Cell Applications," in *IEEE Transactions on Energy Conversion*, vol. 34, no. 4, pp. 2168-2179, Dec. 2019.

[24] C. A. Villarreal-Hernandez, O. F. Ruiz-Martinez, J. C. Mayo-Maldonado, G. Escobar, J. E. Valdez-Resendiz and J. C. Rosas-Caro, "Minimum Current Ripple Point Tracking Control for Interleaved Dual Switched-Inductor DC–DC Converters," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 1, pp. 175-185, Jan. 2021.

[25] Z. Yan, J. Zeng, W. Lin and J. Liu, "A Novel Interleaved Nonisolated Bidirectional DC–DC Converter With High Voltage-Gain and Full-Range ZVS," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7191-7203, July 2020.

[26] R. Hu, J. Zeng, Z. Yu, Z. Yan and J. Liu, "Secondary Side Cascaded Winding-Coupled Bidirectional Converter With Wide ZVS Range and High Conversion Gain," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 1444-1454, April 2021.

[27] Chen, S.-J.; Yang, S.-P.; Huang, C.-M.; Chen, Y.-H. Interleaved High Step-Up DC–DC Converter with Voltage-Lift and Voltage-Stack Techniques for Photovoltaic Systems. *Energies* 2020, 13, 2537. https://doi.org/10.3390/en13102537.

[28] M. Packnezhad and H. Farzanehfard, "Fully Soft Switched Interleaved High Step-Up/Down Bidirectional Converter With No Pulsating Current at Low Voltage Source," in *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2021.3120484. 2021 (early access).

[29] P. Mohseni, S. Rahimpour, M. Dezhbord, M. R. Islam and K. M. Muttaqi, "An Optimal Structure for High Step-Up Non-Isolated DC-DC Converters with Soft-Switching Capability and Zero Input Current Ripple," in *IEEE Transactions on Industrial Electronics*, 2021 (early access).

[30] Li, Wuhua; Xu, Chi; Yu, Hongbing; Gu, Yunjie; He, Xiangning: 'Analysis, design and implementation of isolated bidirectional converter with winding-cross-coupled inductors for high step-up and high step-down conversion system', *IET Power Electronics*, Vol. 7, no. 1, pp. 67-77, Feb. 2014.

[31] N. Molavi, M. Esteki, E. Adib and H. Farzanehfard, "High step-up/down DC-DC bidirectional converter with low switch voltage stress," *The 6th Power Electronics, Drive Systems & Technologies Conference* (PEDSTC2015), 2015, pp. 162-167.

[32] Y. Hsieh, J. Chen, L. Yang, C. Wu and W. Liu, "High-Conversion-Ratio Bidirectional DC–DC Converter With Coupled Inductor," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 210-222, Jan. 2014, doi: 10.1109/TIE.2013.2244541.

[33] M. J. Schutten, R. L. Steigerwald and J. A. Sabate, "Ripple current cancellation circuit," *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2003. APEC '03., 2003, pp. 464-470 vol.1, doi: 10.1109/APEC.2003.1179254.

[34] M. R. Mohammadi, A. Amoorezaei, S. A. Khajehoddin and K. Moez, "A High Step-Up/Step-Down LVS-Parallel HVS-Series ZVS Bidirectional Converter With Coupled Inductors," in *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1945-1961, Feb. 2022, doi: 10.1109/TPEL.2021.3106668.

[35] H. Moradisizkoohi, N. Elsayad, and O. Mohammed, “A voltage quadrupler interleaved bidirectional DC-DC converter with intrinsic equal current sharing characteristic for electric vehicles,” *IEEE Trans. Ind. Electron*., vol. 68, no. 2, pp. 1803–1813, Feb. 2021.

[36] S. B. Santra, D. Chatterjee, Y. P. Siwakoti and F. Blaabjerg, "Generalized Switch Current Stress Reduction Technique for Coupled- Inductor based Single Switch High Step-Up Boost Converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no.2 pp. 1863-1875, April 2021.

[37] R.W. Erickson and D. Maksimovic, “Fundamentals of Power Electronics”, 3rd edition. Springer, USA, Aug. 2020.

Chapter-7

Selection Methods of Passive Components in BDC connected to LVDC Microgrid

The application of BDC converter connected to microgrid is very important. As per the discussion, the BDC should operate instantaneously during any power mismatch between sources to load. The mismatch problem is critical when source is PV panel due to its intermittent power generation. Therefore, for maintaining constant DC link voltage is necessary for stable microgrid operation and it is a major challenge. The BDC should operate instantaneously, but power converter cannot alone make the system fast and reliable. The system components are also source of delay during transition event. The large delay make system unstable even though BDC's are highly efficient and fast acting. Therefore, proper selection of system components especially passive components like capacitor, inductor is very critical. In this chapter the passive components selection procedure for BDC connected microgrid is discussed in details.

7. Selection Methods of Passive Components in BDC connected to LVDC Microgrid

7.1. Introduction

In the previous consecutive chapters, the high efficiency, high voltage gain and low stress BDC converter with less current ripple is discussed. In this chapter the application of BDC in microgrid is discussed for reliable operation. The general structure of BDC connected to microgrid is shown in Fig.7.1.

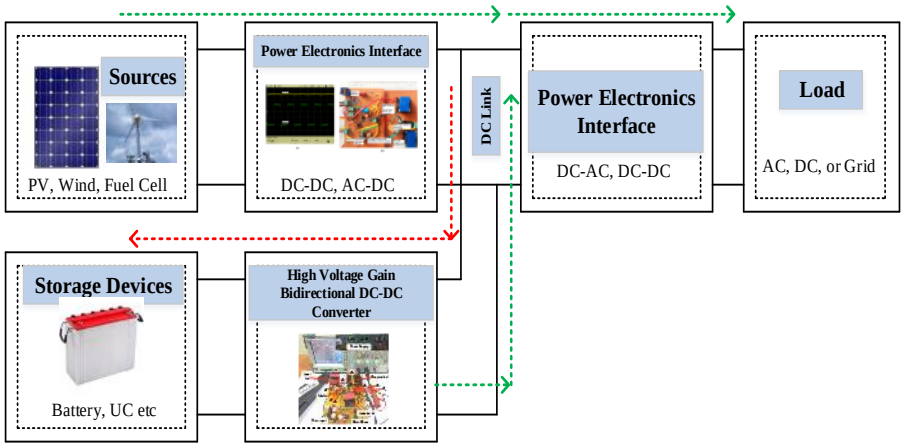


Fig. 7.1. BDC connected to microgrid.

The application of BDC converter connected to microgrid is very important. As per the discussion the BDC should operate instantaneously during any power mismatch between sources to load. The mismatch problem is critical when source is PV panel due to its intermittent power generation. Therefore, for maintaining constant DC link voltage is necessary for stable microgrid operation and it is a major challenge. The BDC should operate instantaneously, but power converter cannot alone make the system fast and reliable. The system components are also source of delay during transition event. The large delay makes system unstable even though BDC's are highly efficient and fast acting. Therefore, proper selection of system components especially passive components like capacitor, inductor are very critical. In this chapter the passive components selection procedure for BDC connected microgrid is discussed in details.

7.2. Proposed Capacitor Selection for PV Interfaced Converter

Power electronics converters (PEC) are interfaced in the configurations of photovoltaic (PV) power generation system [1]. Generally, a capacitor is connected between the PV panel and power converter to filter voltage ripple and current ripple so that ripple content will not affect the PV panel [1]. There are three regions of operation of PV sources i.e.,

constant current region, constant voltage region, and constant power region [2]. Constant power region is the required mode of operation for extracting maximum power from the PV panel. Different MPPT algorithms [2] are found in the literature to ensure PV operation in the constant power region. In the static or slow environmental change conditions PV panel voltage and current do not change much and therefore these MPPT algorithms can operate accurately. The selection of capacitance is not important in a static condition. However, these algorithms perform inaccurately under dynamic environmental conditions [3] as they rely on the voltage and current sensing information. PV panel voltage changes with irradiation `variation operated in MPP condition as shown in Fig. 7.2.

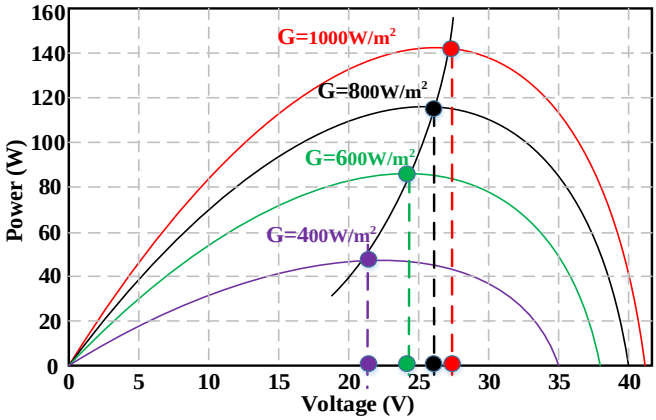


Fig. 7.2. PV voltage change at MPP with irradiation (G) variation.

The capacitor voltage does not change immediately with irradiation variation due to circuit time constant. Again, the sensing and processing delay of the algorithm takes additional time. These delays in PV system should be as small as possible for tracking error-free MPP operation. Several advanced control techniques [4-5] are proposed by researchers to track reference power changes accurately with irradiation and temperature variation. There are two approaches i.e., using (a) advanced control technique (b) low capacitance value to optimize settling time [6], found in the literature to extract maximum power from PV under rapidly changing environmental conditions. Different adaptive control techniques like FPPT as proposed by H.D. Tafti *et.al*. [7] using modern digital signal processor (DSP) confirms good MPP operation under sudden irradiation change. Again, multi-mode FPPT is proposed by H.D. Tafti *et.al*. [8], where small adjustment in voltage is processed in controller to achieve fast dynamics. For multi-string structure under inhomogeneous irradiation, maximum power point tracking error is nullified by time-sharing MPPT [9] technique. This problem is also addressed by S. Selvakumar *et.al*. [10], where the fast determination of global maximum power point (GMOP) is achieved in conjunction with a boost converter.

However, capacitor selection-based solution to minimize settling time for error-free point tracking is not yet explored which is simple and cost-effective. Capacitor selection based on PV micro inverter [11-13] does not concentrate on the impact of capacitance for MPP operation. Lowering the perturbation period compared to system settling time can improve MPPT performance but it increases steady-state oscillation. The correct capacitance value between the PV panel and PEC with accurate perturbation time can eliminate error in MPPT performance in varying conditions. In this chapter initially impact of PV panel parameter and capacitance value on MPPT is discussed including ripple power effect. Finally, the capacitance value is selected for the minimization of settling time which allows low perturbation frequency operation and error-free MPPT on dynamic environmental conditions. This also guides the inductor value selection to avoid oscillations in DC link voltage.

7.3.1. System Configuration and Dynamics

Boost converter is selected as PV interfaced PEC for analyzing and testing the effects of output capacitance (C_f) on MPPT. The configuration is shown in Fig. 7.3. Simple perturbation-based technique (P & O) is considered to extract MPP from PV panel in this work because it is simple and effective [1], [14].

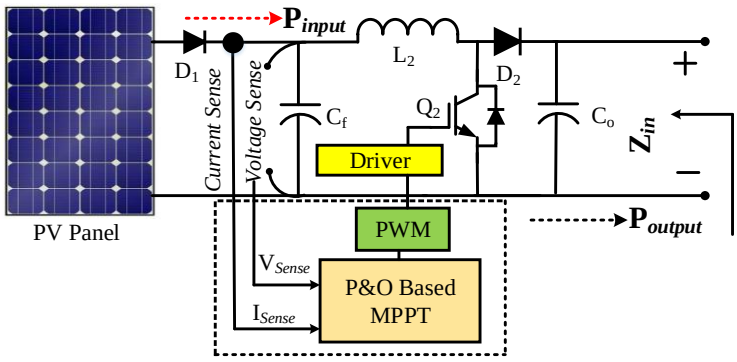


Fig. 7.3. PV system with boost converter.

Sensed voltage and current signal from a solar PV panel is essential for duty ratio determination of boost converter to extract maximum power. When irradiation changes at loaded condition, the capacitor (C_f) voltage, i.e., the PV panel voltage, should change to a new value as per Fig. 7.2 immediately. However, the circuit time constant introduced by the capacitor between the PV panel and the boost converter, C_f, restricts the immediate voltage change as shown in Fig. 7.4. This time delay is considered as source side time constant delay in this work. This delay together with the time required to sense the capacitor (C_f) voltage V_f, PV current and the processing time create an additional delay. Therefore,

the total time delay considered while analyzing the performance of maximum power point extraction under irradiation change is the combination of source-side time constant delay and sensing-processing delay.

The quantity P_{K1} in Fig. 7.4 represents the reference power from PV and P_{Ka1} is the actual power after implementing the MPPT algorithm. Slow rate irradiation change with minimum delay ensures constant power region or MPPT operation and considered as ideal case as shown in Fig. 7.4.

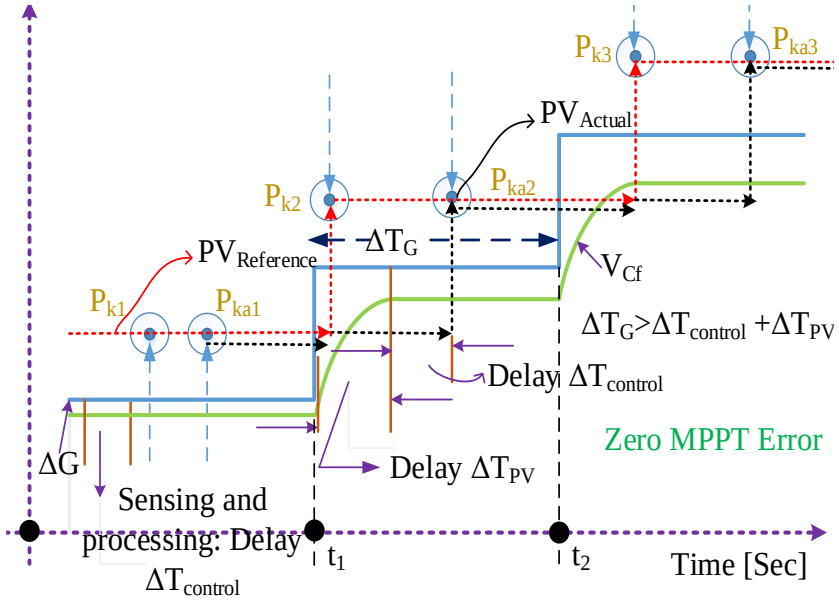


Fig. 7.4. Ideal MPPT dynamics with zero error under irradiation change, where ΔG is change in irradiation, ΔTpv is time delay due to PV time constant.

A high value of C_f is practically recommended to decoupling the power from the DC side to the AC side and minimize the voltage ripple [10]. However, a large capacitance value increases the source side time constant so that the voltage change is not instantaneous after an irradiation change. Thus, change in control signal (voltage and current) takes time as well as processing the control decision (duty ratio) to track maximum power lags in tracking actual maximum power. This is considered a non-ideal case of tracking maximum power and creates a non-negligible error. From Fig. 7.5 it is clear that change in irradiation varies reference maximum PV panel power but due to delay in control signal the converter is unable to change duty ratio and hence creates a significant error in tracking maximum power. This problem is more pronounced when irradiation change time is less compared to PV panel time constant with capacitor and MPPT tracking error increases as shown in Fig. 7.5. The reference power P_{K2} and actual power after MPPT P_{Ka2} are not the same because P_{Ka2} holds the previous power condition as duty ratio does not change. Therefore, the

minimum circuit time constant will ensure an accurate MPPT performance. This also eliminates the usage of complex control techniques like adaptive control [15]-[16] etc. for extracting MPP.

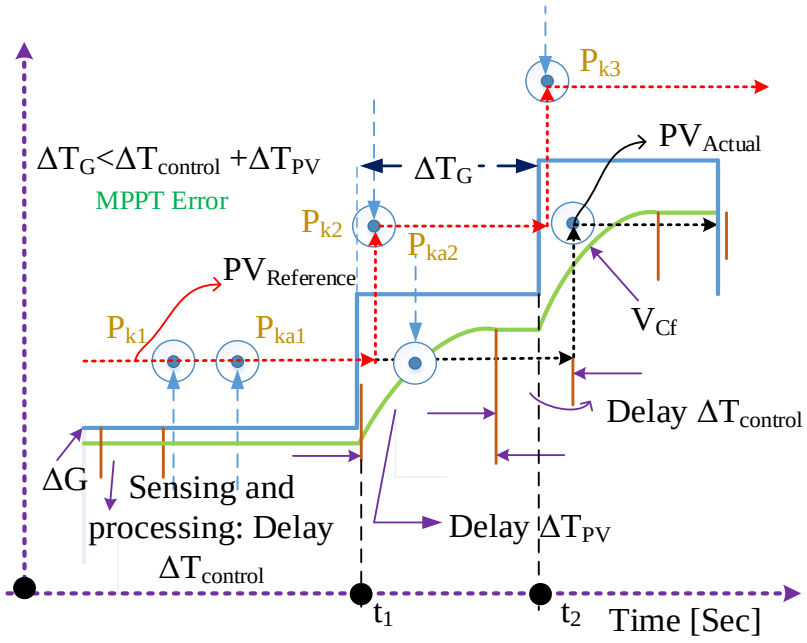


Fig. 7.5. MPPT dynamics with tracking error under irradiation change, where ΔG is the change in irradiation, ΔTpv is time delay due to PV time constant.

7.3.1.1. System dynamics from PV equivalent circuit model

System dynamics under irradiation variation can be derived using an equivalent circuit model of PV. Single diode model [1] of the PV panel is adopted in this chapter as shown in Fig. 7.6. The output current and voltage from one PV cell are $I=I_{ph}-I_d-I_{sh}$ and V respectively.

$$I_d = I_{se}\left[\exp\left(\frac{V+IR_{se}}{nV_t}\right)-1\right], \; I_{sh} = \frac{V+IR_{se}}{R_{sh}}. \tag{7.1}$$

$$\text{Thus, } I = I_{ph} - I_{se}\left[\exp\left(\frac{V+IR_{se}}{nV_t}\right)-1\right] - \frac{V+IR_{se}}{R_{sh}} \text{ and } V_t = \frac{T_c K}{q} \tag{7.2}$$

where, q: charge of the electron ($q=1.6\times10^{-19}$C) K: Boltzmann Constant. T: Temperature in K. R_{sh}: Shunt resistance, R_{se}: Series resistance, *n*: Ideality factor and I_{se}: Reverse bias saturation current.

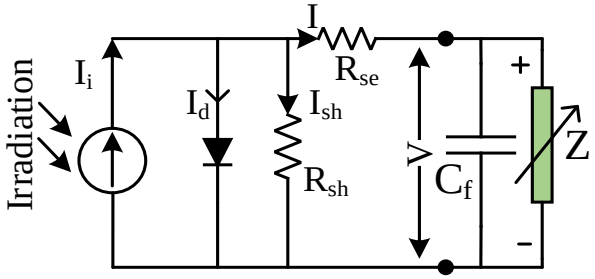


Fig. 7.6. Single diode model of PV panel.

From the equivalent circuit (Fig. 7.6) of PV, the voltage and current dynamics can be easily derived both in open circuit and loaded condition. The open circuit PV voltage equation (3) across capacitor (C_f) is

$$v(t)=i_i(t)R_{sh}\left[u(t)-u(t)e^{\frac{-t}{C_f(R_{se}+R_{sh})}}\right] \tag{7.3}$$

Where, u(t)= Step voltage, v(t)= PV voltage and i_i=PV current.

The output PV voltage contains steady-state as well as transient information. System dynamics can be expressed by equation (7.4).

$$v(t)_{transient}=i_i(t)R_{sh}e^{\frac{-t}{C_f(R_{sh}+R_{se})}} \tag{7.4}$$

Under loading condition, the transient equation (7.4) can be written as

$$v(t)_{transient}=\frac{i_i(t)}{\left[\frac{1}{R_{sh}}+\frac{1}{Z}\left(1+\frac{R_{se}}{R_{sh}}\right)\right]}e^{\frac{-t(Z+R_{se}+R_{sh})}{C_f Z(R_{sh}+R_{se})}} \tag{7.5}$$

The transient slope of the PV voltage should be maximum to attain faster transient response under irradiation change and can be derived from equation (7.4) and (7.5) which is

$$|M|=\left|\frac{dv_{o\_transient}}{dt}\right|_{t=0}=\frac{i_i(0)R_{sh}}{C_f(R_{sh}+R_{se})}=\frac{I_iR_{sh}}{C_f(R_{sh}+R_{se})} \tag{7.6}$$

Where $i_i(0)=I_i$.

Short circuit (SC) condition of PV panel provides worst transient performance. However, during MPPT operation of PV converter, the impedance is non-zero. Therefore, designing a maximum M value ensures minimum error in tracking maximum power at rapidly changing environmental conditions. But finding maximum M value requires information about series resistance (R_{se}), shunt resistance (R_{sh}) which are temperature and irradiation dependent. In this work PV panel parameters are determined through an extraction model originally proposed by J.A.Gow *et.al*. [17], which is accurate for power electronics application. It is described by the following equations.

$$I_i=K_oV\left(1+K_1T\right) \tag{7.7}$$

$$I_d=K_2T^3e^{\left(\frac{K_6}{T}\right)},\ R_{se}=K_3+\frac{K_4}{V}+K_5T,\ R_{sh}=K_8e^{K_9T} \tag{7.8}$$

Where, K_o=-5.729X10^{-7}, K_1=-0.1098, K_2=44.5355, K_3=1.47, K_4=1.612X10^3, K_5=-4.474X10^{-3}, K_6=-7.31X10^3, K_8=2.303X10^6 and K_9=-2.711X10^{-2}. V= PV Voltage at different temperature (T), irradiation (G), and T=Ambient temperature in Kelvin (K).

From equation (7.6) and (7.7), the maximum slope (M) of PV panel KC 200GT is calculated which is a function of the irradiation, temperature and different values of C_f. Theoretical results are reported in Fig. 7.7 where the base value of C_f is taken as 1000µF for calculation.

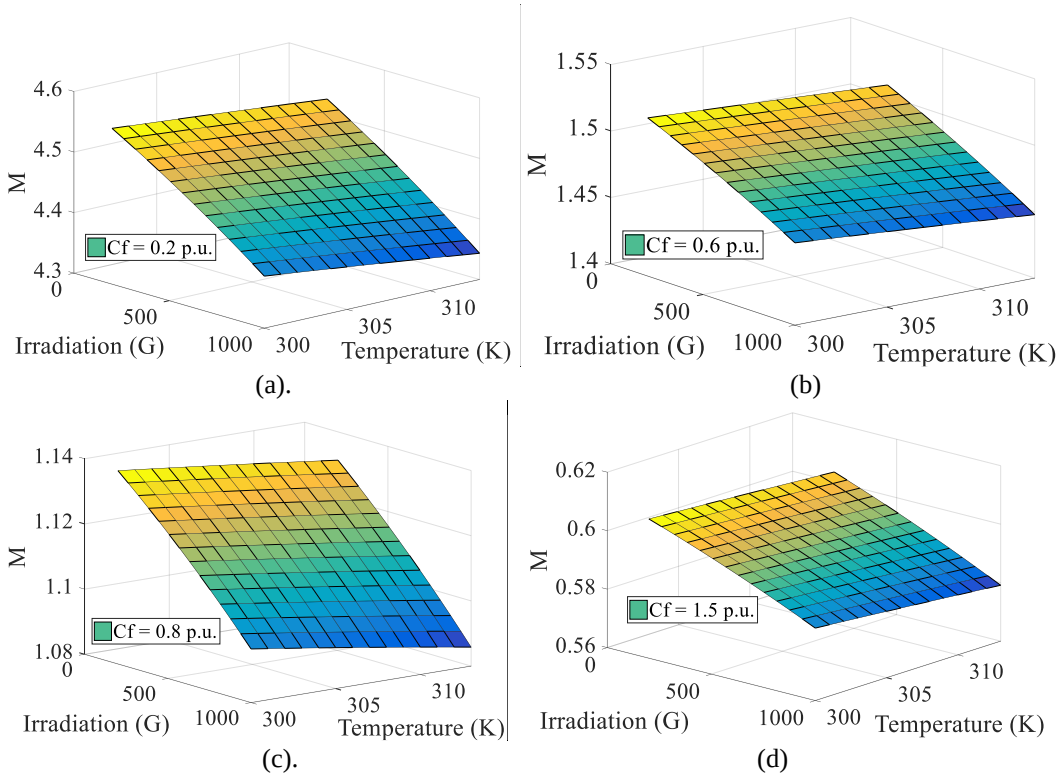


Fig. 7.7. Change in M with variation in ambient temperature T (K) and solar irradiation G (Watt/m^2) for different capacitor values.

It is evident from Fig. 7.7 that at C_f=0.2 p.u. the transient delay is least for different temperature (T) and irradiation (G) as the slope (M) is maximum. Similarly, for C_f=1.5 p.u. provides longer transient delay as the slope is very small compared to C_f=0.2 p.u. Thus, theoretically, very low capacitance ensures better MPP tracking performance. However, in practice, the capacitance value should not be too low based on PV panel rating and ripple power effect.

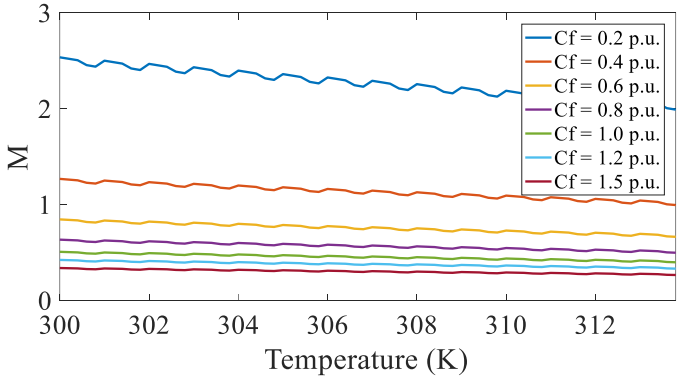


Fig. 7.8. The value of M at different ambient temperature in Kelvin.

Fig.7.8 reports the effects of temperature variation on M, considering different p.u. values

of C_f. Again, according to Fig.7.8 low capacitor ensures higher M value for better dynamic response under temperature variation and at constant irradiation. Temperature increment not only degrades PV panel efficiency [1] but also decreases slope (M) which further degrades MPP performance

7.3.1.2. Ripple power effect on capacitor (C_f) selection

DC link capacitor (C_o) before H bridge voltage source inverter (VSI) plays an important role in capacitor (C_f) selection as this value can be indirectly determined through comparison of Z_{in} looking from the output terminal of the boost converter. Therefore, the steps are initially to find the optimum value of C_o for minimizing ripple power when VSI is connected to the grid and secondly to find out effective input impedance of boost converter taking the calculated C_o value. Finally comparing Z_{cdc} and Z_{in} the accurate capacitor (C_f) value is derived. The system of analysis is shown in Fig. 7.9 and Fig.7.11. Line inductance is considered as L_i and S_1-S_4 are MOSFET switches. V_{dc} is the dc-link capacitor voltage.

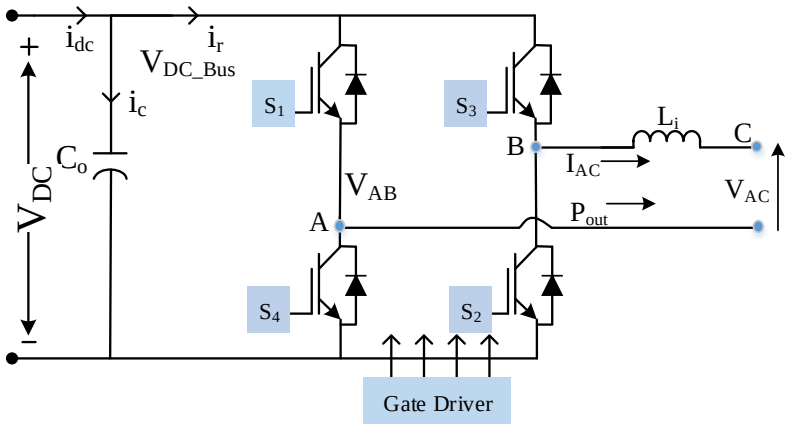


Fig. 7.9. Single-phase full-bridge inverter.

Let, the low-frequency component output voltage to be sinusoidal and equal to $V_{AB}=V_m \sin\omega t$ and $I_{AC}=I_m \sin(\omega t-\varphi)$ where ω is grid frequency and φ is phase angle difference between V_{AB} and I_{AC}. Thus, the instantaneous power injected to the grid is

$$P_{out}=V_{AC}I_{AC} \text{ with } V_{AC}=V_m \sin\omega t-\omega L_i I_m \cos(\omega t-\varphi).$$

The output power can be sub-divided into $P_{out}=P_{av}+P_{ripple}$ where if I_{AC} is controlled in phase to V_{ac}. The derivation of ripple power is mentioned in appendix A,

$$P_{av}=\frac{V_m I_m}{2}\cos\varphi \text{ and } P_{ripple}=-\frac{V_m I_m}{2}\cos(2\omega t-\varphi)-\frac{\omega L_i I_m^2}{2}\sin(2\omega t-2\varphi) \quad (7.9)$$

Line inductance is very small and therefore by neglecting it, equation (8) can be rewritten as

$$P_{ripple} = -\frac{V_m I_m}{2}\cos(2\omega t - \varphi) = \sqrt{P_{av}^2\left(1-\left(\frac{\sin\varphi}{\cos\varphi}\right)^2\right)}\sin(2\omega t - 2\varphi + \psi) \quad (7.10)$$

Thus, $P_{ripple} = B\sin(2\omega t - 2\varphi + \psi)$ (7.11)

Where, $B = \sqrt{P_{av}^2\left(1-\left(\frac{\sin\varphi}{\cos\varphi}\right)^2\right)}$

The voltage ripple of dc-link capacitor is determined from ripple power expression. This voltage ripple contains dominant 2nd order harmonics of line frequency and elimination of this harmonics is essential for successful decoupling between DC to AC side which is still a major problem [18]. Capacitor voltage dynamic equation can be written as,

$$V_{dc} i_{dc} + V_{dc} C_o \frac{dv_{dc}}{dt} = B\sin(2\omega t - 2\varphi + \psi) + P_{av} \quad (7.12)$$

The ripple power creates an extra circulating loss within the boost converter which degrades the life of the PV system. Large capacitors are generally recommended to avoid this effect. The voltage equation across C_o can be obtained by solving,

$$\left.\begin{aligned} P_{cap} = P_r = V_{dc} i_c &= -\frac{V_m I_m}{2}\cos(2\omega t - \varphi) \\ V_{dc} C_o \frac{dv_{dc}}{dt} &= -\frac{V_m I_m}{2}\cos(2\omega t - \varphi) \end{aligned}\right\} \quad (7.13)$$

The dc-link capacitor voltage as well as the maximum and minimum capacitor voltage result as

$$V_{dc} = \sqrt{\left(N - \frac{V_m I_m}{2C_o\omega}\sin(2\omega t - \varphi)\right)} \quad (7.14)$$

$$V_{dc\_max} = \sqrt{\left(N + \frac{V_m I_m}{2C_o\omega}\right)} \quad (7.15)$$

$$V_{dc\_min} = \sqrt{\left(N - \frac{V_m I_m}{2C_o\omega}\right)} \quad (7.16)$$

Where, $V_{av} = \frac{V_{dc\_max} + V_{dc\_min}}{2}$, $N = V_{av}^2 + \left(\frac{V_m I_m}{4V_{av} C_o \omega}\right)^2$

Equations (7.15) and (7.16) can be greatly simplified in

$$V_{dc\_max} = V_{av} + \frac{V_m I_m}{4V_{av} C_o \omega} \quad (7.17)$$

$$V_{dc\_min} = V_{av} - \frac{V_m I_m}{4 V_{av} C_o \omega} \tag{7.18}$$

From equations (7.15) the range of C_o can be derived

$$C_o \geq \left(\frac{V_m I_m}{4\left(V_{dc\_max} - V_{av}\right) V_{av} \omega} \right) \tag{7.19}$$

Therefore, the minimum capacitor is

$$C_{o\_min} = \frac{V_m I_m}{\left(V_{dc\_max}^2 - V_{dc\_min}^2\right) \omega} \tag{7.20}$$

Maximum dc-link voltage can be calculated by taking minimum voltage at 1 p.u. for different value of capacitances. Similarly, from equation (7.19) the minimum capacitance value is derived which is 0.2724 p.u. for an average voltage of 1.0 p.u. as shown in Fig. 7.10.

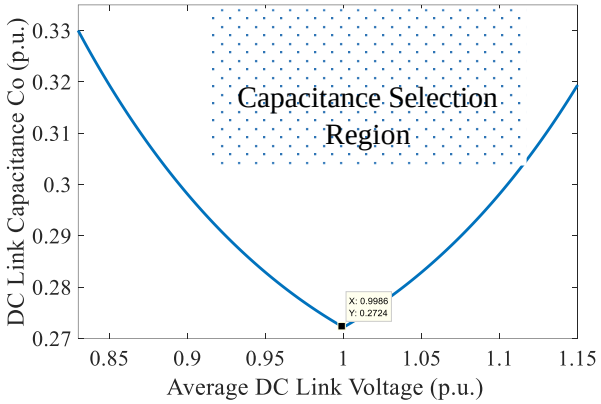


Fig. 7.10. DC link capacitance (C_o) selection region with minimum capacitance point.

The region above the minimum capacitance point as denoted in the Fig. 7.10 is capacitor selection region for proper decoupling

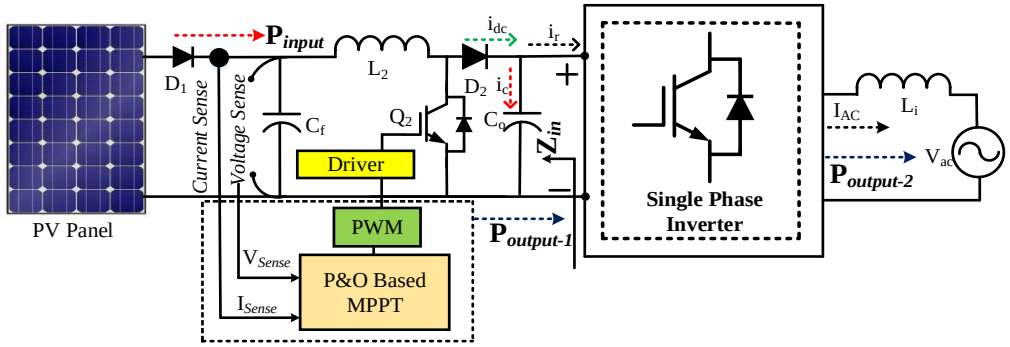


Fig. 7.11. System Configuration

Using (7.12) and (7.13) the capacitor current (i_c) can be obtained as,

$$i_c = \frac{-\frac{V_m I_m}{2}\cos(2\omega t-\varphi)}{\sqrt{\left[\left(V_{av}+\frac{V_m I_m}{4V_{av}C_o\omega}\right)^2-\frac{V_m I_m}{2C_o\omega}\left(1+\sin(2\omega t-\varphi)\right)\right]}} \quad (7.21)$$

The dc current (i_{dc}) can be measured by applying KCL at the node of boost converter load which is, $|i_{dc}|=|i_c+i_r|$ as shown in Fig. 7.9 and Fig. 7.11. Further, the capacitor current for different capacitor values is determined and plotted as shown in Fig. 7.12 (a). It is clear from the figure that the capacitor current does not vary much with changing capacitor value at a constant average dc-link voltage. But the capacitor current is prone to change with changes in average dc-link voltage at a constant capacitor value as shown in Fig. 7.12 (b).

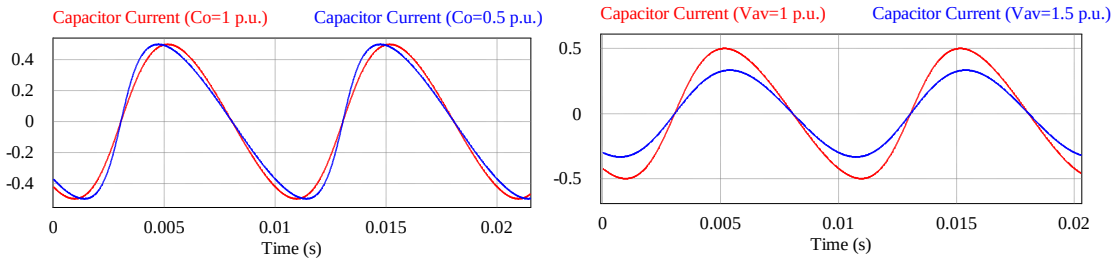


Fig. 7.12. Capacitor current (in p.u.) variation with (a) capacitance variation with constant dc-link voltage (in p.u.) (b) Variation in average dc link voltage (in p.u.) at constant capacitance.

Again, $I_{AC}=I_m\sin(\omega t-\varphi)$, is only valid if dc link voltage is greater than the maximum value of ac side voltage ($V_{dc}>V_m$). Therefore, 100 Hz ac component ripple can be decoupled with low-value capacitor C_o.

7.3.1.3. Selection procedure

As per the discussion in PV panel parameter C_f value should be low for accurate MPP extraction under irradiation variation. However, C_o is having a minimum value as given in equation (7.19) for proper decoupling. Thus, comparing the effective equivalent impedance (Z_{in}) looking from C_o with Z_{Cdc}, the correct C_f value is determined which ensures proper power decoupling and error-free maximum power tracking. For a boost converter, the input impedance (Z_{in}) depends on the duty ratio (D), C_f and inductor L_2. The R_f value is the combination of R_{se}, R_{sh}, and ESR of inductor L_2.

$$Z_{in}=\frac{1}{D^2}\frac{s^2L_2C_fR_f+sL_2+R_f}{1+sR_fC_f} \quad (22)$$

For large C_f value Z_{in} is dominated by inductor L_2. However, C_f value should not be too high to make error-free power point tracking. Hence input impedance (Z_{in}) is plotted taking

C_f=0.2 p.u. and other parameters from Table-1 with frequency variation greater than 1 kHz. Again, the impedances (Z_{cdc}) of C_{dc} are plotted under different C_{dc} values as per the minimum value requirement as given in equation (7.19). From Fig. 7.13, it is clear that the Z_{in} is higher than Z_{cdc} for all frequencies greater than 1 kHz.

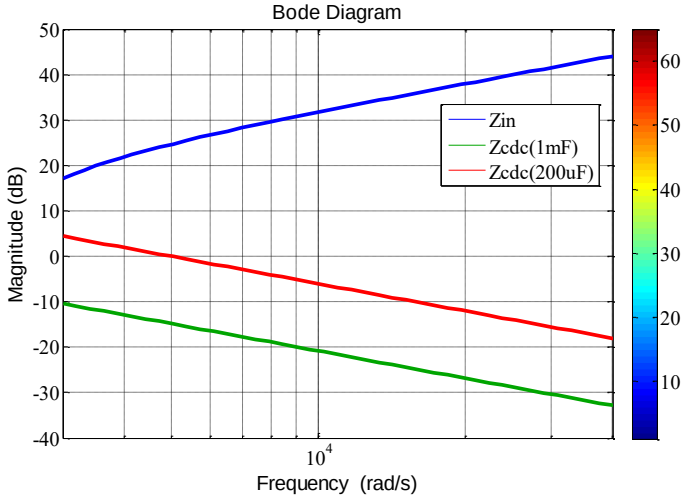


Fig. 7.13. Input impedance (Z_{in}) of boost converter with impedance (Z_{cdc}) of C_{dc}.

Thus, proper decoupling is achieved from DC to AC side and high-frequency component of the boost converter is achieved successfully. Therefore, the PV voltage is regulated properly using a DC-DC boost converter with small ripple. This is achieved with full-bridge ac current regulation using small dc-link capacitor and source-side capacitor value minimization. The settling time [19] depends on the capacitor value both in MPP region and constant current region (CCR) which are respectively,

$$T_{\Delta} = -\frac{1}{\xi_{PV}\omega_n}\ln\left(\Delta\sqrt{1-\xi_{PV}^2}\right) \tag{7.23}$$

$$\text{And } T_{\Delta} = -\frac{1}{\xi_{PV}\omega_n}\ln\left(\frac{\Delta}{2}\sqrt{1-\xi_{PV}^2}\right) \tag{7.24}$$

Where $\xi_{PV} \approx \frac{1}{2}\left(\frac{1}{r_{pv}}\sqrt{\frac{L_2}{C_f}} + R_f\sqrt{\frac{C_f}{L_2}}\right)$ and $\omega_n \approx \frac{1}{\sqrt{L_2 C_f}}$

The worst dynamic performance of PV is at short circuit condition, therefore ζ_{PV} at short circuit (SC) condition is the guiding parameter of selecting perturbation frequency.

$$\xi_{PV\_SC} \approx \frac{R_f}{2}\sqrt{\frac{C_f}{L_2}} \tag{7.25}$$

Therefore, the perturbation time interval (ΔT) should be greater than $T\Delta$ in short circuit (SC).

$$|\Delta T\rangle|T_{\Delta}| = \frac{1}{\xi_{PV\_SC}\omega_n} \ln\left(\Delta\sqrt{1-\xi^2_{PV\_SC}}\right) \quad (7.26)$$

Thus, for low capacitor value, the settling time becomes lower and low perturbation frequency can effectively track the MPP under steady and dynamic condition. This settling time is important in MPP tracking performance. For lower settling time, the MPP performance is better compared to higher settling time as shown in the Fig. 7.14. The error ($\int|P_{PV}-P_{MPP}|$) is calculated using adding difference P_{MPP} and P_{PV} which is running within continuous while loop in Lab-View programme under a step variation of irradiation.

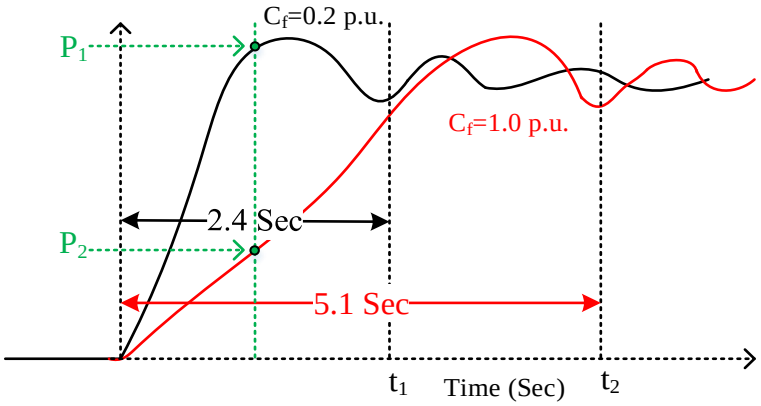


Fig. 7.14. MPPT performance and settling time with different capacitance value.

Therefore, correct selection of the capacitance (C_f) is essential to reduce settling time so that MPP performance can be improved. It should be mentioned that the PV power should reach its steady-state before the next MPPT perturbation is applied. Therefore, the settling time will determine the maximum MPPT sampling rate. Finally, the low capacitance at source side (C_f) and dc-link capacitance (C_o) ensures correct MPP tracking of PV and successful decoupling of DC to AC side. The system configuration to validate the theoretical finding is mentioned in TABLE-7.1.

TABLE-7.1
SYSTEM CONFIGURATION

Components	**Parameters**	**Part Number**
PV Panel (One Unit)	V_{oc}=32.9 V, I_{sc}=7.61 A P_{max}=200 W	KC 200GT
Boost Converter	V_{in}=20 to 40 V V_o=80 V , L_2= 1mH C_o =400uF , C_f=200uF f_{sw}=10kHz	**MOSFET**: IRF640 **Ferrite Core**: PQ **Optocoupler** (6N137) **based Gate Driver**: IR2110
H bridge Inverter	PWM method= Sin-triangle PWM Carrier Frequency (f_c)=5 kHz	MOSFET: IRF 640 Gate driver: IR2110

	1kVA	
Central Controller for boost converter and H bridge Inverter	Programming in Lab-View Scan Interface.	NI cRIO 9082 Module: NI 9401, NI 9227 (current sensor) NI9225 (Voltage Sen sor)
PV interfaced capacitor (C_f)	C_f=200 uF@ 350V, 1000uF@450V (Electrolytic)	ST1047, H045
Transformer	Step-Up type, 1kVA	Turns Ratio (1:5)

The performance of proposed error-free maximum PV power extraction system with correct capacitance value is compared with existing techniques like adaptive control, flexible multi-MPPT control, though all the existing methods are based on control techniques.

TABLE-7.2
PERFORMANCE COMPARISON

Methods	**Processing Delay & Hardware Complexity**	**Settling Time (Sec)**	**Tracking Error***
PV Micro inverter with P& O algorithm [3]	High Low ADC requirement (Approx 10kspa) **Computational Barden**: Low	Min-6.5	≈16-17%
PV Microinverter with adaptive P&O control [10]	Medium Fast ADC Rrquirement. (Approx.30ksps) **Computational Barden**: Medium	Min-0.034 Max-5.1	1-2%
Flexible Multi-MPPT Control. [20]	Medium Fast ADC Rrquirement. (Approx.30ksps) **Computational Barden**: High	Min-3.0	Medium
Adaptive FPPT Control [7]	Medium Fast ADC Rrquirement. (Approx.30ksps) **Computational Barden**: High	Min-1.2 Max-10.5	Min-3.3% Max-14.4%
Proposed capacitor selection-based P&O MPPT.	Low Low ADC requirement (Approx 10kspa) **Computational Barden**: Low	Min-2.4	Min-2.9%

From TABLE-7.2, it is clear that all the existing methods for tracking error-free maximum power are based on advanced control techniques. These control techniques increase computation burden and do not guarantee a zero error maximum power extraction under the changing environment as they are based on same voltage and current dynamics. The proposed technique guarantees true error-free power extraction as voltage and current dynamic changes quickly as per change in irradiation and temperature.

7.3.2. Results and discussion

From the previous discussion, it is clear that for low capacitance value ensures better performance of MPP tracking from PV under varying environmental conditions. It also confirms better performance at low perturbation frequency when a perturbation-based technique is used for extracting maximum power. PSIM 9.1.1 software platform is used for simulating the proposed system and 500W practical PV laboratory prototype system is used for validating the proposal. From Figs. 7.15 (a) and 7.15 (b) it is evident that MPP performance is better at C_f=0.2 p.u. than C_f=1.0 p.u. case.

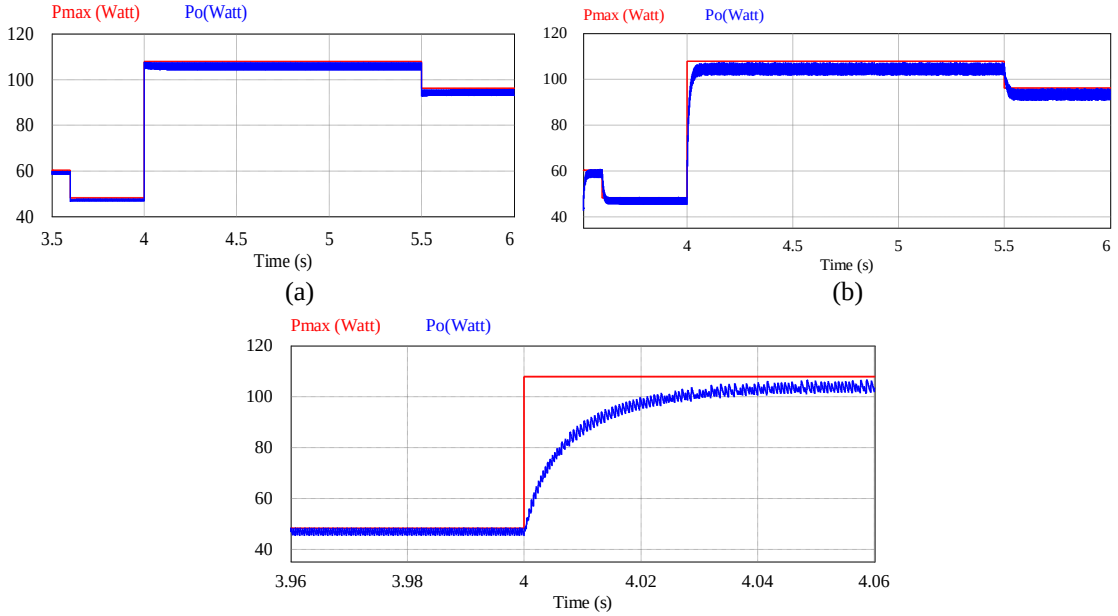


Fig. 7.15. (a) Power point tracking with C_f=0.2 p.u. (b) Power point tracking with C_f=1 p.u. (c) Zoomed view at t=4sec in power point tracking with C_f =1.0 p.u.

Delay is higher with high C_f in MPP tracking. The high value capacitor takes a larger time to settle the new voltage value as shown in Fig. 7.16 (a) during irradiation change at 4 sec whereas the voltage change is almost immediate at low C_f. Therefore, the MPP error is greater with a large value of capacitor (C_f).

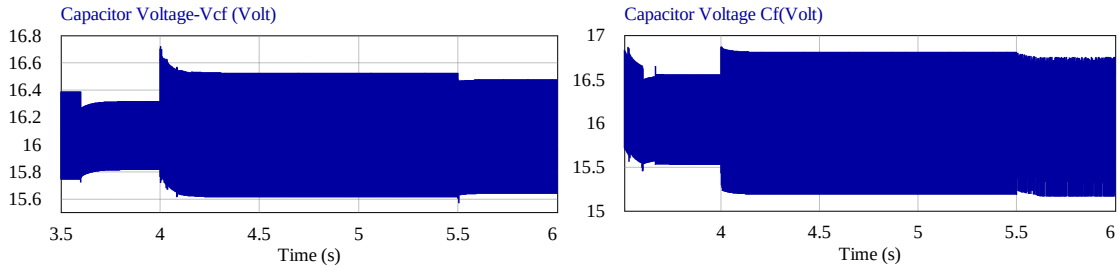


Fig. 7.16. (a) Capacitor voltage for C_f=1.0 p.u. (b) Capacitor Voltage for C_f= 0.2 p.u.

The proposed concept is applied in 500W prototype PV panel system as shown in Fig. 7.17. The control environmental condition is designed using NI-cRIO 9082.

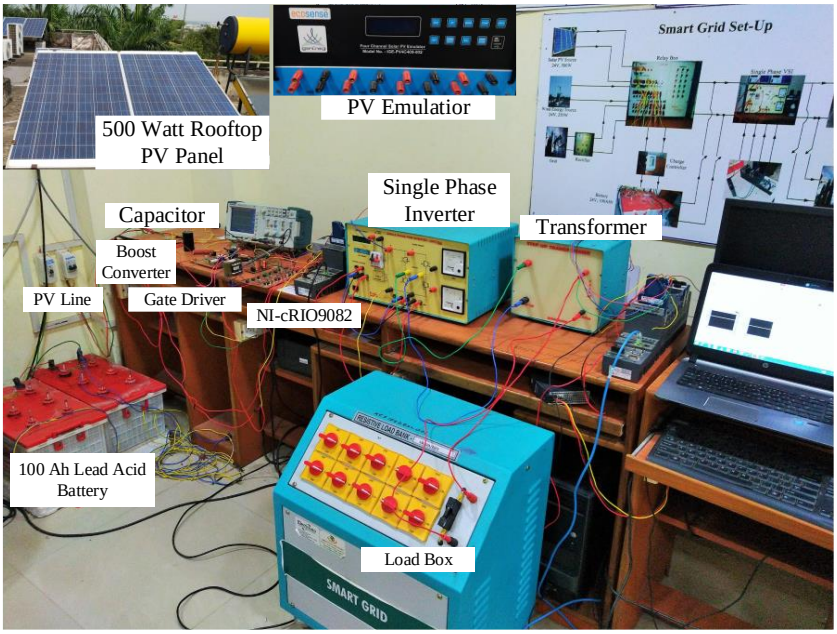
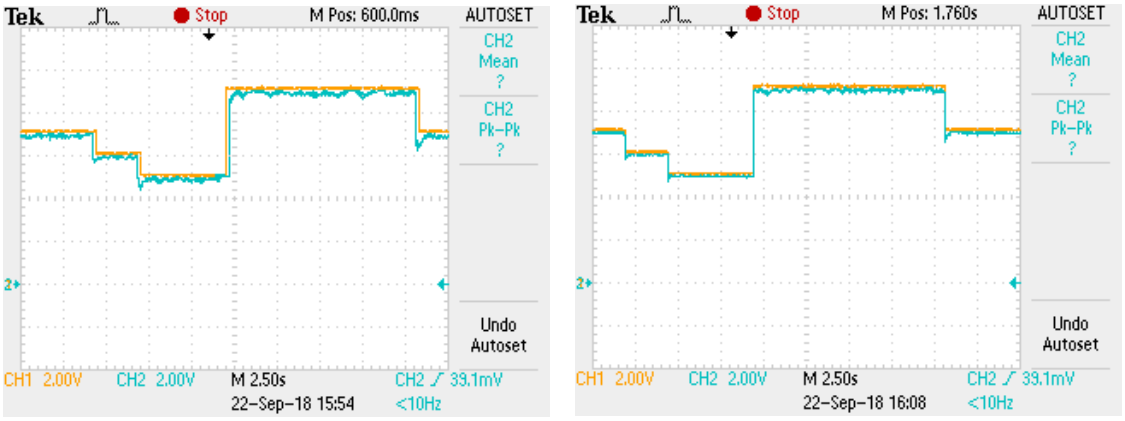


Fig.7.17. Hardware set up.

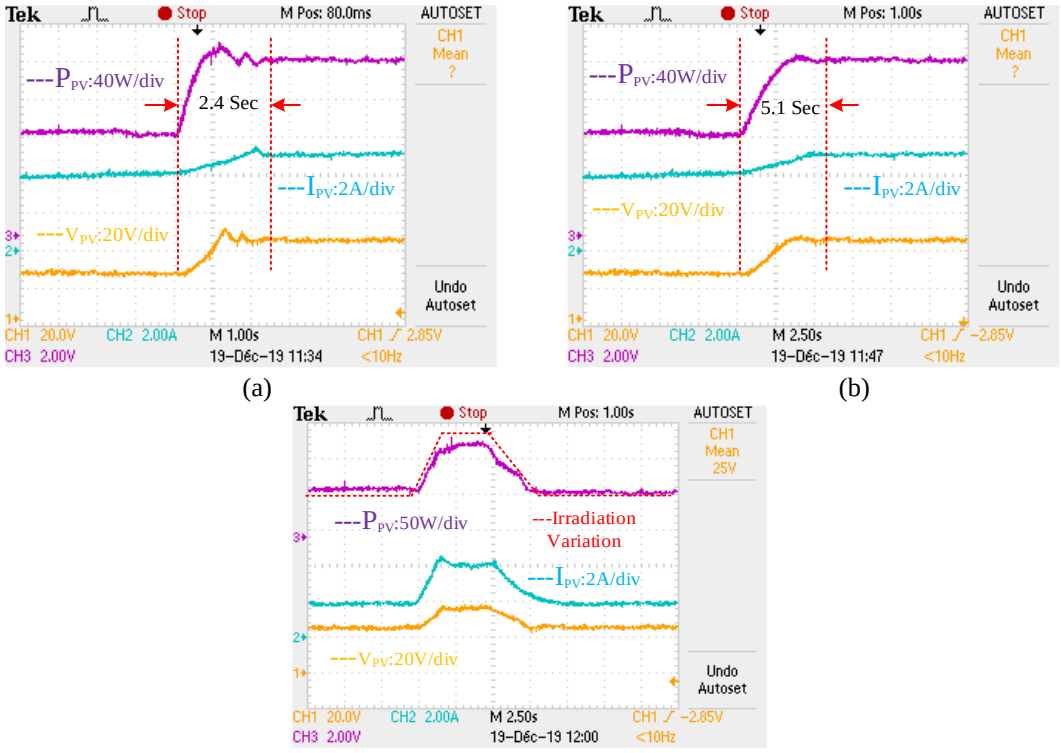
The MPP power is calculated by measuring PV voltage (V_{cf}) and current. Temperature effect is ignored as temperature is almost constant during measurement. MPP tracking performance is tested for different irradiation variations (600W/m^2-500W/m^2-400W/m^2-800W/m^2-600W/m^2) with low capacitance (C_f=0.2 p.u.) as shown in Fig. 7.18 (b). Under the same conditions, the tracking performance degrades with higher capacitance (C_f=1.0 p.u.) as shown in Fig. 7.18 (a). The practical results as shown in Fig.7.18 (a) and Fig. 7.18 (b) confirms that MPP error is less with low capacitance i.e., at C_f =0.2 p.u compared to C_f=1.0 p.u. The hardware results matches with the simulated results.



(a) (b)

Fig. 7.18. Maximum power point (MPP) tracking performance (a) with C_f=1.0 p.u. (b) with C_f=0.2 p.u. **Y Axis**: [**Yellow-P_{MPP}** Maximum power point, **Blue-PV available power**] (**20 Watt/div**), **X Axis**: Time (**2.5s/div**).

Perturb and observe (P & O) MPPT method is tested at a step irradiation changes from 300 W/m^2 to 1000 W/m^2 with higher capacitance and lower capacitance value. It is found that the same P and O MPPT algorithm performs better as settling time is less (2.4 sec) with lower capacitance (C_f=0.2p.u.) compared to higher capacitance (C_f=1p.u.) as shown in Fig.7.19 (a) and Fig. 7.19(b). Fig. 7.19 (c) shows a better tracking performance under a pulse irradiation variation.



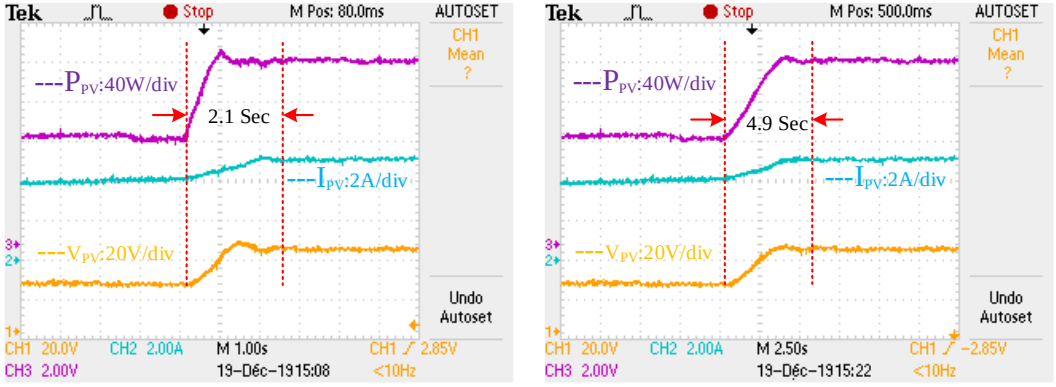
(a) (b)

(c)

Fig. 7.19. P&O Performance at step irradiation change (300 W/m2-1000W/m^2) with different capacitance (a) C_f=0.2p.u. (b) C_f=1.0p.u. (c) Better tracking performance with Cf=0.2 p.u. (300 W/m^2-700 W/m2-300 W/m^2)

Another testing (step change of irradiation from 300 W/m^2-1000W/m^2) is performed

implementing incremental conduction (IC) method of MPPT for performance verification with lower value of capacitance. The settling time is less i.e., 2.1 sec for lower capacitance (C_f=0.2p.u.) whereas it is higher i.e., 4.9 sec for higher capacitance (C_f=0.2p.u.) in IC method of MPPT as shown in Fig. 7.20.



(a) (b)

Fig. 7.20. IC Performance at step irradiation change (300 W/m^2-1000W/m^2) with different capacitance (a) C_f=0.2p.u. (b) C_f=1.0 p.u.

A comparison is performed with P & O and IC method as mentioned in TABLE-7.3, which confirms betterment in settling time and error tracking performance with using low capacitance value.

Table-7.3
Performance Comparison

Methods	**Settling Time (Sec)**	**Tracking Error***
P & O Method with C_F=0.2 p.u.	≈2.4	2.9%
P & O Method with C_F=1.0 p.u.	≈5.1	6.8%
IC Method with C_F=0.2 p.u.	≈2.1	2.74%
IC Method with C_F=1.0 p.u.	≈4.9	6.47%

The error in tracking MPP increases with a higher capacitance value as shown in Fig. 7.21.

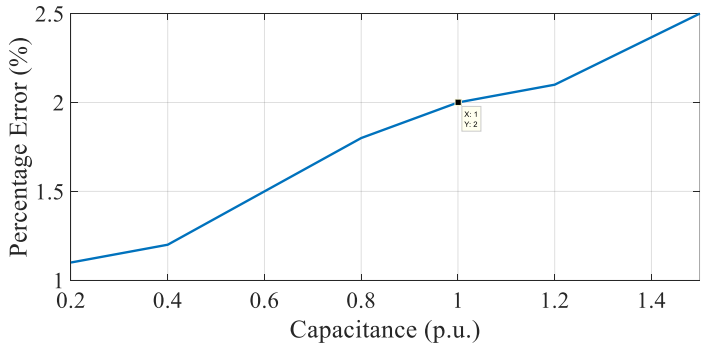


Fig. 7.21. MPP Error for different (C_f) in p.u. @ 500W PV Panel.

However, low capacitance value has a restriction in practical application based on the power of PV system. For a small power PV system, a low capacitance value is suitable. As shown in TABLE-7.4 the preferable design of PV based power extraction system is simulated and

tested. The MPPT performance at partial shading condition is tested with C_f=200µF. Two 250-Watt PV panels are connected in series with uniform irradiation at 800 W/m^2. Irradiation is changed to 200 W/m^2 in one panel during operation to achieve partial shading effect.

Table-7.4
Capacitor Selection Value With Wattage and Error

Capacitor Selection value (Electrolytic)	**Power of the System**	**Irradiation Variation**	**Error**
1000uF (Simulated)	4000W	800-1000 watt/m^2	72W
1000uF (Simulated)	2000W	800-1000 watt/m^2	42W
800uF (Simulated)	1200W	800-1000 watt/m^2	30.5W
800uF (Simulated)	1000W	800-1000 watt/m^2	24W
200uF @ 350Volt (Simulated and Tested)	500W	800-1000 watt/m^2	6W

The power extraction performance at shaded condition with C_f=0.2 p.u is better compared to high C_f=1.0 p.u. as shown in Fig. 7.22 (a) and Fig. 7.22 (b). As P & O algorithm fails to track the global maximum point (GMP) under partial shading therefore better algorithm with low capacitance (C_f) value performs better in terms of tracking GMMP.

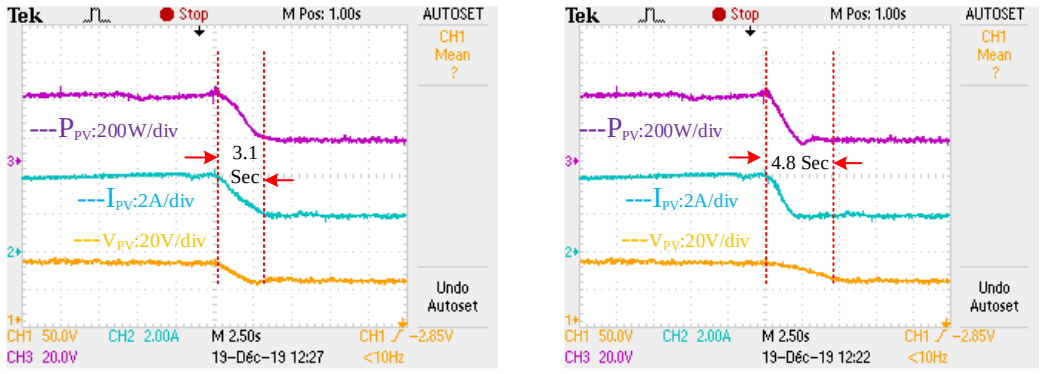


Fig. 7.22. PV output at partial shading (a) with C_f= 0.2 p.u. (b) with C_f=1.0 p.u.

Delay is measured in lab view font panel using waveform chart. NI 9225 (voltage sensor) and NI 9227 (current sensor) are used to measure PV power and analog channel NI 9263 is used after power scaling for analog power output as a voltage signal as shown in Fig. 7.23.

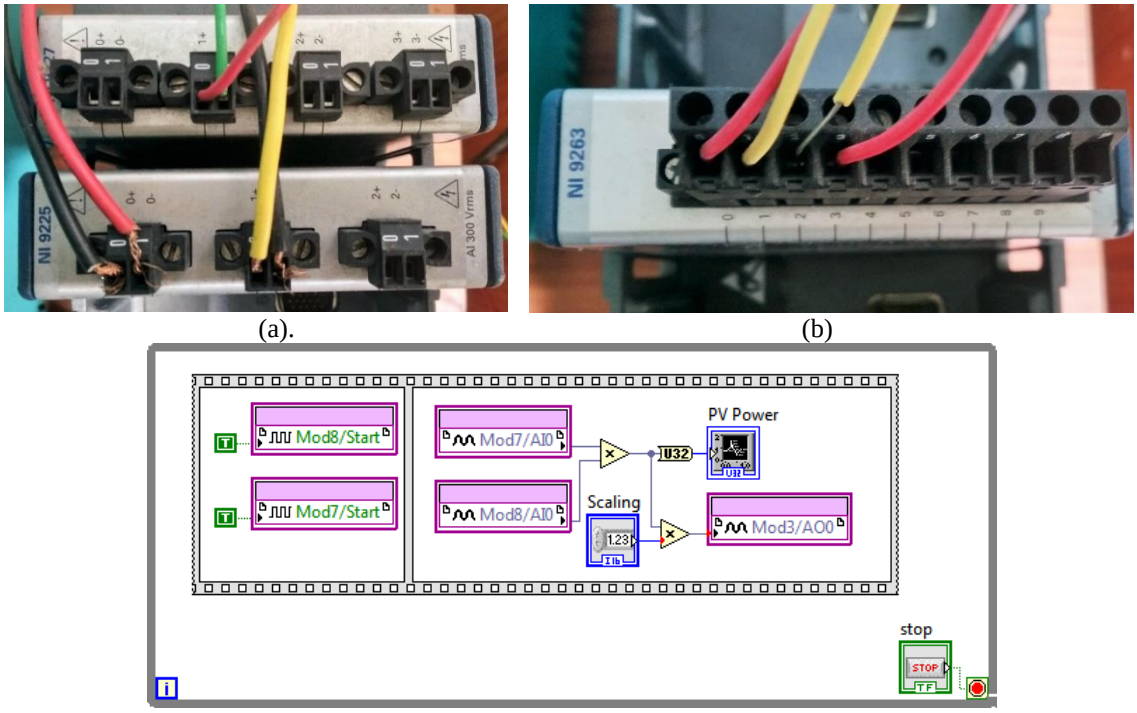


Fig. 7.23. (a) NI 9225, NI 9227 module (b) NI 9263 analog output module (c) Programme in Lab-View for the measurement.

From the analysis, it is clear that the impact of capacitor (C_f) on MPPT performance of PV panel using fixed perturbation frequency under irradiation and temperature variation is not negligible. The capacitor (C_f) value is selected based on parameters like maximizing M, settling time and ripple power. This selection further confirms the perturbation frequency which guarantees accurate MPP tracking under varying environmental conditions. Based on 500W prototype study, it is found that in an average extra 4.5W power is lost if C_f value is selected as 1000µF instead of 200µF. Again, with low capacitance (C_f) value reduces the settling time in each perturbation. Therefore, perturbation frequency can be limited to extract correct MPP for different environmental conditions. The capacitor value helps in extracting maximum power from PV using simple P&O algorithm and also reduces system delay time during any perturbance of source voltage or load variation.

7.3. Inductor Value Selection for Boost converter and BDC

The inductor value can be designed based on the switching frequency and inductor current ripple similarly like the procedure used for swiched mode power supply design. However, for the PV dominated microgrid there is a need to crosscheck another major condition which if neglected can leads to sustained oscillations in the DC link voltage. The PV panel as per characteristics can be considered as dependent current source as shown in Fig. 7.24 (a). Therefore, connecting boost converter directly i.e., inductor direct conection with dependent current source as shown in Fig. 7.24(b) is a wrong and PV panel has to bear the

ripple current which degrades the PV panel life. Therefore, capacitor is required for supplying the ripple current and it has a huge impact on MPPT performance which is discussed before. The capacitor value is already calculated from the analysis discussed in this chapter. But, if inductor value is selected based on ripple current then there may be sustained oscillation as there is a formation of LC resonant tank as shown in Fig. 7.24(c) and if resonating time is same as switching time then oscillation will come at the DC link output of boost converter. The switching time or perturbance time is already selected based on MPPT algorithm. So, only component left is inductor. Thus, inductor value should be such so that

$$\pi\sqrt{L_i C_f} >> \frac{1}{f_{sw}} \tag{7.27}$$

The equation (7.27) guides the accurate value of the inductor for PV connected converter.

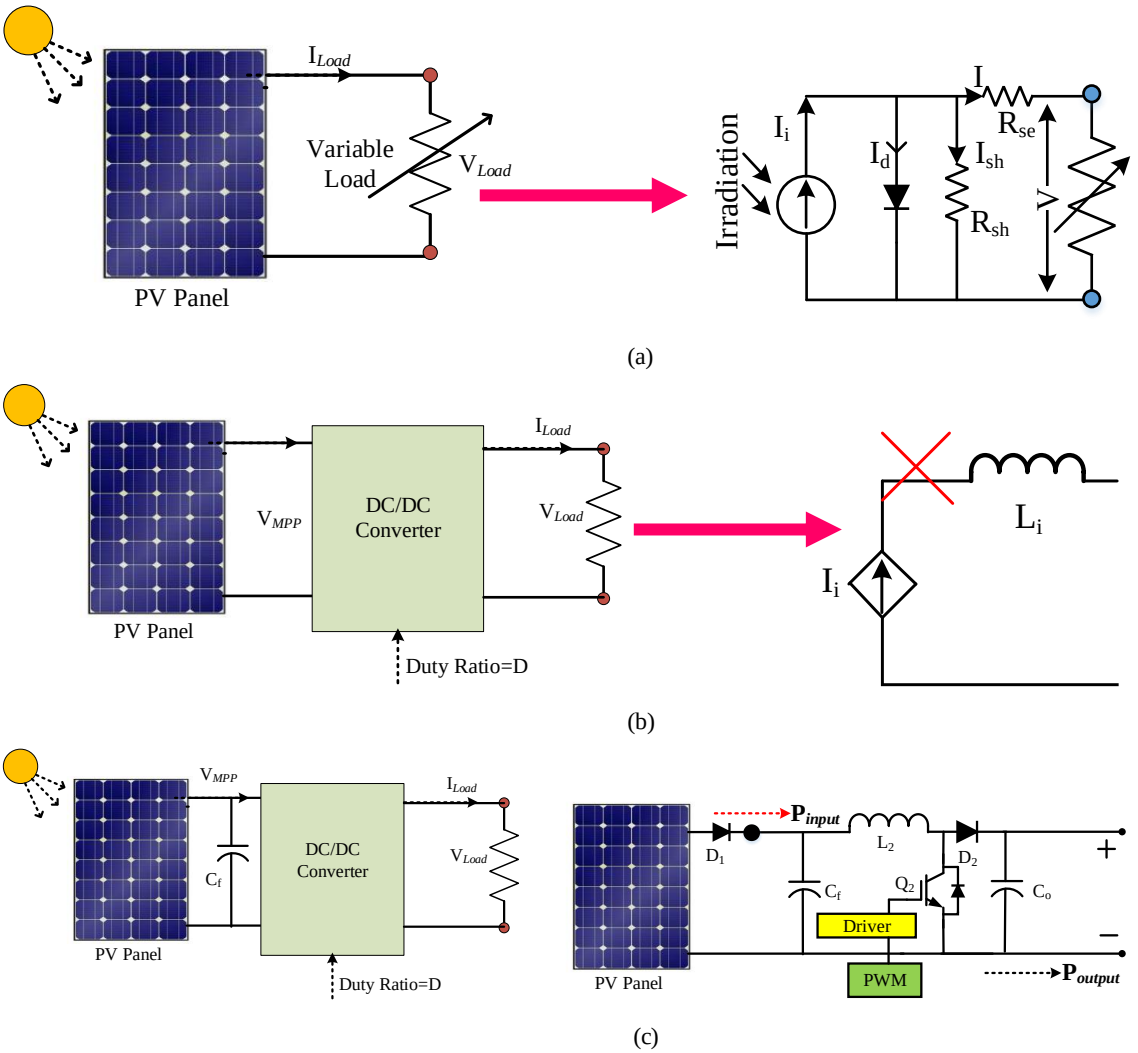


Fig. 7.24. PV panel connected converter (a) equivalent circuit model (b) dependent current source with serier inductor (b) correct configuration.

7.4. Design of LVDC Microgrid including Storage Interface

The procedure discussed for selecting capacitor and inductor for PV connected microgrid system is very important for achieving less time constant for improving transient performance from the system. Thus, this system configuration with faster BDC ensures better dynamic performance. A laboratory prototype of 48V, 1kW DC microgrid is designed using NI-cRIO 9082 as central controller for performance verification of proposed BDC. The hardware set-up is shown in Fig. 7.25.

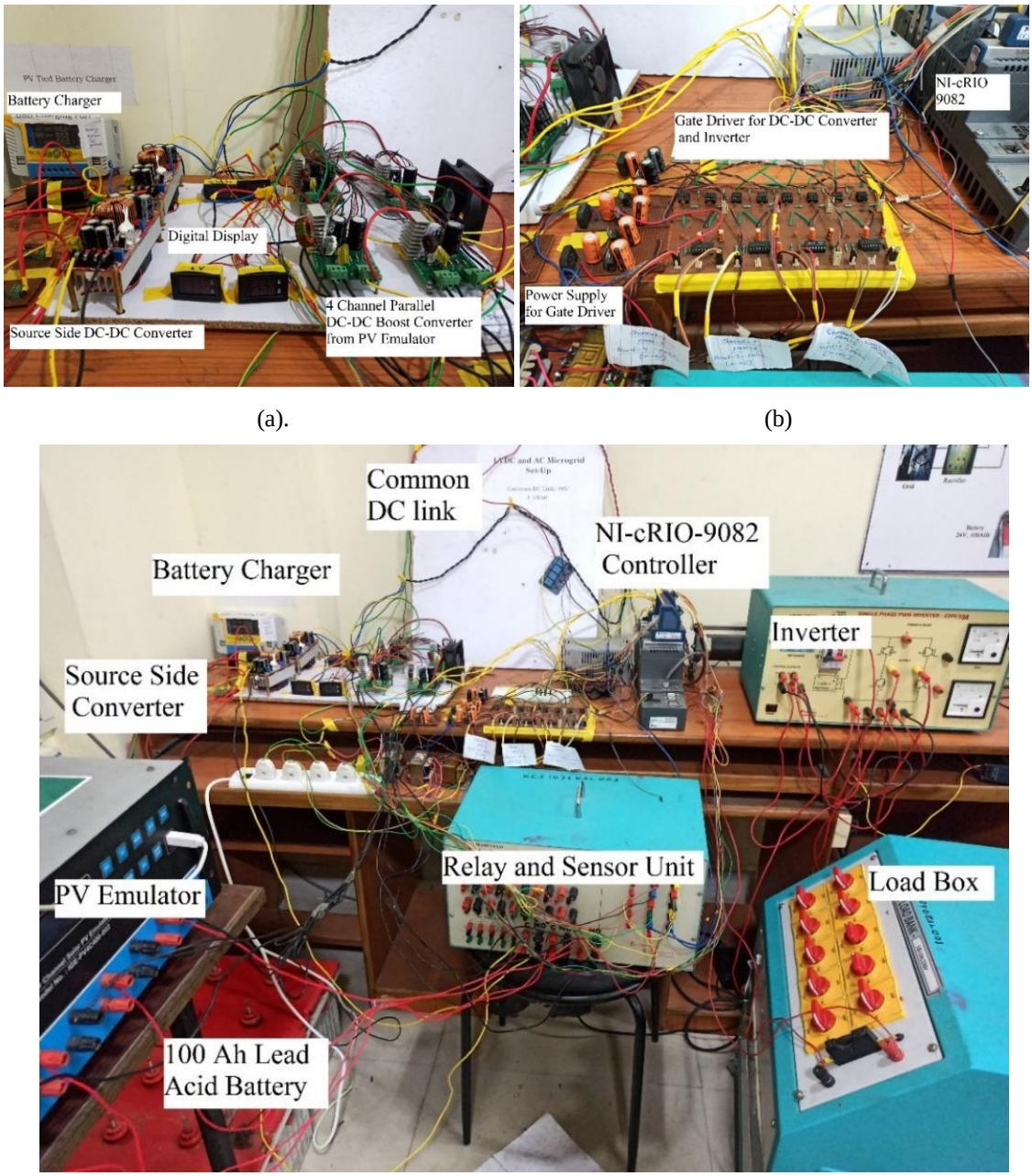


Fig. 7.25. (a) Four parallel PV channel boost converter (b) gate driver circuit using IR2110 (c) total automated set-up.

7.5. Importance of Circuit Delay in LVDC Microgrid

When all the subsystems in a microgrid are connected in cascaded both from PV power string or from battery power string or combined the circuit time constant increases. For example, PV main string total delay is

$$\tau_{PV}+\tau_{DC/DC}+\tau_{system}=\tau_{string\text{-}1} \tag{7.28}$$

Similarly, battery power string delay is

$$\tau_{battery}+\tau_{BDC}+\tau_{system}=\tau_{string\text{-}2} \tag{7.29}$$

For faster switching from PV power to battery power to meet load demand and stabilize the DC link voltage both these delays should be as small as possible. By making faster DC/DC or BDC converter will not solve the whole system dynamic performance. Thus, the system delay is very critical for achieving faster response and enhanced stability.

7.6. Summary

In this chapter the importance of accurate selection of passive components of PV dominated microgrid system is discussed. The capacitor and inductor value selection procedure and its impact on system dymamic performance is tested. The guideline for selecting system components is discussed in detailed in this chapter. The circuit time constant reduction is equally important as reduction in time constant of BDC or DC/DC converter for dynamic performance improvement.

7.7. Publications and References

Publications:

Journal:

S. B. Santra, D. Chatterjee, K. Kumar, M. Bertoluzzo, A. Sangwongwanich and F. Blaabjerg, "Capacitor selection Method in PV Interfaced Converter Suitable for Maximum Power Point Tracking", **IEEE Journal of Emerging and Selected Topics in Power Electronics**, Vol. 9. No. 2, pp. 2136-2146, April 2021.

Conference:

S. B. Santra, D. Chatterjee, S. Banerjee, K. Kumar and M. Bertoluzzo, "Selection of capacitor in PV system for Maximum Power Point Tracking**, Proceedings of 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)**, IIT Madras, India, 2018.

References

[1] Yongheng Yang, Katherine A. Kim, Frede Blaabjerg, and Ariya Sangwongwanich “Advances in Grid-Connected Photovoltaic Power Conversion Systems”, 1st edition, *Woodhead Publishing*, Aug. 2018.

[2] C.S. Solanki, “Solar Photovoltaics Fundamentals, Technologies and Applications”, 2nd edition, New Delhi, India: *PHI Learning Private Limited*, 2011.

[3] D. Sera, T. Kerekes, R. Teodorescu, and F. Blaabjerg, "Improved MPPT method for rapidly changing environmental conditions," *IEEE International Symposium on Industrial Electronics*, Montreal, Que., 2006, pp. 1420-1425.

[4] D. Sera, R. Teodorescu, J. Hantschel, and M. Knoll, "Optimized Maximum Power Point Tracker for Fast-Changing Environmental Conditions," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2629-2637, July 2008.

[5] G. Escobar, S. Pettersson, C. N. M. Ho, and R. Rico-Camacho, "Multisampling Maximum Power Point Tracker (MS-MPPT) to Compensate Irradiance and Temperature Changes," in *IEEE Transactions on Sustainable Energy*, vol. 8, no. 3, pp. 1096-1105, July 2017.

[6] S.B.Santra, D.Chatterjee, S.Banerjee, K.Kumar, and M. Bertoluzzo, “Selection of Capacitor in PV System for Maximum Power Point Tracking”, in *Proceedings of IEEE International Conference on Power Electronics, drives and energy systems (PEDES-2018), IIT Madras*, India, Dec-2018. ISBN: 978-1-5386-9316-2/18/$31.00 ©2018 IEEE.

[7] H. Dehghani Tafti, A. Sangwongwanich, Y. Yang, J. Pou, G. Konstantinou, and F. Blaabjerg, "An Adaptive Control Scheme for Flexible Power Point Tracking in Photovoltaic Systems," in *IEEE Transactions on Power Electronics*. 34, no. 6, pp. 5451-5463, June 2019.

[8] Tafti, Hossein Dehghani, et al. "A Multi-Mode Flexible Power Point Tracking Algorithm for Photovoltaic Power Plants." *IEEE Transactions on Power Electronics*, Vol. 34, no.6, pp. 5038-5042, June 2019.

[9] W. Feng, et al. "An Improved Submodule Differential Power Processing-Based PV System with Flexible Multi-MPPT Control." *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol.6, no.1, pp. 94-102, March 2018.

[10] S. Sankar, et al. "High-Speed Maximum Power Point Tracking Module for PV Systems." *IEEE Transactions on Industrial Electronics*, vol. 66, no.2, pp. 1119-1129, Feb 2019.

[11] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2711-2726, June 2013.

[12] R. W. Erickson and A. P. Rogers, "A Microinverter for Building-Integrated Photovoltaics," *24th Annual IEEE Applied Power Electronics Conference and Exposition, Washington*, DC, 2009, pp. 911-917. doi: 10.1109/APEC.2009.4802771.

[13] S. Jiang, D. Cao, Y. Li, and F. Z. Peng, "Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking," in *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4711-4722, Nov. 2012.

[14] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Power Electronics and Control Techniques for Maximum power harvesting in Photovoltaic System" Boca Raton, FL, USA: CRC Press, 2013.

[15] Yang, Y, Wen, H., "Adaptive perturb and observe maximum power point tracking with current predictive and decoupled power control for grid-connected photovoltaic inverters", *Journal of Modern Power System And. Clean Energy*, vol. 7, no.2, pp.422-432, March 2019.

[16] L. Piegari, R Rizzo; I. Spina; and P. Tricoli, "Optimized Adaptive Perturb and Observe Maximum Power Point Tracking Control for Photovoltaic Generation." *Energies*, vol.8, no.5, pp. 3418-3436, April 2015.

[17] J. A. Gow and C. D. Manning, "Development of a photovoltaic array model for use in power-electronics simulation studies," in *IEE Proceedings - Electric Power Applications*, vol. 146, no. 2, pp. 193-200, Mar 1999.

[18] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," in *IEEE Transactions on Industry Applications*, vol. 36, no. 5, pp. 1419-1429, Sept.-Oct. 2000.

[19] J. Kivimäki, S. Kolesnik, M. Sitbon, T. Suntio, and A. Kuperman, "Revisited Perturbation Frequency Design Guideline for Direct Fixed-Step Maximum Power Point Tracking Algorithms," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4601-4609, June 2017.

[20] Hu, Jiefeng, et al. "A model predictive control strategy of PV-Battery microgrid under variable power generations and load conditions." *Applied Energy*, vol. 221, pp. 195-203, July 2018.

Chapter-8

Conclusions and Future Works

In this chapter the achievement through this work is summarized as conclusion and works need to be done for further betterment and unsolved question is left as future scope.

8. Conclusions and Future Works

8.1. Conclusion

This current work started with several unsolved topological question and requirement to design high efficiency; high voltage gain bidirectional DC-DC converter suitable for storage interface in microgrid. The designed converter can also be applied to auxiliary power supply for EV. Coupled inductor based non-isolated BDC topologies are designed for less than 1kW rating and peak efficiency achieved is greater than 95%. GaN-FET based wide bandgap device is also adopted for achieving better efficiency. The main contributions of this thesis are,

(a) Proposed a new coupled inductor based generalized boost structure which can provide voltage gain >10 at duty ratio range between 0.4-0.5 using coupled inductor with number of turns n=2. The proposed circuit has inherent low switch current stress at low voltage side main switch.

(b) Proposed a new high gain, high efficiency coupled inductor based bidirectional DC-DC converter suitable for 48V-380V interface system in microgrid. The designed converter is able to operate at base average efficiency of 93% in all loading conditions during both buck and boost mode of operation. Single turn (n=1) winding coupled inductor is used for designing the circuit. The circuit has parallel path structure at low voltage side to share large current.

(c) Proposed a new L-D based GaN-FET driver for reliable switching operation of GaN-FET based converter. The proposed gate driver is used for GaN-FET based implementation of proposed coupled inductor based BDC converter. 1-1.5% efficiency improvement is found compared to MOSFET after using GaN-FET switch. The proposed GaN-FET driver ensures zero false triggering event with larger drain current with dead time.

(d) Proposed a new circuit which can potentially replace the interleaved structure for minimizing input current ripple of low voltage side. The proposed structure also helps in designing high voltage conversion factor in both the operating modes. The ripple current is very low at low voltage side of BDC and it allows to select very low value of filter capacitor. The source ripple current is almost flat for variations in operating duty ratio.

(e) In the last chapter passive component design technique is discussed especially for PV dominated microgrid. The capacitor selection procedure is proposed for achieving error free MPPT operation from PV using simple P&O algorithm. The capacitor selection procedure also ensures less circuit delay from system point of view. In this chapter inductor selection criteria is also mentioned for achieving faster microgrid response. This helps BDC circuit to act quickly during mode changeover and ensures stable DC link voltage for all disturbances.

Therefore, the current study is important for finalizing high efficiency topology of BDC especially for microgrid and EV application. This work also provides system passive component selection method for faster response and better utilization of PV power.

8.2. Future Works

The future works which are necessary to investigate in the continuation of this current work are

(a) The stability of DC/AC/hybrid microgrid using BDC under sudden disturbance from source side or load side or both needs to be investigated. The implementation of exact higher order model of BDC is a challenge in microgrid stability issue.

(b) Slow response time from BDC as well as microgrid impacted on frequent line tripping of grid connected microgrid. This frequent tripping during mismatch events needs to be investigated. How the system response time impacted on the stability and relevant guideline needs to be explored.

(c) Internal stability of AC/DC microgrid using BDC needs to be investigated.

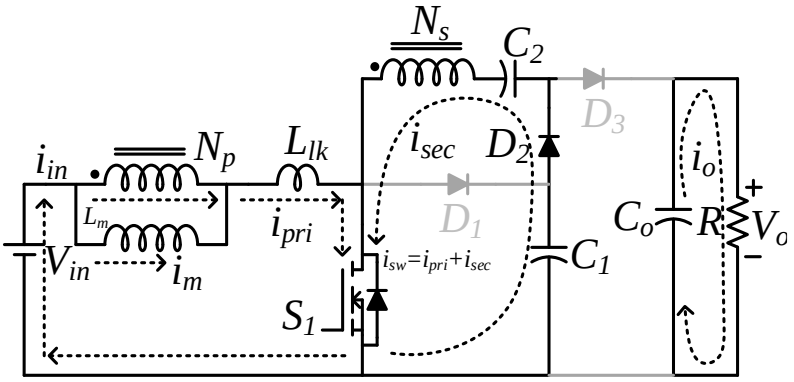
Appendix

1. *Detailed Derivation and Important circuit*
2. *Programme File, DSP and LabVIEW FPGA*

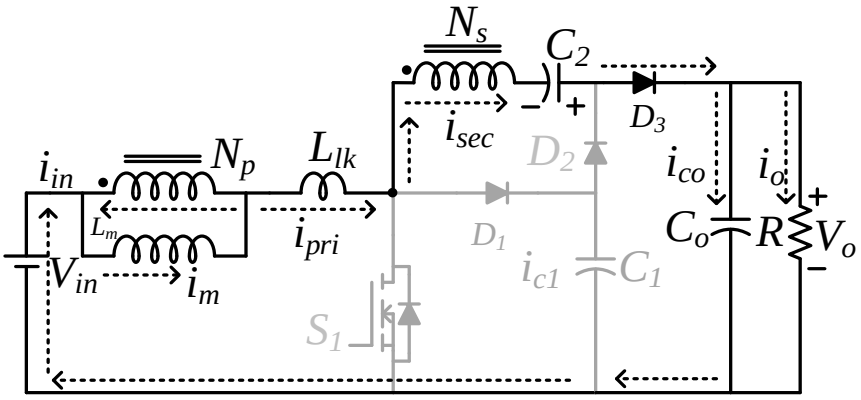
Derivations:

Chapter-3

Voltage Gain Derivation: S_1 is the main switch of the proposed topology. When S_1 is ON energy is stored in the magnetizing inductance.



(a)



(b)

Fig. A.1 Coupled inductor based generalized boost converter circuit for (a) ON time (b) OFF time.

The voltage equations from Fig. A.1 (a) are

$$v_{dc} = v_{L1} + v_{Lk} \tag{A.1}$$

Where, $v_{Lk} = (1-k)v_{dc}$ and $k = \dfrac{L_m}{L_m + L_{Lk}}$

Therefore, $v_{L1} = kv_{dc}$, $v_{L2} = nkv_{dc}$ (A.2)

$$v_{L2} + v_{c1} = v_{c2} \tag{A.3}$$

$$nkv_{dc} + v_{c1} = v_{c2} \tag{A.4}$$

During OFF time of S_1 the voltage equation from the circuit

$$v_{dc} + v_{L1} + v_{Lk} = v_{c1} \tag{A.5}$$

$$v_{dc} + v_{L1} + (1-k)v_{dc} = v_{c1} \tag{A.6}$$

$$v_{L1} = v_{c1} + (k-2)v_{dc} \tag{A.7}$$

Applying volt-sec balance in primary inductor L_1 capacitor voltage C_1 is derived i.e.

$$kdv_{dc} = [v_{c1} + (k-2)v_{dc}][1-d] \tag{A.8}$$

By solving this equation,

$$v_{c1} = v_{dc}\left[\frac{2d(k-1)+(2-k)}{1-d}\right] \tag{A.9}$$

Similarly, voltage across C_2 can be derived which is

$$nkv_{dc} + v_{dc}\left[\frac{2d(k-1)+(2-k)}{1-d}\right] = v_{c2} \tag{A.10}$$

$$v_{dc}\left[nk + \frac{2d(k-1)+(2-k)}{1-d}\right] = v_{c2} \tag{A.11}$$

Again, applying volt-sec balance at secondary inductor the output voltage equation is derived

$$nkdv_{dc} = [v_0][1-d] - [nk + \frac{2d(k-1)+(2-k)}{1-d}][1-d] \tag{A.12}$$

$$[v_0][1-d] = nkdv_{dc} + [nk + \frac{2d(k-1)+(2-k)}{1-d}][1-d] \tag{A.13}$$

By solving this equation output voltage equation is derived i.e.

$$\frac{v_0}{v_{in}} = \left[\frac{nk + 4d(k-1) + 2(2-k)}{1-d}\right] \tag{A.14}$$

For ideal coefficient of coupling k=1 the voltage gain of the boost stage can be derived as

$$\frac{v_0}{v_{in}} = \left[\frac{n+2}{1-d}\right] \tag{A.15}$$

Chapter-3

Loss calculation and theoretical efficiency determination:

As per suggestion, theoretical loss calculation in the proposed DC-DC converter at 100W is mentioned based on selected components summarized in Table-A1.

Theoretical loss calculation includes,

Table-A1

(a)	MOSFET Losses	Conduction loss Switching Loss
(b)	Diode Losses	Conduction Loss Switching Loss due to reverse recovery
(c)	Coupled Inductor Losses	Core loss Conduction loss
(d)	Capacitor losses	Conduction loss due to ESR

The detailed discussion of loss estimation for 100 W is mentioned below.

Diode Losses:

(i) Diode Conduction Loss (P_{dc})

IN5401 diode is used in designed prototype. The cut in voltage (Vγ) is 0.61 V. The dynamic on state resistance for the diode is calculated from datasheet which is 12mΩ.

Now, for calculation of diode conduction loss [1-2], RMS and average value of diode current is essential as mentioned in equation (1)

$$P_{dc} = i_{d(RMS)}^2 r_{d(on)} + v_\gamma i_{d(avg)} \quad \text{(A.16)}$$

**

[1] Application note *ST microelectronics* AN604. https://www.st.com/resource/en/application_note/cd00003894-calculation-of-conduction-losses-in-a-power-rectifier-stmicroelectronics.pdf.

[2] Mohan, N., Undeland, T. M., & Robbins, W. P. "*Power electronics: Converters, applications, and design*", New York: Wiley, 1995.

For diode D_1 the RMS current and average current is respectively mentioned in equation (A.17) and (A.18)

$$i_{d1(RMS)} \simeq \frac{n+2}{1-D} i_o \sqrt{D_b} \quad \text{Where } D_b=0.08 \text{ (from equation (13) for D=0.5, n=1} \quad \text{(A.17)}$$

$$\text{And } i_{d1(avg)} \simeq \frac{n+2}{1\text{-D}} i_0 \mathrm{D_b} \tag{A.18}$$

Similarly, for diode D_2 RMS current and average current is respectively mentioned in equation (A.19) and (A.20)

$$i_{d2(RMS)} \simeq \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(v_{c1}\sqrt{\frac{C_{eq}}{L_2}}\sin\left(\frac{2\pi}{T_s}t\right)\right)^2 dt} \tag{A.19}$$

For D=0.5 duty ratio and $t_r=DT_s$ the diode D_2 RMS current can be rewritten as

$$i_{d2(RMS)} \simeq \frac{v_{c1}}{2}\sqrt{\frac{C_{eq}}{L_2}} \text{ and average current } i_{d2(avg)} \simeq \frac{v_{c1}}{\pi}\sqrt{\frac{C_{eq}}{L_2}} \tag{A.20}$$

Similarly, for diode D_3 RMS current and average current is respectively mentioned in equation (A.21) and (A.22)

$$i_{d3(RMS)} \simeq i_0\sqrt{1\text{-}D_b\text{-}D} \tag{A.21}$$

$$i_{d3(avg)} \simeq i_0 \tag{A.22}$$

Conduction loss for D_1:

$$i_{d1(RMS)} \simeq 8.33\sqrt{0.08} = 2.35\text{A} \text{ and } i_{d1(avg)} \simeq 8.33X\,0.08 = 0.664\text{A}$$

$$\text{Thus, } P_{dc} = i_{d(RMS)}^2 r_{d(on)} + v_\gamma i_{d(avg)} = (0.06 + 0.405)\text{W} = 0.46\text{W}$$

Conduction loss for D_2:

$$i_{d2(RMS)} \simeq \frac{2.1}{2}\text{A} = 1.05\text{A} \text{ and } i_{d2(avg)} \simeq \frac{2.1}{\pi}\text{A} = 0.668\text{A}$$

$$\text{Thus, } P_{dc} = i_{d(RMS)}^2 r_{d(on)} + v_\gamma i_{d(avg)} = (0.013 + 0.407)\text{W} = 0.41\text{W}$$

Conduction loss for D_3:

$$i_{d3(RMS)} \simeq 1.38\sqrt{0.5} = 0.975\text{A} \text{ and } i_{d3(avg)} \simeq 1.38X\,0.5 = 0.69\text{A}$$

$$P_{dc} = i_{d(RMS)}^2 r_{d(on)} + v_\gamma i_{d(avg)} = (0.010 + 0.42)\text{W} = 0.43\text{W}$$

Total diode conduction loss=1.3W

(ii) *Diode Switching Loss* (P_{dsw}):

During turn OFF time due to reverse recovery there is a power loss [3-5]. This loss can be derived by taking ideal diode switching current waveform as shown in Fig. A2.

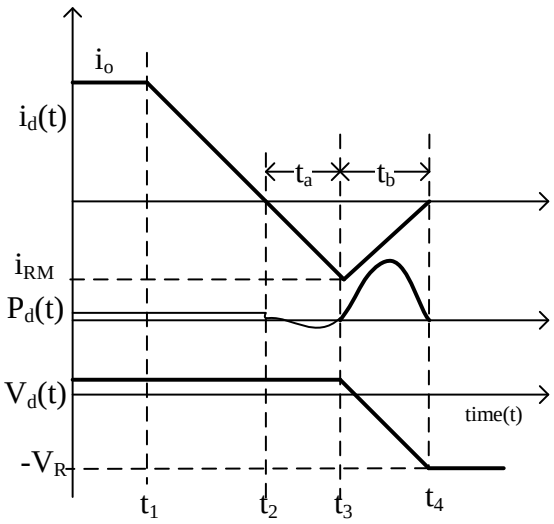


Fig. A2. Diode turn-OFF loss due to reverse recovery.

Peak reserve diode current (i_{RM}) can be determined from the data sheet which depends reverse blocking voltage.

The reverse recovery time (t_{rr})= $\frac{i_{RM}}{\frac{di_d}{dt}}(1+s)$,where s is the softness factor= $\frac{t_b}{t_a}=\frac{Q_b}{Q_a}$, $t_{rr}=t_a+t_b$

Total reverse recovery charge (Q_{rr})=Q_a+Q_b= $\frac{1}{2}t_{rr}i_{RM}$

The switching loss in diode can be derived

$$(P_{dsw})=\frac{1}{T_{sw}}\int_{t_1}^{t_4} v_d(t)i_d(t)dt \approx \frac{v_{d\max}i_{RM}t_b}{6} f_{sw} = \frac{v_R i_{RM} Q_b}{3} f_{sw} \quad \text{(A.23)}$$

Where $V_{dmax}=V_R$=Reverse diode voltage or blocking voltage.

**

[3] Application note *ST* microelectronics AN5028.

https://www.st.com/resource/en/application_note/dm00380483-calculation-of-turnoff-power-losses-generated-by-a-ultrafast-diode-stmicroelectronics.pdf.

[4] F. Casanellas, "Losses in PWM inverters using IGBTs," in *IEE Proceedings - Electric Power Applications*, vol. 141, no. 5, pp. 235-239, Sept. 1994.

[5] O. Al-Naseem, R. W. Erickson and P. Carlin, "Prediction of switching loss variations by averaged switch modeling," *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, New Orleans, LA, USA, 2000, pp. 242-248 vol.1.

Switching loss for diode D_1

V_R=24V, i_{RM}=0.2μA from datasheet for 24 volts. Change of diode current (D_1) is same as change in magnetising inductance current in the primary winding of coupled inductor.

$$\frac{di_{d1}}{dt} = \frac{di_{Lm}}{dt} = \frac{12}{44}\text{V/μSec} = 0.27\text{V/μSec}$$

The softness factor (S<1) can be found from datasheet which is 0.3

Thus, $t_{rr} = \frac{i_{RM}}{\frac{di_{d1}}{dt}}(1+s) = 0.96\mu\text{Sec}$

$$Q_{rr} \cong \frac{1}{2} t_{rr} i_{RM} = 0.096\text{nC} \text{ and } Q_b = \frac{Q_{rr}}{\left(1+\frac{1}{s}\right)} = \frac{Q_{rr}}{4.33} = 0.022\text{pC}$$

Thus, the switching loss (P_{d1sw}) = $\frac{v_{d\max} i_{RM} t_b}{6} f_{sw} = \frac{v_R i_{RM} Q_b}{3} f_{sw} = \frac{24 \times 0.2 \times 0.022 \times 50}{3} \times 10^{-15}\text{W}$

=0.0018pW

Switching loss for diode D_2

V_R=48V, i_{RM}=0.5μA from datasheet for 48 volt. Change of diode current (D_2) is same as change in secondary inductance current of coupled inductor.

$$\frac{di_{d2}}{dt} = \frac{di_{L\sec}}{dt} = \frac{24}{8.2}\text{V/μSec} \approx 2.926\text{V/μSec}$$

The softness factor (S<1) can be found from datasheet which is 0.5

Thus, $t_{rr} = \frac{i_{RM}}{\frac{di_{d2}}{dt}}(1+s) = 0.253\mu\text{Sec}$

$$Q_{rr} \cong \frac{1}{2} t_{rr} i_{RM} = 0.063\text{pC} \text{ and } Q_b = \frac{Q_{rr}}{\left(1+\frac{1}{s}\right)} = \frac{Q_{rr}}{3} = 0.0211\text{pC}$$

Thus, the switching loss (P_{d2sw}) = $\frac{v_{d\max} i_{RM} t_b}{6} f_{sw} = \frac{v_R i_{RM} Q_b}{3} f_{sw} = \frac{48 \times 0.5 \times 0.0211 \times 50}{3} \times 10^{-15}\text{W}$

=0.0844pW

Switching loss for diode D_3

V_R=48V, i_{RM}=0.5μA from datasheet for 48 volts. Change of diode current (D_2) is same as change in secondary inductance current of coupled inductor.

$$\frac{di_{d3}}{dt} = \frac{di_{L\sec}}{dt} = \frac{24}{8.2}\text{V/μSec} \approx 2.926\text{V/μSec}$$

The softness factor (S<1) can be found from datasheet which is 0.5

Thus, $t_{rr}=\frac{i_{RM}}{\frac{di_{d3}}{dt}}(1+s)$=0.253µSec

$Q_{rr} \cong \frac{1}{2} t_{rr} i_{RM}$ =0.063pC and $Q_b = \frac{Q_{rr}}{\left(1+\frac{1}{s}\right)} = \frac{Q_{rr}}{3} = 0.0211\text{pC}$

Thus, the switching loss (P_{d2sw}) = $\frac{v_{d\max} i_{RM} t_b}{6} f_{SW} = \frac{v_R i_{RM} Q_b}{3} f_{SW} = \frac{48 \times 0.5 \times 0.0211 \times 50}{3} \times 10^{-15}$W

=0.0844pW

Therefore, total diode conduction and switching loss=1.32W

MOSFET Losses:

Total MOSFET losses [6-7] can be written as

$$P_{MOSFET} \cong i^2_{SW(RMS)} r_{d(on)} + \frac{v_{sw\max} i_{sw\max} f_{sw}}{6}\left(t_r + t_f\right) \quad \text{(A.24)}$$

Switching voltage stress (V_{swmax}) of the MOSFET is 24V and the dynamic 'on' state resistance of MOSFET at this condition is 35mΩ.

The switch RMS current is $\approx \frac{(n\text{D}+n+2)\sqrt{\text{D}}}{(1\text{-D})} i_o \sqrt{1+\frac{1}{3}\left(\frac{\Delta i_m}{i_o}\right)^2}$ =6.2A

The rise time (t_r) and fall time (t_f) can be calculated from MOSFET datasheet which are 60nSec and 45nSec respectively.

The maximum switch current (i_{swmax}) =9.1A

$P_{MOSFET} \cong i^2_{SW(RMS)} r_{d(on)} + \frac{v_{sw\max} i_{sw\max} f_{sw}}{6}\left(t_r + t_f\right)$ =1.34+0.1911=1.53W

Therefore, total MOSFET conduction and switching loss=1.53W

**

[6] T. Nag, S. B. Santra, A. Chatterjee, D. Chatterjee and A. K. Ganguli, "Fuzzy logic-based loss minimisation scheme for brushless DC motor drive system," in *IET Power Electronics*, vol. 9, no. 8, pp. 1581-1589, 29 6 2016.

[7] R.W.Erickson and D.Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA, Kluwer, 2001.

Coupled Inductor Core losses and copper losses:

Core Loss:

Core loss is calculated form designed core parameter [7] (PQ core), A_g=1.61cm^2, l_m=7.47cm.

Change of flux density (dB) = $\frac{v_{in}DT_s}{nA_g}$ =0.0298T

The power density (Watt/cm^3) can be calculated from datasheet [7] of core material which in this case is 0.03Watt/cm^3.

Thus, the core loss (P_c) = (Watt/cm^3) ($A_g l_m$) =0.03X1.61X7.47 Watt=0.36 Watt.

** Steinmetz's equation can also be used for calculating core loss.

Copper Loss:

The resistance of primary winding and secondary winding is respectively18mΩ and 92mΩ.

Thus, copper loss for primary winding is ($P_{cu\text{-}pri}$) = $i_{pri\_RMS}^2 r_{pri}$

And copper loss for secondary winging is ($P_{cu\text{-}sec}$) = $i_{sec\_RMS}^2 r_{sec}$

The primary winding RMS current can be calculated from the simplified waveform as shown in Fig. A.3.

The x value of the primary current waveform is

$$x \cong \frac{n+2}{1-D} i_o \tag{A.25}$$

The RMS current of primary winding and secondary winding of coupled inductor are

$$i_{pri(RMS)} = \sqrt{x^2 + x\left(x\text{-}I_{pri\_min}\right)(1\text{-}D) + \frac{\left(x\text{-}I_{pri\_min}\right)^2}{3}(1\text{-}D) + \frac{v_{c1}}{\pi}\sqrt{\frac{C_{eq}}{L_2}}\left(1\text{-}\cos\left(2\pi D\right)\right) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{A.26}$$

$$i_{sec(RMS)} = \sqrt{i_{sec}^2 \times (1\text{-}D\text{-}D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{A.27}$$

From the charge balance of capacitor currents as shown in Fig. A.3. the D_b value can be derived theoretically which is

$$D_b = \frac{v_{c1}D}{2\pi i_o}\sqrt{\frac{C_{eq}}{L_2}}\left(1\text{-}\cos\left(2\pi D\right)\right) \times \left(\frac{1\text{-}D}{n+2}\right) \tag{A.28}$$

Similarly, from capacitor current switching waveform the RMS value of capacitor currents are derived

$$i_{c_2(RMS)} = \sqrt{i_{sec}^2 \times (1\text{-}D\text{-}D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{A.29}$$

$$i_{c_1(RMS)} = \sqrt{I_{pri\_min}^2 \times D_b + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2}D\text{-}\frac{\sin 4\pi D}{4\pi}} \tag{A.30}$$

$$i_{c_o(RMS)} = \sqrt{i_o^2 \times \left(D\text{+}D_b\right) + \left(i_{sec}\text{-}i_o\right)^2\left(1\text{-}D\text{-}D_b\right)} \tag{A.31}$$

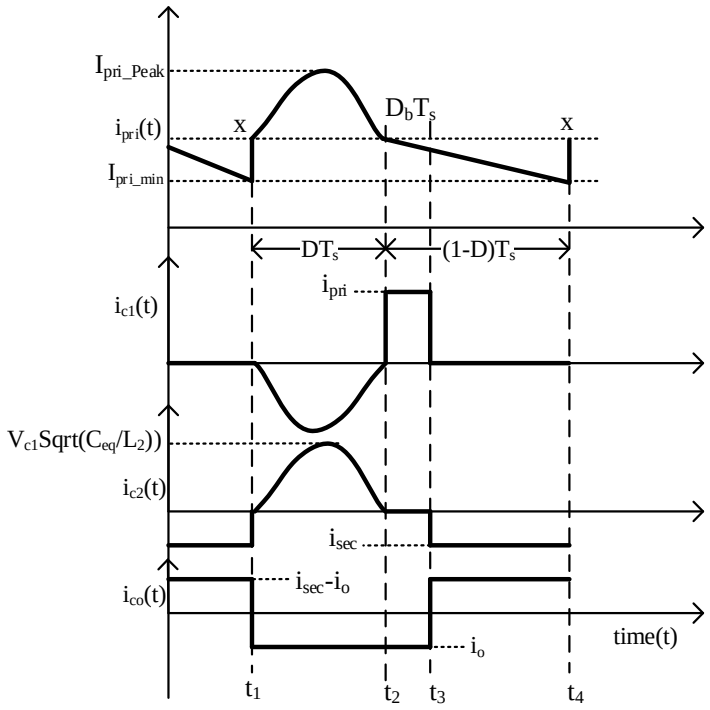


Fig.A.3. Simplified current waveform of capacitors and primary current of coupled inductor.

The average value of load current (i_o) is 1.388A and minimum value of primary current (I_{pri_min}) is 4.2A.

By putting all the values in equation (A.26) and (A.27) the RMS current of primary winding is 9.88A

D_b value is calculated from equation (A.28) which is 0.08 for D=0.5 and RMS current of secondary winding is 2.97A derived from equation (A.27).

Therefore, copper loss in primary winding is $P_{cu\_pri}=9.88^2X0.018W=1.75W$

Copper loss in the secondary winding is $P_{cu\_sec}=2.97^2X0.024W=0.21W$

Thus, total winding loss= (1.75+0.21+0.36) W=2.32W

Capacitor ESR loss:

The ESR value can be estimated from datasheet tan (δ) and voltage stress information. The ESR for capacitor C_1 is 0.005**Ω**, for C_2 is 0.046**Ω** and for C_o is 0.004**Ω**. The RMS current for capacitors C_1, C_2 and C_o are respectively calculated from equation (A.29), (A.30) and (A.31). The RMS current values for capacitors C_1, C_2 and C_o are respectively 2.57A, 2.97A and 2.16A.

Thus, ESR loss for capacitor C_1=0.033W, ESR loss for capacitor C_2=0.40W, ESR loss for capacitor C_o=0.018W

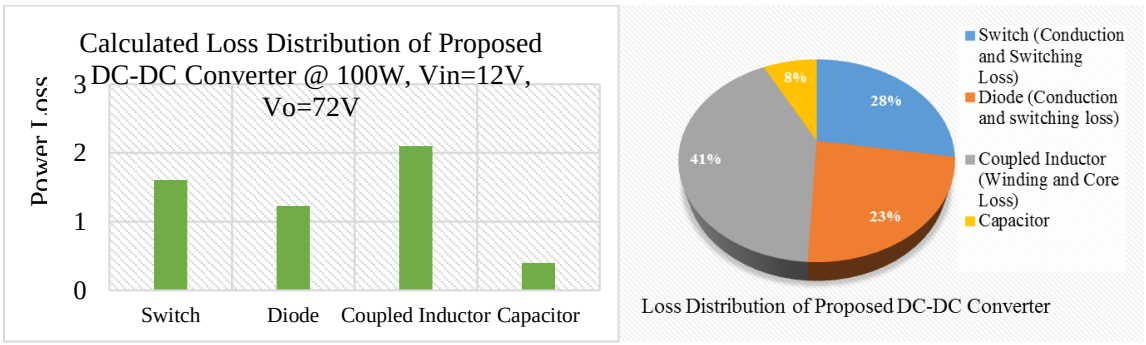
Total capacitor ESR loss=0.451W

Therefore, total loss distribution of the proposed converter for 100W, where V_{in}=12V, V_{out}=72V, D=0.5, *n*=1 and R_L=51.84**Ω**.

Loss Component	Value (W)	(%)	Value (W)
Diode conduction loss	1.30W	**23%**	**1.32W**
Diode Switching loss	0.02W		
Diode Total Loss			
MOSFET Loss (Conduction+Switching)		**27.2%**	**1.53W**
Winding Core loss	0.36W	**41.28%**	**2.32W**
Winding Copper loss	1.96W		
Total winding loss			
Capacitor ESR losses		**8%**	**0.451W**
Total estimated loss of proposed converter			**5.62W**

Thus, estimated efficiency of the proposed converter at 100W is 94.37% and loss distribution is shown in Fig. 3.

The measured efficiency is **93.2%** at the same 100W condition using power quality analyser APLAB-PQA2100E. The difference between theoretical estimated efficiency and practical measurement is due to ignorance of different circuital parameters like skin effect, proximity effect, exact transient time for switching events etc. Current waveforms are also considered as ideal for theoretical calculation which create differences in measured and calculated efficiency.



(a). (b)

Fig. A.4. (a) & (b) Loss distribution of the proposed DC-DC converter.

Similarly, estimated efficiency is calculated form theoretical loss and compared to measured efficiency at different power points through power quality analyser APLAB-PQA2100E as shown in Fig. A.5.

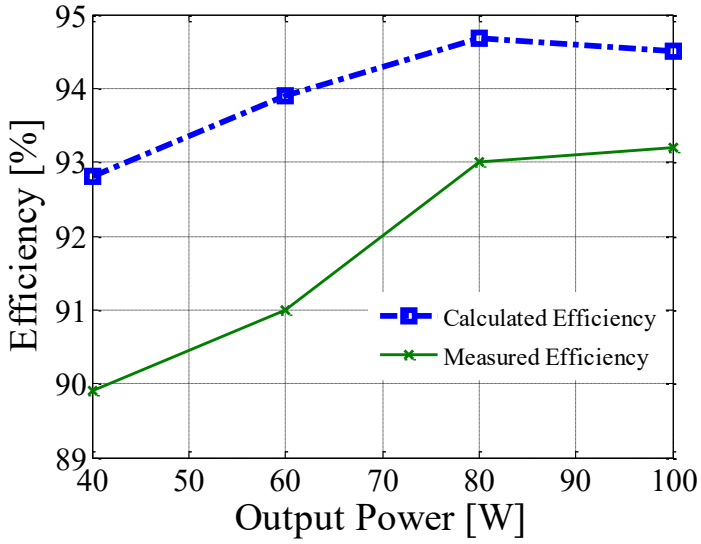


Fig. A.5. Estimated and measured efficiency of the proposed DC-DC converter.

Appendix-B

Chapter-6

Loss Analysis and Sample Calculation of Coupled Inductor based BDC with RIRC

The RMS currents of active switches, coupled inductor windings, capacitors are required to estimate losses of the proposed converter. However, different parameters vary based on operating conditions and in theoretical loss estimation these effects are ignored like skin effect, proximity effect, transient time for switching events etc. Current waveforms are also considered as ideal for theoretical calculation.
As per suggestion, theoretical loss calculation of the proposed BDC converter in both modes are performed based on selected components at 250W. The loss distribution is added as pie graph in the revised manuscript.
Theoretical loss calculation includes,

(a)	MOSFET Losses	Conduction loss Switching Loss
(b)	Coupled Inductor Losses	Core loss Conduction loss
(c)	Capacitor losses	Conduction loss due to ESR

Loss Calculation of boost mode at 250W:

MOSFET Losses:

Conduction Loss: The conduction loss of MOSFET switch can be easily determined by using equation (B.1)

$$P_{MOSFET} \cong i_{SW(RMS)}^2 r_{d(on)} \tag{B.1}$$

For S_1:
The RMS current for switch S_1 in boost mode is

$$i_{S1\text{-}RMS} \approx \frac{2+n+D}{(2+2n)\sqrt{D}} i_{LV} \tag{B.2}$$

For *n=1* and D=0.5 the S_1 RMS current is 6.44A. Therefore, the conduction loss when switch on state resistance is 0.075Ohm is

$P_{S1\_conduction} \approx 6.444^2 \times 0.075 = 3.11W$

For S_2:
The RMS current for switch S_2 in boost mode is

$$i_{S2\text{-}RMS} = \frac{2+2n}{1-D}\sqrt{D_b} i_{HV} \text{ Where, } D_b = \frac{v_{c1} D}{4\pi i_{HV}} \sqrt{\frac{C_{eq}}{L_2}} (1-\cos(2\pi D)) \times \left(\frac{1-D}{n+1}\right) \tag{B.3}$$

Putting all values i.e. D_b=0.08, *n=1* D=0.5 the RMS current for S_2 is calculated as1.47A. Thus, the conduction loss of switch S_2 is

$P_{S2\_conduction} \approx 1.47^2 \times 0.075 = 0.162W$

For S_3:

The RMS current for switch S_3 in boost mode is

$$i_{S3\text{-RMS}} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(v_{ceq}\sqrt{\frac{C_{eq}}{L_2}}\sin\frac{2\pi}{T_s}t\right)^2 dt} \quad \text{(B.4)}$$

Putting all values i.e. *n=1* D=0.5 the RMS current for S_3 is calculated as 3.15 A. Thus, the conduction loss of switch S_3 is

$P_{S3\_conduction} \approx 3.15^2 \times 0.075 = 0.744\text{W}$

For D_1:

The RMS current for switch D_1 in boost mode is

$$i_{D1\text{-RMS}} = \frac{i_{Lm}}{n}\sqrt{1-D} \text{ and } i_{D1\text{-Avg}} = \frac{i_{Lm}}{n}(1-D) \quad \text{(B.5)}$$

IN5401 diode is used in designed prototype. The cut in voltage (Vγ) is 0.61 V. The dynamic on state resistance for the diode is calculated from datasheet which is 12mΩ.

Now, for calculation of diode conduction loss, RMS and average value of diode current is essential as mentioned in equation (B.6)

$$P_{dc} = i_{d(RMS)}^2 r_{d(on)} + v_\gamma i_{d(avg)} \quad \text{(B.6)}$$

**Note:

(a) Application note *ST microelectronics* AN604.
https://www.st.com/resource/en/application_note/cd00003894-calculation-of-conduction-losses-in-a-power-rectifier-stmicroelectronics.pdf.

(b) Mohan, N., Undeland, T. M., & Robbins, W. P. "*Power electronics: Converters, applications, and design*", New York: Wiley, 1995.

$$P_{dc} = i_{d(RMS)}^2 r_{d(on)} + v_\gamma i_{d(avg)} = (0.045 + 0.76)\text{W} = 0.80\text{W}$$

For S_4:

The RMS current for switch S_6 in boost mode is

$$i_{S4-\text{RMS}} \approx i_{\text{Lm-min}}\sqrt{(1-D)} \quad \text{(B.7)}$$

Putting all values i.e. *n=1* D=0.5 and i_{Lmin}=1.567 A, the RMS current for S_4 is calculated as 1.11 A. Thus, the conduction loss of switch S_6 is

$P_{S4\_conduction} = 1.11^2 \times 0.075 = 0.092\text{W}$

For S_5:

The RMS current for switch S_5 in boost mode is

$$i_{S5\text{-RMS}} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(v_{ceq}\sqrt{\frac{C_{eq}}{L_2}}\sin\frac{2\pi}{T_s}t\right)^2 dt} \quad \text{(B.8)}$$

Putting all values i.e. *n=1* D=0.5 the RMS current for S_5 is calculated as 3.15 A. Thus, the conduction loss of switch S_5 is

$P_{S5\_conduction} \approx 3.15^2 \times 0.075 = 0.744\text{W}$

Thus, total conduction loss

$P_{conduction} = 3.11 + 0.162 + 0.744 + 0.80 + 0.092 + 0.744 = 5.652\text{W}$

The switching loss is negligible due to soft switching of all active switches. Therefore, the switching loss is considered as zero.

Therefore, total MOSFET loss is 5.652W

Coupled Inductor Core losses and copper losses:

Core Loss:

Core loss is calculated form designed core parameter [1] (PQ core), A_g=1.61cm^2, l_m=7.47cm.

Change of flux density (dB) $= \frac{V_{in} DT_s}{nA_g}$ =0.0298T

The power density (Watt/cm^3) can be calculated from datasheet [1] of core material which in this case is 0.03Watt/cm^3.

Thus, the core loss (P_c) = (Watt/cm^3) ($A_g l_m$) =0.03X1.61X7.47 Watt=0.36 W.

** Steinmetz's equation can also be used for calculating core loss.

Reference: [1] R.W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 3rd edition. Springer, USA, Aug. 2020.

Copper Loss:

The resistance of primary winding and secondary winding is respectively 52mΩ and 265.7mΩ.

Thus, copper loss for primary winding is ($P_{cu\text{-}pri}$) = $i_{pri\_RMS}^2 r_{pri}$

The primary winding RMS current can be calculated using equation (B.9),

$$i_{pri(RMS)} = \sqrt{\left[(x^2 + x(x - I_{pri\_min})(1-D) + \frac{(x - I_{pri\_min})^2}{3}(1-D) + \frac{v_{c1}}{\pi}\sqrt{\frac{C_{eq}}{L_2}}(1-\cos(2\pi D)) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2} D - \frac{\sin 4\pi D}{4\pi}) \right]} \quad \text{(B.9)}$$

Where x=6.92 A, I_{pri_min}=2.71 A and D=0.5. The RMS value of winding primary current is 7.8A.

Thus, primary winding copper loss= 3.21W.

Similarly, the winding-2 RMS current can be calculated using equation (B.10)

$$i_{C_2(RMS)} = i_{winding\text{-}2\ (RMS)} = \sqrt{i_{HV}^2 \times (1-D-D_b) + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2} D - \frac{\sin 4\pi D}{4\pi}} \quad \text{(B.10)}$$

The RMS value of the current is 1.38 A. Therefore, the winding-2 copper loss=0.5W.

Lastly, winding-3 RMS current can also be calculated using equation (B.11)

$$i_{C_3(RMS)} = i_{C_4(RMS)} = i_{winding\text{-}3(RMS)} = \sqrt{i_{HV}^2 \frac{1-D}{3D}(4\text{-}D)} \quad \text{(B.11)}$$

Winding-3 RMS current is 0.7020 A. Therefore winding-3 copper loss is 0.1 W.

Total conduction loss of coupled inductor is = (0.1+0.5+3.21) W=3.81W

Core loss of the coupled inductor is =0.36W

Total Winding loss= 4.17 W

Capacitor ESR losses:

The ESR value can be estimated from datasheet tan (δ) and voltage stress information. The ESR for capacitor C_1 is 0.045Ω. For C_2, C_3, and C_4 it is 0.046Ω. ESR of C_{HV} is 0.040Ω. The RMS current for capacitors C_2, C_3 and C_4 are respectively calculated from equation (B.10) and (B.11). The capacitor C_1 and C_{HV} RMS current can also be determined from equation (B.12) and (B.13)

$$i_{C_1(RMS)} = \sqrt{I_{pri\_min}^2 \times D_b + \frac{v_{c1}^2}{2\pi^2}\frac{C_{eq}}{L_2} D - \frac{\sin 4\pi D}{4\pi}} \quad \text{(B.12)}$$

$$i_{c_{HV}(RMS)} = \sqrt{i_{HV}^2 \times (D+D_b) + (i_{winding-2} - i_{HV})^2 (1-D-D_b)} \quad \text{(B.13)}$$

The RMS current values for capacitors C_1, C_2, C_3, C_4 and C_{HV} are respectively 1.52A, 1.38A, 0.70A, 0.70A and 1.52A.

Thus, ESR loss for capacitor C_1=0.103W

ESR loss for capacitor C_2=0.1W

ESR loss for capacitor C_3, C_4=0.022W

ESR loss for capacitor C_{HV}=0.0924W

Total capacitor ESR loss=0.339W

Therefore, total loss distribution of the proposed converter in boost mode at 250W, where V_{LV}=48V, V_{HV}=380V, D=0.5, *n*=1 and R_L=578 Ω is mentioned in Table-B1.

Table-B1

Loss Component	Value (W)	(%)	Value (W)
MOSFET+ Diode Loss (Conduction +Switching)		**55.62%**	**5.652W**
S_1	3.11W	**30.61%**	
S_2	0.162W	**1.59%**	
S_3	0.744W	**7.32%**	
S_4	0.092	**0.90%**	
S_5	0.744W	**7.32%**	
D_1	0.80W	**7.87%**	
Winding Core loss	0.36W	**41%**	**4.17W**
Winding Copper loss	3.81W		
Total winding loss			
Capacitor ESR losses		**3.33%**	**0.339W**
Total estimated loss of proposed converter			**10.16W**

Similarly, loss distribution of the proposed BDC in buck mode is calculated by RMS currents equations at 250 W where V_{LV}=48V, V_{HV}=380V, D=0.5, *n*=1 and R_L=9.216 Ω. However, the current expression for five switches and one diode for buck mode of operation is mentioned here. These equations are used for calculating the theoretical power loss for the proposed BDC under buck operating mode.

In the buck mode operation of proposed BDC, the switch current stress of S_1 is same as peak magnetising current as it only conducts during freewheeling time like conventional buck converter.

$$i_{S1\_Peak} = i_{S2\_Peak} = i_{Lm\_Peak} \quad \text{(B.14)}$$

Similarly, the peak current of high voltage side switch S_4 is

$$i_{S6\_Peak} \cong \frac{D n V_{LV}}{(1-D) L_2} (t_3 - t_2) \quad \text{(B.15)}$$

Where, t_3-t_2 =D_cT_s

The average magnetizing current during buck mode of operation is

$$i_{Lm} = \frac{n+1-nD}{n+1} i_{LV} \text{ and } \Delta i_{Lm} = \frac{v_{LV}(1-D)T_S}{L_m} \quad \text{(B.16)}$$

The RMS values of switch currents during buck mode are derived from operating current waveform as mentioned in the chapter 6.

$$i_{S1-RMS} = i_{Lm\text{-}min}\sqrt{1-D+\frac{2}{i_{Lm\text{-}min}}+\left(\frac{\Delta i_{Lm}}{i_{Lm\text{-}min}}\right)^2} \quad \text{(B.17)}$$

$$i_{S2\text{-}RMS} = \frac{D}{6(n+1)}\sqrt{\frac{5D}{3}}i_{LV} \text{ and } i_{S3\text{-}RMS} = \frac{D\sqrt{1-D}}{6\sqrt{3}(n+1)}i_{LV} \quad \text{(B.18)}$$

$$i_{D1\text{-}RMS} = \frac{nD\sqrt{D}}{2\sqrt{3}(n+1)}i_{LV} \text{ and } i_{S5\text{-}RMS} = \frac{nD\sqrt{1\text{-}D}}{2\sqrt{3}(n+1)}i_{LV} \quad \text{(B.19)}$$

$$i_{S4\text{-}RMS} = \frac{i_{Lm\text{-}min}}{n}\sqrt{D+\frac{D}{3}\left(\frac{\Delta i_{Lm}}{i_{Lm\text{-}min}}\right)} \quad \text{(B.20)}$$

The distribution is mentioned in Table-II.

Table-II

Loss Component	Value (W)	(%)	Value (W)
MOSFET Loss (Conduction +Switching)		**35.75%**	**4.29W**
S_1	1.8W	**15%**	
S_2	0.29W	**2.41%**	
S_3	0.586W	**4.8%**	
S_4	0.37W	**3.0%**	
S_5	0.063W	**5.25%**	
D_1	0.628W	**5.0%**	
Winding Core loss	0.37W	**53.91%**	**6.47W**
Winding Copper loss	6.1W		
Total winding loss			
Capacitor ESR losses	1.27W	**10.4%**	**1.27W**
Total estimated loss of proposed converter			**12.03W**

The loss distribution pie graph for boost and buck mode at 250W are shown in Fig. B1 and Fig. B2 respectively.

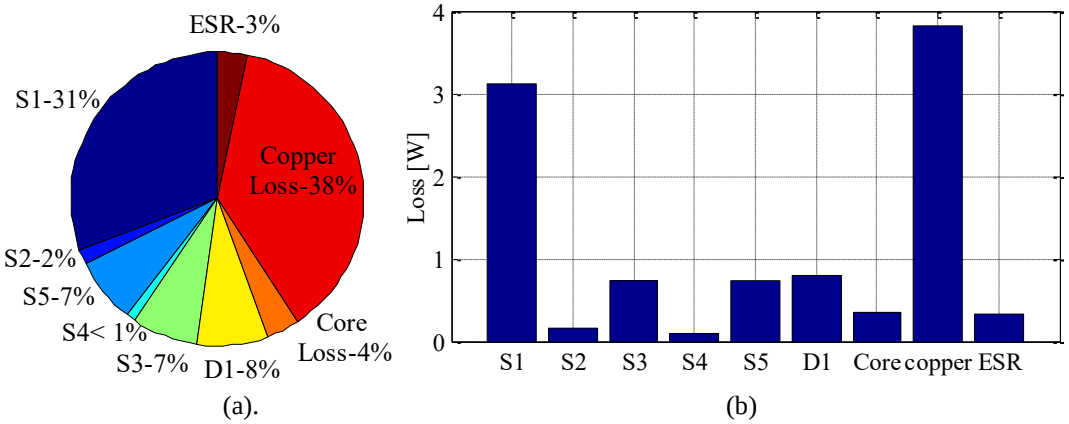
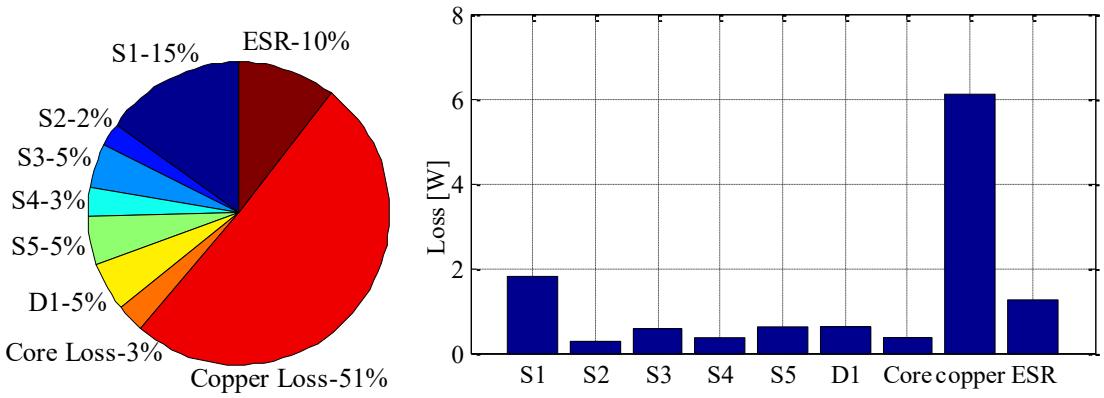


Fig. B1. Loss distribution of proposed BDC in boost mode (a) % share of loss (b) individual component wise loss.



(a). (b)

Fig. B2. Loss distribution of proposed BDC in buck mode (a) % share of loss (b) individual component wise loss.

Chapter-7

Derivation for ripple power:

Ripple Power is derived from inverter node voltage (V_{AB}) and line inductance (L_i) as shown in Fig. B3.

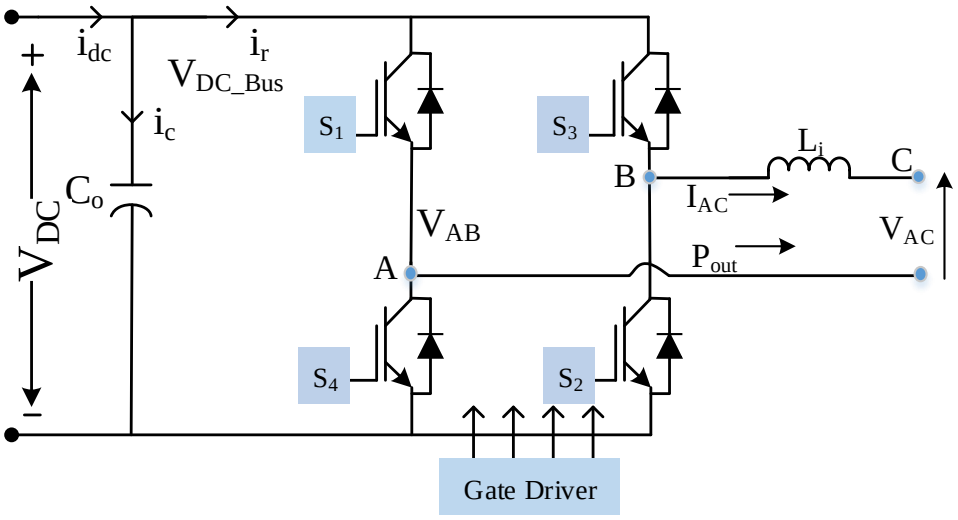


Fig. B3. Single-phase full-bridge inverter.

Let the node voltage $V_{AB}=V_m \sin \omega t$ and $I_{AC}=I_m \sin(\omega t-\varphi)$ where ω is grid frequency and φ is phase angle difference between V_{AB} and I_{AC}.

Thus, the instantaneous power injected to the grid is $P_{out}=V_{AC}I_{AC}$

Now, $V_{AC}=V_{AB}-V_L = V_m \sin \omega t - L_i \dfrac{di_{ac}}{dt} = V_m \sin \omega t - \omega L_i I_m \cos(\omega t-\varphi)$ (B.21)

The output power can be subdivided into P_{av} and P_{ripple} where $P_{out}=P_{av}+P_{ripple}$

$P_{out}=V_{AC}I_{AC}$ (B.22)

=

$$\{V_m \sin \omega t - \omega L_i I_m \cos(\omega t-\varphi)\} I_m \sin(\omega t-\varphi) = V_m I_m \sin \omega t \sin(\omega t-\varphi) - \omega L_i I_m^2 \cos(\omega t-\varphi)\sin(\omega t-\varphi)$$

$$= \left(\frac{V_m I_m}{2}\right) 2\sin\omega t \sin(\omega t - \varphi) - \left(\frac{\omega L_i I_m^2}{2}\right) 2\cos(\omega t - \varphi)\sin(\omega t - \varphi)$$

$$= \left(\frac{V_m I_m}{2}\right)\cos\varphi - \left(\frac{V_m I_m}{2}\right)\cos(2\omega t - \varphi) - \left(\frac{\omega L_i I_m^2}{2}\right)\sin(2\omega t - 2\varphi)$$

$$= \left(\frac{V_m}{\sqrt{2}}\right)\left(\frac{I_m}{\sqrt{2}}\right)\cos\varphi - \left(\frac{V_m I_m}{2}\right)\cos(2\omega t - \varphi) - \left(\frac{\omega L_i I_m^2}{2}\right)\sin(2\omega t - 2\varphi) \quad \text{(B.23)}$$

$$= P_{av} + P_{ripple}$$

Where, $P_{av} = \left(\frac{V_m I_m}{2}\right)\cos\varphi$ and $P_{ripple} = -\left(\frac{V_m I_m}{2}\right)\cos(2\omega t - \varphi) - \left(\frac{\omega L_i I_m^2}{2}\right)\sin(2\omega t - 2\varphi)$

Now for low line inductance ripple power (P_{ripple}) can be written as

$$P_{ripple} = -\left(\frac{V_m I_m}{2}\right)\cos(2\omega t - \varphi) \quad \text{(B.24)}$$

Appendix-C

Gate Driver Hardware Circuit using IR2110

The gate driver for MOSFET based CIBDC is shown in Fig. C_1.

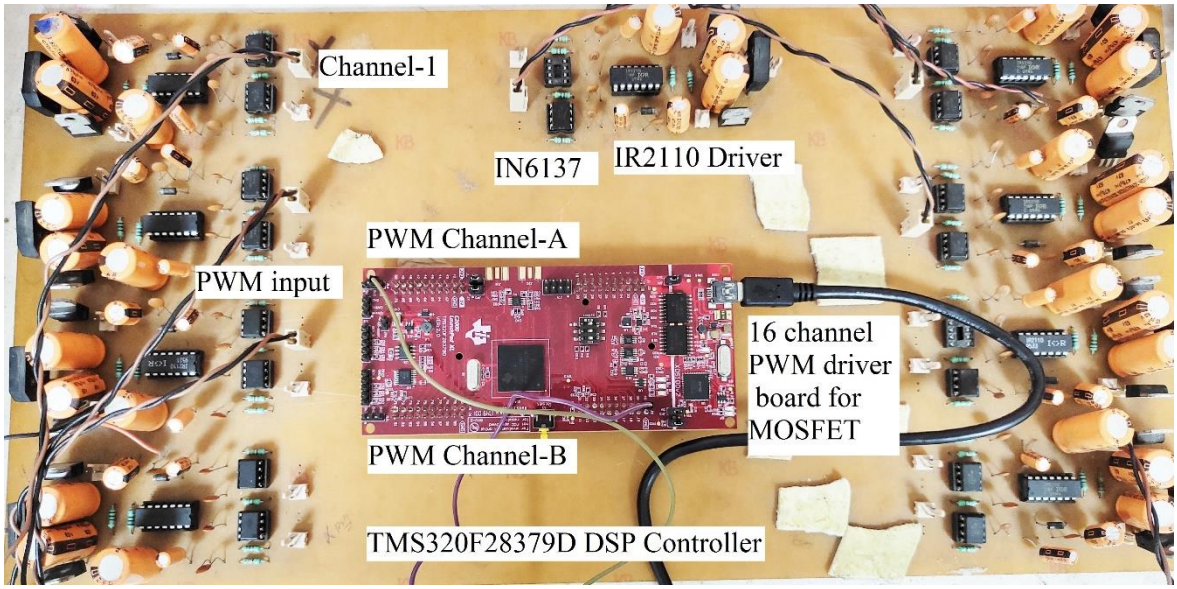


Fig. C1. 16 channel gate driver circuit using IR2110 and TMS320F28379D DSP board.

For closed loop control Lab-VIEW based NI-cRIO 9082 is used in this work. There are voltage sensor NI9225 (300V rms) and NI 9227 embedded current sensor is used for the control loop implementation. NI 9401 digital input/output module is used for PWM pulse generation as shown in Fig. C2.

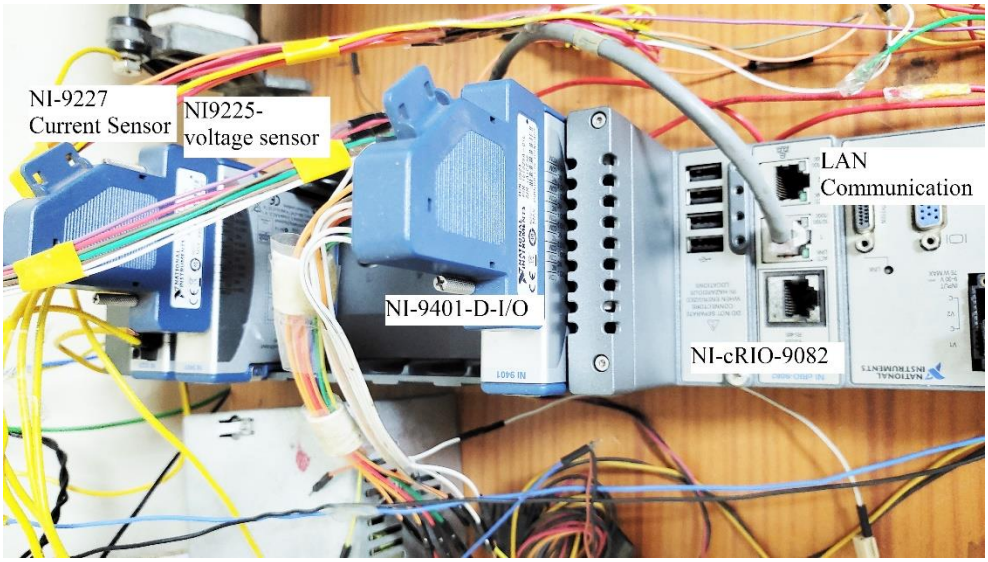


Fig. C2. NI-cRIO 9082 based controller with different sensors (NI 9225 and NI9227)

DSP Programme for Complementary Pulse with Dead time for Controlling BDC:

```
#include "math.h"
#include "cgen.h"
#include "c2000.h"
int MHZ=200;
#define _SYS_MHZ_ 200
int MEP_ScaleFactor;

static SIM_STATE tSim={0,0,0
,0,0,0,0,0,0,0,0,0,1,1,0,0,0,0,0,0};
SIM_STATE *sim=&tSim;
static INTERRUPT void cgMain()
{
static int _squareCnt1=0;
static int _squareCnt13=0;
  if ((++_squareCnt1 > 10000?(_squareCnt1>=20000?_squareCnt1=0,1:1):0))
    {GPBSET = 0x4L;}
  else
    {GPBCLEAR = 0x4L;};
  if ((++_squareCnt13 > 10000?(_squareCnt13>=20000?_squareCnt13=0,1:1):0))
    {GPBSET = 0x10L;}
  else
    {GPBCLEAR = 0x10L;};
  { long _duty32 = (long)16384*4;
    CMPA1 = (int)(_duty32>>15);
    CMPAHR1 = (int)((((_duty32&0x7FFF)*MEP_ScaleFactor)>>6)&0xFF00)+0x180;
```

```
  }
  CMPB1 = (int)(((long)16384*4)>>15);
  { long _duty32 = (long)16384*4;
    CMPA2 = (int)(_duty32>>15);
    CMPAHR2 = (int)((((_duty32&0x7FFF)*MEP_ScaleFactor)>>6)&0xFF00)+0x180;
  }
  CMPB2 = (int)(((long)16384*4)>>15);

  endOfSampleCount = TIMER2TIM;

}

void main()
{
  EALLOW;
  SYSPLLCTL1 = 0;
  CLKSRCCTL1 = 2;  //Internal Osc 1
  CLKSRCCTL2 = 0;  //Internal Osc 2
  SYSPLLMULT = 0x14;       // set PLL to 20xOSC = 200 MHZ
  SYSPLLCTL1 = 1;   // Enable PLL
  while(!(SYSPLLSTS&1));   // Wait for PLL lock
  { int divSel;
    for (divSel =63; divSel >= 0; divSel--)
      { SYSCLKDIVSEL = divSel;      // Ramp up freq
        SysCtlDelay(15);
      }
  }
```

```
SYSPLLCTL1 = 3;   // Use PLL
PERCLKDIVSEL = 0x10;
PCLKCR0 = 0x10020;
PCLKCR1 = 0x1;
PCLKCR2 = 0x3;
EDIS;
TBPRD1 = 0x3;
AQCTLA1 = 0x90;
AQCTLB1 = 0x600;
EALLOW;
TZCTL1 = 0x0;
TZSEL1 = 0x0;
DCACTL1 = 0x0;
DCBCTL1 = 0x0;
while (!SFO(1)) {}
if (MEP_ScaleFactor > 256) {MEP_ScaleFactor = 33;}
EALLOW;
HRCNFG1 = 0x2;
EDIS;
TBPRD2 = 0x3;
AQCTLA2 = 0x90;
AQCTLB2 = 0x600;
DBCTL2 = 0xc;
DBRED2 = 0x1;
DBFED2 = 0x1;
EALLOW;
TZCTL2 = 0x0;
```

```
 TZSEL2 = 0x0;
 DCACTL2 = 0x0;
 DCBCTL2 = 0x0;
 HRCNFG2 = 0x2;
 EDIS;
simInit( 0 );
 EALLOW;
 GPAMUX1 = 0x55;
 GPACSEL1 = 0x22220000;
 GPACSEL2 = 0x22222222;
 GPACSEL3 = 0x22222222;
 GPACSEL4 = 0x22222222;
 GPBDIR = 0x14;
 GPBCSEL1 = 0x22202022;
 GPBCSEL2 = 0x22222222;
 GPBCSEL3 = 0x22222222;
 GPBCSEL4 = 0x22222222;
 GPCCSEL1 = 0x22222222;
 GPCCSEL2 = 0x22222222;
 GPCCSEL3 = 0x22222222;
 GPCCSEL4 = 0x22222222;
 GPDCSEL1 = 0x22222222;
 GPDCSEL2 = 0x22222222;
 GPDCSEL3 = 0x22222222;
 GPDCSEL4 = 0x22222222;
 GPECSEL1 = 0x22222222;
 GPECSEL2 = 0x22222222;
```

```
  GPECSEL3 = 0x22222222;
  GPECSEL4 = 0x22222222;
  GPFCSEL1 = 0x22222222;
  GPFCSEL2 = 0x22222222;
  EDIS;
  startSimDsp();
  installInterruptVec(-2,7,&cgMain);
  TIMER2PRD = 0x2710; // 32-bit Timer Period Low
  TIMER2PRDH = 0x0; // 32-bit Timer Period High
  TIMER2TCR |= 0x4020; //Interrupt enable, Timer Reset
  EALLOW;
  PIECTRL = 1; // Enable PIE Interrupts
  EDIS;
  IER |= 0x2000; //CPU Interrupt enable
  resetInterrupts();
  enable_interrupts();  // Global Start Interrupts
  TBCTL1 = 0x1c32; // Start timer
  TBCTL2 = 0x1c36; // Start timer
  EALLOW;
  PCLKCR0 |= 0x80000; // Start all PWM timers
  EDIS;
  dspWaitStandAlone();
}
```

PWM generation through Lab-VIEW FPGA for one main switch.

Similar programme can be paralleled using Lab-VIEW FPGA as it is a parallel processor. The sample programme for 50 kHz 0.4 duty ratio is shown in Fig. C3.

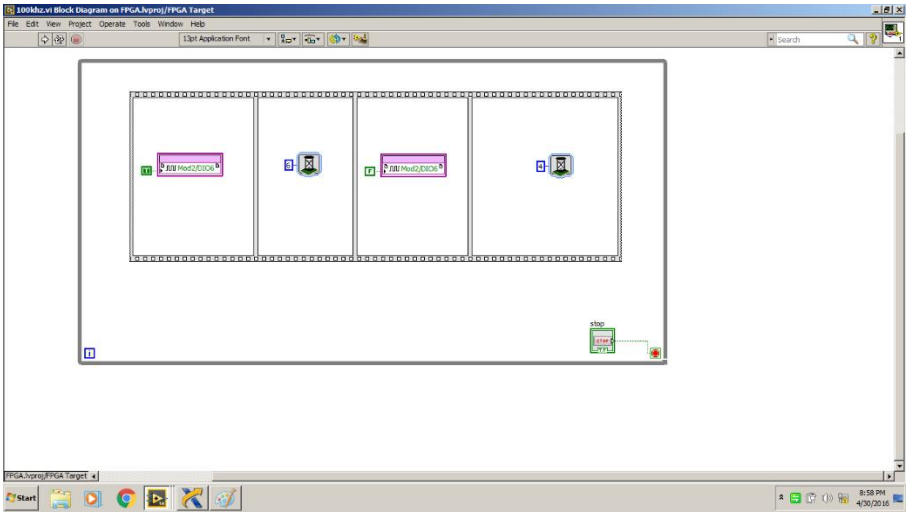


Fig. C3. Lab-VIEW FPGA graphical programming.