BACHELOR OF ENGINEERING IN MECHANICAL ENGINEERING EXAMINATION, 2022

(1st Year, 1st Semester)

ELECTRONICS

Time : Three hours Full Marks : 100

Answer any **two(2)** from **(a), (b) and (c):**

1. (a) i. Define Intrinsic and Extrinsic semiconductors with example.
   ii. Draw the Energy band diagram of p-n junction diode.
   iii. Define ripple factor of a rectifier.
   iv. What is thermal run-away?
   v.Explain the conduction mechanisms for an n- type semiconductor.
   vi.Define Intrinsic and Extrinsic semiconductors with example. [1+1+1+1+3+3]

(b) i. An ideal diode offers _____ resistance when forward biased and _____ resistance when it is reverse biased.

ii. Draw and explain the V-I characteristics of a p-n junction diode for both forward and reverse bias condition.

iii. What is forbidden energy gap? Explain.
iv. Explain the working principle of a Zener diode. [2+4+2+2]

(c) i. What is Fermi level? What happens to Fermi level when temperature is increased?
ii. Name the elements which are used as N-type impurities and P-type impurities.

iii. What do you mean by transition capacitance in PN-junction?
iv. What is meant by the term "Barrier potential"? What is the value for Germanium diode? [3+2+3+2]

Answer any **three(3)** from (a), (b), (c) and (d):

4. i) Derive the expression and calculate the value for (i) dc load current, (ii) ripple factor and (iii) rectification efficiency of a center tapped full wave rectifier
ii) Draw a positive diode clamper circuit. Explain its operation
iii) A 10 V peak sinusoidal voltage is applied to the input of a positive diode limiter. Draw the circuit with proper bias to limit the output to +5 V. [4+4+2]

(b)i) Draw and explain the input and output characteristics of a bipolar junction transistor operated in common base (CB) mode.
ii) What do you mean by biasing of a transistor? Draw the basic three configurations of n-p-n transistor.
iii) Derive the relationship between α and β of BJT. Given $\alpha = 0.98$, find the value of β. [3+2+5]

(c) i) Draw and explain the transfer characteristics of an ideal OPAMP.
ii) Draw and explain the output characteristics of an enhancement mode MOSFET.
iii) Explain the pinch-off phenomenon in JFET with a neat diagram. [4+4+2]

(d) i) What are the advantages of negative feedback in an amplifier.
ii) Derive the voltage gain for an inverting and a non-inverting amplifier using OPAMP.
iii) Explain the working principle of OP-AMP integrator and differentiator with proper circuit diagram and suitable input and output waveforms. [4+3+3]

Answer any **one(1)** from (a), (b)

3. (a) i. What is an integrated circuit?
ii. What is common-mode rejection ratio, input bias current, input offset voltage and output offset voltage of an operational amplifier?
iii. Define slew rate.[2+6+2]

(b) i. Describe the use of an operational amplifier as an adder.
ii. Explain virtual ground in an op-amp.
iii. Explain how square and triangular waveforms can be produced using OP AMPs. [3+3+4]

Answer any **three(3)** from(a), (b), (c) and (d):

4. (a) i. Convert base of the following numbers:
i.i. $(7864)_{10} \equiv (?)_{16}$
i.ii. $(7.FD6)_{16} \equiv (?)_{8}$
i.iv. $(5157.632)_{8} \equiv (?)_{16}$
ii. Obtain 2's complement of $(11101011)_2$ and $(10101100)_2$.
iii. Add $(46)_{10}$ and $(27)_{10}$ using BCD numbers. [6+2+2]

(b) i. State De-Morgan's theorem. Show its logic implementation.
ii. Simplify the following Boolean expression:
$f = (A + B)(\bar{A}\bar{C} + C)\left(\overline{\bar{B} + AC}\right)$ and $f = A + \bar{A}B + \overline{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D.$ [4+6]

(c) i. Obtain the minimal sum of products expression for the following function and implement the same using only NAND gates.

$$f(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2)$$

ii. Realize the Boolean expressions using basic gates $f = \{D(\overline{A + B}) + \bar{B}(C + D)\}$ and $f = \left(\overline{A\bar{B}C + A + \overline{B + C}}\right)$.[6+4]

(d) i. Draw the symbols of universal gates. Write their truth table (for 2-input gate).
ii. What is half-adder? Design a half-adder using only NOR gates. [4+6]

Answer any **one(1)** from (a) and (b):

(a) i. What is D flip-flop?
ii. Describe the working of SR flip-flop with circuit diagram and truth table.
iii. What is the advantage of D flip-flop over an SR flip-flop?
iv. What is clock? What is the purpose of the clock signal? [2+4+2+2]

(b) i. What is meant by edge triggering?
ii. Give the difference between positive edge triggering and negative edge triggering.
iii. Explain the operation of master slaveflip-flop and show how the race around condition is eliminated in it. [2+2+6]