

B. INS. & ELEC. ENGINEERING 3RD YEAR 2ND SEMESTER EXAMINATION 2022

ANALOG MOS CIRCUIT DESIGN

FULL MARKS: 100

TIME: 3 HOURS

List of Course Outcomes (CO):

- CO1: Classify and analyze different types of MOS amplifiers (K4, A1-recognize).
 CO2: Explain and interpret the importance of differential amplifiers (K3, A1)
 CO3: Describe and explain the behavior of current mirrors (K2, A1)
 CO4: Explain and analyze the frequency response of MOS amplifiers (K4, A1)

Instructions to the Examinees:

- Each module is mapped with the corresponding CO
- Attempt questions from **ALL** the modules
- Alternative questions exist within a module, not across the modules
- Different parts of same question should be answered together
- Clearly state any assumption and derive the necessary equation(s) for calculation
- Unless otherwise stated, use the device data shown in Table I and assume $V_{DD} = 3V$ where necessary

Table I

| Symbol | Value | Unit |
|----------------|-------|-------------|
| $V_{th,n}$ | 0.7 | V |
| $V_{th,p}$ | -0.8 | V |
| γ_n | 0.45 | $V^{1/2}$ |
| γ_p | 0.4 | $V^{1/2}$ |
| $\mu_n C_{ox}$ | 50 | $\mu A/V^2$ |
| $\mu_p C_{ox}$ | 25 | $\mu A/V^2$ |
| λ_n | 0.1 | V^{-1} |
| λ_p | 0.2 | V^{-1} |

MODULE 1

(ATTEMPT ANY FOUR FROM THE FOLLOWING)

1.

- (a) Write down the condition for a p-MOS device to operate in the saturation region.
- (b) Sketch I_X and trans-conductance of the transistor as a function of V_X for the circuit in Fig. 1 as V_X varies from 0 to V_{DD} .

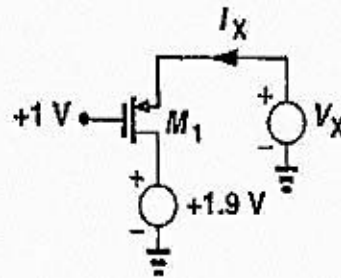


Fig. 1

2+8

2.

- (a) What do you understand by body effect? How does it affect the threshold voltage of MOSFET?
- (b) Draw the MOS small-signal model by taking channel-length modulation and body effect into your consideration.
- (c) Sketch g_m and g_{mb} as a function of the bias current I_1 in Fig. 2.

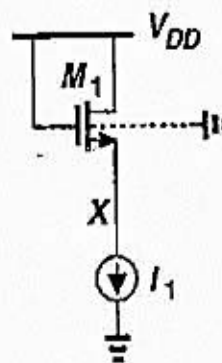


Fig. 2

3+2+5

3. Draw and explain the transfer characteristics of the circuit shown in Fig. 3. Sketch the drain current and trans-conductance of the MOS device as a function of the input voltage.

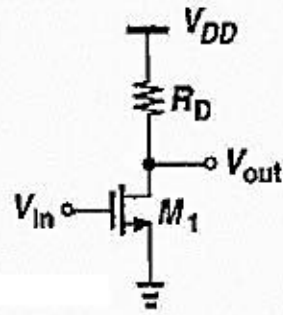


Fig. 3

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4. Sketch v_{out} versus v_{in} for the circuit in Fig. 4 as v_{in} varies from 0 to V_{DD} . Identify the important transition points.

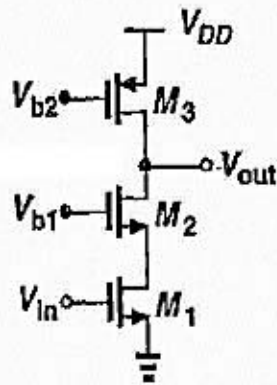


Fig. 4

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5. Calculate the voltage gain of the circuit shown in Fig. 5. Assume $\lambda \neq 0$ and $\gamma \neq 0$

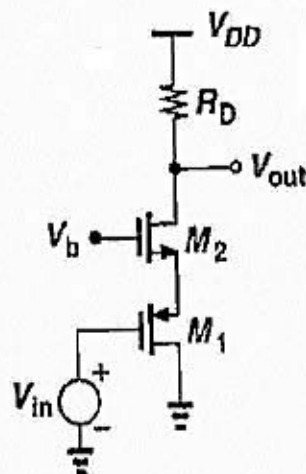


Fig. 5

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MODULE 2

(ATTEMPT ANY THREE FROM THE FOLLOWING)

- 6.
- (a) What do you mean by differential signals?
- (b) Show that the equivalent G_m for a differential amplifier falls to zero for $\Delta v_{tn} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$, where the symbols enjoy their usual significances.
- 2+8
- 7.
- (a) What is the significance of tail current source in a differential amplifier? Explain.
- (b) Plot the input-output characteristics of a differential pair as the device width and tail current vary.
- (c) How is the input common-mode level of a differential amplifier limited?
- 3+5+2
8. A differential pair uses input NMOS devices with $W/L = 50/0.5$ and a tail current of 1 mA . What is the equilibrium overdrive voltage of each transistor? How is the tail current shared between two sides if $v_{tn1} - v_{tn2} = 50 \text{ mV}$? What is the equivalent G_m under this condition?
- 10
- 9.
- (a) Under which condition a common mode input signal produces non-zero differential output? Explain.
- (b) Find out the expression for differential gain by considering mismatches in trans-conductance of two MOS devices and non-ideal tail current source.
- 3+7

MODULE 3

(ATTEMPT Q. NO. 9 AND ANY ONE FROM THE REST)

10. Find out the drain current of M_4 in Fig. 6 if all of the transistors are in saturation.

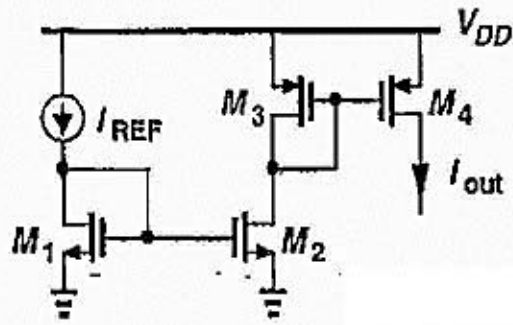


Fig. 6

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11. In Fig. 7, assuming all of the transistors are identical, sketch I_X and V_B as V_X drops from a large positive value.

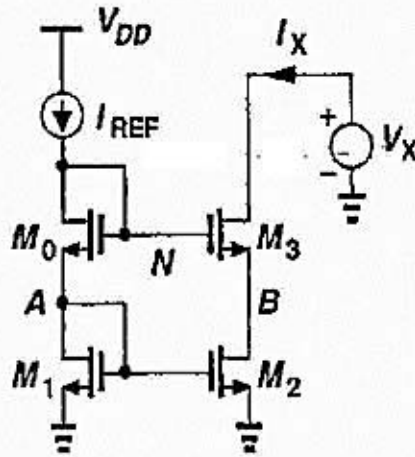


Fig. 7

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12. In Fig. 8, sketch V_X and V_Y as a function of I_{REF} . If I_{REF} requires 0.5V to operate as a current source, what is its maximum value?

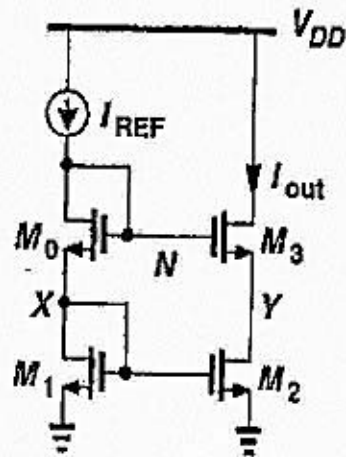


Fig. 8

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MODULE 4

(ATTEMPT ANY ONE FROM THE FOLLOWING)

13. Calculate the transfer function of the circuit shown in Fig. 9.

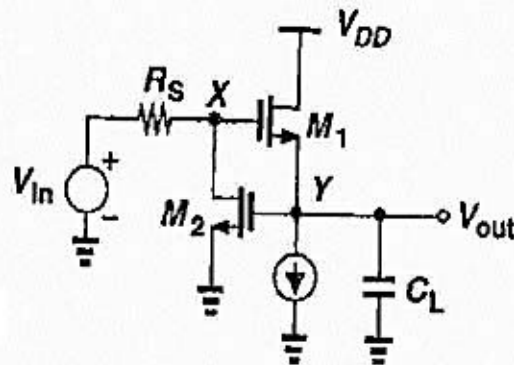


Fig. 9

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14. Estimate the poles of the circuit in Fig. 10 below.

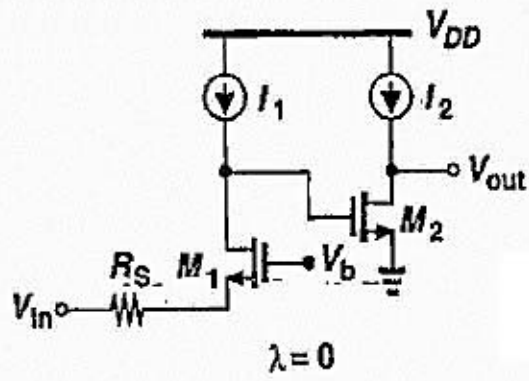


Fig. 10

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