B.E. Electronics & Telecommunication Engineering

Third Year, Semester 2 Examinations, April / May 2022

Embedded Systems Ref. No.: Ex/ET/PC/H/T/325/2022

Time: 3 Hours **Full Marks: 70**

Instructions: (i) Questions must be answered serially. (ii) All parts of the same Section / Question must be answered at ONE place, only.

Section 1: **(10 Marks)**

1. Execution behavior is _____ for certain types of Embedded Systems. (1 mark)
2. _____ is an example for typical data transmission ES. (1 mark)
3. Explain the salient features of RISC Design Philosophy (4 marks)
4. Identify and explain in brief the key building blocks of an ARM based Embedded device, a microcontroller. (4 marks)

Section 2: **(25 Marks)**

1. (i) Identify the number of available Ports, and also the (ii) dedicated Port in Intel 8051 Microcontroller Unit (MCU). (2 Marks)
2. List and explain the 8051 MCU Bus Control Signals. (4 Marks)
3. (i) The amount of Program Memory (PM) and Data Memory (DM) available in 8051 is _____ and _____ respectively. (ii) Explain the reason behind the logical separation of PM and DM in 8051 MCU. (1+1)
4. (i) The 8051 is provided with _____ Interrupt Sources, and they can be independently enabled / disabled through _____ Register of 8051 MCU. (2Marks) (ii) List the 8051 MCU Interrupt Priority Structure (2 Marks). (iii) List the conditions, that could block the hardware generated LCALL in 8051 MCU. (3 Marks)
5. The _____ Special Function Register is used to invoke reduced power saving modes in 8051 MCU. Explain the available power saving modes in 8051. (3 Marks).
6. External Memory access is through _____ only. (1 Mark)
7. Regarding the I/O Port Structure, each Port Pin consists of _____ (2 Marks)
8. The Bit 1 and 2 of TMOD register of 8051 is at Logic 1 and 0 respectively, and other bits are at logic 0. (Note that the LSBit is Bit 0). Explain the operation of 8051 Timer, for this condition of the TMOD register. (4 Marks).

Section 3: **(10 marks)**

1. The ARM Processor, like all RISC Processor, uses a _____ architecture. Data Processing is carried out solely in _____. The _____ converts signed 8-bit / 16-bit numbers to 32-bit values (1+1+1 mark).
2. What is the function and importance of barrel shifter unit in the ARM core data flow model? (2 marks)

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3. (i) Identify the ARM mode, which cannot change the mode by writing directly into the mode bits of the concerned register. (ii) Identify the ARM mode, which do not have a set of associate banked registers. (1+1 Mark).
4. List the name of the banked registers available in the ARM core during the execution of the Interrupt Request mode (IRQ). (3 marks)

Section 4: **(20 Marks)**

1. Explain the operation of Indexed Addressing mode in 8051 MCU with the corresponding instruction, using example. (3 marks)
2. Write an 8051 Assembly Language Program (ALP) to implement XOR logic with minimum instructions. The final output must be made available at P1.0 and what is the Physical address of P1.0 (3 marks).
3. Explain with an example ALP, the addressing mode used by all the conditional instructions, and how the effective destination address is computed. (5 Marks)
4. In the 8051 Assembly instruction, [MOV C,20H], identify the actual location of the address 20H. (2 Marks)
5. Explain the Read-modify-write operation with a suitable 8051 assembly instruction (3 marks)
6. Write an 8051 ALP to implement Y = (M*X)+Y without using MUL AB instruction; Assume 8-bit result. (4 Marks)

Section 5: **(5 Marks)**

1. Indicate the Start and Stop conditions in I2C communication Protocol. (2 Marks)
2. SPI bus Protocol is Asynchronous in nature (True / False)
3. Identify the most important Trade-off in the Hardware – Software Co-Design (1 Mark)
4. A _____ captures and describes the System Characteristics. (1 Mark) (Model)