Ref. No.: Ex/EE/PC/B/T/225/2022

B. ELECTRICAL ENGINEERING 2ND YEAR 2ND SEMESTER EXAMINATION, 2022

Subject: SEQUENTIAL SYSTEMS & MICROPROCESSORS Time: 3 Hours Full Marks: 100

Use a separate Answer-script for each Part

Part I (50 marks)

Question 1 is compulsory

Answer ***Any Two*** questions from the rest (2×20)

Question No.		Marks
Q1	Answer ***any Two*** of the following:	
	(a) A fictitious flip-flop with two inputs A and B is designed such that for AB= 00 and 11 the output becomes 0 and 1, respectively. For AB= 01, flip-flop retains previous output while output complements for AB= 10. Determine the truth table and excitation table for this flip-flop.	5
	(b) Show how a $\bar{R}\bar{S}$ flip-flop can be converted to a RS flip-flop.	5
	(c) Explain how SR Flip-Flop can be used in toggle mode.	5
	(d) Starting from the excitation table develop the state diagram for J-K flip-flop.	5
Q2	(a) (i) What is Excitation Table for a Flip-flop? How is it different from the Truth Table? (ii) With the help of Excitation Table show how SR-flip-flop can be converted to JK-flip-flop.	4+6
	(b) Consider, the sequential circuit shown in Figure Q2(b). It has only input *CLK* in the form of a fixed frequency binary pulses that triggers both the flip-flops. An output X is generated from flip-flop outputs as shown. (i) Show, with the help of state table, how the flip-flop values (or states) and output X change with input *CLK*. (ii) Draw the corresponding state transition diagram.	8+2

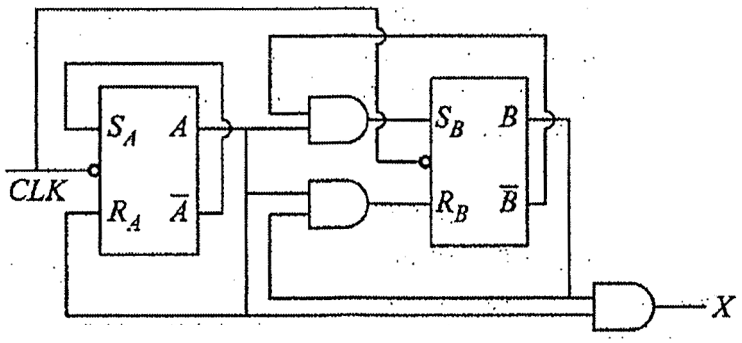


Figure Q2(b)

Q3 (a) (i) What are Synchronous and Asynchronous Counters?
(ii) Design 3-bit binary Synchronous Up-Counter using JK-Flip-Flops. 2+8

(b) (i) Show how a 4-bit Shift-Right Register can be realized using D flip-flops.
(ii) Explain, with the help of timing diagram, how a number "0100" can be entered serially into the register. 4+6

Q4 (a) (i) Justify that the circuit shown in Figure Q4(a) is a Mod-3 counter.
(ii) Show that if one connects the B output of the counter to the clock input of another J-K Flip-Flop, with both J and K of the 3rd Flip-Flop being connected to $+V_{CC}$, then the circuit becomes a Mod-6 counter. 4+6

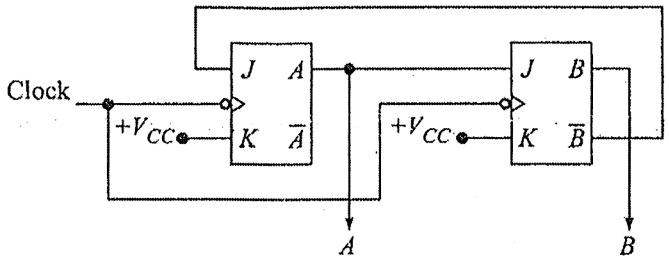
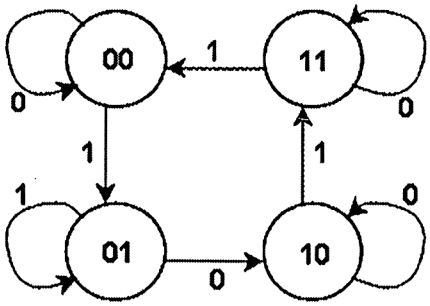


Figure Q4(a)

(b) Suppose we wish to design a circuit that detects a sequence of three or more consecutive 1s in a string of bits coming through an input line (i.e., the input is a serial bit stream).
(i) Draw the corresponding state transition diagram.
(ii) Obtain, with the help of state table, the logic circuit for the sequence detector realized employing D flip-flops. 4+6

Q5 (a) Design a synchronous sequential circuit having the following state transition diagram with the help of JK flip-flops.



10

(b) What is Universal Shift-Register? With the help of a neat diagram briefly explain the different modes of operation for 4-bit Universal Shift-Register. 2+8

Ex/EE/PC/B/T/225/2022

BACHELOR OF ELECTRICAL ENGINEERING EXAMINATION, 2022

(2nd Year, 2nd Semester)

SEQUENTIAL SYSTEMS AND MICROPROCESSORS

Time: Three hours (50 marks for each Part) Full Marks: 100

Use a separate Answer-Script for each Part

PART- II

Answer *any five* questions.

1.a) How many memory locations can be addressed by a microprocessor with 14 address lines? (2+3)
Discuss the functions of program counter and stack pointer of Intel 8085 microprocessor.

b) Briefly explain the functions of the following pins of 8085 microprocessor : (3+2)
(i) S_0, S_1(ii) IO/$\overline{M}$.

2.a) Specify the addressing modes of the following 8085 instructions: (5)
i. CMC ii. ORA B iii. SUI 05H iv. MOV B,Mv. STA 8000H

b) Explain how lower order address bus can be time multiplexed to be used as data bus in 8085 architecture. (5)

3.a) Distinguish between the opcode fetch and memory read/write machine cycles showing their timing diagrams. (5)

b) Explain why wait state is required and also draw a logic circuit for generation of wait state. (5)

4. The initial content of Accumulator of 8085 is considered to be 7FH and all the bits of the flag register are reset. Write the content of accumulator and the flag register after execution of each of the following instructions separately: (10)
(i)DCR A (ii) MOV B,A (iii) CPI 90H (iv) ADI 92H (v) RAL

5. Discuss the function of the instruction CALL and also the steps involved in execution of the instruction. (10)

Or

Discuss the function of the instruction RST and also the steps involved in execution of the instruction.

6.a) If a 4MHz crystal frequency is connected with 8085 microprocessor, what is the value of system clock frequency? Calculate the delay time for the following subroutine for the same microprocessor (2+4)

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        MVI   B, 38H
Loop 2: MVI   C, FFH
Loop 1: DCR   C
        JNZ   Loop 1
        DCR   B
        JNZ   Loop 2
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b) How you can use SIM instruction to manipulate the masking of the interrupts. (4)

7.a) Draw the timing diagram for MVI M, 80H, the hex code for MVI M being 36H. (7)

b) Explain Maskable and Non maskable Interrupt. (3)

8. Write assembly language program in 8085 to perform the following operations: (4+6)

(i) to clear the content of the flag register
(ii) to multiply two 8 bit numbers