THRESHOLD VOLTAGE MODELLING OF DP-DG MOSFET INCORPORATING QUANTUM MECHANICAL EFFECTS

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This work is dedicated to my Parents
and my beloved brothers for their selfless sacrifice
and support

Table of CONTENT

ACKNOWLEDGEMENT..i
List of Tables ii
List of Figures iii
List of Publications v
ABSTRACT vi

CHAPTER 1: INTRODUCTION AND ORGANIZATION OF THESIS

1.1 Introduction 2
1.1.1 Moore's Law...5
1.1.1.1 Beyond Moore's Law..7
1.2 Recent works in low dimensional semiconductor era 9
1.3 Motivation...14
1.4 Organization of Thesis..15

CHAPTER 2: BASICS ON LOW DIMENSIONAL DEVICE STRUCTURES

2. Device Scaling 18
2.1 Short Channel Effects (SCEs) 20
2.2 Different SCEs associated with device miniaturization...............................22
2.2.1 Electric field becomes two dimensional in nature.....................................22
2.2.1.1 Drain Induced Barrier Lowering (DIBL) 22
2.2.1.2 Threshold voltage Roll-off 24
2.2.1.3 Surface Scattering 24
2.2.2 High Electric Field Strength 25
2.2.2.1 Velocity Saturation 25
2.2.2.2 Hot Electron effects 26

2.2.2.3 Impact Ionization near the drain 27
2.2.2.4 Parasitic Bipolar effect 28
2.2.2.5 Gate Oxide charging 28
2.2.3 Channel Length Modulation 29

CHAPTER 3: THRESHOLD VOLTAGE MODELLING OF DP-DG MOSFET INCORPORATING QUANTUM MECHANICAL EFFECTS

3.1 Impacts of Dielectric Pockets 32
3.2 Quantum Confinements in MOSFETs 34
3.2.1 Types of Quantum Confinements 36
3.2.1.1 Inversion charge Model 39
3.2.1.2 Threshold voltage Model 40
3.2.1.3 Effects of Quantum Confinements 42
3.3 Proposed structure of DP-DG MOSFET 43
3.4 Analytical Modelling of DP-DG MOSFET 46
3.4.1 Inversion Charge Modelling 51
3.4.2 Threshold Voltage Modelling 52
3.4.2.1 Classical Threshold Voltage Modelling 54
3.4.2.2 Quantum Threshold Voltage Modelling 54

CHAPTER 4: RESULT AND DISCUSSIONS

4. Results and Discussions 59
4.1 Surface Plot 59
4.1.1 Surface plot along channel length 59
4.1.2 Surface plot along channel thickness 60
4.2 Electric field 61
4.3 Deviation of Quantum Threshold Voltage from Classical counterpart...61
4.4 Quantum Threshold Voltage 62

4.5 Subthreshold Slope 64
4.6 Comparison of DP-DG MOSFET with other MOSFETs 65

CHAPTER 5: CONCLUSION & FUTURE SCOPES OF THE PRESENT WORK

5.1 Conclusions 68
5.2 Future Scopes of the present work 70

REFERENCES..71

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List Of Tables ***Page No.***

Table 1: Typical Values of the Parameters Used for DP-DG MOSFET..59

List Of Figures ***Page No.***

Fig. 1.1:(a) Birth of the Microprocessor in 1971, The Intel 4004 –2,300Transistors………...3
Fig. 1.1:(b) A Very Early 32-Bit Microprocessor –1981, The HP Focus Chip,
Hewlett-Packard Co. – 450,000Transistors………………………….................................4
Fig.1.2: Intel Pentium 4 micro Processor – 2003 (55 million transistors)……………………4
Fig: 1.3: ITRS 2013, MPU/ASIC half pitch and gate length trends with the
increment of areal density per year………………………………………………………....6
Fig 2.1: The barrier $\varphi_B(\varphi_{B1} > \varphi_{B2} > \varphi_{B3})$ which is to be crossed by an electron
on its way from the source to the drain reduces as channel length is decreased……………..23
Fig. 2.2: Cross section view of MOSFET...25
Fig.2.3: Generation of electron-hole pair through Impact Ionization………………………..27
Fig.2.4: Channel Length Modulation in a MOSFET...30
Fig. 3.1: Carrier energy quantization at the Si–SiO_2 interface in a MOS capacitor.................34
Fig. 3.2:(a) Schematic illustration of the conduction band bending of a bulk and
PD SOI MOSFET in inversion regime showing the different energy levels
resulting from the quantization effects of the 2-D electron gas
confined in the surface potential well...35
Fig. 3.2: (b) Corresponding electron distributions in the direction
perpendicular to the interface for the classical and quantum-mechanical case.......................35
Fig. 3.3: Energy-band diagrams in a vertical cross-section in the
Silicon film of DG n-channel MOSFETs showing two possible cases
of carrier confinement:
i) electric field-induced quantum confinement (EC-QM) and
ii) t_{Si}-induced structural confinement (SC-QM) due to the narrow potential
well defined by thin Silicon film 36
Fig.3.4: Bell-shaped paraboloids showing the total energies including transverse
kinetic energies for the first two sub-bands..38
Fig.3.5: Variation of threshold voltage versus thickness of the Si film….............................42
Fig.3.6: Schematic diagram of DP-DG MOSFET...44
Fig 3.7:(a) Case I: Schematic cross section of Double Gate MOSFET incorporating
Dielectric Pocket (DP-DG)..45
Fig 3.7:(b) Case II: DP-DG MOSFET with Dielectric Pocket at the interface of
S/D regions (i.e. partially inside the S/D region and partially inside the channel region)
and both at the S/D region...45
Fig 3.7:(c) Case III: DP-DG MOSFET with Dielectric Pocket in the
channel and at both source and drain regions...45
Fig 3.7:(d) Case IV: DP-DG MOSFET with Dielectric Pocket
at the drain side only...45
Fig 3.7:(e) Case V: DP-DG MOSFET with Dielectric Pocket at the interface
of S/D regions (i.e. partially inside the S/D region and partially inside the channel
region) and at drain side only..45
Fig 3.7:(f) Case VI: DP-DG MOSFET with Dielectric Pocket in the channel region

and at the drain side only..45
Fig. 4.1: Variation of surface potential along channel length with respect to
V_{gs} fixed at 0.3V and V_{ds} used as variable parameter..60
Fig.4.2: Rectangular well formed along film thickness with perturbation with
fixed gate and drain voltage at 0.3V and 1V respectively..60
Fig.4.3: Variation of surface potential & surface electric field along channel length
with respect to V_{gs} fixed at 0.3V and V_{ds} used as variable parameter.....................................61
Fig. 4.4: Variation of along channel length with fixed V_{gs} and V_{ds} at 0.3V and
0.5V with Na as variable parameter..62
Fig. 4.5: Quantum Vth along channel length with fixed V_{gs} and V_{ds} at 0.3V and
0.5V with Na as variable parameter..63
Fig. 4.6: Variation of Quantum Vth with respect to y_1 and y_3 (whereas y_2 length
remain same) with Na as variable parameter and V_{gs} and V_{ds} fixed at 0.3V and
0.5V respectively..63
Fig.4.7: Variation of Sub-Threshold Slope along channel length with fixed $V_{gs}$and
V_{ds} at 0.3V and 0.5V respectively& channel doping used as variable....................................64
Fig.4.8: Comparison between quantum V_{th} of DG MOSFET and DP-DG MOSFET
along channel length where for both V_{gs} and V_{dsat} 0.5V and 0.5V respectively......................65
Fig.4.9: Comparison between quantum V_{th} of DMDG SOI and DP-DG MOSFET
along channel length for different channel doping where for both $V_{gs}$and V_{dsat}0.6V
and 0.5V respectively...66

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ABSTRACT

Downscaling he feature size of silicon based MOSFETs has been limited by device performance degradation as a result charge sharing between source and drain region which effectively reduces the gate control over the channel region leading to several unwanted short channel. Some of the major Short Channel Effects (SCEs) are enhanced leakage current, reduced threshold voltage, and increased channel electric field at the drain side affecting device reliability, *Channel Length Modulation* (*CLM*) and *Drain Induced Barrier Lowering (DIBL)* effect.

Two popular approaches are now being adopted to overcome the problems associated with SCEs so as to extend Moore's Law for CMOS devices: (i) using channel materials other than silicon to improve carrier transport properties and (ii) advance device engineering techniques to improve the electrostatics of CMOS. High-k material and new gate electrode materials are being extensively used to improve carrier transport properties in addition to new material in the source/drain region to reduce channel resistance and carrier injection properties of the device. Some of the contemporary device engineering concepts used to control these small-geometry effects are: lateral channel engineering (i.e. Lightly Doped Drain, Halo MOSFET and Dielectric Pocket/ Insulated Shallow Extension MOSFET), substrate engineering (Silicon On Insulator and Silicon On Nothing MOSFET) and gate electrode engineering (Dual Gate FET, Split Gate, Double Gate MOSFET, Tri Gate and FinFET) techniques.

Focussing on the technique of lateral channel engineering, the performance of the CMOS technology can be improved by placing insulating layer near the drain side to suppress the drain side electric field and hence Hot Carrier Effects i.e. Insulated Shallow Extension (ISE) MOSFET also known as Dielectric Pocket (DP) MOSFET. ISE MOSFET provides better dielectric isolation from drain to source region resulting in lower threshold voltage roll-off and punch-through effect. To obtain further enhancement in gate controllability over the channel region and to eliminate floating body effect arising in bulk MOSFETs, gate engineering is now being adopted resulting in Dual gate MOSFETs. DG MOSFETs possess higher channel mobility because of undoped silicon body and avoids undesirable effect of threshold voltage roll-off arising due to channel dopant fluctuation. However, the DG MOSFET suffers

from enhance parasitic (gate to source (C_{gs}) and gate to drain (C_{gd})) capacitances as compared to bulk MOSFET. Incorporation of lateral channel engineering into a DG MOSFET by introducing Dielectric Pockets at side wall of DG MOSFET results in a new device design known as Dielectric Pocket Double Gate (DP-DG) MOSFET, which significantly decreases the parasitic capacitance and also reduces the dopant-out diffusion from the Source/Drain to the channel region.

However, considering device dimension in sub micron regime, device performance will be inevitably affected by quantum phenomena. This necessitates the incorporation of quantum mechanical effects while investigating the device performance of such ultra nano dimensional device structures.

The present dissertation reports an analytical quantum mechanical threshold voltage modelling for Dielectric Pocket Dual Gate (DP-DG) MOS structure for low-power applications. Due to ultrathin architecture, classical models are not enough to accurately model the potential profiles, threshold voltage characteristics and charge inversion phenomena for DP-DG MOSFET devices. So, in this study, perhaps for the first time, carrier quantization model has been adopted with the proposed structure by developing an analytical quantum mechanical (QME) model to achieve more accurate features for DP-DG ultrathin architecture. To obtain the overall potential, threshold voltage and inversion charge profile, 2-D Poisson and Schrödinger equations have been solved self consistently for the proposed structure. The analytical results have been validated against the simulation results using ATLAS device simulator.

CHAPTER1:

INTRODUCTION AND ORGANIZATION OF THESIS

1.1 Introduction

1.2 Recent works in low dimensional semiconductor era

1.3 Motivation

1.4 Organization of the thesis

1.1 INTRODUCTION

Unprecedented growth in information technology (I.T), and communications market has been mainly enabled by continuous progress in silicon-based complementary metal-oxide-semiconductor (CMOS) technology. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is one of the successful and most manufactured electronic devices in the history of electronics. This progress has been made possible only because of considerable reduction in the device dimensional, which also results in higher device density and better device performance. The economic productivity has also been continuously increasing with every new technology generation due to the reduction in cost-per-chip. In addition to its scalability, the unique properties of CMOS transistor such as high input resistance, zero static power dissipation, simple layout and process steps have made MOSFET as the main component of the current integrated circuits (ICs). Nowadays, semiconductor technologies based ICs are everywhere and indispensable in our daily life. These include not only microprocessor, memory chips but also ranging from portable electronics (i.e. multimedia devices and high definition display) to telecommunications, transportation and medical instruments. These broad applications are possible only because of the mixed signal technologies which enable large scale integration of non-digital functions such as analog/radio frequency signal processing, data conversion between analog and digital functions.

Towards the end of the 1950's, in 1958 "integrated circuits" came into existence with the invention of First Integrated Circuit by Jack Kilby from Texas Instruments. The first integrated circuit [1], consisting of one transistor and four other devices on one chip, won Nobel Prize in the year 2000. The new era of Small Scale Integration (SSI) Technology was pioneered by the first commercial Planar IC invented by Fairchild. It was a One Binary Digital (Bit) Memory Device consisting of 4 Transistors and 5 Resistors on a Chip. In 1962, Radio Corporation of America (RCA), Sarnoff Laboratories introduced a new form of transistor named as Metal-Oxide Semiconductor Field-Effect Transistor [2]. The invention of integrated circuit became very important as they improved the power of electronics devices. Over the years the number of

transistors on these chips increased substantially from Intel Corporation's first 1,024 bit memory chip DRAM to today's processor containing almost 55 million transistors on a single chip. As of 2012, the highest transistor count in a commercially available processor is more than 2.5 billion. The beginning of Large Scale Integration (LSI) Technology was started with the birth of Intel's microprocessor 4004 (Fig.1.1 (a)) consisting of 2300 transistors in 1971. [2]. It was the first 'computer on a chip'. Processors in 1970's usually had only nMOS transistors which was inexpensive but consumes power at sleep mode or idle mode. 1980's processors replaced nMOS with CMOS which consumes very less idle power. The method of coupling two complementary MOSFETS (P-channel and N-channel) into one high/low switch, known as CMOS, means that digital circuits dissipate very little power except when actually switched. As the number of transistors per chip increased, the less idle power consumption of CMOS over BJTs made CMOS the dominant technology in present era. At the beginning of 1980's the Very Large Scale Integrated (VLSI) circuit era begins with the introduction of Hewlett-Packard's 32-Bit Microprocessor, the HP Focus Chip, comprising of 450,000 Transistors (Fig. 1.1 (b)).

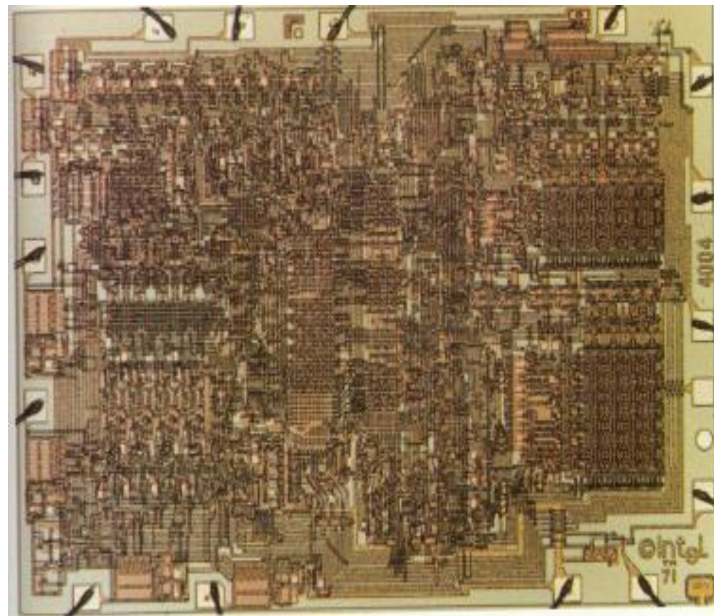


Fig. 1.1 (a)

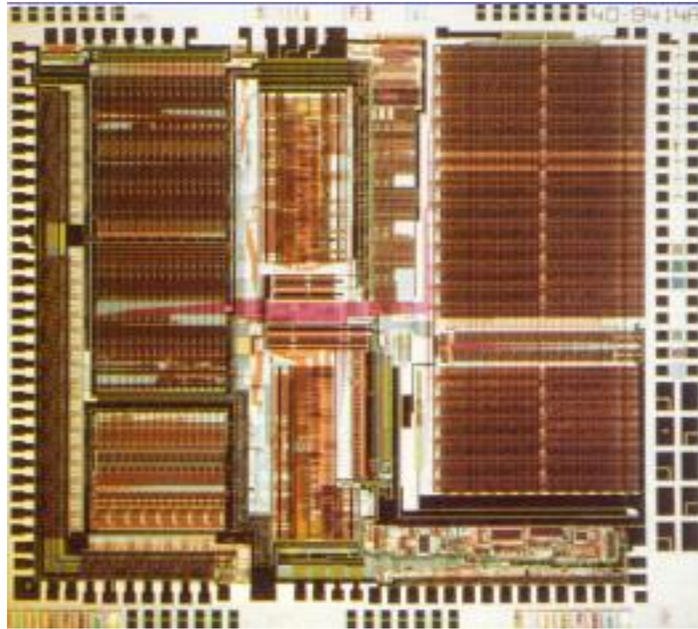


Fig. 1.1 (b)

Fig.1.1: (a) Birth of the Microprocessor in 1971, The Intel 4004 – 2,300 Transistors; (b) A Very Early 32-Bit Microprocessor –1981, The HP Focus Chip, Hewlett-Packard Co. – 450,000 Transistors

In 2003, Intel has launched Pentium 4 with 55 million transistors (Fig.1.2). So, in recent times, miniaturization has become the key aspect in semiconductor industry. Microelectronics industry has evolved to nano electronics with the tremendous progress of downscaling of device dimensions. Since the late 1960s, number of transistors on a silicon chip has increased with exponential dependency.

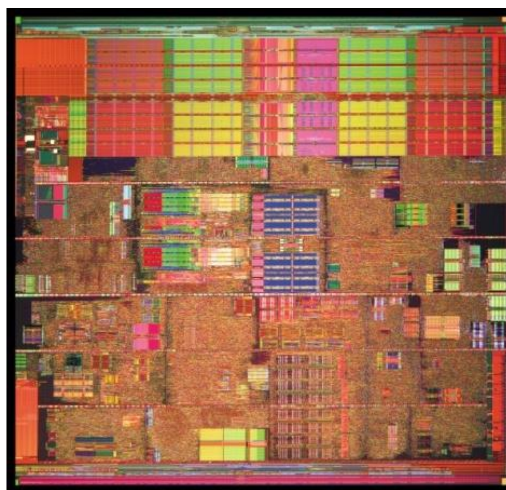


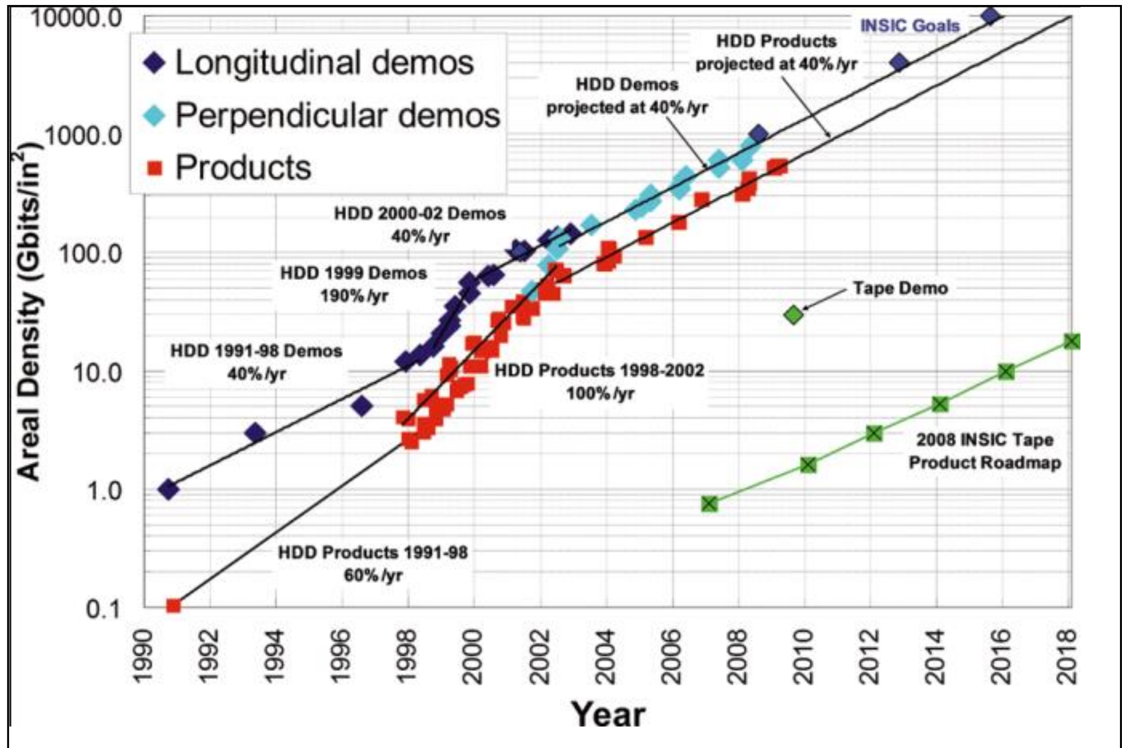
Fig.1.2 Intel Pentium 4 micro Processor – 2003 (55 million transistors)

1.1.1 Moore's Law

Miniaturization of feature size for integrated circuits has been the principal motivation behind these trends and it has led to substantial improvement of productivity, quality and economic acceptability [3]. As predicted by the historical Moore's Law (published by Gordon Moore in 1965), the number of transistors per integrated chip is roughly doubling every 2 years. According to him:

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years.

This prediction has since been known as the Moore's law and been remarkably followed by the semiconductor industry for the last four decades (Figure 1.3).The initiative taken by semiconductor companies and academia since early 90's to predict accurately the future of the industry gave birth to the International Technology Roadmap for Semiconductors (ITRS) organization [4]. Every year, ITRS issues a report that describes the type of technology, design tools, equipment and metrology tools that need to be developed to keep pace with the exponential progress of semiconductor devices predicted by Moore's law. The semiconductor industry's workhorse technology is silicon CMOS, and the building block of CMOS is MOSFET (MOS field-effect transistor). To keep up with the frantic pace imposed by Moore's law, the dimensions of transistors have reduced by half every three years. The sub-micron dimension barrier was overcome in the early 1980's, and by 2010 semiconductor manufacturers have produced transistors with a 32nm gate length. By the early of 2010, a group of leading companies (Intel, AMD etc) published their commercial microchips using CMOS with 32nm process in ITRS. According to ITRS, the continued downscaling has reduced the cost per function by 25-29% per year since 1992 and boost up the electronic market growth historically by 17% per annum. After major corrections in the 2008–09, models of MPU/ASIC half pitch and gate length trends to have remaining unchanged till 2013. The gate length trend is evidencing a slower 3.8 year cycle beginning from 2009 (32nm) to 2028 (5nm) which also indicate that the 10 nm threshold in physical dimension of MOS are to be anticipated by the years of 2020-25.



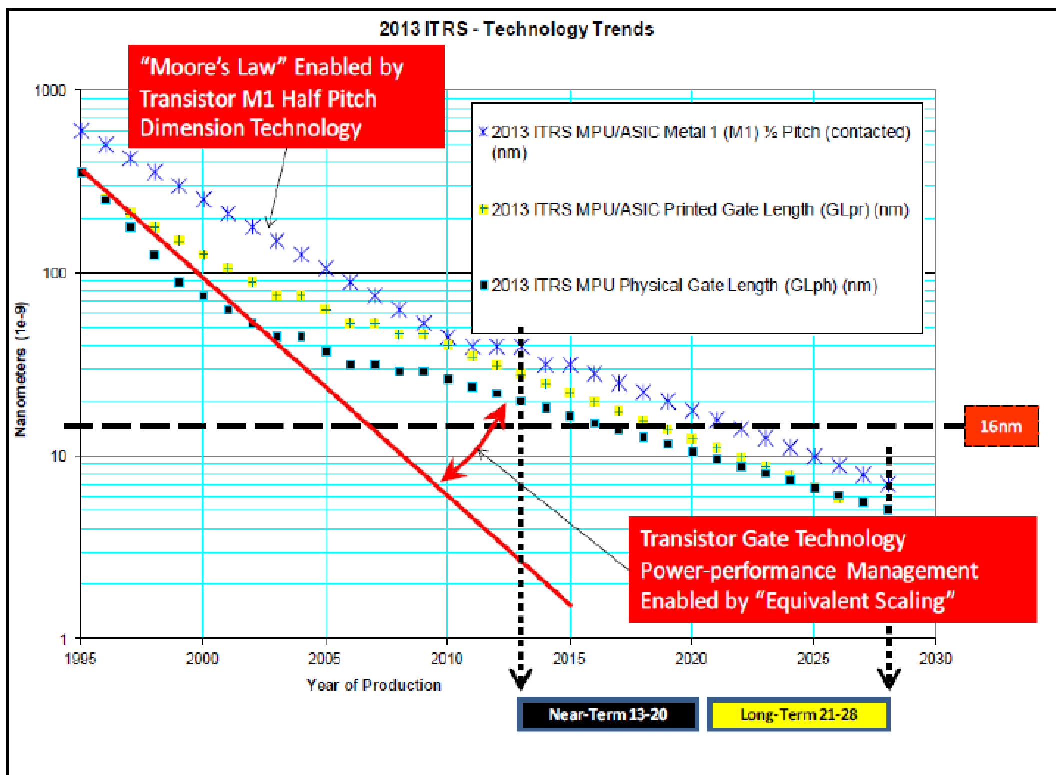


Fig: 1.3: ITRS 2013, MPU/ASIC half pitch and gate length trends with the increment of areal density per year

However scaling beyond 30nm can be more difficult and bounded by the fundamental limits of classical semiconductor physics. Thus the reliability of low dimension MOS will decrease eventually with in increment of cost due to the complexity of fabrication procedure. This is fully reflected in slower economic growth of electronic industries in recent times. With every technological node, it is getting clear that after a certain period of time, the aforementioned fundamental geometrical limits will be reached.

1.1.1.1 Beyond Moore's law:

The ideal scaling method proposed by Dennard [5] increases the device functionality and packing density without inhibiting the requirement of power consumption providing the chip area constant. Practically it has been observed that with the aggressive trend of downscaling for the last 30 years proceeding since early 1970s, the gate length, gate oxide thickness and junction depth were decreased with 100 times, while the supply voltage is decreased only 10 times and the chip area was increased 10 times. As a consequence 100 times increase of clock frequency was gained associated with the nuisance of 100,000 times increment in power consumption.

Several drawbacks start to degrade the performance of the MOSFET, as the channel length of the device shrinks to nanometre regime. Polysilicon gate depletion, Boron penetration and several Short Channel Effects such as Threshold Voltage Roll-Off, Hot Carrier Effects (HCE), Drain-Induced-Barrier-Lowering (DIBL), Sub-threshold conduction and junction leakages become significant factors, which barricade the further scaling according to Moore's Law. Decrease in threshold voltages due to scaling causes early channel conduction and leads to a lower noise margin and off-state leakage.

This has led to planar bulk MOS structures to evolve into several new alternative structures and to introduce new material on silicon-on-insulator (SOI) MOSFET Technology. The International Technology to Roadmap of Semiconductors (ITRS) has set up the new concept of scaling other than 'Geometrical Scaling'. This type of scaling termed as 'Equivalent Scaling', emphasizes on innovative design, software solutions, new materials / device structures [4]. Since 2007, ITRS has addressed the concept of 'functional diversification' under the title 'More than Moore' (MtM). This concept

addresses an emerging category of devices that incorporate functionalities which do not necessarily scale according to Moore's law. This MtM approach which mainly focuses in non-digital functionalities such as RF communication, power control, passive components, sensors and actuators, allows the non-digital functionalities to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) systems. As the technology is moving forward, it became challenging to satisfy apparently conflicting condition of precision and simplicity. Retaining the same functionality with device miniaturization can be achieved only by equivalent scaling i.e. incorporating new device structures. Several researchers have put forward alternative structures to replace the bulk MOS structures. Several unconventional geometries MOS structures like Strain Silicon, Multiple Gate MOSFET and binary metal alloy gate SOI/SON MOSFET structure have also been studied experimentally as well as theoretically in recent times and they exhibit improved performance under the influence of different SCEs in nano dimensional region. In 2009, ITRS has reported some credible candidates to conventional bulk SOI MOSFET structures in 22 nm or beyond such as Carbon Nanotube FETs, Graphene Nanoribbon FETs, Nanowire Field-Effect Transistors (NWFETs), III-V channel replacement devices, Ge channel replacement devices, Unconventional Geometries for FET devices.

Furthermore, as the device dimension is comparable to the de Broglie's wavelength due to swift downscaling of device dimension, oxide thickness has to be scaled down proportionally. Ultrathin oxide with high channel doping levels consequences a strong increase of the electric field at the Si/SiO_2 interface, which creates a sufficiently steep potential well. In that circumstances quantum mechanical tunnelling starts to degrade the device performance. Probability of tunnelling mechanism increased exponentially as the device thickness is scaled down with proper ratio with the channel length.

1.2 Recent works in low dimensional semiconductor era:

Since the invention of the field effect transistors, it has grown to be the most important device/component in the integrated circuits [6]. The basic concept of Field Effect Transistor (FET) was patented by Lilienfeld in 1930 [7]. Practically point contact transistor came to into existence in 1947. After 30 years from the invention of the FET concept, in 1960, it was finally reduced to practice in Si–SiO_2 by Kahng and Attala [8]. To keep pace with the tremendous advancement of integrated circuit technology, aggressive miniaturization of device dimension took place. With the commencement of nanotechnology era, gradual miniaturization gives rise to several drawbacks which degrades the device performance. To overcome these shortcomings, conventional MOSFET structure has been modified instead of simple downscaling. Silicon On Insulator (SOI) MOSFET and Silicon On Nothing (SON) MOSFET are the two unconventional structures to hold back the negative aspects of conventional MOS device in nano meter regime [9]. SOI development was first developed in early 1990 in the Advanced Silicon Technology Centre (ASTC) of the IBM Microelectronics Division. Outcome of this effort came into existence, when a power PC using CMOS-SOI technology was developed in the year of 1994.

In 1985, charge based large-signal model for thin film SOI MOSFET was developed considering floating body effects [10]. The effects of the interface parameters on the back and the front threshold voltages were described [11]. The relation of the sub-threshold swing with current capability of the MOSFET with gate length 0.1 µm, became an important concern as low voltage operation requires the investigation of sub-threshold characteristics. To minimize the leakage current, sub-threshold slope has to be small. While operating in sub-threshold region, floating body effect in PD SOI MOSFET causes a shift in sub-threshold slope to a smaller value than the ideal theoretical value. In 1986, Davis et al., observed a better performance in sub-threshold slope in an n-channel MOSFET on SOI substrate [12].

In 1989, K. K Young proposed a two-dimensional short-channel analytical threshold voltage model for fully depleted SOI MOSFET. This model is based on the solution of 2D Poisson's equation which includes the vertical field and lateral field effects under parabolic potential profile approximation [13]. In 1990, an analytical solution of the

Poisson's equation for SOI MOSFET using an infinite series method including both the thin silicon channel and the gate and buried oxide regions was developed by Jason C. S. Woo et al., [14].

In 1991, Tokunaga et al., [15] studied the dependency of substrate bias on sub-threshold slope in n-channel FD SOI MOSFETs. Dependency of temperature as well as drain bias on sub-threshold slope was also measured in this work. At low drain voltage, the experimental results can be explained by a simple capacitor model. For large drain voltages, the sub-threshold characteristics were very sharp for large negative substrate biases. The threshold voltage variation with temperature is significantly smaller in fully depleted devices than in bulk devices.

In 1997, a new structure Dual material gate field effect transistor (DMGFET) was proposed by Long et al., [16]. In this novel structure, gate was constituted of two materials having different work functions placed side by side touching each other. As the threshold voltage near drain end is found to be more negative than that in the source end, Short Channel Effects (SCEs) is reduced due to the shielding effect. In 1998, Jeffrey W. Sleight et al., presented a fully continuous compact model of SOI MOSFET for circuit simulations [17]. This model shows flexibility to make transitions between fully-depleted (FD) and partially depleted (PD) behaviour during the device operation. Later on, a generic new type of field effect transistor (FET), dual material gate (DMG) FET, based on the concept of applying different gate bias in split gate was proposed and demonstrated. But, due to the limitation of the fringing field capacitance between the two amalgamated metal gates, which increases with the decrease of separation between the two gates, some asymmetric structures were reported in [18-19] in which the channel field distribution was assumed to be continuous. The DMGFET consists of two laterally contacting materials with different work functions in such a way that the threshold voltage near the source is more positive than that near the drain (for n channel FET) resulting in a more rapid acceleration of charge carriers in the channel and a screening effect to suppress short-channel effects [20].

In 1998, quantum mechanical calculation was implemented in extremely thin SOI MOSFET structure to evaluate the energy distribution of the electrons and the effect of a drift electric field parallel to the Si–SiO_2 interfaces. Transport properties of electrons in extremely thin SOI MOSFET have been studied using Monte Carlo

simulation method considering contribution of phonon, surface-roughness at both interfaces and coulomb scattering [21]. Decrement of mobility can be greatly explained by the increment of phonon scattering and greater confinement of electron in the electrons in extremely thin silicon film. Next year F. Ga´miz et al., investigated the inversion layer mobility of electrons in SOI MOSFET with a silicon film thickness as low as 5 nm. The Poisson and Schrodinger equations have been solved self-consistently solved to explain quantization effects [22].

In 2000, an analytical current-voltage model for ultra-short channel SOI MOSFET was developed including the velocity overshoot, series resistance and self-heating effects by J. B. Roldán et al., for circuit simulation [23].In the same year, a novel structure namely Hetero Material Gate (HMG) MOSFET was suggested by Zhou et al., [24]. An analytical model for the partially-depleted (PD) silicon-on-insulator (SOI) MOSFET above threshold was developed incorporating front-back interface coupling with all the possibilities; accumulated, neutral, and depleted back interface by M. Youssef Hammad et al., in 2001 [25]. For the first time the “pseudo-two-dimensional” approach (which was used successfully to model lateral fields in bulk-Si devices) is extended to SOI devices in this paper. As the interface coupling and floating-body effects are integrated together in a new, “unified” algorithm, it is applied to tied-body as well as floating-body devices. In the same year, Keunwoo Kim, and Jerry G. Fossum [26] established from their numerical device-simulation results, supplemented by analytical characterizations that an asymmetrical double-gate (DG) CMOS utilizing n+ and p+ polysilicon gates can be superior to symmetrical-gate counterparts. It was also found from their analysis that an asymmetrical Double Gate MOSFET, optimally designed and having only one dominant channel, is capable to yield comparable and even higher drive currents at low supply voltages. In 2002, T. Ernst et al., proposed a compact analytical model for lateral field penetration in the buried oxide and underlying substrate for FD SOI MOSFET [27]. An analytical threshold voltage model for fully depleted single-gate SOI MOSFETs considering the two-dimensional effects was established in 2003 by Kunihiro Suzuki et al., [28]. Dependence of channel-doping concentration, gate oxide and buried-oxide thickness on Short Channel Effects (SCEs) was also presented in this work. In the next year, a new model for Silicon-on-nothing (SON) transistors with thin fully depleted Si film and ultrathin buried oxide was

established by Jérémy Pretet and Stephane Monfray et al., where several intrinsic mechanisms of operation in SON MOSFETs such as substrate depletion by source and drain via doping modulation, low coupling between the front and back gates and role of ultrathin buried oxide were incorporated [29].

In 2002, Donaghy et al., described the basic concept and design details of a vertical transistor incorporating DP for 50-nm channel length with a 350-nm channel thickness [30]. In 2006, Jayanarayanan *et al.* [31] and Gili *et al.* [32] demonstrated experimentally the fabrication feasibility of 50- and 70-nm vertical MOSFETs with DP, respectively, i.e., DPV MOSFET, using conventional lithography process. However, the fabrication process had also some limitations, which are as follows: 1) relatively thick gate oxide is required in the case of vertical DP architecture due to the limitation in the processing furnace, and 2) high channel doping is also required in the case of vertical DP architecture (nearly 1×10^{18} cm^{-3}). Furthermore, in the fabrication scheme proposed by Gili *et al.,* [32], dopant penetration was there, from polysilicon drain into the single crystal substrate that reduces the effective channel length. Another major issue in the vertical architecture is the control of excessive overlap capacitance of the gate over the source and drain. In 2008, Riyadi *et al.,* [33] reported a fabrication process scheme for vertical MOSFET incorporating DP where they studied the impact of RTA time on DIBL and sub-threshold slope (*S*). In 2009, Kok and Ibrahim presented the simulation study of 50-nm vertical MOSFET incorporating DP [34] with a very high channel doping concentration. In the verge of 2012 Kumari et al., [35] proposed a new structure by incorporating the effect of vertical dielectric pocket in the dual gate MOSFETs and observed better performances.

In 2005, a physics-based analytical model was developed in two parts for nano-scale MOSFET by Giorgio Mugnaini et al., [36]. The said model covers the whole range from drift-diffusion to ballistic transport regimes, incorporating quantum confinement effect. In the same year, an explicit analytic solution of the channel potential of undoped-body symmetric dual-gate devices was presented by Adelmo Ortiz-Conde et al., [37].

In 2006, a HiSIM-SOI circuit simulation model based on a complete surface-potential description was reported by Norio Sadachika et al., [38] including SCEs. In the next year, W. Wu et al., developed a surface potential based PSP-SOI model for

partially depleted (PD) SOI MOSFET [39]. This model includes SOI specific effects by including floating body simulation capability, parasitic body currents and capacitances and nonlinear body resistance. Guohe Zhang et al., in 2008, proposed a novel approximation of 2-D potential function perpendicular to the channel FD SOI MOSFET with vertical Gaussian profile [40]. One year later, in 2009, Te-Kuang Chiang developed a new analytical sub-threshold behaviour model for the short-channel tri-material gate-stack SOI MOSFET [41].

In 2010, Weimin Wu et al., presented a complete surface-potential-based compact model of dynamically depleted SOI MOSFET [42]. Different technological solutions have been invented to fabricate some improved SOI MOSFET structure as they have received considerable attention in recent times [43-45]. In 1994, ST-Microelectronics invented the fabrication process [46] and Toshiba Electronics invented Empty Space in Si (ESS) process [47]. Silicon-On-Void (SOV) was created by Chinese Institute of Microelectronics [48].

A more efficient SON structure was developed by V. Kilchytska et al., [49], using Silicon layer transfer over a pre-etched cavity through wafer bonding technique. Based on famous work on fundamental computational limit by Lloyd in 2000, it is well understood that there remains the possibility of a huge improvement in computing capability with further miniaturization. But, this requires new innovative ideas to overcome these challenges physically as well as practically. Therefore, researchers have investigated several alternatives for future ultra-dense circuitry. As the devices go well beyond conventional semiconductor device technology, constant refinements in existing semiconductor technology and different quantum mechanical phenomena are adopted to make them function properly in nanometre regime. All these revolutionary nano-electronics devices have one essential structural feature in common that either there is a small “island” or “potential well or wire” in which carriers are confined. Using advanced fabrication techniques such as MBE and MOCVD, semiconductor structures with a precision of a single atomic layer that restrict the movement of the carriers to low dimensions, is grown. Depending on the extent and type of confinement of the electrons in the island, well or wire, revolutionary solid-state nano-electronic devices are classified into three basic categories. Recently researchers have studied some revolutionary nano-electronic devices as follows:

1. Carbon Nanotube Transistors
2. Carbon Nanotube Memory Devices
3. Quantum-Computing Devices
4. Single Electronic Devices
5. Spintronics
6. Magnetic Memory Devices

According to the report of The International Technology Roadmap for Semiconductors (ITRS) 2009, some probable evolutionary solid state transistor structures for present and future nano-electronics era,(e.g., 22 nm and 16 nodes) has predicted. Those include:

1. III-V channel replacement devices,
2. Ge channel replacement devices,
3. Unconventional Geometries for FET devices; Multiple Gate, Dielectric pocket incorporation, Strain Silicon, Work-Function-Engineering-Gate SON MOSFET etc.

1.3 Motivation:

Downscaling of silicon based MOSFET has almost reached its saturation limit due to increase in charge sharing between source and drain region which results in reduction of gate control over the channel depletion charges and also leads to the emergence of sever Short Channel Effects (*SCEs*). The major key issues in reducing the size of the CMOS transistor are: unacceptable leakage current which does not allow the further reduction in threshold voltage, higher electric field at the drain side which worsens the device reliability, punch through effect and enhance *Channel Length Modulation* (*CLM*) and *Drain Induced Barrier Lowering (DIBL)* Effect. This posed a fundamental limitation on the maximum performance improvement that can be achieved by down scaling the feature size of CMOS technology. Thus, due to those ever increasing *SCEs*, two major approaches are introduced to extend Moore's Law for CMOS devices and these are: (i) channel materials other than silicon to improve carrier transport properties and (ii) advance device engineering techniques to improve the electrostatics of CMOS.

Use of high-k material and new gate electrode material have improved carrier transport properties as well as new material in the source/drain region which reduced channel resistance and carrier injection properties of the device.

As suggested in the introduction section the newly prescribed DP-DG (ISE) MOS architecture [35, 50] explores a huge impact of evolution on surface potential, electric field, threshold voltage (*VT*), *Drain Induced Barrier Lowering* (*DIBL*), sub-threshold slope (*S*), drain current (*Ids*), trans-conductance (*gm*), device efficiency (*gm*/*Ids*) and *Voltage Transfer Characteristics* (*VTCs*) that greatly simplifies the device characteristics assessment. But in real time era, due to reduction of channel length and device dimension at sub micron (~ nanometre) regime, another important phenomena "Quantum Mechanical Effects (QME)" [51] would prevail the device characteristics. In this regime, the calculation of drain current, threshold voltage, sub-threshold slope including quantum effects become significant to observe the device characteristics and to obtain the accurate values of the device parameters. Thus in the initial section of present literature a Quantum Mechanical Model for ISE/ DP-DG MOSFET has been developed to study the various parameters in terms of 2-D Atlas simulation.

In the next section of this thesis work, efforts have been made to develop a superior model with reliability issues of ISE MOSFET that can be further suppressed by using lower work function of the metal gate near the drain side. Thus the impact of DMG on the performance of ISE MOSFET has been studied at nano-metric regime by including the effects of QME.

1.4 Organization of the Thesis:

This thesis is focused on a physics based quantum analytical modelling of Dielectric Pocket Double Gate MOSFET. A detailed modelling of overall potential profile of the body, inversion charge density and quantum threshold voltage, is therefore the main objective of this study.

Basics on Low Dimensional Device Structures are presented in **Chapter 2.** This segment explains the several problems as the device dimension goes to nano-meter

regime. Need for miniaturization and different Short Channel Effects (SCEs) associated with device miniaturization are also discussed in this section. Procedures to overcome these drawbacks are also discussed here including the need for new innovative device structures.

In the **Chapter3** a new structural concept of Double Gate MOSFET incorporating Dielectric Pocket (DP-DG) MOSFET has been developed. Conventional planner CMOS devices experienced several undesirable effects as the device dimension approaches to sub 20 nanometre regimes. To overcome these problems new alternative revolutionary nano-electronics devices were invented which works on the principle of quantum mechanics. This chapter is devoted to origin of quantization, basic principle of quantum mechanics, different types of carrier confinement in those MOS structures. Basic procedure of modelling the carrier concentration and corresponding drain current using self consistent solution of Schrödinger and Poisson's equation was introduced theoretically in this section. Thereby classical threshold voltage for this device has been formulated. Change in threshold voltage due to quantum effects has also been formulated and added to the original classical V_{th} to find the quantum counterpart.

In the **chapter 4** deals with all the results of the present work along with discussions of the quantum effects observed on the proposed DPDG MOSFET architecture. Different parameters such as transconductance, inversion charge, effects of quantum threshold voltage on channel length sub-threshold swing etc are also deduced in details. The results obtained from the analytical models are explained through graphical representation. The role of various MOS parameters like the gate length, applied drain and gate bias are taken into account. Superiority of DP DG MOSFET is established by the comparison of obtained device characteristics with other structure.

Finally, the conclusions and future work are described in the last chapter. Since the thesis deals with analytical modelling of DP DG MOSFET and comparative performance analysis of the same with DMDG SOI/SON, DMG and DP MOSFETs., validity of the model will be best understood when it will be cited in literature.

CHAPTER 2: BASICS ON LOW DIMENSIONAL DEVICE STRUCTURES

2. DEVICE SCALING
2.1 SHORT CHANNEL EFFECTS
2.2 DIFFERENT SCEs ASSOCIATED WITH DEVICE MINIATURIZATION
2.2.1 ELECTRIC FIELD
2.2.1.1 DIBL
2.2.1.2 V_T ROLL OFF
2.2.1.3 SURFACE SCATTERING
2.2.2 HIGH ELECTRIC FIELD STRENGTH
2.2.2.1 VELCITY SATURATION
2.2.2.2 HOT ELECTRON EFFECT
2.2.2.3 IMPACT OF IONIZATION NEAR DRAIN
2.2.2.4 PARASITIC BIPOLAR EFFECT
2.2.2.5 GATE OXIDE CHARGE
2.2.3 CHANNEL LENGTH MODULATION

2. DEVICE SCALING

The continuous improvisations in device miniaturization and concomitant increase in device density and circuit complexity on a single chip have realized the tremendous boost in the computing capability. Integrated circuit have become the fundamental building block in modern digital electronics and computing. The basic scaling rule of MOSFET was published by R. Dennard et al., [52]. Preserving the transistor performance with scaling down was the key of microelectronics technology evolution. The thumb rule of scaling consisted in the reduction of device size keeping the electric field in the silicon or silicon dioxide to such values as to avoid increased leakage current in MOS transistors and the breakdown fields in Si or SiO_2 materials. Depending on the scaling approach, the electric field in silicon can be constant or variable. To keep the electric field constant, according to this rule, the device dimension and supply voltage of MOSFET should be reduced by the same scaling factor S. The doping concentration should be increased by the same factor S. As a result, the electric field in MOSFET remains constant despite the technology node. Moreover, the circuit speeds up by the same factor S and the power dissipation per circuit is reduced by S^2.

Continuous downscaling of the device feature size per year and doubles the number of transistors on a LSI in every two years. In 19th April 1965, Gordon E. Moore predicted in his article “Cramming more components onto integrated circuits” , published in the Electronics magazine, by McGraw-Hill editors, that the number of transistors per each integrated circuit chip would continue to double every 24 months. A memory with a density of 65000 components was in production at Intel, ten years later, in agreement with Moore’s prediction. Depending on Moore’s law, the feature size is continuously shrinking as the transistor number increases and this trend will continue until a value of 14 nm in 2020.

In order to improve the packing density and the device performance, MOSFETs have been scale downed successfully over the past few decades. There are two primary device structures that have being studied and used for CMOS technology. One is the bulk structure, where a transistor is directly fabricated on the semiconductor substrate. The other is termed as SOI (Silicon-On- Insulator), where a transistor is built on a thin

silicon layer, which is separated from the substrate by layer of insulator. The bulk structure is relatively simple from the device process point of view, and it is still the standard structure in almost all CMOS based products.

In the traditional implementation of the bulk MOSFET, the gate electrode is made heavily (n or p) doped polycrystalline silicon. It is separated from the bulk silicon substrate by a thin insulating or dielectric layer of SiO_2. The channel region underneath the gate is moderately doped. The source and the drain regions, upon which the other electrode contacts are formed, are heavily doped to form n-p (or p-n) junctions to the oppositely doped substrate. The simplest transistor scaling approach involves reducing the vertical and horizontal dimensions, as well as the supply voltage, by the same factor in an attempt to keep the electric fields in the scaled MOSFET the same as before (contact-field scaling). However, actual scaling implementations have been based on slightly modified approaches where the geometry and voltages are reduced by different factors (generalized scaling).

In early generation transistors with large gate lengths (long channel MOSFETs), the vertical electric field in the channel (due to gate to source voltage) is much larger than the lateral channel electric field (due to drain to gate voltage). In such a case (gradual channel approximation), the physics of transistor operation can be divided into two independent halves, i.e. gate-controlled charge formation in the channel, and the drain-controlled charge transport. The Threshold voltage V_T, the voltage at which the device turns on, is dependent only on gate voltage. Application of the gate voltage lowers the potential barrier near the source and allows carriers to flow through the device. The subthreshold swing is a measure of how sharply the drain current increases as a function of gate voltage during switching from OFF to ON state, and measured in mV/dec. Under normal transistor operation, fundamental thermo-dynamical constrains the subthreshold swing to be greater than 60mV/dec at room temperature. Degraded 2-D electrostatics at short gate lengths increases this value which in turn leads to higher off-state leakage current for the same V_T. With the diminution of channel length as advancement of technological requirement, control of gate over the channel weakens due to enhances proximity between source and drain. As a consequence, Short Channel Effects (SCEs) become one of the major problems arise associated with the scale down MOSFETs, when the channel length is shrink to the order of source and drain depletion

layer width. SCEs lead to several reliability issues as the basic device parameters (e.g. V_T), become dependent on channel length. SCEs subjugate the controllability of the gate voltage over potential distribution in the channel and drain current, leading to reduction of subthreshold slope and increment of drain off current. This degradation is attributed to charge sharing by the drain and gate electric fields in the channel depletion layer as indicated in Poon and Yau's model, which is reported as the first SCE model [53]. These short channel effects are mainly described by two physical phenomena,

I. Limitation on drift characteristics of electron in the channel

II. Modification of threshold voltage due to shortening of channel length.

2.1 Short Channel Effect (SCE):

As the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the "**Short Channel Effects"** starts plaguing MOSFETs. For all practical purpose, it seems impossible to scale the dimensions of classical "bulk" MOSFETs below 20 nm. If that limitation cannot be overcome, Moore's Law would have been met to its end around 2015.

In reality, the potential barrier at the source is controlled by the gate as well as the drain through their respective coupling capacitances to that point. The gradual channel approximation is just a simplification of the complicated 2-D electrostatics in the MOSFET channel. While the simplification holds in long channel devices, as the gate length is reduced, the drain influence becomes stronger. As a result, it becomes harder for the gate to control the source barrier and turn off the channel. The 2-D effects can be manifested in various ways:

i. Reduction in threshold voltage with shrinking gate length (V_T roll-off).

ii. V_T reduction with increasing drain voltage (drain induced barrier lowering)

iii. Degraded subthreshold swing.

Collectively these phenomena are known as "**Short Channel Effects**" and these tend to increase the off-state static leakage power.

A simple tool, called the Voltage Doping Transformation (VDT) [54] can be used to render the effects of shrinking device parameters such as gate length or drain voltage into electrical parameters. In the particular case of short channel effect, the following expression can be achieved from the VDT model:

$$SCE = 0.64\frac{\varepsilon_{si}}{\varepsilon_{ox}}[1+\frac{x_j^2}{L_{el}^2}]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} \qquad (2.1)$$

Where L_{el} is the electrical/effective channel length, V_{bi} is built in potential, t_{ox} is gate oxide thickness, x_j is the source to drain junction depth and t_{dep} is the penetration depth of the gate field in the channel region, which is equal to the depth of the depletion region underneath the gate in a bulk MOSFET. The parameter EI is called "Electrostatic Integrity" factor. It depends on the device geometry and is a measure of the way the electric field lined from the drain influence the channel region, thereby causing SCE effects.

Thus far, device designers have tried to suppress SCE in short gate length devices by a number of methods:

i. Reducing the gate oxide thickness to improve the gate control over the channel,

ii. Lowering the source/drain junction depth (especially near the gate edge, where the source/drain regions are called extensions) to reduce the drain coupling to the source barrier.

iii. Increasing the channel doping to terminate the electric field lines which originate from the drain and propagates towards the source. In modern bulk MOSFETs, the channel doping is tailored to have complicated vertical and lateral profiles (super-halo doping) so as to minimize the impact of gate length variations on the short channel effects.

2.2Different Short Channel Effects (SCEs) associated with device miniaturization:

2.2.1 Electric field becomes two dimensional in nature:

In a small geometry MOSFET, the current flow in the channel between the source and the drain is controlled by a two-dimensional electric field vector. Therefore, the simple one-dimensional Gradual Channel Approximation (GCA) approach fails to account for some of the device characteristics observed in such a small-dimension. The physical consequences of the potential profile two-dimensionality can be understood as follows.

2.2.1.1 Drain Induced Barrier Lowering (DIBL):

As the dimensions of MOSFET are reduced to sub micron regime, the drain voltage prevails to make a stronger impact on the channel region and an adverse effect called **Drain Induced Barrier Lowering (DIBL)** starts acting upon MOSFETs. In weak inversion, the potential barrier between the source and the channel preserves the delicate balance between the drift and the diffusion currents. This barrier height for mobile carriers should ideally be mastered exclusively by the gate voltage in order to increase the transconductance to it maximum value [55]. In short channel device structure, DIBL is caused by the encroachment of the depletion region from the drain into the channel at high drain to source voltage (V_{ds}). Here, barrier height for channel carriers (at the edge of source) reduces by the influence of high drain electric field. The channel potential is strongly modified by this depletion region and the potential barrier between drain and channel lowers as the channel length is further reduced. That is why the term “barrier lowering” is used to identify these phenomena. Now, increased numbers of carrier are able to be injected into the channel from the source. As a result, the threshold condition is achieved at a lower gate voltage (V_{gs}) than the standard one since the drain has already created a large portion of the depletion region.

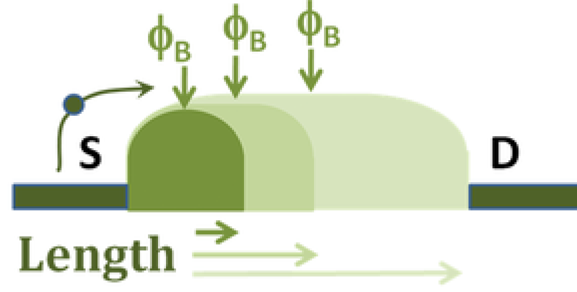


Fig 2.1: the barrier φ_B (φ_{B1}> φ_{B2}> φ_{B3}) which is to be crossed by an electron on its way from the source to the drain reduces as channel length is decreased

The effect of DIBL is more prominent in the subthreshold region and it can be modelled from the subthreshold current with the gate bias curve, as a simple change in the threshold voltage. But at extremely short lengths, the gate loses the entire control over the turning-off process of the device. Then, these effects are impossible to be modelled by a simple threshold adjustment model [56]. Apart from that, DIBL has an impact on the drain current with the gate voltage curve in the active mode, resulting a fall in MOSFET output resistance. At this condition, the maximum drain current is controlled not only by the gate voltage, but also by the drain voltage.

The strength of DIBL is measured as the difference in threshold voltage (V_T) between a low and high drain bias over a wide range of gate length [57]. Higher value of DIBL is a denotation of inferior short-channel features. In practice, DIBL can be calculated as:

$$DIBL = \frac{V_T^{dd} - V_T^{low}}{V_{dd} - V_{dd}^{low}} \tag{2.2}$$

Where V_T^{dd} is the threshold voltage measured at high drain bias, V_T^{low} is the threshold voltage measured at low drain bias, V_{dd} is the supply voltage and V_{dd}^{low} is the low drain voltage.

Also according to VDT model, DIBL can also be expressed as:

$$DIBL = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}}[1+\frac{x_j^2}{L_{el}^2}]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} \tag{2.3}$$

Where L_{el} is the electrical/effective channel length, V_{bi} is built in potential, t_{ox} is gate oxide thickness, x_j is the source to drain junction depth and t_{dep} is the penetration depth of the gate field in the channel region.

However, as the MOSFET is not normally operated at a low drain bias, DIBL itself is not a parameter which is directly related to device operation, but rather indicates the degradation of device performance such as strong threshold voltage roll-off and high off current (I_{off}) in subthreshold regime.

2.2.1.2 Threshold Voltage Roll-Off (V_T roll-off):

In order to achieve the threshold condition in MOS devices, the channel charge must be depleted by application of an appropriate bias in gate. But in short channel devices, due to the presence of SCE, DIBL the channel properties are influenced and modified by the drain voltage as much as by the gate voltage. As an outcome of this adverse coupling between the source/drain region and the channel, which becomes stronger as the gate length is reduced; threshold voltage is lower for MOSFET with shorter gate length.

Based on the expressions of (2.1) and (2.3), the threshold voltage (V_T) of a MOSFET can be represented as:

$$V_T = V_{T\infty} - DIBL - SCE \tag{2.4}$$

$V_{T\infty}$ is the threshold voltage of a device where SCE is not applicable. The declination of the threshold voltage inferred by the reduction of gate length produces the adverse effect called the "**Threshold Voltage Roll-off**".

2.2.1.3 Surface Scattering:

Due to the lateral extension of the source and drain depletion layer into the channel region, the effective channel length flinches when the transistor dimensions are cut down. As a consequence, the longitudinal electric field component yielded by drain to source voltage $\mathcal{E}_y$, increases; hence the surface mobility essentially becomes field-dependent (Fig. 2.2). The surface scattering (which is resulted from the collisions of mobile carriers in the channel by the influence of $\mathcal{E}_x$) causes reduction in the mobility as the carrier transport in a MOSFET is confined within the narrow inversion layer. In the direction parallel to the interface, carriers move with great difficulty leading to

average surface mobility which is about half as much as that of the bulk mobility even for small values of $\mathcal{E}_y$.

2.2.2 High Electric Field Strength:

If the applied voltage is not reduced considerably, with the continuous scaling down of the channel length, the channel electric field increases substantially [58]. This result in breakdown and some other effects in short channel devices as discussed below.

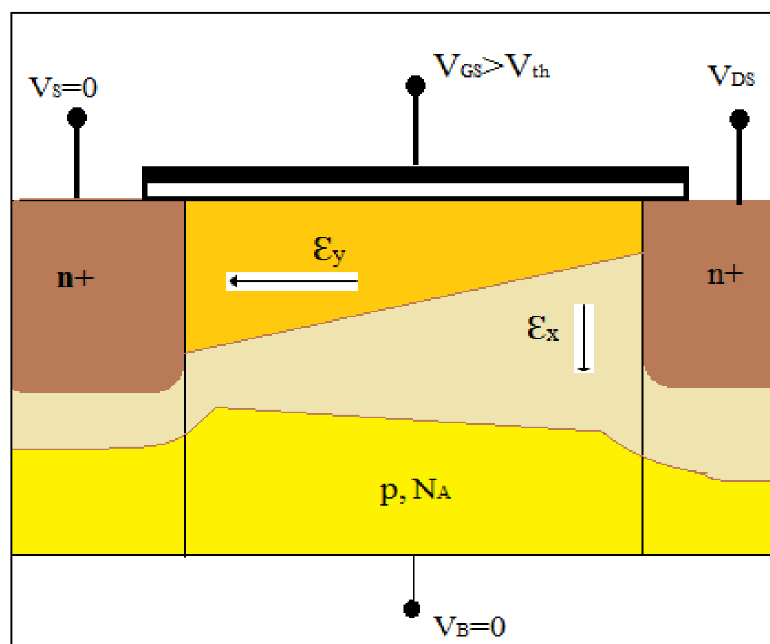


Fig. 2.2: Cross section view of MOSFET

2.2.2.1 Velocity saturation

Another outcome of channel length reduction is the "velocity saturation" which results from the presence of high lateral electric field ($\mathcal{E}_y$) in the channel. At low $\mathcal{E}_y$, the drift velocity of mobile carriers in the channel varies linearly with the electric field intensity. However, as $\mathcal{E}_y$ increases above 10^4 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of 10^7 cm/s around $\mathcal{E}_y$=10^5 V/cm at 300 K. The performances of the devices where the channel length is short, the parameters

are affected by velocity saturation. Here, the drain current is limited by velocity saturation leading to reduction of the transconductance in the saturation mode. After incorporating velocity saturation, the maximum transconductance (g_m) achievable by a MOSFET can be defined as

$$g_m = WC_{ox}V_{ds(sat)} \tag{2.5}$$

2.2.2.2 Hot Electron Effects:

Another important consequence of the high source-drain electric field strength is the strong carrier heating associated with this field. Due to short channel length, electrons cannot release its excess energy gained from the high electric field at the drain. This excess energy heated up the electrons giving rise to “hot electrons”. The term “hot electron effects” was first coined by Conwell et al., [59] to describe non-equilibrium electrons in semiconductor. In this case electrons obey “drifted heated Fermi Dirac distribution” rather than Fermi Dirac distribution. Electron distributions can be represented by the Fermi function with a higher effective temperature. However, this concept is not so relevant for metals because the electron mobility does not vary significantly with their energies. However, in case of semiconductors, the carrier mobility varies considerably with the effective temperature making the “hot-electron” phenomenon very much prolific. This effect is seen where the electrons are able to rise above the conduction band. As the “hot” electrons have sufficient kinetic energy, instead of being conducted through the material to a collector or recombining with holes, the ‘hot’ electrons can penetrate the semiconductor material. These electrons give away their excess energy in the form of phonons. In MOSFETs, it can also be noticed that these ‘hot’ electrons may jump from the drain to the gate or the substrate, consequently heating up the devices and increasing the device leakage currents.

2.2.2.3 Impact ionization near the drain:

High drain-source voltage in short channel device give rise to another undesirable SCE namely impact ionization near the drain. The chance of occurrence of impact ionization is greater in n-MOS than in p-MOS due to higher mobility of electrons. In short channel MOSFETs the if electric field strength near the drain exceeds the minimum value, electron with enough kinetic energy can knock a bound electron out of its bound state and promote it to a state in the conduction band, giving rise to the formation of an electron-hole pair.

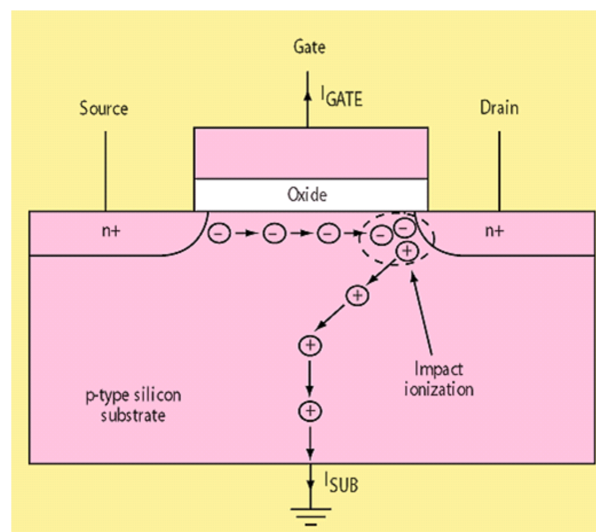


Fig.2.3: Generation of electron-hole pair through Impact Ionization

Under this high channel electric field, most of the electrons are attracted towards the drain end and the holes reach the substrate to form a portion of the parasitic substrate current. The region between the source and drain can act as the base of an n-p-n BJT where the source and drain plays the role of emitter and collector respectively with the substrate region acting as the base. This hole generated from avalanche breakdown creates a voltage drop in the substrate material. If this drop created by hole current becomes as high as 0.6 V, substrate-source junction gains a forward bias and conducts a significant current. Then similar to the injection of electrons from emitter to base in a BJT, electrons can be injected from the source to the substrate. As the electrons travel

towards the drain, they can gain enough energy to create new electron-hole pairs making impact ionization a cumulative process. This process is depicted in Fig.2.3.

2.2.2.4 Parasitic Bipolar Effect:

The impact ionization at the drain end causes carrier multiplication which results in hole injection into the substrate. These injected holes serve the purpose of forward biasing the source substrate junction giving rise to Parasitic Bipolar Effect. The holes injected into the substrate increases the net positive charge within the p-type substrate which induces a positive bias on the substrate with respect to the grounded source forward biasing the p-n junction. This forward bias encourages further injection of electrons (as minority carriers) from the source to the p-type substrate underneath the inversion layer which effectively increases the drain current. These electrons arrive at the drain and again create more electron-hole pairs through avalanche multiplication. The net positive feedback existing between the avalanche breakdown and the parasitic bipolar action results in breakdown at lower drain voltage.

2.2.2.5 Gate Oxide Charging:

High electric field in the channel becomes sufficient to heat up the channel electrons to a high kinetic energy such that they can transfer from the semiconductor channel into the gate oxide. These carriers slowly degrade the quality of the oxide and significantly alter the device threshold voltage and may lead over time to failure of the oxide. So, breakdown of oxides and oxide reliability becomes two major concerns, with the gradual scaling down of device dimension. This type of short-channel effect in low dimensional devices is termed to as time dependent destructive breakdown (TDDB) or hot electron aging. Oxides other than silicon dioxide having larger dielectric constants have been considered as alternate oxides and are typically referred to as high-k dielectrics. Due to the larger dielectric constant of these high-k dielectrics, the same gate capacitance can be obtained with a thicker oxide. However, the challenge in using these alternate oxides lies in obtaining the same stability, reliability and breakdown voltage as silicon dioxide. Oxides of interest include Al_2O_3, ZrO, TiO and HfO_2.

2.2.3 Channel Length Modulation (CLM):

One of several short-channel effects in MOSFET scaling, **channel length modulation** (**CLM**) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance. Channel length modulation occurs in all field effect transistors, not just MOSFETs.

To understand the effect, first the notion of **pinch-off** of the channel is introduced. The channel is formed by attraction of carriers to the gate, and the current drawn through the channel is nearly a constant independent of drain voltage in saturation mode. However, near the drain, the gate and drain jointly determine the electric field pattern. Instead of flowing in a channel, beyond the pinch-off point the carriers flow in a subsurface pattern made possible because the drain and the gate both control the current. In the figure at the right, the channel is indicated by a dashed line and becomes weaker as the drain is approached, leaving a gap of uninverted silicon between the end of the formed inversion layer and the drain (the *pinch-off* region).

The resulting channel length is approximately equal to the metallurgical channel length minus the source and drain depletion region width. This result in an output conductance defined as the nonzero slope of the drain-current versus drain voltage for the device. The channel-length-modulation effect typically increases in small devices with low-doped substrates. The punch-through effect is an extreme case of channel length modulation where the channel length reduces to zero. The channel length modulation can be reduced by proper scaling and by increasing the doping density as the gate length is reduced.

Another important phenomena occurs in operation of MOSFET is Punch through. Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate becomes strongly dependent on the drain-source voltage. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is obviously undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

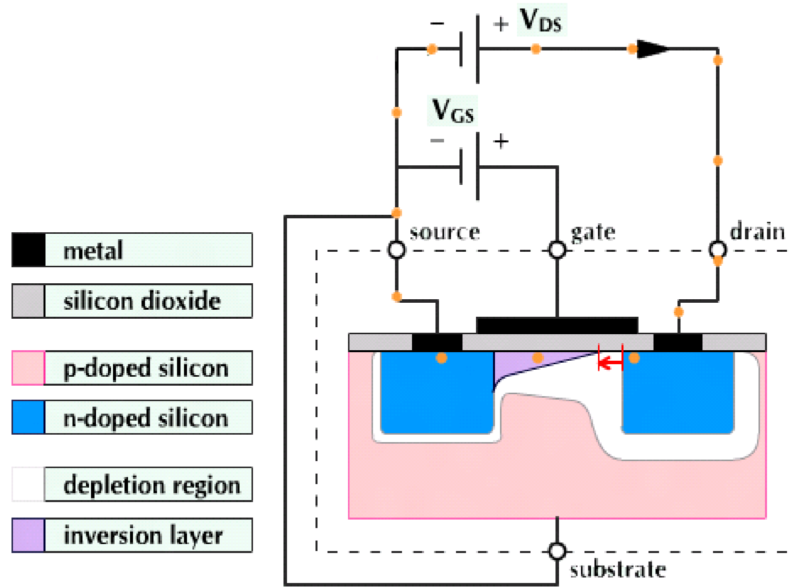


Fig.2.4: Channel Length Modulation in a MOSFET

CHAPTER 3: THRESHOLD VOLTAGE MODELLING OF DP-DG MOSFET INCORPORATING QUANTUM MECHANICAL EFFECTS

3.1 IMPACT OF DIELECTRIC POCKETs

3.2 QUANTUM CONFINEMENT IN MOSFETs

3.2.1 TYPES OF QUANTUM CONFINEMENTs

3.3 PROPOSED STRUCTURE OF DP-DG MOSFET

3.4 ANALYTICAL MODELLING

3.4.1 INVERSION CHARGE MODELLING

3.4.2 THRESHOLD VOLTAGE MODELLING

3.4.2.1 CLASSICAL THRESHOLD VOLTAGE MODELLING

3.4.2.2 QUANTUM THRESHOLD VOLTAGE MODELLING

3.1 IMPACT OF DIELECTRIC POCKETS

According to ITRS, scaling of CMOS structures below 90nm gate length requires advanced lateral channel engineering techniques to overcome the effect of high gate leakage current. Dielectric Pocket (DP) implantation is one of the several interesting and well established advanced lateral channel engineering techniques for modern nano devices. Pocket implantation such as super halo or steep halo has been proposed to shield the electric field penetration from the drain to source region. However, this technique may results in an increased threat of avalanche breakdown and band to band leakage current. As stated before, the Dielectric Pocket (DP) MOSFET received serious attention in the last few years to meet the aforementioned challenges while retaining the high heat dissipation ability of Bulk CMOS. In order to overcome the device performance degradation at sub-100 nm regime, extensive consideration has been devoted to explore the potential benefits of two non-classical devices i.e. ISE/DP and SON MOSFET to form a single device design i.e. Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET.

Thereafter, the emphasis has been shifted towards multi gate MOSFET design i.e. Double Gate (DG) MOSFET to further enhance the gate controllability over the channel region and to eliminate floating body effect arising in bulk MOSFET. DG MOSFET possesses higher channel mobility because of undoped silicon body and avoids undesirable effect of threshold voltage roll-off arising due to channel dopant fluctuation. However, the DG MOSFET suffers from enhance parasitic (gate to source (C_{gs}) and gate to drain (C_{gd})) capacitances as compared to bulk MOSFET. In order to overcome this problem, Dielectric Pockets were placed at side wall of DG MOSFET resulting in new device design known as Dielectric Pocket Double Gate (DP-DG) MOSFET. This significantly decreases the parasitic capacitance and also reduces the dopant-out diffusion from the Source/Drain to the channel region.

In addition, CMOS circuit design demands the accurate modelling of non-classical devices for describing the behaviour of various electrical parameters prior to the device fabrication. This requires exact solution of the basic semiconductor equation i.e. Poisson's equation, continuity equation, current transport equation and other related

equations. The solution of these equations invariably involved numerical analysis. The situation becomes even more complex for nano-scale devices where 2- dimensional or 3- dimensional effects are to be accounted in modelling. Thus, a two dimensional analytical model which can give approximately same results as obtained from the device simulation within acceptable tolerance would be very useful. Furthermore, in nano-scale regime, the process variation has also major impact on the device behaviour.

The present literature mainly focuses on the modelling and simulation of a novel non-classical architecture, DP-DG MOSFET and thereby including the quantum mechanical effects along the channel region tries to improve the electronic characteristics of this present architecture proposed by Kumai et al., [2012].

In the DP-DG architecture, the impact of insulating layers on the single gate device geometry architecture is presented by combining the features of two advance MOSFET designs i.e. Insulated Shallow Extension MOSFET and Double Gate MOSFET resulting in new device architecture known as Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET. The physics behind the operation of proposed DP-DG MOSFET is explored by developing an efficient two dimensional analytical channel potential model. The model is further extended to derive the temperature dependent drain current expression from sub-threshold to saturation region[35]. The performance of the device has also been analysed at different channel length, drain bias, channel thickness and side pillar thickness. The unique features of DP-DG MOSFET i.e. higher immunity against temperature variation with electrical parameters like threshold voltage roll-off, sub-threshold slope and DIBL have been studied in this literature.

In addition, this study also deals with the development of a 2-D analytical model for DP-DG MOSFET design which account for the impact of quantum molecular effect on the threshold voltage, sub-threshold slope and DIBL.

Continuous scaling of the MOSFET dimensions has made silicon technology viable for high-performance logic, memory and RF applications. However this adversely affects the analog performance of the device. Extensive consideration has been given to analyze the performance of various non-classical devices such as Dual Gate (DG) MOSFETs, Silicon On Nothing (SON) and DP-DG MOSFETs for high temperature analog performance through extensive device simulations. Results reflect

that ISESON MOSFET shows better immunity against temperature variation in terms of *gm/Ids* ratio, early voltage, output resistance and device gain thus proving its efficacy for low-voltage low-power analog applications[35]. The use of gate stack architecture (high-k/SiO_2) further helps to increase the on-current (*Ion*) and bring out a simultaneous reduction in off-current (*Ioff*), thereby greatly increasing the *Ion/Ioff* ratio, which is an indicator of better switching characteristics in digital circuits. Also the much better linearity performance i.e. higher *VIP2*, *VIP3* and *IIP3* is seen in case of DP-DG MOSFET as compared to ISE and SON MOSFETs even at the high operating temperature[35].

3.2 QUANTUM CONFINEMENT in MOSFETs

As MOSFET scaling being challenged by quantum mechanical effects, short channel effects (SCEs) became critical issue while device modelling. In that circumstance, further downscaling of MOSFETs in the deep sub-micrometer domain requires ultrathin oxides and high channel doping to minimize the drastic increase of SCEs. The increment of substrate doping and shrinking of gate oxide thickness effects consequences an enhancement of the field strength at the Si/SiO_2 interface which creates a sufficiently steep potential well for inducing the quantization of carrier energy as shown in Fig.3.1 [59].

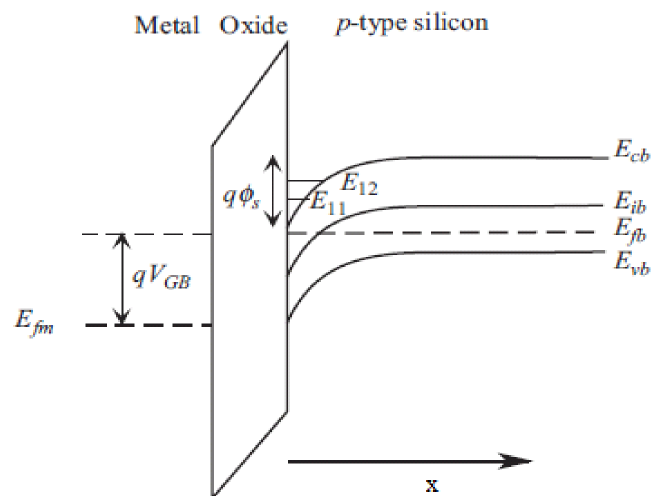


Fig. 3.1: Carrier energy quantization at the Si–SiO_2 interface in a MOS capacitor

Carriers are then confined in a vertical direction in a quantum well which was formed by the silicon conduction band bending at the interface and the oxide/Si conduction band-offset. As the wavelengths of the inverted carriers in the potential well are comparable to the feature size of the well width, behaviour of the carriers in such a potential well is governed by quantum mechanics. From the laws of quantum mechanics it is known that the allowed energies are quantized in the direction of confinement (x-direction). This results a splitting of the energy levels into sub-bands, such that the lowest of the allowed energy levels for electrons in the well does not coincide with the bottom of conduction band.

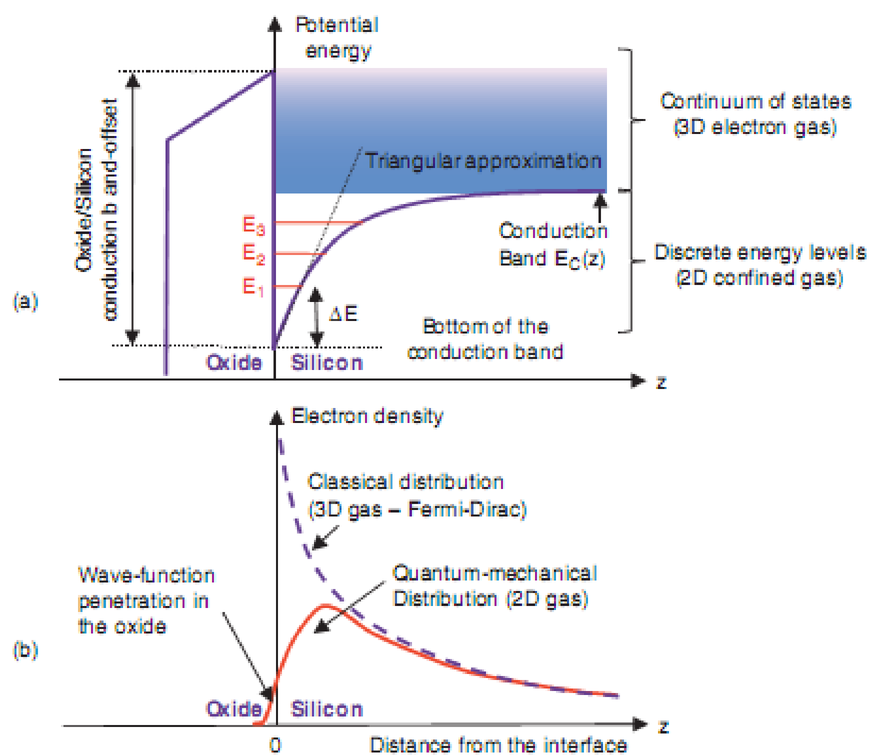


Fig. 3.2: (a) Schematic illustration of the conduction band bending of a bulk and PD SOI MOSFET in inversion regime showing the different energy levels resulting from the quantization effects of the 2-D electron gas confined in the surface potential well. (b) Corresponding electron distributions in the direction perpendicular to the interface for the classical and quantum-mechanical case.

Carriers residing at lowest energy levels behave like quantized carriers while those residing at higher energies, can behave like classical (3-D) particles with three degrees of freedom as they are not as tightly confined in the potential well. This can be explained from the Fig.3.2. Further rise of the surface electric field pushes away the

maximum of inversion charge from the interface into Si film and the system becomes more quantized with more carriers confined in the potential well. Therefore, quantum-mechanical confinement modifies the carrier distribution considerably from 3-D or classical system to 2-D system. As the total density-of-states in a 2-D system is less than that in a classical system, total population of carriers will be smaller for the same Fermi level than in the corresponding 3-D system. Thus higher gate voltage is required to populate a 2-D inversion layer to have the same number of carriers as the corresponding 3-D system, leading to an increase of the threshold voltage of a MOSFET.

3.2.1 Types of Quantum Confinement:

Carriers in ultrathin MOSFET are confined due to two main phenomena namely electrical confinement and structural confinement as depicted in Fig. 3.3

1. Strong electric field at the interface leading to electric field-induced quantum confinement (EC-QM).
2. t_{Si}-induced structural quantum confinement (SC-QM) due to the narrow potential well defined by thin Silicon film.

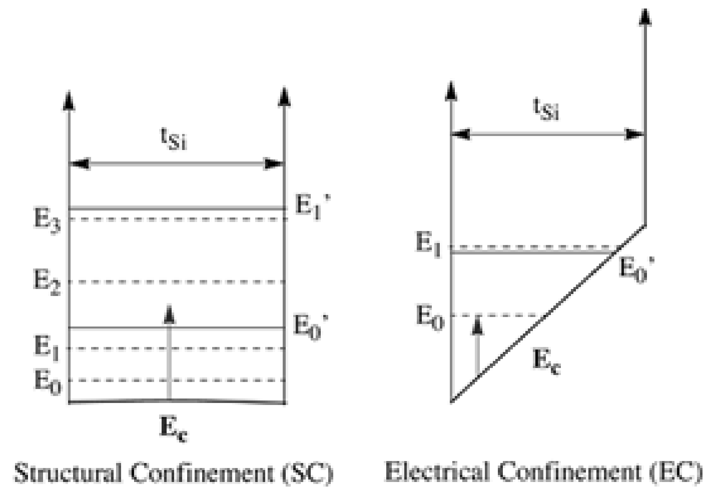


Fig. 3.3: Energy-band diagrams in a vertical cross-section in the Silicon film of DG n-channel MOSFETs showing two possible cases of carrier confinement: i) electric field-induced quantum confinement (EC-QM) and ii) t_{Si}-induced structural confinement (SC-QM) due to the narrow potential well defined by thin Silicon film

Carriers in thin-film DG MOSFET and ultrathin short channel DP-DG MOSFETs are subjected to both structural confinement as well as electric field-induced quantum confinement.

Further downscaling of the oxide thickness reduces the width of the SiO_2 potential barrier and eventually results an decrement of separation of the carriers in the semiconductor from the gate terminal. With the reduction of the width of the barrier, the quantum tunnelling probability of carriers through the barrier enhances. In that circumstances the gate oxide which acts as an insulating material in classical mechanically, no longer holds good in the presence of tunnelling. In my present thesis, gate current due to tunnelling phenomenon is neglected. Behaviour of trapped electron in triangular or rectangular potential well can be analyzed by only self-consistent solution of the Schrodinger and Poisson equation.

Potential in the bulk semiconductor varies periodically in all three dimensions. With the help of effective mass approximation we can neglect the variation in y and z directions. So, $V_E(\vec{r})$ can be equated to $V_E(x)$ only in x directions [60]. Using the effective mass approximation, the electron wave function can be written as the product of the Bloch function at the bottom of the conduction band and an envelope function. Schrodinger equation can be written as [61]:

$$-\frac{\hbar^2}{2m_{l,t}^*}\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)\psi+V(x)\psi=E\psi \tag{3.1}$$

Electron wave function can be written as

$$\psi(x,y,z)=\psi_x(x)\psi_y(y)\psi_z(z) \tag{3.2}$$

Finally the Schrodinger equation becomes

$$-\frac{\hbar^2}{2m_{l,t}^*}\left(\frac{\partial^2\psi_x}{\partial x^2}\psi_y\psi_z+\frac{\partial^2\psi_y}{\partial y^2}\psi_x\psi_z+\frac{\partial^2\psi_z}{\partial z^2}\psi_x\psi_y\right)+V(x)\psi_x\psi_y\psi_z=E\psi_x\psi_y\psi_z \tag{3.3}$$

Here E is the total energy which is the summation of energies in all three directions and E can be expressed as $E=E_x+E_y+E_z$. Decoupling the equation (3.3)

we can get the corresponding Schrodinger equation for all three dimensions as follows:

$$-\frac{\hbar^2}{2m_{l,t}^*}\frac{\partial^2\psi_x}{\partial x^2}+V(x)\psi_x=E_x\psi_x \tag{3.4}$$

$$-\frac{\hbar^2}{2m_{l,t}^*}\frac{\partial^2\psi_y}{\partial y^2}=E_y\psi_y \tag{3.5}$$

$$-\frac{\hbar^2}{2m_{l,t}^*}\frac{\partial^2\psi_z}{\partial z^2}=E_z\psi_z \tag{3.6}$$

Electron kinetic energies in the paraboloids are depicted in the Fig.3.4. Kinetic energy along the direction of motion of electron can be expressed as

$$E_x=\frac{\hbar^2k_x^2}{2m_x}$$

Finally the potential profile as well as carrier concentration of confined electrons (for n-channel MOS) can be found from the coupled one dimension Schrodinger-Poisson equation

$$\frac{d^2\phi(x)}{dx^2}=\frac{qN_A(x)}{\varepsilon_{si}}-\sum_i\frac{Q_{inv,i}}{q\varepsilon_{si}}\left|\psi(x)\right|^2 \tag{3.7}$$

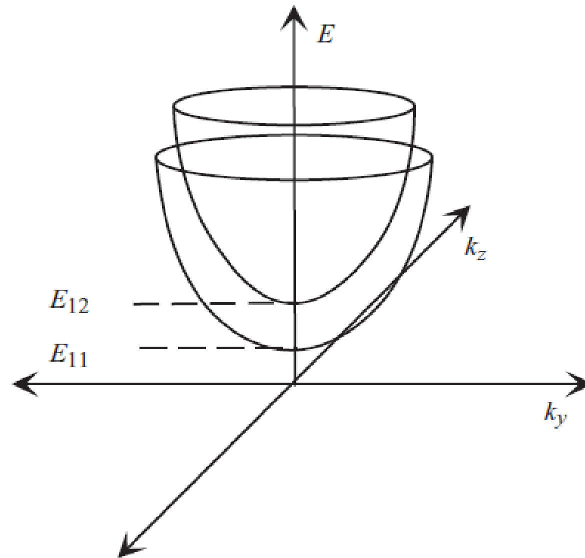


Fig.3.4: Bell-shaped paraboloids showing the total energies including transverse kinetic energies for the first two sub-bands

Where $Q_{inv,i}$ is the inversion charge sheet density of the ith sub-band and $\psi(x)$ is the carrier wave function on the ith sub-band. Carrier wave function is already defined in eqn 3.4. $\phi(x)$ is the surface potential which is found removing the y variable from the 2D Poisson equation. $m_{l,t}^{*}$ is the effective mass of electrons, which is determined by the crystal orientation and band structure of the silicon. As the sub-band energy varies according to the effective mass of the electrons, different effective masses along longitudinal and transverse valley are considered. The Si-SiO_2 interface is considered to be parallel with the [100] plane of the silicon, by which MOSFETs best performance is obtained.

3.2.1.1 Inversion Charge model:

Classical Inversion Charge is derived from the integration of the electron charge density over the entire film thickness. Expression of electron density is found assuming a 3-D distribution of carriers, governed by the Maxwell-Boltzmann statistics. Quasi Fermi level $V_F(x)$ of single gate MOSFET for both classical as well as quantum case is defined as [69]

$$V_F(x) = -\frac{k_B T}{q}\left(\frac{m}{n}\right)\times\times\ln\left[\exp\left\{\left(-\frac{V_D\left(\frac{m}{n}\right)^{-1}}{\frac{k_B T}{q}}\right)-1\right\}\left(\frac{x}{L}\right)^{\frac{C_1}{V_g - V_{FB}}}+1\right]\left(a_1 t_{si}\right)^{\frac{V_D}{3c_1}} \quad (3.8)$$

$$\left(\frac{m}{n}\right) = 2 + b_1\left(V_G - V_{FB}\right)$$

Where $a_1 = 0.2\ nm^{-1}$, $b_1 = 0.05/V$, $c_1 = 1/V$.

The quasi-Fermi level varies between $V_S = 0$ at the source end and V_D at the drain end and has a linear variation in the channel for low drain voltages.
According to quantum theory, electrons in the potential well behaves as 2-DEG and their kinetic energy in the direction perpendicular to the surface is quantized. It is essential to analyze the electron wave function to finally derive the inversion charge expression. Electron wave function can be determined by solving Schrödinger’s and

Poisson's equation self-consistently. In quantum mechanical (QM) approach Schrödinger equation for our potential well can be written as

$$\frac{\partial^2\psi(y)}{\partial y^2}+\frac{2qm_{l,t}^*}{\hbar^2}(E_{i,trian,l,t}-E_0))\psi(y)=0 \tag{3.9}$$

Here, $E_{i,trian,l,t}$ is the Eigen energy for electron residing in ith sub-band in the potential well $\psi(y)$ is the electron wave-function and E_0 is the electrostatic potential energy of the electron residing in the potential well. The energy levels are created according to the carrier confinement and it depends on the nature of potential well as well as doping.

3.2.1.2 Threshold Voltage Model:

Classical model defines the threshold voltage as the gate voltage corresponding to the condition when the surface potential Φ_S equals to twice multiplication of Fermi potential $2\Phi_B$ .Fermi potential is defined as,

$$\phi_B=\frac{KT}{q}\ln\left(\frac{N_A}{N_i}\right) \tag{3.10}$$

As a consequence the inversion charge density at the surface is equal to the doping concentration at the threshold and beyond that voltage the surface is inverted. According to the prediction of classical theory, when silicon film thickness is decreased keeping the doping concentration constant, the threshold voltage decreases in a fully depleted SOI MOSFET [51]. This result can be explained classically by the reduction of depletion charge qN_at_{Si}, in the channel when the film thickness is decreased. However, practically when the film thickness is below 10 nm, the depletion charge is very small and can usually be neglected. Carrier distribution is also changed significantly from 3D free electron to 2 DEG (Two Dimensional Electron Gas). In this case, two non-classical contributions to threshold voltage have to be taken into account. The first contribution comes from the fact that the concentration of inversion carriers needs to be bigger than what classical theory predicts in order to reach threshold. Thus the potential in the thin silicon film is larger than the classical potential.

The second contribution arises from the splitting of the conduction band into sub-bands. The lowest sub-band is well above the bottom of the conduction band when the energy is quantized. Hence the concentration of inversion charge is much lower than in classical case with the assumption $\Phi_S = 2\Phi_B$. In order to invert the carriers the required band bending for quantum case is larger than $2\Phi_B$. So, extra amount of gate voltage is required to generate the band bending [70-71]. If the thickness of the film is further decreased, the minimum energy of the sub bands i.e. the minimum energy in the conduction band as well as the separation of the sub band increases, which indicates more higher gate voltage is required to reach any particular inversion carrier concentration compared to classical case. This causes the threshold voltage to increase in quantum case. This phenomenon of threshold voltage in quantum case was first reported in 1993 by Omura et al., [72] and later has been confirmed and measured by several research groups. As the threshold condition $\Phi_S = 2\Phi_B$ is not appropriate in quantum model, threshold voltage is defined for consistency of the classical model as the gate voltage at which the inversion charge reaches the amount predicted by classical theory. Variation of quantum as well as classical threshold voltage with the thickness of the channel is depicted in Fig.3.5.

$$Q_{INV,QM}(V_{GS}=V_{TH,QM})=Q_{INV,CL}(V_{GS}=V_{TH,CL}) \quad (3.11)$$

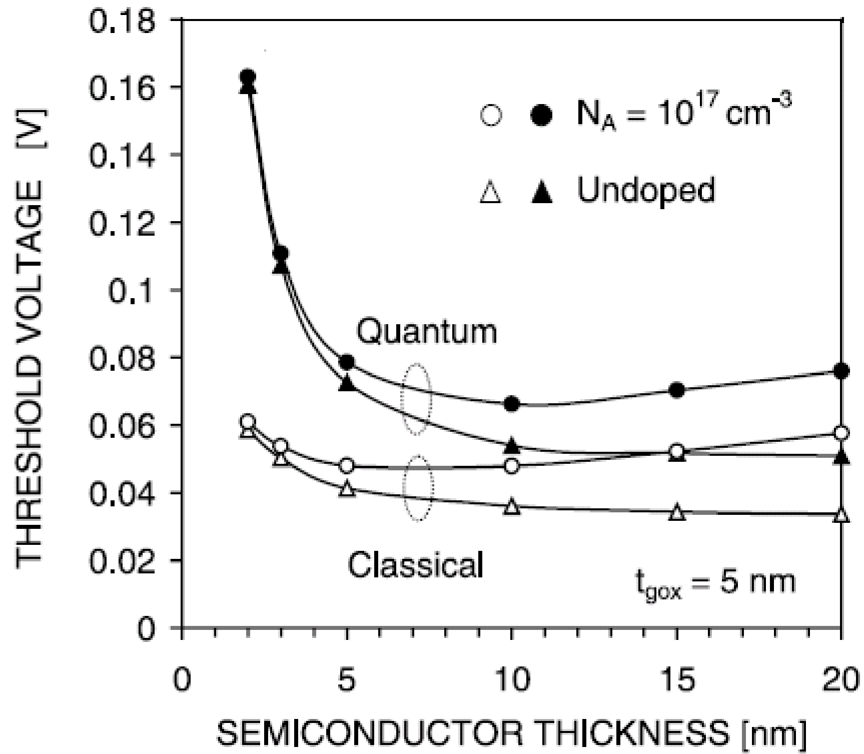


Fig.3.5: Variation of threshold voltage vs thickness of the Si film

3.2.1.3 Effects of Quantum Confinement:

As the thickness and/or width of a MOSFET is reaching below 10 nanometres, behaviour of electrons cannot be explained from classical theory and quantum mechanical effects start to influence in several phenomena in MOSFET resulting the formation of energy sub-bands. Electrons in the silicon film behave as two dimensional electron gas which is significantly different from three dimensional bulk electrons as predicted by classical theory. In case of multi-gate FETs, when the thickness is reaching values that are less than 10 nanometres, the electrons in the “channel” form either a two-Dimensional Electron Gas (2DEG) in case of double-gate device or a one-Dimensional Electron Gas (1DEG) in case of triple or quadruple-gate MOSFET.

3.3 PROPOSED STRUCTURE of DP-DG MOSFET:

Sufficient research outcomes related to DP architectures have been published in the last decade. One of the pioneer literatures on DP architecture had been published by Donaghy *et al.,* [62], where with 50-nm channel length and 350-nm channel width a vertical transistor incorporating DP was demonstrated in details. In next few years 50- and 70-nm vertical MOSFETs with DP (DPV MOSFETs) were also proposed by Jayanarayanan *et al.,* [62] and Gili *et al.,* [63]. But those proposed models have several architectural limitations as (1) for the processing furnace thick gate oxide has been required for DPV, and(2) higher channel doping ~ 10^{18} cm^{-3} is required for DPV architecture. In 2012 Kumari *et al.,* proposed a new architecture by incorporating dielectric pockets in a dual gate MOSFET to rectify the alleviate limitations. The structure proposed by them was found to exhibit better subthreshold performance compared to previous proposed DP MOSFET models. Being motivated by the improved features of this DP-DG structure, quantum mechanical effects have been incorporated in a nano scale DP-DG MOS structure and performed the detailed quantum analytical modelling. In DP-DG MOSFET, dielectric pocket has been introduced at the interface of the channel and the S/D region (inside the source/drain region) as shown in figure 3.6. Thus the DP-DG MOSFET combines the advantages of both DG and DP MOSFET. The advantages of the DP-DG MOSFET over conventional devices are: 1) enhanced gate controllability 2) lower sub-threshold slope and threshold voltage roll-off and 3) suppression in hot carrier effects due to lower drain side electric field.

The schematic cross section for the proposed DP-DG MOSFET is depicted in figure 3.6. The proposed structure has a single material front gate and a back gate is fabricated along with two dielectric pockets incorporated at the drain-channel and channel-source junction, respectively. In the figure the channel length is represented by L. The front gate oxide thickness, back gate oxide thickness and the corresponding film thickness are denoted as t_f, t_b and t_{si} respectively.

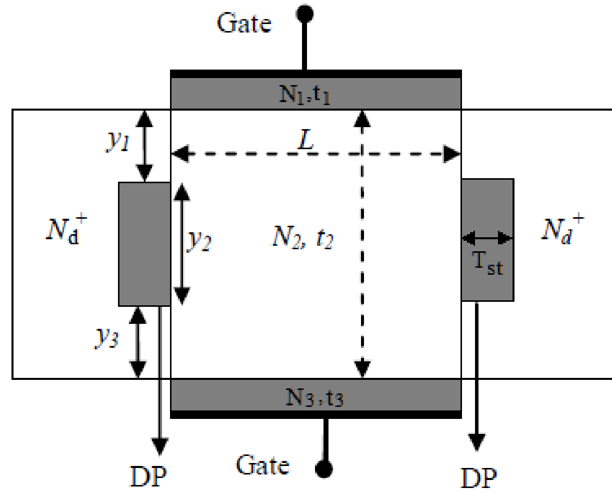


Fig. 3.6: Schematic diagram of DP-DG MOSFET: L is the Channel Length, t_1 and t_3 are front and back gate oxide thickness & $t_2(t_{si})$ is the channel thickness & y_1 and y_3 represent the shallow extension depths & T_{st} represents the thickness of the DP. N_1, N_2 (N_a), N_3 represent upper gate oxide, channel, lower gate oxide doping concentration respectively

The shallow extension depths and the thickness of the Dielectric Pocket incorporated in the structure are represented by y_1, y_3 respectively where as y_2 is the length of the DP and T_{st} is the thickness of those dielectric pockets. Both the source and drain regions are highly doped while the channel doping is kept low in the architecture. This quantum analytical modelling scheme of DP-DG architecture may serve as a useful tool for device physics and design with better optimization in channel length and thickness down to deca-nanometre.

According to Jurczak *et al.* and Kaur *et al.* [65-66], Dielectric Pockets (DP) are present mainly inside the source and drain regions and its advantages have also been discussed. For fabricating the vertical Dielectric Pocket MOSFET, two methods are reported in the literature:

1) *Case I)*:- Dielectric Pocket is present at the side wall of the drain region i.e. completely inside the drain region fabricated by Gili *et al.* as shown in figure 3.7 (a).
2) *Case II)*:- Dielectric Pocket is present at the interface of the source/drain and channel region i.e. partially inside the channel and partially inside the drain region fabricated by Jayanarayanan *et al*. as shown in figure 3.7 (b).

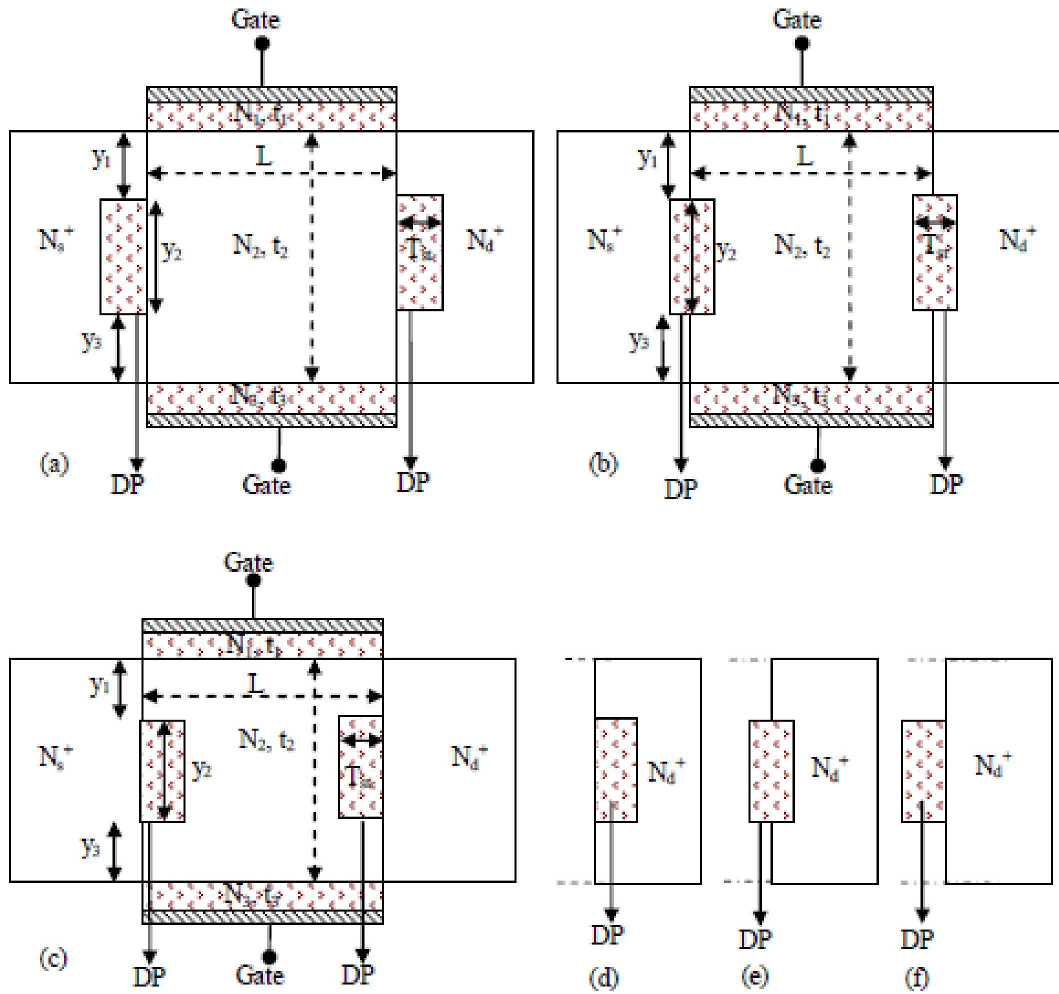


Fig 3.7: (a) Case I: Schematic cross section of Double Gate MOSFET incorporating Dielectric Pocket (DP-DG): L is the channel length, t1 and t3 represents the front and back gate oxide thickness, t2 is the channel thickness. y1 and y3 represents the shallow extension depth and Tst is the thickness of the DP, N1, N2 and N3 are the doping in the upper gate oxide, channel region and lower gate oxide respectively, Ns + and Nd + are the source and drain doping equal to 1026 m-3; (b) Case II: DP-DG MOSFET with Dielectric Pocket at the interface of S/D regions (i.e. partially inside the S/D region and partially inside the channel region) and both at the S/D region (c) Case III: DP-DG MOSFET with Dielectric Pocket in the channel and at both source and drain regions, (d) Case IV: DP-DG MOSFET with Dielectric Pocket at the drain side only (e) Case V: DP-DG MOSFET with Dielectric Pocket at the interface of S/D regions (i.e. partially inside the S/D region and partially inside the channel region) and at drain side only (f) Case VI: DP-DG MOSFET with Dielectric Pocket in the channel region and at the drain side only

The position of the dielectric pocket can also be changed due to process variation i.e., inside the channel region. Thus, in addition to above two cases, one more case is considered in this literature as:

3) Case III):- Dielectric Pocket is present completely inside the channel region as shown in figure 3.7 (c).

Also, it can be observed that, Dielectric Pocket in case of vertical MOSFET has been present only at the drain side. Thus three more cases are considered in the analysis in which DP is present at the drain side only as shown in figure 3.7 (d)-(f) i.e. *Case IV-VI*. In view of the above, the simulation of DP-DG MOSFET with six different cases has been carried out.

As the position of DP shifts inside the channel region, propagation delay of the device increases due to significant enhancement in gate capacitance (C_{gg}). This is so because, as DP penetrates inside the channel, channel length decreases and the effective gate drain overlap region increases. This results in the enhancement in fringing capacitance of the device. The enhancement of gate capacitance (C_{gg}) in case III-VI also leads to enhancement in the dynamic power dissipation of the device which further increases the *PDP* of the device. It can also be observed that the noise margin discussed previously is almost constant with the variation in the position of Dielectric Pocket. The almost negligible change in the noise margin (*NM)* is associated with the marginal change in the subthreshold slope (*S)* of the device.

3.4 ANALYTICAL MODELLING:

Quantum Mechanical confinement of inversion-layer carriers are well-known to affect the threshold voltage and gate capacitance of highly scaled bulk and DG MOSFETs significantly. The rapid downscaling of MOSFETs requires ultrathin oxides and high channel doping levels to minimize the drastic increase of short channel effect which in turn increases the electric field at the semiconductor-oxide interface and creates a sufficiently steep potential well for inducing the quantization of carrier energy. Now the carriers developed for the surface potential are then confined along the vertical direction of the quantum well. This carrier quantization effect appears in the submicron range due to two types of confinements namely structural confinement (appears for sub-micron dimensions) and electrical confinement (for applied transverse electric field). Thus to describe the analytical modelling of DP-DG structure, one first need to calculate the potential model and there by incorporating the effect of quantum well

along channel thickness, the quantum confinement of DP-DG can be demonstrated. To find the potential profile of such structure, both Poission and Schrodinger equations need to solve along the channel region. Using superposition technique the 2-D potential across the channel region is divided into 1-D Poission equation [$\Phi_{Lj}(y)$] with Laplace equation [$\Phi_{pj}(x, y)$], where the 2-D Poission equation for DP-DG can be represented as:

$$\frac{\partial^2 \phi_j(x,y)}{\partial x^2} + \frac{\partial^2 \phi_j(x,y)}{\partial y^2} = \frac{qN_j}{\varepsilon_j} \tag{3.12}$$

Where j = 1, 2, 3 for three different regions and N_j is the doping concentration in different regions. Now

$$\phi_j(x,y) = \phi_{Lj}(y) + \phi_{pj}(x,y) \tag{3.13}$$

Where the One-Dimensional solution for Poission's equation is given by

$$\phi_{Lj}(y) = \frac{qN_j}{2\varepsilon_j}\left(\sum_{i=1}^{j} t_i - y\right)^2 + A_{j1}\left(\sum_{i=1}^{j} t_i - y\right) + A_{j2} \quad \text{for} \quad \sum_{i=1}^{j-1} t_i \le y \le \sum_{i=1}^{j} t_i \tag{3.14}$$

Where the constants A_{j1} and A_{j2} can be obtained by considering the continuity of the electric flux and potential at the boundaries of different dielectric materials, so that $\Phi_{Lj}(y)$ satisfies the Poisson's equation for their respective regions.

In the vertical direction boundary conditions in the respective regions are given a

$$\phi_{Lj}(y) = \phi_{L(j+1)}(y) \qquad \text{at } y = \sum_{i=1}^{j-1} t_i \tag{3.15}$$

$$\varepsilon_j \frac{d\phi_{Lj}(y)}{dy} = \varepsilon_{j+1}\frac{d\phi_{L(j+1)}(y)}{dy} \qquad \text{at } y = \sum_{i=1}^{j-1} t_i \tag{3.16}$$

$$\phi_{L1}(0) = V_{gs} - V_{fb} \;(3.17)\; \phi_{L3}(t_1 + t_2 + t_3) = V_{gs} - V_{fb} \tag{3.18}$$

The 1-D potential in the channel region i.e. j=2 are given as:

$$\phi_{L2} = \frac{qN_2}{2\varepsilon_2}(t_1 + t_2 - y)^2 + A_{21}(t_1 + t_2 - y) + A_{22} \tag{3.19}$$

and from above boundary conditions by solving we get,

$$A_{21} = \frac{-qN_2t_2(\frac{t_1}{\varepsilon_1}+\frac{t_2}{2\varepsilon_2})}{t_2+\frac{\varepsilon_2}{\varepsilon_3}t_3+\frac{\varepsilon_2}{\varepsilon_1}t_1} \quad \text{and} \quad A_{22} = (Vgs - Vfb) + \frac{q\varepsilon_2 N_2 t_2 t_3(\frac{t_1}{\varepsilon_1}+\frac{t_2}{2\varepsilon_2})}{t_2+\frac{\varepsilon_2}{\varepsilon_3}t_3+\frac{\varepsilon_2}{\varepsilon_1}t_1}$$

On similar fashion, for the 2-D potential, the Laplace equation is given as:

$$\frac{\partial^2 \phi_{pj}(x,y)}{\partial x^2} + \frac{\partial^2 \phi_{pj}(x,y)}{\partial y^2} = 0 \tag{3.20}$$

Now the 2-D solution for the corresponding electro static potential $\phi_{pj}(x, y)$ along the channel region ($t_1 \le y \le t_1+t_2$) is

$$\phi_{p2}(x,y) = \left[\sum_{n=1}^{\infty} b_{2n} \frac{(\sinh(K_n(L-x)))}{\sinh(K_n(L))} + \sum_{n=1}^{\infty} c_{2n} \frac{\sinh(K_n(x))}{\sinh(K_n(L))}\right] \times \sin(K_n(t_1+t_2-y)+\beta_2) \tag{3.21}$$

Thus the solution for the 2-D Poission equation along the channel region has been performed with the scale length approach along with the superposition method. This procedure represents an excellent representation of the 2-D potential in the middle region (maximum of the potential barrier) of the channel without any fitting parameters. The corresponding chosen boundary conditions of this solution of 2-D potential equation:

$$\phi_{p1}(x,y) = 0 \text{ at } y = 0 \text{ (i.e., } \beta_1 = 0) \quad \text{and } \phi_{p3}(x,y) = 0 \text{ at } y = t_1 + t_2 + t_3$$

So that the nth half period of the sinusoidal wave would exists in between the solution. Now to satisfy the above mentioned criterion, $\beta_3 = n\pi$ is taken into account (n is an integer), along with $K_n = n\pi/\lambda$ where λ denotes the characteristic length achieved from the boundary conditions of the continuity potential.

In the present study the conventional boundary conditions for the DG architecture has been modified with the influence of the presence of DP at both the sidewall of the channel as shown in Figure 3.6, 3.7 by taking help of depletion approximation and continuity requirements of the lateral electric flux density along those incorporated dielectric pockets. Those conditions are:

$$\phi_{p2}(0,y) = V_{bi} \text{ for } t_1 \le y \le t_1 + y_1 \tag{3.22}$$

$$\phi_{p2}(L,y)=V_{bi}+V_{ds} \text{ for } t_1 \le y \le t_1+y_1 \tag{3.23}$$

$$\phi_{p2}(0,y)=\varphi_{ps}+[V_{bi}-\varphi_{ps}]\times\left[\frac{(y-(t_1+y_1))}{(t_2-y_1)}\right] \text{for } t_1+y_1 \le y \le t_1+t_2-y_3 \tag{3.24}$$

$$\phi_{p2}(L,y)=\varphi_{pd}+[V_{bi}+V_{ds}-\varphi_{pd}]\times\left[\frac{(y-(t_1+y_1))}{(t_2-y_1)}\right] \text{for } t_1+y_1 \le y \le t_1+t_2-y_3 \tag{3.25}$$

$$\phi_{p2}(0,y)=V_{bi} \text{ for } t_1+t2-y3 \le y \le t_1+t_2 \tag{3.26}$$

$$\phi_{p2}(L,y)=V_{bi}+V_{ds} \text{ for } t_1+t2-y3 \le y \le t_1+t_2 \tag{3.27}$$

Where the values of φ_{ps} and φ_{pd} can be calculated from the depletion approximation along with sidewall boundary electric flux density continuity requirements (i.e., at x=0 and x=L). Consequently the constants achieved in the equation (3.21) b_{2n} and c_{2n} along the channel can be evaluated from the set of equations (3.24)-(3.27) with the orthogonality of the fourier series as:

$$b_{2n}=\frac{D_1+D_2+D_3-D_4}{0.5[t_2+(\sin(2\beta_2)-\sin(2(K_n t_2+\beta_2)))/2K_n]} \tag{3.28}$$

where

$$D_1=(\frac{V_{bi}}{K_n})[\cos\{K_n(t_2-y_1)+\beta_2\}-\cos(K_n t_2+\beta_2)]$$

$$D_2=(\frac{\varphi_{ps}}{K_n})[\cos\{K_n(t_2-y_1-y_2)+\beta_2\}-\cos\{K_n(t_2-y_1)+\beta_2\}]$$

$$+(\frac{V_{bi}-\varphi_{ps}}{K_n})[\frac{1}{K_n(t_2-y_1)}]\ [\sin\{K_n(t_2-y_1-y_2)+\beta_2\}-\sin\{K_n(t_2-y_1)+\beta_2\}]+(\frac{V_{bi}-\varphi_{ps}}{K_n})[\frac{y_2}{(t_2-y_1)}]$$

$$\cos\{K_n(t_2-y_1-y_2)+\beta_2\}$$

$$D_3 = (\frac{V_{bi}}{K_n})[\cos(\beta_2) - \cos\{K_n(t_2 - y_1 - y_2) + \beta_2\}]$$

$$D_4 = [-\frac{qN_2\cos(\beta_2)}{\varepsilon_2 K_n^3} - \frac{qN_2 t_2^2 \cos(K_n t_2 + \beta_2)}{2\varepsilon_2 K_n} + \frac{qN_2 t_2 \cos(K_n t_2 + \beta_2)}{\varepsilon_2 K_n^2} + \frac{qN_2 \cos(K_n t_2 + \beta_2)}{\varepsilon_2 K_n^3}]$$

$$+A_{21}[\frac{\sin(K_n t_2 + \beta_2) - \sin(\beta_2)}{K_n^2} - \frac{t_2 \cos(K_n t_2 + \beta_2)}{K_n}] + A_{22}\frac{\cos(\beta_2) - \cos(K_n t_2 + \beta_2)}{K_n}$$

And $c_{2n} = \dfrac{D_1^{'} + D_2^{'} + D_3^{'} - D_4}{0.5[t_2 + (\sin(2\beta_2) - \sin(2(K_n t_2 + \beta_2)))/2K_n]}$

where

$$D_1 = (\frac{V_{bi} + V_{ds}}{K_n})[\cos\{K_n(t_2 - y_1) + \beta_2\} - \cos(K_n t_2 + \beta_2)]$$

$$D_2 = (\frac{\varphi_{ps}}{K_n})[\cos\{K_n(t_2 - y_1 - y_2) + \beta_2\} - \cos\{K_n(t_2 - y_1) + \beta_2\}]$$

$$+(\frac{V_{bi} + V_{ds} - \varphi_{ps}}{K_n})[\frac{1}{K_n(t_2 - y_1)}]\ [\sin\{K_n(t_2 - y_1 - y_2) + \beta_2\} - \sin\{K_n(t_2 - y_1) + \beta_2\}] + (\frac{V_{bi} + V_{ds} - \varphi_{ps}}{K_n})[\frac{y_2}{(t_2 - y_1)}]$$

$$\cos\{K_n(t_2 - y_1 - y_2) + \beta_2\}$$

$$D_3 = (\frac{V_{bi} + V_{ds}}{K_n})[\cos(\beta_2) - \cos\{K_n(t_2 - y_1 - y_2) + \beta_2\}]$$

Thus, the complete 2-D electrostatic potential equation along the channel region would be:

$$\phi_2(x, y) = \phi_{L2}(y) + \phi_{p2}(x, y) \qquad (3.29)$$

Thus from the coefficients calculated above, the complete nature of the potential profile across the channel region can be achieved.

3.4.1 Inversion Charge Modelling:

To achieve an estimation of inversion charge generated across the channel region, the Schrodinger equation must be solved across the developed rectangular potential well along the depth of channel region. As in rectangular potential well, the confinement of the quantization effect occurs only in one direction so 1-D Schrodinger equation is sufficient to demonstrate the whole picture inside the channel region of DP-DG MOSFET. Thus for a rectangular potential well having a small perturbation and with bottom at E_0, the corresponding 1-D Schrodinger equation is given by.

$$\frac{\partial^2\psi}{\partial y^2}+\frac{2m^*_{l,t}}{\hbar^2}(E-E_0)\psi=0 \tag{3.30}$$

To find the electron energy states in the rectangular potential well, standard separation of variable method have been adopted here to solve the equation (3.30). The expression for electron energy of states for 1-D Schrodinger equation in rectangular potential well is:

$$E^i_{l,t}=E_0+\frac{\hbar^2\pi^2 i^2}{2m^*_{l,t}t_{si}^2}\ \text{With}\quad E_0=\frac{E_g}{2}-\Phi(x,\frac{t_1}{2})$$

Where ψ is electron wave function, ħ is reduced Plank's constant (1.0546×10^{-27} cm^2 g s^{-1}), E is the energy of the electron wave function, m^*_l and m^*_t are the longitudinal and transverse electron effective masses and I represents a positive integer.

A first order perturbation for the external electric field $\Delta E=\langle\psi^*_i\,|\,H\,|\,\psi_i\rangle$ is also added to evaluate the energy levels. H in the above external electric field equation represents the Hamiltonian operator given as $H=-q[{}^{qN_2}\!/_{2\varepsilon_2}(t_1+t_2-y)^2+A_{21}(t_1+t_2-y)+A_{22}]$ where ψ^*_i is the complex

conjugate of ψ_i, the wave function associated with i[th] energy level. Thus the overall energy level is given as:

$$E^{\sim i}{}_{l,t} = E^{i}{}_{l,t} + \Delta E \tag{3.31}$$

As per crystallography, out of silicon's six energy valleys, four are transverse and rest of those two are longitudinally aligned. For each valley, charge per unit length is

$$Q = \sum_i q \int_{E^{\sim i}{}_{l,t}}^{\infty} N_{2D} f(E) d(E) \tag{3.32}$$

Where N_{2D} is the 2-D density of states of electrons and f(E) represents Fermi-Dirac (FD) distribution. The final expression for the inversion charges by including all the six valleys of Silicon described above and the FD energy level E_F is given by

$$Q_{inv,q} = \frac{qkT}{\pi\hbar^2} \sum_i [\sqrt{m^*{}_l m^*{}_t} g_t \ln[1 + \exp(-\frac{1}{V_t}(E^{\sim i}{}_l - \phi_{S1}(x) + E_F(x)))]$$

$$+ m^*{}_t g_t \ln[1 + \exp(-\frac{1}{V_t}(E^{\sim i}{}_l - \phi_{S1}(x) + E_F(x)))] \text{ for} 0<x<L \tag{3.33}$$

3.4.2 Threshold Voltage Modelling:

In this study, the Threshold voltage model including quantum effects of DP-DG MOSFET can be calculated by equating the integrated charge at the virtual cathode position to a critical charge (as calculated in equation 3.33). Now in general the threshold voltage is nothing but the gate voltage (V_{gs}) at which the minimum surface potential (i.e., $\phi_2(x_{min}, y)$) is same as the twice of Fermi level potential (φ_F). Thus by differentiating the channel potential of equation (6.10) at the minimum surface potential,

$$\frac{\partial \phi_2(x,y)}{\partial y} \Big|_{x=x_{min}}^{y=t_1+t_2} = 0 \tag{3.34}$$

And,

$$0=[\sum_{n=1}^{\infty}b_{2n}\frac{K_n\cosh(K_n(L-x_{\min}))}{\sinh(K_n(L))}-\sum_{n=1}^{\infty}c_{2n}\frac{\cosh(K_n(L-x_{\min}))}{\sinh(K_n(L))}] \quad (3.35)$$

Now from the above two equations the expression for minimum surface potential (x_{min}) can be achieved as:

$$x_{\min}=\frac{1}{2K_n}[\frac{b_{2n}\exp(K_nL)-c_{2n}}{c_{2n}-b_{2n}\exp(-K_nL)}] \quad (3.36)$$

Now by substituting the expression of x_{min} in equation (3.22), the value of minimum surface potential can be achieved. Now to obtain the threshold voltage, the minimum surface potential must be of same value with $2\varphi_f$. Thus the expression for Threshold voltage can be given by:

$$V_{th}=2\varphi_f-[b_{2n}\frac{\sinh(K_n(L-x_{\min}))}{\sinh(K_n(L))}-c_{2n}\frac{\sinh(K_n(L-x_{\min}))}{\sinh(K_n(L))}]$$

$$\sin(K_n(t_2)+\beta_2)+\frac{qN_2}{2\varepsilon_2}t_2^2-A_{21}t_2+V_{fb}-[\frac{\frac{\varepsilon_2 qN_2t_2t_3}{\varepsilon_3}(\frac{t_1}{\varepsilon_1}+\frac{t_2}{2\varepsilon_2})}{t_2+\frac{\varepsilon_2}{\varepsilon_3}t_3+\frac{\varepsilon_2}{\varepsilon_1}t_1}] \quad (3.37)$$

Where, b_{2n} and c_{2n} are the constant terms, V_{fb} is the flat band voltage.

Now as equating the inversion charge at virtual cathode position with normal inversion charge cannot be solved directly, so an unconventional procedure has been adopted by solving the equation in two sectors. In the first portion, *classical threshold voltage model,* the threshold voltage incorporating SCEs has been calculated where as in second section the deviation of classical and quantum threshold voltage has been derived. Thus the generalized expression for quantum threshold voltage is:

$$V_{th}^{q}=V_{th}^{cl}+\Delta V_{th}^{q} \quad (3.38)$$

3.4.2.1 Classical Threshold Voltage Modelling:

As discussed in Munteanu *et al.,*[65], the usual definition of V_{th} as the gate voltage where $\phi_2(x, y)=2\varphi_f$ does no more apply DP-DG MOSFET, where two channel coexist. Now in the nano scale regime, due to SCEs there exist some variations in the threshold voltage which would introduce a new factor in the model in order to account the DIBL effect. The Sub-threshold voltage slope can express as $SS = \frac{\partial V_{GS}}{\partial \phi_2(x_{\min}, y)}$ and it gives as [66]

$$SS = 0.1[\frac{2[\cos(K_n t_2 + \beta_2)]\sin(\beta_2)}{2K_n t_2 + \sin(2\beta_2) - \sin(2(K_n t_2 + \beta_2))}[\frac{\sin(K_n(L - x_{\min})}{\sin(K_n L)} + \frac{\sin(K_n(x_{\min})}{\sin(K_n L)}] + 1]^{-1}$$

(3.39)

This factor plays a dominant role to calculate the Classical threshold voltage. Normally Classical threshold voltage is used for encountering the change in threshold voltage (V_{th}) due to DIBL and calculated by translating the effective change in V_{gs} through the Sub-threshold slope factor as:

$$V_{th}^{cl} = V_{th}(1 - SS) \tag{3.40}$$

3.4.2.2Quantum Threshold Voltage Modelling:

As the quantum effect on threshold voltage can be measured by equating the integrated charge at the virtual cathode end with a critical charge (Q_T), so in quantum threshold voltage modelling the expression for the critical charge has to be calculated initially. The calculation of Q_T has been made by considering the classical and quantum inversion charge models at the virtual cathode position separately and thereby the difference between the surface potential for the classical and quantum states can be evaluated.

For classical model, at threshold voltage,

$$Q_T = Q_{T_{inv,cl}} = \int_{t_1}^{t_1+t_2} qn_i \exp(\frac{\phi_2(x_{\min}, y)}{V_t})dy$$

$$= qn_i \exp(\frac{\phi_{p2}(x_{\min})}{V_t}) \int_{t_1}^{t_1+t_2} \exp(\frac{\frac{qN_a}{2\varepsilon_2}(t_1+t_2-y)^2 + A_{21}(t_1+t_2-y) + A_{22}}{V_t})dy$$

(3.41)

Where at threshold voltage,

$$\phi_{p2}(x_{\min}) = \phi_{p2}(x_{\min}, t_1+t_2)$$

As the numerical value of A21 is negative, so it can be written as $A_{21} = -|A_{21}|$

Then by solving above equation the final equation become

$$Q_T = Q_{T_{inv,cl}} = \frac{\sqrt{\pi} qn_i}{2P_1} \exp(\frac{\phi_{p2}(x_{\min})}{V_t}) \exp(\frac{A_{22}}{V_t} - \frac{|P_2|^2}{4P_1}) \times [erfi(P_1 t_2 + \frac{|P_2|}{2P_1}) - erfi(-\frac{|P_2|}{2P_1})]$$

(3.42)

Where $P_1 = \sqrt{\frac{qN_a}{2\varepsilon_2 V_t}}$ and $P_2 = \frac{A_{21}}{V_t} = -\frac{|A_{21}|}{V_t}$

On the other side, for weak inversion region Fermi level lies much below the conduction band and that is why Fermi-Dirac distribution by Boltzmann statistics. Thus by using quantum mechanical approach the critical charge can be calculated as

$$Q_T = Q_{T_{inv,q}} = \frac{qkT}{\pi\hbar^2} \exp(\frac{\phi_{p2}(x_{\min})}{V_t}) \times \sum_i [\sqrt{m_l^* m_t^*} g_t \exp(-\frac{E_l^{\sim i}}{V_t}) + m_t^* g_l \exp(-\frac{E_t^{\sim i}}{V_t})]$$

(3.43)

Now, by equating (3.42) and (3.43) it can be written

$$\frac{qkT}{\pi\hbar^2} \exp(\frac{\phi_{p2}^{cl}(x_{\min})}{V_t}) \sum_i (\sqrt{m_l^* m_t^*} g_t \exp(-\frac{E_l^{\sim i}}{V_t}) + m_t^* g_l \exp(-\frac{E_t^{\sim i}}{V_t}))$$

$$= \frac{\sqrt{\pi} qn_i}{2P_1} \exp(\frac{\phi_{p2}^{q}(x_{\min})}{V_t}) \exp\left(\frac{A_{22}}{V_t} - \frac{P_2^2}{4P_1}\right) [erfi(P_1 t_2 + \frac{|P_2|}{2P_1}) - erfi(-\frac{|P_2|}{2P_1})]$$

or,

$$\frac{\phi_{p2}^{cl}(x_{\min})-\phi_{p2}^{q}(x_{\min})}{V_t}=\ln\left(\frac{\sqrt{\pi}qn_i}{2P_1}\right)+\left(\frac{A_{22}}{V_t}-\frac{P_2^2}{4P_1}\right)+\ln\{erfi(P_1t_2+\frac{|P_2|}{2P_1})-erfi(-\frac{|P_2|}{2P_1})\}$$

$$-\ln(\sum_i(\sqrt{m_l^*m_t^*}\,g_t\exp(-\frac{E_l^{\sim i}}{V_t})+m_t^*g_l\exp(-\frac{E_t^{\sim i}}{V_t})))$$

$$\therefore\Delta\phi_{p2}^{q}(x_{\min})=V_t[\ln(\frac{\pi^{\frac{3}{2}}n_i\hbar^2}{2P_1kT})+(\frac{A_{22}}{V_t}-\frac{P_2^{\,2}}{4P_1})+\ln\{erfi(P_1t_2+\frac{|P_2|}{2P_1})-erfi(-\frac{|P_2|}{2P_1})\}$$

$$-\ln(\sum_i(\sqrt{m_l^*m_t^*}\,g_t\exp(-\frac{E_l^{\sim i}}{V_t})+m_t^*g_l\exp(-\frac{E_t^{\sim i}}{V_t})))] \qquad (3.44)$$

Now, the change in threshold voltage ΔV_{th}^{q} can be calculated from $\Delta\phi_{p2}^{q}(x_{\min})$ as follows:

$$\Delta V_{th}^{q}=\frac{1}{V_t\ln 10}*0.1[\frac{2[\cos(K_nt_2+\beta_2)]\sin(\beta_2)}{2K_nt_2+\sin(2\beta_2)-\sin(2(K_nt_2+\beta_2))}[\frac{\sin(K_n(L-x_{\min})}{\sin(K_nL)}+\frac{\sin(K_n(x_{\min})}{\sin(K_nL)}]+1]^{-1}$$

$$*V_t[\ln(\frac{\pi^{\frac{3}{2}}n_i\hbar^2}{2P_1kT})+(\frac{A_{22}}{V_t}-\frac{P_2^{\,2}}{4P_1})+\ln\{erfi(P_1t_2+\frac{|P_2|}{2P_1})-erfi(-\frac{|P_2|}{2P_1})\}$$

$$-\ln(\sum_i(\sqrt{m_l^*m_t^*}\,g_t\exp(-\frac{E_l^{\sim i}}{V_t})+m_t^*g_l\exp(-\frac{E_t^{\sim i}}{V_t})))] \qquad (3.45)$$

Where SS is Sub-threshold Voltage and I_{ds} is drain current in sub-threshold region

Now, substituting the value of (3.45) and (3.40) in (3.38) quantum threshold voltage V_{th}^{q} is obtained as:

$$V_{th}{}^{q}=V_{th}(1-0.1[\frac{2[\cos(K_nt_2+\beta_2)]\sin(\beta_2)}{2K_nt_2+\sin(2\beta_2)-\sin(2(K_nt_2+\beta_2))}[\frac{\sin(K_n(L-x_{\min})}{\sin(K_nL)}+\frac{\sin(K_n(x_{\min})}{\sin(K_nL)}]+1]^{-1})$$

$$+\frac{1}{V_t\ln 10}*0.1[\frac{2[\cos(K_nt_2+\beta_2)]\sin(\beta_2)}{2K_nt_2+\sin(2\beta_2)-\sin(2(K_nt_2+\beta_2))}[\frac{\sin(K_n(L-x_{\min})}{\sin(K_nL)}+\frac{\sin(K_n(x_{\min})}{\sin(K_nL)}]+1]^{-1}$$

$$*V_t[\ln(\frac{\pi^{\frac{3}{2}} n_i \hbar^2}{2P_1 kT}) + (\frac{A_{22}}{V_t} - \frac{P_2{}^2}{4P_1}) + \ln\{erfi(P_1 t_2 + \frac{|P_2|}{2P_1}) - erfi(-\frac{|P_2|}{2P_1})\}$$

$$-\ln(\sum_i (\sqrt{m_l^* m_t^*} g_t \exp(-\frac{E_l^{\sim i}}{V_t}) + m_t^* g_l \exp(-\frac{E_t^{\sim i}}{V_t})))] \quad (3.46)$$

CHAPTER 4: RESULTS AND DISCUSSIONS

4.1. SURFACE PLOT

4.1.1. SURFACE PLOT ALONG CHANNEL LENGTH

4.1.2. SURFACE PLOT ALONG CHANNEL THICKNESS

4.2. ELECTRIC FIELD

4.3. DEVIATION OF QUANTUM THRESHOLD VOLTAGE FROM CLASSICAL COUNTERPART

4.4. QUANTUM THRESHOLD VOLTAGE

4.5. SUB-THRESHOLD SLOPE

4.6. COMPARISON OF DP-DG MOSFET WITH OTHER MOSFETS

4. RESULTS & DISCUSSIONS:

A detailed analytical model has been developed for DP-DG MOSFET that includes quantum confinement effects. However, some other effects like scattering effect; mobility degradation etc. has been neglected while developing this model to keep the model simple. Also it is justified to neglect the above mentioned effects here only weak inversion or sub-threshold region are considered where these effects are negligible. Here, Analytical results are compared with the results of DPDG MOSFET ATLAS 2D simulator data for the validation of the structure. The corresponding values of various parameters of the proposed structure which are extensively used for this study are given in Table 1.

Table 1: Typical Values of the Parameters Used for DP-DG MOSFET

PARAMETERS	VALUES
Channel length (L)	20 nm
Work function Φm	4.63 eV
Front Gate Oxide tf	2 nm
Back Gate Oxide tb	2 nm
Film Width tsi	5nm
Body Doping Na	1*1e+20m-3
Source/Drain Doping ND	1*1e+26m-3
Shallow Extension Depth (y1, y3)	5 nm
Dielectric Pocket Thickness (Tst)	5 nm
Dielectric Pocket height (y2)	10 nm

4.1. Surface Plot:

4.1.1. Surface Plot along Channel Length:

Fig.4.1 shows the variation of surface potential along the channel length for different gate voltages. From figure it has been observed that the DPDG MOSFET structure makes the nature of the potential profile is found almost symmetric and the potential minimum is found almost at the middle of the channel. From the figure it can be clearly observed that the proposed structure is much immune to DIBL effect as the drain voltage variations do not show a considerable impact at source side. The figure also

shows that the impact of Vds on the minimum surface potential is negligible due to the presence of side pillars. As a result, lower threshold voltage roll off with variation in Vds is observed in the proposed DP-DG MOSFET structure compared to other devices [35].

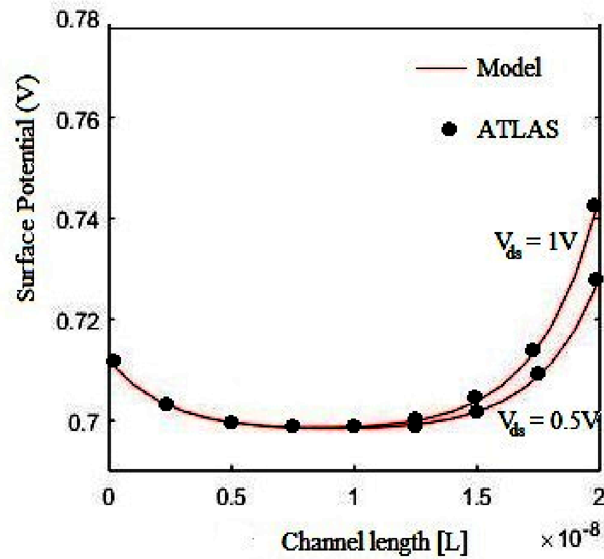


Fig. 4.1 Variation of surface potential along channel length with respect to Vgs fixed at 0.3V and Vds used as variable parameter

4.1.2. Surface Plot along Channel Thickness:

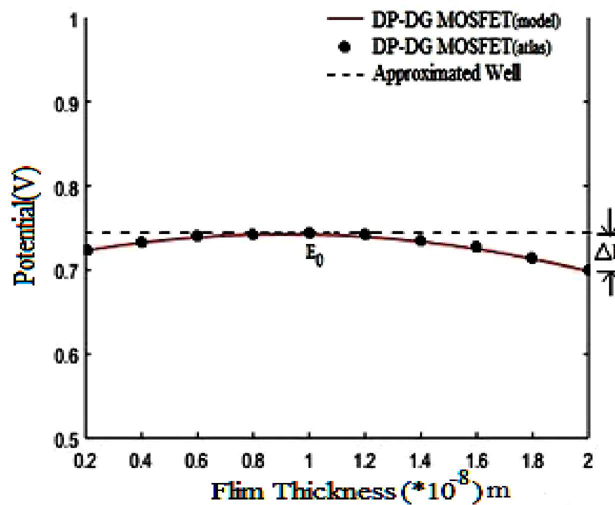


Fig.4.2 Rectangular well formed along film thickness with perturbation ΔE with fixed gate and drain voltage at 0.3V and 1V respectively

Under symmetrical gate and weak charge inversion rectangular well is formed along channel thickness [68] and this is clear from fig.4.2. There is some perturbation of ΔE due to incorporation of dielectric pocket in channel length.

4.2. Electric Field:

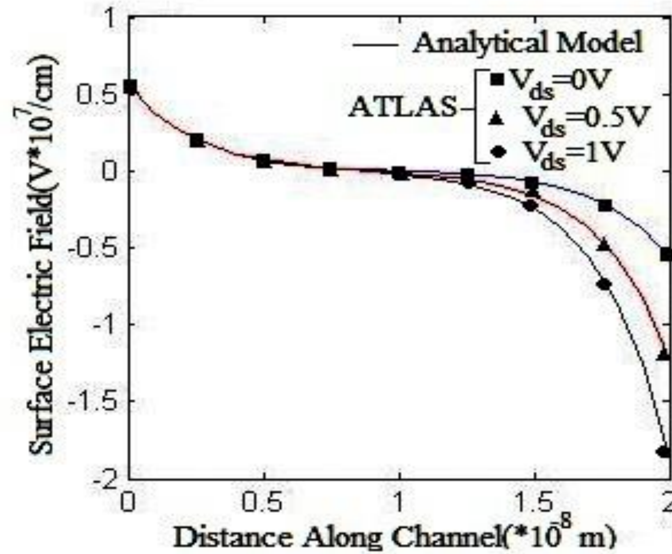


Fig.4.3 Variation of surface potential & surface electric field along channel length with respect to V_{gs} fixed at 0.3V and V_{ds} used as variable parameter

The surface electric field increases at the drain side with increase in drain bias (V_{ds}) as shown in figure 4.3 is mainly responsible for the Hot Carrier Effects (HCEs).

4.3. Deviation of Quantum Threshold Voltage from classical counterpart:

Quantum threshold voltage is found by adding the shift in threshold voltage due to quantization with the classical threshold voltage. Fig.4.4 shows the variation of ΔV_{th}^{q} with respect to channel length for different values of channel doping at a fixed film thickness and the structure has small roll off and it becomes quantum threshold voltage is always greater than classical one almost constant as length increases. Here, V_{ds} and V_{gs} are taken as 0.5V and 0.3V respectively for Na = $1x10^{21}$ m^{-3} and $1x10^{20}$ m^{-3}. As the degrees of freedom are restricted in quantum case, carriers are confined in some particular sub-bands especially in first sub-band [73].It has been observed that dependence of ΔV_{th}^{q} on doping density is much more than that of channel length .

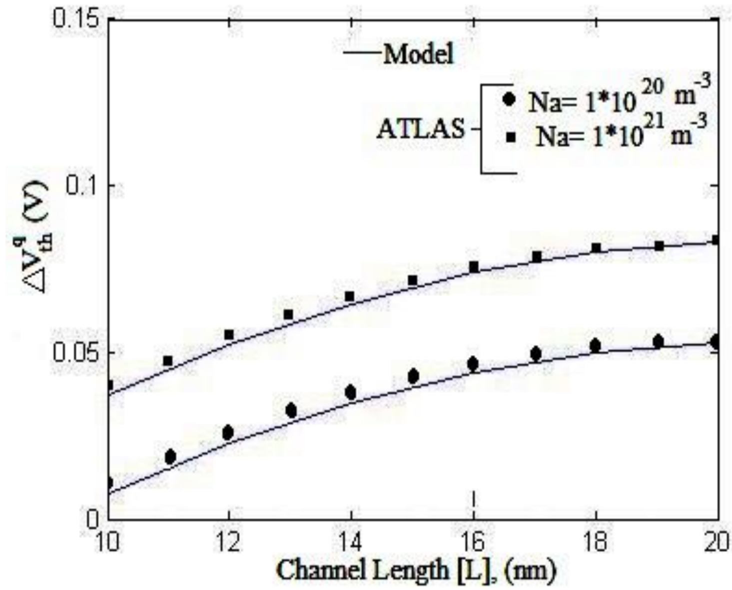


Fig. 4.4 Variation of ΔV_{th}^{q} along channel length with fixed V_{gs} and V_{ds} at 0.3V and 0.5V with Na as variable parameter

ΔV_{th}^{q} >0 signifies that the quantum threshold voltage is always greater than classical one. This is because within a specific range of energy, the energy levels are separated by a larger amount resulting in an overall decrease in total charge. This in turn necessitates the application of an increased voltage level to achieve same amount of inversion charge at the virtual cathode position [51]. As length decreases, ΔV_{th}^{q} decreases. As channel doping increases, a higher voltage is required to form the inversion channel between the source and the drain that's why ΔV_{th}^{q} increases with increase in doping concentration of channel.

4.4. Quantum Threshold Voltage:

Fig.4.5 shows the quantum threshold voltage along channel length for different doping concentration. Quantum threshold voltage is found by adding the shift in threshold voltage due to quantization with the classical threshold voltage. Here, V_{ds} and V_{gs} are taken as 0.5V and 0.3V respectively for Na = $1x10^{20}$ m^{-3} and $1x10^{21}$ m^{-3}.

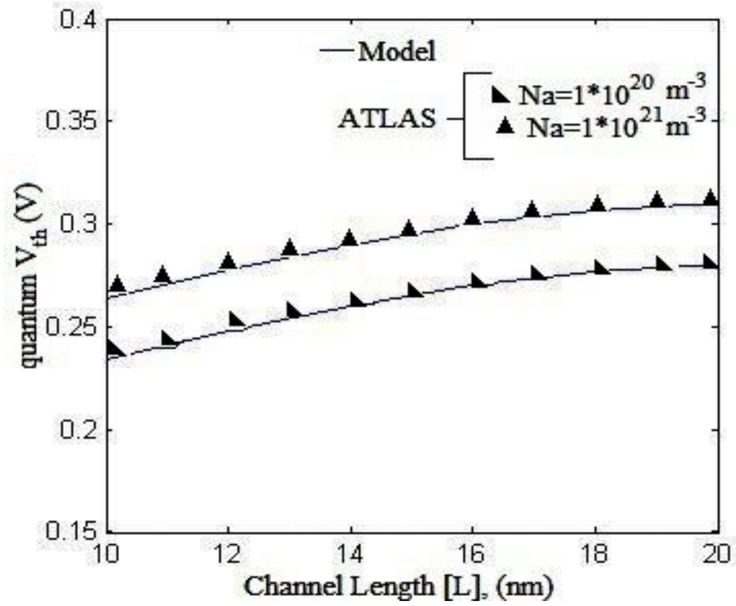


Fig. 4.5: Quantum V_{th} along channel length with fixed V_{gs} and V_{ds} at 0.3V and 0.5V with Na as variable parameter

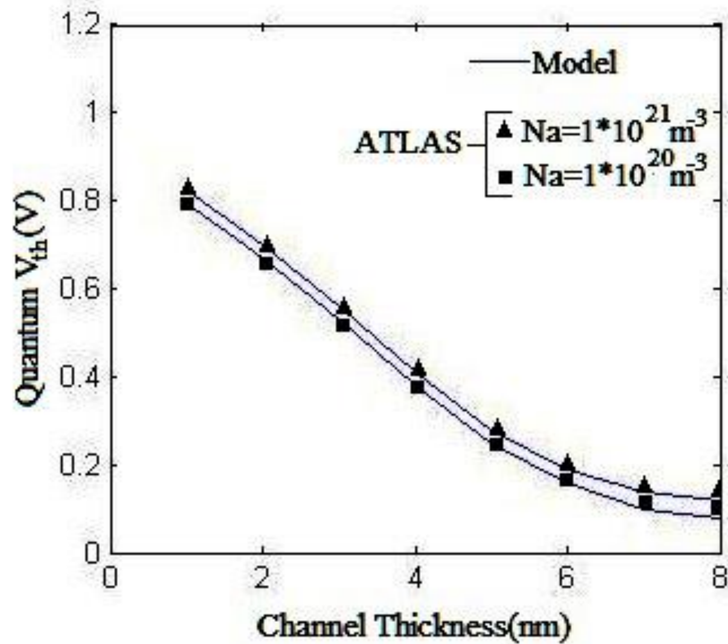


Fig. 4.6: Variation of Quantum V_{th} with respect to y_1 and y_3 (whereas y_2 length remain same) with Na as variable parameter and V_{gs} and V_{ds} fixed at 0.3V and 0.5V respectively

As the degrees of freedom are restricted in quantum case, carriers are confined in some particular sub-bands especially in first sub-band [73]. As length increases ΔV_{th}^{q} increases and as channel doping increases ΔV_{th}^{q} also increases, shown in fig 4.4, which, in turn, causes the quantum V_{th} to increase as evident in fig.4.5. Fig.4.6. shows quantum V_{th} variation with channel thickness with respect to shallow extension depth (y_1 and y_3) at fixed y_2 (since, $t_{si}=y_1+y_2+y_3$). It can be observed from the figure that a decrease in the channel thickness increases the quantum V_{th}. This can be explained by the fact that with the increase in channel thickness, the width of potential well increases which in turn decreases the separation of energy levels within the potential well. On the contrary, a reduction in channel thickness increases the separation of energy levels which effectively introduces the quantization behaviour. Reduction in channel length and channel thickness introduces energy quantization which results in reduction of SCEs due to the increase in effective band gap of silicon channel as a result of quantum effect [74].

4.5. Sub-Threshold Slope:

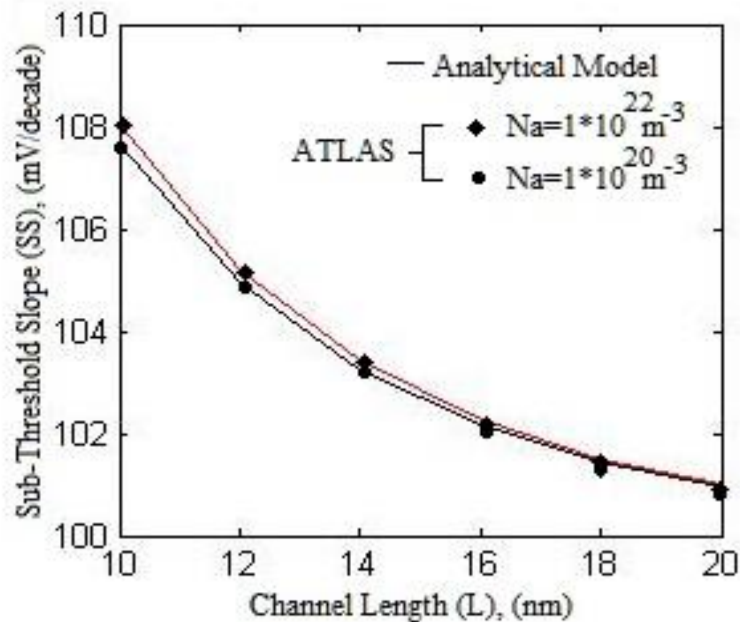


Fig.4.7. Variation of Sub-Threshold Slope along channel length with fixed V_{gs} and V_{ds} at 0.3V and 0.5V respectively& channel doping used as variable

In fig.4.7 variation of sub-threshold with respect to channel length is shown for different channel doping concentration and it is very clearly from picture that value of

sub-threshold increases when channel doping concentration increases and channel length decreases as threshold voltage increases for those two reasons also which is shown in fig.4.5.

4.6. Comparison of DP-DG MOSFET with other MOSFETs:

The variation of quantum threshold voltage of DP-DG MOSFET and DG MOSFET along channel length is shown inFig.4.8. It is observed that the quantum threshold voltage of DP-DG MOSFET is less than DG MOSFET SCEs resulting from the incorporation of Dielectric Pocket in DP-DG MOSFET is reduced.

Similarly, the variation of quantum threshold voltage of DP-DG MOSFET and DMDG SOI along channel length for different channel doping is shown in fig.4.9. DP-DG MOSFET has low threshold voltage than DMDG SOI. This can be attributed to the fact that the potential coupling ratio ($P_{CR} = \phi_f / \phi_b$) of DP-DG MOSFET is reduced due to the absence of back gate oxide layer. Moreover, incorporation of Dielectric Pocket in the proposed device structure reduces the threshold voltage.

The lower threshold voltage of DP-DG MOSFET signifies that this device is more immune to SCEs than above mentioned devices which, in turn, increase the current

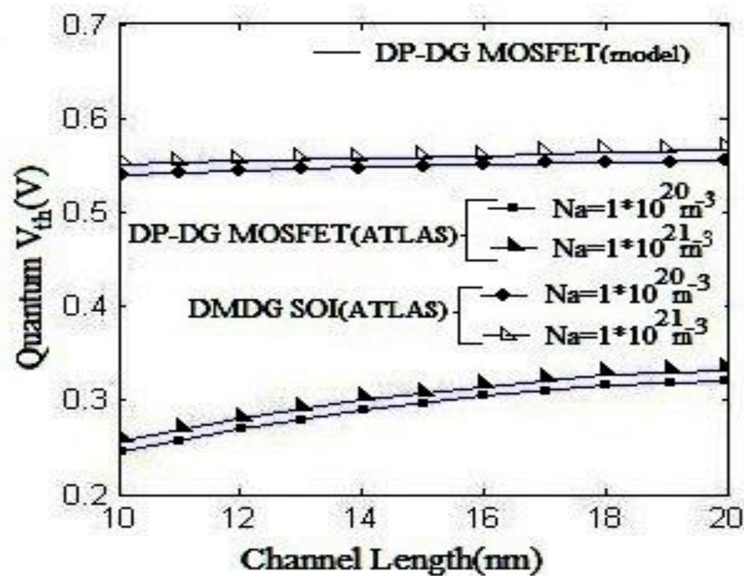


Fig.4.8. Comparison between quantum V_{th} of DG MOSFET and DP-DG MOSFET along channel length where for both V_{gs} and V_{dsat} 0.5V and 0.5V respectively

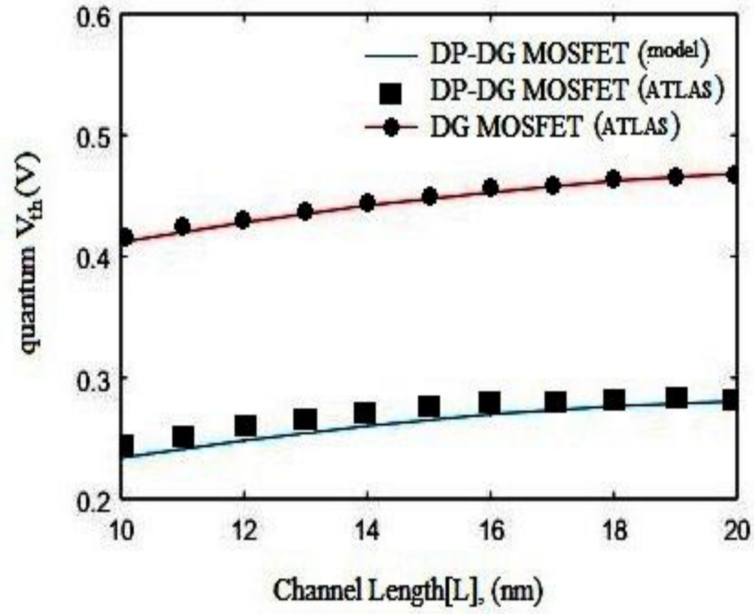


Fig.4.9. Comparison between quantum V_{th} of DMDG SOI and DP-DG MOSFET along channel length for different channel doping where for both V_{gs} and V_{dsat} 0.6V and 0.5V respectively

handling capability and switching speed making the proposed device a suitable alternative in modern VLSI era to increase packing density of chips.

CONCLUSION & FUTURE SCOPES OF THE PRESENT WORK

5.1 CONCLUSIONS

5.1.1 IMPACTS OF DIELECTRIC POCKETS IN DOUBLE GATE MOSFET

5.2 FUTURE SCOPES OF THE PRESENT WORK

5.1 CONCLUSIONS:

Ongoing trend of research in nano-scale devices will lead to the development of device structures having dimension of less than 10nm in order to satisfy the ever increasing demands of low power consuming high speed devices required for high density IC packaging. Rapid downscaling of MOSFET structure results in strong short channel effects and consequently a higher leakage current which limits further device miniaturization. Effective mitigation of short channel effects is the major challenge for future MOSFETs. The desired solution can be achieved by advancement in material engineering and/or development of new device geometry to cope up with short channel effect. Double-Gate (DG) MOSFETs in the last decade has become the subject of intensive research and an impressing number of studies have substantiated its enormous potentiality to force back the integration limits to which single gate MOSFETs are subjected to. Although the operation of DG transistor is almost similar to the conventional MOSFET, the physics of DG MOSFET is much more complicated. Physical phenomena such as 2D electrostatics or carrier quantization need to be considered, since DG structures are precisely used to design very integrated devices (with short channel and extremely thin films). Therefore, new compact models, consecrated for the circuit simulation, have to be developed for DG MOSFET [76]. Several interesting models have been proposed for the classical (i.e. without quantum effects) drain current in long channels DG [75-79] or for short channel DG operating in the sub-threshold regime [80]

The work presented in this dissertation is mainly focused on Quantum Mechanical Effects of Dielectric Pocket MOSFET from lateral channel engineering, MOSFET from substrate engineering and Double Gate MOSFET from gate electrode engineering techniques that can overcome the demerits associated with bulk MOSFET and improve device performance. In addition, CMOS circuit design demands the accurate modelling of non-classical devices for describing the behaviour of various electrical parameters prior to the device fabrication. This requires exact solution of the basic semiconductor equation i.e. Schrodinger equation, Poisson’s equation, continuity

equation, and other related equations. The solution of these equations invariably involves numerical analysis. The situation becomes even more complex for nano-scale devices where 2- dimensional or 3- dimensional effects are to be accounted in modelling. Thus, a two dimensional quantum mechanical model which can give approximately same results as obtained from the device simulation within acceptable tolerance would be very useful. Furthermore, in nano-scale regime, the process variation has also major impact on the device behaviour.

The impact of insulating layers (or dielectric pockets) on the performance of double gate MOSFET has been discussed by considering presence of dielectric pocket at the side wall of the source/drain regions i.e. Dielectric Pocket Double Gate MOSFET. The literature explores the impact of Dielectric Pocket on the performance of Double Gate i.e. DP-DG MOSFET through an efficient 2-D analytical model solved using superposition technique and consequentially comparing the results with the conventional double gate and DMDG SOI MOSFETs. The proposed model includes evaluation of surface potential, electric field, classical threshold voltage (V_{th}), sub-threshold slope (S), quantum threshold voltage (V_{th}^{q}) that greatly simplifies the device characteristics assessment.

From surface potential model (fig 4.1), it can be concluded that surface channel potential is symmetric and minima shifts negligibly with increasing drain biases. This results in excellent immunity against drain-induced barrier lowering (DIBL) and channel length modulation (CLM). From electric field model (fig 4.3), it can be concluded that this device gives better prevention to hot carrier effect (HCE). Due to quantization effect a deviation is observed between classical and quantum threshold voltage (fig 4.4). Deviation is positive i.e. quantum threshold voltage is more than classical threshold voltage. As the film thickness is reduced, quantum threshold voltage is increased due increase in effective band gap of Silicon and that can be concluded from fig(4.6). This device offers relatively lower threshold voltage when compared to other devices like DMDG SOI MOSFET, DG MOSFET etc. ensuring higher current drive, lower SCE and increased transconductance than the later mentioned devices. The results of our proposed DP-DG MOSFET structure with quantum effects are quite close to the available SILVACO ATLAS simulated data which strongly supports the accuracy of our model.

5.2 FUTURE SCOPES OF THE PRESENT WORK

The present model is reasonable as well as realistic enough which is predicted from analytical modelling of its the surface potential, threshold voltage and inversion charge. However, there are still some issues that can be addressed to make the model even more realistic. In present model these effects have been avoided to keep the model simple.

1. The model has been solved using 2D Poisson equation. A 3D Poisson equation can be solved to verify the overall potential profile even more accurately.
2. Similarly a 3D Schrodinger equation instead of 1D equation will predict the charge profile more precisely.
3. A binary metal gate alloy or Work Function Engineering Gate (WFEG) can be incorporated in the DP-DG architecture which can adjust the overall field through the adjustment of vertical field and can diminish the asymmetry in surface potential profile in a short channel device thereby controlling the DIBL notably.

REFERENCES

1. Sergey Edward Lyshevski (Editor), Nano and Molecular Electronics: Hand Book, CRC Press, Taylor & Francis, NW, 2007.
2. http://csanad.hubpages.com/hub/Semiconductor-Industry
3. G. Moore: Cramming more components onto integrated circuits. Electronics, 38, 114 (1965)
4. The International Technology Roadmap for Semiconductor 2009, 2010, 2011, 2012, 2013.
5. R.H. Dennard, F.H. Gaensslen, H.-N. Yu, V.L. Rideout, E. Bassours, A.R. LeBlanc, J. Solid-State Circuits SC-9 (1974) 256.
6. R.H. Dennard, F.H. Gaensslen, H.-N. Yu, V.L. Rideout, E. Bassours, A.R. LeBlanc, J. Solid-State Circuits SC-9 (1974) 256
7. J. E. Lilienfeld, "Method and apparatus for controlling electric currents," U.S. Patent 1 745 175, 1930
8. D. Kahng and M. M. Atalla, "Silicon–silicon dioxide field induced surface devices," presented at the IRE Solid-State Device Res. Conf., Pittsburgh, PA, June 1960.
9. Colinge JP. Silicon on insulator technology: materials to VLSI. 2nd ed. Norwell, MA: Kluwer: Kluwer Academic Publishers; 1997.
10. H.K. Lim and J.G. Fossum, "A charge based large signal model for thin film SOI MOSFETs", IEEE Transaction on Electron Devices, Vol. 32, pp. 446-457, 1985.
11. F. Balestra, J. Brini and P. Gentil, "Deep depleted SOI MOSFETs with back potential control: A numerical simulation", Solid State Electron., Vol. 28, pp.1031-1037, 1985.
12. J. R. Davis, A.E. Glaccum, K. Reeson and P.L.F. Hemment, "Improved subthreshold characteristics of n-channel SOI transistors", IEEE Electron Devices Lett., Vol. 7, pp.570, 1986.

13. K. K. Young, “Short-channel effects in fully depleted SOI MOSFET's,” IEEE Trans. Electron Devices, Vol. 36, pp. 399-402, 1989.
14. Jason C. S. Woo, Kyle W. Terrill And Prahalad K. Vasudev, “Two-Dimensional Analytic Modeling of Very Thin SOI MOSFET’s”, IEEE Transactions On Electron Devices, Vol. 37. No. 9, 1999 (1990).
15. K. Tokunaga and J.C. Strum, “Substrate bias dependence of subthreshold slopes in fully depleted silicon-on-insulator MOSFETs”, IEEE Transaction on Electron Devices, Vol. 38, pp. 1803-1807, 1991.
16. Long Wei, K. K. Chin, “Dual material gate field effect transistor (DMGFET)”, International Electron Devices Meeting, IEDM '97, Technical Digest, 1997, Page(s): 549 – 552.
17. Jeffrey W. Sleight and Rafael Rios, “A Continuous Compact MOSFET Model for Fully and Partially-Depleted SOI Devices”, IEEE Transactions On Electron Devices, Vol. 45, No. 4, 821 (1998).
18. Cheng Baohong, V. R. Rao, J. C. S. Woo, “Sub-0.18 μm SOI MOSFETs using lateral asymmetric channel profile and Ge pre-amorphizationsalicide technology”, IEEE International SOI Conference, 1998.
19. Cheng Baohong, V. R. Rao, J. C. S. Woo, “Exploration of velocity overshoot in a high performance deep sub-0.1-μm SOI MOSFET with asymmetric channel profile”, IEEE Electron Device Letters, Volume: 20 , Issue: 10.
20. W. Long, H. Ou, J.-M. Kuo, and K. K. Chin, “Dual material gate (DMG) field effect transistor,” IEEE Trans. Electron Devices, vol. 46, pp. 865-870, 1999.
21. F. Gámiz, J. A. López-Villanueva, J. Roldán, J. E. Carceller, and P. Cartujo, “Monte Carlo simulation of electron transport properties in extremely thin SOI MOSFET’s,” IEEE Trans. Electron Devices, vol. 45, pp. 1122–1126, May 1998.
22. F. Gámiz, J. B. Roldán, P. Cartujo-Cassinello, J. E. Carcellar, J. A. López-Villanueva, and S. Rodriguez, “Electron mobility in extremely thin single-gate silicon-on-insulator inversion layers,” J. Appl. Phys., vol. 86, no. 11, pp. 6269–6275, 1999.
23. J. B. Roldán, F. Gámiz J. A. López-Villanueva and P. Cartujo-Cassinello, “Deep Submicrometer SOI MOSFET Drain Current Model Including Series

Resistance, Self-Heating and Velocity Overshoot Effects”, IEEE Electron Device Letters, Vol.21, No. 5, 239 (2000).

24. X. Zhou, “Exploring the novel characteristics of Hetero-Material Gate Field-Effect transistors (HMGFET’s) with gate-material engineering”, IEEE Transaction on Electron Devices, Vol. 47, Page(s) 113-120, January 2000.
25. M. Youssef Hammad and Dieter K. Schroder, “Analytical Modeling of the Partially-Depleted SOI MOSFET”, IEEE Transactions On Electron Devices, Vol.48, No. 2, 252 (2001).
26. Keunwoo Kim, and Jerry G. Fossum, “Double-Gate CMOS: Symmetrical-Versus Asymmetrical-Gate Devices”, IEEE transaction on Electron Devices, Vol.48, No. 2, pp. 294-299, Feb 2001.
27. T. Ernst, C. Tinella , C. Raynaud , S. Cristoloveanu, “Fringing fields in sub-0.1 lm fully depleted SOI MOSFETs: optimization of the device architecture”, Solid-State Electronics 46, 373–378 (2002).
28. Kunihiro Suzuki and Sergey Pidin, “Short-Channel Single-Gate SOI MOSFET Model”, IEEE Transactions On Electron Devices, Vol. 50, No. 5, 1297, 2003.
29. J. Pretet, S. Monfray, S. Cristoloveanu, T. Skotnicki, “Silicon-on-Nothing MOSFETs: Performance, Short-Channel Effects, and Backgate Coupling”, IEEE Transactions on Electron Devices, 2004; 51(2), 240-246.
30. D. C. Donaghy, S. Hall, V. D. Kunz, C. H. D. Groot, and P. Ashburn, Investigating 50 nm channel length vertical MOSFETs containing a dielectric pocket in a circuit environment,” in *Proc. ESSDERC*, Florence, Italy, 2002, pp. 499–502.
31. S. K. Jayanarayanan, S. Dey, J. P. Donnelly, and S. K. Banerjee, “A novel 50 nm vertical MOSFET with dielectric pocket,” *Solid State Electron.*, vol. 50, no. 5, pp. 897–900, 2006.
32. E. Gili, T. Uchino, M. M. A. Hakim, C. H. De Groot, O. Buiu, S. Hall, and P. Ashburn, “Shallow junctions on pillar sidewalls for sub-100-nm vertical MOSFETs,” *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 692–695, Aug. 2006.
33. M. A. Riyadi, Z. A. F. M. Napiah, I. Saad, and R. Ismail, “Characterization analysis of a novel approach in fabrication of CMOS compatible vertical

MOSFETs incorporating a dielectric pocket,” in *Proc. ICSE*, 2008, pp. 639–642.
34. O. P. Kok and K. Ibrahim, “Simulation of two-dimensional 50 nm vertical metal oxide semiconductor field effect transistor incorporating a dielectric pocket,” *Jpn. J. Appl. Phys.*, vol. 48, no. 11, p. 111 201, Nov. 2009.
35. V. Kumari, M Saxena, R.S. Gupta, M. Gupta, “Two-Dimensional Analytical Drain Current Model for Double-Gate MOSFET Incorporating Dielectric Pocket”, *IEEE Trans. Electron Devices,* vol. 59, no. 10, pp. 2567-2574, Oct. 2012.
36. Giorgio Mugnaini and Giuseppe Iannaccone, “Physics-Based Compact Model of Nanoscale MOSFETs—Part I: Transition From Drift-Diffusion to Ballistic Transport”, IEEE Transactions On Electron Devices, Vol. 52, No. 8, 1795 (2005).
37. Adelmo Ortiz-Conde, Francisco J. García-Sánchez, and SlavicaMalobabic, “Analytic Solution of the Channel Potential in Undoped Symmetric Dual-Gate MOSFETs”, IEEE transaction on Electron Devices, Vol. 52, No. 7, pp. 1669-1672, July 2005.
38. Norio Sadachika, Daisuke Kitamaru, YasuhitoUetsuji, Dondee Navarro, MarmeeMohdYusoff, Tatsuya Ezaki, Hans Jürgen Mattausch and Mitiko Miura-Mattausch, “Completely Surface-Potential-Based Compact Model of the Fully Depleted SOI MOSFET Including Short-Channel Effects”, IEEE Transactions On Electron Devices, Vol. 53, No. 9, 2017 (2006).
39. W. Wu, X. Li , G. Gildenblat , G.O. Workman , S. Veeraraghavan , C.C. McAndrew , R. van Langevelde , G.D.J. Smit , A.J. Scholten , D.B.M. Klaassen, J. Watts, “PSP-SOI: An advanced surface potential based compact model of partially depleted SOI MOSFETs for circuit simulations”, Solid-State Electronics 53, 18–29 (2009).
40. Guohe Zhang, Zhibiao Shao and Kai Zhou, “Threshold Voltage Model of Short-Channel FD-SOI MOSFETs With Vertical Gaussian Profile”, IEEE Transactions On Electron Devices, Vol. 55, No. 3, 803 (2008).

41. Te-Kuang Chiang, “A new two-dimensional analytical subthreshold behavior model for short-channel tri-material gate-stack SOI MOSFET’s”, Microelectronics Reliability 49, 113–119 (2009).
42. Weimin Wu, Wei Yao, Gennady Gildenblat, “Surface-potential-based compact modeling of dynamically depleted SOI MOSFETs”, Solid-State Electronics 54, 595–604 (2010)
43. Jurczak M, Skotnicki T, Paoli M, Tormen B, Martins J, Regolini J L, Dutartre D, Ribot P, Lenoble D, Pantel R, Monfray S, 2000 “Silicon-on-Nothing (SON)-an Innovative Process for Advanced CMOS” IEEE Transactions On Electron Devices 47(11) 2179.
44. Sato T, Nii H, Hatano M, Takenaka K, Hayashi H, Ishigo K, Hirano T, Ida K, Tsunashima Y 2002 “Fabrication of SON(Silicon on Nothing)-MOSFET and Its ULSI Applications” IEIC Technical Report, 102(178) (SDM2002 66-106) 99-104.
45. Kilchytska V, Chung T M, Olbrechts B, VovkYa, Raskin J P, Flandre D 2007 “Electrical characterization of true Silicon-On-Nothing MOSFETs fabricated by Si layer transfer over a pre-etched cavity” Solid-State Electronics 51 1238.
46. S.Monfray, F.Boeuf, P.Coronel, G.Bidal, S.Denorme&T.Skotnicki “Silicon-On-Nothing (SON) applications for Low Power technologies” STMicroelectronics, 850 rue J.Monnet, 38920 Crolles, France (2008).
47. I. Mizushima, T. Sato, S. Taniguchi, Y. Tsunashima, Appl Phys Lett. 77 (2000), 3290.
48. W. H. Bu, R. Huang, M. Li, et al., Chin J. Phys, 15 (2006) 2751.
49. V. Kilchytska, T.M. Chung, B. Olbrechts, Ya. Vovk, J. P. Raskin, D. Flandre, Solid-State Electronics 51 (2007) 1238.
50. V. Kumari, M Saxena, R.S. Gupta, M. Gupta "Analytical Modelling of Dielectric Pocket Double-Gate MOSFET Incorporating Hot-Carrier-Induced Interface Charges", *IEEE Trans. Device and Materials Reliability*, 90 – 399, vol. 14(1), March 2014.
51. S. Naskar and S. K. Sarkar, “Quantum Analytical Model for Inversion Charge and Threshold Voltage of Short-Channel Dual-Material Double-Gate SON

MOSFET”, *IEEE Trans. Electron Devices,* vol. 60, no. 9, pp. 2734-2740, Sep. 2013

52. R. H. Dennard, F. H. Gaensslen, H-N, Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc," Design of ion-implanted MOSFET‟s with very small physical dimensions," IEEE J. Solid-State Circuits, vol. SC-9, pp. 256-268, 1974.
53. H.C. Poon, L.D. Yau, R.L. Johnston, D. Beecham, “DC Model for Short-Channel IGFET's”, *IEEE Intl. Electron. Devices Meeting, pp. 156-159*, December 1973.
54. T. Skotnicki, G. Merckel, T. Pedron, “The voltage-doping transformation: a new approach to the modeling of MOSFET short-channel effects,” *IEEE Electron Device Letters 9,* 109, 1988.
55. Anurag Chaudhry and M. Jagadesh Kumar, "Controlling Short-channel Effects in Deep Submicron SOI MOSFETs for Improved Reliability: A Review", *IEEE Trans. on Device and Materials Reliability, Vol.4*, pp.99-109, March 2004.
56. YannisTsividis “Operational Modeling of the MOS Transistor (Second Edition ed.)” *New York: McGraw-Hill. p. 268; Fig. 6.11.* ISBN 0-07-065523-5, 1999.
57. Kidong Kim et al.,"Two-Dimensional Quantum-Mechanical Modeling for Strained Silicon Channel of Double-Gate MOSFET," *Journal of the Korean Physical Society, Vol. 45,* pp. S909-S913, December 2004.
58. C. Galup-Montoro and M. C. Schneider, MOSFET Modeling for Circuit Analysis and Design, Hackensack, NJ: World Scientific, 2007.
59. E. M. Conwell, “High Field Transport in Semiconductors”, Solid State Physics Supplement 9 (Academic Press, New York, 1967).
60. A.B. Bhattacharyya, Compact MOSFET Models for VLSI Design, John Wiley & Sons (Asia) Pte Ltd.
61. Paul Harrison, Quantum Well, Wires & Dots, John Wiley & Sons Pte Ltd.
62. I. Saad, Zuhir, H. M, Pogaku, D. Bakar A. R. A, Bolong N, Khairul, A. M, Ghosh, B, Ismail, R, Hashim, U, Investigation of incorporating Dielectric pocket (DP) on vertical Strained_SiGe impact ionization MOSFET

(VESIMOS-DP)", *Semiconductor Electronics (IESC),* pp. 249-253, doi: 10.1109/SMElec.2012.6417134, Sept. 2012.

63. Bonnaud, O., Zhang, P., Jacques, E., &Rogel, R. (Invited) "Vertical Channel Thin Film Transistor: Improvement Approach Similar to Multigate Monolithic CMOS Technology", *ECS Transactions*, *37*(1), 29-37, 2011.
64. Kumari, V.; Saxena, M.; Gupta, R.S.; Gupta, M. "Analytical Modeling of Dielectric Pocket Double-Gate MOSFET Incorporating Hot-Carrier-Induced Interface Charges", *IEEE Trans. Device and Materials Reliability*, 90 – 399, vol. 14(1), March 2014
65. Lacord, J., Huguenin, J. L., Skotnicki, T., Ghibaudo, G., & Boeuf, F. "Simple and efficient MASTAR threshold voltage and subthreshold slope models for low-doped double-gate MOSFET", *IEEE transactions on electron devices*, *59*(9), 2534-2538, 2012.
66. J. Chang, A.K. Kapoor, L.F. Register, and S.K. Banerjee, "Analytical Model of Short-Channel Double-Gate JFETs," *IEEE Transaction On Electron Devices,*Vol. 57, no. 8, pp. 1533-1537, 2010.
67. J. Kim, W. Sun and H. Shin, "A new I-V model for surrounding gate MOSFET considering Gate voltage dependent quantum effect", vol. 100(8), pp. 1072-1079, 2013.
68. Jihyun Kim, Wookyung Sun, Seunghye Park, Hyein Lim, Hyungsoon Shin," A Compact Model of Gate-Voltage-Dependent Quantum Effects inShort-Channel Surrounding-Gate Metal-Oxide-Semiconductor Field-Effect Transistors", Journal of Semiconductor Technology and Science Vol.11 No.4,pp.278-286,2011.12
69. Amara Amara, Olivier Rozeau, Planar Double-Gate Transistor, Springer 2009.
70. A. S. Spinelli, A. Benvenuti, and A. Pacelli, "Self-consistent 2-D model for quantum effects in n-MOS transistors", Electron Devices, IEEE Transactions on, vol. 45, no. 6, pp. 1342-1349, 1998.
71. F. Pregaldiny, C. Lallement, and D. Mathiot, "Quantum surface potential model suitable for advanced MOSFETs simulation", IEEE International Conference on Simulation of Semiconductor Processes and Devices 2003, pp. 227-230.

72. Y. Omura, S. Horiguchi, M. Tabe, K. Kishi: Quantum-mechanical effects on the threshold voltage of ultrathin SOI n MOSFETs. IEEE Electron Device Letters 14-12, 569 (1993)
73. H. Davies, “The physics of low dimensional semiconductors.” New York: Plenum, 1998
74. P.R. Kumar and S. Mahapatra, “Analytical modeling of quantum threshold voltage for triple gate MOSFET”, Solid-State Electron, vol. 54, no. 12, pp. 1586-1591, Dec.2010.
75. T. Skotnicki, G. Merckel, T. Pedron: The voltage-doping transformation: a new approach to the modeling of MOSFET short-channel effects. IEEE Electron Device Letters 9, 109 (1988)
76. T. Skotnicki : Heading for deca-nanometre CMOS - is navigation among icebergs still a viable strategy? Proceedings of the 30th European Solid State Device Research Conference. Frontier Group, Gif-sur-Yvette, France, 19 (2000)
77. W.Xiong, K. Ramkumar, S.J. Jamg, J.T. Park, J.P. Colinge: Self-aligned ground-plane FDSOI MOSFET. Proceedings of the IEEE International SOI Conference, 23 (2002)
78. T. Sekigawa and Y. Hayashi: Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate. Solid-State Electronics 27, 827 (1984)
79. T. Sekigawa, Y. Hayashi, K. Ishii: Feasibility of very-short-channel MOS transistors with double-gate structure. Electronics and Communications in Japan, Part 2. 76-10, 39 (1993)
80. T. Skotnicki: Ultimate scaling of SOI MOSFETs. MIGAS Short Course, Villard de Lans, France (2004)