Buck Converter fed Four Switch Three Phase Inverter based BLDC Motor Drive without Current Controlled PWM technique

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CERTIFICATE

This is to certify that the thesis entitled '**Buck Converter fed Four Switch Three Phase Inverter based BLDC Motor Drive without Current Controlled PWM technique**' submitted by **Shri Kashif Bakht Muhammad Nab**i in partial fulfilment of the requirements for the award of Master of Engineering degree in Electrical Engineering at Jadavpur University, Kolkata is an work carried out by him under our supervision and guidance. To the best of our knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any degree or diploma.

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Dedicated

To
my beloved country,

INDIA

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ABSTRACT

The aim of this project is to explore the possibility of introducing a buck converter at the input side of a conventional four switch three phase inverter based BLDC motor drive for speed control applications. This has been done by regulating the input D.C. link voltage using PWM technique. An arrangement has also been made for storing the dissipative energy during the freewheeling period of the pulse width. The proposed drive system has the novel feature of not employing current controlled PWM technique, thereby further reducing cost and complexity. Simulation of the proposed drive system has been performed by using the *MATLAB /SIMULINK* tools and satisfactory results are obtained.

Keywords—*BLDC Motor, Speed control, Buck Converter, Four Switch Three Phase Inverter, Energy recovery, Matlab / Simulink*

CHAPTER-1

INTRODUCTION

Brushless Direct Current (BLDC) motors are finding great usage in industry these days due to their innate stability, easiness in control, high torque weight ratio, good power factor, high power density, high efficiency and less maintenance due to replacement of mechanical brush with electronic commutation. Speed control of BLDC motor is commonly achieved through Pulse Width Modulation (PWM) of input voltage source.

However, in spite of having all these technical advantages the main concern is the cost of BLDC drive. For reducing the cost of inverter for a three phase BLDC motor drive it was found that two switches may be reduced from the conventional six switch inverter due to inherent characteristics of the BLDC motor.

While developing such a drive system it was found that due to reduced number of switches, phase C current became uncontrollable leading to a phenomenon called *asymmetric voltage PWM,* which could lead to breakdown of the system. Such a problem was solved by employing the current controlled PWM technique.

However in the conventional Four Switch Three Phase Inverter (FSTPI) based BLDC motor drive with current controlled PWM there is no scope for saving of the dissipative energy during the turn off time of the PWM. Moreover, since, the PWM is current controlled so the speed control of the system is difficult. This is because; in the current controlled PWM FSTPI based BLDC motor drive the input supply voltage is fixed. As a result except for modes 2, 5 every other mode has to run at half the rated supply voltage leading to poor speed response. Thus for better speed control of BLDC motor a topology is required where the input supply voltage is controlled through PWM, which will again lead to the problem of *asymmetric voltage PWM* due to the introduction of voltage vectors into the system.

This problem has been solved in the proposed drive. The project work proposes a simple, cost effective buck converter fed four switch three phase inverter based BLDC motor drive for speed control application. This has been done by regulating the input DC link voltage using PWM technique. An arrangement has also been made for storing the dissipative energy during the freewheeling period of the pulse width. The proposed drive system has the novel feature of not employing current controlled PWM technique, thereby further reducing cost and complexity. Simulation of the drive system has been performed on Matlab / Simulink platform.

A brief over view of the chapters discussed in this thesis is given below.

Chapter 1 serves as an introduction to the project, narrates the importance of buck converter fed four switch three phase inverter based BLDC motor drive, highlights the energy saving feature of the proposed drive and mentions the advantage of using voltage controlled PWM technique in place of current controlled PWM used in conventional four switch three phase inverter (FSTPI) based BLDC motor drive without introducing asymmetric voltage PWM.

Chapter 2 gives a brief account of the previous work done in the area of FSTPI based BLDC motor drive, the drawbacks of conventional FSTPI based BLDC motor drive is also mentioned here which serves as the motivation behind the project.

Chapter 3 discusses a basic 3ϕ BLDC motor's working principle, its construction, characteristics, and applications. The theory behind closed loop speed control and the related aspects is explained.

Chapter 4 gives a brief account of the conventional buck converter fed six switch inverter based BLDC motor drive system. The discussion provides the pros and cons of the conventional based drive system commonly used for speed control of 3ϕ BLDC motor. Such a discussion allows one to explore the possibility of extending the benefits of the conventional buck converter fed six switch inverter based BLDC motor drive system to a FSTPI based BLDC motor drive system.

Chapter 5 discusses in detail the conventional FSTPI based BLDC motor drive using current controlled PWM technique for back emf compensation. The chapter helps to understand the issue of asymmetric voltage PWM in detail and thus helps in formulating methods in order to suppress such issue in the proposed drive.

Chapter 6 gives a detailed account of the proposed buck converter fed FSTPI based BLDC motor drive. Here the topology has been discussed in full detail and appropriate solution has been suggested for removing the various problems faced by the proposed drive system.

Chapter 7 discusses the energy saving mechanism of the proposed drive. It also depicts the manner in which the stored dissipative energy can be utilised for future use.

Chapter 8 depicts various results of the simulation of the proposed drive performed on Matlab / Simulink platform.

Chapter 9 is a discussion on the various advantages and drawbacks of the proposed drive system with respect to other six switch inverter based drive systems.

Chapter 10 lists the future scope of work that may be done in the proposed drive system for better performance.

CHAPTER-2

MOTIVATION OF THE PROJECT

2.1. BACKGROUND OF THE PROJECT

Analysis of a BLDC motor shows that at any point of time only two phases are activated whereas the third phase remains silent [9]. Taking advantage of such a condition it was thought that two switches of any phase could be eliminated without any problem. However such elimination led to the unique problem of *asymmetric voltage vector*, that is, the two space vectors corresponding to the switching of phase C became absent resulting in uncontrolled voltage supply during space vector pulse width modulation (SVPWM) of the input supply voltage. The absenteeism of the above mentioned voltage vectors can be attributed to the direct connection of phase C with the midpoint of the D. C. bus voltage as shown in figure 1. Such a direct connection of phase C without any control mechanism leads to uncontrolled flow of current leading to distortion of current waveforms from the ideal quasi square shape. All this necessitated the introduction of a new control mechanism for the four switch inverter based BLDC motor drive. Accordingly a novel technique by the name *current controlled PWM* technique was introduced in [1], where in the currents of active phases were independently controlled using PWM by fixing the input supply voltage. This ensured that the phase current distortion got eliminated. The current controlled PWM technique of removing phase current distortion has been discussed in detail in chapter 5.

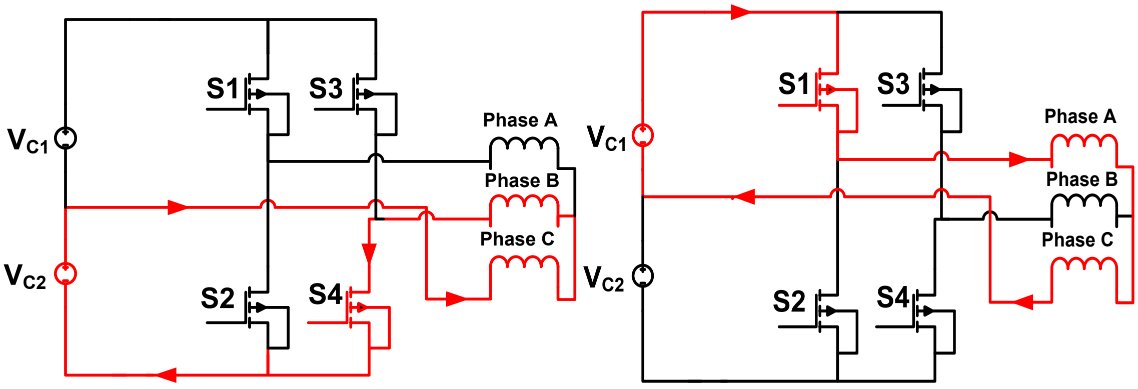


Fig. 1: Uncontrolled current flow through phase C

2.2 DRAWBACKS OF THE FOUR SWITCH THREE PHASE INVERTER BASED BLDC MOTOR DRIVE WITHCURRENT CONTROLLED PWM TECHNIQUE

As stated above, a conventional FSTPI based BLDC motor drive employing current controlled PWM technique requires the input side voltages to be fixed to prevent introduction of voltage vectors into the system which could lead to asymmetric voltage PWM resulting in distortion in phase currents. However such fixing of the input side voltage has a negative impact on the speed response of the system as the BLDC motor has to run at half the rated speed for four out of six modes. Chapter 5 gives a more elaborate description of the reason behind poor speed response of the system. However such a poor speed response renders the conventional FSTPI based BLDC motor drive practically useless for speed control applications.

Also in the conventional FSTPI based BLDC motor drive no arrangement has been made for saving the dissipative energy during freewheeling period of the PWM pulse width.

2.3 NECESSITY OF SPEED CONTROL

The above mentioned drawback of the conventional FSTPI based BLDC motor drive has necessitated the control of input side supply voltage for speed control applications. Accordingly, a possibility of introducing buck converter at the input supply terminals for supply voltage modulation has been explored in the proposed model which has been thoroughly discussed in chapter 6. Also arrangement has been made in the proposed drive in the form of rechargeable batteries for saving the dissipative energy during the PWM off period.

CHAPTER-3

BRUSHLESS DC MOTOR

3.1 OPERATING PRINCIPLE

BLDC motor is a type of synchronous motor. This means the magnetic field generated by the stator and the magnetic field generated by the rotor rotate at the synchronously.BLDC motors are of single-phase, 2-phase and 3-phase types. Amongst these, 3-phase motors are the most popular and widely used. The stator windings are connected to DC supply which can be varied using PWM signals.The commutation process of a BLDC motor is controlled electronically. This prevents mechanical wear and tear and losses, thereby increasing efficiency. In order to rotate the BLDC motor, the stator windings should be energized in a proper sequence in order to generate a rotating magnetic field that ‘drags’ the permanent magnet mounted rotor along with it. Therefore it is important to know the position of the rotor in order to understand which stator winding has to be energized following the energizing sequence [9].

3.2 CONSTRUCTION

- **STATOR**

The stator windings of BLDC motor have two variants -- trapezoidal and sinusoidal motors. This classification is made on the basis of the interconnection of coils in the stator windings to give the different types of back electromotive force (emf) wavefoms.This leads to the current waveform aquiring corressponding shapes of trapezoid or sinusoid . Sinusoidal current profile leads to the torque output becoming smoother than the trapezoid with the only disadvantage of extra winding interconnections, thereby increasing copper cost [10].

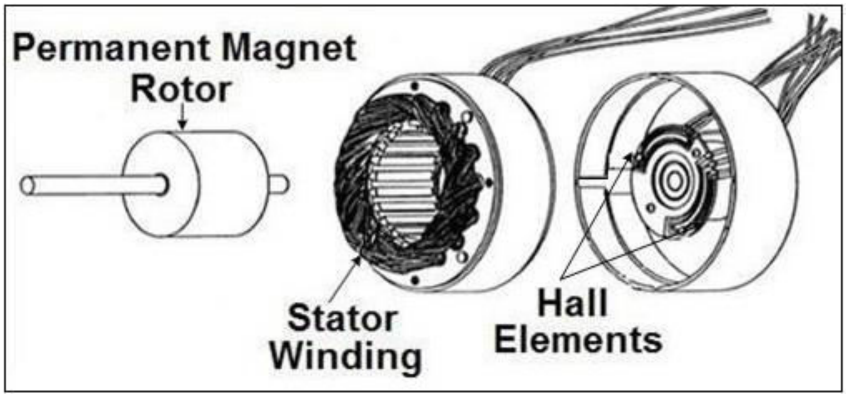


Fig. 2 : Different parts of a typical BLDC motor

- **ROTOR**

As the name suggests, the rotor is made up of permanent magnet. Permanent magnets are chosen based on specific requirements. Ferrite magnets are generally used, however rare earth alloy magnets are also becoming popular. The main parameter for selecting permanent magnet is the flux density per unit volume.

- **HALL SENSORS**

Rotor position is sensed using hall effect sensors embedded into the stator of the motor. Hall effect sensor determines the rotor's position by giving value 1when unlike poles are closest and value 0 when like poles are closest [8]. Then this digital output is sent to the electronic controller which spins the rotor at the right time by properly energizing the stator windings in the right sequence for proper direction of rotation.

3.3 BACK EMF

The equations relating the back emf generated in the stator phases of the BLDC motor to the speed is shown below.

$$E_b=K_E* \omega \qquad \text{..............} \ (1)$$

$$\text{Or, } \omega = E_b / K_E \qquad \text{..............} \ (2)$$

where E_b : per phase back emf , K_E : back emf constant and ω : rotor speed.

$$E_b=V-I_a*r_a \qquad \text{..............} \ (3)$$

where V: supply voltage, I_a : phase current and r_a : phase resistance

$$T= K_T*I_a \qquad \text{.............} \ (4)$$

where T: Torque, K_T: Torque constant and I_a: phase current

3.4 CLOSED LOOP CONTROL

As evident from equation 2 and 3 the speed of a BLDC motor is dependent on the back emf which in turn is dependent on supply voltage. Thus by controlling the input supply voltage one can easily control the speed. The input supply voltage can be controlled by changing the duty cycle of a chopper. Thus speed can be controlled in a closed loop by measuring the actual speed of the motor. The error in the set speed and actual speed is calculated. A Proportional plus Integral plus Derivative (PID) controller can be used to amplify the speed error and dynamically adjust the PWM duty cycle.

3.5 MECHANISM OF CONTROL

Figure 3 shows that when electrical currents flow through Q1, Q3, and Q4, then terminals A and B have the battery voltage, while terminal C has zero potential. In this state, a current will flow from terminal A to C, and another current from B to C. It is assumed that the solid arrows in this figure indicate the directions of the magnetic fields generated by the currents in each phase. The dotted arrow in the centre of the delta connected stator winding, indicated as F1, represents the resultant magnetic field in the stator. The rotor is placed in such a position that the field flux indicated by F2 will have a 90° angle with respect to the stator's magnetic field as shown in the figure. In such a state a clockwise torque (F1 x F2) will be produced on the rotor. Similarly as other groups of switches are turned on and off in the following sequence, as shown in table 1; the resultant stator mmf drags the rotor along with it in clockwise direction as shown in figure 4. The rotational direction may be reversed by complementing the digital output of the position sensor.

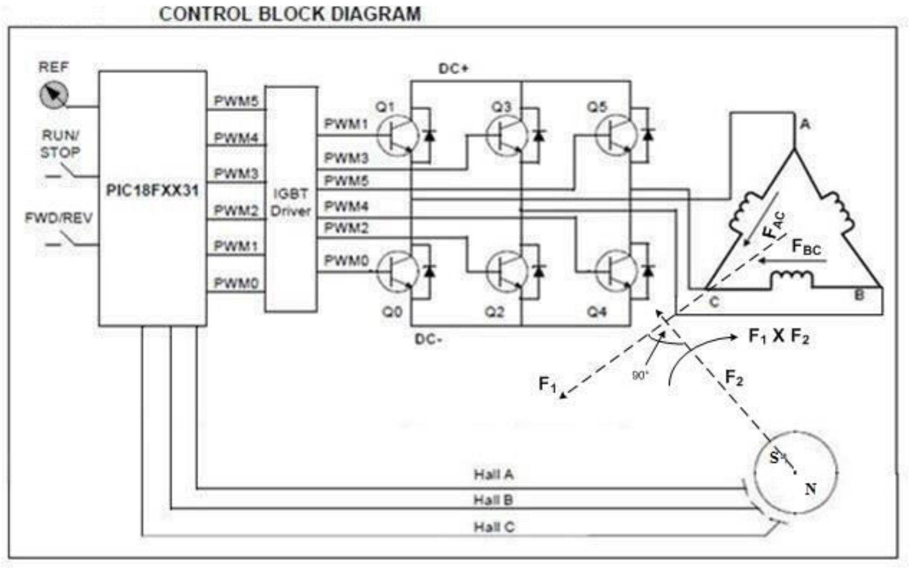


Fig. 3 Schematic showing Control mechanism of a typical BLDC motor

Table 1: Switching sequence for clockwise rotation

ON-OFF Sequence	1	2	3	4	5	6
Q0	0	1	1	1	0	0
Q1	1	0	0	0	1	1
Q2	0	0	0	1	1	1
Q3	1	1	1	0	0	0
Q4	1	1	0	0	0	1
Q5	0	0	1	1	1	0

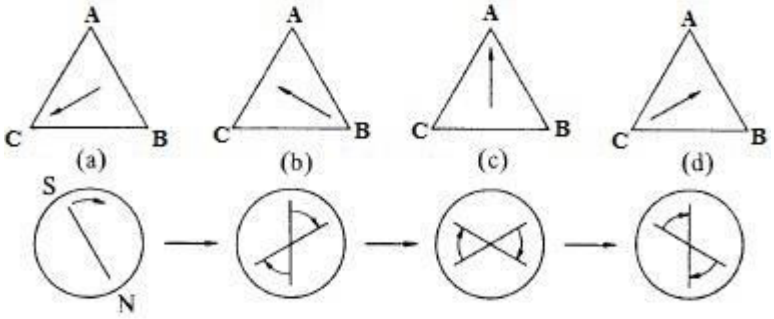


Fig. 4 : Clockwise revolution of stator magnetic field and rotor

3.5 TORQUE SPEED CHARACTERISTICS

Figure 5 shows the torque speed characteristic of a typical BLDC motor. Since the torque speed characteristic is linear and drooping in nature; hence speed can be controlled only by controlling the terminal voltage [2].

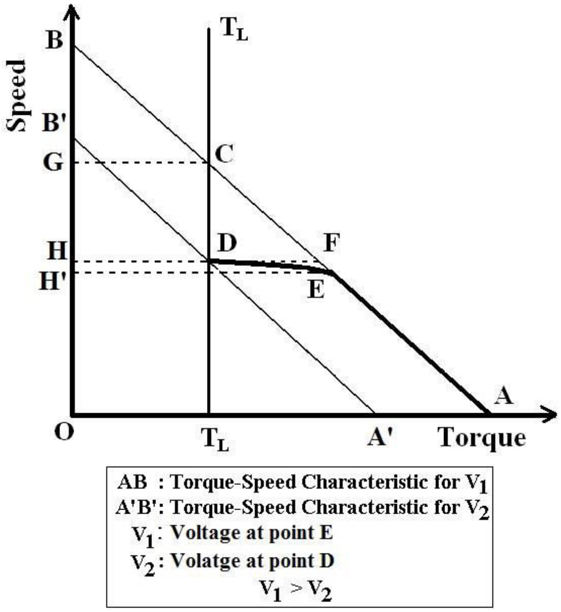


Fig. 5 : Torque Speed characteristics of an ideal BLDC motor

The BLDC motor operates with open loop operating point C on speed-torque characteristic curve and runs with speed OG for load torque T_L and applied voltage V_1 . Hence OG is termed as the open loop speed for the motor. When voltage is applied the motor starts from point A and reaches up to point C following the curve AB due to its inherent characteristics. Now suppose if the motor is to be operated with the load torque T_L

and the speed indicated by OH is to be achieved. Hence after starting, when the motor traverses the curve AB and reaches the point E, the PID controller judges that this speed OH' is very close to the set speed OH. At this stage the torque at point E, denoted by T_E, is still greater than T_L. Therefore T_E must be reduced to make it equal to T_L in order to achieve the desired speed at that load. This can be achieved by simply reducing the voltage level. Controller must be properly designed in order to reduce the voltage from V_1 to V_2 at point E. In this way the motor traverses the path ED and reaches the desired operating point D and runs with set speed maintaining the same load torque.

CHAPTER-4

CONVENTIONAL SIX SWITCH INVERTER BASED 3ϕ BLDC MOTOR DRIVES

4.1 BIPOLAR VSI FED BLDC DRIVE

This drive system employs a Voltage Source Inverter (VSI) for modulation of D.C link voltage in order to control the speed of a BLDC motor. The term bipolar indicates that the flow of current is bidirectional, that is, from rectifier to inverter and vice versa. This drive system is primarily used for high power motor (>100 Watts).

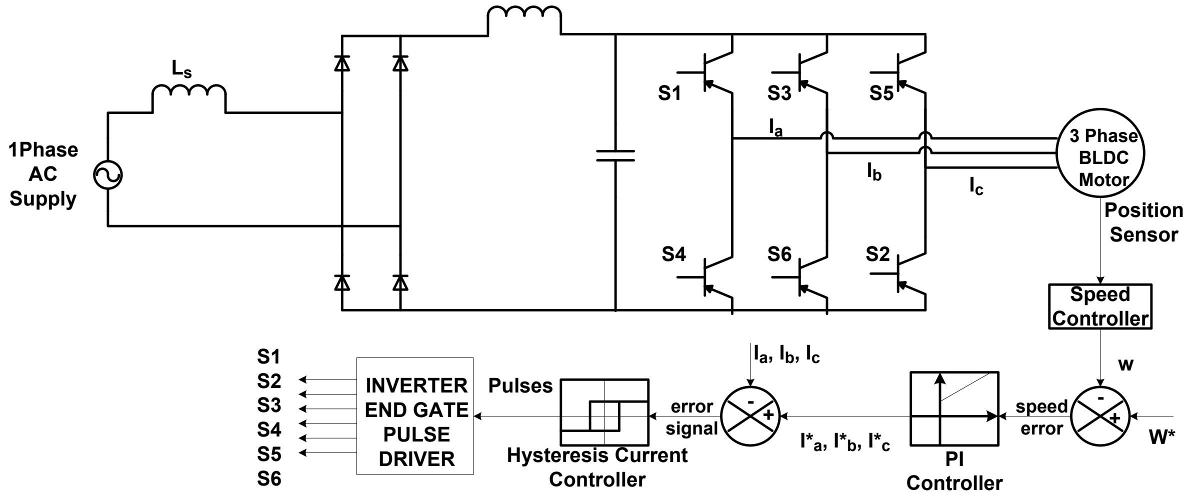


Fig. 6: Schematic showing a typical Bipolar VSI fed BLDC Drive System

The drive system is fed from a single phase AC supply which is rectified to get the DC link voltage. The error in speed (difference of actual speed, w, and set speed w*) is processed through a PI controller to limit the error within a specified range. This conditioned signal from the PI controller is then used to generate the reference phase current signals (I^*_a, I^*_b, I^*_c) using the position sensor output. The instantaneous phase currents (I_a, I_b, I_c) are then compared with the reference phase current signals in order to generate the error in current profile of the three phases. This current error signal is then passed through the hysteresis current controller to limit the error within a specific tolerance band (generally 5%). The pulses then generated from the hysteresis controller is then used to control the firing angle of the inverter switches, there by modulating the D.C link voltage for necessary reduction of error in speed.

4.2 UNIPOLAR VSI FED BLDC DRIVE SYSTEM

This type of drive system is primarily used for low power motor (< 100 Watts), hence its utilisation is very small. However as compared to a Bipolar VSI fed BLDC Drive the switching losses in this type of drive is reduced by half due to reduction in the number of switches. The above schematic can be explained as before. From the schematic it is noticed that this drive system employs a DC voltage source at its input unlike the Bipolar VSI fed drive where an AC voltage source is employed as input, hence there is no need for rectification. Also it is noted that the flow of current in this drive system is unidirectional hence the name, Unipolar.

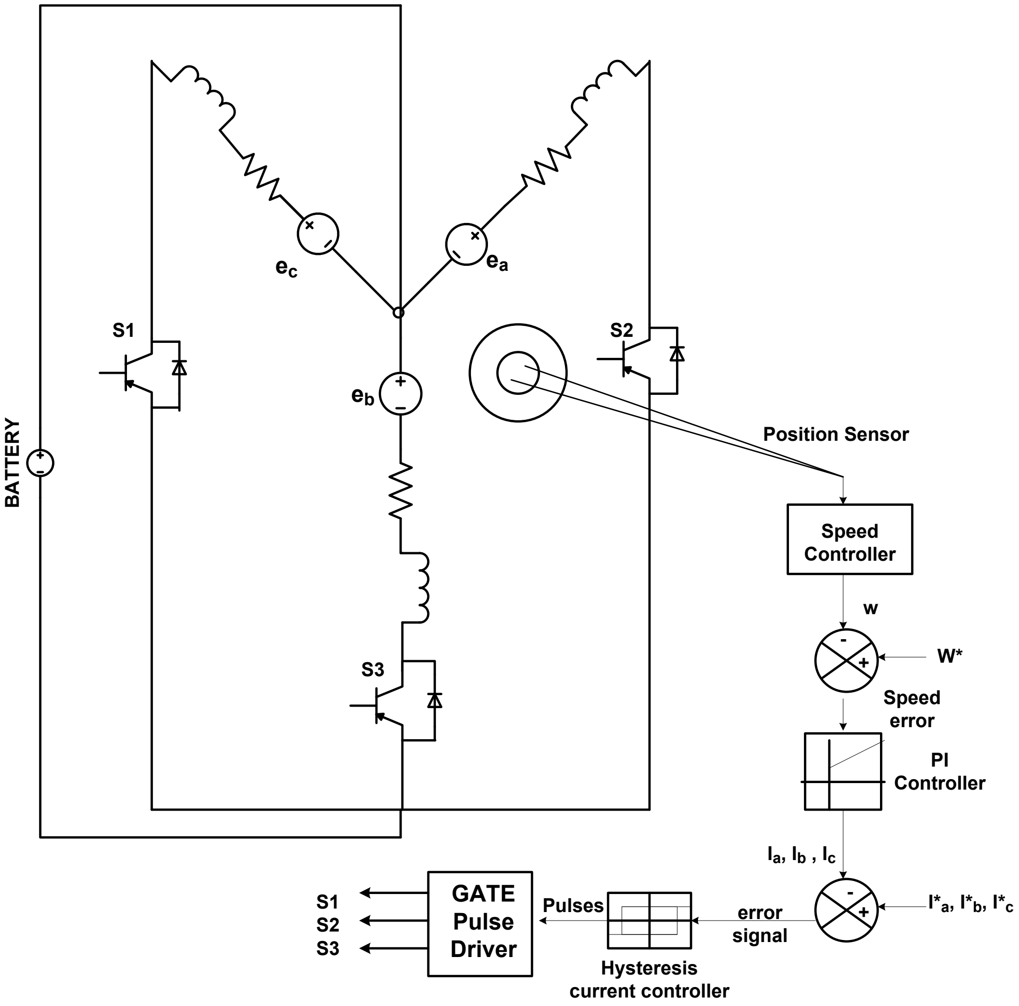


Fig. 7: Schematic showing a typical Unipolar VSI fed BLDC Drive System

4.3 CSI FED BLDC MOTOR DRIVE

This drive employs a Current Source Inverter (CSI) for modulation of the DC link voltage. Since, Current Source Inverter is employed so constant current is maintained by connecting an inductor between the rectifier and inverter. The reference DC link (I^*_d) current through the inductor is generated using the error in speed, thus by reducing the error in the DC link current, reduction of error in speed occurs automatically. Therefore the error signal generated in the DC link current is passed through a hysteresis current controller in order to generate pulses for firing of inverter switches in a controlled manner, thereby modulating the DC link voltage for reducing the speed error.

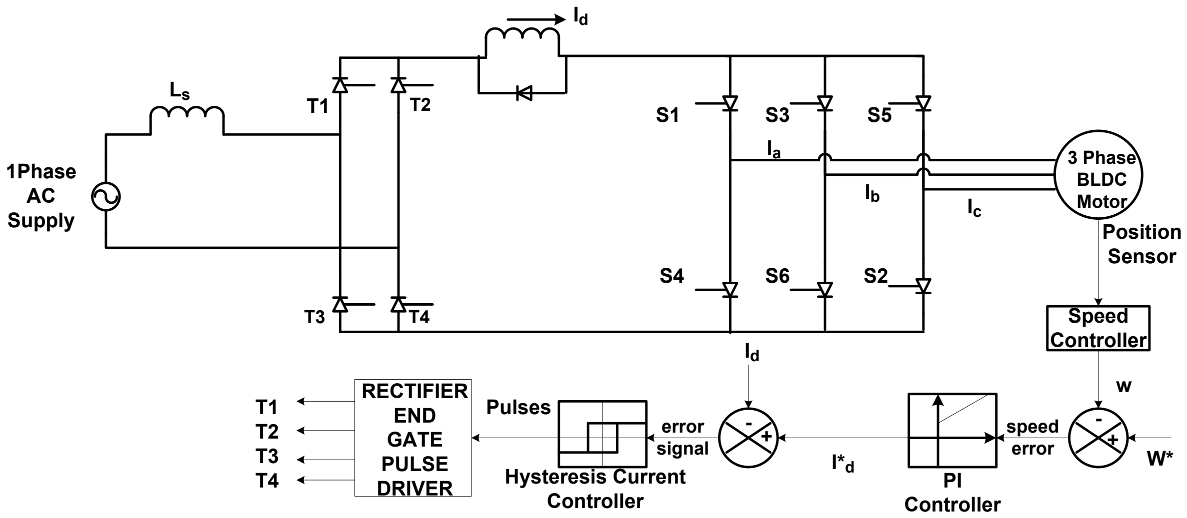


Fig. 8: Schematic showing a typical CSI fed BLDC Motor Drive System

This drive system however is has the disadvantage of being bulky and costly because of the need for a filter in order to generate the DC link bus voltage. Since the filter to be employed needs to be of handle a wide range of frequency hence it becomes bulky and costly. In order to do away with such a need for a filter the following topology is utilised.

4.4 BUCK CONVERTER FED CSI BASED BLDC MOTOR DRIVE

The following topology (figure 9) is employed using a conventional six switch/three leg inverter for controlling the speed of a BLDC motor. The biggest advantage of such topology is that unlike a conventional CSI (Current Source Inverter) topology of a BLDC motor drive there is no need for bulky filter of wide range frequency. Moreover switching of the switches in the inverter is of low frequency, occurring only when current commutation is required during the various modes. As a result switching losses are also reduced as compared to conventional VSI (Voltage Source Inverter) fed topology of BLDC motor drive. In the proposed drive the aim is to extend the advantages of the conventional buck converter fed CSI topology of BLDC motor employing six switch inverter to a low cost four switch inverter based BLDC motor drive along with additional benefits like no requirement of current sensing and energy saving.

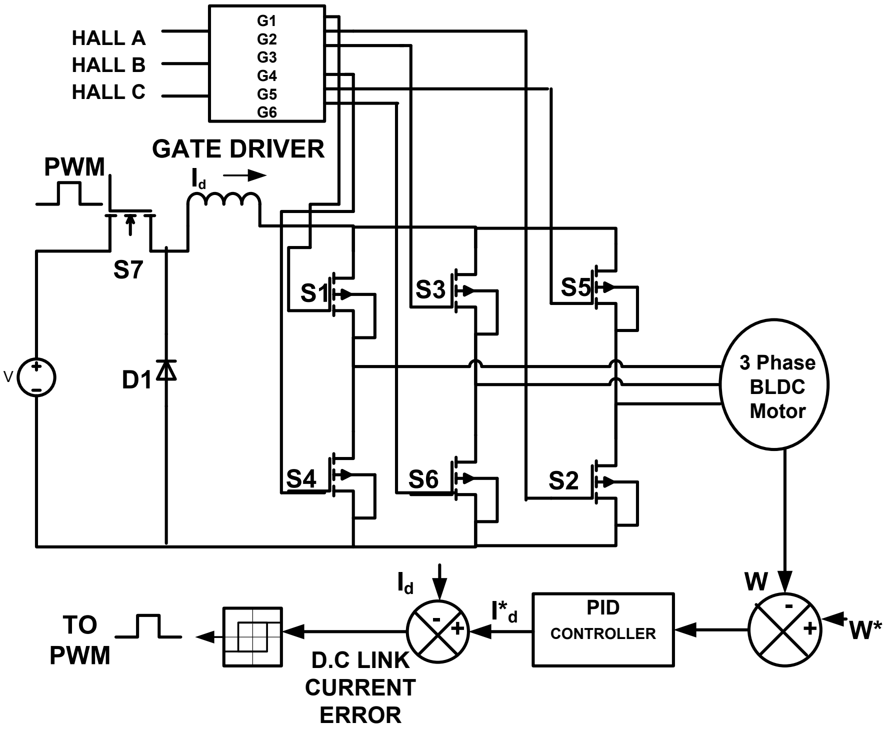


Fig. 9: Schematic of Conventional Buck Converter fed CSI topology of BLDC motor drive

CHAPTER-5

FSTPI BASED BLDC MOTOR DRIVE WITH CURRENT CONTROLLED PWM TECHNQUE FOR BACK EMF COMPENSATION

5.1 THEORY BEHIND FSTPI BASED BLDC MOTOR DRIVE

As discussed previously in chapter 3, a BLDC motor requires proper switching for generating rotating magnetic field in the right direction so that the rotor is dragged along with it. Figure 10 shows the ideal back emf waveforms and current profile of a typical BLDC motor with respect to the angular position of the rotor. From this figure one can easily find out the exact angular position of the rotor when commutation is required.

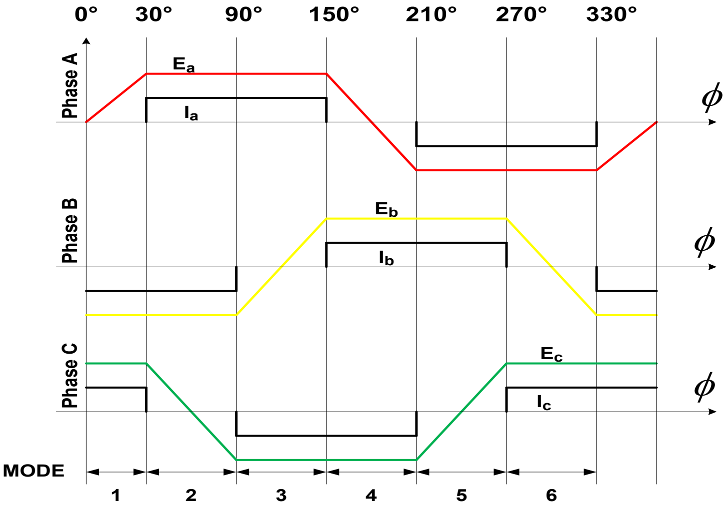


Fig.10: Voltage and Current waveforms during the six modes of operation in a BLDC motor

Moreover the above figure shows that at any point of time only two phases are active and the third one is inactive. This fact along with phase current relationships has been depicted in table 2 for ease of understanding.

Table 2 : Condition of phases during various modes of operation

Mode	Current equation	Active Phases	Silent Phase
1 (0°<Ø<30°)	$I_b + I_c = 0$ & $I_a = 0$	C,B	A
2 (30°<Ø<90°)	$I_a + I_b = 0$ & $I_c = 0$	A,B	C
3 (90°<Ø<150°)	$I_a + I_c = 0$ & $I_b = 0$	A,C	B
4 (150°<Ø<210°)	$I_b + I_c = 0$ & $I_a = 0$	B,C	A
5 (210°<Ø<270°)	$I_a + I_b = 0$ & $I_c = 0$	B,A	C
6 (270°<Ø<330°)	$I_a + I_c = 0$ & $I_b = 0$	C,A	B

Thus from table 2 one can easily infer that a BLDC motor acts as a two phase motor instantaneously and hence requires only four switches (that is, two switch per phase) for control instead of six. This fact was utilized in [1] and a drive system was developed for a typical BLDC motor using four switch inverter as shown in figure 11.

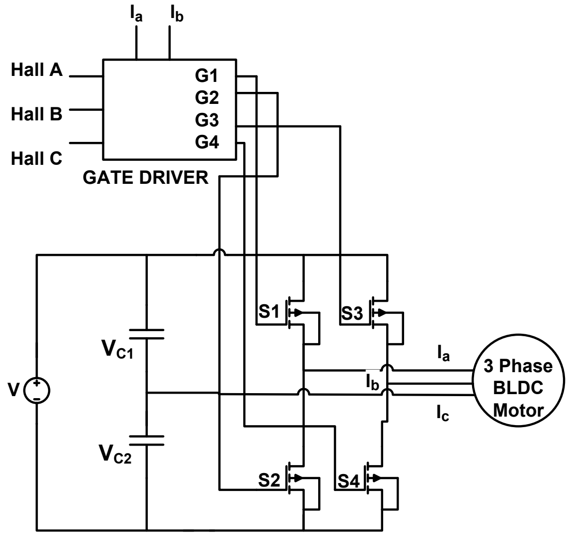


Fig. 11: Conventional FSTPI based BLDC motor drive

5.2 THE SIX MODES OF OPERATION

From figure 11, one can easily notice that current in phase A is controlled using switches S1 and S2 and current in phase B is controlled using switches S3 and S4. Thus the six modes of operation (table 1) covering 360°of rotor's angular movement can be achieved easily by proper switching of switches S1, S2, S3, and S4. Thus based on table 2 the proper switching pattern for conventional FSTPI based BLDC motor is depicted in table 3.

Table 3 : Switching sequence of FSTPI based BLDC motor drive

MODES	ROTOR POSITION (Ø)	ACTIVE PHASES	SILENT PHASES	SWITCHING DEVICES
1	0°<Ø<30°	C,B	A	S_4
2	30°<Ø<90°	A,B	C	S_1 & S_2
3	90°<Ø<150°	A,C	B	S_1
4	150°<Ø<210°	B,C	A	S_3
5	210°<Ø<270°	B,A	C	S_2& S_3
6	270°<Ø<330°	C,A	B	S_2

The six modes of operation with the exact manner of current flow is pictorially depicted in the following figure.

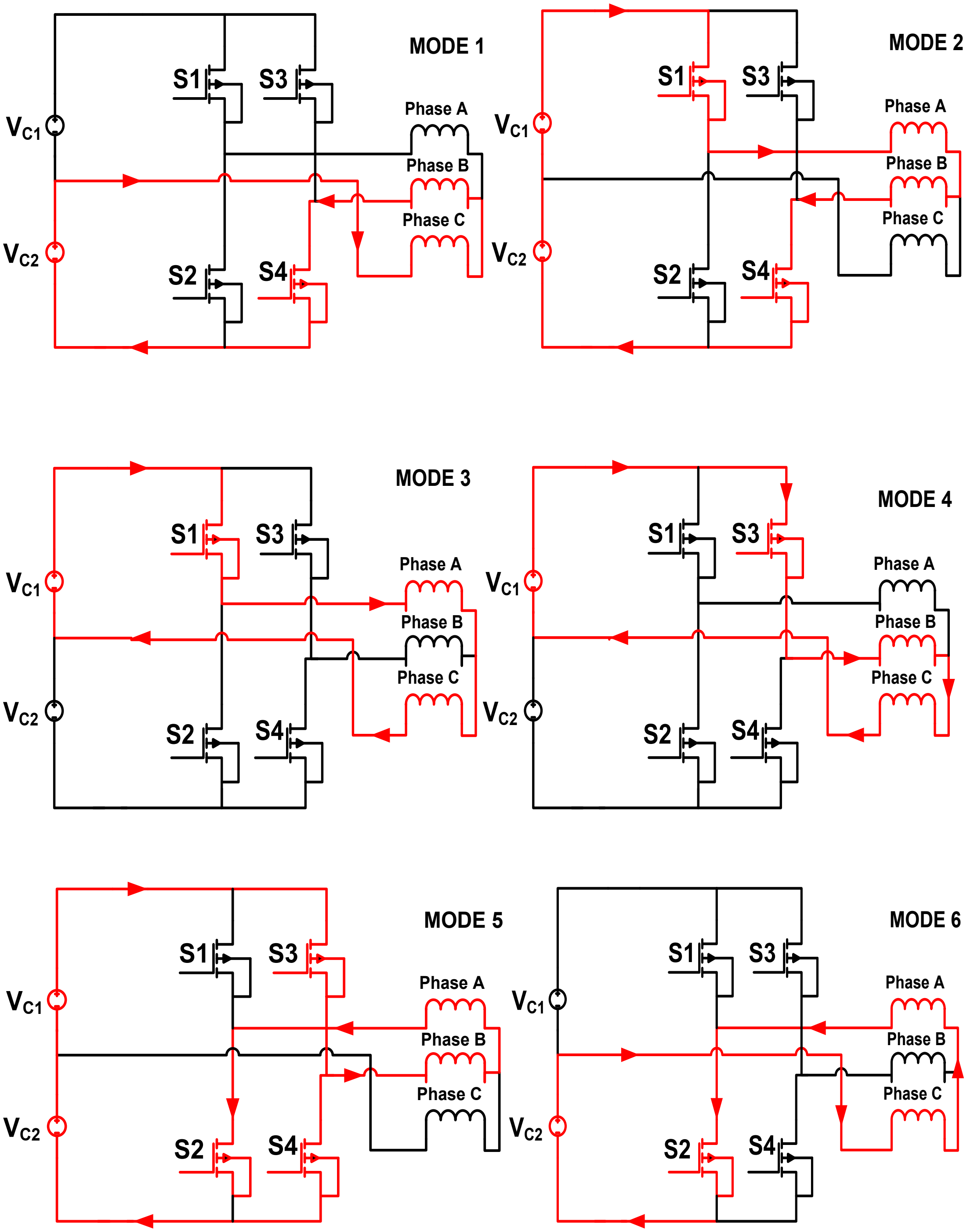


Fig.12 Modes of Operation

5.3 ISSUE OF ASYMMETRIC VOLTAGE PWM

As discussed in the earlier section, a BLDC motor can theoretically be controlled using four switches. However it is observed that elimination of two switches along phase C led to the unique problem of '*asymmetric voltage PWM'* [1]. The main reason behind asymmetric voltage PWM was the unnecessary flow of current along phase C due to the absence of controlling switch along it when only phase A and B remained excited (mode 2 and 5). The following figure 13 gives a pictorial description of the preceding text.

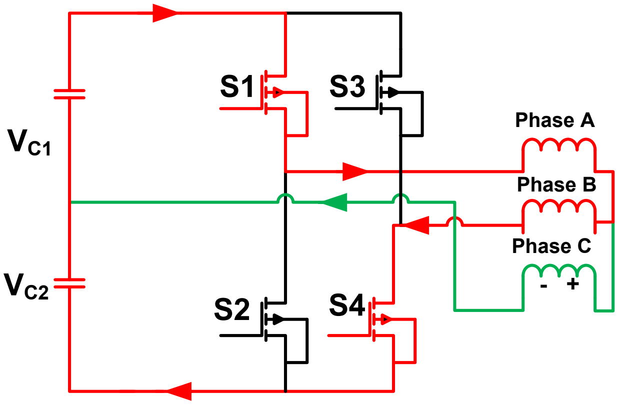


Fig. 13 Back emf induced current along phase C

That is, during modes 2 and 5 there is no requirement of current flow along phase C as evident from the ideal current waveform shown in figure 10 and the current equations depicted in table 2. But due to the induced back emf in phase C due to active phases A and B during modes 2 and 5 there is a tendency for the current to flow along phase C during such modes. This tendency could not be stopped due to the absence of controlling switch along phase C in the conventional four switch three phase inverter based BLDC motor drive. As a result of this unnecessary flow of current along phase C the phase current waveforms get distorted from the desired quasi-square shape as shown in the following figure 14. This typical condition is termed as *'asymmetric voltage PWM'* phenomenon. It is also observed from figure 14 (iii) that the current in phase C cannot stabilize along the zero level which can be very dangerous as such a condition leads to breakdown of the system.

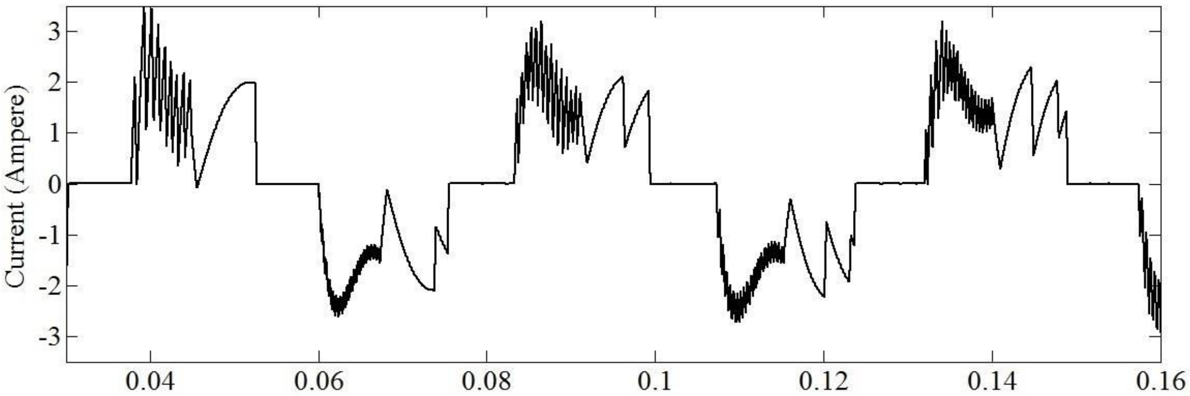


Fig.14(i)Current profile of phase A with back emf problem

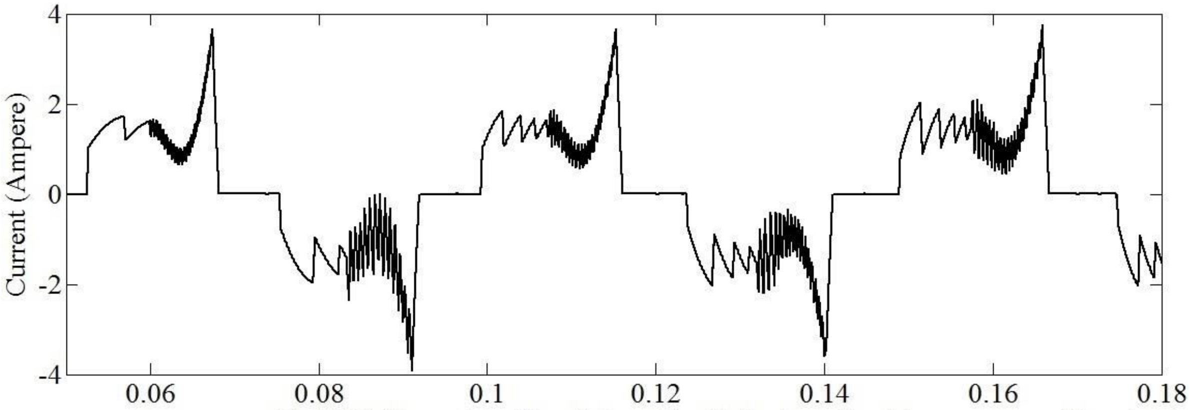


Fig.14(ii) Current profile of phase B with back emf problem

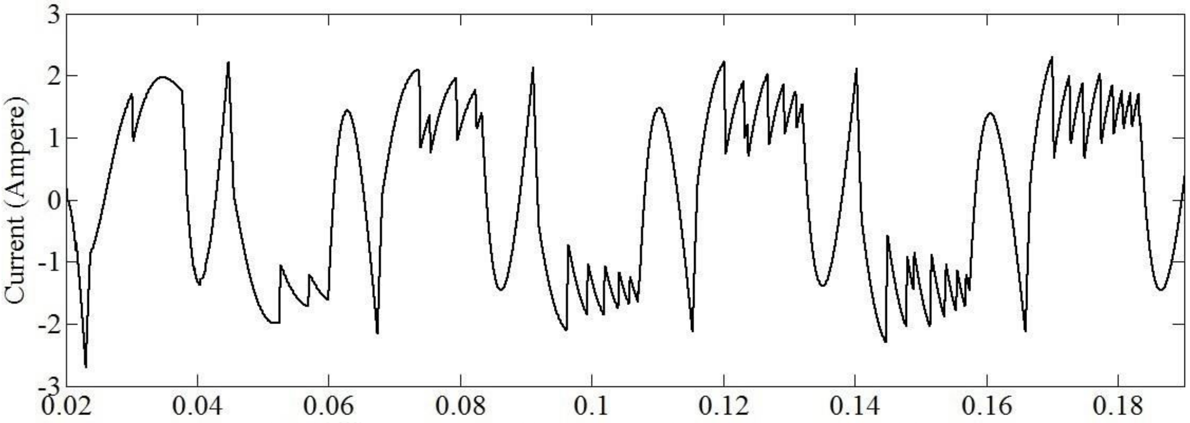


Fig.14(iii) Current profile of phase C with back emf problem

5.4 CURRENT CONTROLLED PWM TECHNIQUE FOR BACK EMF COMPENSATION

To solve the unique problem of *'asymmetric voltage PWM'* a novel technique was developed in [1] by the name *'Current Controlled PWM'*. In the said technique voltage controlled PWM was replaced with current controlled PWM using the reference current generated from the closed loop speed error. The main idea behind such technique was that if the current in phase A and B is controlled independently using PWM (figure 15) then the distortion in phase A and B current waveforms from ideal characteristics could be eliminated and since the phase C current is indirectly associated with the phase A and B currents at any point of time (table 2); the distortions produced in it could also be tackled effectively. Thus this technique resulted in the stabilization of phase C current at zero level, an essential condition to prevent break down of the system (Fig. 17 (iii)). The reference current signals of phase A and B (I_{a_ref} and I_{b_ref}) for comparison with instantaneous currents in the respective phases are generated using Fig. 10 and Table 3.

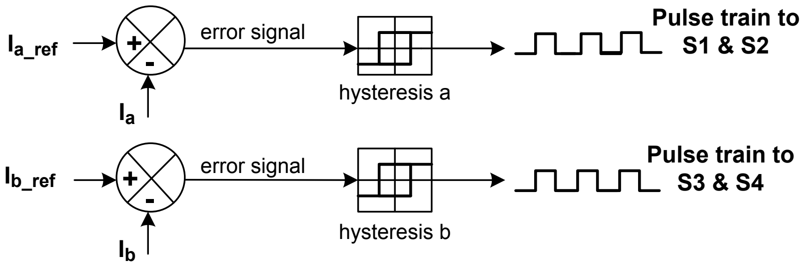
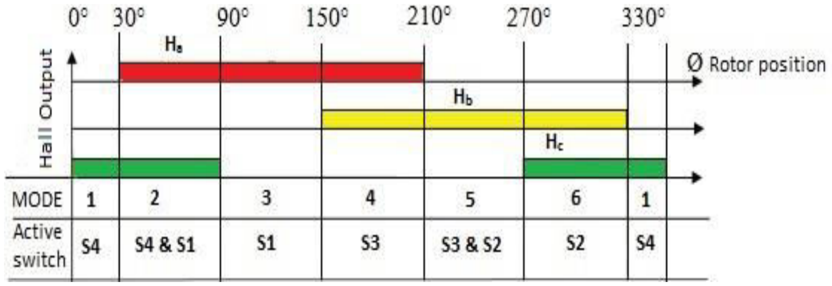


Fig. 15: Current controlled PWM technique for back emf compensation



MODE	1	2	3	4	5	6	1
Active switch	S4	S4 & S1	S1	S3	S3 & S2	S2	S4

Fig. 16: Hall sensor output voltage for rotor position detection

Table 4 : Reference current generation sequence

Hall Sensor Output			**Active Phases**	**Switching Devices**	**I_{a_ref}**	**I_{b_ref}**
h_a	**h_b**	**h_c**				
0	0	1	C,B	S_4	0	$- i_{ref}$
0	1	0	B,A	S_2 & S_3	$- i_{ref}$	$+ i_{ref}$
0	1	1	C,A	S_2	$- i_{ref}$	0
1	0	0	A,C	S_1	$+ i_{ref}$	0
1	0	0	A,B	S_1 & S_4	$+ i_{ref}$	$- i_{ref}$
1	1	0	B,C	S_3	0	$+ i_{ref}$

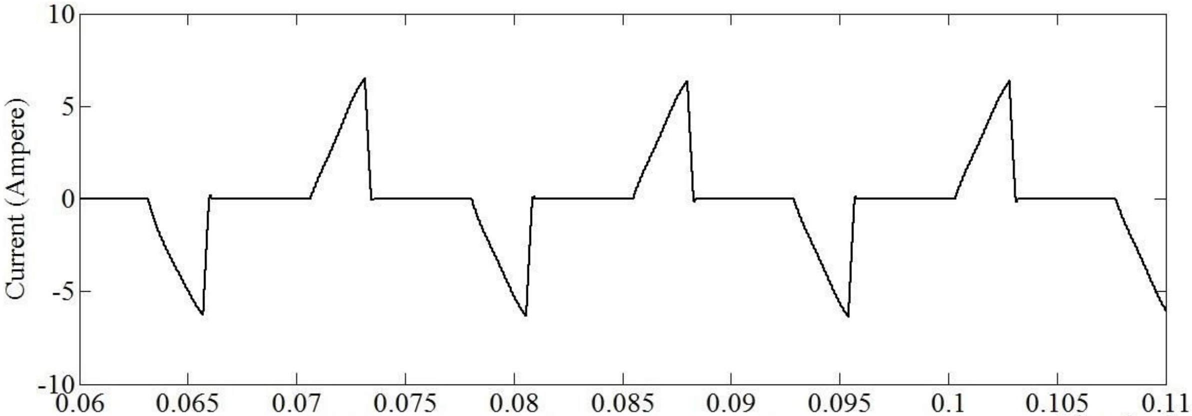


Fig.17 (i) Current profile of phase A after back emf compenstion

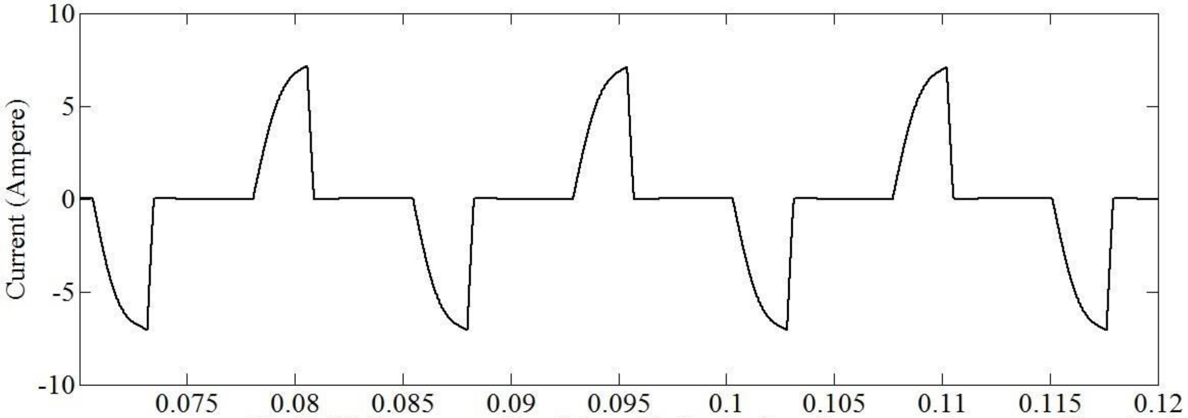


Fig 17 (ii) Current profile of phase B after back emf compensation

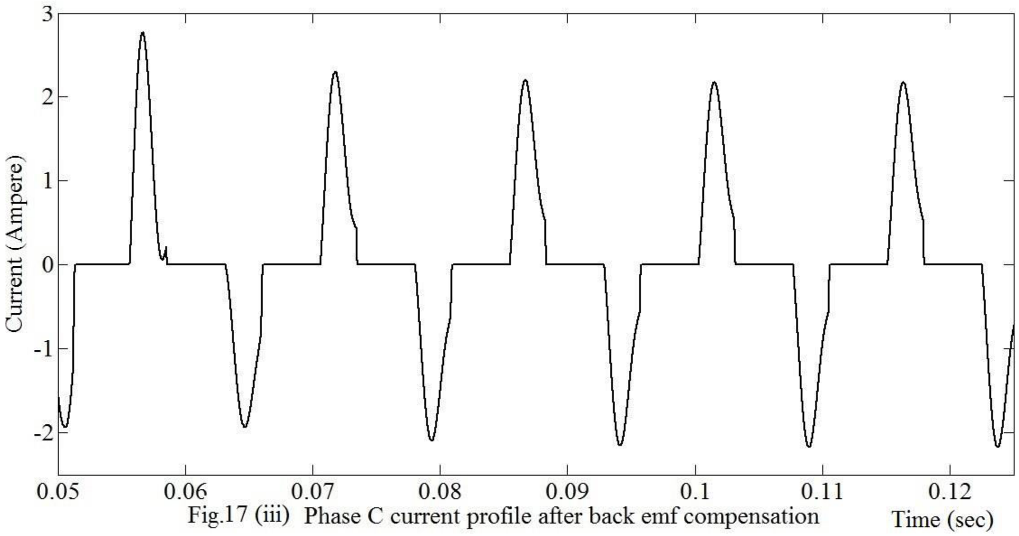


Fig.17 (iii) Phase C current profile after back emf compensation

CHAPTER-6

PROPOSED BUCK CONVERTER FED FSTPI BASED BLDC MOTOR DRIVE

6.1 INTRODUCTION

As discussed earlier, for the effective speed control of a FSTPI based BLDC motor the input supply voltage must be modulated using a buck converter. This is a necessity so that the motor operates at rated voltage during all the six modes of operation. Therefore the proposed model introduces a buck converter at the input supply voltage end of a conventional FSTPI based BLDC motor drive in the form of switches S5 and S6 as shown in figure 18.Arrangement has also been made in the form of batteries B1 and B2 for storing the dissipative energy during freewheeling period of the PWM pulse [2]. Different parts of the proposed model have been discussed in detail under the following heads.

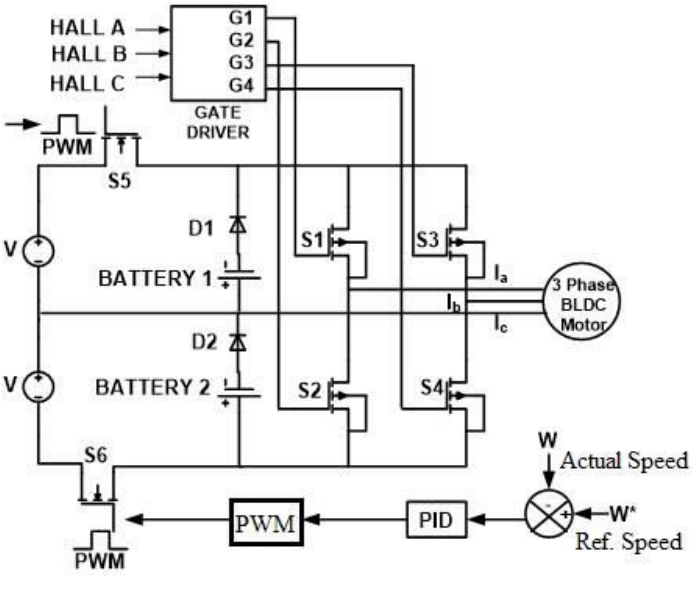


Fig. 18: Proposed Buck converter fed FSTPI based BLDC motor drive

6.2 SCHEMATIC FOR SPEED CONTROL

For the effective speed control of a Buck converter fed FSTPI based BLDC motor the schematic shown in figure 19 is developed.

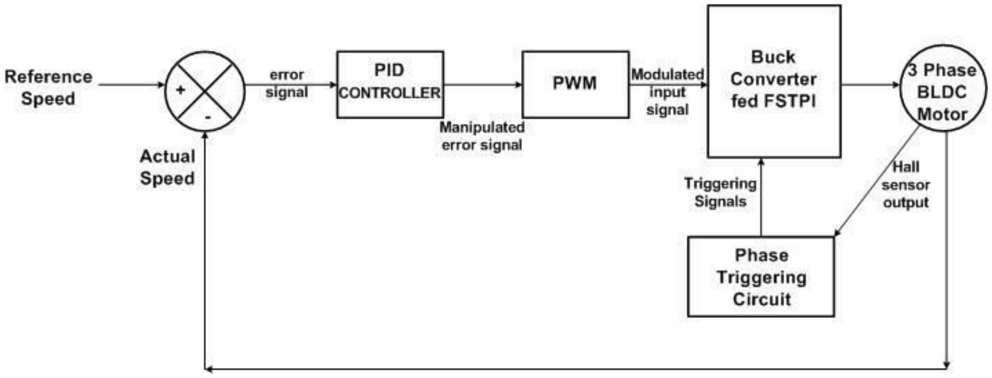


Fig. 19: Schematic for Speed Control of BLDC motor

6.2.1 SPEED ERROR BLOCK

In this block, the actual speed is compared with the set speed and the error generated is sent to the PID controller for appropriate conditioning.

6.2.2 PID CONTROLLER BLOCK

The aim of the PID Controller is to amplify the speed error [5]. The proportional gain (K_P) is set for quick response, whereas, the Integral gain (K_I) is used to reduce the speed error and the derivative gain (K_D) is used to reduce the overshoot and ripples in the speed response. The values set for these gains depend on the designer's judgement for achieving the best possible speed response [6]. The output of the PID controller is sent to the PWM block for generating the right amount of duty cycle for reducing speed error.

6.2.3 PWM BLOCK

Pulse Width Modulation technique is applied mainly to change the duty ratio of an input quantity in order to control the output quantity at desired level. That is,

$$V_O=\alpha * V_i \text{---------} (5)$$

where V_O : output voltage , V_i : Input Supply , α: Duty ratio; α may be defined as T_{on}/T; switching time period : $T= T_{on} +T_{off} =1/F_s$;F_s: switching frequency.

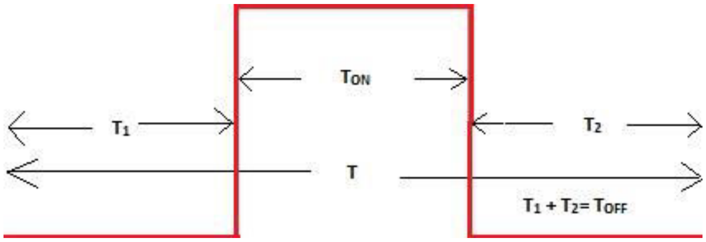


Fig. 20: One Time period of a PWM Pulse

6.3 CHANGE OF DUTY CYCLE

The output from the PID controller acts as the reference signal with which the triangular carrier wave is compared. That is, if the speed error is large (actual speed less than set speed), the reference signal generated has a low value. Thus the reference signal when compared with the triangular wave, generates a duty cycle of large size, thereby increasing the T_{on}; which results in an increased level of input supply voltage for reducing the speed error. The opposite occurs when the error is small.

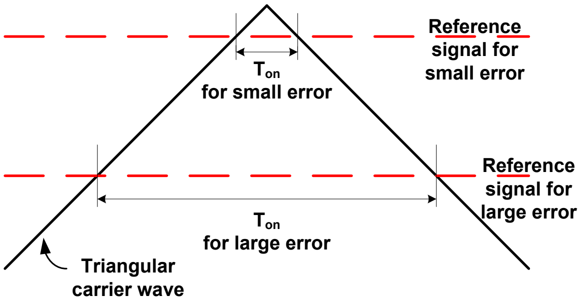


Fig. 21 : Duty cycle generation method for large and small errors

The PWM thus generated is sent to the Buck converter switches (S5 and S6) to modulate the D.C link voltage for reducing speed error.

6.4 GATE DRIVER BLOCK

In this block switching functions are generated in order to provide gate pulse to the switches in the Four Switch Inverter for generating the three phase AC supply for the BLDC motor. The switches are turned on and off as required during various modes for proper commutation of the three phase currents. As discussed earlier, analysis of the BLDC motor voltage and current profile shows that any one time only two phases of a BLDC motor are active; whereas the third phase is inactive [1]. Thus at such instances a three phase BLDC motor is converted into two phase. Figure 10 and table 2 give a pictorial description of the above paragraph. Thus based on figures 10, 16 and table 3 switching pattern of the inverter switches is developed as follows.

Table 5: Switching Pattern of Inverter switches

Mode	HALL SENSORS			Active Phases	Silent Phase	SWITCHING DEVICES
	h_a	h_b	h_c			
1 (0°<Ø<30°)	0	0	1	C,B	A	S_4
5 (30°<Ø<90°)	0	1	0	A,B	C	S_2 & S_3
6 (90°<Ø<150°)	0	1	1	A,C	B	S_2
3(150°<Ø<210°)	1	0	0	B,C	A	S_1
2(210°<Ø<270°)	1	0	1	B,A	C	S_1 & S_4
4(270°<Ø<330°)	1	1	0	C,A	B	S_3

From the table 5 it is clear that the rotor position can be easily sensed using hall position sensor output. Thus based on hall sensor output the following switching functions [3] for the two leg inverter switches may be generated for proper current commutation using electronic circuits.

$$S1= h_a * h_{\bar{b}} \quad ; \quad S2= h_{\bar{a}} * h_b \quad ; \quad S3= h_b * h_{\bar{c}} \quad ; \quad S4= h_{\bar{b}} * h_c \text{------} \ (6)$$

($h_{\bar{x}}$ represents complemented form of a hall position sensor output)

6.5 LOCATION OF BUCK CONVERTER SWITCHES IN THE PROPOSED DRIVE

As evident from the proposed model in Fig.18, since there happen to be two voltage sources in the proposed drive, therefore in order to mimic a conventional buck converter fed six switch inverter based BLDC motor drive [2] where only one voltage source is present we have to provide two switches; one for each voltage source. Moreover during modes 1, 3, 4, 6 (figure 12) the two voltage sources are involved in the current loop one at a time. Thus placing a switch along any one of the voltage sources would not be helpful when that source is not utilized and the other source (without having a switch) is in operation. Thus the need for two separate switches for the two voltage sources is justified. Now, it can be assumed that both the switches should be placed along the positive polarity of the two source voltages just like the conventional model, but analysis of Modes 1,3,4,6 (figure 12) shows that the switch which has to be connected along phase C has to face bidirectional current. This rules out the possibility of using unidirectional switches like BJT, IGBT, GTO, Thyristor along phase C. Thus the only remaining switch in such case is a MOSFET. However use of MOSFET along phase C shows that although it can handle bidirectional current it gives rise to back emf problem. This is mainly because the parasitic diode inside the MOSFET switch S6 along phase C provides a short circuit path for the unnecessary flow of phase C current during Modes 2,5 which is undesirable as the phase C current during such modes should have been zero (Fig. 22).

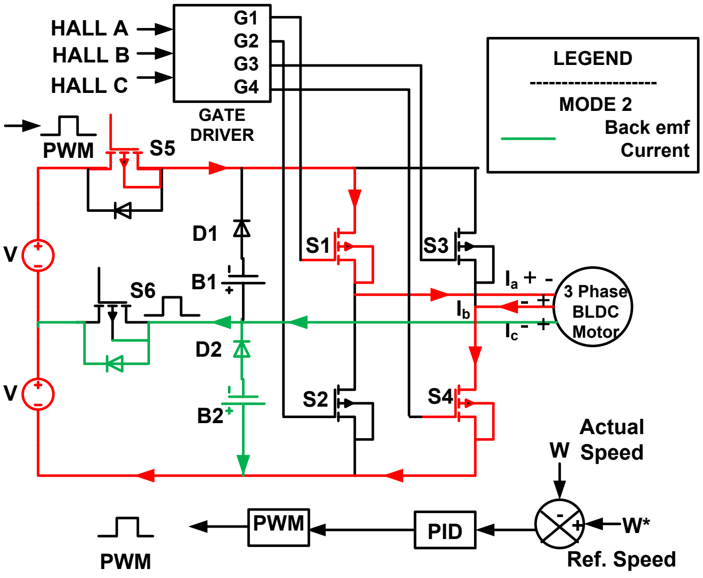


Fig. 22 : Back emf problem with MOSFET switch along phase C

This gives re-emergence of back emf problem (Fig. 23). Therefore the only solution to such problem is to remove the MOSFET switch S6 along phase C and place it along the negative terminal of the lower supply voltage (Fig.18). However with the removal of a controlling switch along phase C, the said phase would once again become uncontrollable, once again leading to the flow of undesired current in phase C. Therefore the following strategy is devised for removing the back emf problem altogether.

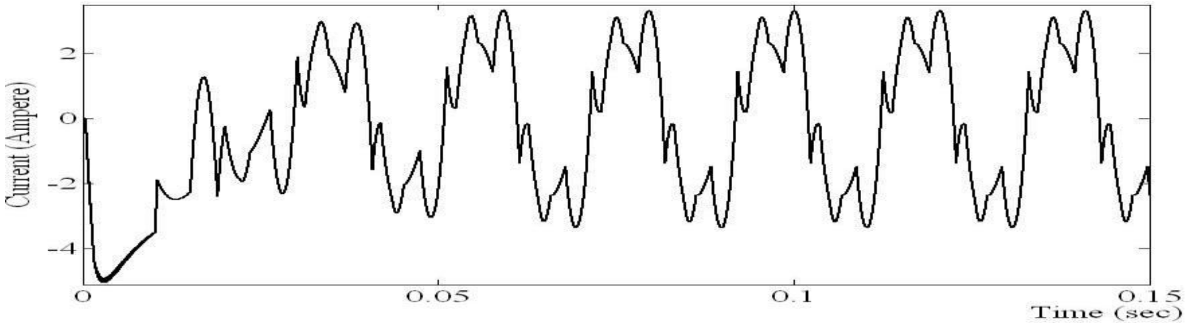


Fig. 23 : Current profile of Phase C with MOSFET along it

6.6 TECHNIQUE FOR COMPENSATING FOR BACK EMF PROBLEM

The proposed drive (Fig. 18) shows that along with the freewheeling diode an arrangement has been made in the form of two batteries for storing the dissipative energy during the off period of the PWM pulse. Detailed analysis shows that during modes 2, 5 phase C back emf develops a polarity as shown in Fig.24 in order to supply the undesired current from C to neutral point N. Because of such polarity diode D2 turns on, thereby putting the battery B2 in the circuit (battery B2, diode 2, phase C, phase B, switch S4/S3). As a result battery 2 voltage opposes the phase C back emf, and thereby prevents any undesired flow of current.

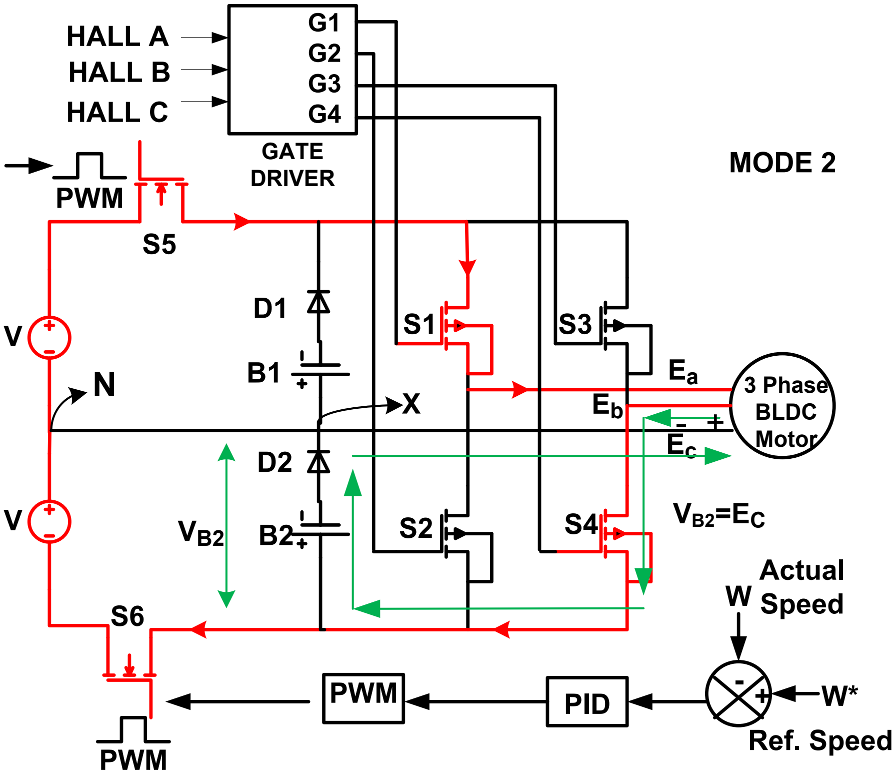


Fig.24 Schematic of battery 2 voltage opposing phase C back emf

During modes 3, 4 when legitimate current has to flow from C to N, the battery 2 voltage does not oppose the phase current I_C, because switches S3, S4 remain open during the respective modes, as a result battery B2 never forms part of a closed loop circuit. Also, during other modes (1, 6), the diode D2 is turned off (because of phase C polarity) so that battery 2 is again isolated. Moreover, since the switch (S6) connected between the lower supply voltage and the battery B2 is unidirectional, as will be seen later (section 6.10), so its orientation allows current to flow only towards the negative end of the lower supply voltage and not from it, thereby ensuring that no closed circuit is formed through the lower supply voltage, S6, battery B2, diode 2 and back.

6.7 CHOICE OF SWITCHES FOR BUCK CONVERTER

As described in section 6.5 the switches of the buck converter has to be placed along the positive terminal of upper source voltage and negative terminal of lower source voltage (Fig. 18). However, close analysis shows that even such placement of switches leads to current distortion (Fig. 26).

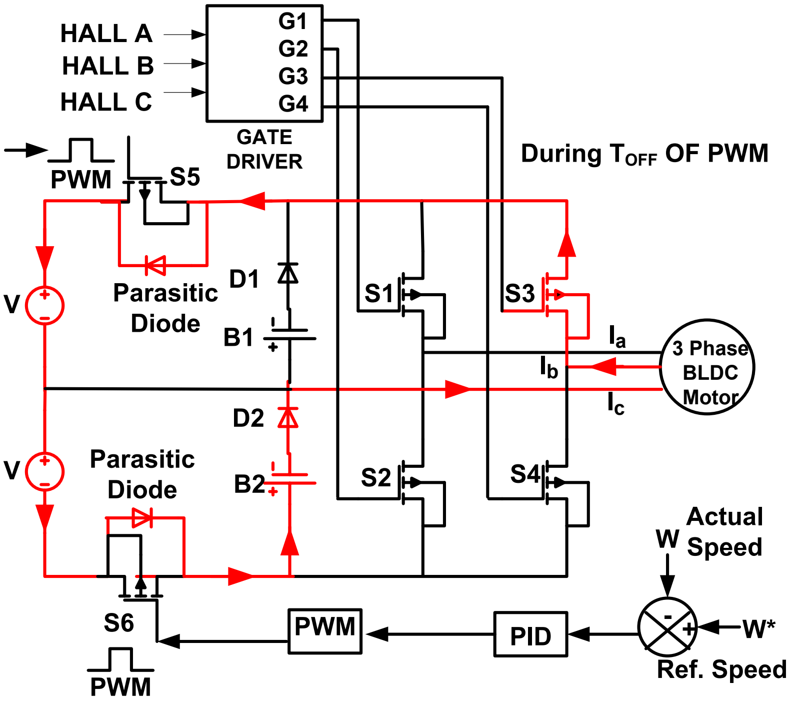


Fig. 25 : Schematic showing undesirable current flow through parasitic diode

This is because since the MOSFET switches have parasitic diode, therefore unwanted current may flow from the source voltages through the parasitic diode of MOSFET switch S6, battery B2, diode D2, phase C winding , phase B winding and then back through the freewheeling diode of switch S3 and parasitic diode of MOSFET switch S5 (Fig.25) during the turn off peiod of the pwm pulse (as the phase inductances change polarity during the turn off peiod of the pwm pulse; diodes D1 and D2 are turned on thereby completing a closed circuit). This again leads to waveform distortion. Therefore the need arises for eliminating such parasitic diode.

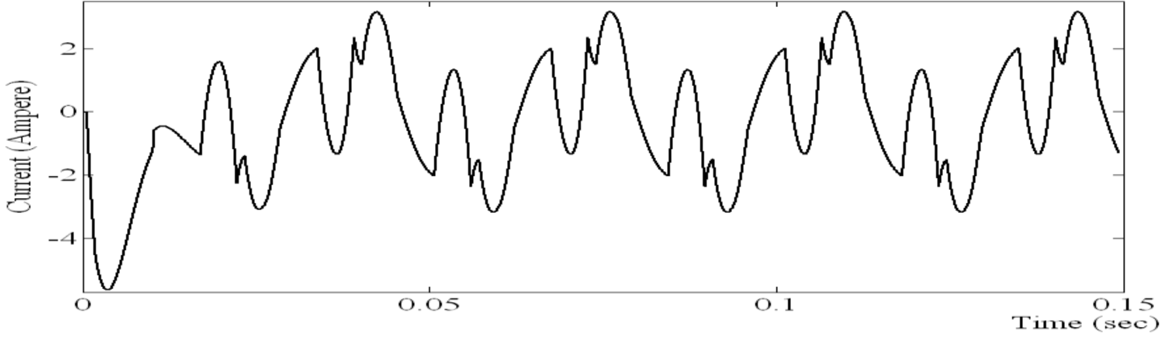


Fig. 26 : Current profile of Phase C with MOSFET switches in Buck converter

Moreover close observation of the six modes of operation (Fig. 12), shows that the current along the positive end of the upper source voltage and that along the negative end of the lower source voltage is always unidirectional. Thus a solution emerges where the MOSFET switches of the buck converter can be replaced with unidirectional switches. Since the switches employed in the buck converter are PWM controlled, hence high frequency switching occurs, so the switches used in the buck converter should have relatively low switching losses. Therefore the ideal switch for performing the above mentioned operations is, IGBT.

Thus all sources of back emf and undesirable current flow is eliminated by properly selecting and locating switches and batteries as discussed above. The simulation performance of the proposed drive leads to satisfactory results and is depicted in Chapter 8.

CHAPTER-7

SCOPE OF ENERGY RECOVERY

7.1 INTRODUCTION

As discussed in the earlier section (section 6.6), the battery used in the proposed drive plays the crucial role of tackling the back emf problem. However, it can also play an advantageous role by storing the dissipate energy during the freewheeling period. Following discussion depicts the manner in which batteries save energy during the turnoff period of the PWM pulse.

Energy saving capability of battery is discussed by undertaking case study of two modes-2 and 3 during the turn off period of the PWM pulse. Energy saving mechanism during other modes are similar that of the above modes.

7.2 MODE-2; PWM PULSE OFF

As is evident from table 3, during mode-2 switches S1 and S4 are on. During the on period of the PWM pulse buck converter switches S5 and s6 are on, thereby allowing the source voltages to supply the current for phase A and B through switches S1 and S4. As the PWM off pulse arrives, the switches S5 and S6 turn off, however the phases A and B of the BLDC motor being inductive in nature tend to sustain the earlier direction of current through them (fig.12; Mode-2). For this, these phases reverse their polarity, thereby turning on diodes D1 and D2. As a result current is sustained through these phases following the closed loop path of B1-D1-S1-phase A- phase B-S4- B2-D2 (fig 27). Thus charging of batteries B1, B2 happens during the PWM off pulse due to the flow of freewheeling current through them.

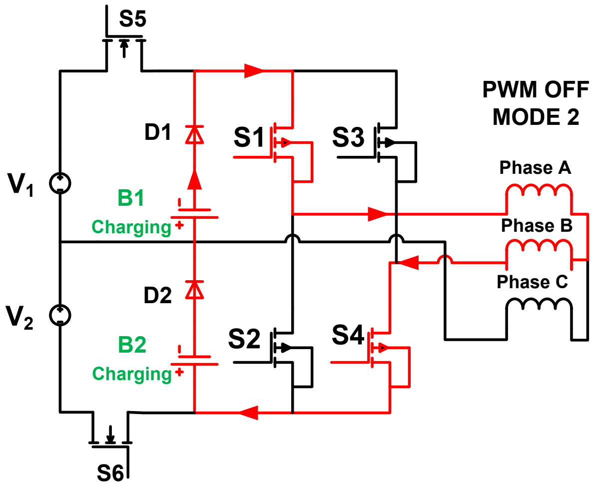


Fig. 27 : Energy recovery mechanism during mode2; PWM-off

7.3 MODE-3;PWM PULSE-OFF

Similarly during mode 3, current during the PWM on period is through switch S1, phase A, phase C and back to the source. As the switch S5 turns off during the PWM off period, the polarity of phases A and C reverses, thereby turning on the diode D1. As a result direction of current is sustained through S1-phase A-phase C-B1-D1.This freewheeling current through the battery B1 charges it up and thus helps recover the energy which could have been dissipated (fig. 28).

Energy recovered through these batteries, as described above, could then be used for feeding other auxiliary loads thereby increasing the overall efficiency of the system.

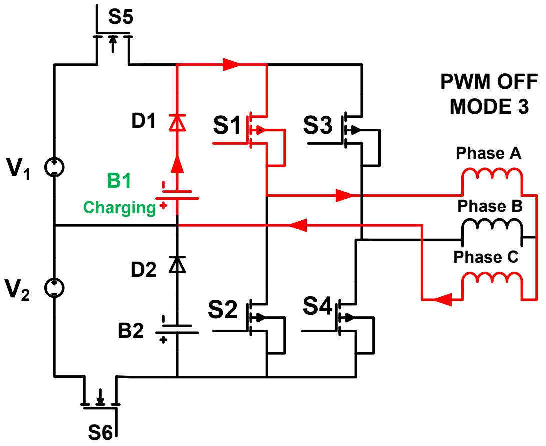


Fig. 28 : Energy recovery mechanism during mode3; PWM-off

7.4 UTILISATION OF RECOVERED ENERGY

From the point of view of practical application, say an electric car, the dissipative energy stored in the batteries B1 and B2 can be utilised to charge up the input side rechargeable batteries during the off line period of the motor (that is, when the motor is out of operation).

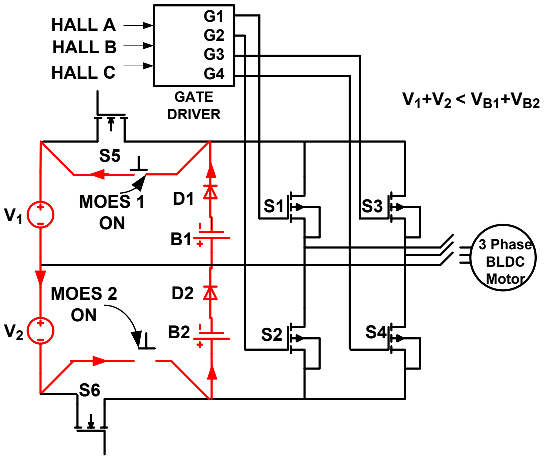


Fig. 29 :Arrangement for utilising recovered energy during the offline mode of BLDC motor

For this an arrangement has to be made such that when the motor is unexcited, mechanically controlled electric switch (MOES) is turned on thereby feeding power from the batteries B1 and B2 to the input side rechargeable batteries (figure 29).As a result the input side rechargeable batteries get replenished with fresh charge for the next cycle of operation. MOES 1 and MOES 2 are turned on when the motor is disconnected from the three phase supply. If the input side voltages, V1 and V2 combined, is less than the battery voltages VB1 and VB2 then the diodes D1 and D2 turn on thereby charging up the input side rechargeable batteries. The moment input side voltages V1 and V2 becomes equal to or slightly more than the battery voltages VB1 and VB2, diodes D1 and D2 turn off thereby preventing any unnecessary discharge of the input side rechargeable batteries during the offline operation of the motor.

CHAPTER-8

SIMULATION RESULTS

The developed topology was simulated on the Matlab / Simulink platform and satisfactory results were obtained which have been depicted in the following figures. The values assigned to the various parameters used in the proposed drive for simulation have been depicted in the table 6 and 7.

Table 6 : BLDC Motor Parameters

Stator Phase resistance (ohm)	2.8750
Stator Phase Inductance (Henry)	8.5*10^-3
Flux linkage	0.175
K_v (Voltage constant)	146.6077
K_t (Torque constant)	1.4
Inertia (J/Kg*m^2)	0.8*10^-3
Friction Factor (N*m*s)	10^-3
Pole Pairs	4

Table 7 : Details of other parameters used in the drive

Supply Voltage	60V each
Reference Speed	300 rpm
Torque applied	2 N-m
K_P	5
K_I	1
K_D	10
Battery voltage	60 V (each)
Battery Type	Lithium Ion

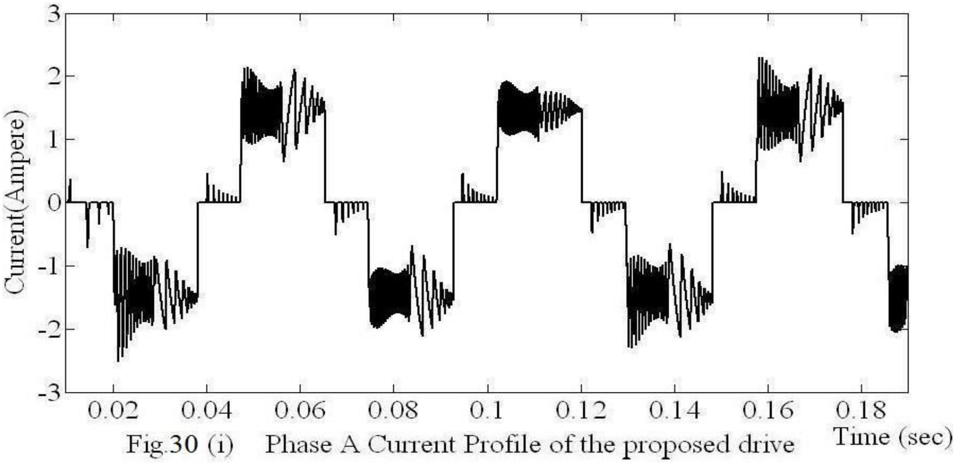


Fig.30 (i) Phase A Current Profile of the proposed drive

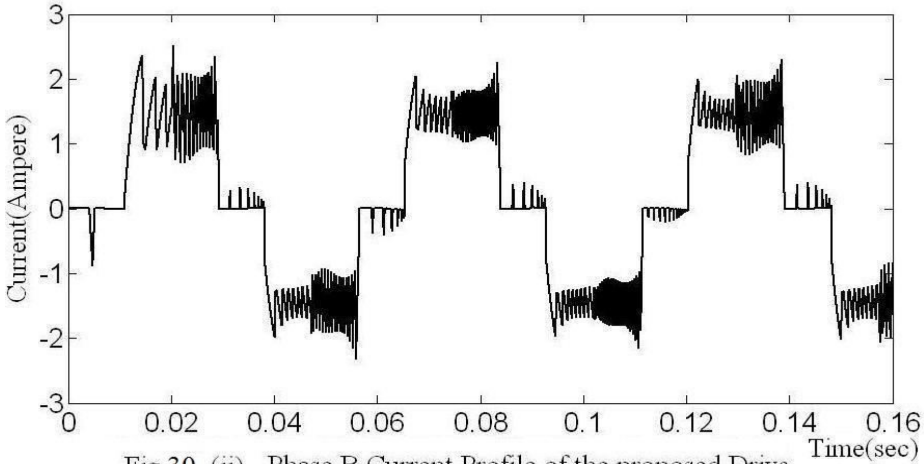


Fig.30 (ii) Phase B Current Profile of the proposed Drive

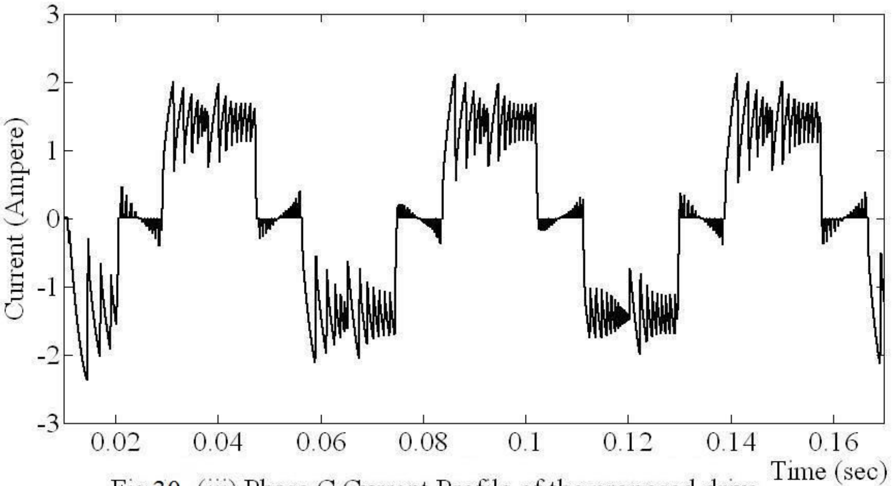


Fig.30 (iii) Phase C Current Profile of the proposed drive

The figures shown above [Fig. 30 (i) ; Fig. 30 (ii) ; Fig. 30 (iii)] represent the phase currents of the BLDC motor run using the proposed drive system. As evident from the figures; the phase current waveforms are very close to the ideal quasi – square shape of a typical BLDC motor's current wave form and also the current wave form of Phase C has finally stabilized at zero level [Fig. 30 (iii)], thereby preventing any damage to the system. Hence these results are considered satisfactory.

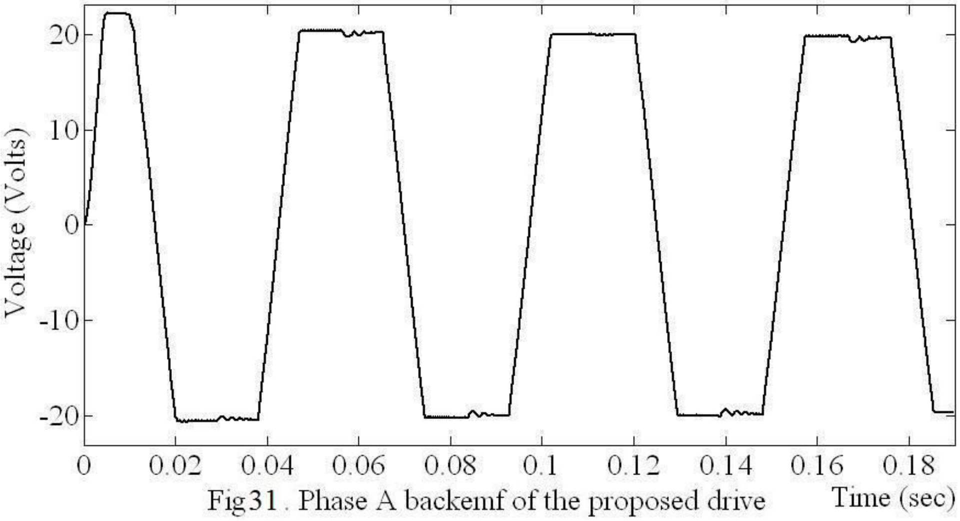


Fig31 . Phase A backemf of the proposed drive

The back emf waveform of phase A of the BLDC motor run using the proposed drive system, depicted in Fig. 31, is of ideal trapezoidal nature and therefore this result is acceptable.

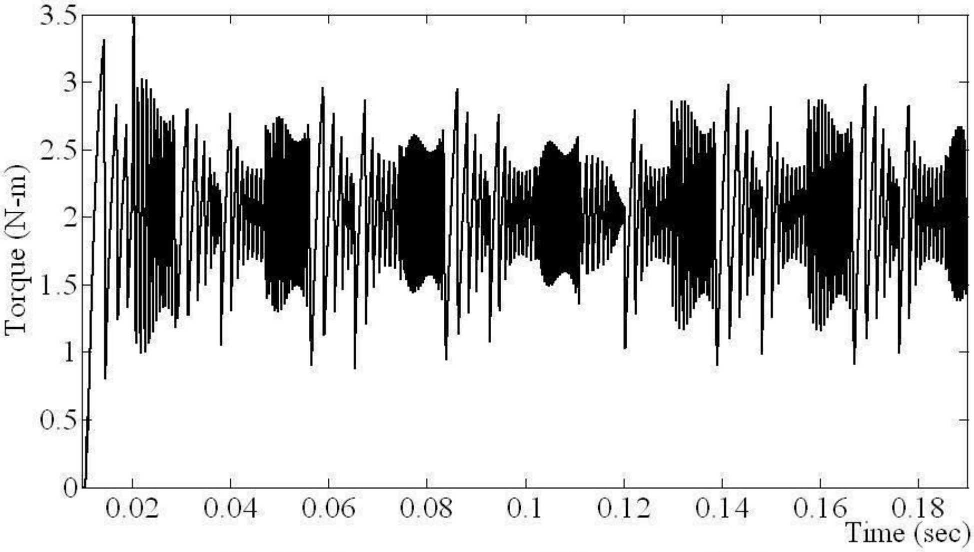


Fig.32 Torque response of the proposed drive

The torque response of the overall proposed drive system depicted in figure 32, shows that the torque always remains finite, positive and continuous, all of which are characteristics of ideal torque response of a typical BLDC motor. Moreover from the figure it is seen that the torque revolves around 2 N-m, which is the applied torque to the overall system. Hence the torque response seems satisfactory and acceptable.

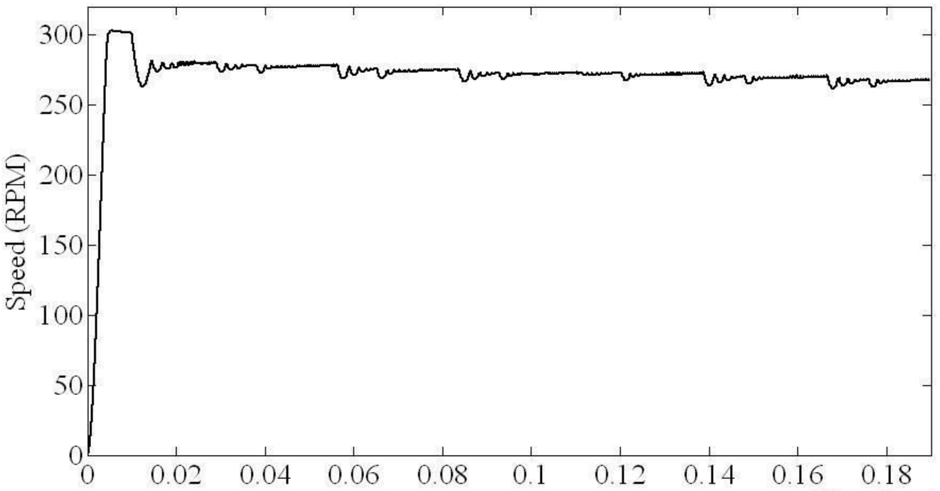


Fig.33 Speed response of the proposed drive

From the speed response of the proposed drive system depicted in figure 33 it is observed that the speed quickly rises till the desired speed limit of 300 r.p.m and then finally stabilises around 250 r.p.m. Since the drop in speed is within reasonable limit; therefore the speed response can be considered acceptable.

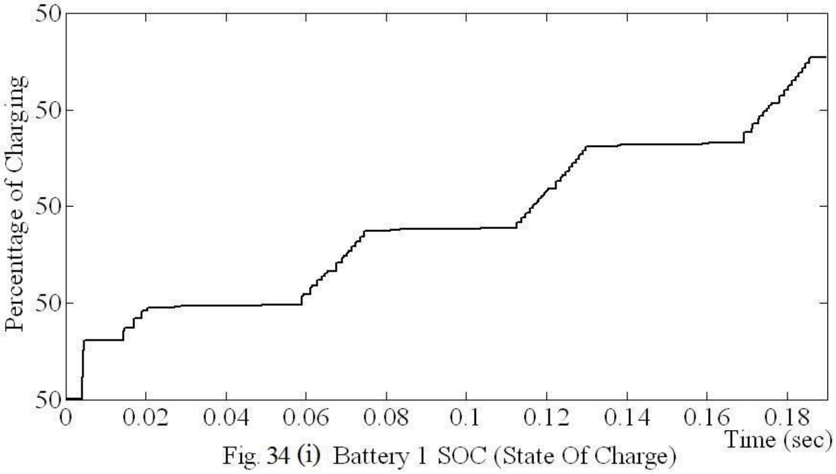


Fig. 34 (i) Battery 1 SOC (State Of Charge)

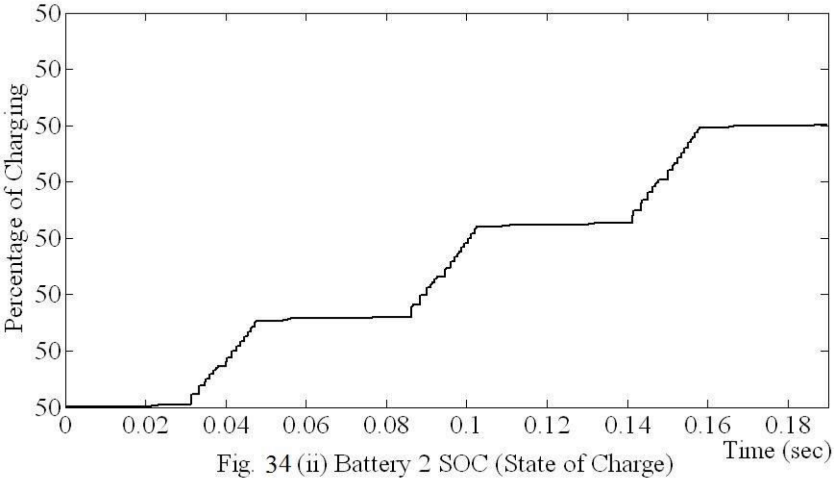


Fig. 34 (ii) Battery 2 SOC (State of Charge)

The above figures [Fig. 34 (i) and Fig. 34 (ii)] represent the state of charge of the rechargeable batteries. Initially the batteries are kept charged till 50% in order to depict any real life situation. As the drive system starts running, it is observed that the batteries start charging in a staircase manner. This nature of the charging validates the theory of energy saving during off period of the PWM pulse. This is because, during the on period of the PWM pulse battery’s state of charge is held constant whereas, the moment off period of PWM pulse arrives both the batteries start charging linearly. This cycle repeats itself as evident from the above figures.

Hence based on the above results it is concluded that the proposed drive system performs satisfactorily and achieves the target of speed control and energy saving during off period of PWM pulse after tacking the issue of *‘asymmetric voltage pwm*’ using a novel technique for back emf compensation.

CHAPTER-9

DISCUSSION & CONCLUSION

After analysing the performance of the proposed drive system from the simulation results one can safely conclude that even though it contains more current ripple than the six-switch converter based drive, the results are acceptable and satisfactory. Thus in this paper a successful attempt has been made to extend the buck converter topology of a conventional six switch inverter based BLDC motor drive [2] to a low cost Four switch inverter based BLDC motor drive. While doing so number of benefits has been achieved, as discussed below:

(1) The requirement of current controlled PWM in a conventional FSTPI based BLDC motor drive has been done away with, without reintroducing the back emf problem. This has eliminated the need for current sensors [4] used in conventional FSTPI based BLDC motor drive, leading to reduction in cost and complexity.

(2) In the current controlled PWM FSTPI based BLDC motor drive the input supply voltage was uncontrolled. As a result except for modes 2,5 every other mode had to run at half the rated supply voltage, this was because if the rated voltage had been applied during modes 1,3,4,6 then during modes 2,5 the two voltages (upper and lower) would have serially added up and exceeded the rated voltage of the motor, thereby seriously damaging it. Thus in the conventional FSTPI based BLDC motor drive speed control was inherently difficult. This problem has been solved [7] in the proposed drive where the input supply is controlled through the buck converter switches because of which rated voltage may be applied during modes 1,3,4,6 and during modes 2, 5 when the supply voltages serially add up to get doubled the PWM duty cycle is set such that the doubled up voltage at the input is steeped down to rated value. In this way the motor can be run at rated voltage during all modes, unlike earlier, resulting in better speed response (figure 33).

(3) The proposed drive system also has storage elements in the form of batteries which store the dissipative energy during the turn off period of the PWM pulse, leading to a more energy efficient system, unlike the conventional current controlled PWM technique of driving FSTPI based BLDC motor.

(4) Low frequency switching occurs in the four switch inverter as the gating of the inverter switches does not happen from current controlled PWM, thereby reducing switching losses.

(5) As compared to the conventional buck converter fed six switch inverter based BLDC motor drive [2], the proposed system despite requiring two additional voltage sources and batteries has successfully reduced the number of switches in the inverter from 6 to 4, leading to an overall reduction in the number of switches from 7 (buck converter fed six switch inverter based BLDC motor drive) to 6 (proposed drive).

CHAPTER-10

FUTURE SCOPE

The proposed model has been found to behave satisfactorily based on simulation results. However its hardware implementation is necessary in order to ascertain its practical viability.

From the above simulation results one can easily note that the system performance with regards to speed response is still quite stiff and therefore appropriate mechanisms should be developed in the drive system for smoother speed control.

Moreover it is also noted that the current response of the three phases contains a lot of noise which needs to be suppressed further. Therefore appropriate noise reduction technique needs to be employed for better phase current profile.

It is also noted that future work may include the study of financial feasibility of the proposed drive system with regards to introduction of two additional battery and its contribution to overall system efficiency by storing the dissipative energy of the freewheeling period of the PWM pulse

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