PHASE LOCKED LOOP (PLL)

A PLL is a feedback system where an oscillator-generated signal is phase and frequency locked to a reference signal. The use of this loop is in comparing frequencies of two waveforms and then adjusting the frequency of the waveform in the loop to equal the input waveform frequency.
PLL Fundamentals
The heart of the PLL is a phase comparator which along with a voltage controlled oscillator (VCO), a filter and an amplifier. All parts are connected to form a closed loop frequency feedback system.

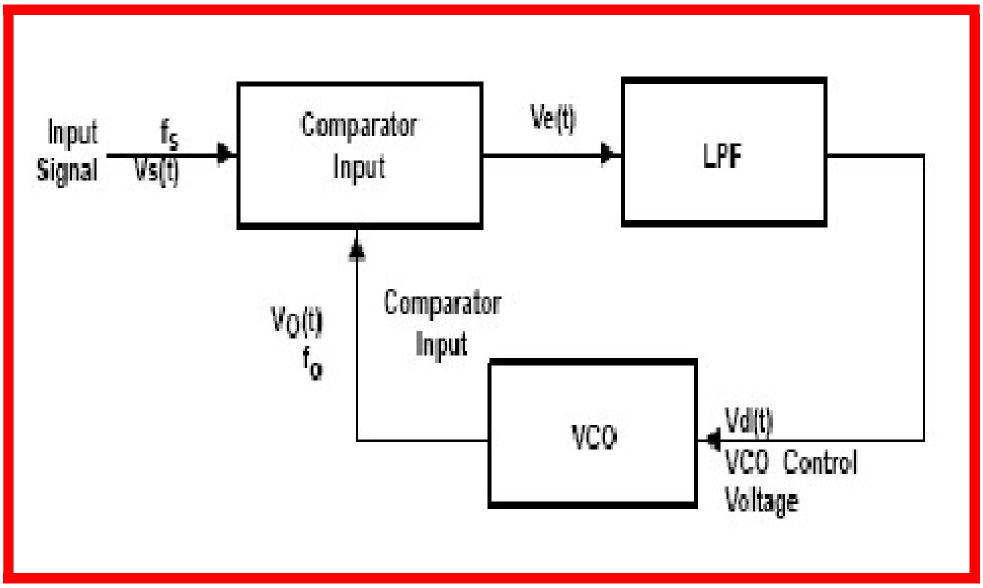


Fig. Block diagram of PLL

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, $V_d(t)$, from the LPF also is zero, which causes the VCO to operate at a set frequency, f_o, called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency difference of the input signal and the VCO. The error voltage, $V_e(t)$, is filtered and applied to the control input of the VCO. $V_d(t)$ varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to lock in frequency with the signal input; i.e., when the PLL is in lock, the VCO frequency is identical to the signal input, except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the lock range of the system. The lock range always is larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the capture range of the PLL system.

1. **Multiplier as Phase Detector**

A phase detector is simple multiplier. A gain value is associated with it.
The output of the multiplier is made up of two periodic waveforms—one has the frequency of the difference of the frequencies of the two input sinusoid and the other wave's frequency is their sum.
Let

$$V_s(t) = A\sin(\omega_i t)\ \ and\ V_o(t) = B\cos(\omega_o t)$$

The output $V_e(t)$ of the phase comparator is

$$V_e(t) = K_1 AB\sin(\omega_i t)\cos(\omega_o t)$$
$$= \frac{K_1 AB}{2}\ [\sin(\omega_i + \omega_o)t + \sin(\omega_i - \omega_o)t]$$

Where K_1 is the multiplier/phase detector gain.

2. **The Low Pass Filter/Loop Filter**

When $V_e(t)$ is passed through an ideal low pass filter, the sum frequency component is removed and the filter output becomes,

$$V_d(t) = \frac{K_2 AB}{2}\ \sin(\omega_i - \omega_o)t$$

Where K_2 is another constant.

3. **Voltage Controlled Oscillator**

The voltage-controlled oscillator (VCO) ideally generates a periodic signal with a frequency that linearly depends on the input (control) voltage $V_d(t)$. Grounded input drives the VCO to run at its free-running frequency ω_{FR}.
Assuming a linear gain of K_{VCO} (rad/s-V) for this block, output frequency is found to be:

$$\omega_o = \omega_{FR} + K_{VCO} V_d(t)$$

Where ω_o is the VCO output frequency, K_{VCO} is the VCO gain in rad/s-V). $V_d(t)$ drives the VCO. The VCO frequency ω_o is compared with the input frequency ω_i and adjusted until it is equal to the input frequency. When ω_o becomes ω_i with some phase difference the PLL is then in the Locked state.
When the loop reaches the locked condition

$\omega_i = \omega_o$, w.r.t. frequency

And $\omega_i t = \omega_o t + \emptyset$, w.r.t. phase

Where $\emptyset$ is the phase difference between input and output.

Then, the phase comparator output, under locked condition, becomes

$$V_e(t) = K_1 A \sin(\omega_i t) B \cos(\omega_i t - \emptyset)$$

$$= \frac{K_1 AB}{2}[\sin\emptyset + \sin(2\omega_i t - \emptyset]$$

The low pass filter output becomes

$$V_d(t) = \frac{K_2\ AB}{2}\sin\emptyset$$

It can be expressed as

$$V_d(t) = K_d F(0)\sin\emptyset$$

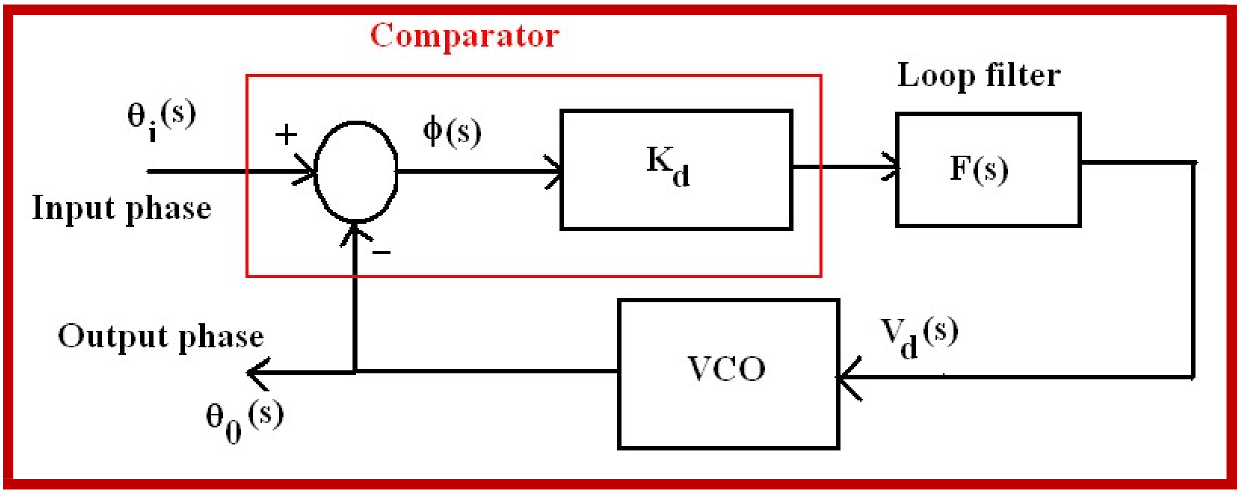
Where K_d is the phase comparator gain $(=\frac{K_1 AB}{2})$ in volts/sec and F(0) is the filter gain at zero frequency (D.C.) and

$$K_d F(0) = \frac{K_2\ AB}{2}$$

And for very small $\emptyset$, $\emptyset = \sin\emptyset$ and the above relation may be approximated as

$$V_d(t) \approx K_d F(0)\ \emptyset \quad \text{(for very small } \emptyset\text{)}$$

Linear Model For Locked PLL For Small $\emptyset$



From the VCO characteristics

$$\omega_0 = \omega_{FR} + K_{VCO} V_d(t)$$

Or

$$\omega_0 - \omega_{FR} = K_{VCO} V_d(t)$$

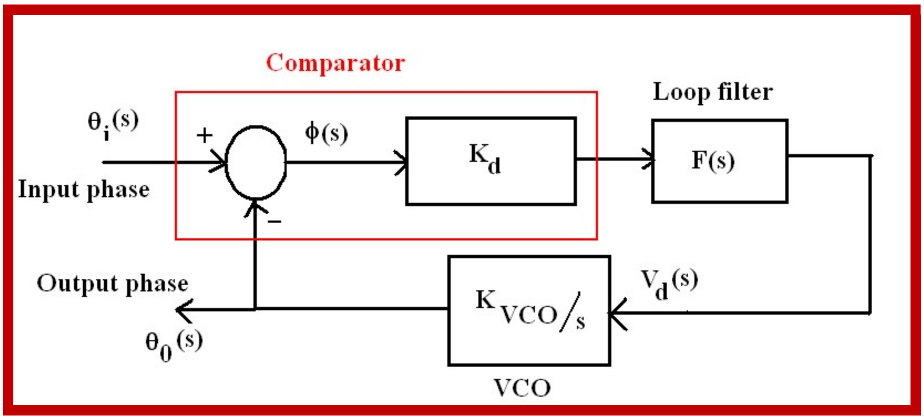
Assuming the center frequency as reference, the output phase is

$$\frac{d\theta_0(t)}{dt} = \omega_0 - \omega_{FR} = K_{VCO} V_d(t)$$

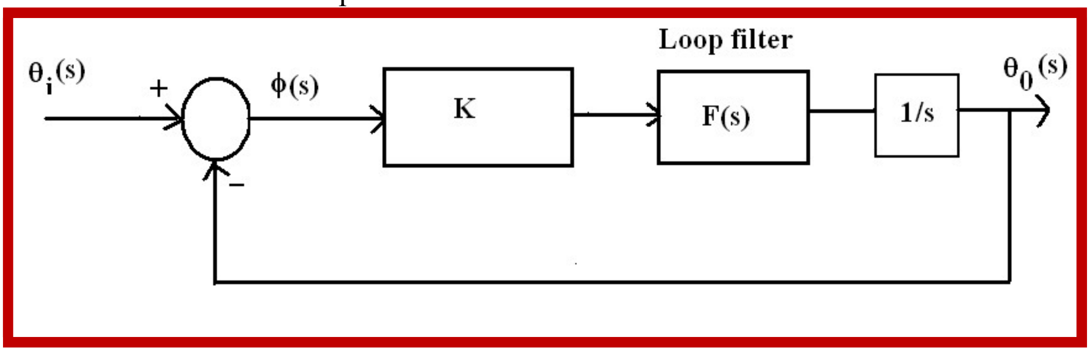
Taking the Laplace transform

$$s\theta_0(s) = K_{VCO} V_d(s) \text{ or } \frac{\theta_0(s)}{V_d(s)} = \frac{K_{VCO}}{s},$$

Thus the linear model becomes



The above model can be represented as



Where K = $K_d K_{VCO}$

The closed loop transfer function is

$$H(s) = \frac{\theta_0(s)}{\theta_i(s)} = \frac{KF(s)}{s + KF(s)}$$

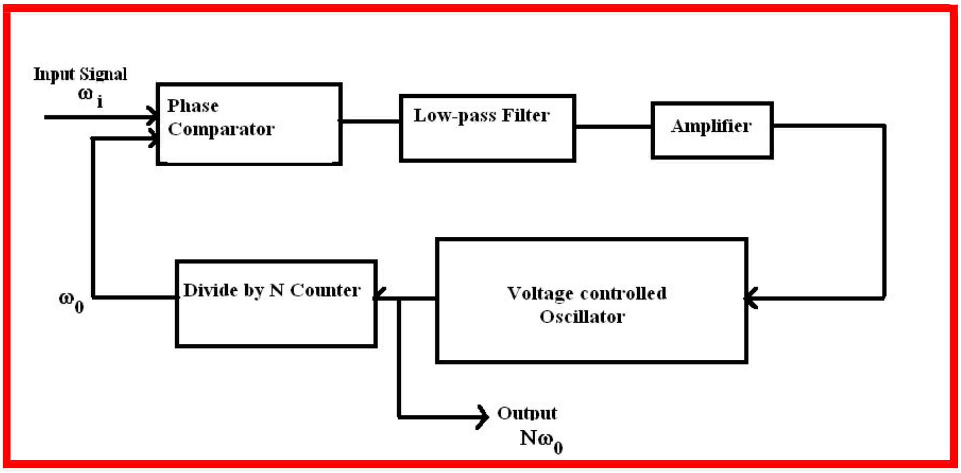
The Lock Range and Capture Range

Lock Range : The Lock range is the range of input signal frequencies considering both sides of the centre frequency of the VCO, for which the loop remains under locked condition once it has captured the input signal.

Capture Range : The capture range is the range of input signal frequencies, considering both sides of the centre frequency of the VCO, for which the loop will lock when starting from an unlocked condition.

Applications of Phase Locked Loop

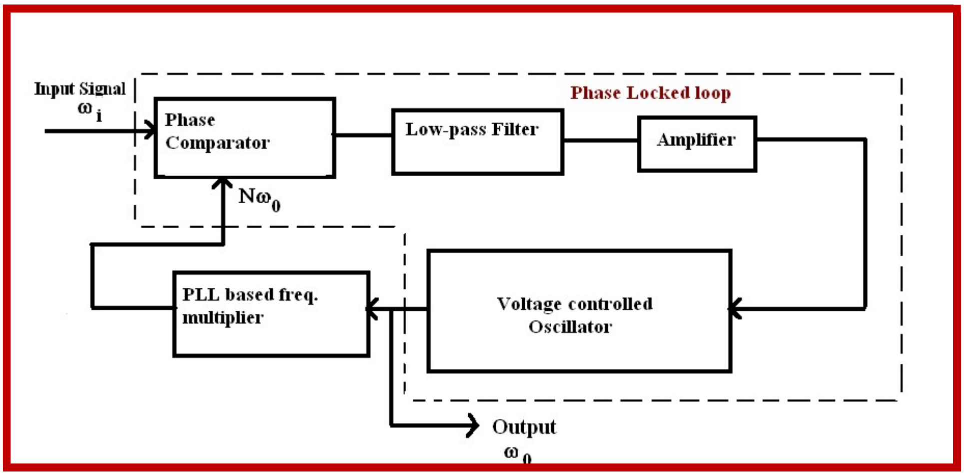
1. Frequency Multiplication



Under locked condition, $\omega_i = \omega_0$

Thus , output frequency = Nω_0 = Nω_i = N x input frequency

2. Frequency Division

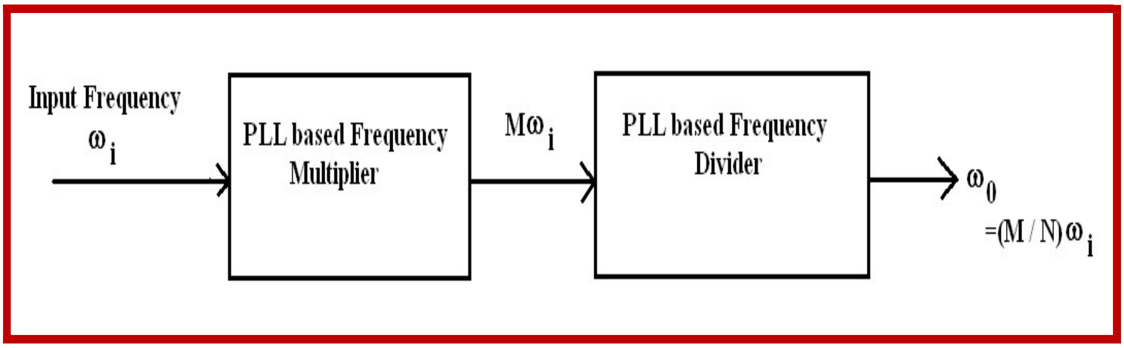


The division of input signal frequency can be made with the help of a PLL and PLL based frequency multiplier is connected in the feedback loop as shown in the diagram. The vco output signal frequency is multiplied and under locked condition, the output of the PLL based frequency multiplier will be equal to the input frequency.

Under locked condition,

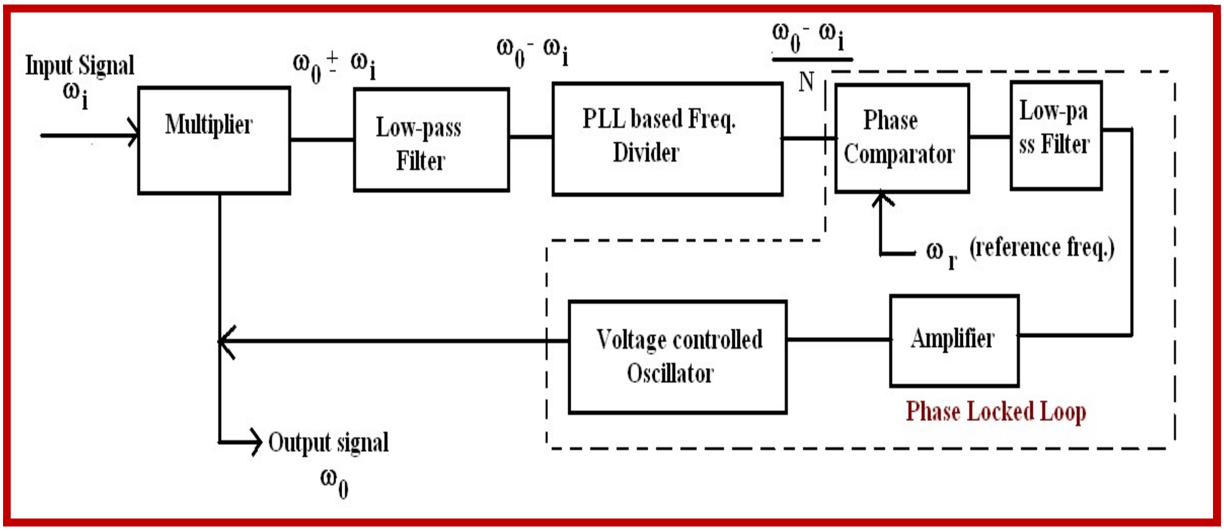
$$N\boldsymbol{\omega_0} = \boldsymbol{\omega_i} \quad \text{i.e.,} \quad \boldsymbol{\omega_0} = \frac{\boldsymbol{\omega_i}}{\boldsymbol{N}}$$

3. Fraction frequency multiplication



The limitation of the PLL based frequency multiplier lies in the fact that it cannot multiply the input signal frequency by a fractional number. Then a PLL based frequency multiplier and divider are cascaded in order obtain a fractional frequency. In the above diagram the 1st PLL will multiply the input signal frequency $\boldsymbol{\omega_i}$ by an integer M, so that the output will be M$\boldsymbol{\omega_i}$. The output of the 1st PLL is passed to the 2nd PLL, which will divide the frequency by N and will produce output frequency equal to (M/N) $\boldsymbol{\omega_i}$, where M < N.

4. PLL based Frequency Translator

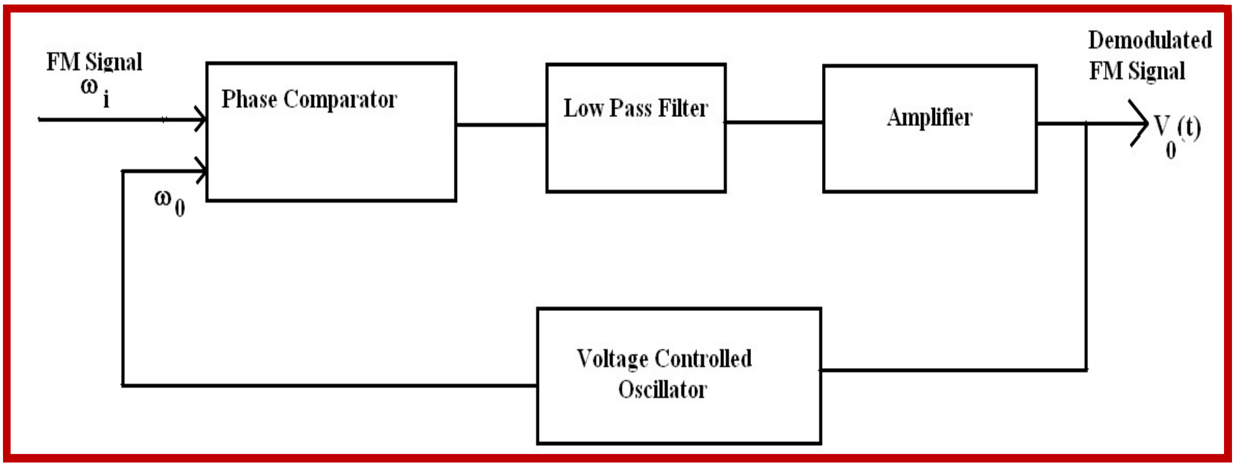


The frequency of the input signal can be shifted to a desired value by small amount. The input signal frequency ω_i is multiplied by VCO output signal frequency ω_0 by frequency multiplier. The output of the multiplier contains the sum and difference of the two frequencies as $(\omega_0 + \omega_i) and\ (\omega_0 - \omega_i)$. The output of the multiplier is then passed to low pass filter having cut-off frequency equal to $(\omega_0 - \omega_i)$. The output of the low pass filter is then passed to the PLL based frequency divider, which divides the frequency on its output by an integer N. The output of the divider is passed as one of the input to the phase comparator inside the PLL. The other input of the phase comparator is fed by a frequency ω_r, generated by an external oscillator. When the PLL is under locked condition

$$\frac{\omega_0 - \omega_i}{N} = \omega_r \text{ or, } \omega_0 = \omega_i + N\omega_r$$

i.e. output frequency = input frequency + N x reference frequency.

5. PLL as Frequency Demodulator



FM signal is fed to the one of the input of the phase comparator used as a frequency multiplier. The instantaneous frequency of the FM signal given by

$\omega_i(t) = \omega_c + kv_i(t)$, where $v_i(t)$ is the modulating signal and ω_c is the carrier frequency used for the frequency modulation and k is the constant in *radian-s^{-1}-volt^{-1}*. For VCO, the instantaneous output frequency can be expressed as

$$\omega_0 = \omega_{vco} + k_{vco}v_0(t)$$

Where ω_{vco} is the free running frequency and k_{vco} is the constant of the VCO.

Under locked condition

$$\omega_0 = \omega_i$$

Or

$$\omega_{vco} + k_{vco}v_0(t) = \omega_c + kv_i(t)$$

Or

$$v_0(t) = \frac{\omega_c - \omega_{vco} + kv_i(t)}{k_{vco}}$$

If the carrier frequency is made equal the free running frequency of the VCO, then

$$v_0(t) = \frac{kv_i(t)}{k_{vco}}$$

Thus the output of the amplifier will be proportional to the modulating signal and the output of the amplifier may be considered as the demodulated FM signal.