

DIGITAL SIGNAL PROCESSORS

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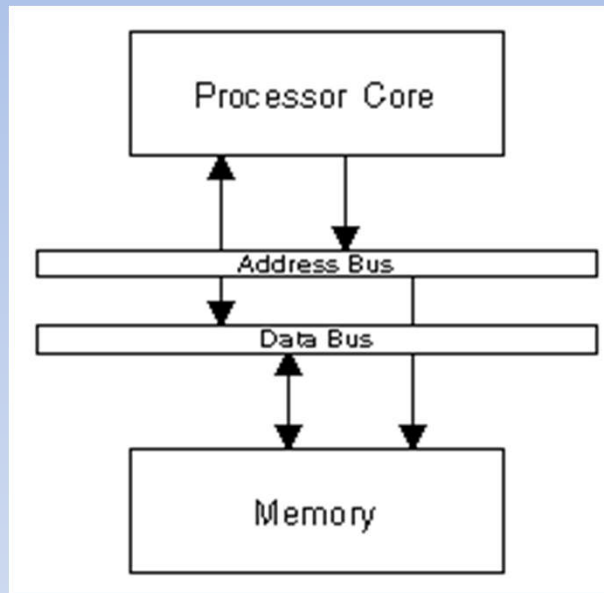
Processor Architecture

Categorized by memory organization

- Von Neumann architecture -> **Microprocessors**
 - Harvard architecture ->
 - Modified Harvard architecture ->
- } **Digital Signal Processors**

Processor Architecture

Categorized by memory organization



Program and Data
memory

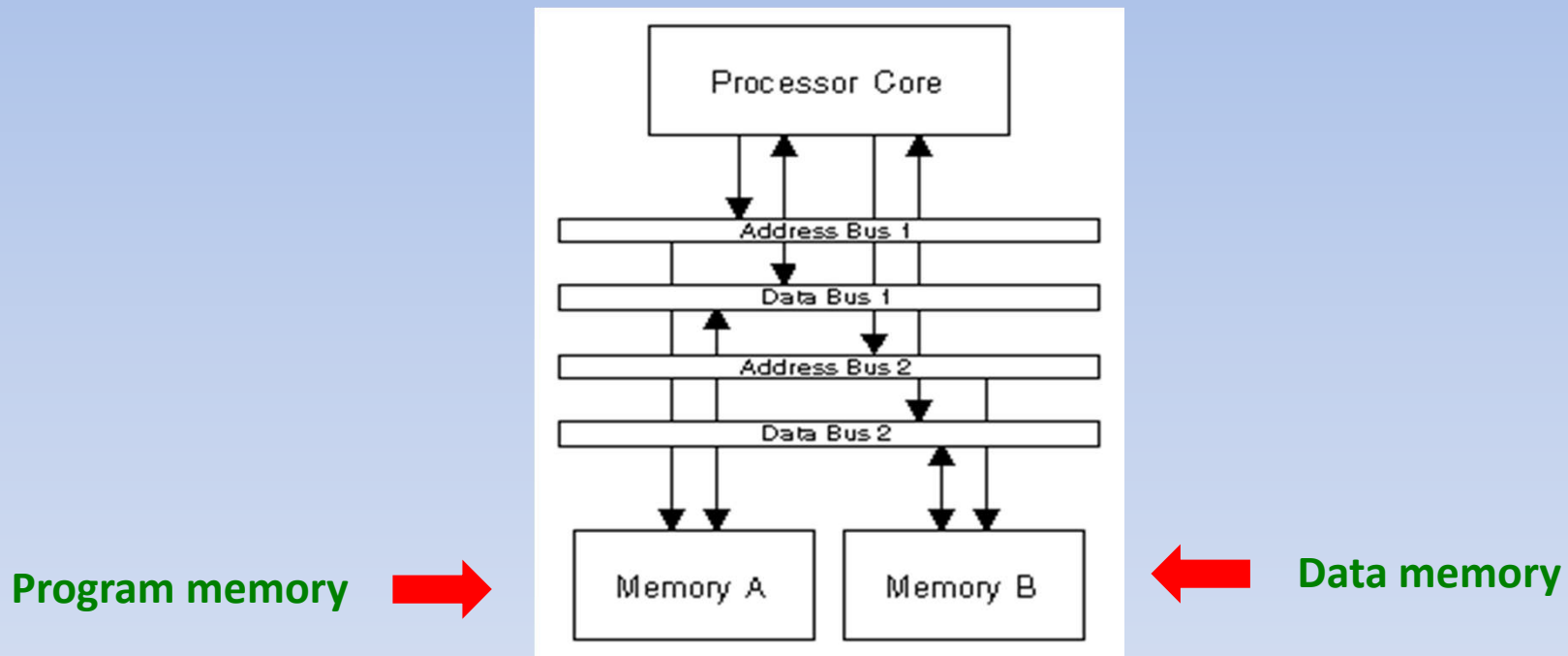


Von Neumann architecture

The Von Neumann architecture is a design model for a stored-program digital computer that uses a processing unit and a single separate storage structure to hold both instructions and data.

Processor Architecture

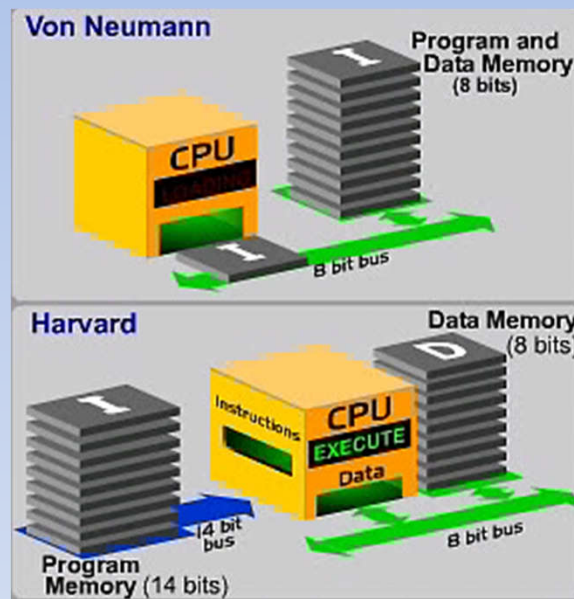
Categorized by memory organization



Harvard architecture

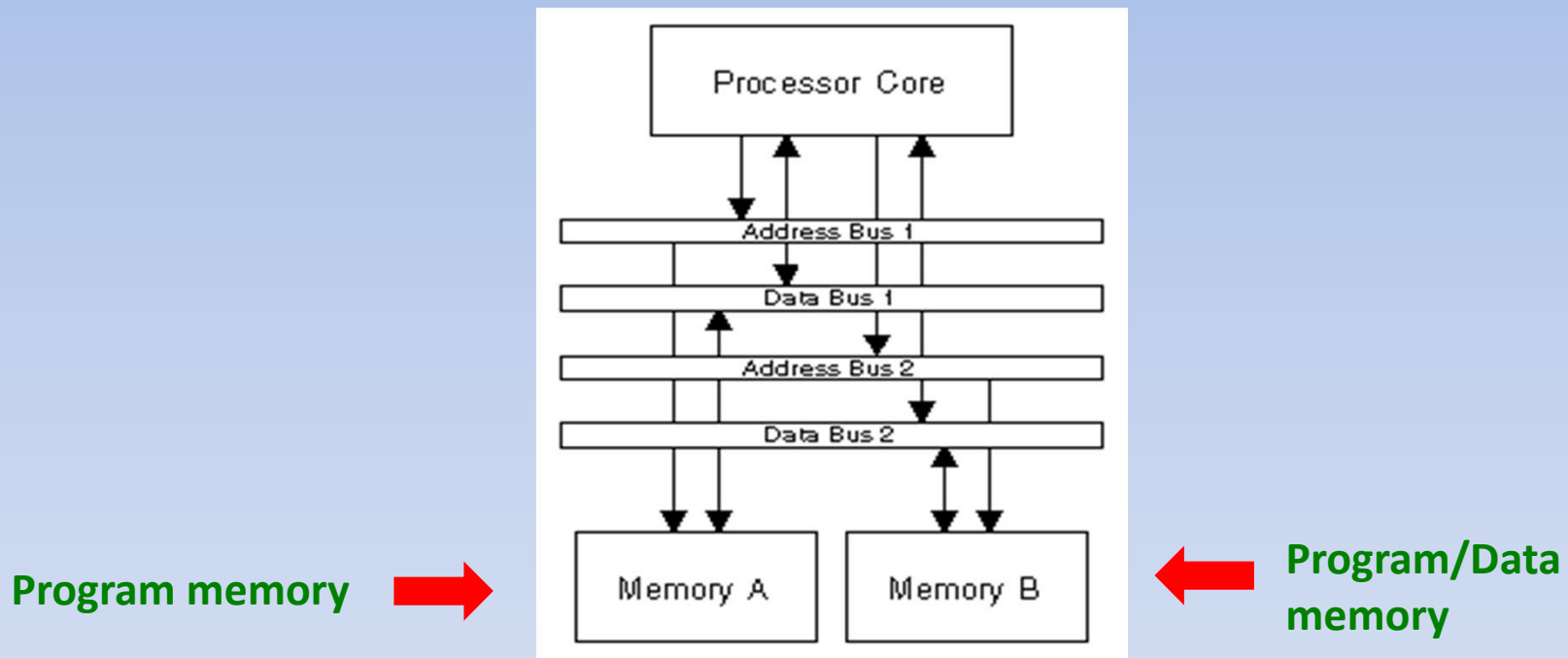
The Harvard architecture is a computer architecture with physically separate storage and signal pathways for instructions and data.

Von Neumann versus Harvard



Processor Architecture

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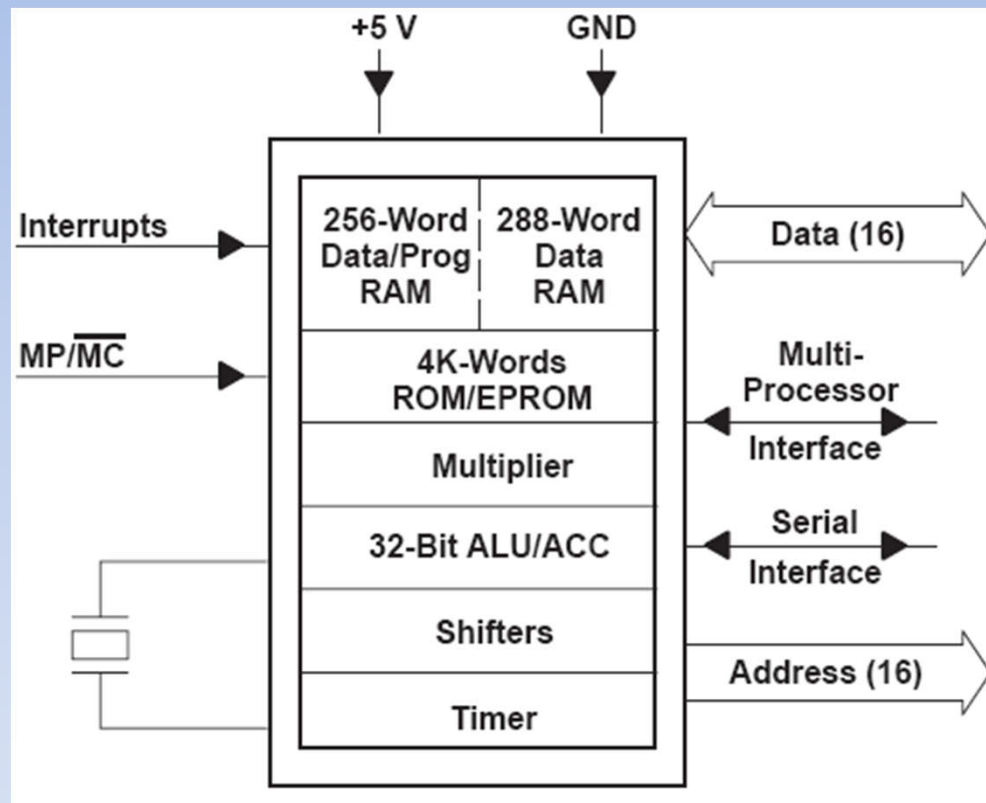


Modified Harvard architecture

The Modified Harvard architecture is very much like the Harvard architecture but provides a pathway between the data memory and the CPU that allows some words from the data memory to be treated as instructions.

Processor Architecture of TMS320C25

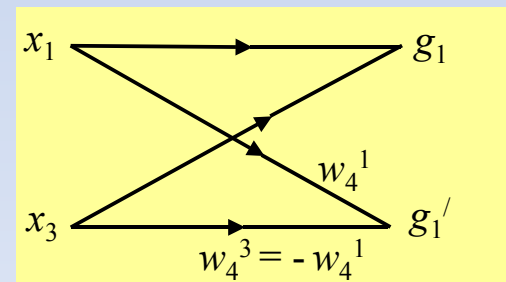
A second generation Digital Signal Processor from Texas Instruments with **Modified Harvard architecture**



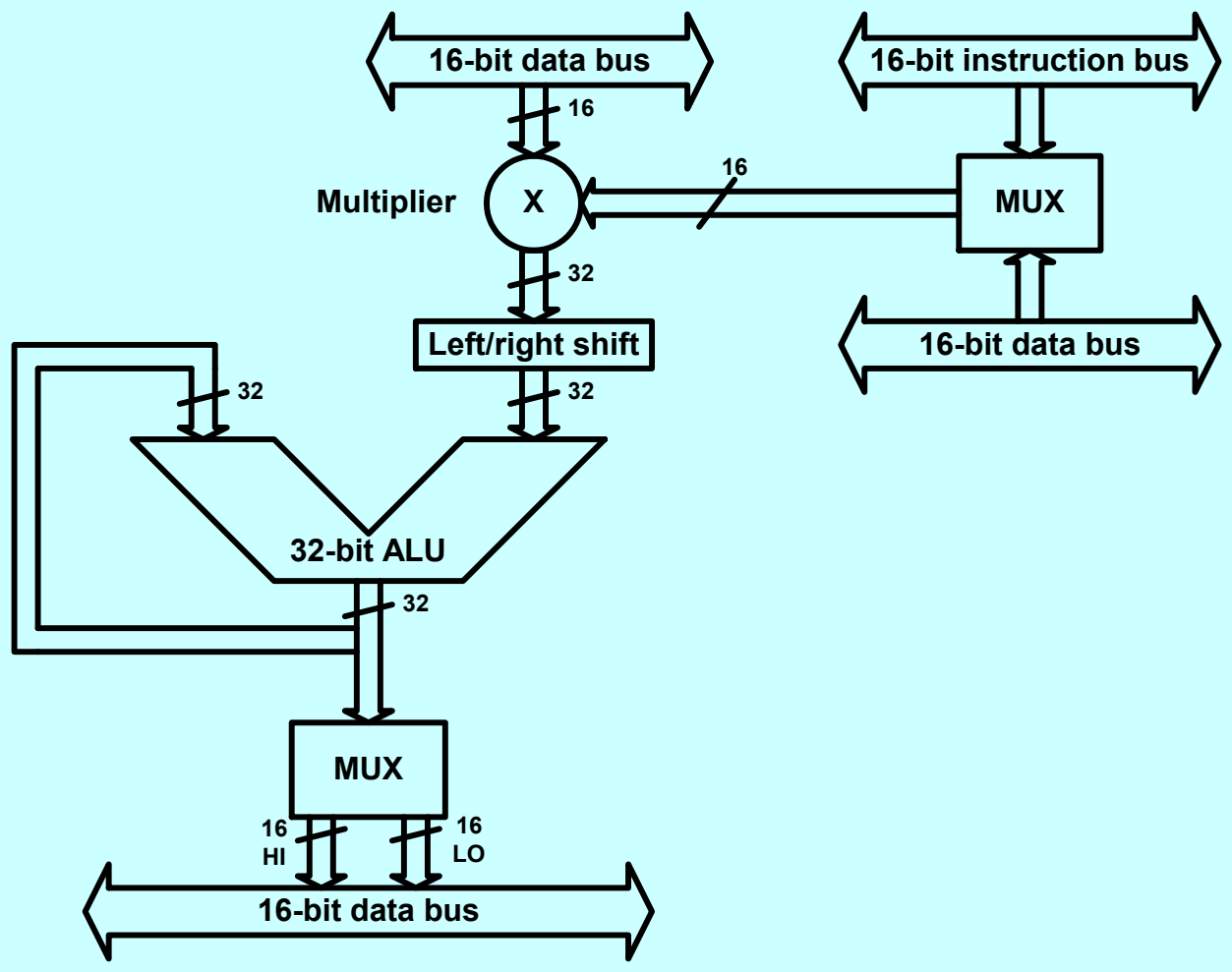
- **Single-cycle Multiply/Accumulate Instructions**
- **Bit-reversed Indexed-Addressing Mode for Radix-2 FFT**

Single-cycle Multiply/Accumulate Instructions are necessary for a Digital Signal Processor to implement FIR/IIR digital filters and FFT algorithms for real-time applications.

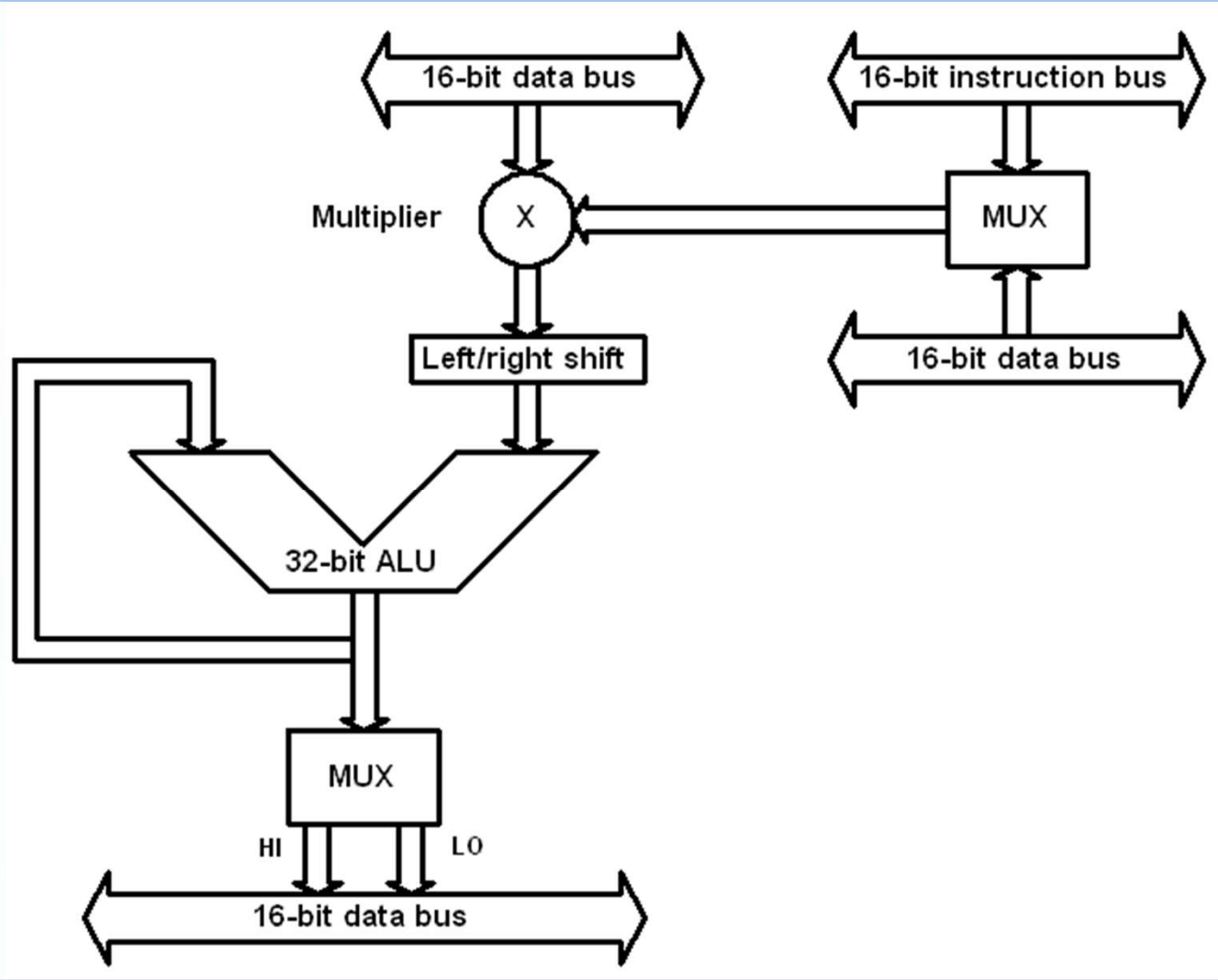
Computation of butterfly for radix-2 FFT



TMS320C25 Multiply/Accumulate Operation



TMS320C25 Multiply/Accumulate Operation



TMS320C25 Benchmarks (40 MHz Clock)

- FIR filter tap ~ 100 nano Sec per tap
- 256 tap FIR filter sample rate ~ 37 KHz
- Second order IIR filter sample rate ~ 1 MHz
- 8-point FFT sample rate ~ 50 KHz
- Single PID control loop sample rate ~ 750 KHz

Thank You