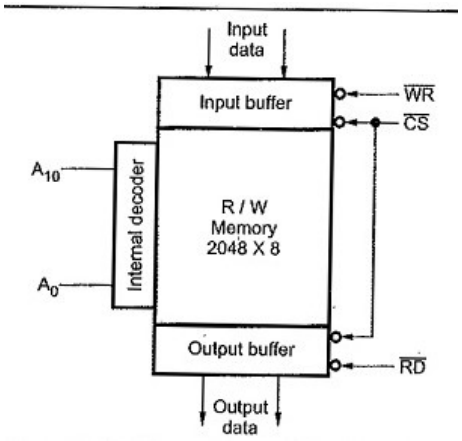
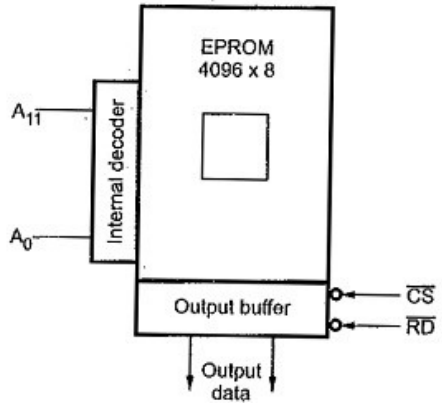
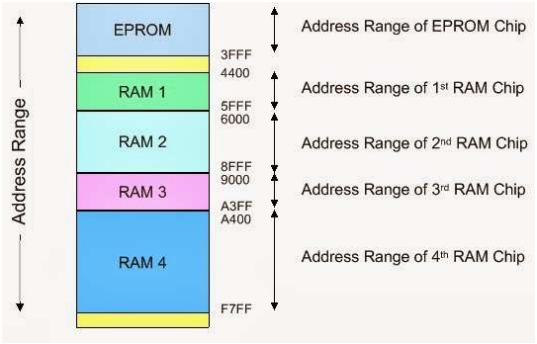
Read/Write memories consist of an array of registers, in which each register has unique address. The size of the memory is N x M where N is the number of registers and M is the word length, in number of bits.





RAM



8085 can access 64Kbytes memory since address bus is 16-bit.

When both, EPROM and RAM are used, the total address space 64Kbytes is shared by them. Generally EPROMs are used for storing Programs and RAMs are used for storing data

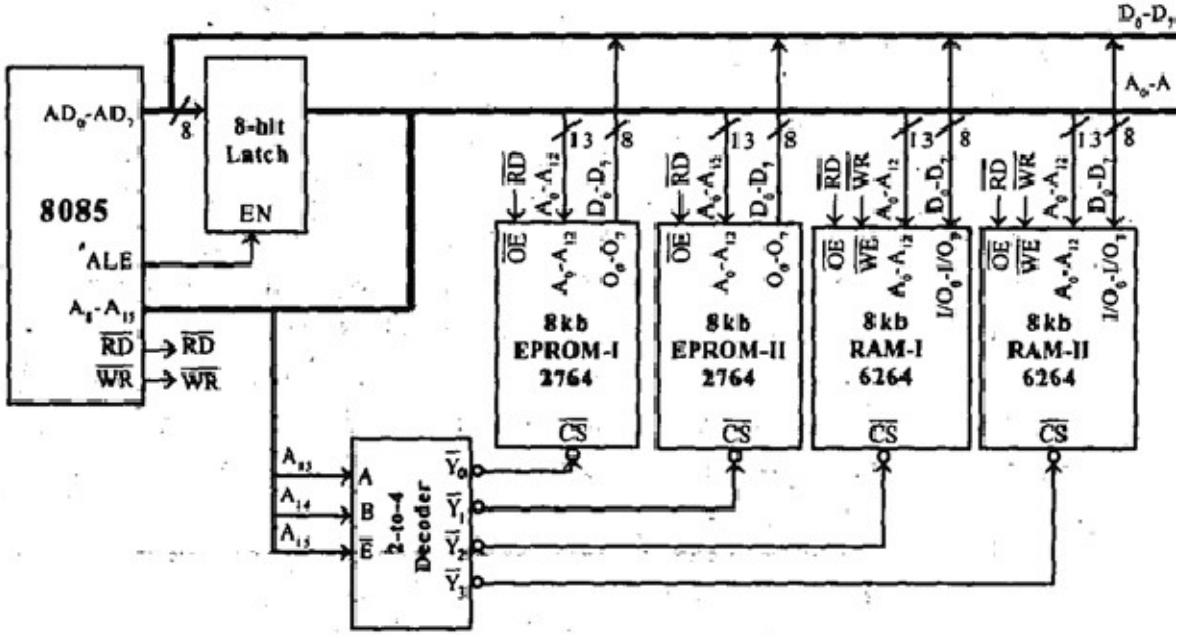
program memory (EPROM) should be located from address 0000H since reset address of 8085 microprocessor is 0000H.
It is not necessary to place RAMS and EPROMs in consecutive Address blocks

Memory Interface follows the following steps.

- *Select the chip*
- *Identify the register*
- *Enable the appropriate buffer*.

An Example of Memory Interfacing :**Full Address Decoding**

Consider a system in which 32kb memory space is implemented using four numbers of 8kb memory. Interface the EPROM and RAM with 8085 processor using 2 Nos. 8KB EPROMs



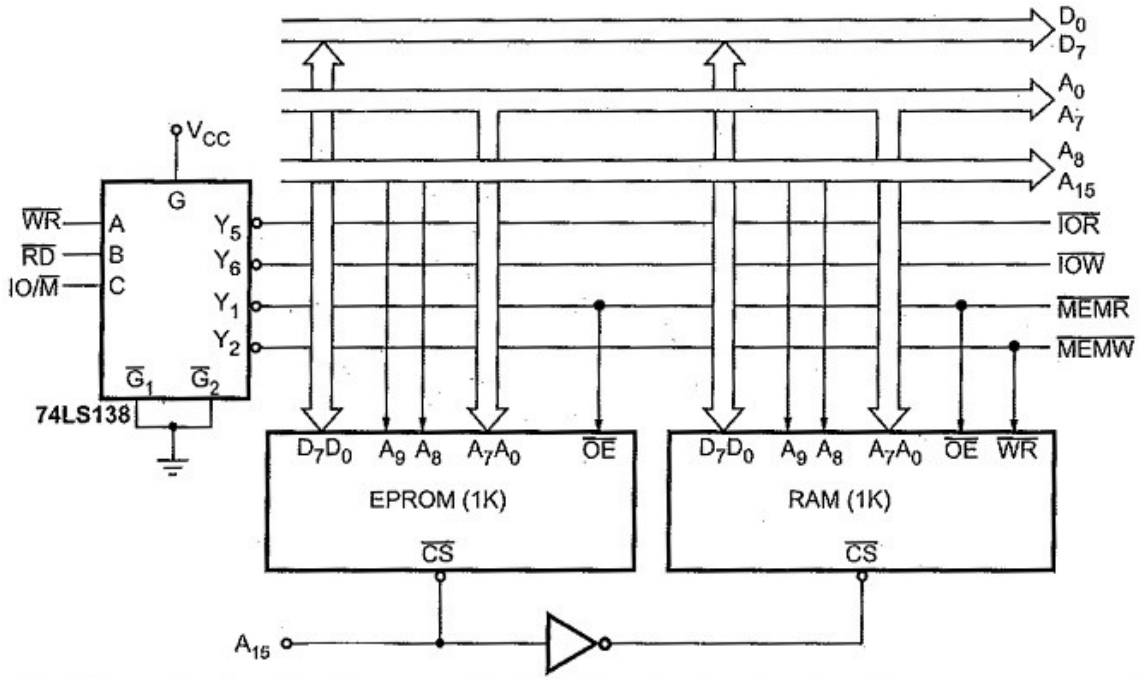
Device	Binary address																Hexa address
	Decoder enable/input			Input to address pins of memory IC													
	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
8kb EPROM - I	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFF
8kb EPROM - II	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	2001
	0	0	1	0	0	0	0.	0	0	0	0	0	0	0	1	0	2002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFF
8kb RAM - I	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4001
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	4002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	5FFF
8kb RAM -II	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6000
	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	6001
	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	6002
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7FFF

Address lines A0- A12 of the processor are connected to 13 address pins of all the memory.

address lines and A13 - A14 can be decoded using a 2-to-4 decoder to generate four chip select signals

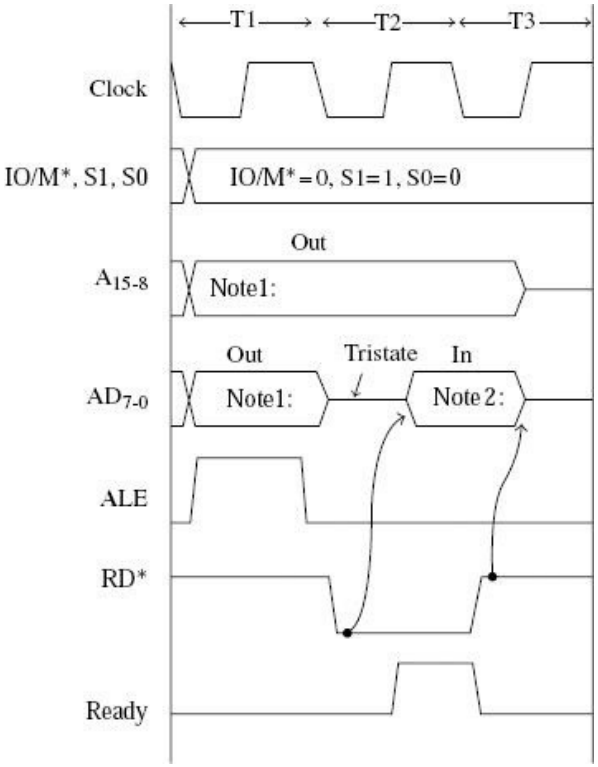
address line A15 can be used to enable the decoder

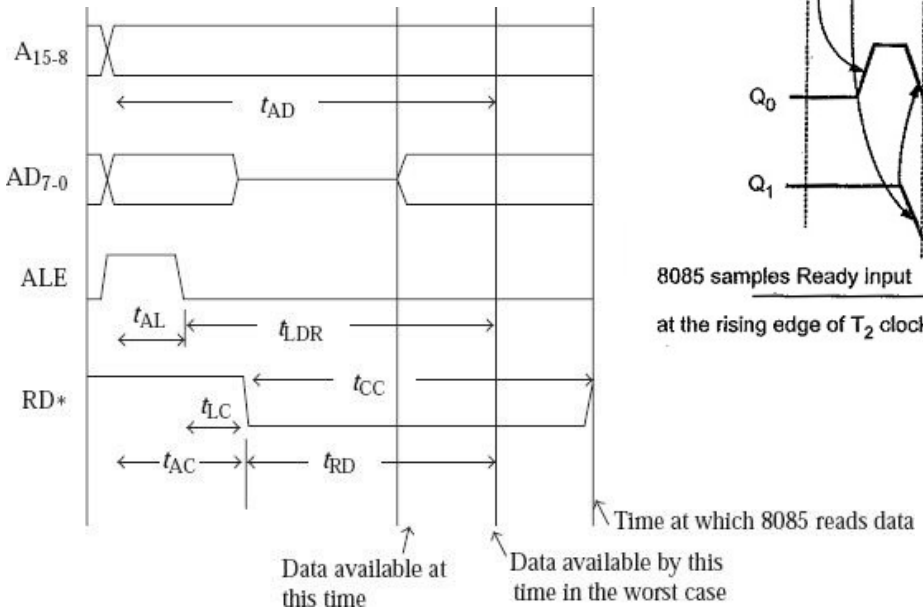
An Example of Memory Interfacing: Partial Address Decoding

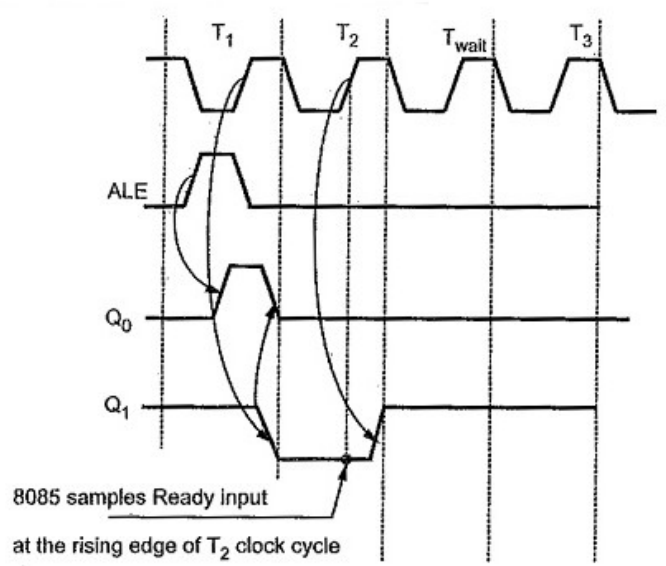


Decoder Logic is Eliminated
Works for small Systems
Leads to shadow addresses

Wait State Generation

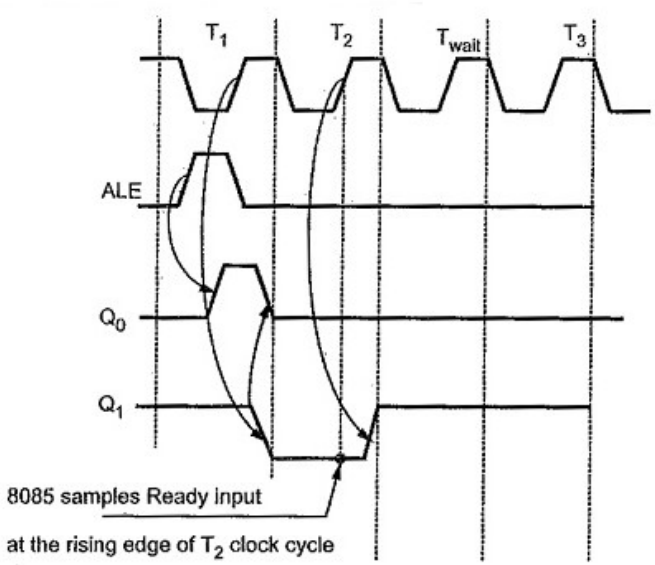


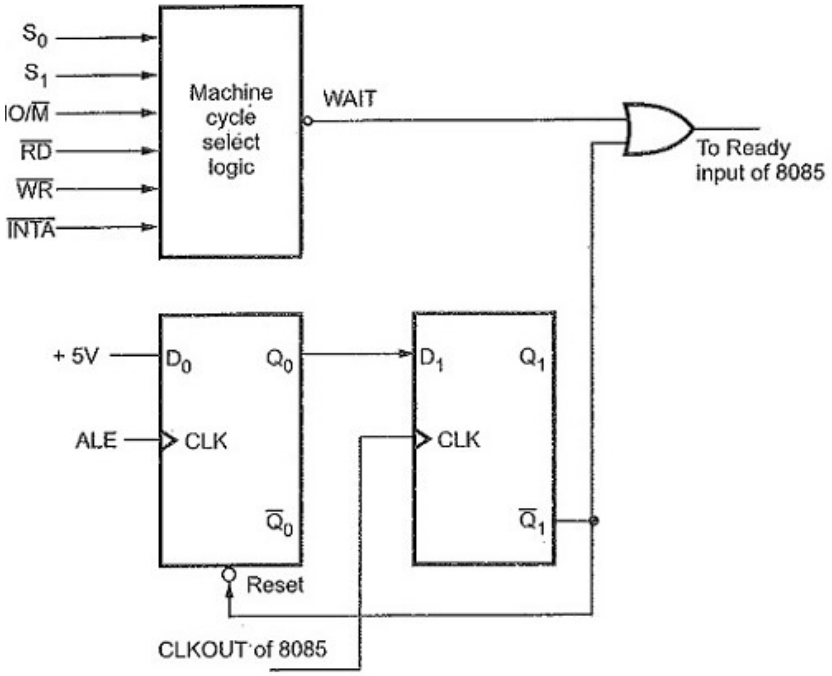


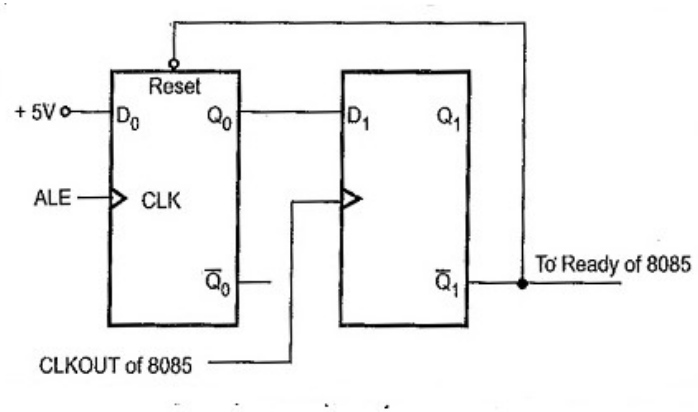


At the end of the state T2 in a machine cycle, 8085 processor senses the Ready input pin. If it is logic 0, 8085 processors enter the T wait state, else it enters to the T3 state. The Ready input is permanently fixed to logic 1.

Wait State Generation : Contd..







In T1, the ALE signal is activated, which makes output Q_0 of the first D flip-flop HI.

In the next rising edge of the CLKOUT signal of the 8085, the output of the second D flip-flop goes LO and resets the first D flip-flop making its Q_0 output LO,. At next low to high transition of CLKOUT, f the second D flip-flop goes high making READY pin high and inactivating reset input of the first flip-flop.