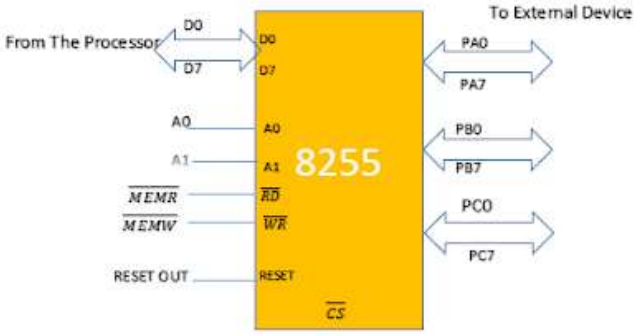
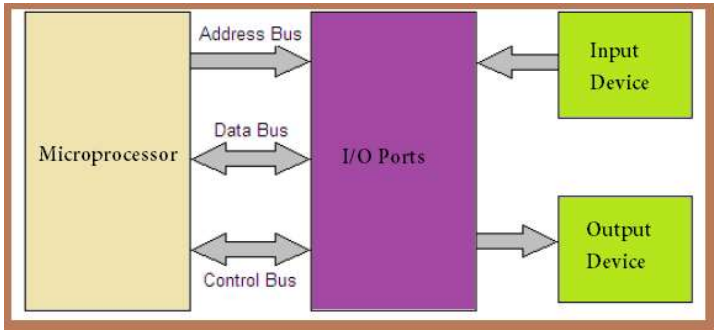
The 8255 is a programmable peripheral interface (PPI).



The 8255 works in two modes.
Two modes 1. I/O Mode
2. BSR Mode(Bit Set Reset)

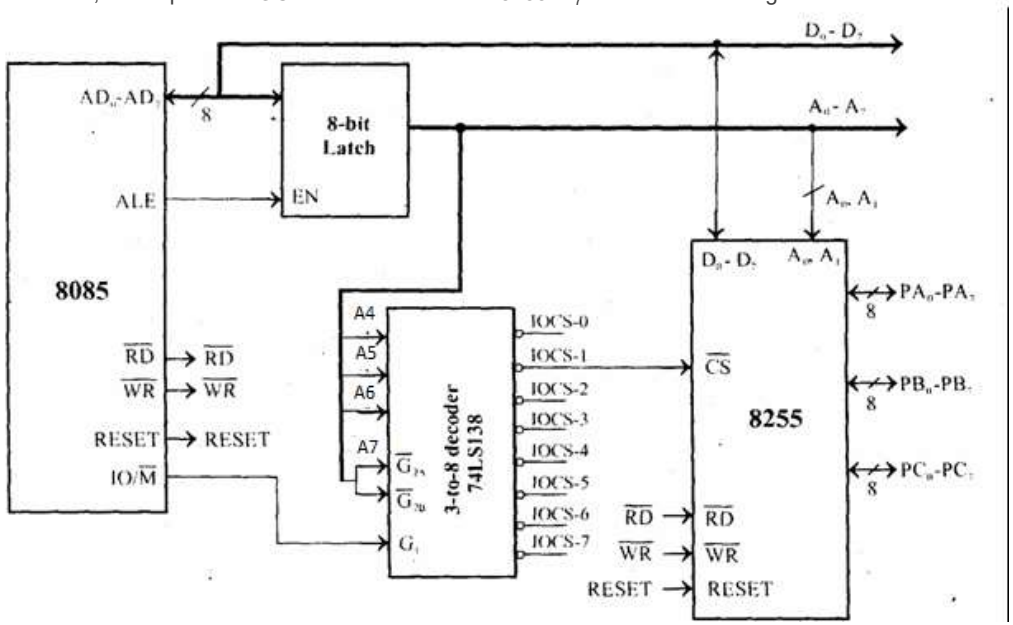
It has 3 Ports : Each Port contains 8 Pins
Port A, Port B, Port C - C upper and C lower

1.Read (RD): Microprocessor reads data from the selected port of 8255
2.Write(WR): Microprocessor writes data to the selected port if 8255
3.Reset : Reset as I/P Mode
4.Chip Select: To select 8255 IC.



The 8255 can be either memory mapped or I/O mapped in the system. In the schematic shown in above is I/O mapped in the system. In this slide an I/O Mapped interfacing is chosen (**I/O using IN or OUT commands**).

The address lines A_4, A_5 and A_6 are decoded to generate eight chip select signals (IOCS-0 to IOCS-7) and in this, the chip select IOCS- 1 is used to select 8255. A_7 is used for enabling the decoder



A_0 and A_1 are used for port selection

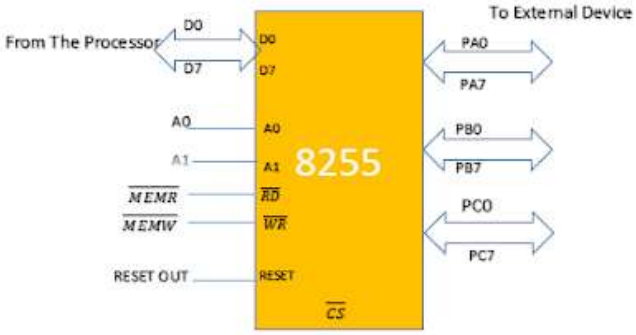
CS A1 A0

0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	CR
1	X	X	

For example, **for this configuration**, if we consider this configuration and the don't care states as zeroes, the following holds

Internal Device	Binary Address								Hexa Address
	Decoder input and enable				Input to address pins of 8255				
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Port-A	0	0	0	1	x	x	0	0	10
Port-B	0	0	0	1	x	x	0	1	11
Port-C	0	0	0	1	x	x	1	0	12
Control Register	0	0	0	1	x	x	1	1	13

Of course we can alter base address by altering A_2 to A_6 . The base address is listed in the manual and can be set using **Dip Switches**



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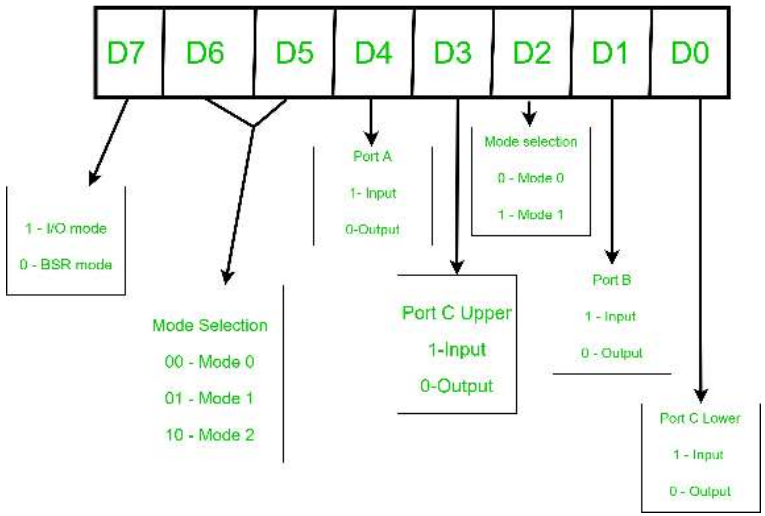
Control Word Format

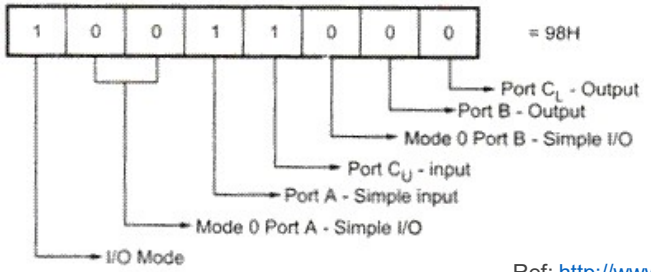


Write a program to initialize 8255 in the configuration given below:
1. Port A: Simple input
2. Port B: Simple output
3. Port CL: Output
4. Port Cu: Input

Assume address of the control word register of 8255 as 83H.

CS	A1	A0	
0	0	0	PORT A
0	0	1	PORT B
0	1	0	PORT C
0	1	1	CR
1	X	X	

MVI A, 98H :
OUT 83H



Q. Compute the address (operand of OUT) for the schematic in previous slide.

Ref: http://www.8085projects.info/Program66.html

Q. For the example in the previous slide, after calculating the base address, can you write an Assembly level program that reads 100 2 Byte integers using Port A and Port B and stores them in Memory Locations starting from 2000H at intervals of 1ms. Assume that you have a subroutine delay located at 4000H written for you which causes the delay when invoked.

The 8255 modes of operation : I/O Mode Mode 0

Port A, port B provide simple I/O operation. The two halves of port C can be either used together as an additional 8-bit port, or they can be used as individual 4-bit ports.

This mode is selected when the most significant bit (D7) in the control register is 1.

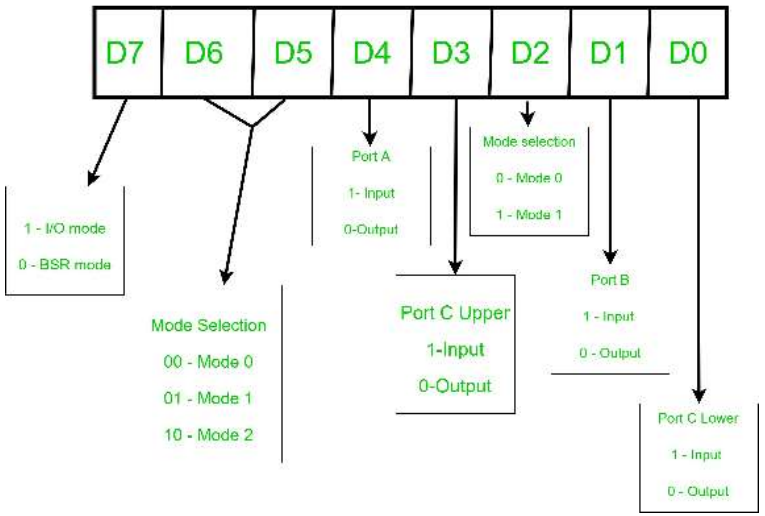
Mode 0 – Simple or basic I/O mode:
Port A, B and C can work either as input function or as output function. The **outputs are latched** but the **inputs are not latched but buffered**

In the **input mode**, the 8255 gets data from the external peripheral ports and the CPU reads the received data via its data bus. The CPU first selects the 8255 chip by making CS low. Then it selects the desired port using A_0 and A_1 lines. The CPU reads the data from the external peripheral device via the system data bus.

In the **output mode**, the 8255 first sends the data on its data bus. The CPU first selects the 8255 chip by making CS low. Then it selects the desired port using A_0 and A_1 lines. The CPU then writes the data to the external peripheral device via the system data bus.

Mode 1 – Handshake or strobed I/O:
In this either port A or B can work and port C bits are used to provide handshaking **(e.g. Printer Interfacing).** Both inputs and outputs latched

Control Word Format



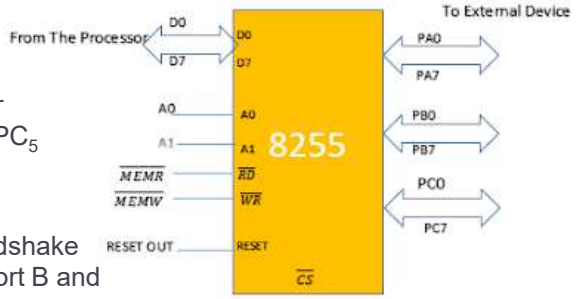
Q.What should be the control word if the 8255 Is selected in Mode 0 with Port A acting as Input Port B acting as Output and Port C acting as a full Port of 8 bits acting as an Input?

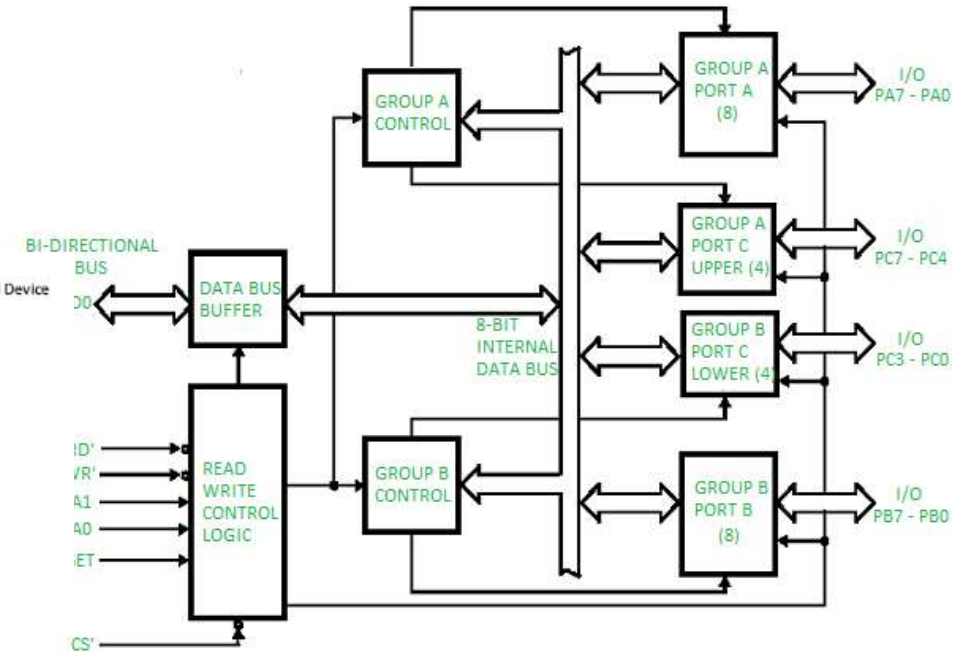
The 8255 modes of operation : I/O Mode Mode 1

Two ports i.e. port A and B can be used as 8-bit i/o ports.
Each port uses three lines of **port C** as handshake signal and remaining two signals can be used as i/o ports.
Interrupt logic is supported.
Input and Output data are latched
Mix and Match (Mode 0 and Mode 1) and input/output possible

Port C lines PC_3-PC_5 provide strobe lines for port A. This group including port A and PC_3-PC_5 from **group A**.

Port C lines PC_0-PC_2, provide strobe or handshake lines for port B. This group which includes port B and PC_0-PC_2 is called as **group B**





Deep Reading: Gaonkar/
https://nptel.ac.in/content/storage2/courses/106108100/pdf/Teacher_Slides/mod3/M3L2.pdf

The 8255 modes of operation : I/O Mode Mode 2

1. The single 8-bit port in group A is available.
2. The 8-bit port is bidirectional and additionally a 5-bit control port is available.
3. 3 I/O lines are available at port C.(PC_2 – PC_0)
4. Inputs and outputs are both latched.
5. The 5-bit control port C (PC_3-PC_7) is used for generating / accepting handshake signals for the 8-bit data transfer on port A.

Deep Reading: Gaonkar/
https://nptel.ac.in/content/storage2/courses/106108100/pdf/Teacher_Slides/mod3/M3L2.pdf

The 8255 modes of operation : BSR Mode

In this mode any of the 8-bits of port C can be set or reset depending on D_0 of the control word. The bit to be set or reset is selected by bit select flags D_3, D_2 and D_1 of the CWR as follows:

D_3	D_2	D_1	Selected bits of port C
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Can be used to generate Multiple Clock signals operating at programmable frequencies.

Q. Imagine that a subroutine delay is implemented in a 8085 based system which causes a delay of 100 micro sec. each time it is invoked. Assume further that this subroutine is written for you and is located in Memory location 2000H. Write an Assembly level program to produce a clock of frequency approximately 1KHz. Using bit D_2 of Port C of an 8255

Ref
https://nptel.ac.in/content/storage2/courses/106108100/pdf/Teacher_Slides/mod3/M3L2.pdf