Abstract

Error free digital wireless communication system is the ultimate goal to be achieved by communication engineers. In pursing such quest, tremendous efforts are being made by researchers to reduce the effect of channel noises. Presence of channel noises increase Bit Error Rate (BER) and degrade the performance of the communication systems considerably. Broadly, channel noises may be divided into two groups: random bit errors and burst errors. Random errors have no relation between one another whereas in burst errors a group of consecutive bits become erroneous. Researchers have developed various error correcting mechanisms to reduce the effect of such errors. Error Correcting Codes (ECC) designed for random errors are not effective for burst errors and vice versa. In most practical systems, both random and burst errors may exist together. Usually, techniques to overcome burst error are applied before ECC in order to ensure data fidelity from both types of errors. Interleaving technique is traditionally used to enhance the quality of digital transmission over a bursty channel. Interleaving is a process to rearrange code symbols so as to spread burst of errors into random like errors and can be handled by ECCs. Convolutional and block are the most popular types of interleavers being deployed in majority of the modern day communication systems to protect data against burst error.

Interleavers help to preserve data integrity during transmission over noisy channel against burst errors. The advantage is encompassed with drawbacks like additional memory requirement, system complexity and increased delay. Improved design of interleavers and efficient use of resources of the implementation platform make the interleaver a good choice to protect data from error bursts. **In case of convolution interleaver being used in DAB applications, memory wastage in the incremental shift registers is an issue to be addressed in design and implementation along with the operating speed of the circuit.** The permutation steps as prescribed in the standard documents for block interleavers of various OFDM based Broadband Wireless Access (BWA) applications like

WLAN, WiMAX, MIMO WLAN and LTE/LTE-A involves complex mathematical functions like floor, modulus and square. Implementation of these functions on hardware platform is very difficult due to the absence of direct digital hardware. Conventionally, Look-up Table (LUT) based approach is used which suffers from the drawbacks like slower speed of operation and large resource (especially memory) occupancy. **Therefore, resource efficient and low latency block interleaver design for the aforesaid applications is an important research area to work and contribute.**

In line with the formulation of research problem, efforts have been made to resolve the bottlenecks by proposing novel algorithms / efficient designs of the interleavers. MATLAB programmes are developed to verify the correctness of the novel algorithms. The proposed algorithms / designs are then transformed into digital hardware. VHDL models of these hardware have been prepared by judicious use of embedded resources available inside the reconfigurable target platform i.e. FPGA. Such efforts have clearly resulted in reduction of FPGA resources requirement with important achievement of improved speed performance. Consumption of lower power by the proposed designs is another important outcome to be reported. Timing simulations of the interleaver address generators / interleavers have been extensively carried out to verify functionality of the proposed hardware designs.

In the work to design efficient convolutional interleaver for DAB application, FPGA's embedded Shift registers (SRLC16) are used to model the incremental memory. This modelling lowers the hardware resource occupancy of FPGA in addition to reduction in memory wastage over existing implementations. In the issue of block interleaver design for IEEE 802.11 a/g based WLAN transceiver, two approaches namely improved LUT based and Finite State Machine (FSM) based have been proposed. The former technique demonstrates reduction in resource utilization like slices, flip flop and LUTs over conventional LUT based approach with improved operating speed of the Interleaver. Similar results are also obtained for FSM based implementation with further faster performance.

WiMAX is based on IEEE 802.16 d/e standard which employs special type of block interleaver. In this work, improved LUT based technique has been designed to generate de-interleaver addresses. The improvement in terms of memory saving and faster circuit operation over the conventional LUT based approach could be achieved. In addition, the author designed FSM based interleaver for the WiMAX application. Finally, a low-complexity and novel technique is proposed to efficiently implement the address generation circuitry of the 2-D de-interleaver used in the WiMAX transceiver. All these approaches result in resource efficient and high speed interleaver/de-interleaver implementations on FPGA platform. Transceiver used in MIMO WLAN employs multi stream block interleaver. In this work, hardware efficient model of MIMO WLAN interleaver eliminating the need for floor and modulus functions has been designed. To improve the performance of the address generator, embedded DSP blocks have been utilized. The work is also extended to model the interleaver memory using FPGA's embedded memory and thus provides complete hardware interleaver solution. The proposed work shows noticeable improvement in terms of maximum frequency and power consumption over the existing works. In the final phase, hardware efficient Quadratic Permutation Polynomial (QPP) interleaver address generator for LTE/LTE-A communication system is demonstrated. The address generator involves a quadratic equation and modulus function which do not have direct digital circuitry. A novel algorithm has been proposed to eliminate the need of squarer and modulus function. The algorithm is converted into efficient digital hardware and is implemented on FPGA platform with improved test results over conventional implementations.