Design of Multi-channel Frequency Hopping Spread Spectrum Transceiver for Wireless Communication

Thesis submitted by

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CERTIFICATE FROM THE SUPERVISORS

This is to certify that the thesis entitled **"Design of Multi-channel Frequency Hopping Spread Spectrum Transceiver for Wireless Communication"** submitted by **Mr. Anukul Chandra Baishya**, who got his name registered on 10.08.10 for the award of **Ph. D. (Engg)** degree of Jadavpur University is absolutely based upon his own work under the supervision of **Prof. M. K. Naskar** and **Prof. P. P. Sahu** and that neither his thesis nor any part of the thesis has been submitted for any degree/ diploma or any other academic award anywhere before.

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Dedicated to My family.....

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Abstract

Despite the fact that spread spectrum communication technique was originally used by military for interference rejection and enciphering, use of spread spectrum for jamming resistance became a popular concept by the end of World War-II. Further investigation of spread spectrum motivated by the need of highly jamming resistant communication systems, resulted in many other applications like energy density reduction, high resolution ranging and multiple access etc. Recently, spread spectrum techniques have found their way into many other consumer and industrial applications such as PCS phones, cordless telephones, wireless card readers, bar code scanners, blue tooth communication and so on. The overall system performance of any spread spectrum communication system is directly affected by the speed and reliability of the spread spectrum transceiver and hence demands for high transmission rate, high quality and security necessitate high speed and at the same time high performance spread spectrum transceivers.

This thesis is specifically focused on the design and analysis of frequency hopping spread spectrum transceiver for wireless communication applications with particular attention to transmitter and receiver system design. This work also attempts to address the issues associated with the design of some of the critical CMOS RF analog circuits employed in the proposed architecture. The key analog circuit block in the transmitter is the Voltage Controlled Oscillator (VCO) with reasonably wide bandwidth. We have designed a new CMOS current starved voltage controlled ring oscillator (CSVCRO) and verified it by simulating in CMOS technology. The VCO architecture proposed here provides high linear relationship between oscillation frequency ranging from 0.7-1.75GHz over a control voltage ranging from 1.2-2V and results in a large tuning range of 75%. The phase noise achieved is -88dBc/Hz at an offset frequency of 1MHz. The linear frequency sweep is obtained without employing any additional compensation techniques resulting in less circuit complexity, die area and power consumption. We have also custom-designed the digital and mixed signal circuits such as 4-bit data word generator, PN sequence generator, 8:1 multiplexer, serial-to-parallel (S2P) converter, Digital-to-analog converter (DAC)etc. using the standard architectures in order to complete the transmitter system.

The key analog circuit blocks in the receiver section are the RF front-ends such as Low noise amplifier (LNA), wide band or frequency independent precision rectifier and

the Frequency-to-voltage converter (FVC). We have designed a CMOS based low noise amplifier with L-type input matching network and Π-type output matching network. The input L-type matching network is used to fix the Q-factor whereas the output Π-type matching network provides an extra degree of freedom to adjust the bandwidth. Simulation results reveal that a gain of 22.7 dB for the frequency range of 0.9 to 6GHz and noise figure (NF) of $\geq$ 2.5 dB are obtained and are reasonably good in comparison to the reported works. We have also conceptualized a new sinusoidal full wave precision rectifier architecture which was implemented with discrete components and validated by experimentation. The circuit gives a d.c. output voltage, the magnitude of which is nearly the same as the peak input voltage over a frequency range of 50Hz to 1MHz with a very low ripple voltage and low harmonic distortion. The architecture was modified in order to remove the frequency dependency that arises at the present high frequency application and was implemented using CMOS technology. Simulation results reveal that the circuit rectifies small (mV) a.c. signals at 1GHz and a little beyond.

We have also designed and implemented the sub-circuits like analog-to-digital converter (ADC), parallel-to-serial converter (P2S), Differentiator, Integrator, Logarithmic and anti-logarithmic amplifiers, Comparator, Coding network etc. using standard topologies in order to complete the receiver system.

The successful design of the individual RF blocks (analog, digital and mixed signal) and their simulation results demonstrate that it is feasible to achieve a fully integrated frequency hopping spread spectrum transceiver architecture as proposed in this thesis without employing PLL, FLL or DDFS for frequency synthesizing with reasonably good noise performance.

Keywords: VCO, FVC, Phase noise, LNA, Precision rectifier, Ripple voltage, Harmonic distortion, Noise figure, PLL.

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Glossary of Terms

ALU	Arithmetic and Logical Unit
EDA	Electronic Design Automation
RF	Radio Frequency
CMOS	Complementary Metal Oxide Semiconductor
VCO	Voltage Controlled Oscillator
DDFS	Direct Digital Frequency Synthesizer
IFH	Interpolated Frequency Hopping
DSP	Digital Signal Processing
FVC	Frequency to Voltage Converter
VLSI	Very Large Scale Integration
HF	High Frequency
FHSS	Frequency Hopping Spread Spectrum
SPICE	Simulation Program with Integrated Circuit Emphasis
PSPICE	Personal Simulation Program with Integrated Circuit Emphasis
HSPICE	Hailey Simulation Program with Integrated Circuit Emphasis
IF	Intermediate Frequency
SNR	Signal to Noise Ratio
BER	Bit Error Rate
PN	Pseudo Noise
DAC	Digital to Analog Converter
LNA	Low Noise Amplifier
AWR	Advanced Wave Research
EM	Electro Magnetic
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
LAN	Local Area Network
MAN	Metropolitan Area Network
WAN	Wide Area Network
PAN	Personal Area Network
TV	Television
VHF	Very High Frequency
UHF	Ultra High Frequency

SHF	Super High Frequency
GPS	Global Positioning System
PCS	Personal Communication System
TVRO	Television Receive-Only
DBS	Data Base System
FM	Frequency Modulation
MW	Micro Wave
FDMA	Frequency Division Multiple Access
FDD	Frequency Division Duplexing
FSK	Frequency Shift Keying
TDMA	Time Division Multiple Access
GSM	Global System for Mobile Communication
GPRS	General Packet Radio Service
EDGE	Enhanced Data for GSM Evolution
ITU	International Telecommunication Union
IMT	International Mobile Telecommunication
UMTS	Universal Mobile Telecommunication System
CDMMA	Code Division Multiple Access
WCDMA	Wideband Code Division Multiple Access
3GPP	Third Generation Partnership Program
IPv6	Internet Protocol version 6
QoS	Quality-of-Service
OFDM	Orthogonal Frequency Division Multiplexing
OFDMA	Orthogonal Frequency Division Multiple Access
AMC	Adaptive Modulation and Coding
MIMO	Multi-input Multi-output
ARQ	Automatic Repeat Request
HARQ	Hybrid Automatic Repeat Request
IEEE	Institute of Electrical and Electronics Engineers
WiMAX	Worldwide Interoperability for Microwave Access
UMB	Ultra Mobile Broadband
NTT	Nippon Telegraph and Telephone
TACS	Total Access Communication System
NMT	Network Management Tool
AMPS	Advanced Mobile Phone Service
N-AMPS	Narrowband Advanced Mobile Phone Service
PACS	Picture Archiving and Communication System
PDC	Personal Digital Cellular
PHS	Packet Handling System
CDPD	Cellular Digital Packet Data
DECT	Digital Enhanced Cordless Telephone

TD-CDMA	Time Division Code Division Multiple Access
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
EV-DV	Evolution Data and Voice
EV-DO	Evolution Data Optimized
WiBro	Wireless Broadband
HMAN	Hybrid Metropolitan Area Network
HSPA	Evolved High Speed Packet Access
LTE	Long Term Evolution
VHT	Very High Throughput
USSR	Union of Soviet Socialist Republic
SCORE	Signal Communications by Orbiting Relay Equipment
LEO	Low Earth Orbit
DVB-S	Digital Video Broadcasting System
GEO	Geostationary Earth Orbit
AM	Amplitude Modulation
PM	Pulse Modulation
DSB	Double Sideband
SSB	Single Sideband
LO	Local Oscillator
ASK	Amplitude Shift Keying
FSK	Frequency Shift Keying
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
DPSK	Differential Phase Shift Keying
BPSK	Binary Phase Shift Keying
BEP	Bit Error Probability
AWGN	Additive White Gaussian Noise
PSD	Power Spectral Density
MPSK	M-ary Phase Shift Keying
SEP	Symbol Error Probability
BFSK	Binary Frequency Shift Keying
DSSS	Direct Sequence Spread Spectrum
THSS	Time Hopping Spread Spectrum
ACF	Auto Correlation Function
CCF	Cross Correlation Function
MLSR	Maximum Length Shift Register
FFH	Fast Frequency Hopping
SFH	Slow Frequency Hopping
PLL	Phase Locked Loop

ROM	Read Only Memory
PA	Power Amplifier
VSWR	Voltage Standing Wave Ratio
RL	Return Loss
IRL	Input Return Loss
ORL	Output Return Loss
CAD	Computer Aided Design
NF	Noise Figure
NQS	Non Quasi Static
PMOS	P-type Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
NBTI	Negative Bias Temperature Instability
DIBL	Drain-Induced Barrier Lowering
GIDL	Gate-Induced Drain Leakage
ULSI	Ultra Large Scale Integration
BSIM	Berkeley Short-channel IGFET Model
ACM	Accurate and Compact MOSFET model
CAPOP	Capacitor Model Selector Parameter
UCB	University of California Berkeley
TSMC	Taiwan Semiconductor Manufacturing Company
S2P	Serial to Parallel
CMRR	Common Mode Rejection Ratio
JFET	Junction Field Effect Transistor
PHEMT	Pseudomorphic High Electron Mobility Transistor
GBW	Gain Bandwidth Product
FLL	Frequency Locked Loop
AFC	Automatic Frequency Control
OTA	Operational Transconductance Amplifier
BJT	Bipolar Junction Transistor
PSRR	Power Supply Rejection Ratio
UGB	Unity Gain Bandwidth
TC	Thermometer Code
AOI	And-Or-Invert
P2S	Parallel to Serial
FFT	Fast Fourier Transform
CFSK	Continuous Frequency Shift Keying

Symbols and Notations

ω_c	Angular frequency
β	Modulation index
Γ	Reflection coefficient
$\phi_{\tilde{S}}$	Power spectral density
P_S	Symbol error probability
G_p	Processing gain or spreading factor
T_c	Chip duration
$CCF_{(i,j)}$	Cross correlation function of two codes C_i and C_j
ACF_i	Auto correlation function at time iT_c
T_s	Symbol duration
R_s	Symbol rate
BW	Null bandwidth
B_{nn}	Null bandwidth
$W_{hopping}$	Frequency band over which the system hops
Z_L	Load impedance
Z_S	Source impedance
Z_O	Characteristic impedance
Q	Quality factor of reactive elements
Q_L	Loaded quality factor (Q)
P_l	Power dissipated by resistor
W_m	Average magnetic energy stored in inductor
W_e	Average electric energy stored in capacitor
I_L	Current through inductor
V_C	Voltage across capacitor
I_i	Incident current
I_r	Reflected current
V_i	Incident voltage
V_r	Reflected voltage
S^I	Current scattering parameter
S^V	Voltage scattering parameter
S_{11}	Input reflection coefficient
S_{21}	Forward transmission or insertion gain

S_{12}	Reverse transmission or insertion gain
S_{22}	Output reflection coefficient
NF	Noise figure
V_{gs}	Gate to source voltage
V_{gs}	Gate to source voltage
V_{ds}	Drain to source voltage
V_{th}	Threshold voltage
V_{dd}	Drain voltage
V_{od}	Overdrive voltage of MOSFET
V_{dsat}	Drain to source voltage when $V_{gs} - V_t = V_{ds}$
C_{ox}	Oxide capacitance
t_{ox}	Gate oxide thickness
W	Device (MOSFET) width
L	Device (MOSFET) length
g_m	Transconductance
μ_n	Electron mobility
C_{ov}	Parallel plate capacitance of MOSFET
C_{jsb}	MOSFET junction (source-to-bulk) capacitance
C_{jdb}	MOSFET junction (drain-to-bulk) capacitance
C_{gc}	Capacitance between gate and channel of MOSFET
C_{cb}	Capacitance between channel and bulk of MOSFET
C_{gs}	Capacitance between gate and source of MOSFET
C_{gd}	Capacitance between gate and drain of MOSFET
C_{sb}	Capacitance between source and bulk of MOSFET
C_{db}	Capacitance between drain and bulk of MOSFET
ω_T	Frequency at which MOSFET current gain falls to unity
ω_{max}	Frequency at which MOSFET power gain falls to unity
Φ_S	Surface potential (MOSFET)
Φ_F	Fermi level of substrate (MOSFET)
ϵ_{ox}	Dielectric constant of oxide
S	Scaling parameter (semiconductor technology)
L_{min}	Minimum channel length of MOSFET
W_{min}	Minimum channel width of MOSFET
N_A	Substrate doping
f_T	Cut-off frequency of MOSFET
f_{max}	Maximum oscillation frequency of MOSFET
KP_n	Transconductance parameter for NMOS transistor
KP_p	Transconductance parameter for PMOS transistor
T_{pd}	Propagation delay
f_{osc}	Oscillation frequency
$\Delta\omega$	Offset frequency

G_aA_s	Gallium Arsenide
A_D	Differential mode gain
A_{CM}	Common mode gain

Chapter 1

Introduction

1.1 Problem overview

This dissertation addresses the problems encountered in the design of frequency hopping spread spectrum communication systems [2–7] employing widely distributed radio elements, providing wide area coverage, using higher order modulation techniques, multiple data rates, and requiring multiple access. It provides a brief description of the various spread spectrum approaches as well as considerations to determine the suitability of the frequency hopping spread spectrum (FHSS) against its counterparts. It also presents a system model reflecting the level of sophistication the modern digital communication systems are striving to achieve through the innovative applications of new technologies. In the process of illustrating how the frequency hopping spread spectrum techniques would apply to such sophisticated systems, it identifies especially the problems associated with high speed CMOS analog circuit design that need to be addressed. In order to fill an existing gap between the CMOS circuit designers and the communication system designers, and also to establish a suitable reference point, some of the more commonly encountered circuit design techniques for communication systems are included.

The main engineering challenge posed by this thesis is analog radio frequency (RF) circuit design using CMOS technology [8, 9]. Due to low power requirement and high operating frequency, design of radio frequency transceiver subsystems encounters many challenges.

Other related challenges include the choice of transceiver type. Different types of transceivers such as homodyne, heterodyne, image reject etc. have certain advantages and disadvantages and the challenge is to choose or propose an architecture so that the disadvantages are minimized and at the same time advantages are maximized.

The functional building blocks of the transceiver proposed in this thesis include spread-

ing unit, baseband to RF converter (VCO), low noise amplifier, frequency-to-voltage converter (FVC), de-spreader and a decoder. Design of these units also exhibit trade-offs among gain, noise, linearity, power dissipation, operating frequency and supply voltage.

1.2 Motivation

Recent years witnessed a tremendous growth of low power and low cost radio transceivers for wireless communication applications. This could occur because of the introduction of digital signal processing in wireless communication driven by the development of high performance low power and low cost CMOS technology suitable for very large scale integration (VLSI) [10, 11]. However, the RF analog front-end remains the bottleneck for low-cost RF systems for various reasons, the most prominent ones being high power consumption, narrow operating bandwidth, larger space requirement, design complexity etc. These units consume more than 50% of the total power during data communication. Preliminary literature survey on the design of radio-frequency transceivers shows that the transmitter is one of the most power hungry units in any transceiver system. Since the ultimate requirement is directed towards full integration of both digital and analog circuit blocks on the same die, the RF analog front-end needs to be pushed towards higher levels of integration in low power CMOS technology. Also RF front-ends need to detect very week but high frequency signals and have to transmit high frequency high power levels and therefore, high performance and at the same time low power circuits are required. These drawbacks can either be fully or partially circumvented by properly choosing the transceiver architecture, circuit topology, device models, reducing the number of power-hungry interface circuits and finally systematic optimization of different circuit blocks. While transistor technology scaling [12–16] and improved circuit techniques are likely to contribute to evolutionary advances towards this goal, architectural innovations of the transceiver may lead to revolutionary improvements.

1.3 Literature review

A general review of conventional frequency-hopping system design approach is useful before any alternative proposal is introduced. A typical frequency hopped transmitter and receiver is shown in Fig.1-1 and 1-2 respectively. In the transmitter, a pseudorandom hopping code is used to control the output frequency of a PLL-based synthesizer. The carrier is then modulated with a data signal and transmitted. In the receiver, the same pseudorandom hopping code and the IF is subtracted from the incoming signal in the frequency domain and the resulting signal is the FM carrier modulated with the data

and centered at the IF. This output contains significant energy at IF and thus frequency hopping presents an opportunity to be used in CDMA. In frequency hopping CDMA, each user is allotted a different hopping code and if the different hopping codes have low cross correlation, several users can simultaneously occupy the same frequency band only with gradual degradation in SNR performance [17]. Frequency-hopping provides resistance to stationary interference and multipath fading since the carrier is regularly being hopped in frequency. The effectiveness of a particular frequency-hopping system for a given transmission channel depends on factors such as the hopping rate, the size of the hops, and the number of data symbols transmitted during each hop interval [18].

The core block of an FHSS system is the frequency synthesizer. An agile and accurate

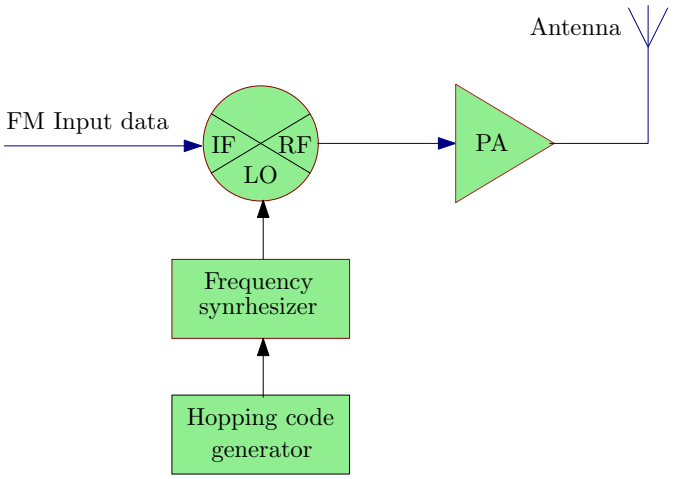


Figure 1-1: Typical frequency hopping transmitter

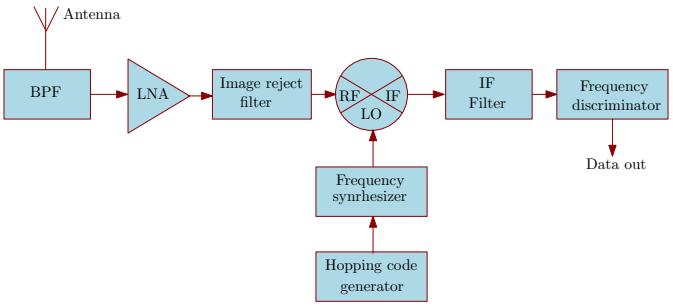


Figure 1-2: Typical frequency hopping receiver

frequency hopping system demands a fast settling behavior as well as a high degree of accuracy in the frequency synthesis. Conventional hop frequency synthesizers are based on phase-lock-loop (PLL) with digitally controllable dividers [19]. Another means to accurately synthesize the frequency, is to use a mixed-signal approach. The accuracy and the fast settling behavior are realized through the use of a direct-digital frequency synthesizer (DDFS) and a digital-to-analog converter (DAC) is used to translate the discrete time periodic waveform from the DDFS in a continuous waveform with specified spectral characteristics [20]. The VCO and the frequency divider are the main sources of power dissipation in a PLL-based synthesizers. The 900 MHz PLL [19] dissipates

5mA current from a 3V supply which results in a total power consumption of 15mW out of which 12mW is dissipated by the VCO itself. In direct-digital frequency synthesizer, a sine wave is synthesized in digital domain using a simple accumulator and a phase-to-sine amplitude converter. In its simplest form this converter is a read-only memory (ROM). A DAC and a low-pass filter (LPF) are used to convert the sinusoidal samples into an analog waveform. The main function of the N-bit phase accumulator is the N-bit addition. The energy required for an addition by an arithmetic and logical unit (ALU) can be considered in the range of 250 pJ per addition and the power consumption of the phase accumulator can be predicted by the following equation [21]:

$$\mathrm{P_{phase-acc}} = \mathrm{f_{ref-clk}} \times \mathrm{E_{add}} \tag{1.1}$$

where, $f_{ref-clk}$ is the reference clock frequency and E_{add} is the energy per N-bit addition. From eqn.(1.1) it can be predicted that the phase accumulator consumes a significant amount of power. The second most power hungry block in a DDFS is the ROM. It is a known fact that words longer than 14-bits need a very large ROM even if compression techniques are used. It is revealed from [22] that most of the power consumption in a ROM is from the pre-charge or the evaluation of the memory cells. Therefore, it can be concluded that the power consumption of the DDFS excluding DACs is highly significant and not suitable for low power wireless applications.

Apart from large power consumption, two more major drawbacks encountered in PLL-based frequency-hopping are *spectral splatter*, and *transient mismatch* between the transmit and the receive synthesizers [23]. During a hop transient, simple frequency-hopping systems do not have any control over the transmitted frequency spectrum, and many undesired frequency components are present in the output of the transmitter. This phenomenon is known as spectral splatter and results in a loss of useful transmitter energy during each hop, as well as adjacent channel interference. In addition to this, if a mismatch in the hopping transient of the receive synthesizer and the transmit synthesizer occurs, bursts of frequency error takes pace in the receiver IF at the hopping rate, resulting in overall degradation of the receiver signal-to-noise ration (SNR). Some common solutions employed to reduce spectral splatter and the effects of synthesizer mismatch are voltage-controlled oscillator (VCO) pretuning [23], ping-ponging multiple synthesizers [23], and transient hop interval dwell and guard times [24]. These methods are briefly reviewed below.

VCO pre-tuning mechanism employs a digital-to-analog converter and a summing unit placed in the synthesizer PLL between the loop filter and the VCO of both the transmitter and the receiver. When a frequency hop occurs, the VCO control voltage gets changed directly, as well as the normal loop frequency control, in a coordinated manner and results in the reduction of the effects of transient mismatch. Since the DAC and the summing units are outside the loop, the output frequency of the synthesizer can be changed rapidly, and the loop catches up after wards, removing residual error.

Frequency-hopping systems that “ping-pong” two synthesizers in both the transmitter

and the receiver can also be designed. In this arrangement, the second synthesizer is preset for the next hop frequency while the first synthesizer frequency is being transmitted. In order to transmit the next frequency, the two synthesizers are exchanged (ping-ponged), eliminating the effects of PLL transient error. To avoid the effects of IF

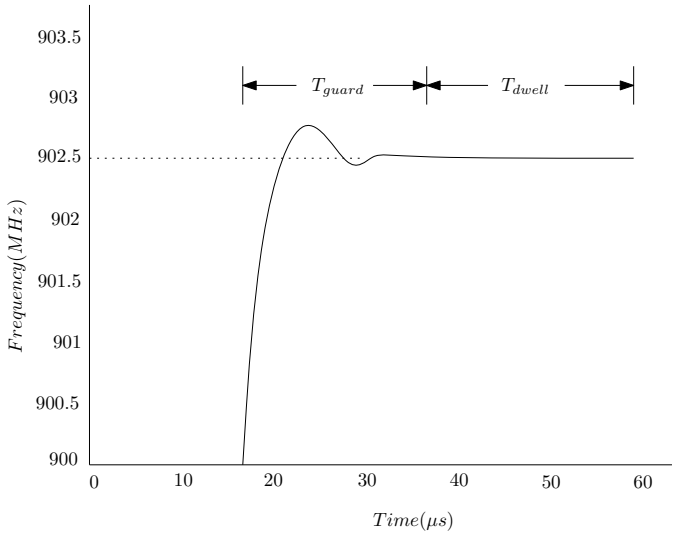


Figure 1-3: Illustration of hop transient

error, transient guard and dwell times, as shown in Fig.1-3, are frequently employed in frequency-hopping systems. In this approach, the IF signal is not sampled at the receiver until the loop transients are settled out during a frequency hop. Thus, the received data is not corrupted as the IF contains no frequency error during the sample or dwell time. The transmitter output power is turned off in some systems, during the guard times in order to reduce or eliminate the spectral splatter produced by the hop transients.
Although the above solutions are quite effective, they results in higher system complexity and cost or a reduction in effective data-sampling time that increases the receiver bit error rate (BER).
Another alternative solution to the problems encountered in simple frequency hopping, known as interpolated frequency hopping (IFH) is provided in [25]. This approach replaces the analog complexities associated with conventional frequency synthesizers with digital complexities. The differences between a standard frequency-hopping system and the IFH are the inclusion of a digital filter placed between the hopping-code generator and the synthesizer-control word input in both the transmitter and the receiver, as well as differences in the digital-signal processing (DSP) to be performed on the discriminator output in the receiver. In IFH, the pseudorandom hopping code is passed through a digital interpolation filter prior to controlling the synthesizer instantaneous frequency output. IFH, in addition to reducing the problems like spectral splatter and IF error, provides the receiver with a continuous stream of data that can be sampled over the entire symbol interval and thereby gives an opportunity to improve the received IF power. Interpolation of the hopping code is used in IFH to reduce the high frequency content of the hopping steps, thereby reducing the PLL phase error. The result of this filtering is

a carrier that moves smoothly and continuously in frequency. There exists a possibility to use higher code rates for a given synthesizer with IFH compared to simple frequency-hopping, because IFH produces constant phase error, which increases with the code rate. As the code rate increases, the SNR of the receiver will decrease proportionally, and eventually, reception will become impossible. In conventional frequency-hopping, as code rates begin to approach the loop settling time, dwell times become unusable and reception also becomes impossible. This transition should be more gradual with IFH than hopping. There may exist a point where reception with IFH is still possible when reception with conventional frequency-hopping is not. This approach increases the digital complexity of the system, but reduces the analog problems. As VLSI technologies continue to progress, this tradeoff is increasingly demanded, particularly for low-power VLSI applications.
Another novel FH synthesizer technique is proposed by Lopelli et al. [26]. This technique is based on digital frequency pre-distortion and this approach reduces the complexity of the hopping synthesizer. Significant communication robustness is achieved on the receiver side using an offset insensitive demodulation algorithm and DSP techniques to overcome non-idealities in the transmitted spectrum. The architecture proposed in [26], requires simple digital techniques and low-complexity, low-frequency analog building blocks, based on frequency pre-distortion. In this approach, the incoming data, together with the desired hopping code, addresses a particular cell in the ROM which has been split into two blocks depending on the modulation bit. In each of the memory cells, the pre-distorted word is stored that will drive the DAC with a pre-defined data bit. The DAC then directly drives the varactor array, changing the capacitance and therefore the VCO oscillation frequency according to the desired frequency bin and data.

1.4 Objectives of the study

In order to design the proposed FHSS transceiver and address the challenges associated with the design process, a four-staged approach as presented below was followed.

1.4.1 Identification of functional requirements

The design of a frequency-hopped spread spectrum transceiver requires at least a minimum set of standard specifications. The proposed transceiver system should be able to spread an incoming data signal into a wide band signal and also retrieve the original data signal from the spread spectrum signal. To achieve this, existing literature was studied and analyzed to identify the functional requirements. A consolidated list of the requirements were worked out for the proposed transceiver and is presented below.

The transceiver system must–

- accept an incoming binary signal
- spread this signal into a wide band signal by using frequency hopping
- allow the user to select the frequency hopping sequence
- accept an wideband incoming FHSS signal
- despread this signal using the correct frequency hopping scheme
- designed for standard CMOS process technology
- complete system and subsystems must be evaluated by SPICE, PSPICE or HSPICE

1.4.2 System specifications

The following list presents the general system specifications for the proposed frequency hopped spread spectrum transceiver.

- Fast frequency hopping (FFH) will be used where there are several symbols per hop that is, FFH transmits one or multiple symbols over each frequency i.e., $T_c = kT_s$, where k is some integer.
- No intermediate frequency (IF) will be used for mixing of data signal. The input signal will be baseband signal and will be directly converted to high frequency signal to be transmitted by the transmitter.
- The output signal at the receiver must have a BER of less than 10^{-3}.
- The FHSS modulator and demodulators will not employ band pass filters. These filters are required by systems implementing antennas and hence outside the scope of this thesis.
- The output power of the proposed transmitter will not be high enough to drive an antenna without adding external power amplifier. The specifications of the power amplifier depends upon the transmission system employed and hence outside the scope of this thesis.
- The hopping sequence will be user selectable as a particular PN sequence of length 15.

- Four channel transmission will be implemented where the channel bandwidth is around 1.25 MHz.
- Only four forward channels will be supported.
- The data signal will be directly wide band modulated and no overhead or error correction information will be added.

1.4.3 Identification and design of sub-circuits

Existing literature was studied and analyzed in order to arrive at a new functional frequency-hopped spread spectrum transceiver architecture. The list of major digital and analog sub-circuits those are proposed to be designed and validated through simulation in this work are as listed below.

Digital Sub-circuits:

- Input data signal generator representing the data coming out from four different channels.
- PN sequence generator for providing user selectable PN sequence of length 15.
- PN sequence selector to facilitate selection of appropriate sequence based on incoming data from the four channels.
- Serial-to-parallel converter which will convert the serially out PN sequence into two-bit parallel output.
- Digital-to-analog converter which will convert the two-bit parallel outputs of serial-to-parallel converter into corresponding analog voltage levels.
- Analog-to-digital converter to convert the analog output of the frequency-to- voltage converter at the receiver.
- Analog-to-digital converter to convert the analog output of the FVC at the receiver end into digital signal.
- Correlator which will correlate the received digital signal with locally generated PN sequence.
- Decoder which will decode the received data into original digital data at the receiver.

Analog Sub-circuits:

- Voltage controlled oscillator which will generate sinusoidal signals of four different frequencies corresponding to four analog voltage levels available at the output of DAC at the transmitter.
- Low noise amplifier as RF front-end at the receiver.
- Frequency-to-voltage converter which will convert the output of the LNA into analog voltage levels based on the input signal frequency. We must get four analog voltage levels corresponding to the four different frequencies generated by the VCO at the transmitter.
- High pass active filter which forms part of the FVC at the receiver.
- Logarithmic and anti-logarithmic amplifiers which form part of the precision rectifier used to construct the FVC.
- Differentiator and Integrator circuits to be employed in the proposed precision rectifier.
- Square rooting circuit to be employed in constructing the rectifier.
- Comparator to compare the incoming PN sequence with locally generated PN sequence at the receiver.

1.4.4 Validation through simulation

The problem to be addressed by this thesis is mainly an RFIC design problem and the circuits and subcircuits designed will be validated through simulation. The analog and digital subsystems of the transceiver will be designed and simulated under the following simulation environment.

1.4.4.1 Simulation environment

Any new electronic system needs to be established by validation through simulation. The transceiver system proposed in this thesis is required to operate in the gigahertz regime and hence "AWR Microwave Office", which is a user friendly EDA tool with all of the possibilities necessary for accurate modeling of microwave components and circuits provides the simulation environment. It contains a linear, non-linear, harmonic-balance, time domain, EM simulation and physical layout viewer. HSPICE [27], the latest time domain solver is also incorporated in this tool. An accurate and extensive list (library) of circuit elements are also provided, which is an important requirement for accurate modeling [28]. This EDA tool is also well-known for supporting a good number of CMOS processes.

1.5 Major contributions of this thesis

In this work attempt was made to develop a fully integrable CMOS FHSS transceiver architecture for wireless communication applications. In the transmitter, the VCO directly converts the four available analog voltage levels to the corresponding frequencies to be fed to the power amplifier for onward transmission. In the receiver, an FVC is employed to convert the four signal frequencies to the corresponding analog voltage levels for subsequent processing leading to the recovery of the transmitted signals from the four channels. The major contributions of this thesis may be summarized as follows:

- The efforts made towards the design of a frequency independent 90^0 phase shifter which was required by the FVC employed in the receiver section resulted in the development of a novel precision rectifier, now known as *Pythagorean rectifier*. The precision rectifier architecture was implemented using discrete components and validated experimentally. Thus, we realized a novel precision full-wave rectifier using an all-pass filter as a 90^0 phase shifter. The circuit gives a d.c. output voltage that is almost the same as the peak input voltage over a frequency range of 50 Hz to 1 MHz with a very low ripple voltage and low harmonic distortion. Oscilloscope traces of the rectified waveform for the proposed circuit show a ripple voltage of $\sim$ 12mV obtained with an input voltage of amplitude $\sim$ 1 V and frequency 100 kHz.

- The above precision rectifier architecture was modified to overcome some of the drawbacks such as frequency dependency and the design was simulated using CMOS technology in order to achieve a fully integrable frequency independent precision rectifier for low power and at the same time high frequency applications.

- The precision rectifier proposed in this work employs differentiator and integrator circuits and in order to accomplish these, we designed two high frequency two-stage operational amplifiers, one using CMOS and the other using BiCMOS technology in order investigate their performances at multi-gigahertz regime. The performance parameters such as gain, frequency response, phase margin, CMRR, PSRR, power consumption etc achieved are compared and it was found that, as far as two-stage op amp is concerned, CMOS technology is more suitable candidate than its BiCMOS counterpart particularly for low power RF design.

- We have also implemented a two stage operational amplifier architecture using CMOS technology suitable for low power RF applications. The circuit was designed by using RF model of BSIM3v3 using CMOS technology. In the closed loop configuration the proposed op amp was found to offer a gain of 22.69 dB, a unity gain bandwidth of more than 11.31GHz, a phase margin of nearly 45^0. The slew rate of the op amp was found to be 39.21V/ns while the power consumption

was 83.8mW. All these attributes associated with the proposed op amp makes it suitable candidate for low power RF applications.

- A fully integrable current starved voltage controlled ring oscillator (CSVCRO) was designed to employ in the transmitter section. The VCO architecture proposed and designed for this work provides high linear relationship between oscillation frequency ranging from 0.7 ∼1.75 GHz over a control voltage ranging from 1.2 to 2V and results in a large tuning range of 75%. The phase noise achieved is −88 dBc/Hz at an offset frequency of 1 MHz. The linear frequency sweep is obtained without employing any additional compensation techniques resulting in less circuit complexity, die area and power consumption.

- A CMOS low noise amplifier with L-type input matching network and π-type output matching network, operating within the bandwidth of $0.9 \sim 6$ GHz was designed for the receiver section. The input L-type matching network was used to fix the Q factor whereas the output π-type matching network provides an extra degree of freedom to adjust the bandwidth. It is seen from the simulation results that the gain of ~ 22.7 dB for the frequency range of $0.9 \sim 6$ GHz and noise figure (NF) of < 2.5 dB are obtained and found to be reasonably good in comparison to the reported works.

- Another important outcome of this study is the project proposal "Design of an Ultra-low power FHSS Spread spectrum Transceiver for Wireless Communication Applications" that was accepted and approved by Indian Space Research Organisation (ISRO) involving a fund of Rs. Twenty nine lakh and fifty thousand.

Apart from the above contributions, the following analog, digital and mixed signal circuits were also designed using high speed CMOS technology and simulated in order to complete the system:

- 4-bit data generator
- PN sequence generator
- 8 : 1 multiplexer
- Parallel-to-serial (P2S) and Serial-to-parallel (S2P)converter
- Analog-to-digital (ADC) and Digital-to-analog converter (DAC)
- Logarithmic and Anti-logarithmic amplifier circuits (high speed)
- Voltage Comparator circuit
- Frequency-to-voltage (FVC) converter etc.

Although the performances of the above circuits are are not compared with the literature and yet we believe these too add to our contributions.

1.6 Organization of the Thesis

The work proposed in this thesis has been presented in seven chapters. This section briefly describes the flow of presentation of the proposed work.

Chapter 1 introduces the research problem and also defines the major objectives of the work proposed.

Chapter 2 is about review of wireless communication in general. Evolution of wireless communication technology from 1G to 4G has been incorporated in this chapter. Spread spectrum communication systems have also been reviewed in this chapter with special emphasis on frequency hopping spread spectrum communication. Available literature survey on frequency hopped transceiver architecture was carried out in order to find out some generality based on which a new yet efficient architecture could be proposed.

Chapter 3 is about review of basic radio frequency circuit design using CMOS technology. RF CMOS devices, both long channel and short-channel have been incorporated in this chapter along with a brief review of RF MOSFETs.

The aim of Chapter 4 is to identify, design and simulate the various analog, digital and mixed signal subsystems required by the proposed transmitter. A brief summary of MOSFET models, process parameters, design of digital and analog cells using MOSFETs are incorporated in this chapter.

Chapter 5 is about the receiver. Various sub-circuits of the proposed receiver were identified, designed using CMOS technology and validated through simulation.

System integration and performance evaluation of the proposed frequency-hopped spread spectrum transceiver is presented in chapter 6.

Chapter 7 presents some of the readily visible future scopes and concludes the present work.

Chapter 2

Review of Wireless Communication Systems

2.1 Introduction

The word "wireless"was originally coined by Guglielmo Marconi. Radio communication is nearly 100 years old and not a contemporary invention as it appears today. The most important breakthrough for modern mobile communication was the concept of cellular mobile communication system developed by AT & T Bell Laboratories during 1970s [29]. In this direction, the rapid growth of integrated circuit technology has enabled us to produce low cost, efficient and more reliable cellular hand sets, radio, television and other wireless devices. Most importantly, the appliances which had earlier wired control now use radio link [30]. The appliances that use radio link in stead of wired control were termed as "wireless"and the term stuck.

The tremendous popularity of wireless systems in recent years has led to the commoditization of RF transceivers (radios) whose prices have gone down dramatically. The relatively lower cost allows us to consider having two or more radios in the same device. Wireless systems that use multiple radios in a collaborative manner dramatically improve system performance and functionality over the traditional single radio wireless systems that were popular in the recent past.

The explosive growth of mobile and wireless communication that took place during the last decade has radically changed the life of people with the migration of wireless communication from voice-centric to data-centric. Mobile communication has gone through evolutions from first generation (1G) analog system to third generation (3G), fourth generation (4G) technologies being available now. Evolution of wireless network has also taken place from low speed Local Area Networks (LAN) to Broadband Wireless LANs, Wireless Metropolitan-Area Networks (MANs), Wireless Wide-Area Networks

(WANs), Wireless Personal-Area Networks (PANs)[31, 32] and so on. Broadband wireless data service has also expanded leading to Satellite TV broadcasting and Regional Area Networks for Digital TV. The data rate has also increased from 10kbps to 1Gbps for 4G networks. Apart from all these, the 4G network is expected to provide services never seen before [33–35].

2.2 Block diagram of communication system

Communication systems transmit information or data from one point to another. A general digital communication system block diagram is shown in Fig.2-1. This communication system also represents remote sensing systems like radar and sonar in which both transmitter and receiver are located at the same place. Analog signals such as au-

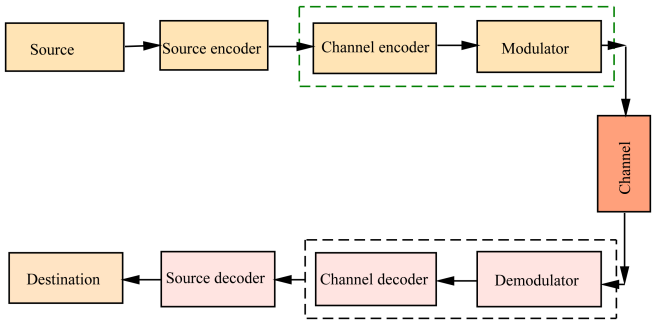


Figure 2-1: General communication system block diagram

dio, speech, image or digital data such as text or multimedia are generated at the source. The source encoder converts the input data into binary data which is subjected to the channel encoder so that the binary data sequences can be reliably reproduced at the receiver. The stream of channel encoded data is then modulated to generate waveforms for transmission over the channel which is a physical or radio link. The above procedure is reversed at the receiver to finally restore the original source of information. There are three types of commonly used channels such as wireless channels, optical channels and guided wave channels. The atmosphere or the free space may be the wireless channel. Coaxial cable dominated the guided wave channels for some time which is now being replaced by optical fiber, which is a special type of guided-wave channel.

2.3 Wireless Communication Systems

An explosive growth in wireless communication systems has taken place over the last two decades. Wireless communication systems have migrated from first-generation narrow band analog systems (1G) to second-generation narrow band digital systems (2G) and

to the current third-generation wide band multimedia systems (3G), future or fourth generation (4G) being available in the near future as shown in Fig.2-2.

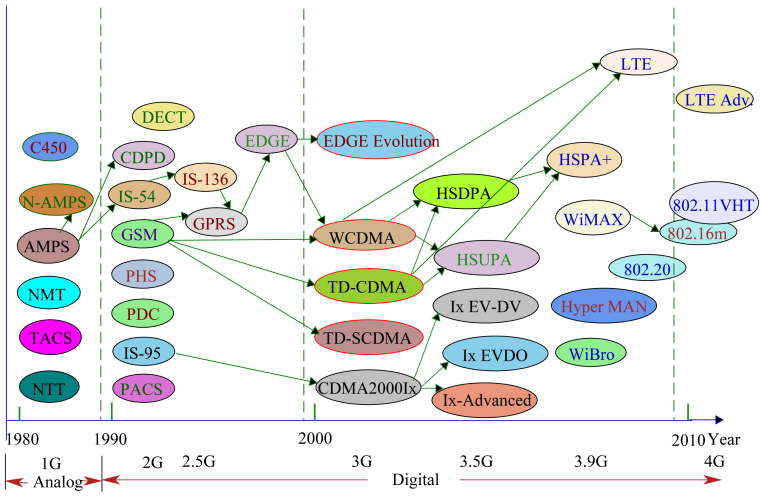


Figure 2-2: Evolution of mobile communication systems

2.3.1 First-generation systems (1G)

The first-generation (1G) mobile systems were based on analog systems which covers voice communication systems deployed before 1990 in the frequency band 450 MHz to 1GHz [36]. They employ frequency division multiple access (FDMA) coupled with frequency division duplexing (FDD). In 1G system, analog frequency modulation is used for speech modulation while frequency shift keying (FSK) is used for control signaling. The cell radius is within the range of 2 km to 40 km. Due to the use of FDMA/FDD in 1G systems, each user needs to occupy two frequency bands, one for uplink and the other for downlink demanding one transceiver for each band. The 1G system gained popularity all over the world although they suffer from shortcomings like small coverage area, poor speech quality, poor battery performance etc. Introduction of digital communication has almost eliminated these shortcomings resulting in the 2G system.

2.3.2 Second-generation systems (2G)

The second-generation systems were introduced in the early 1990s. They were based on circuit switched data communication and provide wire-line quality digital voice services [32, 33]. The digital implementation of 2G systems employed new access techniques-time-division multiple access (TDMA) and code-division multiple access (CDMA). Apart from 2G cellular systems, wireless LAN, satellite radios and 2G cordless phones were also introduced during this period. Many 2G standards were developed during this period

but Global System for Mobile Communication (GSM) and Interim Standard-95 (IS-95) were the most dominant among all others [37] as shown in Fig.2-2. The typical operating frequency band for these standards is 900 MHz to 1.9 GHz. The migration of 2G to 3G started with the deployment of General Packet Radio Service (GPRS) over GSM and IS-136. GPRS made a transition from circuit switched data to packet switched data resulting in an increase in data rate from 9.6 kbps to 38.4 kbps. The introduction of Enhanced Data for GSM Evolution (EDGE) which is a convergence of GSM and IS-136, further enhanced the data rate to 384 kbps.

2.3.3 Third-generation systems (3G)

The third-generation cellular systems are being deployed worldwide. International Telecommunication Union (ITU) developed the 3G standard under the name International Mobile Telecommunication-2000 (IMT-2000) or Universal Mobile Telecommunication System (UMTS) [38]. The 3G system (3G, 3.5G, and 3.9G) is a wide band communication system and as a general requirement, it demands a data rate of 2Mbps at stationery mobile, 384 kbps at pedestrian speed and 144 kbps in moving vehicle. The 3G system is targeted to be a global system with global roaming. It is based on packet switching and deployed in the 2GHz frequency band. The two main 3G standards are Wideband CDMA (WCDMA) and CDMA-2000 which are administered by Third Generation Partnership Program (3GPP) and Third Generation Partnership Program-2 (3GPP2) of ITU respectively. The WiMAX (802.16e) has been recently included in the ITU-2000 suit and is now a strong contender of WCDMA and CDMA-2000.

2.3.4 Fourth-generation systems (4G)

Active research is ongoing in 4G mobile radio systems and ITU-R has defined IMT Advanced for 4G systems targeting peak data rate of about 100 Mbps for highly mobile (at speeds up to 250km/hr), 1Gbps for pedestrian speed or stationery access. The development of IMT-Advanced [39] is nearing its completion and expected to be deployed by 2015. The following enabling technology features are supposed to be present in 4G wireless systems.

- Ubiquitous, mobile and seamless communication.
- Downlink data rate of 100 Mbps at stationary conditions and 100 Mbps at 250 miles/hr in wide coverage area.
- Data rate of 1Gbps at stationery conditions at local area.
- High capacity with spectral efficiency of the order of 10 bits/s/Hz.

- Internet based mobility with IPv6 [40].
- Smart spectrum with dynamic spectrum allocation within 3 to 10GHz band [41].
- Quality-of-Service (QoS) driven [42, 43].
- Dynamic soft channel management [44].

The 4G system will provide TV and movies on a moving cellular phone. Both mobile cellular and wireless networking functions will be integrated in 4G systems. The main technique to be used in 4G systems is OFDM because it is possible to combine OFDM with CDMA or TDMA or can be extended to OFDMA for multiple access. Following are some of the enabling technologies for 4G systems:

- 4G system requires a wide variation of adaptive RF bands, data rates, BERs, channel access modes and power control [40]. These can be achieved by software-defined radio. Another requirement of 4G system is seamless adaptation of radio access techniques, which can also be achieved by software-defined radio.
- Dynamic spectrum management and real time band allocation for each user is performed by cognitive radio [45].
- The most suitable modulation and coding scheme is selected jointly by adaptive modulation and coding (AMC) based on channel conditions.
- A high spectral efficiency is achieved by using MIMO or multiple antenna techniques.
- Hybrid-ARQ (HARQ) which combines the advantages of ARQ and channel coding, increases the throughput.

In addition to the above, spectrum flexibility and multi-hop relaying are found to be useful in extending the spectrum range for high data rates [40]. Some of the above techniques are incorporated in 3G systems like WiMAX, IEEE 802.20, CDMA 2000, $3GPP2$ UMB etc. Fig.2-2 demonstrates the evolution of mobile communication systems [41, 42].

2.3.5 Satellite Communications

Apart from the above, satellite communication which is another type of wireless communication has become popular due to its wide coverage area achieved through deployment of satellites. The satellite communication concept was first suggested by Arthur C. Clarke in 1945 [46]. The concept was realized when the USSR launched Sputonik-I in

1957 and the USA launched SCORE in 1958. Mobile satellite communication employs low earth orbit (LEO) satellites so that time delays can be kept at minimum possible values. There are another two types of satellite communication systems, medium earth orbit and geo-stationery orbit. Apart from being a stand alone wireless system, mobile communication systems can also be integrated with terrestrial mobile systems.
Mobile satellite networks have become a crucial component of future global communication infrastructure and are intended to complement and extend the existing terrestrial systems to provide global coverage. Satellites are also used for broadcasting purposes as seen in Digital Video Broadcasting System (DVB-S). Satellite broadcasting systems can tolerate longer time delays and hence geostationary earth orbit (GEO) satellites are employed in broadcasting systems. GEO satellites are deployed at an altitude of $35,786$ km above the equator line and one satellite covers one-third of the earth.
Global Positioning System (GPS) is another highly popular satellite communication application. It has attracted the interest of military as well as consumer market due to its capability of determining the position of the user with high level of accuracy. The propagation delay which is a potential source of error in GPS system is accurately tracked by employing spread spectrum tracking technique. The GPS system has altogether 24 satellites in circular orbits at a height of $12,211$ miles above the earth [44]. Eight satellites in each of the three orbits are inclined at an angle of 55^0 with respect to the equator and are separated by 120^0. The orbital period of each satellite is 12 hrs and each satellite uses two carrier frequencies 1572.42 and 1227.60 MHz. Any point on the earth is visible by at least four satellites at any given time.

2.4 Wireless Communication Spectrum

Electromagnetic waves in the frequency range 3Hz to 3000 GHz, called radio waves, are extremely widely used in modern technology, particularly in telecommunication. To prevent interference between different users, the generation and transmission of radio waves is strictly regulated by national laws, coordinated by an international body, the International Telecommunication Union [47].
The frequency band from 1MHz to 30GHz as shown in Fig.2-3 nearly covers all the wireless devices excluding the devices those are controlled by infra-red. The RF portion of this spectrum provides better radio communication properties with minimum engineering efforts and resources. The modeling of RF devices, circuits and antennas is relatively easier and simpler in this band compared to higher frequency bands. As a result, most of the radio communications are accommodated in this band making it the most crowded one in the spectrum. As a result of this spectral crowding, continuous efforts are being made to push the boundaries of spectral power, coding techniques etc. to maximize the information throughput yet utilizing minimum spectrum.

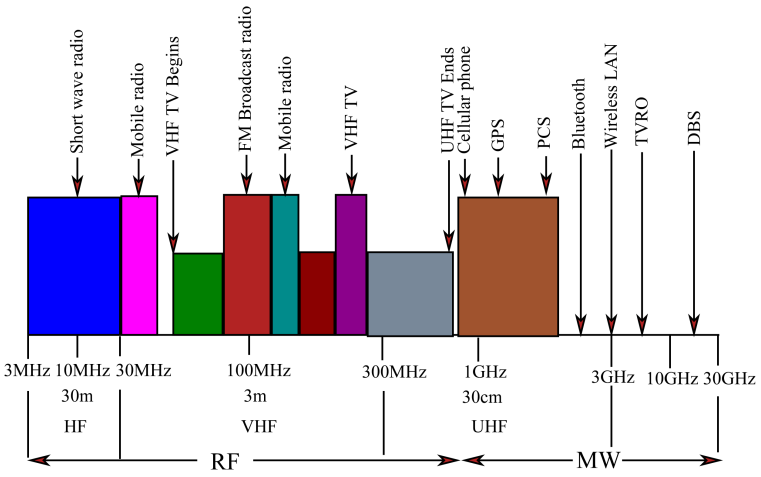


Figure 2-3: Electromagnetic Spectrum for Radio and Microwave

2.5 Spread spectrum communication

Spread spectrum communication technique was originally used by military for military guidance and communication systems mainly for the purpose of interference rejection and enciphering. By the end of World War-II, use of spread spectrum for jamming resistance became a popular concept. Further investigation of spread spectrum was primarily motivated by the need of highly jamming resistant communication systems [2]. As a result, many other applications of spread spectrum like energy density reduction, high resolution ranging and multiple access have emerged. This system is called spread spectrum because of the fact that the transmission bandwidth is much higher than the minimum bandwidth required for transmission of the information. In cellular digital communication, spread spectrum modulation scheme is used as a multiple access technique [17].

There are two types of spread spectrum schemes-i) Direct sequence Spread Spectrum (DSSS) and ii) Frequency Hopping Spread Spectrum (FHSS). In direct DSSS, data is spread while the carrier frequency is kept fixed. In FHSS, the data is directly modulated and the carrier frequency is hopped by channel hopping. In spread spectrum communication, spreading of the spectrum is achieved by either of these two schemes [3]. Apart from these two spreading techniques, there exists another spreading technique known as time hopping spread spectrum (THSS) in which signal transmission is randomized in time.

The first two modulation schemes are called spectral spreading while the time hopping is known as temporal spreading. Temporal hopping has the advantages of reduced interference, time diversity and low instantaneous signal power of the transmitted signal while frequency diversity, low power spectral density (PSD) of the transmitted signal and reduced band-limited interference can be achieved by spectrum spreading.

Spread spectrum techniques provide a number of advantages such as resistance to eaves-

dropping, resistance to multipath fading, interference rejection and multiple access capabilities. The interference rejection capability of a spread spectrum system can briefly be described with reference to Fig.2-4 shown below:

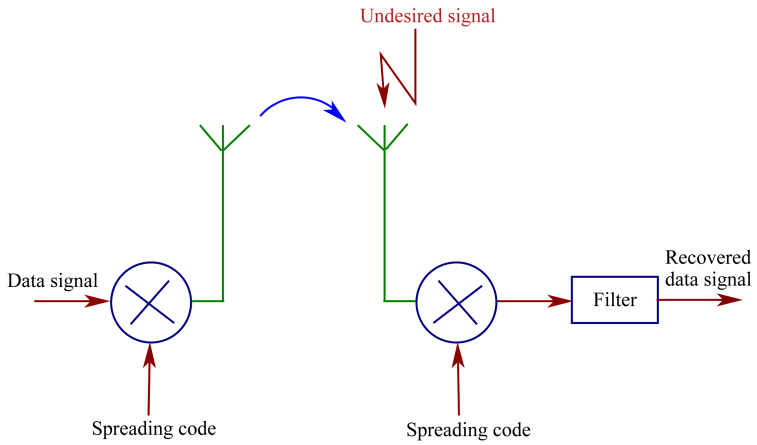


Figure 2-4: Basic spread spectrum technique

- At the transmitter end the data signal is multiplied by the spreading signal once to spread the signal.
- At the receiver the received signal is multiplied by the spreading code once more which is followed by filtering for recovery of the data signal.
- Thus, the data signal gets multiplied twice while the undesired signal mainly introduced by the channel, gets multiplied only once.

2.5.1 Spreading sequences

A spreading sequence is a periodic deterministic sequence given by $c = \{c_k\}$, with a finite period N. The duration of each c_k is the chip period T_c. The spreading waveforms are generated by spreading sequences using a real chip amplitude shaping function having peak amplitude of unity. For a given symbol duration T, the chip duration T_c should be chosen so that T is an integer multiple of T_c. The processing gain or spreading factor is then defined by

$$G_p = {}^{T}/_{T_c} \tag{2.1}$$

The spreading code is called *short code* when $G_p = N$ and *long code* when $G_p << N$. In a short code, each data symbol is spread by full period of the spreading sequence while each data symbol is spread by a portion of the spreading sequence in a long code. The length of a code is the period of that code. Assuming a short code, the code length may be defined as $G_p T_c$ that is G_p. The two codes, c_i and c_j are orthogonal if their

cross-correlation function (CCF) over the period of the code is zero.
That is,

$$CCF\,(i,j) = \int_{0}^{G_p T_c} c_i\,(t)\; c_k\,(t)\, dt = 0, \quad \text{for} \quad i \neq j \tag{2.2}$$

The orthogonality property of spreading codes permits multiple information streams to be multiplexed for onward transmission.
The process of data recovery from the composite spread spectrum signal by applying the same CDMA code that is used for spreading is called de-spreading. To obtain the original data by correlation, the auto-correlation function (ACF) of the spreading sequence must be a Dirac delta function. The desired ACF at a given time iT_c is given by

$$ACF(i) = \begin{cases} G_p, & i = 0 \\ 0, & otherwise \end{cases} \tag{2.3}$$

The receiver achieves a finite interference suppression factor of ACF/CCF for non-orthogonal spreading sequences.
Spreading codes are selected on the basis of the following factors:
Autocorrelation: This property helps to de-spread the original code perfectly and to mitigate the ISI. It is also helpful in synchronization and reduction of interchip interference in a rake receiver.
Cross-correlation: This property ensures all the codes to be orthogonal so that all other users' information is demodulated as noise at the receiver. Orthogonality between the codes must be guaranteed for unsynchronized systems with arbitrary delay.
Number of codes: A large number of codes can support large number of users since all users in cell and in the surrounding cells must have different codes to identify them.
The popular spreading sequences used for uplink in the CDMA systems are the m-sequence, Gold sequence and Kasami sequence. All of the above sequences have good cross-correlation property. The m-sequence, apart from having good ACF property, also provides $(2^{\mathrm{m}} - 1)$ codes. The Gold sequence, which is obtained by a subset of m-sequences, can have $(2^{\mathrm{m}} + 1)$ number of codes. The Kasami sequence can also have a large number of codes.

2.5.2 Pseudo-noise (PN) sequence

Pseudo-noise (PN) sequences can be used as spreading codes although PN sequences of any given length are not always orthogonal to one another. Typically, maximum length shift register (MLSR) is employed to generate PN sequences and hence PN sequence is also called m-sequence. The block diagram of MLSR sequence generator is shown in Fig.2-5. At each instant of time, the register right shifts its content by one bit. The addition used is a modulo-2 addition. The output equation of the PN sequence generator

is given by

$$a_n = c_1 a_{n-1} + c_2 a_{n-2} + ... + c_r a_{n-r} = \sum_{i=1}^{r} c_i a_{n-i} \tag{2.4}$$

where, $(c_1, c_2, \ldots, c_r)$ are connection weights with 1 for connection and 0 for no connection, a_i's are the bits in the register. The maximum period of the generated sequence is $(2^m - 1)$ where, m is the number of stages of the shift register. The length of an

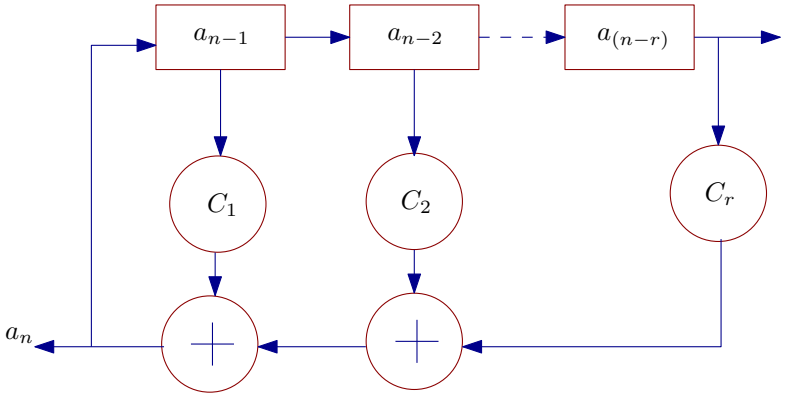


Figure 2-5: MLSR sequence generator

m-sequence is always odd and is given by $(N = 2^m - 1)$. The m-sequence satisfies all the three properties of a random sequence [48] as described below.

Balance property- In order to achieve good balance, the number of binary ones in each period of the sequence should differ from the number of binary zeros by at most one digit. That is, out of the total length of $(2^m - 1)$, (2^{m-1}) bits should be 1 and $(2^{m-1} - 1)$ bits should be 0, since the case of all zero is prohibited.

Run property- A run is a sequence of single type of binary digits. The length of the run is the number of digits in the run. It is desired that in each period, one-half of the runs of each type are of length 1, about one-fourth are of length 2, one-eighth are of length 3 and so on. In other words, the probability of n continuous 0 or 1 is $1/2^n$, for $n \leq m - 1$ and $1/2^{m-1}$, for $n = m$.

Shift property- If the sequence gets shifted by any number of non-zero elements, the resulting sequence shall have half of the elements same as in the original sequence and the other half different from the original sequence.

The m-sequence is a cyclic code which can be generated and characterized by a polynomial called generator polynomial. It can be analyzed by algebraic coding theory. The autocorrelation property of an m-sequence with period N approaches very close to the desirable case given by

$$ACF(i) = \begin{cases} N, & i = kN \\ -1, & i \neq kN \end{cases} \tag{2.5}$$

where, k is any integer. The m-sequences are ideal for minimizing the ISI effect because their normalized $\overline{ACF}(i) = ACF(i)/ACF(0)$ very closely approaches to the delta function $\partial(i)$ for large values of N. The m-sequence provides a suppression factor of $ACF/CCF = N$. A pair of m-sequences exists for each m with CCF's, -1, $-t(m)$, and

$t(m) - 2$ where

$$t\,(m) = \begin{cases} 2^{(m+1)/2} + 1, & for \quad m \quad \text{odd} \\ 2^{(m+2)/2} + 1, & for \quad m \quad \text{even} \end{cases} \tag{2.6}$$

This pair of m-sequences for which the above three valued CCF's exist, is known as *preferred-pair of m-sequences*. The number of m-sequences for an MLSR of length m is given in [2] which is much smaller than its sequence length and unable to provide sufficient number of codes for CDMA applications. The maximum cross-correlation levels are also very large and hence it cannot be used alone in CDMA systems.

Gold sequences

The preferred-pair of m-sequences are used to generate Gold sequences by a process of all possible cyclically shifted modulo-2 additions of the preferred pair [5, 49]. Since preferred-pair is used, both auto-correlation and cross-correlation of Gold sequence takes on the values $\{-1, \ -t\,(m)\,, \ t\,(m) - 2\}$, where $t(m)$ is given by eqn.(2.6) [50]. Gold sequences have lower peak cross-correlations than m-sequences and worse auto-correlation property than m-sequences. The preferred-pair along with the family of $2^m - 1$ derived sequences are collectively known as Gold codes. For two m-sequences of order m, there are $(2^m + 1)$ Gold codes which are balanced with (2^{m-1}) ones and $(2^{m-1} - 1)$ zeros. The Gold code finds extensive applications in spread spectrum communication systems such as IS-95, WCDMA, UTRA-TDD, GPS, Satellite systems etc.

If an additional 0 is attached to the original Gold code, the cross-correlation can be changed from -1 to 0, since the Gold code has cross-correlation of -1 for many of its offsets. Thus, from a preferred pair of two r-stage MLSRs, a total of $2r$ orthogonal Gold codes can be obtained by zero-padding. Orthogonal Gold codes have better auto-correlation property than Walsh code but same cross-correlation property. Orthogonal Gold codes have been used in WCDMA for fast cell search.

Kasami sequences

The Kasami sequences [51, 52] have properties similar to those preferred pairs of m-sequences. They are also generated from m-sequences in fashion similar to that of Gold sequence. Let us consider two m-sequences with periods (2^{m-1}) and $(2^{m/2} - 1)$ are generated from two preferred polynomials $p_1\,(x)$ and $p_2\,(x)$ of order m and $m/2$ respectively. The Kasami sequences are generated by using the long sequence and the sum of long sequence with all $(2^{m/2} - 1)$ cyclic shifts of the short sequence [53]. Hence, the number of Kasami sequences is $2^{m/2}$, each with a period 2^{m-1}. This is known as the small set of Kasami sequences which has $2^{m/2}$ binary sequences of period 2^{m-1} for even m. The off-peak auto-correlation and cross-correlation of Kasami sequences also takes three values $\{-1, \ -t\,(m)\,, \ t\,(m) - 2\}$ where,

$$t\,(m) = 2^{m/2} + 1 \tag{2.7}$$

The large set of Kasami sequences has inferior auto-correlation and cross-correlation

properties as compared to those of small set but it provides a large number of codes.

Walsh sequences

The Walsh code or the Walsh-Hadamard codes are generated by rearranging the Hadamard codes. The Walsh codes and the Hadamard codes are orthogonal to each other and the k-bit Walsh codes can be generated recursively by using

$$B_{n+1} = \begin{bmatrix} B_n & \vdots & B_n \\ \cdots & \cdots & \cdots \\ B_n & \vdots & \overline{B_n} \end{bmatrix} \tag{2.8}$$

The recursion starts from $B_0 = 0$ or 1 and each of the rows of the matrix can be used as a code. The length and also the number of codes can be $2, 4, \ldots\ldots, 2^k$. The correlation of two Walsh codes is non zero only when they are same. The Walsh code can be generated by the Walsh-Hadamard sequence generator [54]. The Walsh codes have perfect orthogonality. When Walsh codes are applied in multi-path channel, there will be interference between users because of the fact that the orthogonality gets destroyed due to delay dispersions in a multi-path environment. The major drawback of Walsh codes lies in the fact that the codewords have poor auto-correlation property. This can be addressed by multiplying the Walsh codes by a scrambling code which improves auto-correlation property without affecting orthogonality. The Walsh codes are used mainly to separate the users completely. The number of Walsh codes is very limited and hence insufficient to be assigned to all users of a given cell and its neighboring cells. This problem is eliminated by multiplying the Walsh code by a scrambling code since the orthogonality of the resulting codes does not change. The first sequence in Walsh code is all-zeros sequence and it provides highest possible auto-correlation given by $ACF\,(n) = N - n$, where N and n are the length of the sequence and number of bit shifts respectively. The all-zero sequence is used as a pilot sequence for the above auto-correlation property.

Barker sequences

A binary sequence whose ACF's have off-peak values 1, 0, or -1 is known as Barker sequence. The Barker sequences excluding their negations and reversals are:

$++-$ length3

$+-++$ and $+---$ length4

$++\,+-+$ length5

$++\,+--+-$ length7

$++\,+---+--+-$ length11

$++\,+\,+\,+--++-+-+$ length13

where, a positive sign represents a positive pulse and a negative sign represents a negative pulse. The Barker sequences of length 11 and 13 are found to have highest auto-correlation property among all the binary codes [5, 52]. Barker sequences are used in

paging systems for word synchronization and the length-11 Barker code is used in IEEE 802.11.

2.5.3 Direct-sequence spread spectrum

Direct sequence spread spectrum (DSSS) is one of the two most widely used spread spectrum systems. In DSSS, the spreading of the information signal is performed at baseband by multiplying the baseband data signal with a spreading sequence. The spreading sequence is essentially a pseudo-random sequence with pulse duration T_c and chipping rate of $R_c = 1/T_c$. Each of the pulses is called a chip and T_c is the chip interval. Given the information symbol duration T_s and symbol rate $R_s = 1/T_s$ is much less than the pulse duration of the information symbol. In other words, $T_c << T_s$. In practice T_s has to be an integral multiple of T_c and the transition of data symbol and chip must occur at the same time. The number of chips in one symbol is referred to as processing gain or spreading factor and expressed as the ratio of $G_p = T_s/T_c$. In other words, processing gain is the ratio of spread bandwidth of the transmitted data to the data rate. Thus, spreading increases the bandwidth by a factor of G_p. Apart from this, processing gain also allows the removal of $(G_p - 1)$ interfering signals from other users. DSSS involves modulo-2 addition of the information signal $d(t)$ and the pseudo-noise sequence $c(t)$ with a higher frequency to produce the spread spectrum signal $T(t)$. The spread signal can be despread back to the original signal $d(t)$ by modulo-2 addition of $c(t)$ with spread signal $T(t)$.
The chip duration of the PN sequence is so chosen so that the data signal is spread over the maximum available bandwidth of the channel. Since a rectangular pulse $g(t)$ of length T, has a null bandwidth $B_{nn} = 2/T$, therefore, for a given channel bandwidth W, we have $T_c = 2/W$ or $R_c = W/2$. This means, the chipping rate is half the channel bandwidth. Higher chipping rate is also achievable but at the cost of complex techniques. Despreading of the DSSS signal is performed at the receiver either by multiplying the spreading sequence with the spread signal or by using modulo-2 addition. Fig.2-6 illustrates the spreading and de-spreading process.
The auto-correlation function of the spreading sequence, $c(t)$, is given by

$$R(t) = \int_{-\infty}^{\infty} c(\tau).c(t-\tau)\, d\tau \tag{2.9}$$

Fourier transform of $R(t)$ gives the power spectral density (PSD) of $c(t)$, i.e.,

$$S(\omega) = \Im[R(t)] \tag{2.10}$$

and

$$R(t) = \Im^{-1}[S(\omega)] \tag{2.11}$$

In order to spread the spectrum uniformly, a constant PSD of $c(t)$ is desirable. The

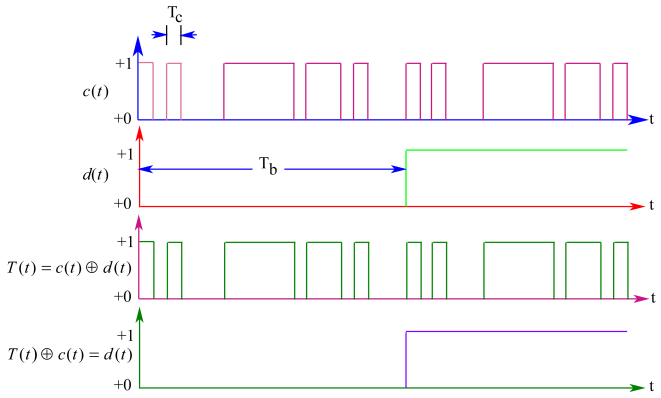


Figure 2-6: DSSS : spreading and de-spreading

auto-correlation function $R(t)$, which is the inverse Fourier transform of $S(\omega)$, is ideally an impulse function $d(t)$ as depicted in Fig.2-7. Practically, $R(t)$ reaches its peak value at $t = 0$. The larger peak values of $R(t)$, the receiver allows more signal-to-noise (SNR) margin resulting in more reliable acquisition and reception of data. To examine how

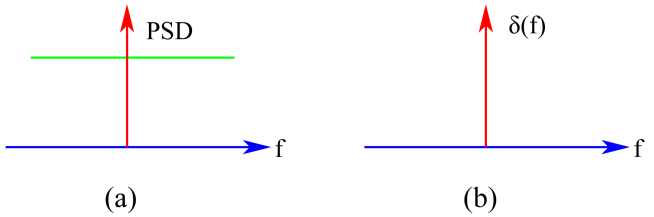


Figure 2-7: (a) Ideal PSD of $c(t)$ (b) Ideal auto-correlation function of $c(t)$

spreading helps suppression of interference, a baseband communication and wideband interference can be considered because of the fact that they are consistent with barrage noise jamming and multiuser applications. Modulo-2 addition of the PN sequence in the transmitter spreads the data over the entire bandwidth available from the channel. Modulo-2 addition of the spread signal with the PN sequence at the receiver provides selective dispreading of the data signal without dispreading the interference signal since it is uncorrelated with the PN sequence and hence continue to occupy the entire bandwidth. The PSD's shown in Fig.2-8 illustrates the technique. If we consider the case

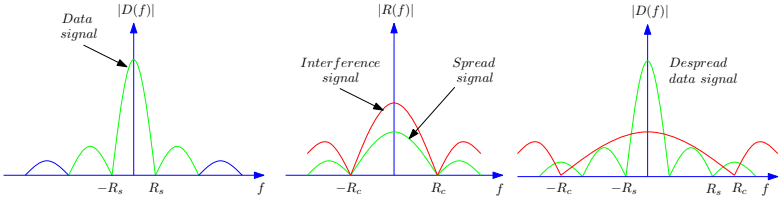


Figure 2-8: Effect of interference on DSSS signal

of only additive white Gaussian noise and no interference, it may be seen that DSSS

provides no advantage. That is, the SNR of the output data remains the same whether spreading is performed or not. The reason is, the noise remains uniform over the entire spectrum even after spreading is performed.
The mainstream technology for 3G mobile communication at present is the DS-CDMA. DS-CDMA has the capability of effectively multiplexing a large number of variable-rate users in a cellular environment. Even though DSSS is used in WCDMA, CDMA-2000, CDMA, it is not a suitable technology for high data rates. With continuous evolution of 3G systems towards higher data rates, DSSS is losing its importance.

2.5.4 Frequency hopping spread spectrum

The frequency hopping spread spectrum (FHSS) is similar to DSSS as far as spreading of the signal over a larger bandwidth than the information bandwidth is concerned. In FHSS, the entire bandwidth is divided into a large number of continuous frequency slots and a PN generator is used to drive a digital frequency synthesizer to hop among the center frequencies of these slots. The hopping pattern of the frequency synthesizer is determined by the output of the PN generator. Fig.2-9 illustrates the hopping pattern of FHSS system in time and frequency domain. In an FHSS system, the spreading effect

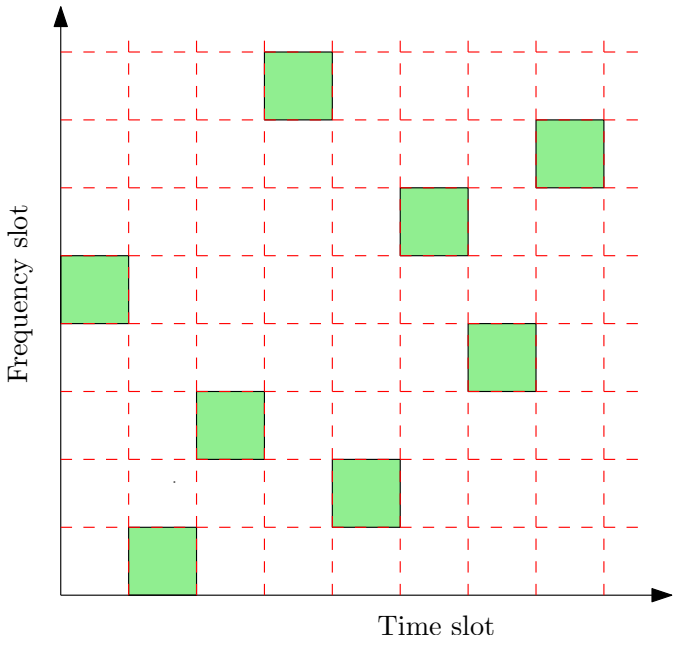


Figure 2-9: Frequency hopping pattern in time and frequency

is achieved by pseudo-randomly hopping the carrier frequency within the available RF band. As in DSSS, the term "chip" means PN code symbol i.e. the shortest uninterrupted waveform present. In FHSS, it refers to the shortest uninterrupted wave form in the system which is the data symbol. The processing gain of an FHSS system is the ratio of

spread signal bandwidth to the information signal bandwidth and can be expressed as

$$G_p = \frac{W_{hopping}}{R_c} \tag{2.12}$$

where, $W_{hopping}$ is the frequency band over which the system hops and the denominator is taken to be the data rate.

Frequency hopping is classified as *fast frequency hopping (FFH)* and *slow frequency hopping (SFH)*. In FFH, the carrier frequency is changed several times during one symbol period. That is, $T_c = T_s/k$, where k is any integer. Thus, FFH spreads each symbol over a large bandwidth and the resulting frequency diversity on each symbol helps combat fading or interference. FFH is not widely used in commercial wireless systems and is being replaced by DS-CDMA technology. In slow frequency hopping, there are several modulation symbols per hop that is, SFH transmits one or multiple symbols over each frequency i.e., $T_c = kT_s$, where k is some integer. The shortest uninterrupted waveform in SFH is the data symbol. Usually, TDMA uses SFH so that each of the time slots are also transmitted on a carrier frequency in accordance with a hopping scheme. The time spent in any frequency is referred to as *hope interval* or *dwell time* and denoted by T_h.

Difference between FFH and SFH:

The main difference between FFH and SFH lies in the fact that in FFH the carrier frequency changes or hops several times during transmission of one symbol while in SFH, the symbol rate is an integer multiple of hop rate. That is several symbols are transmitted on each frequency hop. Fig. 2-10 illustrates FFH and SFH.

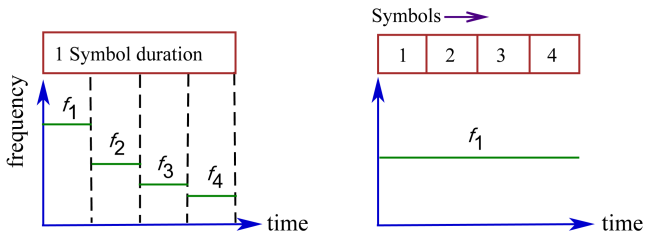


Figure 2-10: FFH and SFH illustration

2.6 Historical Background of Spread Spectrum

The early use of spread spectrum techniques can be traced back to World War-II in the development of radar and ranging techniques. During that time Germany was experimenting with pulse compression techniques that formed the basis for 'chirp'spread spectrum systems [5]. In Chirp spread spectrum, a carrier is swept over a wide band during each pulse interval. This technique is also known as pulsed FM and is primarily used in radar applications. While frequency hopping also traces its root to World War-II, and one of the first patents on a method for synchronizing frequency hopping transmitters

and receivers on submarines was held by the late actress Hedy Lamarr [55]. Since the early applications during World War-II, spread spectrum techniques have mostly been used by the military for secure, jamming free radio communications.
Recently, spread spectrum techniques have found their way into many other consumer and industrial applications such as PCS phones, Cordless telephones, wireless card readers, bar code scanners, blue tooth communication etc.

2.7 Overview of transceiver architecture

Wireless communication has received considerable attention of researchers working on personal communication systems in recent times. During the last decade wireless communication has also brought forth extensive studies in communication techniques and VLSI technology in order to achieve optimum bandwidth utilization, small size, low power consumption, high speed and so on. Unlike wired communication systems, there exist many other factors in wireless communication systems that affect the quality of communication including multi-path fading and co-channel interference [56]. Spread spectrum techniques [6, 57, 58] can solve these non-ideal problems associated with conventional wireless communication systems. A common component of all the spread spectrum communication systems is spread spectrum transceiver whose speed and reliability affects the overall system performance directly. As a result, demands of high transmission rate, high quality and security necessitate high speed and at the same time high performance spread spectrum transceiver.

2.7.1 Transceiver architecture tradeoffs

Low power wireless communication system is an emerging research area and attracting a lot of interest amongst researchers and industries [59–61]. In order to highlight the unsuitability of conventional radio topologies and to prepare the ground for the following chapters some technical concepts and issues will now be described.
The necessary signal processing functions that a conventional FHSS system must include are- up/down conversion, hop/dehop, modulation/demodulation, synchronization and input/output processing.
The architecture of a system defines the necessary functions of the system. There exist two basic types of transceiver architecture: superheterodyne and direct conversion transceivers (Fig.2-11 and 2-12). Superheterodyne receivers, widely used in current cellular systems convert the RF signal to baseband through one or more IF stages and thus they provide wide dynamic ranges and good selectivity for the received signal.
Superheterodye receivers are further classified as low-IF and high-IF depending on IF frequency range relative to the baseband spectrum.

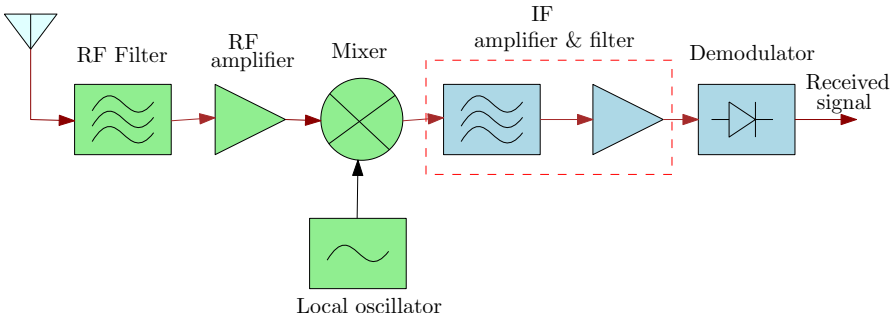


Figure 2-11: Superheterodyne Receiver

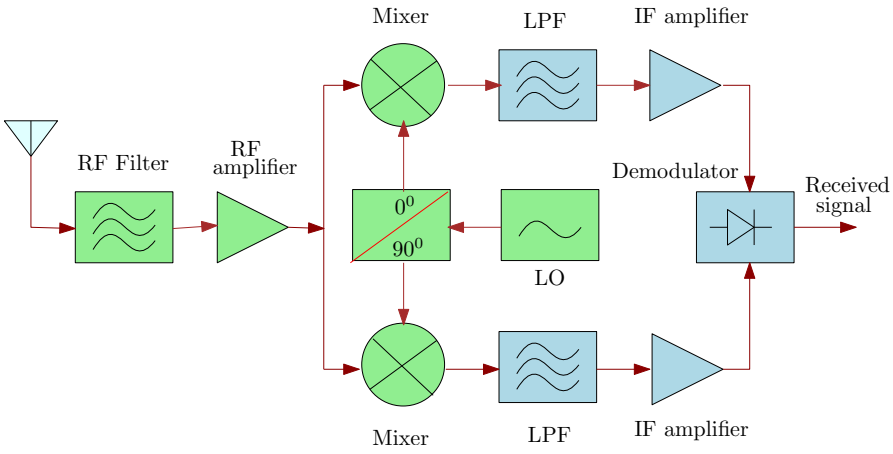


Figure 2-12: Direct-Conversion Receiver

Direct-conversion receivers are gaining much attention for portable communication systems where low power and small area are primary requirement [62, 63]. A direct-conversion architecture, also known as homodyne or zero-IF architecture converts the RF signal directly to base band or vice versa without using IF stages. This architecture eliminates the requirement of image-reject filters and other IF components and thereby makes high level of integration possible. Carrier recovery in direct-conversion receivers are somewhat difficult since it has to be done at RF. For this primary reason, most direct-conversion receivers use non-coherent detection scheme where carrier recovery is not necessary. It may be noted that a typical superheterodyne transceiver requires at least three types of filters- RF, image-reject and channel select filter while image-reject filters are eliminated by both zero-IF and low-IF transceivers.

With advances in digital signal processing and high speed analog-to-digital conversion technologies, IF-sampling receivers are replacing typical base band sampling receivers. Digital IF receivers provide accurate I-Q generation allowing carrier and timing recovery purely in digital domain in coherent applications such as QAM. Table 2.1 summarizes the main advantages and disadvantages of the three types of architecture stated above. One of the most crucial components of frequency hopped transceiver is low power hopping synthesizer. Conventional synthesizers employ analog phase-locked loop technique. The analog PLL based synthesizers have programmable frequency dividers to generate different frequencies as shown in Fig.2-13. The fundamental problem with this

Table 2.1: Advantages and disadvantages of Zero-, Low- and High-IF architectures

–	High IF architecture	Zero IF architecture	Low IF architecture
Advantages	Wide dynamic range Good Rx sensitivity	High integration Low cost, Low power	No dc offset problem High integration Easier carrier recovery
Disadvantages	Costly discrete filters Low integration High power	dc offset problem Tougher RFIC specs I-Q matching necessary Carrier recovery hard	I-Q matching critical Image signal suppression Extra ADC dynamic range –
Filters	RF, Image reject, Channel select	RF, Channel select –	RF, Channel select –
Applications	Fixed IF systems	Non-coherent modulation with no energy at dc (NC-FSK)	Linear modulation with BB spectrum around dc (GMSK)

frequency synthesizer is its speed and limited frequency resolution. Otherwise, it provides wide tuning range and good spectral purity. The hopping rate of this synthesizer is limited by the settling time of the loop which is inversely proportional to the loop bandwidth. Typical settling times of these analog synthesizers are of the order of few hundreds of microseconds [64, 65]. Direct digital frequency synthesis [66–69] combined

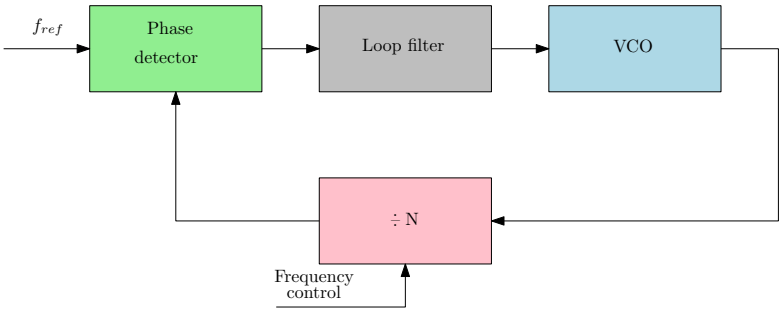


Figure 2-13: Analog PLL based frequency synthesizer

with a digital-to-analog (DAC) converter provides an alternative implementation of fast frequency-agile synthesizer. This synthesizer generates sine wave samples directly from the sine ROM which is addressed by the output of the digital phase accumulator as shown in Fig.2-14. The word-length N of this synthesizer determines the frequency resolution $\left(F_{clk}/2^N\right)$ and the output frequency is given by

$$F_{OUT} = \left(F_{clk}/2^N\right).F \tag{2.13}$$

where, N is the number of bits in the phase accumulator, F_{clk} is the frequency of the system clock and F is the value of the frequency control register. Some of the key advantages of this approach over analog PLL based systems are as follows:

- the hop rate does not depend upon settling time but limited by the system requirement
- it can achieve rapid frequency changes with continuous phase
- the discrete hop frequencies are determined by a PN sequence stored in the memory before the input control register
- the spectral quality of this system depends on phase truncation, amplitude quantization, DAC linearity and the phase noise of the clock source.

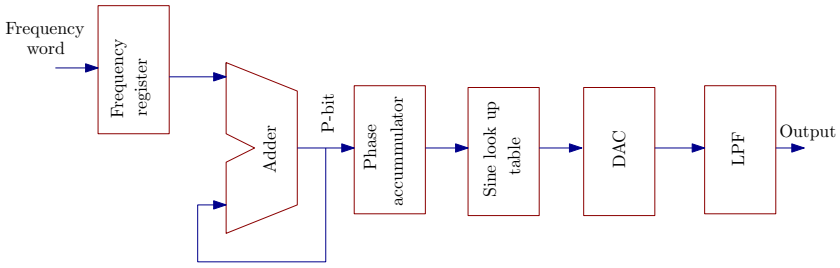


Figure 2-14: Direct Digital Frequency Synthesizer

Another architecture is the open loop modulation architecture where the VCO is tuned to the channel center frequency and the PLL is broken and the VCO is directly modulated by the baseband signal and the output is directly fed to the PA. This architecture is reported to have near-ideal spurious rejection [70, 71] and also does not suffer from frequency pulling problem since the instantaneous frequency of the PA is identical to that of the VCO. The main drawback of this architecture is associated with the linearity of the VCO and its temperature dependency.

2.8 Summary

A brief overview of wireless communication in general and its brief history is introduced. This chapter briefly discusses multiuser communication systems, cellular concepts and various multiple access techniques. A road-map of wireless communication system from first generation 1G to fourth generation 4G have also been discussed. Spread spectrum communication systems along with historical overview are also incorporated in this chapter since the proposed work employs frequency hopping spread spectrum technique. Finally, a brief review of spread spectrum transceiver architecture has been presented here in order to prepare the ground for subsequent work done.

Chapter 3

CMOS RF Circuit Design Concepts

3.1 Introduction

Wireless communication systems with special emphasis on spread spectrum communication systems [2, 4, 72] have been described in chapter 2. The aim of this thesis is to design a radio frequency FHSS wireless transceiver which involves the design of RF analog, digital and mixed signal circuits using low power CMOS devices. It is therefore considered necessary to briefly discuss CMOS RF circuit design concepts here.
A brief review of fundamental concepts of radio frequency circuit design and the basic principles governing the treatment of RF signals are reported [73–75]. The discussion is not exhaustive but considered useful for RF analog front-end design and analysis purposes. References are given which may be consulted for more detailed information. Basics of RF CMOS devices are also incorporated in order to bridge the gap between the classical MOS devices and the state-of-the-art complex MOSFETs. Brief description of RF MOSFET modeling is also incorporated which distinguishes the RF models of MOSFETs from their low frequency counter parts.

3.2 Basic radio frequency concepts

Radio frequency electronics basically deals with generation, acquisition and manipulation of high frequency signals. A clear and correct understanding of the performance parameters and techniques frequently used in RF design are considered essential requirement to accomplish the design activities associated with the transceiver system

proposed in this thesis. In view of the above, some important performance parameters and techniques are briefly introduced in the following subsections along with appropriate references where detailed discussions are available.

3.2.1 RF performance parameters and techniques

Among the most frequently used RF performance parameters and techniques, reflection, reflection coefficient (Γ), voltage standing wave ration (VSWR), return loss (RL), scattering parameters, smith chart, impedance matching and quality factor (Q) are considered as pre-requisites and briefly described below.

Reflection coefficient
Reflection takes place when a power wave travels along a transmission line having impedance discontinuity at some point along the line, a portion of the incident power gets reflected back to the source from the point of impedance discontinuity. As a result, the incident power loses a portion of its original amplitude. Reflection coefficient is one of the many performance parameters that represent the extent to which the impedance at the point of discontinuity is matched. Reflection coefficient is defined as the ratio of the reflected wave to the incident wave. It is defined in terms of impedances as in eqns.(3.1) and (3.2) [76–80].

$$\text{ReflectedCoefficient} = \frac{\text{Reflectedwave}}{\text{Incidentwave}} = \frac{Z_L - Z_O}{Z_L + Z_O} \tag{3.1}$$

where, Z_L is the load impedance and Z_0 is the characteristic impedance of the line.
The load reflection coefficient Γ_L with respect to the source impedance Z_S is expressed as [76, 78].

$$\text{Reflectioncoefficient}(\Gamma_\text{L}) = \frac{\text{Reflectedwave}}{\text{Incidentwave}} = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{3.2}$$

Voltage Standing Wave Ratio (VSWR)
Voltage Standing Wave Ratio is another parameter closely related to reflection coefficient. As the incident wave and the reflected wave travel in opposite directions, their addition generates a standing wave as shown in Fig.3-1.

The ratio of maximum voltage to the minimum adjacent voltage of the standing wave is defined as the VSWR which is mathematically expressed as [76, 78].

$$VSWR = \frac{|V_\text{max}|}{|V_\text{min}|} = \frac{1 + \Gamma_L}{1 - \Gamma_L} \tag{3.3}$$

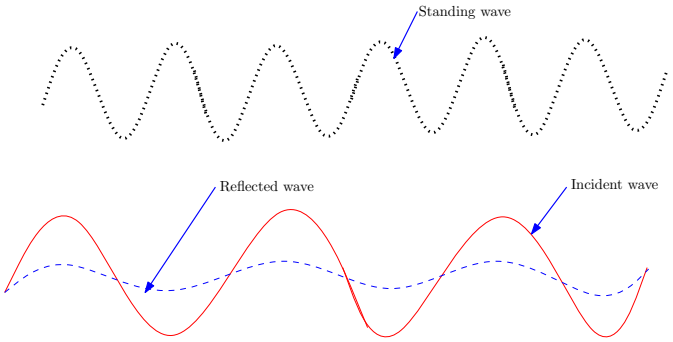


Figure 3-1: Incident wave (solid), Reflected wave (dashed) and standing wave (dotted)

It follows that for the perfectly matched condition, VSWR will take the value 1 : 1, since reflection coefficient will be zero.

Return Loss (RL)
Return Loss is defined simply as the magnitude of the reflection coefficient and expressed in decibels as seen in eqn.(3.4) [76, 78].

$$RL = -20 \log |\Gamma| \, dB \tag{3.4}$$

It follows that for a matched load there is no reflected power and the return loss is ∞ dB whereas a total reflection has a return loss of 0 dB. The terms *input return loss (IRL)* and *output return loss (ORL)* are frequently used to specify whether the return loss is measured at the input or output port of the device under measurement.

The Smith Chart
The Smith chart is one of the most useful and widely used graphical aid for high frequency circuit design applications. It was developed way back in 1939 by P. Smith and it forms an integral part of much of today's computer-aided-design (CAD) tools and high frequency test equipment [78, 81, 82]. The Smith chart, besides being a graphical tool, it also provides a clever means to visualize complex functions. A microwave engineer can develop an intuition by thinking transmission line and impedance matching problems in terms of the Smith chart. It is a fundamental graphical aid used to design impedance matching network. It also serves as a standard means to present graphically the impedance, reflectance, stability circles, gain circles, noise circles etc. The Smith chart, in mathematical point of view, is a 4-D representation of all complex impedances possible with respect to co-ordinates described by complex reflection coefficient. The real utility of the Smith chart lies in the fact that it can be used to convert reflection coefficient to normalized impedances and vice versa using the impedance circles printed on the chart.

Quality Factor (Q)
The quality factor of individual inductor or capacitor gives a measurement of how lossy

the component is or the value of the parasitic resistance present in the component. The Q of an inductor is defined as the ratio of its inductive reactance to its resistance at a given frequency and is a measure of its efficiency. The higher the Q factor, the closer it approaches ideal behaviour. The Q factor of an inductor can be expressed as shown in eqn.(3.5)

$$Q = \frac{\omega L}{R} \tag{3.5}$$

where, Q is the quality factor, ω is the frequency and L is the inductance.
The Q factor of a capacitor is defined as the ratio of its capacitive reactance to its resistance and is given by eqn.(3.6)

$$Q = \frac{X_C}{R} = \frac{1}{\omega RC} \tag{3.6}$$

where, X_C is the capacitive reactance, R is the resistance of the capacitor and C is the capacitance.
The Q factor of RLC resonant circuit is defined as in eqn.(3.7)

$$Q = \omega \frac{average\ energy\ stored}{power\ dissipated} = \omega \frac{W_m + W_e}{P_l} \tag{3.7}$$

where, ω is frequency,
P_l is the power dissipated by the resistor R,
$W_m = \frac{1}{4} |I_L|^2 L$ is the average magnetic energy stored in the inductor L,
$W_e = \frac{1}{4} |V_C|^2 C$ is the average electric energy stored in the capacitor C,
I_L is the current through the inductor L and
V_C is the voltage across the capacitor C.
At resonance, Q is given by eqns.(3.8) and (3.9) as

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC}, \quad \text{(for series RLC circuit)} \tag{3.8}$$

and

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC, \quad \text{(for parallel RLC circuit)} \tag{3.9}$$

The half-power bandwidth for both the circuits is given by

$$BW = \frac{2\Delta\omega}{\omega_0} = \frac{1}{Q} \tag{3.10}$$

When a resonant circuit is coupled to other circuits, the loaded Q denoted by Q_L is different from the unloaded Q. The resonant frequency is fixed by L and C and hence the resonant circuit should be connected to an external resistor R_L. In case of series resonant circuit, R_L should be connected in series with R while R_L should be connected in parallel with R in case of parallel circuit. The resulting external Q denoted by Q_e, is given by

$$\frac{1}{Q} = \frac{1}{Q_e} + \frac{1}{Q} \tag{3.11}$$

Scattering Parameters

Scattering means causing something to split into different components and scattering parameters provide a measure of the degree of separation and the magnitude of different components. It is very difficult to visualize when scattering parameters do not actually exist and in situations like this, it is necessary to define what is meant by 'incident' and 'reflected' components because they can not be identified otherwise. Therefore, the incident current is defined as that current which the transistor would deliver to a conjugate matched load. Even if the matching network does provide a conjugate matched load to the transistor, the validity of incident current does not alter. Since the incident current can be different from the actual current delivered to the matching network, their difference is defined as the reflected current. In a similar way incident and reflected voltages can also be defined. When scattering concept is applied to lumped circuits, the actual currents and voltages can be separated into scattered components according to appropriated definitions leading ultimately to relationships useful for design and analysis of circuits. The scattering concept can be illustrated by considering the one-port network of Fig.3-2. where, the actual current and voltage are

$$I = \frac{E}{Z_0 + Z_L} \tag{3.12}$$

and

$$V = \frac{EZ_L}{Z_0 + Z_L} \tag{3.13}$$

where Z_0 is considered to be internal impedance of the generator. The incident com-

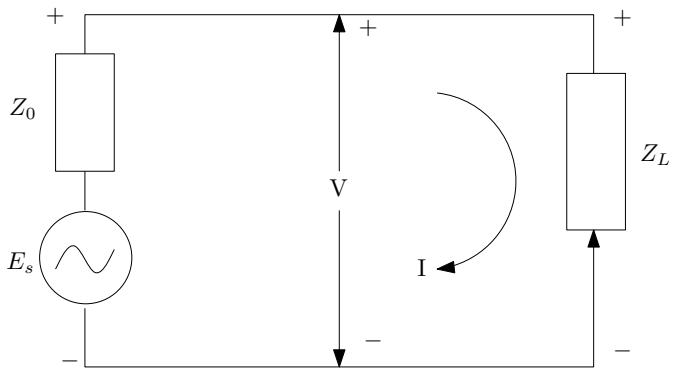


Figure 3-2: One-port network

ponents are obtained when the generator is connected to conjugate matched load, Z_0^*. Thus, the incident current and voltage can be given by eqns.(3.14) and (3.15) respectively.

$$I_i = \frac{E}{Z_0 + Z_0^*} = \frac{E}{2\ \mathrm{ReZ_0}} \tag{3.14}$$

$$V_i = \frac{EZ^*}{Z_0 + Z_0^*} = \frac{EZ_0^*}{2\ \mathrm{ReZ_0}} \tag{3.15}$$

The reflected components can be calculated by using the defining decomposition equa-

tions as

$$I = I_i - I_r \tag{3.16}$$

and

$$V = V_i - V_r \tag{3.17}$$

Using eqns.(3.12), (3.14) and (3.16), we find the reflected current as

$$\begin{aligned} I_r &= I_i - I \\ &= \left(\frac{Z_L - Z_0^*}{Z_L + Z_0}\right) I_i \\ &= S^I I_i \end{aligned} \tag{3.18}$$

where $S^I = (Z_L - Z_0^*)/(Z_L + Z_0)$ is the current scattering parameter for the one-port network. Similarly, using eqns.(3.13), (3.15) and (3.17), reflected voltage can be expressed as

$$\begin{aligned} V_r &= V_i - V \\ &= \frac{Z_0}{Z_0^*}\left(\frac{Z_L - Z_0^*}{Z_L + Z_0}\right) V_i \\ &= \frac{Z_0}{Z_0^*} S^I V_i \\ &= S^V V_i \end{aligned} \tag{3.19}$$

where $S^V = (Z_0/Z_0^*)\, S^I$ is the voltage scattering parameter of the one-port network.
It may be observed from eqn.(3.18) and (3.19) that the incident and reflected components are related to each other through the impedances and scattering parameters. Each scattering parameter and reflected component will be zero when $Z_L = {Z_0}^*$. The impedance Z_0 is made to be a pure resistance so that $Z_0 = R_0$ and it is used as a normalizing or reference resistance. For $Z_0 = R_0$ and $Z_0 = {R_0}^*$ we get

$$S^I = S^V = \frac{Z_L - R_0}{Z_L + R_0} \tag{3.20}$$

In this case the current and voltage scattering parameters are equal and have exactly the same form as the reflection coefficient of a transmission line having characteristic impedance R_0 and terminated in load impedance Z_L.

Impedance Matching

In low frequency circuit design, either voltage gain or current gain concept is used for cascading system blocks and are usually terminated in high load in order to maximize output voltage. In RF circuit design, the voltage seen at the output terminals of a transistor will not be the same as the voltage applied at the input terminals. This happens because parts of the current will pass through the parasitic capacitances. The behavior of the device at RF is thus not known without the knowledge of its equivalent

circuit inclusive of parasitics. The parasitics, which are basically reactive components, do not dissipate power. Thus, if we use input power in stead of voltage or current, we can achieve maximum power transfer by the device by properly terminating it. For this reason circuits are designed at RF frequencies with power transfer considerations. In order to maximize power transfer from source to load, impedance matching is required. If we consider the circuit of Fig.3-3 where the source and load impedances are fixed and can not be altered, our objective will be to design the input and output matching networks so that Z_1 matches Z_S and Z_2 matches Z_L.

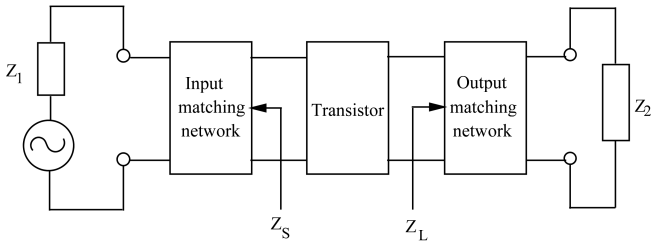


Figure 3-3: Input and output matching network

Impedance matching for complex terminations
Sometimes it so happens that the real parts of the source and load impedances are same but one has a series reactance. The presence of any net reactance between the source and load impedances will reduce the current through the load thereby reducing the power dissipation at load. Maximum dissipation will occur when the load impedance equals the source impedance that is when the net reactance is made zero. This occurs when the load and source impedances are complex conjugates of one another so that they have equal real parts and opposite reactive parts. Thus, a conjugate match can be obtained by adding proper type and amount of reactance to make the net reactance equal to zero.

3.3 Basics of RF MOSFETs

MOSFETs form the basis of this thesis and therefore a brief review of RF MOSFETs is incorporated in this section in view of the requirement of high speed analog, digital and mixed-signal circuits by the proposed transceiver.
The idea and basic concept of CMOS circuit design was invented in 1963 by F. M. Wanlass at Fairchild semiconductor [9]. Gate material used in a modern MOSFET is no longer metal but polysilicon. Thus, modern technology is CPOS (Complementary Polysilicon Oxide Semiconductor) rather than CMOS. The most attractive features of modern MOSFETs are as follows:

- CMOS integrated circuits can be laid out in a small area with high level of inte-

gration.

- Fabrication cost can be kept low by shrinking device dimension (scaling) with each new generation of technology.
- Offers very high operating speeds and at the same time dissipates very small power.
- CMOS circuits can be fabricated with only few defects.
- Ability to combine RF analog and digital circuits on the same die.

Traditionally, the high frequency properties of silicon MOSFETs have been considered inferior to other technologies, including silicon bipolar transistors and transistors based on group III-V materials such as gallium, arsenide etc. However, CMOS technology has now reached a state of evolution, in terms of both frequency and noise performance and is now becoming a strong contender for RF applications in the gigahertz range, covering the frequency range of cell phones, Global Positioning Systems (GPS) and Bluetooth. Circuit design is an integral part of electronics engineering and is as important as fabrication process itself. Advances in fabrication process always pose new challenges to the circuit designers. To take full advantage of new technology, the designers need to update their CAD (Computer Aided Design) tools with precise descriptions of the new devices in terms of models that can be implemented into circuit simulators.
With the increase in the cut-off frequency as technology comes in the submicron regime, CMOS technology has been in the run from its counterpart bipolar technology. In order to scale the devices for different operations, the device models must be physics based to account for the complex dependence of the device properties on dimensions and other processing variables. The model parameters are usually derived from measurement and characterization of the devices. For CMOS devices operating in the radio frequency band, both modeling and characterization are considered to be a challenging task. CMOS technology scaling has the potential of advancing the circuit performance and offers opportunities to operate at higher frequencies with low power consumption.

3.4 Brief Review of RF MOSFETs

MOSFETs are today considered the mainstream transistors due to low power, low cost and higher integration capability. CMOS technology finds numerous RF applications. Beforetime, compound semiconductors such as GaAs, SiGe, InP mainly dominated the high speed communication circuits and RF applications [83–85]. However, the extensive research that took place on RF CMOS applications, especially in Europe and the United States [62, 86, 87] pushed this technology to be considered as the mainstream, even though compound semiconductors still dominate beyond 5GHz applications [88].

The RF characteristics such as the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of Si ULSI extends to several GHz, available bandwidth increases and the frequency of the signal transmitted to VLSI interconnections advances to several GHz [82, 89]. Thus, CMOS technology becomes suitable for both the RF technology of wireless communication applications and digital VLSI applications. However, the necessity of optimization in semi-restricted process conditions and the difficulty in adopting high resistive substrates are some of the issues associated with RF CMOS applications.
There exist over hundred transistor models such as Level1, Level2, Level3, BSIM, HSPICE Level28, BSIM2, BSIM3, BSIM3v3, Model9, EKV model and BSIM4 which are developed for digital, analog and mixed signal applications. In recent times all these models are extended for RF applications too. However, at RF frequencies parasitic effects become prominent and degrade device performance severely and it becomes very difficult to predict device behaviour compared to device modeling for analog and digital applications at d.c. and low frequencies. With the fast growth of wireless communication market, RF designers have started exploring the use of CMOS devices in RF circuits, even though RF modeling accuracy of the CMOS compact models are not satisfactory [75, 90, 91]. One of the commonly adopted modeling approach for RF applications is to build the sub-circuits using the MOSFET models suitable for analog applications. The accuracy of such models depends on how much correctly the sub-circuits are designed with correct understanding of the device physics in high frequency regime.

3.4.1 The basic n-channel MOSFET

A basic n-channel MOSFET consists of two heavily doped n-type regions termed as the source and the drain which form the main terminals of the device as shown in Fig.3-4. The gate is made up of metals in early days and now replaced by heavily doped polysilicon while the bulk is lightly doped p-type substrate which is usually kept at the same potential with the source. For the purpose of quantitative analysis, the device under consideration is assumed to have "long" channel which essentially means "low electric field". Thus, short channel devices will still conform to the long channel equations reasonably well as long as "low electric field" is maintained applying low voltages which will produce small electric field. If a positive gate voltage is applied, holes are repelled away from the surface of the substrate and at certain value of the gate voltage (threshold voltage, V_t) the surface becomes completely depleted of charge. If the gate voltage is increased further, an inversion layer consisting of electrons supplied by the source is induced and thereby develops a conducting path between the source and drain. The device is said to be in strong inversion region when the gate to source voltage (V_{gs}) becomes several (kT/q) above threshold voltage. The induced inversion charge is proportional to the gate voltage above V_t and the induced charge density is constant along the channel provided that the drain to source voltage is zero. If a drain

voltage V_{dd} is applied, the channel potential will increase from zero at the source end to V_{dd} at the drain end. Thus, the net voltage to induce an inversion layer gradually decreases from source end towards the drain end which causes induced charge density to vary from its maximum value at the source towards a minimum at the drain end as shown in Fig.3-4. The channel charge density is expressed in the following form:

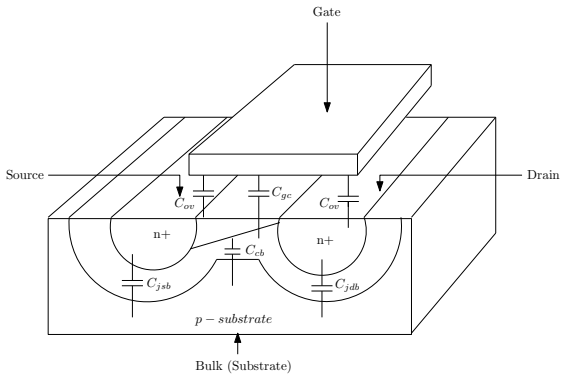


Figure 3-4: MOSFET Capacitances

$$Q_n(y) = -C_{ox}\left[\{V_{gs} - V(y)\} - V_t\right] \tag{3.21}$$

where $Q_n(y)$ is the charge density at position y along the channel, C_{ox} is ε_{ox}/t_{ox} and $V(y)$ is the channel potential at position y. The negative sign indicates that the induced charge is made up of electrons. The equations related to the most important terminal characteristics of the device can now be derived using eqn.(3.22) as follows: The linear region of operation of the device is defined as one in which gate to source voltage (V_{gs}) is large enough or drain to source voltage (V_{ds}) is small enough so that induction of inversion layer is guaranteed for the whole distance of the channel. From eqn.(3.22), it can be seen that the charge density becomes zero when

$$\{V_{gs} - V(y)\} - V_t = 0 \tag{3.22}$$

The charge density first becomes zero at the drain end at some voltage. Therefore, the boundary for the linear region of the device can be defined as

$$\begin{aligned} &\{V_{gs} - V_{ds}\} - V_t = 0 \\ &\Rightarrow V_{ds} = V_{gs} - V_t \equiv V_{dsat} \end{aligned} \tag{3.23}$$

As long as the condition $V_{ds} < V_{dsat}$ is satisfied, the device will be in the linear or active region. Using the equation for channel charge density given by eqn.(3.21) and the definition of linear region defined by eqn.(3.23), we can derive the expression for device current since current is proportional to charge times velocity. Thus, the device current, I_d can be expressed as

$$I_d = WQ_n(y)\,v(y) \tag{3.24}$$

where W is the width of the device and $v(y)$ is the velocity which is the product of electron mobility (n) and electric field E at low electric field. Therefore, eqn.(3.24) can now be written as

$$I_d = WQ_n(y)\,\mu_n E \tag{3.25}$$

Substituting for channel charge density Qn(y) from eqn.(3.21) into eqn.(3.25), we get

$$I_d = -WC_{ox}\left[V_{gs} - V(y) - V_t\right]\mu_n E \tag{3.26}$$

Since the electric field E along the y-direction is simply the negative of the gradient of the voltage along the channel, we can write eqn.(3.26) as

$$I_d = \mu_n WC_{ox}\left[V_{gs} - V(y) - V_t\right]\frac{dV}{dy} \tag{3.27}$$

Integrating eqn.(3.27) along the direction of the channel, we get

$$\int_0^L I_D dy = \int_0^{V_{ds}} \mu_n C_{ox} W\left[V_{gs} - V(y) - V_t\right] dV \tag{3.28}$$

Now, solving for I_D, we get the expression for drain current in the linear region as

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{3.29}$$

It can be observed from eqn.(3.56) that the drain current and drain to source voltage have a nearly linear relationship for small drain to source voltage.
If we increase the V_{ds} such that the channel ceases to extend throughout the channel form source to drain, the field experienced by channel charges ceases to increase which causes the channel current to remain constant even if V_{ds} is increased. This current can be computed simply by substituting V_{dsat} for V_{ds} in eqn.(3.29).

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{gs} - V_t\right)V_{dsat} - \frac{V_{dsat}^2}{2}\right] \tag{3.30}$$

Eqn.(3.30) can be simplified to

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left[\left(V_{gs} - V_t\right)^2\right] \tag{3.31}$$

It can be observed from eqn.(3.31) that drain current in saturation has a square-low dependency on gate source voltage and almost independent of drain voltage. Differentiating eqn.(3.31), the transconductance of the device can be found to be

$$g_m = \mu_n C_{ox}\frac{W}{L}\left(V_{gs} - V_t\right) \tag{3.32}$$

which can also be written as

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{3.33}$$

It can thus be seen that unlike bipolar devices, the transconductance of a long channel MOSFET depends only on the square root of the bias current [12, 92].

3.4.2 Dynamic Elements of MOSFET

The high-frequency performances of circuits are limited by various capacitances associated with MOSFETS. The source and drain regions form reverse biased junctions with the substrate resulting in standard junction capacitances C_{jsb} and C_{jdb} from each of these regions to the substrate as shown in Fig.3-4. In addition to junction capacitances, there also exist various parallel plate capacitances such as gate-source and gate-drain overlap capacitances denoted by C_{ov} as shown in Fig.3-4. These capacitances are highly undesirable but can not be avoided. The source and drain regions get diffused laterally during manufacturing process and bloat out a bit during processing and extend below the gate by some amount. A crude estimate of overlap, L_D may be considered as 2/3 to 3/4 of diffusion depth of source and drain. Therefore, parallel plate capacitance can be expressed as

$$C_{ov} \approx \frac{\varepsilon_{ox}}{t_{ox}} W L_D 0.7 C_{ox} W x_j \tag{3.34}$$

where x_j is the depth of source, drain diffusion,ε_{ox} is dielectric constant of the oxide, t_{ox} is the oxide thickness.
Another parallel-plate capacitance is the gate-to-channel capacitance denoted by C_{gc} in Fig.3-4. Both the source and drain regions extends below the gate and therefore effective channel length decreases by twice the bloat, L_D giving the total value of C_{gc} as

$$\mathrm{C_{gc}} = C_{ox} W \left(L - 2L_D\right) \tag{3.35}$$

Another capacitance C_{cb} exists between the channel and the bulk because the charge carriers on the surface and those on bulk are of opposite type and the depletion region in between them. This capacitance behaves as a junction capacitance and approximate value of it can be given by

$$C_{cb} \approx \frac{\varepsilon_{Si}}{x_d} W \left(L - 2L_D\right) \tag{3.36}$$

where x_d is the depth of the depletion layer and is given by

$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_{sub}} \left|\Phi_s - \Phi_F\right|} \tag{3.37}$$

where the quantity $(\Phi_s - \Phi_F)$ is the difference between the surface potential and the Fermi level in the substrate which has a magnitude of twice the Fermi level both in

linear and saturation region in case of strong inversion.
The channel is not an accessible terminal of the device and therefore contribution of various capacitive terms to the terminal capacitances can not be known without the knowledge of channel charge distribution between the source and the drain. The values of terminal capacitances, in general, depend upon operating regime because bias conditions influence the charge partitioning. When the device is in the linear region, it may be assumed that the channel charge is shared equally between the source and drain and hence half of C_{gc} is added to the overlap terms and the junction capacitances C_{jsb} and C_{jdb} are also augmented by half of C_{cb}.
When the device is in saturation, potential variations in the drain do not affect the channel charge distribution and therefore, there is no contribution to C_{gd} by C_{gc}. The gate-source capacitance is affected by C_{gc} and only about 2/3 of C_{gc} should be added to the overlap term. The capacitance C_{cb} does not contribute anything to C_{db} but contributes 2/3 of its value to C_{sb}.
The gate-bulk capacitance can be considered to be zero in strong inversion since the bulk is shielded from the gate by the channel charge. When the device is off, there is a gate voltage dependent capacitance whose value varies almost linearly between C_{gc} and the series combination of C_{gc} and C_{cb}. Below but near the threshold voltage this value is gets closer to the series combination and approaches the limiting value C_{gc} in deep accumulation where the surface majority carrier concentration increases above that of bulk due to the positive charge induced by the strong negative gate bias. The surface becomes strongly conducting in deep accumulation and can be treated as metal resulting in gate-bulk capacitance that is the full parallel plate value. The approximate terminal capacitances are presented in Table 3.1.

Table 3.1: MOSFET terminal capacitances (approximate)

–	Off	Linear	Saturation
C_{gs}	C_{ov}	$\mathrm{C_{gc}}/2 + \mathrm{Cov}$	$2\mathrm{C_{gc}}/3 + \mathrm{Cov}$
C_{gd}	C_{ov}	$\mathrm{C_{gc}}/2 + \mathrm{Cov}$	C_{ov}
C_{gb}	$\mathrm{C_{gc}C_{cb}}/\left(\mathrm{C_{gc}} + \mathrm{C_{cb}}\right)$	0	0
	$< \mathrm{C_{gb}} < \mathrm{C_{gc}}$	–	–
C_{sb}	C_{jsb}	$\mathrm{C_{jsb}} + \mathrm{C_{cb}}/2$	$\mathrm{C_{jsb}} + \mathrm{C_{cb}}/3$
C_{db}	C_{jdb}	$\mathrm{C_{jdb}} + \mathrm{C_{cb}}/2$	C_{jdb}

3.4.3 High frequency figures of merit

For high frequency performance, two figures of merit ω_T and ω_{max} which are the frequencies at which the current and power gains respectively fall to unity are specifically popular. To derive the expression for ω_T it is assumed that the drain is terminated with

an incremental short circuit while the gate is supplied with an ideal current source. As a result, ω_T does not include information about the drain-bulk capacitance. As a result of current source drive, the series gate resistance has no effect on ω_T . Thus, both r_g and C_{jdb} affects strongly the high frequency performance but ω_T simply ignores it. With the assumption that gate-to-drain capacitance is used to compute the input impedance and its feed forward contribution to output current is negligible then the ratio of drain current to gate current is given by

$$\left|\frac{i_d}{i_{in}}\right| \approx \frac{g_m}{\omega\left(C_{gs}+C_{gd}\right)} \tag{3.38}$$

Eqn.(3.38) has a value of unity at a frequency given by

$$\omega_T = \frac{g_m}{C_{gs}+C_{gd}} \tag{3.39}$$

The frequency at which the power gain becomes unity is quite difficult and more relevant compared to that of current gain. Thus ω_{max} is computed with the following assumptions:

- The input impedance is computed with incrementally shorted drain and ignoring the feed forward current through C_{gd}.
- The feedback from drain to gate through C_{gd} is considered in computing the output impedance because computation of maximum power gain requires conjugate matched termination.

The magnitude of the short circuit current gain at high frequency can approximately be given by

$$\left|\frac{i_D}{i_{in}}\right| \approx \frac{\omega_T}{\omega} \tag{3.40}$$

The resistive part of the output impedance can roughly be given by

$$\begin{aligned} g_{out} &\approx g_m \frac{C_{gd}}{C_{gd}+C_{gs}} \\ &= \omega_T C_{gd} \end{aligned} \tag{3.41}$$

If the conjugate termination has the conductance value given by equation (3.41), the power gain will be maximized and is given by

$$\begin{aligned} \frac{P_L}{P_{in}} &\approx \frac{\frac{1}{2}\left(\frac{\omega_T}{\omega} i_{in}\frac{1}{2}\right)^2 \frac{1}{\left(\omega_T C_{gd}\right)}}{\frac{i_{in}^2 r_g}{2}} \\ &\approx \frac{\omega_T}{\omega^2 4 r_g C_{gd}} \end{aligned} \tag{3.42}$$

The expression given by eqn.(3.42) will have a unity value at a frequency given by

$$\omega_{\max} \approx \frac{1}{2}\sqrt{\frac{\omega_T}{r_g C_{gd}}} \tag{3.43}$$

Now, it is obvious that ω_{max} depends on gate resistance,r_g. The gate resistance can be reduced to small values by proper layout design to achieve larger ω_T. The output capacitance can be tuned out by inductance and hence it will have no effect on ω_{max}. These ω_{max} and ω_T are extrapolated values and the circuits need not be operated at these frequencies. These figures of merit are used for rough indication of high frequency performance of the device.

The lumped model considered above, however, does not apply to an arbitrarily large frequency range. The distributed nature of transistors up approximately 1/10th or 1/5th of ω_T . The lumped model becomes progressively inadequate as frequency increases, the most important shortcoming being the neglect of transit-time or non-quasi-static (NQS) effects.

If a step in gate-to-source voltage is applied, charge gets induced in the channel and drifts towards the drain. Due to finite carrier velocity the induced charge arrives at the drain some time later which implies that the transconductance is associated with a phase delay. This delayed transconductance causes the input impedance to change. As a result, the voltage applied at the gate performs some work on the channel charge. In any correct circuit model this dissipation has to be accounted for. It has been shown in [92] by Van der Ziel that for long channel devices the transit delay causes the gate admittance to possess a real part that increases as the square of frequency:

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{3.44}$$

Assuming that g_{d0} is approximately equal to g_m eqn.(3.44) can be approximately given by

$$g_g \approx \frac{g_m}{5}\left(\frac{\omega}{\omega_T}\right)^2 \tag{3.45}$$

Therefore, it may be concluded that if NQS effects are neglected while computing maximum unity power gain frequency, an over estimate of the true value of ω_{max} is made. We can now derive an approximate expression for ω_T in terms of process parameters, device geometry and operating point with the help of the expression for g_m above.

3.4.4 Short channel MOSFETs

The continuous shrinking of device geometries has resulted in so small devices that various electric field effects become prominent even at low to moderate supply voltages. The scattering of the high-energy photons, carrier velocity ceases to increase with increasing field and at about 10^6 V/m in silicon, the electron drift velocity shows progressively less

dependency on electric field and ultimately saturates at about 10^5 m/s. Unlike long-channel devices, the drain current of short-channel devices saturate when the velocity saturates. In order to introduce velocity saturation, the equation for drain current as obtained in eqn.(3.31) can be rewritten as

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_t) V_{dsat,l} \tag{3.46}$$

where,$V_{dsat,l}$ is the V_{dsat} for long channel devices and is given by $(V_{gs} - V_t)$. It may be stated that drain current saturates when velocity saturates and velocity saturates at smaller voltages for short channel devices. It can therefore be assumed that V_{dsat} diminishes with channel length. A more general expression for V_{dsat} is given in [92] appears as stated below:

$$V_{dsat} \approx (V_{gs} - V_t) \| (LE_{sat}) = \frac{(V_{gs} - V_t)(LE_{sat})}{(V_{gs} - V_t) + (LE_{sat})} \tag{3.47}$$

Drain current now can be expressed as

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_t) [(V_{gs} - V_t) \| LE_{sat}] \tag{3.48}$$

where, E_{sat} is the field strength at which the carrier velocity drops to half of the value extrapolated from low field mobility. It is now obvious that the influence of short channel effects depends on the ratio $(V_{gs} - V_t)/L$ and E_{sat}. If this ratio is small then the device will still behave as a long channel one. As the device gets shortened, less gate overdrive $(V_{gs} - V_t)$ is needed to onset these effects. With the above definition of E_{sat}, the drain current now be expressed as

$$I_D = WC_{ox} (V_{gs} - V_t) v_{sat} \left[1 + \frac{LE_{sat}}{(V_{gs} - V_t)}\right]^{-1} \tag{3.49}$$

For large values of $(V_{gs} - V_t)/L$ compared with E_{sat}, the drain current approaches the following limit:

$$I_D = \frac{\mu_n C_{ox}}{2} W (V_{gs} - V_t) E_{sat} \tag{3.50}$$

It can now be concluded that the drain current eventually ceases to depend on the channel length and the relationship between the drain current and gate-source voltage becomes linear rather than square-law.

3.5 Technology Scaling

The fundamental issue associated with downsizing of MOSFETs is to retain long channel characteristics after miniaturization. Several road maps have been proposed for designing submicron MOSFETs so that they exhibit such behavior. Three of the most

important scaling techniques are constant electric field scaling and its derivatives i.e. constant voltage scaling and constant electrostatics scaling.
The scaling limit of MOSFETs and the improvement of traditional scaling theory [93–97], provide a proper road map for submicron MOSFET design [98]. Reduction in channel-length of MOSFETs is described using scaling theory. It is a standard practice to use a scaling parameter S $((S < 1))$ in order to scale the dimensions of a MOSFET. The typical value of S lies around the neighborhood of 0.7 from one CMOS technology generation to the next generation. Let us consider a process uses a V_{dd} of 2V. The next generation process will then use a V_{dd} of 1.4V. This can be described as follows:

$$V_{dd(nxt)} = V_{dd}.S \tag{3.51}$$

The length of the channel will be reduced to

$$L_{(nxt)} = L.S \tag{3.52}$$

The width of the device will be reduced to

$$W_{(nxt)} = W.S \tag{3.53}$$

The various effects of scaling factor, S of the MOSFET parameters are depicted in Table 3.2.
The most significant features associated with MOSFET scaling are:

Table 3.2: Relation of CMOS parameter with scaling parameter

Sl no.	MOSFET parameter	Scaling factor
1	Supply voltage (V_{dd})	S
2	Channel length (L_{min})	S
3	Channel width (W_{min})	S
4	Gate-oxide thickness (t_{ox})	S
5	Substrate doping (N_A)	S^{-1}
6	On current (I_{on})	S
7	Gate capacitance (C_{ox})	S
8	Gate delay	S
9	Active power	S^{-3}

- reduced device sizes and hence smaller chip size, in other words, high yield and higher number of devices per wafer.
- lower gate delay resulting in higher operating frequency and
- reduced power dissipation.

In addition to the above features, there are some unwanted side effects associated with MOSFET scaling known as *short-channel effects* as described below.

Negative Bias Temperature Instability- In modern PMOS devices, some important device parameters such as threshold voltage is found to shift over time when the gate voltage is kept below the source voltage ($V_{SG} > 0$). The main reason behind this is the trapping of oxide defects and the creation of interface states. NBTI may become significant reliability concern particularly in S_iO_2 gate dielectrics due to time and temperature dependent fluctuations of MOSFET parameters during both ON and OFF states. Although NBTI is also present in NMOS devices, it is more prominent in PMOS.

Oxide Breakdown- The maximum electric field across the MOSFET gate oxide needs to be limited within 10MV/cm for reliable operation of the device. This means 1V/Å of gate oxide of the device. Thus, a device with $t_{ox} = 20$Å, should limit its applied gate voltages to 2V for its reliable operation.

Drain-Induced Barrier Lowering- Drain-Induced Barrier Lowering (DIBL) causes a reduction in the threshold voltage of the MOSFET with the application of drain-to-source voltage. The positive potential at the drain terminal helps to invert the channel towards the drain side of the device and causes a reduction in the threshold voltage. Threshold voltage decreases with increase in V_{DS} and results in an increase in drain current and hence decrease in output resistance of the MOSFET.

Gate-Induced Drain Leakage- Gate-Induced Drain Leakage (GIDL) is associated with drain-to-substrate current leakage [99]. The substrate and surface potentials of a MOSFET are nearly same when the device is in accumulation. If the drain is now at a higher potential, a sudden increase in avalanche multiplication or band-to-band tunneling may take place. As a result, minority carriers below the gate are swept to the substrate contributing to the leakage current.

Gate Tunnel Current- With the scaling down of oxide thickness, the probability of the carriers tunneling through the gate oxide increases. In order to reduce this tunnel current various sandwiches of dielectric materials are being explored.

3.6 MOSFET models used in this thesis

A MOS transistor is described by the MOSFET model and element parameters and two sub-models described by the CAPOP and ACM model parameters. The element statement defines the connectivity of the MOSFET and reference to the MODEL. The MODEL statement specifies whether the device is p-channel or n-channel, level of the device and a number of user selectable parameters of the model [100]. The CAPOP

parameter specifies the models for the gate capacitances of the MOSFET while ACM parameter selects the diode models to be used for the MOSFET bulk diodes. The parameters of the sub-models CAPOP and ACM characterize the gate capacitances and bulk diodes of the MOSFET. MOSFET models are classified according to versions or levels such as LEVEL1, LEVEL2 upto LEVEL64 [101, 102]. The MOSFET model used in this thesis is BSIM3v3 which is a LEVEL49 MOSFET model. This version provides the most stable and up-to-date representation of the UCB BSIM3v3.2.4 model [1, 103]. The CMOS process [8, 9] used in this thesis allows a minimum gate length of $0.35m$. The process allows for n-channel MOSFETs (NMOS), p-channel MOSFETs (PMOS) and many other active and passive devices including resistors, capacitors and diodes to name a few. The most important design parameters used in this thesis are listed in Table 3.3, 3.4 and 3.5.

Table 3.3: NMOS and PMOS Operating voltages. Values in brackets denote absolute maximum values [1]

MOS Transistor	Max V_{GS} [V]	Max V_{DS} [V]	Max V_{GB} [V]	Max V_{DB} [V]	Max V_{SB} [V]
NMOS/PMOS	3.5V (5)V	3.5V (5)V	3.5V (5)V	3.5V (5)V	3.5V (5)V

Table 3.4: Brief summary of NMOS transistor parameters used in this work

NMOS			
Parameter	Min.	Typ.	Max.
Long channel (0.35) VTH [V]	0.35	0.45	0.55
Short channel $(10 * 0.35)$VTH [V]	0.35	0.45	0.55

Table 3.5: Brief summary of PMOS transistor parameters used in this work

PMOS			
Parameter	Min.	Typ.	Max.
Long channel (0.35) VTH [V]	0.35	0.45	0.55
Short channel $(10 * 0.35)$VTH [V]	0.35	0.45	0.55

3.7 Summary of operation of the MOSFETs used in this work

The MOSFET is a four terminal device and can be biased to work in three regions of operation namely, the triode region, saturation region and the sub-threshold region. Since the thesis revolves around low voltage circuit design, the transistors were designed to operate in the saturation region with minimum excess gate-source voltage which is also known as overdrive voltage, V_{OD}. Cases where the transistors were not pushed

too far in the saturation region, channel length modulation [9] were ignored for those designs.

3.7.1 Operation in the triode region

The objective of this section is to find the relation between I_D, V_{DS} and V_{GS} [8]. The oxide capacitance that exists between the gate and the inversion layer can be calculated with the help of the flowing expression:
The oxide capacitance per unit area is given by

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.54}$$

where, ε_{ox} is the dielectric constant of S_iO_2 and t_{ox} is the oxide layer thickness. Actual value of C_{ox} as used in practical designs, can be calculated as

$$C_{ox} = C'_{ox}.A = C'_{ox}.WL \tag{3.55}$$

The transconductance parameter for NMOS transistor is defined as

$$KP_n = \mu_n.C'_{ox} \tag{3.56}$$

and the transconductance parameter for PMOS transistor is defined as

$$KP_p = \mu_p.C'_{ox} \tag{3.57}$$

Therefore, the current flowing to the drain of an NMOS device operating in the triode region can be given as

$$\begin{aligned} I_D &= KP_n \frac{W}{L}\left[(V_{GS} - V_{TH})\, V_{DS} - \frac{V_{DS}^2}{2}\right] \\ &= \mu_n C'_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})\, V_{DS} - \frac{V_{DS}^2}{2}\right] \end{aligned} \tag{3.58}$$

where V_{TH} is the threshold voltage of the device and eqn.(3.58) is valid only for $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{GS} - V_{TH}$. The equation for PMOS device is identical to eqn.(3.58) and can be obtained by replacing the NMOS parameters by equivalent PMOS parameters.

3.7.2 Operation in the saturation region

The channel under the gate oxide starts to 'pinch off'when $V_{DS} \geq V_{GS} - V_{TH}$ driving the transistor into saturation and this value of V_{DS} is termed as $V_{DS,sat}$. Ignoring the channel length modulation effects and assuming V_{GS} to be constant and any increase

in V_{DS} does not cause in increase in drain current, the drain current of NMOS device operating in the saturation region can be expressed as

$$I_D = \frac{KP_n}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{3.59}$$

where $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$. This equation is also referred to as "square law" equation of MOSFETs.
In practical devices, increase in V_{DS} beyond saturation point causes the "pinched off" region move towards the source reducing the effective channel length. This phenomenon is known as channel length modulation and in order to include the effects of channel length modulation eqn.(3.59) can be written as

$$I_D = \frac{KP_n}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left[1 + \lambda\left(V_{DS} - V_{DS,sat}\right)\right] \tag{3.60}$$

This equation assumes that the effective mobility of the majority carriers (μ_n) remains uniform which is not the case in short channel devices. The difference in operation in short channel MOSFETs occurs because of the drifting carriers between channel and gate of the device saturate resulting in what is known as velocity saturation, v_{sat}. This carrier velocity saturation causes a reduction in electron or hole mobility which in turn increases the effective channel sheet resistance. The drain current in the active region is thus expressed by [104].

$$\begin{aligned}\lim_{Ecritical \to \infty} I_D &= \mu_n C_{ox} W\left(V_{GS} - V_{TH}\right) E_{critical} \\ &= C_{ox} W\left(V_{GS} - V_{TH}\right) v_{scl}\end{aligned} \tag{3.61}$$

Eqn.(3.61) implies that the current I_D for short channel MOSFETs is linearly related to the overdrive voltage, $(V_{GS} - V_{TH})$.

3.8 Transistor design parameters

In this thesis an aspect ratio (W/L) of 5/1 was taken as the basis of the designs so that sufficient room is left for future changes that may be needed in the subsequent designs. The length (L) was kept at minimum because of the speed requirement of the proposed circuits. Thus, the following ratio was used for designing the NMOS transistor:

$$\frac{W}{L} = \frac{5}{1} = \frac{1.75}{0.35} \tag{3.62}$$

In order to evaluate the square law equation, the following calculations are required: The dielectric constant, ε_{ox} of S_iO_2 is given by

$$\varepsilon_{ox} = \varepsilon_o \varepsilon_r \tag{3.63}$$

where ε_0 is the dielectric constant of vacuum and ε_r is the relative dielectric constant of S_iO_2. Thus the value of ε_{ox} is calculated as

$$\varepsilon_{ox} = \varepsilon_o\varepsilon_r = 3.97\varepsilon_o = 35.1511^{pF}/_{m} \tag{3.64}$$

The S_iO_2 thickness, $t_{ox} = 7.575nm$ is made available in the TSMC process and therefore, oxide capacitance, C'_{ox} can be calculated as

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 4.64^{fF}/_{\mu m} \tag{3.65}$$

The transconducatnce gain parameter, KP_n can be calculated using the mobility coefficient provided by the TSMC process and eqn.(3.65) as follows:

$$KP_n = \mu_n C'_{ox} = \left(47.58 \times 10^{-3}\right)\left(370 \times 10^{-5}\right)\mu A/V^2 \tag{3.66}$$

Taking the value of V_{TH} from the process parameters along with the values calculated above and appropriate supply voltages, preliminary transistor biasing can be performed by looking into the I-V characteristics, for a sweep of v_{GS}.
In order to maintain power consumption at a lower level, a drain current of $30A$ was considered since an $I_D = 30\mu A$ drives the transistor into saturation. The amount of v_{GS} required to obtain the required drain current can be calculated as follows:

$$\begin{aligned} V_{GS} &= \sqrt{\frac{2I_D}{KP_n}\left(\frac{W}{L}\right)_n} + V_{TH} \\ &= 0.8V \end{aligned} \tag{3.67}$$

The above calculations are equally applicable to PMOS devices as well. Since the mobility of holes is lower than that of electrons, it is a common practice to adjust the width of the transistor to account for this and obtain similar results. The required width of the PMOS transistor is calculated as follows using the adjustment factor.

$$\frac{\mu_n}{\mu_p} = \frac{370cm^2/V.s}{126cm^2/V.s} = 2.94 \cong 3 \tag{3.68}$$

Thus, the width of the PMOS device should have a relation with the width of the NMOS device as stated below:

$$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n \tag{3.69}$$

Therefore,

$$W_p = 3W_n \tag{3.70}$$

The aspect ratio of the PMOS device is thus given by

$$\left(\frac{W}{L}\right)_n = \frac{15}{1} = \frac{52.5\mu m}{0.35\mu m} \tag{3.71}$$

A brief summary of the basic design parameters of the NMOS and PMOS transistors used in this thesis are presented in Table 3.6 below.

Table 3.6: Summary of device parameters used in the thesis

Parameter	PMOS	NMOS
I_D (Bias current)	$30A$	$30A$
W/L(Typical)	15/1	5/1
V_{TH}	0.699	0.499
KP	$58\mu\text{A/V}^2$	$176\mu\text{A/V}^2$
t_{ox}	7.575 nm	7.575 nm
$C_{ox} = \varepsilon_{ox}/t_{ox}$	$4.64\mu\text{f/m}^2$	$4.64\mu\text{f/m}^2$
V_{GS}	$0.98V$	$0.8V$
$V_{DS,sat}$	$261mV$	$260mV$

3.9 Summary

Basic radio frequency concepts and principles governing RF signals have been revisited. Important radio frequency performance parameters and circuit design techniques have been discussed briefly.

As CMOS devices are at the core of this work, a brief review of MOSFET physics is presented. Both long and short channel devices and their distinguishing features are discussed. It is observed that long and short-channel devices exhibit different behavior caused by the difference in mobility with electric field. It is observed that a function of electric field strength distinguishes long from short channel devices. As electric field is dependent on length long channel devices do not exhibit these high field effects as readily as short channel devices do. MOSFET scaling theory along with MOSFET parameters and scaling parameters are also discussed which is not exhaustive but provide some important skills for CMOS RF circuit design. Some popular MOSFET models and their extension to RF applications have also been presented.

Chapter 4

Design of the Proposed FHSS Transmitter

4.1 Introduction

In the preceding chapter the design principles of radio frequency circuits are described. The aim of this chapter is to identify, design and simulate the various analog, digital and mixed signal subsystems required by the proposed transmitter. Since it is proposed to design the transceiver using CMOS technology, a brief summary of MOSFET models, process parameters, design of digital and analog cells using MOSFETs are incorporated in this chapter. The primary focus of this thesis is the design of multichannel FHSS based transceiver and therefore the design of antenna and RF power amplifier are considered to be out of scope of this thesis.

4.2 Proposed transmitter building blocks

A generalized block diagram of the proposed multichannel FHSS transmitter has been shown in Fig.4-1. As the proposed work involves 4 channels, we need to generate PN sequences for 4-bit data words as detailed below. PN sequence generator whose characteristics were described in chapter 2, are designed for 4-channel system to generate 15 PN sequences. The code sequence selector which selects one of the available PN sequences for further processing was custom-designed using the MOSFET described in chapter 3. The output of the PN sequence selector is fed to serial-to-parallel (S2P) converter, the output of which is then applied to a two-bit digital-to-analog converter (DAC). The DAC output is finally applied to voltage controlled oscillator (VCO) which

was also custom-designed. Two different types of VCOs were designed and employed for conversion of the analog output of the DAC, which represents the modulated signal of the corresponding sinusoidal signals.

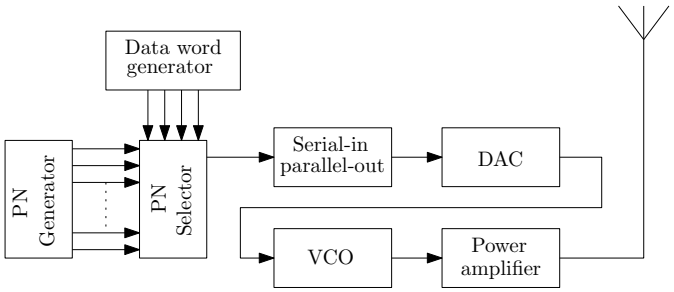


Figure 4-1: Generalized block diagram of the FHSS transmitter

4.2.1 Design of Digital Subsystems

The analysis of digital subsystems here is done from an overview perspective only as most of the text books on CMOS digital design cover these topics in details [105, 106]. Furthermore, not all digital cells are custom-designed as the EDA tool provides such cells as part of its digital library. Instances where the cells are custom-designed have specific mentions.

4.2.1.1 Design of Data word generator

The role of data word generator is to generate 4-bit data word which resembles the four channels. The data word generator consists of four JK flip-flops connected in serial-in serial-out fashion as shown in Fig.4-2. The clock that drives the data word generator is derived from the PN generator divided by mod-15 counter so that the PN sequence from the PN generator and that generated by the data word generator remain in the same phase. The working of the data word generator may be explained with the help the

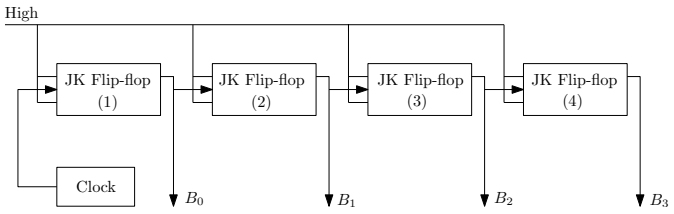


Figure 4-2: Block diagram of Data word generator

block diagram depicted in Fig.4-2. As seen in the figure, the output of the first flip-flop triggers the second flip-flop, output of the second flip-flop triggers the third flip-flop and so on. Thus, by tapping out the output of each flip-flop, we get a 4-bit word given by

(B_3 B_2 B_1 B_0) as shown in Fig.4-3. This 4-bit data word forms the address word for the PN code selector module which is a 16 : 1 multiplexer constructed out of two 8 : 1 and one 2 : 1 multiplexer. This 4-bit word is used to select one of the PN sequences out of 15 sequences produced by the PN sequence generator.

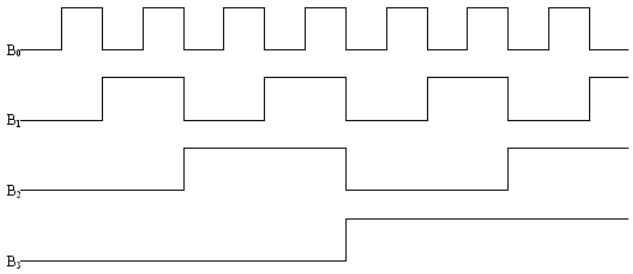


Figure 4-3: Output wave form of data word

4.2.1.2 Circuit design and simulation

The 4-bit data generator was constructed by using four JK flip-flops configured to operate in the master-slave mode. The JK flip-flops were designed using two-input and three input NAND gates which were custom-designed using the MOSFETs described in chapter 3. As usual, the J input acts as set and the K input as reset. The operation is similar to the RS flip-flop except for J = K = 1, when the output of the flip-flop toggles or changes state each time the flip-flop is clocked. The circuit diagram of the nand-based JK flip-flop is depicted in Fig.4-4. The delay elements are used to avoid the metastability. The master stage captures the input and holds it constant and the slave stage copies the previously captured input to the output terminals and holds it constant while the next input is captured. The inverter introduced in the clock signal path to ensure that the master stage operates on the rising edge of the clock pulse and the slave stage on the falling edge. The simulation result of the JK flip-flop circuit of Fig.4-4, depicted in Fig.4-5 describes the operation of the flip-flop.

4.2.1.3 Design of data word generator

The 4-bit data word generator circuit was designed using four master-slave JK flip-flops as described in Fig.4-4 above and simulated in AWR Microwave Office (version 9.05). The detailed circuit diagram is given in Fig.4-6. The input and output terminals are terminated with ports so as to enable this circuit to be used as subcircuit in the transmitter hierarchy. It is found that the simulation result shown in Fig.4-7 agrees with the theoretical result. The delay elements introduced in the feedback loops are purely EDA tool requirements and does not affect the performance of the circuit anyway. The

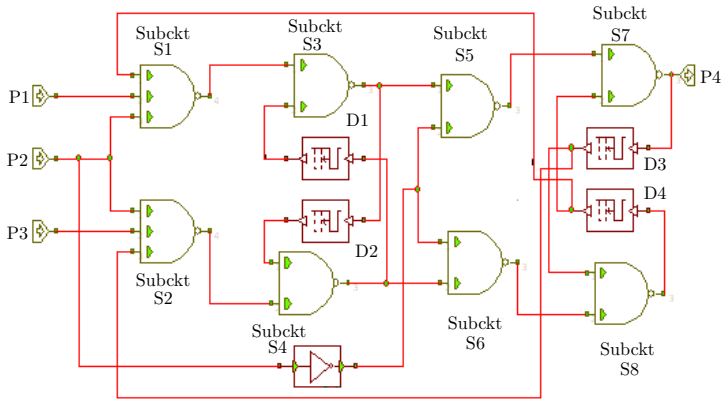


Figure 4-4: Circuit diagram of JK master-slave flip flop

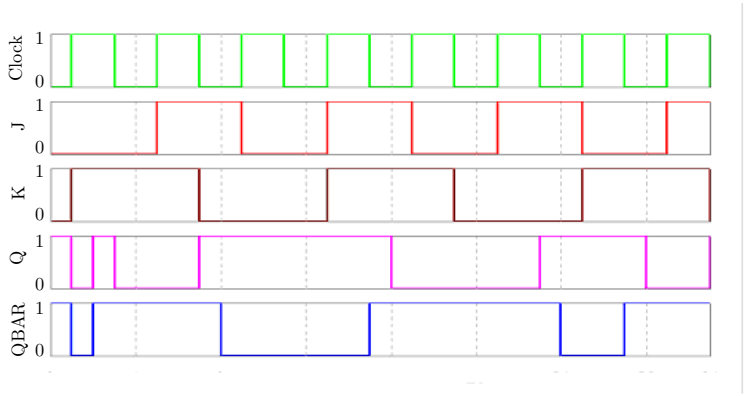


Figure 4-5: Timing diagram of master-slave JK flip-flop

circuit of Fig.4-6 was simulated in AWR Microwave Office (version 9.05) and the resulting output waveforms are shown in Fig. 4-7 along with the input waveforms.

4.2.1.4 Design of PN sequence generator

The PN sequence generator described in chapter 2, which is a maximal length shift register (MLSR) was designed using D-flip flops as shown in Fig.4-8. The top four D-flip flops along with the XOR gate and the delay element constitute the PN sequence generator while the bottom fifteen D-flip flops accomplish the shifting function. The initial input to the first D-flip-flop of the PN generator is set to 'high'with the help of preset circuitry (resistor, capacitor and XNOR gate). The output of different D-flip flops of the MLSR at every clock pulses is tabulated in Table 4.1. The 15 different PN sequences are generated by feeding the output of the first D-flip-flop of the MLSR to a network of serially connected 15 D-flip-flops as shown in Fig.4-8. The network of 15 D-flip-flops is initially set to the first PN sequence as obtained from the output of the first D-flip-flop of the MLSR. The outputs of the serially connected 15 D-flip-flops

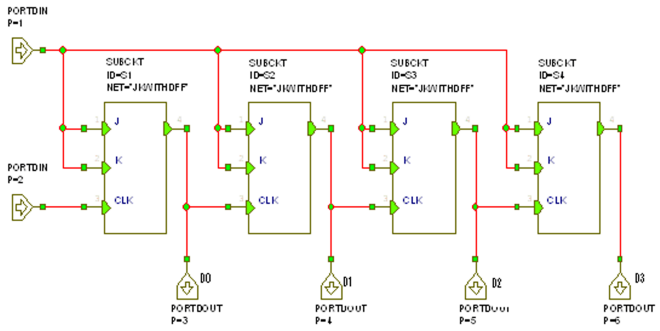


Figure 4-6: Circuit diagram of 4-bit data word generator

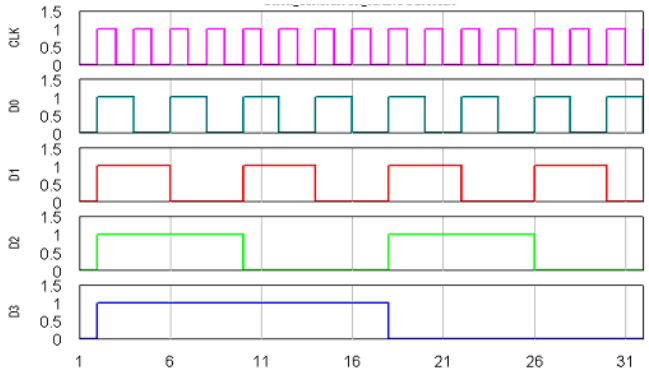


Figure 4-7: Timing diagram of 4-bit data word generator

are tapped out in parallel and are the PN sequences obtained at each clock pulse. The same clock is used for both the MLSR and the D-flip flop shifting network to keep the responses in phase with that of PN generator. These sequences are fed to the multiplexer and are selected according to the control inputs provided by the data word generator. The sequence repeats every 15 clock pulses. The combined circuit consisting of the PN generator and the shifting network shown in Fig.4-8 was simulated using Microwave Office and the resulting wave forms are shown in Fig.4-9.

4.2.1.5 PN Sequence selector design and simulation

The PN sequence selector described in Fig.4-10, is basically a $16:1$ multiplexer constructed with two $8:1$ multiplexers and one $2:1$ multiplexer. The inputs to the PN selector circuit are the 15 different PN sequences from the PN sequence generator and the control inputs are the outputs of the 4-bit data word generator which represents the four channels. The outputs of the PN sequence selector are fed to the serial-to-parallel converter in order to facilitate digital-to-analog conversion. The logic gates employed in the construction of the multiplexer were designed using the MOSFETs described in chapter 2. The circuit of Fig.4-10 was simulated in Microwave office and the simulation results are shown in Fig.4-11. It may be seen that the simulation results obtained satisfy the theoretical expectations and thereby establishes the correctness of the design.

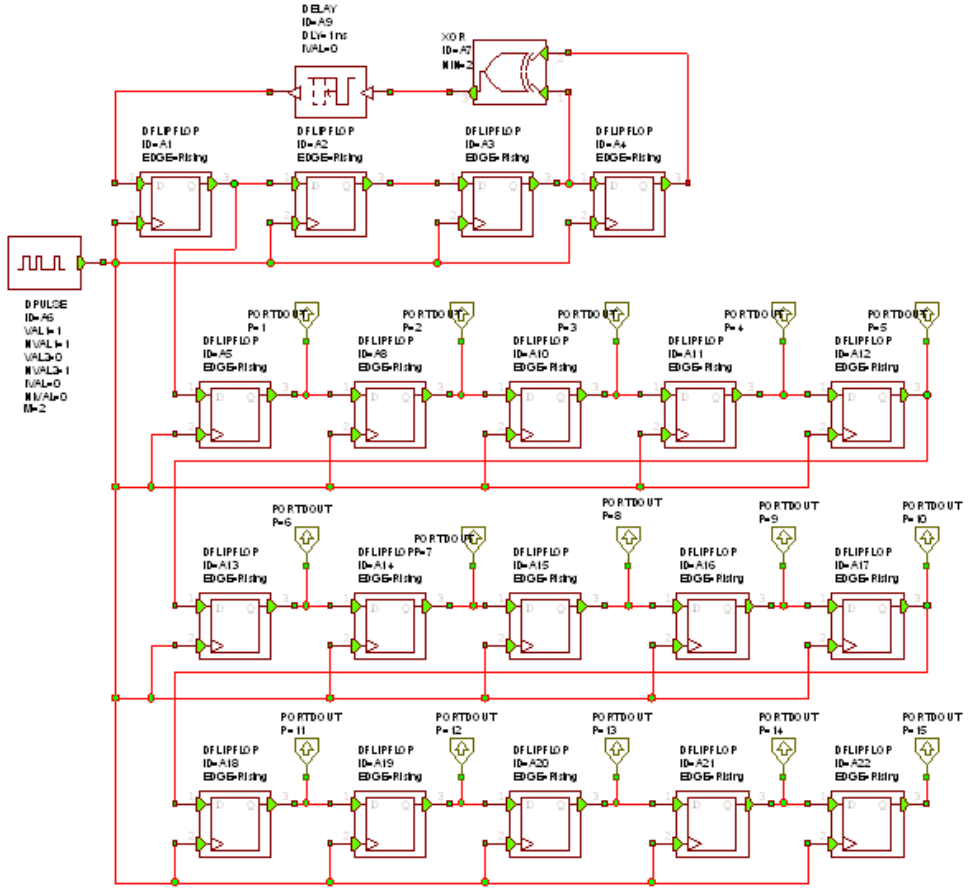


Figure 4-8: Circuit diagram of PN generator and shifting network

4.2.1.6 Serial-to-parallel converter

Serial-to-parallel converter is a type of register in which data is shifted in serially but shifted out in parallel. This type of register also known as serial-to-parallel converter can be constructed with the help of D-flip- flops as shown in Fig.4-12. The outputs of each of the flip-flops are tapped out and the input PN code is thus converted to two-bit parallel output. The two-bit parallel converter was designed with the help of D-flip flops which were constructed using the MOSFETs described in chapter 2. The serial-to-parallel converter circuit as described above is shown in Fig.4-13 while Fig.4-14 depicts the input/output waveforms of the converter.

4.2.1.7 Design of Digital-to-Analog converter (DAC)

A digital-to-analog converter produces an analog output A which is proportional to the digital input D. That is $A = \alpha^{'}D$, where $\alpha^{'}$ is the proportionality factor. Since D is a dimensionless quantity, $\alpha^{'}$ sets both dimension and full-scale range of A. In more general form, we can write $A = \alpha^{'}D \Big/ 2^{m}$ where D is normalized with respect to its full-scale

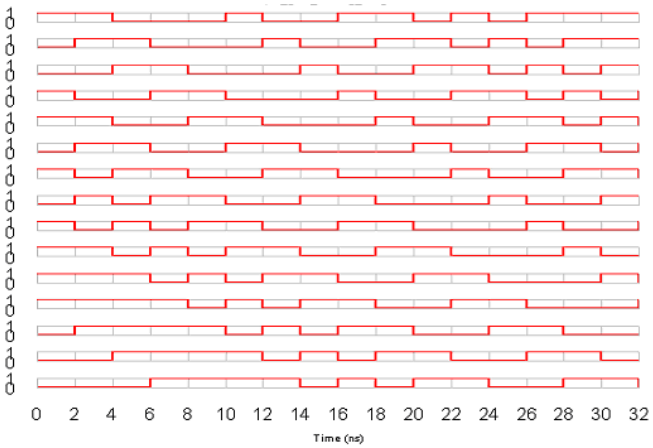


Figure 4-9: PN generator output waveforms

Table 4.1: Input and output of PN generator

Clock pulse	Initial state	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Flipflop(1)	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0	1
Flipflop(2)	0	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0
Flipflop(3)	0	0	1	1	1	1	0	1	0	1	1	0	0	1	0	0
Flipflop(4)	0	0	0	1	1	1	1	0	1	0	1	1	0	0	1	0
XOR O/P	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0	1

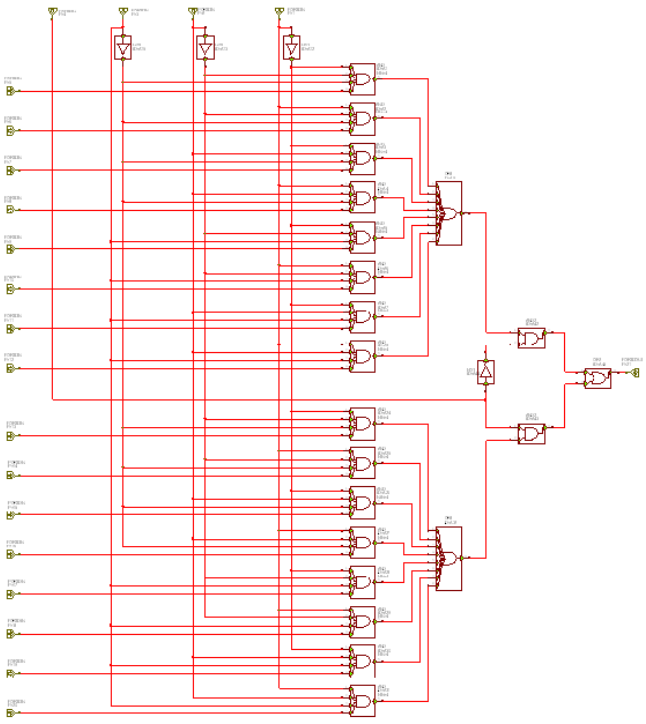


Figure 4-10: Circuit diagram of PN sequence selector

value 2^m and m is the resolution.

It is now obvious from the above discussion that each code at the digital input generates

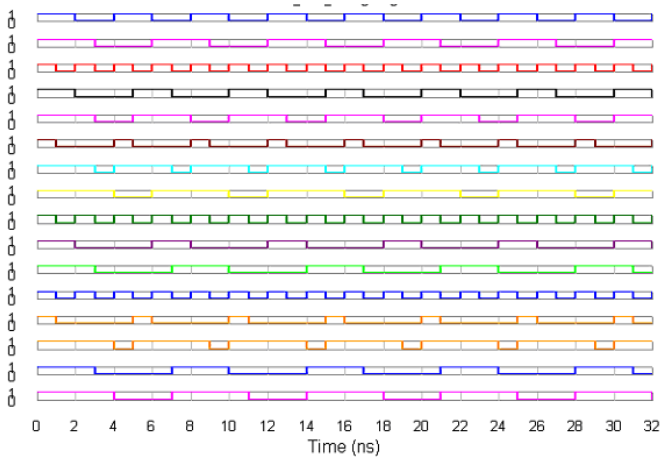


Figure 4-11: Output waveforms of PN sequence selector

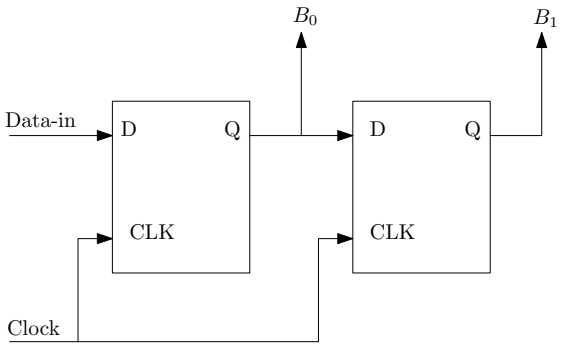


Figure 4-12: Serial-to-parallel converter

voltage, current or charge which defines the DAC architecture as voltage scaling, current scaling or charge scaling.

The popular R2R ladder network has been employed in this work due its inherent features like charge distribution and less layout area requirement.

There are basically two categories of R2R DAC named as current mode and voltage mode DAC. The major shortcoming of current mode DAC arises due to the limited output swing of the op amp used. This shortcoming of limited output swing associated with the current mode DAC can be eliminated by using voltage mode DAC, however, the finite CMMR of the op amp used can affect the linearity of the overall DAC. The ordinary R2R ladder without op amp can drive arbitrary load impedance and they also offer higher speed and stability apart from ratifying non-idealities associated with op amps. The R2R ladder network without op amp which is employed here and simulated in Microwave Office is shown in Fig.4-15 while Fig.4-16 depicts the simulation results.

4.2.2 Design of Analog subsystems

The most critical analog subsystem identified in the transmitter section of the proposed transceiver is the voltage controlled oscillator (VCO). A brief survey of the various types

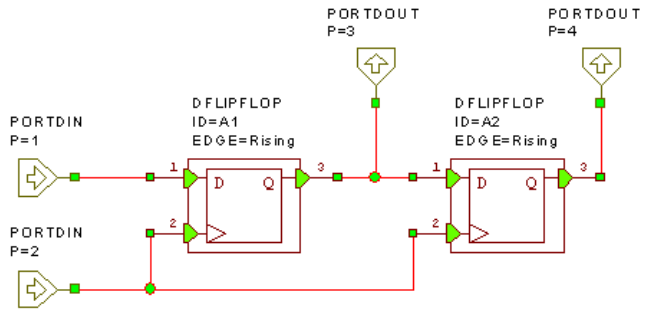


Figure 4-13: Serial-to-parallel converter circuit diagram (2-bit)

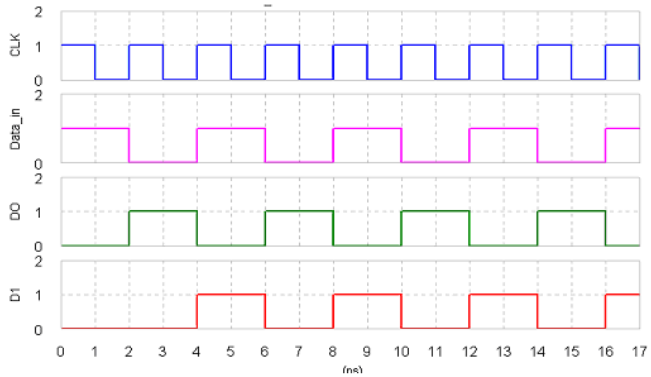


Figure 4-14: Input-output waveform of serial-to-parallel converter

of VCOs and their merits and demerits are incorporated in the following section. Based on the study performed, a new architecture of the ring VCO has been developed and its performance parameters are compared with published works.

4.2.2.1 Design of Voltage controlled oscillator

Voltage controlled oscillator is a device whose output signal frequency is controlled by the analog input signal. Based on the method of oscillation, VCO's can be categorized as resonator-based oscillators, such as LC oscillators and waveform based oscillators, such as ring oscillators [Fig.4-17]. The frequency tuning in ring oscillator is performed by current steering while LC oscillators use variable capacitors (varactors). There exists another waveform-based VCO, known as relaxation VCO. This relaxation VCO uses positive feedback which results in large phase noise and hence not a good choice for the present application [105]. Because of the need of integrability, current-starved ring oscillator is desirable for the present application. Although the ring oscillators suffer from inferior phase noise performance compared to tuned oscillators but their strong attributes like large tuning range and simplicity make them attractive for many applications similar to the present one. A number of low voltage controlled oscillators operating at less than 1V supply voltage have been reported [105, 107–110]. But most of the circuits suffer from either reduced voltage swing or degraded phase noise perfor-

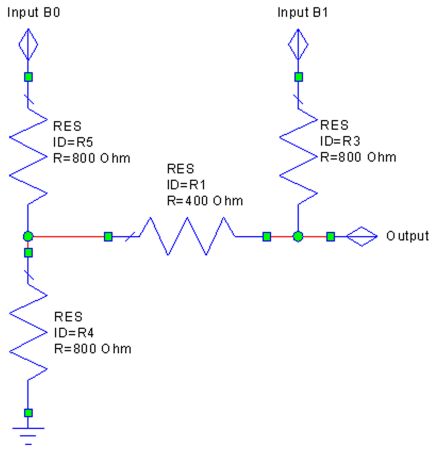


Figure 4-15: R2R ladder network without Op Amp

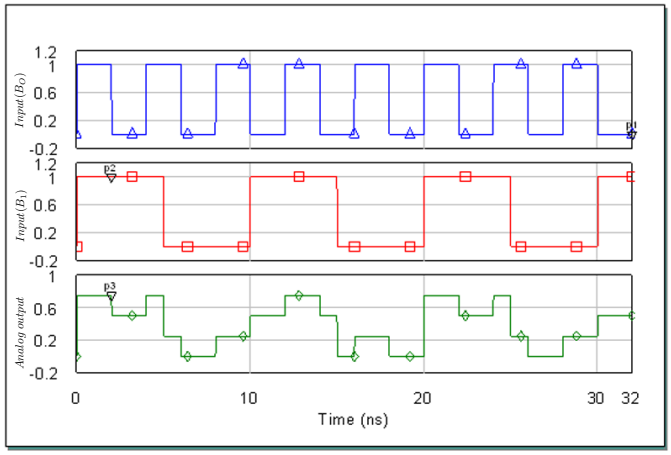


Figure 4-16: Input-output wave forms of DAC

mance due to power supply limitation [111]. The design of ring VCOs involve many trade-offs such as speed, power, dye area and application domain [112]. The proposed ring VCO mainly focuses on architectural innovation and trade-off among the attributes like voltage swing, frequency tuning range, phase noise performance and frequency stability.

The basic ring oscillator structure appears as shown in Fig.4-18. The effective propagation delay of each inverter of the ring oscillator is controlled by a current source as seen in Fig.4-19. The controllable ring oscillator consists of n number of inverters in a ring, where n is odd. It may be assumed for analysis purpose that a propagation delay T_{pd} is associated with each inverter and in the absence of stable d.c. point, a logic level propagates around the loop resulting in one net inversion each round trip. In other words, each delay element provides a phase shift of π/n while the remaining phase shift $(2\pi - (\pi/n))$ is provided by the d.c. inversion [113, 114].

The oscillation period is thus simply twice the propagation delay. Thus, the oscillation frequency can be expressed as

$$f_{osc} = \frac{1}{2n.T_{pd}} \tag{4.1}$$

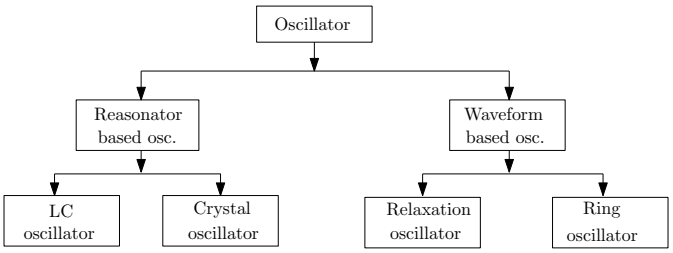


Figure 4-17: Classification of VCO

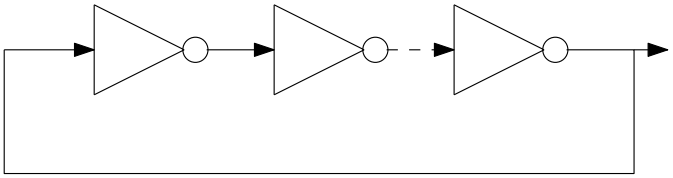


Figure 4-18: Basic ring oscillator

It can be revealed from eqn.(4.1) that the propagation delay is the most natural quantity to be adjusted in order to convert the structure into a controllable ring oscillator. One of the most effective ways to accomplish the adjustment of propagation delay is by varying the current drive of the inverters, where a PMOS current mirror is used to provide limited and variable pull-up current to the CMOS inverter. The oscillation frequency can be altered by adjusting the pull-up current.
The topology chosen for the present application is somewhat similar to the current-starved ring oscillator topology evolved in [115] using genetic algorithm (GA). Here the maximum number of blocks per stage was considered as 4 and maximum number of rows per stage was taken as 2. The proposed VCO is designed using the PMOS current mirror like any other current starved CMOS ring VCO, but does not use the PMOS current source in series with each of the inverter stages. In order to maintain stable current, the aspect ratio of the NMOS current sink in series with the inverter is increased which results in increased small signal output resistance [116].

It is a four stage VCO whose output signal frequency is expected to vary with input voltage. The current through the current mirror increases with increase in input voltage and as a result output frequency increases. The maximum number of blocks per stage was considered 4 and maximum number of rows per stage was taken as 2 for simulation purposes. The architecture was realized with RF models of BSIM4 described in chapter 2.
The circuit shown in Fig.4-20 was subjected to transient simulation in Microwave Office (version 9.05). The simulation results depicted in Fig.4-21 is obtained by applying A 3.5V supply while Fig.4-22 shows the simulations results when the DAC output is used as tuning voltage of the VCO.
Since the S2P converter provides 2-bits in parallel, we get four different analog voltage levels equivalent to 00, 01, 10 and 11. As a result we have four different frequencies at

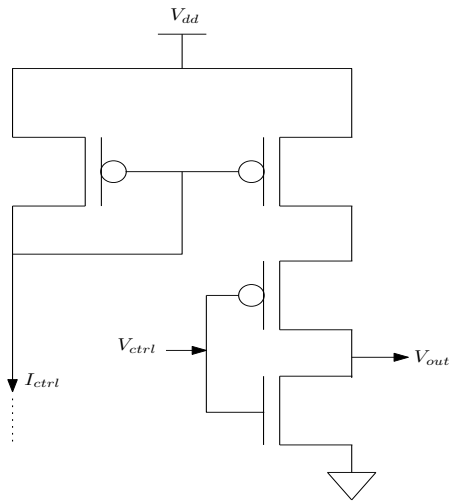


Figure 4-19: Simplified current-starved CMOS inverter

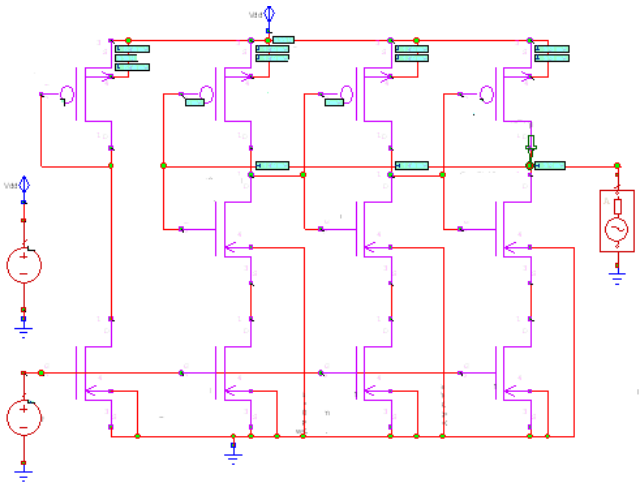


Figure 4-20: Circuit diagram of the proposed VCO

the VCO output corresponding to the four analog voltage levels.

VCO Phase noise

Noise is introduced in the oscillator by the active and passive devices that constitute the oscillator itself. Both the amplitude and phase of the oscillator output are disturbed by this noise. The effect of amplitude noise does not cause any serious problem because it is stabilized by the non-linearity that limits the amplitude of oscillator output. Phase noise, on the other hand, is cumulative and can adversely affect the performance of the communication system since it is essentially a random frequency deviation which may also be viewed as random variation in the zero-crossing points of the time-domain waveform of the oscillator.

Let us consider

$$\gamma(t) = A\cos\left[\omega_0 t + \phi_n(t)\right] \tag{4.2}$$

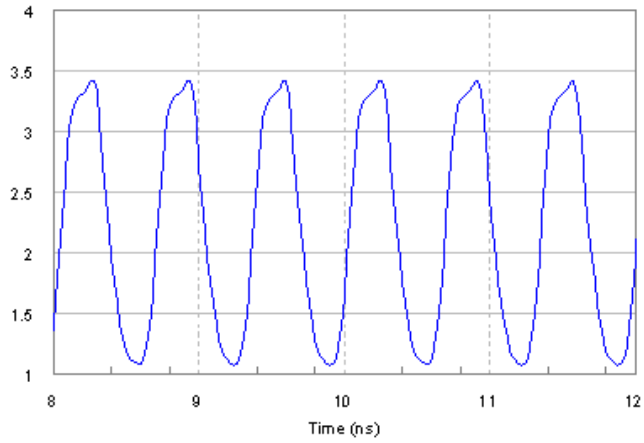


Figure 4-21: Output of the proposed VCO

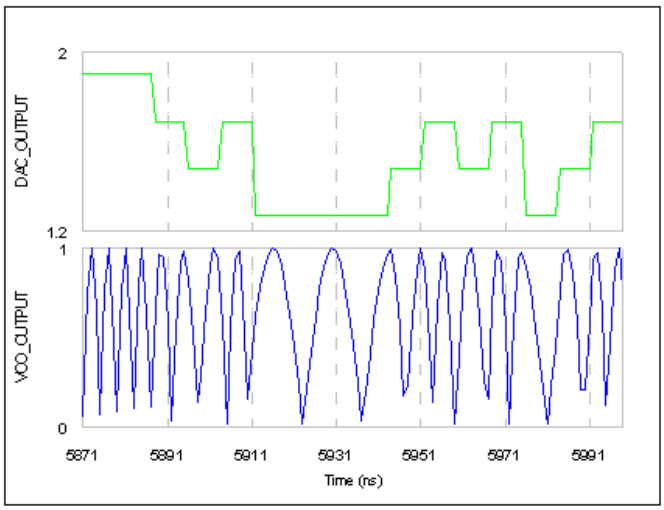
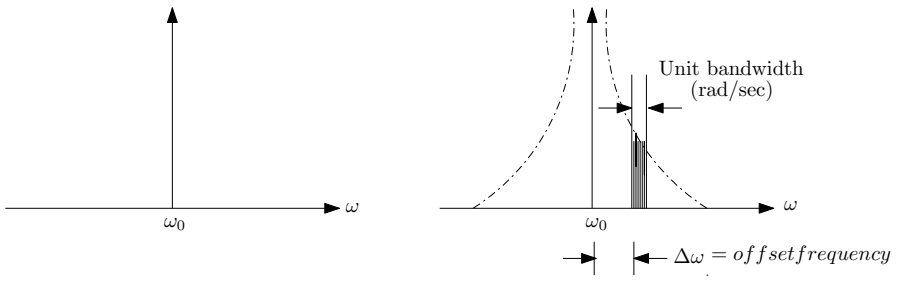


Figure 4-22: Input and output waveforms of VCO

where A = Noiseless oscillator amplitude, ω_0 = Oscillator frequency, $\phi_n(t)$ = Phase noise and $\gamma(t)$ = Oscillator output signal.
Now, for small values of $\phi_n(t)$, we have

$$\begin{aligned}\gamma(t) &= A\cos[\omega_0 t + \phi_n t] \\ &= A[\cos(\omega_0 t)\cos\phi_n(t) - \sin(\omega_0 t)\sin\phi_n(t)] \\ &\approx A\cos(\omega_0 t) - A\phi_n(t)\sin(\omega_0 t)\end{aligned} \tag{4.3}$$

Since, $\cos(\phi_n(t)) \approx \cos(0) \approx 1$ and $\sin(\phi_n(t)) = \phi_n(t)$ for small $\phi_n(t)$. Therefore, the spectrum of noise is effectively translated to the oscillation frequency ω_0. In other words, the phase noise signal amplitude modulates the sinusoidal signal with frequency ω_0. An oscillator is by nature frequency selective, narrow band and high Q circuit and therefore has a tendency to reject out-of band signals to some extent. As a result, the effect of noise sources appears as "skirts" on either side of ideal impulse response of the oscillator in frequency domain as shown in Fig.4-23. This rejection increases for larger values of offsets from ω_0. In order to quantify or measure phase noise, a unit bandwidth



(a) Ideal oscillator (b) Actual oscillator

Figure 4-23: Illustration of phase noise in frequency domain a)Ideal oscillator and b)Actual oscillator

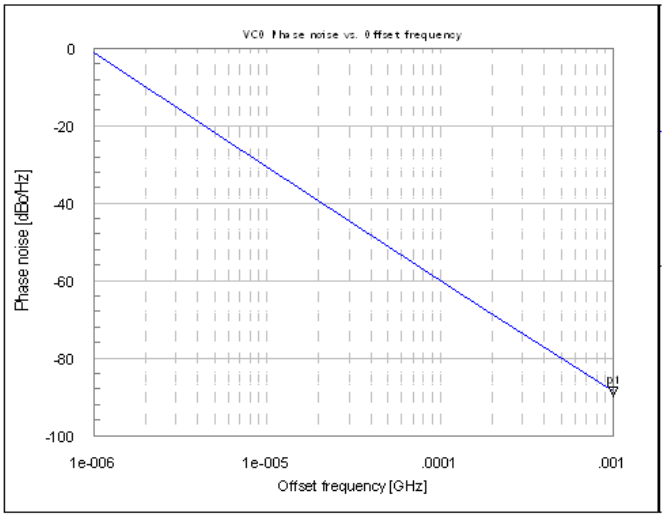


Figure 4-24: VCO phase noise vs. offset frequency

at an offset $\Delta\omega$ with respect to ω_0 is considered and the noise power in this bandwidth is calculated and finally this noise power is divided by the average carrier power.
The VCO circuit shown in Fig.4-20 was simulated for phase noise in AWR Microwave Office tool and the resulting phase noise vs offset frequency response obtained is shown in Fig.4-24.

4.2.2.2 Simulation results and performance comparison

The results obtained by simulating the proposed VCO architecture are presented in Table 4.2 along with some previous works. It can be observed from the table that the proposed VCO in spite of using a different technology, the performance in terms of frequency tuning range is good enough compared to the reported works. The phase noise achieved is reasonably good while the device count and hence die area and power

Table 4.2: Performance comparison of the proposed VCO

Ref. –	Process Technology	No. of stages	Frequency range(GHz)	Tuning range(%)	Phase noise(dBc/Hz)	Offset freq.(MHz)
[111]	0.18μmCMOS	–	5.1-5.2	8.9	-97	1
[117]	0.13μmCMOS	2	1.82-10.18	139.4	-88.4	1
[118]	0.18μmCMOS	$4^{(1)}$	0.4-4.2	–	-121.2	4
[119]	0.12μmCMOS	5	8.4-10.6	23	-85	1
[120]	0.25μmCMOS	4	4.22-5.43	25	-98.5	1
[121]	0.6μmCMOS	4	0.75-1.2	46.2	-117	0.6
[122]	0.18μmCMOS	5	4.3-6.1	35	-85	1
This work	0.35μm**CMOS**	3	0.7-1.75	75	-88	1

requirement is less.

4.3 Summary

This chapter begins with a brief overview of MOSFET models and process parameters. Concept of the proposed FHSS transmitter has been described and the analog, digital and mixed signal subcircuits required for the construction of the transmitter are identified. All these subcircuits are designed and simulated in this chapter. Performance of the most important analog sub-circuits has been compared with previously published works.

Chapter 5

Design of the FHSS Receiver

5.1 Introduction

The receiver section of the proposed transceiver architecture has been conceptualized in this chapter. Each of the essential analog, digital and mixed signal subsystems were identified, designed and simulated. The first order high pass active filter, multiplier, comparator, integrator and differentiator employed in the construction of the receiver are based on RF op amp. All the analog, digital and mixed signal subsystems were designed using RF model of BSIM3v3 made available in Microwave Office by AWR Inc.

5.2 Receiver concept and design

The receiver architecture proposed in this thesis is relatively more complex compared to the transmitter. The block diagram shown in Fig.5-1 depicts the proposed architecture. Although the digital and mixed signal subsystem designs are incorporated in this thesis, the emphasis is on removing the bottlenecks of the analog front-ends.
The receiver section comprises of two key functional analog circuit blocks, the low noise amplifier (LNA) and the frequency-to-voltage converter (FVC) and four digital circuit blocks and two mixed signal circuits as shown in Fig.5-1.
The design descriptions of each of the blocks are given in the sections to follow in a step-by-step manner.
Bottom-up approach was adopted for designing the receiver system, i.e., individual circuit elements were designed and simulated first and these circuit elements were used as sub-circuits in the next higher level units or subsystems until the complete FHSS receiver system was accomplished and validated through simulation.

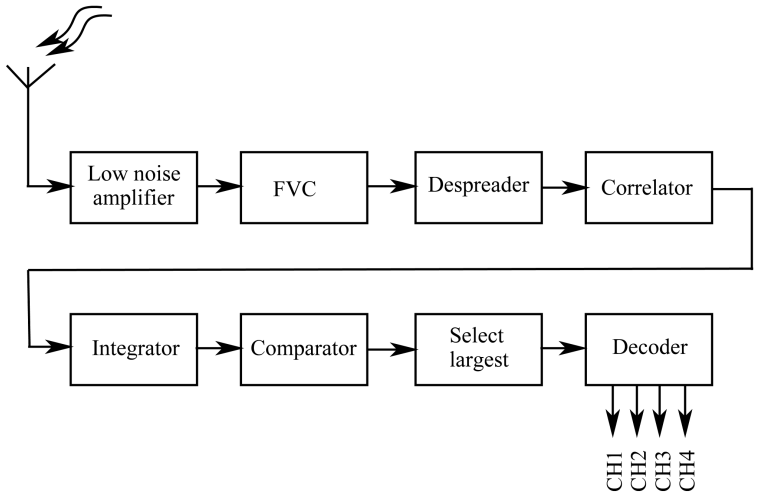


Figure 5-1: Block diagram of the proposed receiver

5.3 Design of Analog Sub-systems

The analog sub-systems of the receiver are conceptualized through extensive analysis of the reported works. The design descriptions of each of the subsystems and their performance analysis are presented in the sections to follow.

5.3.1 Low noise amplifier

Low Noise Amplifier is a special type of amplifier capable of amplifying very weak signals picked up from the noisy signals available from the receiving antenna. LNA is usually placed very close to the antenna and it forms the first RF front-end of the receiver. As such, it has great impact on the overall noise performance of the receiver. It also plays an important role in achieving the desired quality factor of the receiver system. The noise generated by all the subsequent stages can be reduced by using LNA except the noise directly injected by the LNA itself into the desired signal. That is why LNA should essentially pick up the desired signal power and add the least possible noise and distortion to achieve optimum receiver sensitivity. Though high gain LNA's are desired in order to reduce the noise contributions of the later stages, a very high gain may sometimes degrade the overall system linearity. The key features of LNA design may be summarized as follows:

- High gain
- Low noise figure (NF)
- Stability
- Good linearity

- Minimum device complexity
- Minimum power consumption
- Maximum power output

The design of LNA basically involves trade-offs amongst closely related features such as gain, noise figure, stability, power consumption and complexity [123]. Low power, low voltage and ability to operate over wide temperature range and frequency are always the design targets for LNA designers to make it suitable for any good receiver section.

5.3.1.1 Low noise amplifier topologies

Many LNA topologies have been reported in the literature. The following are the most popular and widely used LNA topologies:

- Distributed amplifiers [124]
- Resistive shunt feedback amplifiers [125]
- Cascade amplifiers [126]
- Current reuse amplifiers [127]

Most of the high frequency LNAs such as L-band ($1-2$ GHz), X-band ($8-12.5$ GHz), Ku-band ($12.5-18$ GHz) are designed in GaAs, CMOS, JFET, PHEMT and MOSFET technologies and are used in wide variety of applications such as aircraft, wireless communication, radar systems, global positioning system (GPS) applications and radio astronomy.
In order to design a good receiver section, the LNA needs to be featured by low power, low voltage and ability to operate over a wide temperature range yet capable of providing better performances. Several LNA topologies exist for wide band amplifiers in CMOS technology [123]. The distributed amplifiers can provide considerably high gain-bandwidth product (GBW) at the cost of large power and area [128]. The shunt feedback amplifiers provide wide band matching capability at the cost of high power consumption in order to achieve the desired noise performances [129].
For better performance of LNA, it is required to fix the Q factor in the input matching circuit. It is seen in the previous works that L-section matching networks can fix the Q factor uniquely unlike other configurations. It is also an established fact that π- sections have an extra degree of freedom that allows controlling the bandwidth of the matching network as desired.
In the present application, the LNA is designed with L-section matching network in the

input port while π-section matching network is used in the output port. The block diagram shown in Fig.5-2 depicts the proposed architecture and illustrated in the following sections with the help of circuit diagram and simulation results.

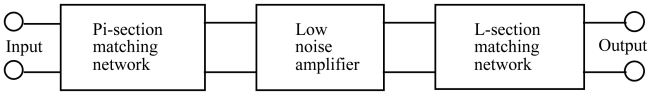


Figure 5-2: Basic block diagram of Low noise amplifier

5.3.1.2 Design description and simulation results of the proposed LNA

The LNA architecture proposed in the previous section is designed and simulated in Microwave Office. As seen in the circuit diagram (Fig.5-3), the input matching circuit consists of capacitors C_1 and C_2 which model the parasitic capacitances associated with the input pad in parallel with the inductor L_1.
The cascode transistors M_1 and M_3 improve the reverse isolation and also lower the Millers multiplied capacitance. The load of the amplifier consists of inductor L_2 and resistance R_1. The transistor M_2 inserted prior to the output port acts as a buffer for the output to an external matching network.
The L-section matching network which can match an arbitrary load to an arbitrary source is used as the input matching network for the proposed LNA. The bandwidth and Q factor are fixed uniquely by varying the parameter values. The use of reactive elements in the matching network minimizes power losses and therefore, L-section matching network consisting of C_1 and C_2 is used in the input matching network while a π-section matching network is used in the output in order to achieve higher degree of freedom of controlling the bandwidth of the output matching network. Moreover, inductive degeneration is used in the circuit to achieve higher level of noise figure (NF).
The proposed LNA was designed and simulated in Microwave Office with a 3.5V supply. The simulated input return loss (S_{11}) is found to be in the range of -9.2 dB to -25 dB in the frequency range of 0.9 GHz to 6 GHz as seen in Fig.5-4. The output return loss (S_{22}) for the same frequency range was found to be -13.3 dB to -26.2 dB as seen in Fig.5-5. The variation in dB gain with frequency is shown in Fig.5-6. It is seen in the figure that the high gain with tolerable flatness (1.7dB) for the frequency range $0.9 \sim 6$ GHz is obtained as 21 dB to 22.7 dB which is better than the results reported in [123, 128, 130] and as shown in Table 5.1. The variation of noise figure (NF) with frequency is shown in Fig.5-7. As seen in the figure, the noise figure for the frequency range 0.9 to 6 GHz is 2 dB to -2.5 dB which is reasonably good in comparison to reported results [123, 128, 130] as shown in Table 5.1.
The return loss of the input and output matching networks of the proposed work is also reasonably good in comparison to some of the reported results [123, 128]. The operat-

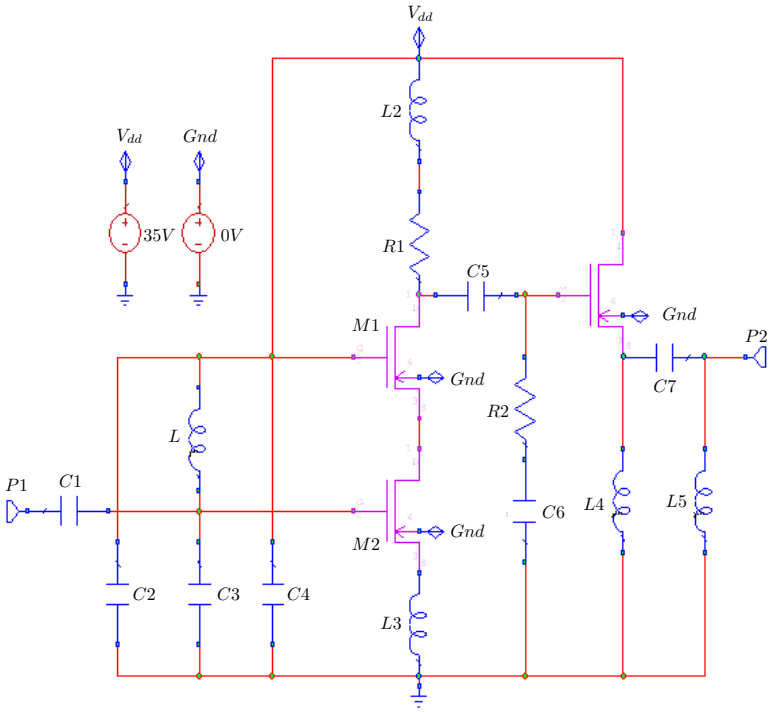


Figure 5-3: Circuit diagram of the proposed LNA

ing bandwidth of the proposed circuit covers both cellular mobile as well as WiMAX applications.

Table 5.1: Comparison of the proposed LNA performance with some reported works

Ref	BW(GHz)	Supply voltage	S_{11} (dB)	S_{22}(dB)	Gain (dB)	Noise figure(dB)	Gain flatness (dB)
[123]	$3-5$	1.8 V	<-4	<-2	$18.9-19.9$	$0.6-0.8$	± 1
[128]	$2-4.6$	1.8V	<-9	<-10	~ 9.8	$2.3-6$	–
[130]	$2-6$	1V	<-12.6	<-14.6	$13.9-14.6$	$2.5-3.5$	± 0.7
This work	$0.9-6$	0.8**V**	<-9.2	<-13.2	$21-22.7$	$2-2.5$	± 1.7

5.4 Design of Frequency-to-voltage converter

Frequency-to-voltage converter (FVC) is a device that generates an output voltage proportional to the frequency of the input signal. FVC is one of the versatile devices that find applications in many areas such as instrumentation, power control systems, low frequency signal processing, frequency meters, as a control unit in voltage controlled oscillators, tachometer read-outs in motor speed control and so on. F/V converters are also employed in phase locked loops (PLLs), frequency locked loops (FLLs), clock buffers, temperature stabilized ring oscillators and so on. The primary requirement for

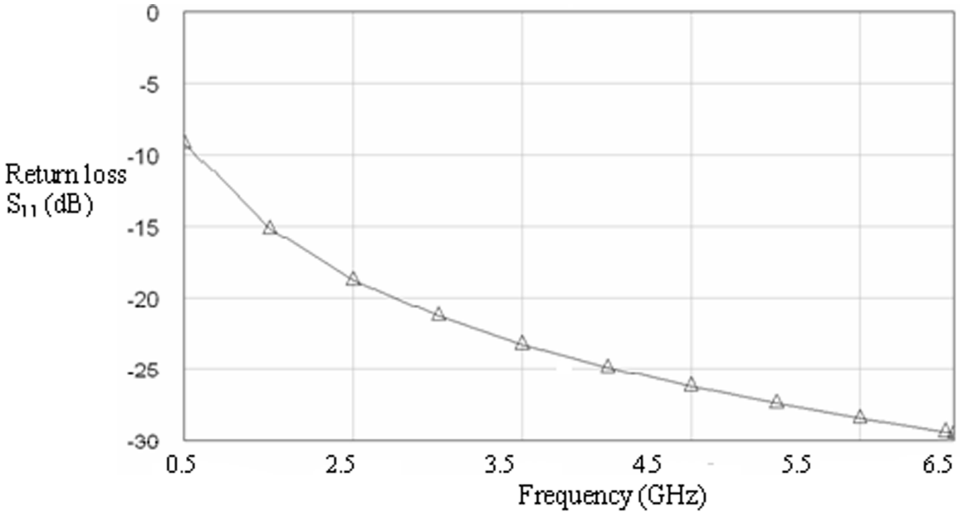


Figure 5-4: Input Return loss S_{11}(dB) vs frequency (GHz)

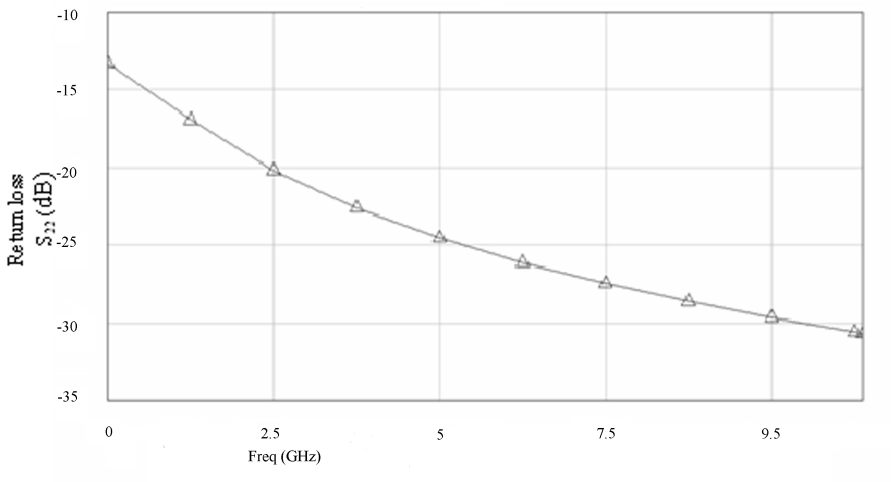


Figure 5-5: Output Return loss S_{22} (dB) vs frequency (GHz)

an efficient and good F/V converter are low ripple, good linearity, fast response and wide range of operating frequency.

5.4.1 Current state-of-art

Most of the previous works on frequency-to-voltage converters are found to be realized mainly based on two fundamental approaches. One of these approaches is based on low pass filtering of fixed duration pulses at a rate fixed by the input signal frequency [131, 132]. The other approach counts the number of pulses in a given time interval. There are numerous other approaches developed over the years for implementing frequency-to-voltage converters. Among them the most promising ones are switched-capacitor circuits, successive approximation and counter based circuits. These

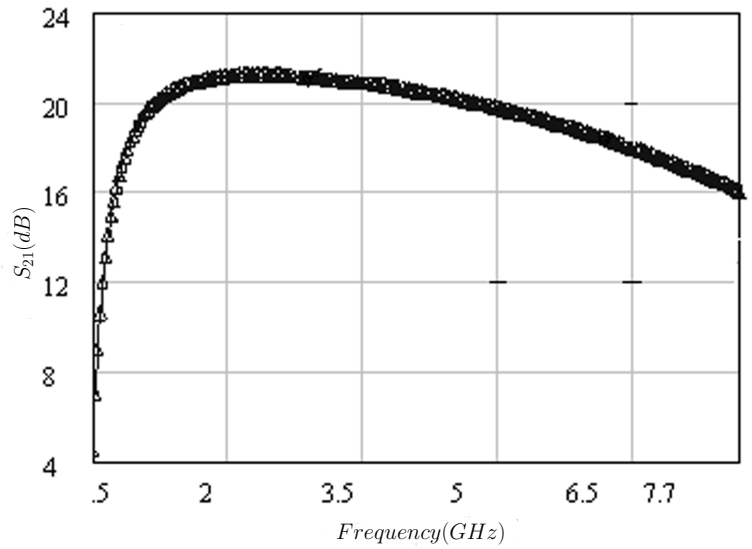


Figure 5-6: Gain vs Frequency response of the proposed LNA

approaches perform well at low and moderately high frequencies and most of them typically fail to operate in the gigahertz range of frequencies. FVCs those employ switched capacitor circuits need two-phase non-overlapping clocks and the use of operational amplifiers. Two-phase clock and operational amplifiers are not generally known to operate at very high frequencies. Thus, FVCs based on these components can therefore, achieve limited speed. The counter based FVCs, on the other hand, have the potential of achieving high accuracy provided that the reference clock speed is much higher than the measured input signal frequency. This pre-condition limits the possibility of counter based circuits to operate in the gigahertz range of frequencies.

The above frequency measuring techniques also become unsuitable when the frequency is very low and measurement of transient variation in frequency is needed. This happens because of the fact that conventional FVC circuits employ time-consuming averaging process. Most of these find limited applications because of their narrow bandwidth of operation. There exist many other methods specifically developed for low frequency applications [133, 134]. An FVC can be achieved by using a voltage-to-frequency converter or other charge balance type voltage-to-frequency converter such as $AD650$, in a phase locked loop configuration. The PLL configuration however is not used for precision frequency-to-voltage conversion because it suffers from inadequate linearity and dynamic range.

Many other methods have recently been developed for frequency measurement of purely sinusoidal signals [135, 136]. The sinusoidal frequency-to-voltage converter is used in communication subsystems like automatic frequency control (AFC), measurement of carrier frequency drift of RF signal after demodulation and so on. Most of the works on sinusoidal F/V converter reported in the literature perform analog or numerical computation on successive samples of the input signal and thus suffers from narrow range of input signal frequency. One approach has been reported [137] which performs math-

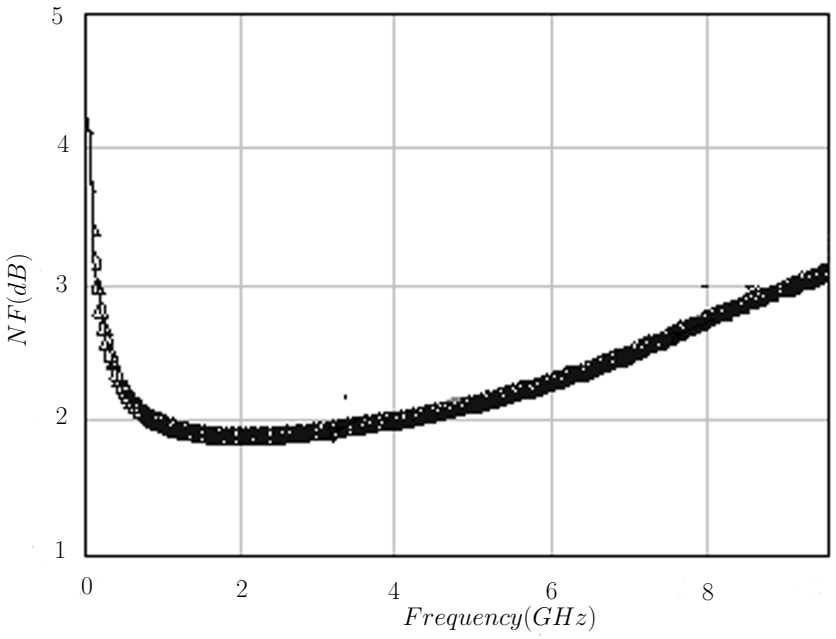


Figure 5-7: Noise Figure (NF) vs. frequency response of the proposed LNA

ematical calculations using non-linear analog circuits. Another significant integrator based F/V converter was proposed by Djemouai et al. [138]. The ideal model of this F/V converter is shown in Fig.5-7. This circuit is found to operate well at moderately high frequencies but its performance in the gigahertz band is limited by several factors. The first drawback lies in the fact that it uses two non-overlapping pulses that must occur within half a period of the input signal requiring the minimum duration of half period of the input signal to be equal to two such pulses. These pulses are also used to control nMOS switches which normally require full swing pulses of sufficient duration for charge transfer. If it is assumed that the duty cycle of the input signal is 50%, then the minimum clock period should be four full swing pulses. This limitation restricts the use of Djemouai et al. configuration in the gigahertz range of frequencies.

Some of the problems associated with the integrator based F/V converter are addressed by Hung Tien Bui et al. [139], where a new algorithm and circuit techniques suitable for higher frequency applications has been proposed. However, these scheme has also been found to suffer from restricted input signal voltage level that is, the input signal voltage level is restricted by the difference of drain supply and the threshold voltage (V_{dd} - V_{th}) and (V_{low} -V_{th}) of the MOS transistor. This scheme finds limited applications where the signal level essentially lies within the range defined by the MOS transistors used. This architecture has been demonstrated to operate at a signal frequency of 5 GHz which is twenty times higher than the previous highest reported in [138] but silent about frequencies beyond 5 GHz. A new low power F/V converter has been proposed in this thesis which is based on non-linear analog circuits suitable for multi-gigahertz application beyond 5 GHz. The proposed architecture also addresses the input signal voltage level constraint present in [133] and described in the following section.

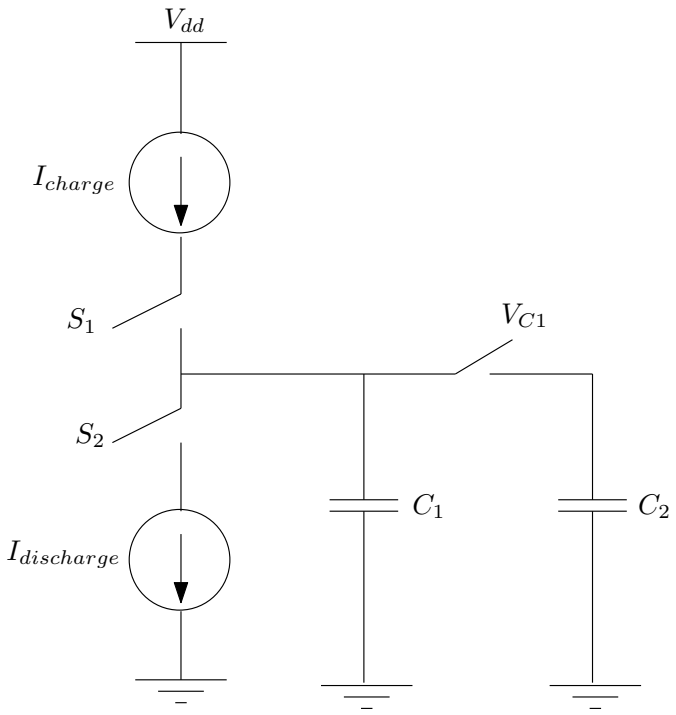


Figure 5-8: Ideal model of the FVC

5.5 Proposed Frequency-to-voltage converter

The F/V converter proposed in this thesis essentially consists of two stages as shown in Fig.5-9. The first stage consists of a high pass active filter constructed with RF op amp. This stage provides the necessary signal path for the desired input signals frequency. The second stage is constructed with precision rectifier (diode rectifier may be used provided signal voltage level > diode knee voltage), the optional third stage consists of a unity gain amplifier followed by a filter circuit to filter out the ripples associated with the rectified output. The unity gain amplifier and the precision rectifier are optional requirement where highly ripple-free d.c. voltages are required and was constructed using a custom designed op amp for RF applications as described in the following subsection. The ideal

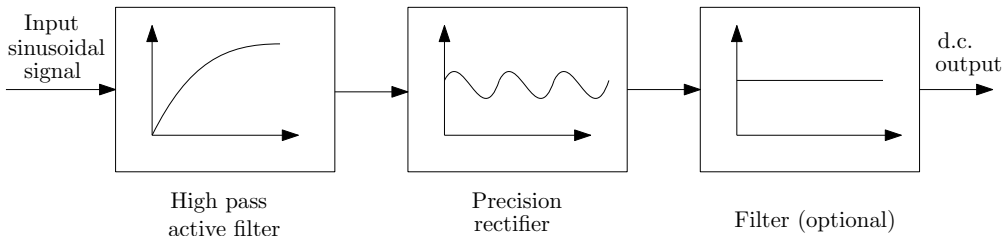


Figure 5-9: Block diagram of the proposed F/V converter

frequency response of a high pass filter is shown in Fig.5-10. It may be observed that the response below the cut-off frequency, f_c has a linear relationship of the output voltage with frequency since input signal voltage is constant. In other words, the output voltage maintains an almost linear relationship with frequency and it increases with increase in

frequency up to the cut-off frequency. This property of high pass filter can efficiently be used to design a novel F/V converter by multiplying the filter output ($V_{gain} = V_{out}/V_{in}$) by the input voltage and employing a precision rectifier next to the filter stage in order to convert the output a.c signal to d.c. The overall system will produce a d.c. voltage proportional to the input signal frequency. The design of the various blocks of the

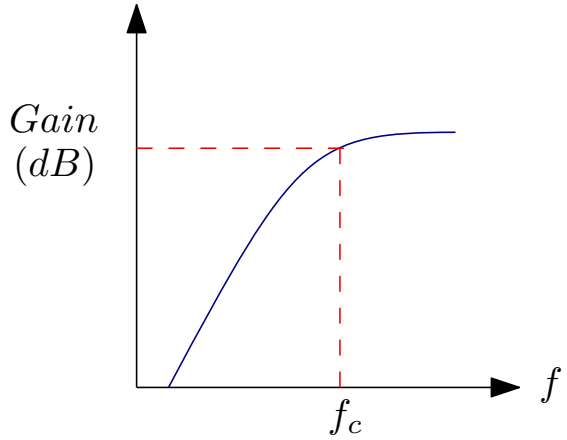


Figure 5-10: Frequency response of an ideal high pass filter

proposed F/V converter are proposed to be designed around operational amplifier and therefore an RF op amp has been designed as described in the section to follow.

5.5.1 Design of RF operational amplifier

The operational amplifier is one of the most important and at the same time versatile building blocks used in analog circuit design. The operational amplifier fits into the category of complex circuits that forms part of analog integrated circuit design building blocks. The operational-transconductance amplifiers (OTAs) with typically very high output resistance are termed as "unbuffered"operational amplifiers and the term "op amp"for such circuits has been accepted and now popularly used. The terms "unbuffered"and "buffered"are frequently used to differentiate high output resistance OTAs and low output resistance OTAs respectively.

Operational amplifiers are basically controlled sources having very high forward gain. In negative feedback configuration, the closed loop transfer function of op amp practically becomes independent of the gain of the op amp. This versatile feature of op amp has been exploited in developing many important analog circuits and systems. The primary requirement of an op amp is sufficiently high open loop gain so that negative feedback concept can be implemented around it. The CMOS op amps find wide range of applications in low power circuits and systems. Most of the CMOS op amps fail to provide sufficiently high gain and hence demand two or more gain stages. Another important term associated with op amps is "compensation", the goal of which is to maintain stability in the negative feedback configuration. Ideally, an op amp should have infinite

differential-voltage gain, infinite input resistance and zero output resistance. But in reality, an op amp only approaches these values.
Amplifiers designed to operate at RF differ from conventional low frequency circuit approaches and hence requires special considerations. Thus stability analysis becomes an important issue with noise and gain figures. The key RF amplifier parameters are gain (dB), operating frequency and bandwidth (Hz), output power (dBm), power supply requirements, input and output reflection coefficient (VSWR) and noise figure (dB).

5.5.2 Two-stage CMOS RF op amp

The architectures of CMOS op amps are similar to their BJT counterparts. The important aspects of a two-stage op amp is presented in figure 5-11. The differential transconducatnce stage provides the input of the op amp and also performs differential to single-ended conversion in many occasions. The differential input stage normally provides a good portion of the overall gain of the op amp. The second stage is typically an inverter which performs differential to single-ended conversion when the differential input stage does not perform the conversion. If the op amp is required to drive a low-resistance load, the inverter stage must be followed by a buffer stage in order to lower the output resistance so that a large signal swing is maintained. Biasing circuits are used to provide necessary biasing to the active devices used so that appropriate operating points for each of the transistors are established. The compensation circuitry is needed for stable closed loop performance of the op amp. When the gain of the op amp is large enough while in negative feedback configuration, the input port fulfills the necessary condition of a *null port* or *nullor*, which is basically a pair of terminals connected to a network where the voltage across the terminals is zero and the current flowing into or out of the terminals is also zero [105]. This null port becomes the familiar *virtual ground* when one of the op amp input is grounded.

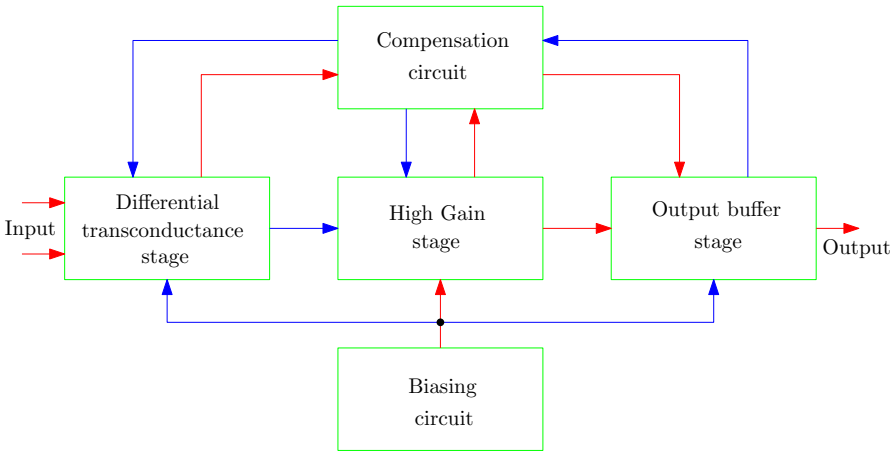


Figure 5-11: Block diagram of two-stage op-amp

5.5.2.1 Design of the proposed two stage RF op amp

The optimum trade-off among power consumption and operating speed of an op amp can be achieved when the transistors are operated in their moderate inversion region of operation [140, 141]. Amplifiers designed to operate at radio frequency differs from conventional low frequency circuit design approaches and demand special considerations [9, 142]. In RF regime stability analysis becomes an issue with noise and gain figures. The key parameters associated with an RF op amp are gain (dB), operating frequency and bandwidth (Hz), output power (dBm), power supply requirement, input and output refection coefficients (VSWR), noise figure (dB) etc. Transistors are mainly used in RF op amps as gain elements. An overview of CMOS op amp design is described in [143]. The proposed operational amplifier circuit was designed using BSIM3v3 MOSFET model made available by AWR for RF application [144]. The differential stage comprises of transistor M1 to M4 as can be seen in Fig.5-12. Transistors M1 and M2 in the differential stage are NMOS type while M2 and M4 are PMOS as usual. The differential stage forms the basic gain stage of the operational amplifier and it provides the gain to any input signal applied to either of the input terminals. Transistors M3 and M4 forms current mirror active load which performs the differential to single ended conversion of the input signal. Transistor M13 acts as a current source and with transistor M12 supply a voltage between the gate and the source of transistors M5, M7 and M9. Transistor M5 acts as a simple current source while M7 serves as a load for M6, which forms the second gain stage in addition to serving as a level shifter. The source follower is formed by transistors M10 and M11 where M10 acts as driver while M11 acts as a load. The parallel connected channels of complementary transistors M10 and M11 forms a resistance "R"provides a compensation technique for improvement of phase margin. This resistance connects the second gain stage to the output and hence acts as a feedback path. Simulation results of the proposed op amp The two stage op amp circuit of Fig.5-12 was constructed using the PMOS and NMOS devices derived above in CMOS technology and were simulated for gain, phase margin, CMRR and PSRR. The simulation results obtained for these parameters for the proposed op amp circuit of Fig.5-12 are shown below.

Frequency Response

The gain of a practical op amp decreases with increase in frequency. This occurs because of stray capacitances, finite carrier mobility in the semiconductor devices and others.

Bandwidth

Bandwidth of an op amp refers to the range of signal frequencies that can be amplified by it without distortion. Bandwidth of an ideal op amp is infinite. Most op amps

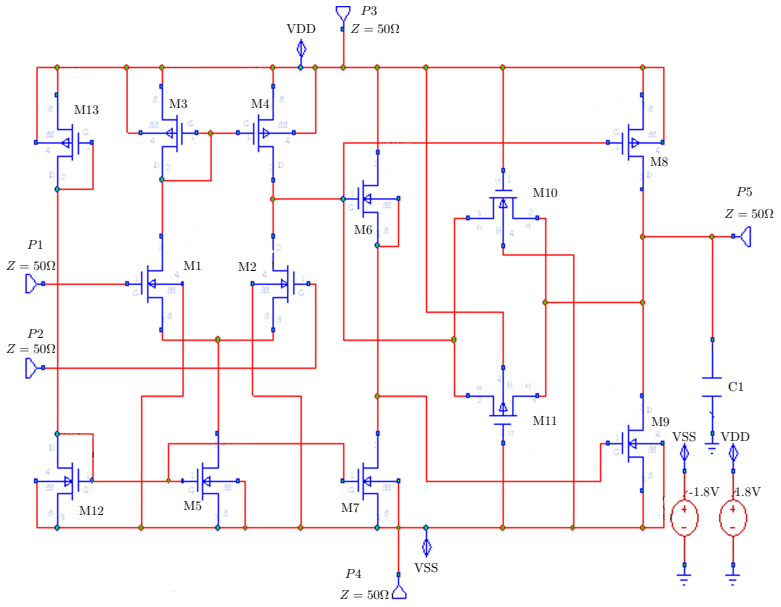


Figure 5-12: Circuit diagram of the proposed Op amp

respond to frequencies down to and including d.c.

The frequency response obtained by simulating the proposed op amp circuit is shown in Fig.5-13. It is observed that a gain of $\sim$ 36 dB and a phase margin of 22.3^0 is obtained for the CMOS op amp. It is also observed that a unity gain bandwidth (UGB) of 4.8 GHz is achieved for the above op amp which is good enough compared with the reported works.

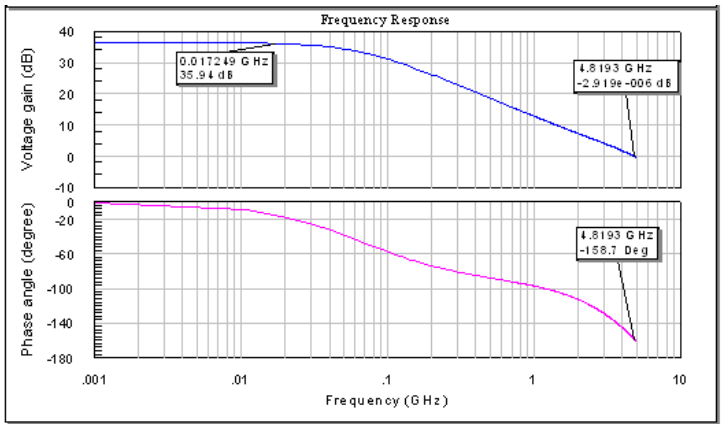


Figure 5-13: Frequency response of the proposed op amp

Common-Mode Rejection Ratio (CMRR)

It measures how much the op amp can suppress noise and is given in decibel form as

$$CMRR = \frac{A_D}{A_{CM}} \tag{5.1}$$

where A_D and A_{CM} are the differential and common mode gains respectively. A high

CMRR is therefore always desired. Typical CMRR for CMOS amplifiers are 60 dB to 80 dB.

The proposed op amp was simulated for CMRR in Microwave Office (version 9.05) and

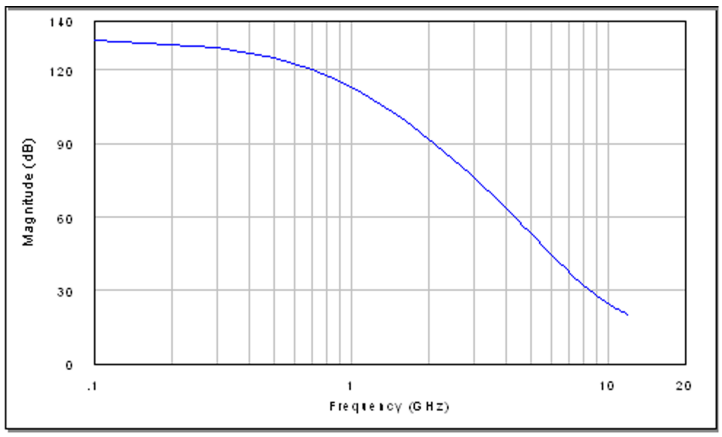


Figure 5-14: Simulation result for CMRR of the proposed op amp

the resulting plot is shown in Fig.5-14. The CMRR in dB was obtained by applying two identical voltage sources in series with the op amp inputs and employing a unity gain feedback. CMRR of 136 dB was achieved for the CMOS implementation of the proposed op amp which is reasonably good.

Power Supply Rejection Ratio (PSRR)

If a small signal is applied in series with the positive or negative power supply, a corresponding signal at the output with a given amplification (APS+ or APS-). The ratio between the differential gain (A_D) and the power supply gain (A_P) leads to two PSRR's. These are two merit factors showing the ability of the op amp to reject noisy signals coming from the power supply. A good PSRR is therefore a highly sought after feature of op amps. Unfortunately, especially at high frequencies, the PSRR achieved is quite poor. A typical value of PSRR is 60 dB at low frequencies and it decreases to 20 to 40 dB at high frequencies. PSRR in dB is expressed as

$$PSRR_{dB} = 20\log_{10}\left(\frac{A_D}{A_P}\right) \tag{5.2}$$

The power supply rejection ratio (PSRR) of the CMOS implementation of the proposed op amp was obtained by simulating the circuit with inputs shorted in unity gain configuration. The value of PSRR(+) obtained is 62 dB as shown in Fig.5-15 below.

Slew Rate

The output of an ideal op amp can change as quickly as the input voltage changes in order to faithfully reproduce the input waveform. The practical limit to the rate of change of voltage at the output of a real op amp is called slew rate. Therefore, the

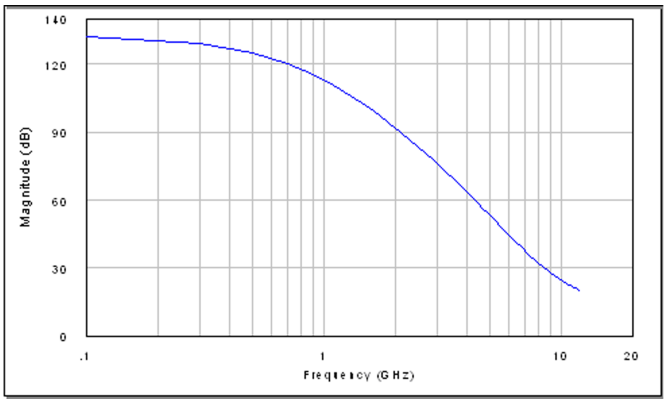


Figure 5-15: Simulation result for CMRR of the proposed op amp

slew rate of an ideal op amp is infinite. The highest sine wave frequency that can be amplified without distortion is given by

$$f_{SLR} = \frac{slewrate}{\pi V_0(\max)} \tag{5.3}$$

where $V_0(\max)$ is the maximum peak-to-peak output voltage swing.
The slew rate of the op amp is calculated from the simulated result shown in Fig.5-16 and found to be 0.45V which again good enough compared with standard op amps.

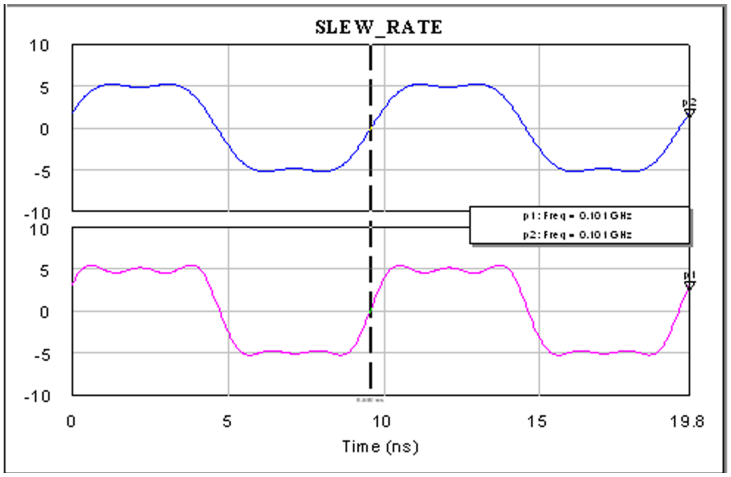


Figure 5-16: Transient response of the CMOS op amp

5.5.3 Basic High Pass First Order Active Filter

The schematic depicted in Fig.5-17 is a modified differentiator which acts a as a first order high pass active filter. The transfer function of this circuit can be derived as

$$\frac{V_{OUT}}{V_{IN}} = H_o \frac{s}{s + \omega_c} \tag{5.4}$$

Or

$$\left|\frac{V_{OUT}}{V_{IN}}\right| = |H_o| \frac{\omega}{\sqrt{\omega^2 + \omega_c^2}} \tag{5.5}$$

where, H_0 is the gain of the network given by $H_o = R_1/R_2$ and ω is the operating frequency while ω_c is the cut-off or break frequency. It can be written from equation (5.4)

$$V_{OUT} = \left(\frac{sH_o}{s + \omega_c}\right) V_{IN} \tag{5.6}$$

Replacing ω by $2\pi f$ and H_0 by R_1/R_2 from equation(5.5), we get

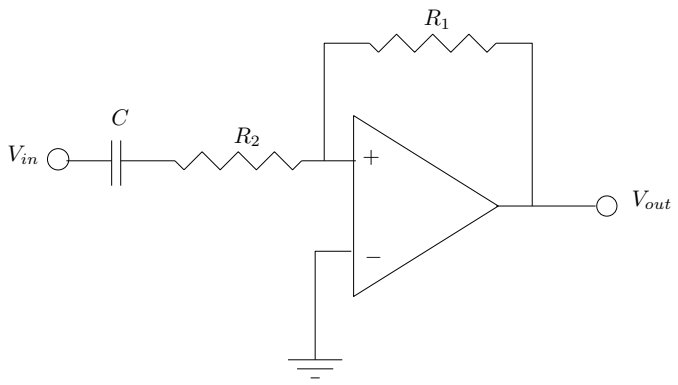


Figure 5-17: First order active high pass filter schematic

$$|V_{OUT}| = \frac{R_1}{R_2} \frac{f}{\sqrt{f^2 + f_c^2}} . V_{IN} \tag{5.7}$$

It is therefore, obvious from equation (5.7) that the output voltage of the network is frequency dependent and increases with increase in frequency until the cut-off or break frequency is reached. Beyond the cut-off frequency the capacitor acts as a short and the input signal is passed to the output. In the region prior to the cut-off frequency, the output voltage increases almost linearly and this region of operation of this network can be employed in designing FVCs with relatively larger bandwidth and good resolution. The circuit diagram of first order high pass active filter described above was constructed using the CMOS RF op amp described above and shown in Fig.5-18 and its frequency response in Fig.5-19. It can be observed from the frequency response plot that the gain (dB) rises linearly from < 0.1GHz upto ~ 3 GHz. It means that the input signal frequency exhibits a nearly linear relationship with output voltage since input signal voltage remains constant.

5.5.4 Proposed Precision Full wave Rectifier

Precise rectification is one of the most vital requirements for many applications such as instrumentation and measurements [87, 145, 146]. In most of the applications [87, 145–147] diodes are used as rectifying element. Since diodes do not operate below the knee

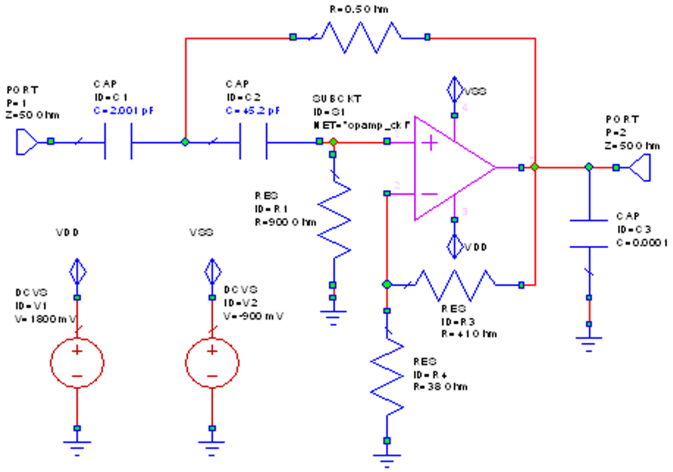


Figure 5-18: Circuit diagram of first order high pass active filter

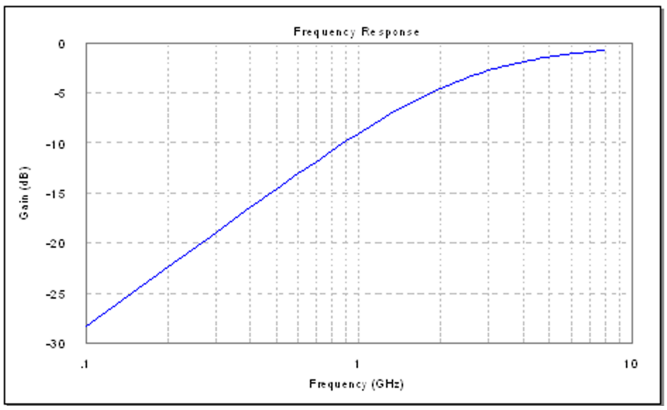


Figure 5-19: Frequency response of high pass active filter

voltage, these rectifiers have the limitation of minimum input signal voltage requirement above the knee voltage. Also, in case of high frequency signals slew rate limitation prevents fast turning on of the diodes and distortion results. It is recently reported in [145, 146] that an operational amplifier with CCII+ type current conveyor [148] can be used, due to the high output impedance of current conveyor to overcome the turn-on resistance of the diodes permitting rectification of low level signals responding to over a frequency of 100KHz. Keeping this in view, a high precision rectifier is proposed in this thesis employing an RF operational amplifier. The block diagram of the proposed precision rectifier is as shown in Fig.5-20. The input sinusoidal signal is passed through a

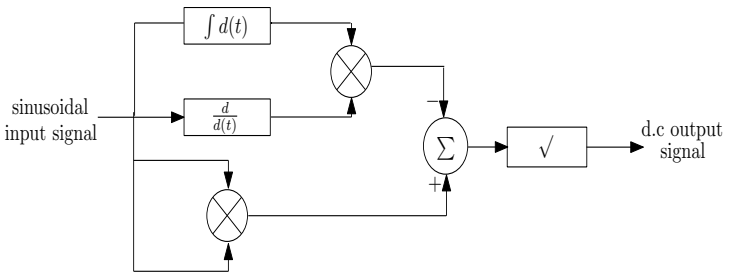


Figure 5-20: Block diagram of the proposed precision rectifier

squaring circuit while the same is also passed simultaneously through a differentiator and an integrator. Both the differentiator and the integrator circuits produce cosinusoidal signals which are multiplied to obtain the square of the cosinusoidal signal. The squares of both the sinusoidal signal and cosinusoidal signal are added together in the summing circuit. The output of the summing circuit is passed through a square root extractor and a dc voltage proportional to the amplitude of the a.c. input signal voltage is obtained at the output.

5.5.4.1 Design of Differentiator and Integrator Circuit

Differentiator

The differentiator is a circuit the output voltage of which is proportional to the time derivative of the input voltage. Fig.5-21(a) gives the circuit diagram of op amp differentiator. The voltage gain transfer function of the ideal differentiator is given by

$$\frac{V_o}{V_{in}} = -\frac{R_F}{(1/C_1 s)} = -R_F C_1 s \tag{5.8}$$

It follows from above equation that the time domain output voltage can be given by

$$\frac{V_o}{V_i} = -R_F C_1 \frac{dV_i}{dt} \tag{5.9}$$

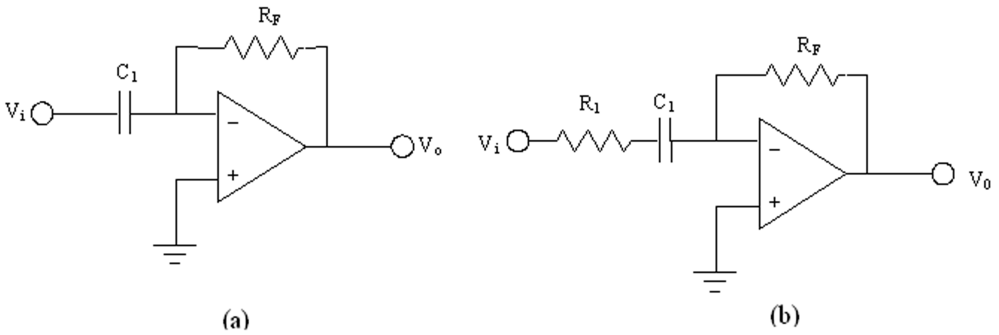


Figure 5-21: Op amp differentiator a)Ideal differentiator and b)Modified differentiator

$$\frac{V_o}{V_i} = -R_F C_1 \frac{dV_i}{dt} \tag{5.10}$$

Thus the circuit performs inverting differentiation with a gain constant $R_F C_1$ and input impedance transfer function given by

$$Z_{in} = \frac{1}{C_1 s} \tag{5.11}$$

The modified differentiator

It follows from equation (5.8) that with $s = j\omega$ the voltage gain of the circuit is $\omega R_F C_1$

and the gain may be very high for large ω. In order to limit the high frequency gain, a resistor is used in series with the capacitance as shown in Fig.5-21(b). At high frequencies C_1 becomes zero and the gain magnitude is limited by R_F/R_1 and the voltage gain transfer function is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + 1/C_1 s} = -\frac{R_F C_1 s}{1 + R_1 C_1 s} \tag{5.12}$$

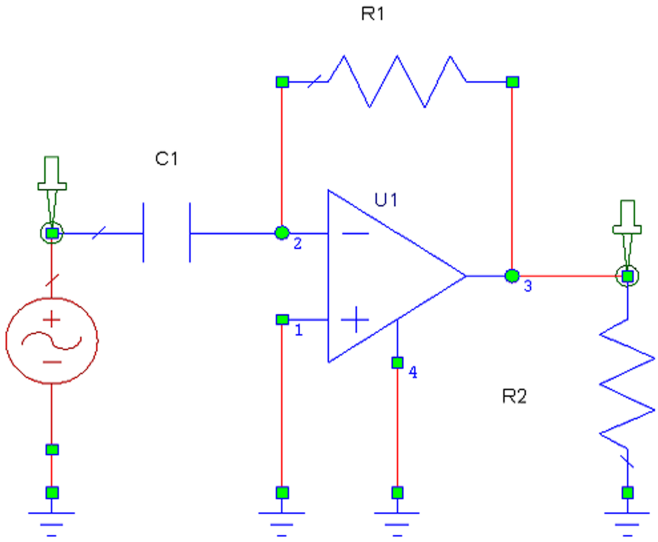


Figure 5-22: Modified op amp differentiator

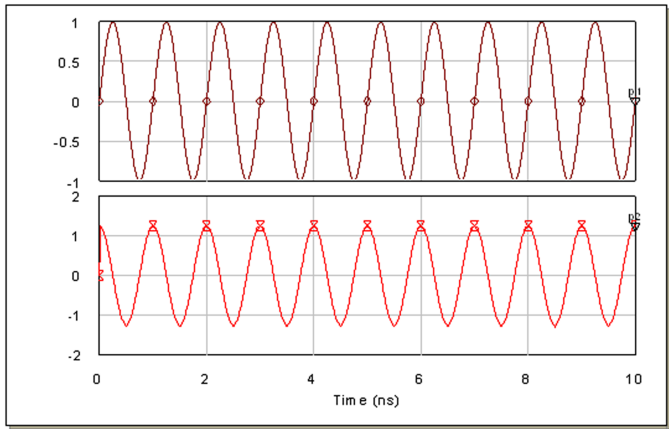


Figure 5-23: Transient response of the differential amplifier (a)Input signal and (b)Output signal

The differentiation function was achieved by employing classical op amp based architectures as shown in Fig.5-21(b) using RF op amp described above. The actual circuit diagram of the modified differentiator is depicted in Fig.5-22 while simulation result for a sinusoidal input frequency of 1 GHz is shown in Fig.5-23. It is seen in Fig.5-23

that the magnitude of the output voltage is approximately the same as the input voltage.

Integrator

Integrator is a circuit whose output voltage is proportional to the time integral of the input voltage. An integrator can be obtained by interchanging capacitor and resistor of the differentiator circuit of Fig.5-21(a)as shown in Fig.5-24(a). The voltage gain transfer

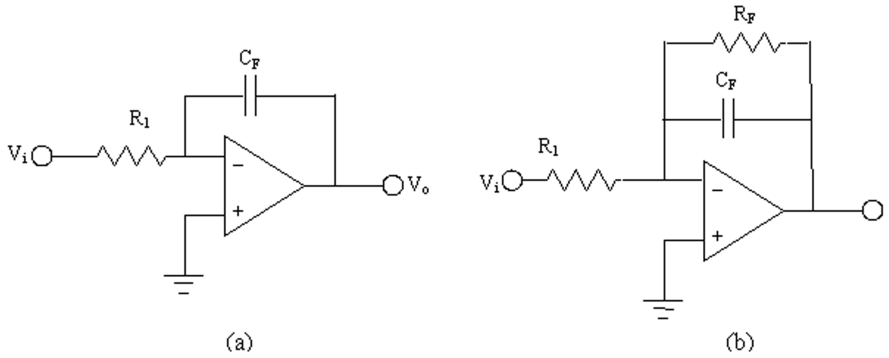


Figure 5-24: Op amp Integrator (a) Ideal Integrator and (b) Modified Integrator

function can be found by replacing R_F by complex impedance of the capacitor C_F in equation (5.8) and is given by

$$\frac{V_o}{V_i} = -\frac{\left(1/C_F s\right)}{R_1} = -\frac{1}{R_1 C_F s} \tag{5.13}$$

Since a division by s in the complex frequency domain is equivalent to time integration in time domain, it follows from equation (5.13) that the time domain output voltage is given by

$$v_o(t) = -\frac{1}{R_F C_1} \int_{-\infty}^{t} v_i(t)dt \tag{5.14}$$

Thus the circuit of Fig.5-24(a) is an inverting integrator with a gain factor $1/R_1C_F$, input resistance R_1 and output resistance 0.

Modified op amp Integrator

At d.c. or very low frequency the ideal integrator given Fig.5-24(a) loses feedback and this can cause undesirable d.c. offset voltage at the output for non-ideal op amps. In order to maintain feedback at d.c. or very low frequency, a resistor R_F is used in parallel with C_F as shown in Fig.5-24(b). The voltage gain transfer function is now given as

$$\frac{V_o}{V_i} = -\frac{R_F \,\|(1/C_F s)}{R_1} = -\frac{1}{R_1 C_F s} \times \frac{R_F C_F s}{1 + R_F C_F s} \tag{5.15}$$

This modified integrator circuit with R_F acts as integrator only for frequencies such that $\omega \succ\succ 1/R_F C_F$.

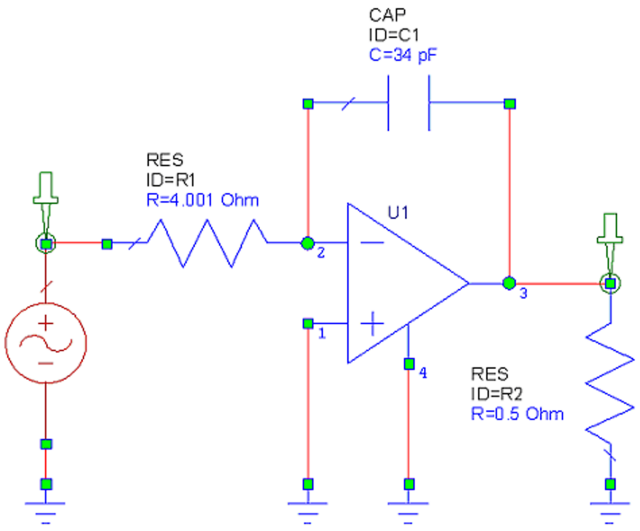


Figure 5-25: Op amp Integrator (a) Ideal Integrator and (b) Modified Integrator

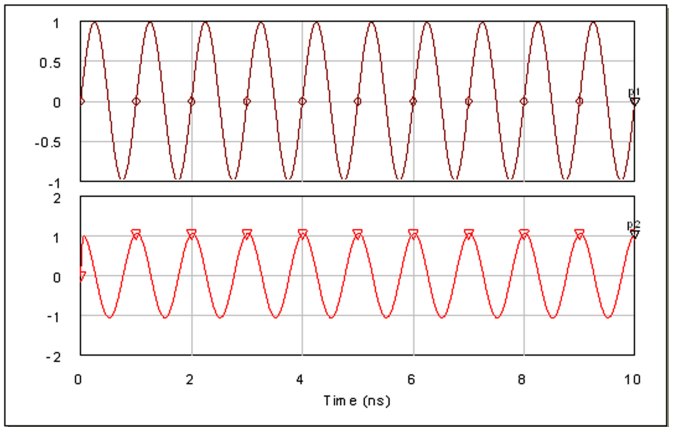


Figure 5-26: Transient response of modified integrator (a)Input signal (1GHz) and (b)Corresponding (1GHz)

The modified integrator shown in Fig.5-24(a) was designed using the same RF op amp described above and employed in the construction of the differentiator (Fig.5-25)and was simulated in Microwave Office. The simulation result for an input signal of magnitude 1 volt and frequency of 1GHz (Fig.5-26(a)) and the resulting output wave form is shown in Fig.5-26(b).

5.5.4.2 Design of Squaring Circuit

The squaring circuit used in the construction of the precision rectifier is accomplished with the help of logarithmic amplifier, summing circuit and antilogarithmic amplifier, the design descriptions of which are presented in the sections to follow. The squaring function is achieved through the use of the following logarithmic identities:

$$\log(m) + \log(n) = \log(mn) \tag{5.16}$$

and

$$anti\log\left(\log\left(mn\right)\right) = mn \tag{5.17}$$

5.5.4.3 Design of Logarithmic Amplifier

Logarithmic and Antilogarithmic amplifiers are non-linear circuits whose output voltage is proportional to the logarithm or exponent of the input voltage. Processes like multiplication, division, compression and decompression, true rms detection etc can be performed using addition and subtraction properties of logarithm using logarithmic amplifiers. There are basically two types of logarithmic amplifiers in use. They are transdiode and diode connected as shown in Fig-5.23. Majority of the logarithmic amplifiers are based on the inherent logarithmic relation between the collector current IC and the base-emitter voltage, V_{be} of the bipolar junction transistor employed. The operation of the transdiode connected logarithmic amplifier can be explained as follows: The resistance R_1 converts the input voltage into a current that flows through the collector of transistor Q_1 and thereby modulates the base-emitter voltage, V_{be} in accordance with the input voltage. The op amp forces the collector voltage to that at the non-inverting terminal that is 0 volts. Employing Ebers-Moll equation, the collector current can be

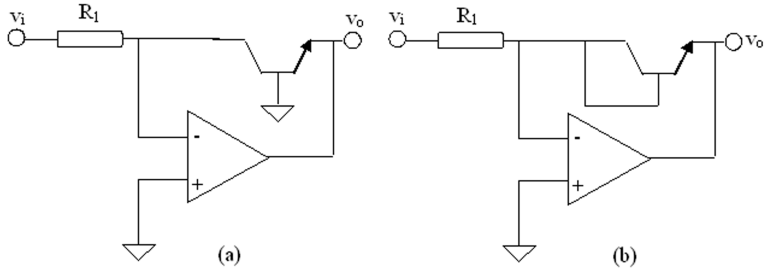


Figure 5-27: Schematic of logarithmic amplifier a)Transdiode connected and b)Diode connected

expressed as

$$\begin{aligned} I_C &= I_S\left(e^{qV_{be}/kT} - 1\right) \\ &= I_S\left(e^{V_{be}/V_T} - 1\right) \\ &\approx I_S e^{V_{be}/V_T} \end{aligned} \tag{5.18}$$

where, I_C= Collector current, I_S= Saturation current, K= Boltzman's constant (1.381x10^{-23})Joules, T= Temperature in degrees Kelvin, q= Electron charge (1.602x10^{-19} Coulombs, V_T= Thermal voltage (=KT/q). At room temperature of 300^{0}K, we get

$$\begin{aligned} I_C &= I_S\left(e^{38.6V_{be}} - 1\right) \\ &\approx I_S.e^{38.6V_{be}} \end{aligned} \tag{5.19}$$

Hence, the output voltage can be given by

$$\begin{aligned} V_{out} &= -V_{be} \\ &= -V_T \ln\left(\frac{I_C}{I_S}\right) \\ &= -2.3\, V_T \log\left(\frac{I_C}{I_S}\right) \\ &= -0.06 \log\left(\frac{I_C}{I_S}\right) \\ &= -0.06 \log\left(\frac{V_{in}}{R_{in} I_S}\right) \end{aligned} \tag{5.20}$$

The above equation yields the expected logarithmic relationship over a wide range of currents yet remaining temperature dependent because of V_T and I_S resulting in scale-factor and offset temperature dependent errors.
The basic logarithmic amplifier described above needs improvement of the following additional components/parameters in order to improve overall performance.

- provision of base-emitter junction protection
- reduction of temperature effects
- bulk resistance and op amp offset errors
- acceptance of bipolar input voltages and currents
- frequency stability

The equation for output voltage for log amp (equation 5.20) reveals that the scale factor of basic transdiode logarithmic amplifier described above is temperature dependent because of the presence of V_T and also because of the existence of a temperature dependent offset because of the presence of I_S.
Compensated Logarithmic Amplifier
A more realistic compensated logarithmic amplifier is described in Fig.5-22. The output voltage in this configuration is essentially the difference of the base voltages of the transistors Q_1 and Q_2 as given below.

$$V_{out} = \frac{R_2}{R_2 + R_3} (V_{be2} - V_{be1}) \tag{5.21}$$

The voltage difference $(V_{be2} - V_{be1})$ is proportional to the current ratio of Q_1 and Q_2 as shown in equation (5.22), assuming that both the transistors are matched.

$$(\mathrm{V_{be2}} - V_{be1}) = -\frac{kT}{qe} \ln \frac{I_{C1}}{I_{C2}} \tag{5.22}$$

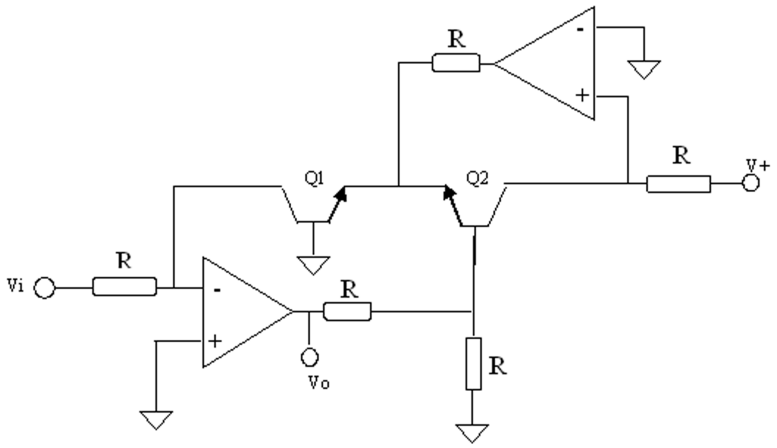


Figure 5-28: Schematic of compensated logarithmic amplifier

where, $I_{C1} = \frac{V_{in}}{R_1}$ and $I_{C2} = \frac{V_{dd}}{R_6}$. Since I_{C2} is fixed, the output voltage is proportional to the natural logarithm of V_{in} and can be given by

$$V_{out} = -\frac{kT}{q}\frac{R_2}{R_2 + R_3} \ln \frac{V_{in}}{V_{dd}}\frac{R_6}{R_1} \tag{5.23}$$

The temperature dependency can be addressed by making the resistor, R_3 suitably temperature dependent. The fact that negative voltages can not be compressed by logarithmic amplifiers has been addressed by suitably shifting the input and output signal levels with the help of level shifters (not shown in the circuit diagram).

The circuit schematic of the compensated logarithmic amplifier shown in Fig.5-28

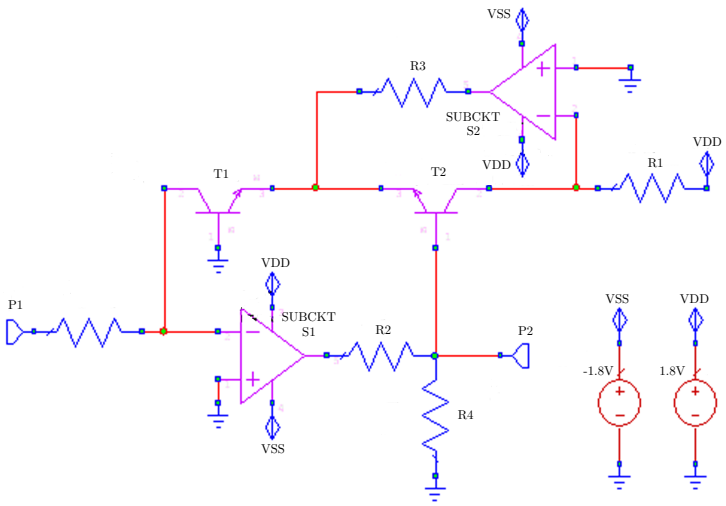


Figure 5-29: Circuit diagram of compensated logarithmic amplifier

was designed using the RF op amp described earlier and is shown in Fig.5-29 below: Simulation result of the logarithmic amplifier of Fig.5-29 is shown in Fig.5-30 and 5-31 for transfer characteristics and transient response respectively. The output voltage is plotted against the logarithm of the input voltage in Fig.5-30. It may be noted that the response is almost linear and therefore it is validated that the output is proportional to

logarithm of the input voltage. The compensated logarithmic amplifier was designed

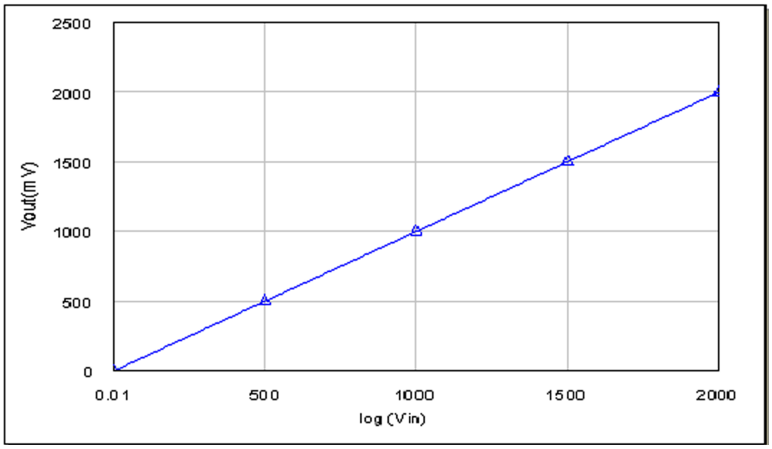


Figure 5-30: Vout vs log (Vin) plot of diode connected logarithmic amplifier

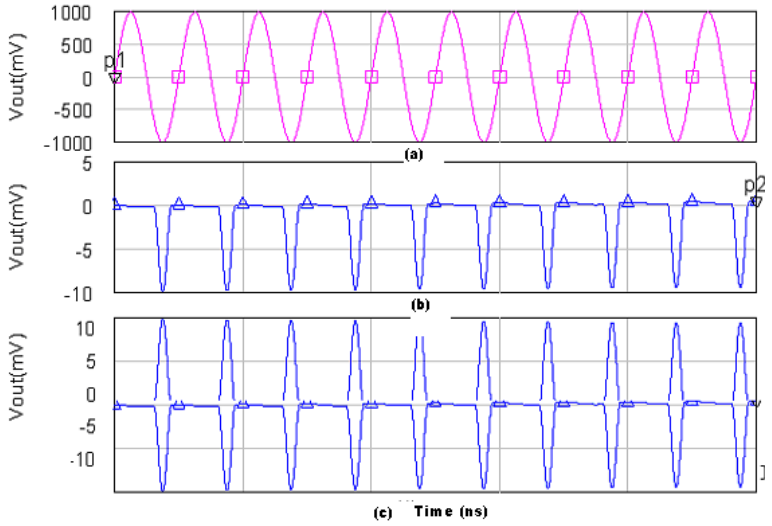


Figure 5-31: Input and output signals of the compensated logarithmic amplifier (a) Sinusoidal input signal (1GHz) (b) Output of logarithmic amplifier for positive half cycle of the input signal (c) Output of the modified logarithmic amplifier.

with the op amp designed and described earlier. The simulation result is shown in Fig.5-31. The output voltage (inverted) of the log amp was plotted against log of the input voltage which resulted in a linear response from 0.01 mV to 2000 mV.

5.5.4.4 Design of antilogarithmic amplifier

The inverse operation to logarithmic compression is exponential expansion and can be performed with following circuit (Fig.5-32). Here the feedback amplifier containing the diode connected transistor Q_1 is similar to the compensated logarithmic amplifier circuit of Fig.5-28 but in this case, it is used to provide a fixed reference current through transistor Q_1. The input voltage to be expanded is applied to the base of Q_1 through a

resistive voltage divider. It may be noted that the emitter current of Q_1 is essentially fixed and therefore the emitter junction voltage is also fixed. Therefore, the base voltage of Q_1 is increased and so is the common emitter voltage of Q_1-Q_2. In other words, the emitter junction forward voltage of Q_2 decreases. For a large enough input voltage the transistor does not function properly and the exponential relationship fails.
The anti-logarithmic amplifier as described above was designed using the same op amp used for the logarithmic amplifier and the simulation results are shown in Fig.5-33. It is observed that the circuit responses satisfactorily.

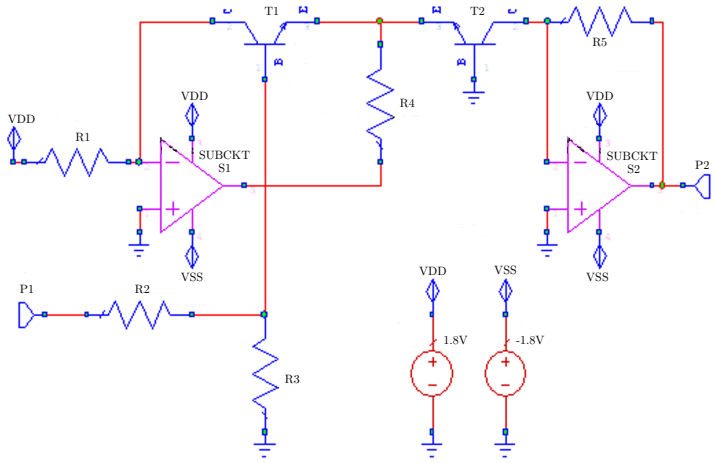


Figure 5-32: Circuit diagram of anti-logarithmic amplifier

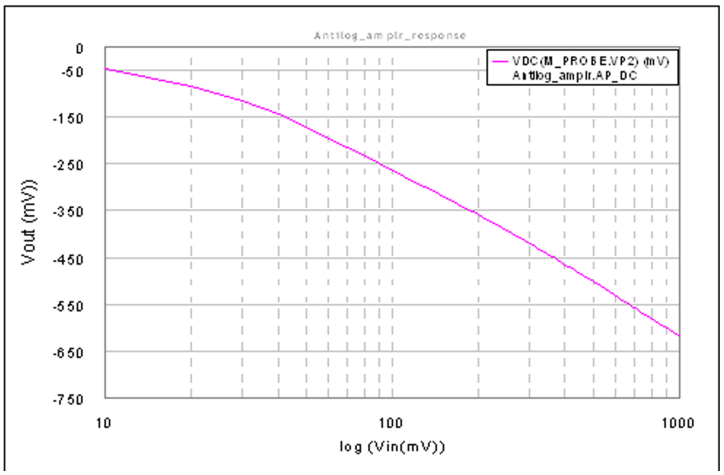


Figure 5-33: Log(Vin) vs. Vout plot of anti-log amplifier

5.5.4.5 Design of the Squaring and Square rooting Circuit

The design descriptions and simulation results of the squaring and square rooting circuits are presented below.
Squaring Circuit

The simplest analog multipliers can be constructed using logarithmic amplifiers. The computation is based on the fact that the anti-log of the sum of the logs of two numbers is the product of the numbers as shown by the following logarithmic identities given by equation (5.24) and can be illustrated with the help of Fig.5-34.

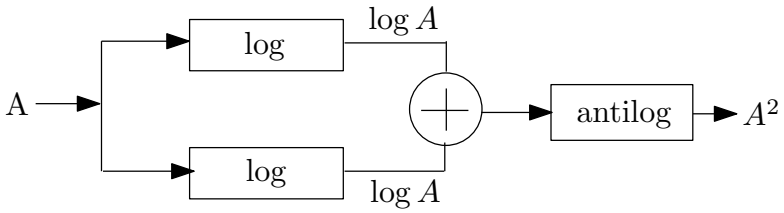


Figure 5-34: Logarithmic multiplier schematic

$$\log(A) + \log(B) = \log(AB) \text{ and} anti - \log(\log(AB)) = AB \tag{5.24}$$

Based on the concept depicted by the schematic of Fig.5-34, the squaring circuit shown in Fig.5-35 was designed using the op amp designed in this chapter. Inputs of both the logarithmic amplifiers S_3 and S_4 are shorted and the input signal was applied at port-1 and the outputs were taken from the port-2.

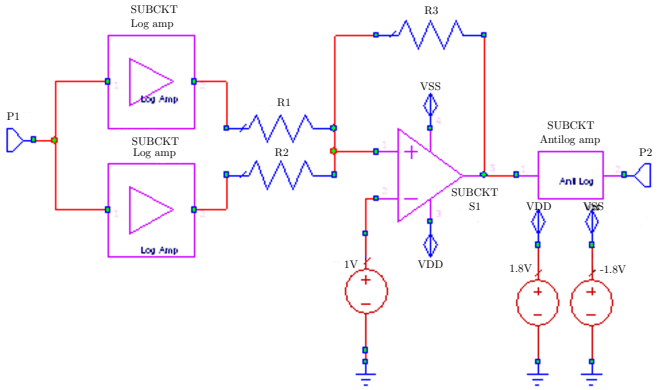


Figure 5-35: Circuit diagram of logarithmic squaring circuit

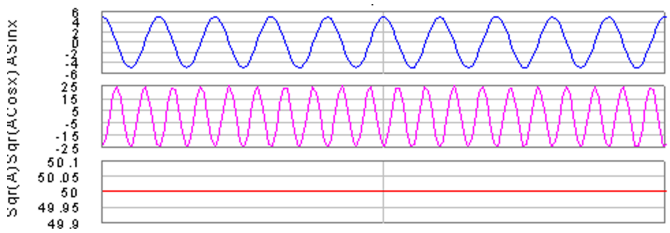


Figure 5-36: Transient response of the squaring circuit

The squaring circuit of Fig.5-35 was simulated for transient response using sinusoidal signal and the output at various stages are shown in Fig.5-36. The sinusoidal input

signal level was shifted appropriately before applying it to the input of the logarithmic amplifier and at the output before applying it to the summer in order to remove the constraint of unipolar conversion exhibited by these types of amplifiers.
In order to achieve the square rooting function, a MOSFET based square rooting circuit [149] as shown in Fig.5-37 was employed. The following equation (5.25) governs the output voltage.

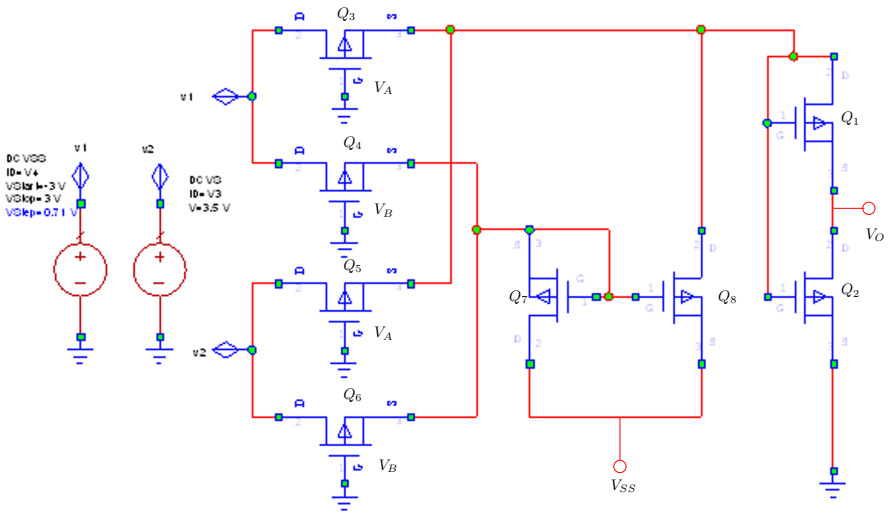


Figure 5-37: All MOSFET square rooting circuit

$$V_O = 2\left(\sqrt{{}^{1}\!/_{K_1} + {}^{1}\!/_{K_2}} - \sqrt{{}^{1}\!/_{K_2}}\right) \mathrm{X} \sqrt{K\left(V_A - V_B\right)\left(V_1 - V_2\right)} \tag{5.25}$$

where, K_1 and K_2 are the aspect ratios of the transistors Q_1 and Q_2 respectively while V_A and V_B are control voltages applied to the gate of the MOSFETs working in the triode region (Q_3 through Q_6.and V_1 and V_2 are input voltages. It is evident from equation 5.25 that the output voltage, V_O is the square root of the difference of the input voltages V_1 and V_2. By grounding either of the input voltages the output voltage can be made proportional to the square root of the input voltage.

5.6 Design of the de-spreader

The frequency-to-voltage converter (FVC) essentially produces four analog voltage levels corresponding to the four input signal frequencies. These four analog voltages are then digitized resulting in two bits in parallel for each of the analog voltages. These parallel bits are then converted to serial bits with the help of the parallel-to-serial converter in order to obtain a bit sequence. Thus, the de-spreader consists one analog-to-digital converter and a 2-bit parallel-to-serial converter. The design descriptions of these two units are presented in the following subsection.

5.6.1 Design of analog-to-digital converter

The simultaneous A/D converter has been chosen here because of the fact that the operational amplifier developed in section 5 can be used to design the comparator which forms part of the converter. This circuit is also known as parallel A/D converter and is constructed out of a series of comparators, each one comparing the input signal to a unique reference voltage as shown in Fig.5-38. The comparator outputs are connected

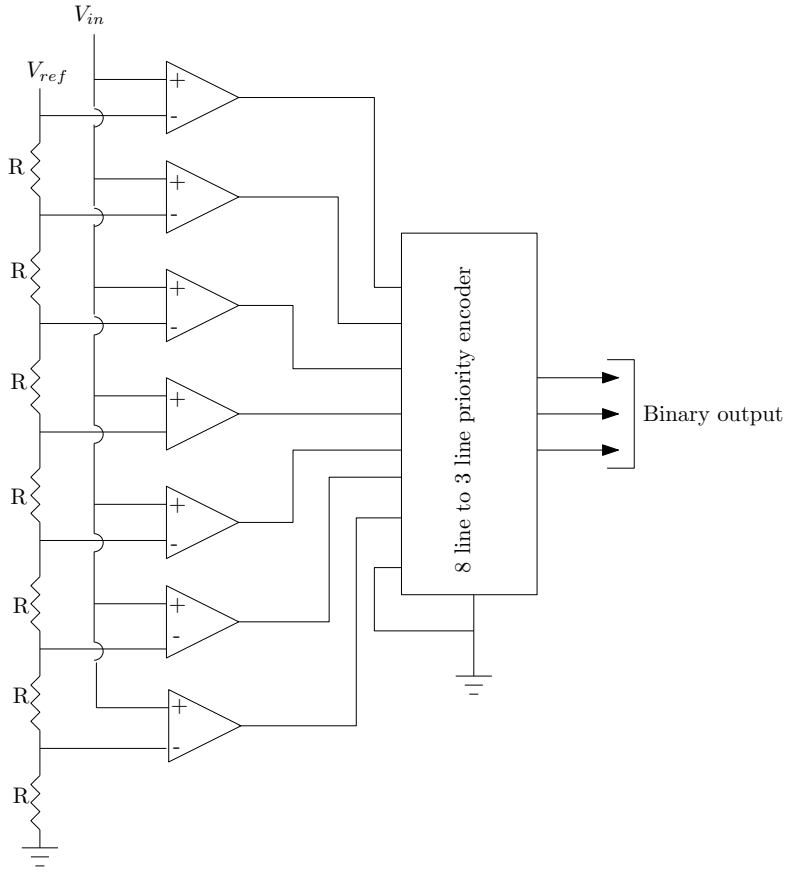


Figure 5-38: Block diagram of 3-bit flash A/D converter

to a priority encoder circuit which produces the binary output. A 3-bit flash analog-to-digital converter circuit is shown in Fig. 5-38 where V_{ref} is a stable reference voltage provided by a precision d.c. power supply (not shown in figure). As the analog input voltage exceeds the reference voltage at each of the comparators, the comparator outputs will sequentially go to a high state. A binary number is generated by the priority encoder on the basis of the highest order active input and ignore all other active inputs. The typical input/output waveforms of a flash A/D converter look as shown in Fig.5-39.

5.6.1.1 Design of high speed comparator

Comparators are the building blocks of flash ADC's since they determine the conversion speed and accuracy. The present application requires a 2-bit ADC hence we need three

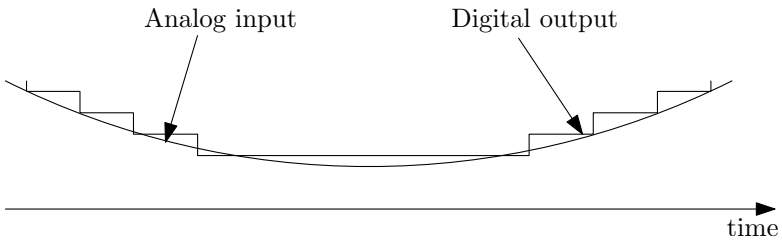


Figure 5-39: Typical output waveform of Flash ADC circuit

comparators which are designed using the operational amplifier described in section 5. The comparator generates a high when the input voltage exceeds the reference voltage and thereby acts as a one-bit ADC. The bias voltage and the transistor widths (W) are carefully chosen so that they remain in saturation. The outputs of the three comparators are in the form of thermometer code (TC) as shown by the values of C_0 , C_1, C_2 in Table 5.2, which is to be converted to 2-bit binary using a digital encoder. In the present application, we converted 2-bit digital signals into corresponding analog signals in the transmitter subsystem which leads us to convert back the analog signals into 2-bit digital signals so that corresponding digital data can be recovered in the receiver. To construct a two bit parallel A/D converter we need three comparators because $2^n - 1$ comparators are required to convert an n-bit digital signal. In the present application, only three comparators are required as only 2-bit digital output is necessary for representing four analog voltage levels. The coding network is designed using K-maps for B_1 and B_0 based on the values shown in Table 5.2. The truth table of the coding network was designed

Table 5.2: Thermometer code for a 2-bit flash AD converter

V_{in}	C_2	C_1	C_0	B_1	B_0
$V_{in} < V_{ref0}$	0	0	0	0	0
$V_{ref0} < V_{in} < V_{ref1}$	0	0	1	0	1
$V_{ref1} < V_{in} < V_{ref2}$	0	1	1	1	0
$V_{in} < V_{ref2}$	1	1	1	1	1

using the three comparator outputs C_0, C_1, C_2 and the resulting binary digits B_0 and B_1 as shown in Table 5.3. The output equations for the binary bits were found from K-maps as shown in equation (5.26) and (5.27).

$$B_0 = C_0\bar{C}_1 + C_0C_2 \tag{5.26}$$

$$B_1 = C_0C_1 \tag{5.27}$$

The resulting coding network consists of AND-OR-INVERT (AOI) as shown in Fig.5-40. The logic gates used for the coding network were designed using BSIM3v3 MOSFET model.

The flash ADC circuit of Fig.5-40 was simulated for voltage transfer characteristics

Table 5.3: Comparator outputs and the resulting binary digits

B_1	B_0	C_0	C_1	C_2
0	0	0	0	0
0	1	1	0	0
1	0	1	1	0
1	1	1	1	1

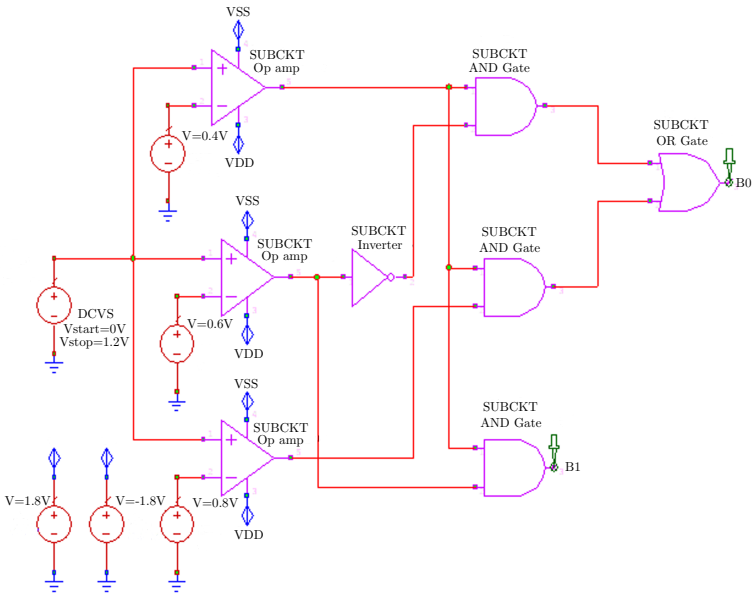


Figure 5-40: Two-bit high speed ADC circuit

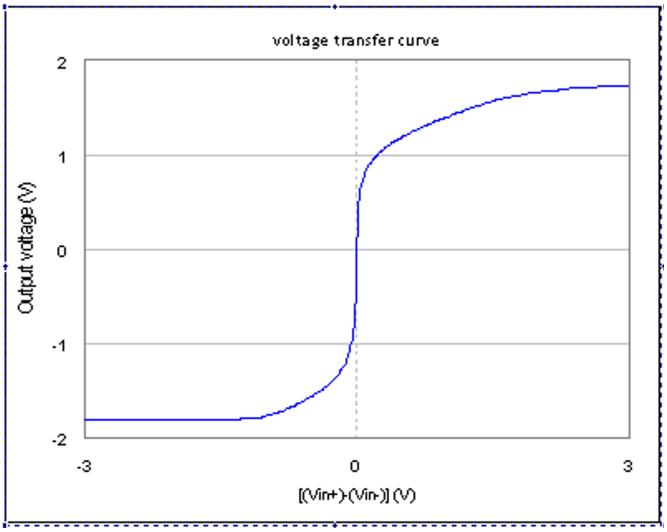


Figure 5-41: Small signal voltage transfer characteristics of comparator

and transient response using Microwave Office (9.05) and the resulting responses are shown in Fig.5-41 and 5-42 respectively. The ADC outputs for reference voltages of 0.4V, 0.6V and 0.8V obtained by simulating the ADC circuit of Fig.5-40 are shown in Fig.5-43. It is seen that digital outputs 00, 01, 10 and 11 are obtained when the analog

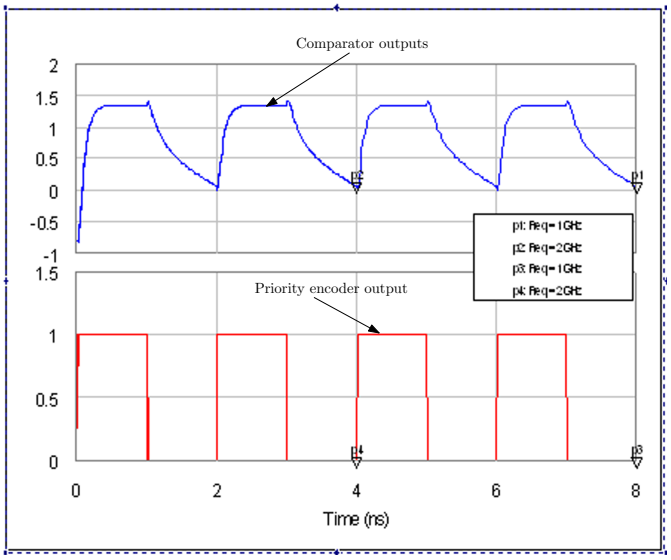


Figure 5-42: Simulation results for transient response of the comparator

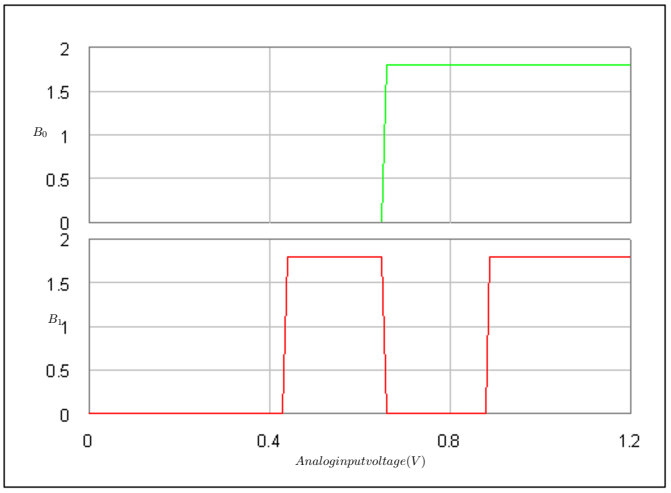


Figure 5-43: Simulation results for transient response of the comparator

input voltage is swiped over 0 to 1.2V.

5.6.1.2 Parallel-to-serial (P2S) converter

The parallel-to-serial converter employed in the present application facilitates loading of parallel input data simultaneously to all stages apart from functioning as conventional parallel-in/serial-out shift registers. The parallel-to-serial converter like parallel-in/serial-out shift registers, stores data, shifts it on a clock by clock basis and delays it by the number of stages times the clock period. In addition, the P2S converter allows us to load data in parallel into all the stages before any shifting operation takes place. The block diagram of a four stage parallel-in/serial-out shift register is shown in Fig.5-44 where D_A, D_B, D_C and D_D are the data loaded in parallel into the four stages. The internal details of the two-stage P2S converter used here is shown in Fig.5-45. As seen in

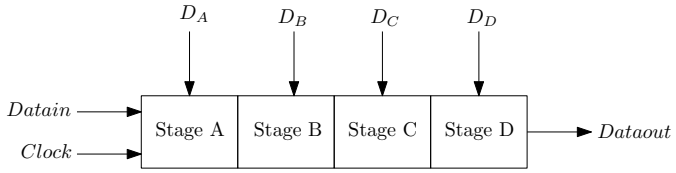


Figure 5-44: Block diagram of four stage parallel-in serial-out shift register

the figure, each stage consists of a D-flip flop for storage, and an AND-OR selector (2:1 MUX) to determine whether data will be loaded in parallel or right-shifted the stored data. These elements are replicated for each stage of the converter. We need two stages as we have to convert two parallel digital data into serial form although more number of stages can be practically feasible. The P2S converter works on two modes. When the

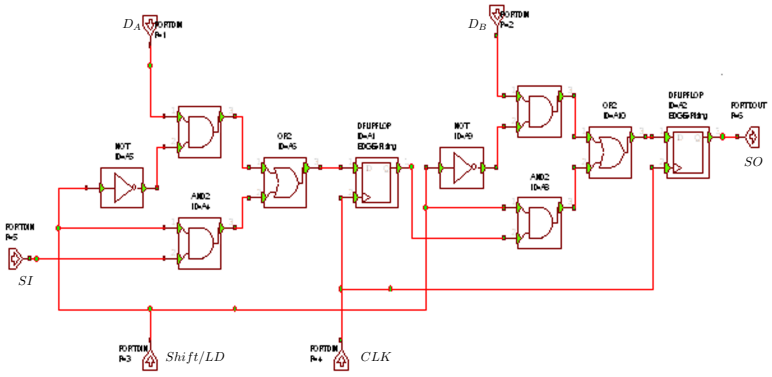


Figure 5-45: Circuit diagram of parallel-in serial-out shift register with load and shift path

SHIFT/$\overline{\text{LD}}$ is logic low, the upper NAND gates connecting parallel data D_A and D_B get enabled and passes data to the D-inputs of the D-flip flops. With the next rising edge clock, the data will be clocked from D to Q of the two flip flops and two bits of data will be loaded at the Q outputs of the flip flops simultaneously. This type of parallel load where data loads on a clock pulse is known as synchronous load. In asynchronous load, loading of data is controlled by preset and clear pins of the flip flops. In any individual device only one type of load is used, synchronous load being more common in relatively newer devices. When the SHIFT/$\overline{\text{LD}}$ is logic low, the lower AND gates of the AND-gate pair feeding the OR gates of each stage get enabled yielding a shift register configuration connecting SI to Q_A, Q_A to Q_B and Q_B to SO. The data already loaded to the Q outputs of the flip flops will be right shifted out to SO on successive pulses. The simulated wave forms shown in Fig.5-46 illustrate both parallel loading of the two bit data and serial shifting of this data. Parallel data D_AD_B is now converted to serial data at the converter output SO.

The waveforms of Fig.5-46 show both parallel loading of two bits of digital data and serial shifting of this data. As seen in the figure, a two bit data 01 is presented to the parallel inputs D_A and D_B. With SHIFT/$\overline{\text{LD}}$ = 0, parallel loading of this data is

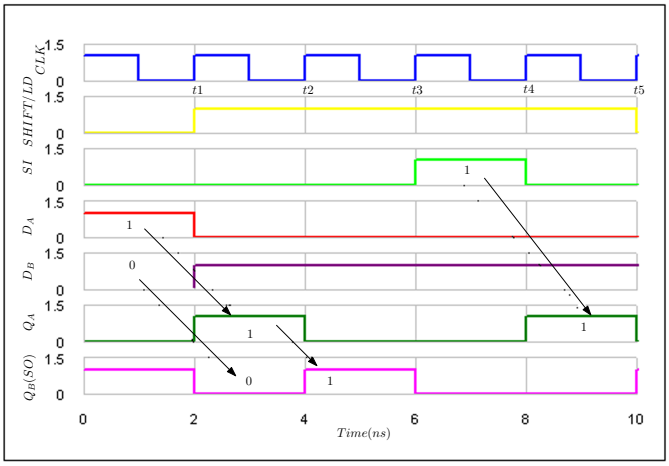


Figure 5-46: Simulation results of the P2S converter of Fig.5-45

enabled. The SHIFT/$\overline{\text{LD}}$ needs to be low for short time duration before and after the clock pulse due to setup and hold time requirements. At time t1 the data 01 at D_AD_B is clocked from D to Q of the flip flops as shown at Q_AQ_B at time t1. This explains the parallel loading of data synchronous to the clock. When SHIFT/$\overline{\text{LD}}$ goes high prior to t2, the shifting network gets enabled and the data 0 at Q_B is shifted out of SO which is same as Q_B. The data 0 at Q_A is shifted to Q_B and Q_A becomes 0 as *datain* is a 0. After t1, Q_AQ_B becomes 01. After t2, Q_AQ_B becomes 00. The left most 0 which was present in Q_A after t1 is now at Q_B and hence SO. At t3 all data from the parallel load is shifted out to SO and at t4 the data 1 present at SI shifts to Q_A. The SI and SO pins enables this shifter to be cascaded to more shift register stages and also provides facilities for serial connections to other chips.

5.6.2 Design of correlator and Integrator

The block diagram of correlator and integrator circuit is shown in Fig.5-47. The correlator correlates the demodulated signal (PN Sequence) with locally generated PN sequence (PN1, PN2,.PN16) with the help of EX-NOR gates. There are 16 states corresponding to 4-bit address word in 4-channel transceiver system, requiring 16 correlator and integrator circuits. The received (modulated) PN sequence is fed to all 16 correlators through one of the two inputs of the EX-NOR gates simultaneously and the locally generated PN sequence is fed to the other input. When a match between the received PN sequence and the locally generated PN sequence occurs, the corresponding EX-NOR gate yields the highest output as shown in Fig.5-48 and 5-49 during that PN sequence duration while the outputs of other correlators will not be high continuously. The correlator outputs are then integrated with the help of R-C integrators. The capacitors of the integrators keep on charging during the PN sequence cycle. A resetting circuit has been introduced in between correlator and integrator so that the output of the correlator

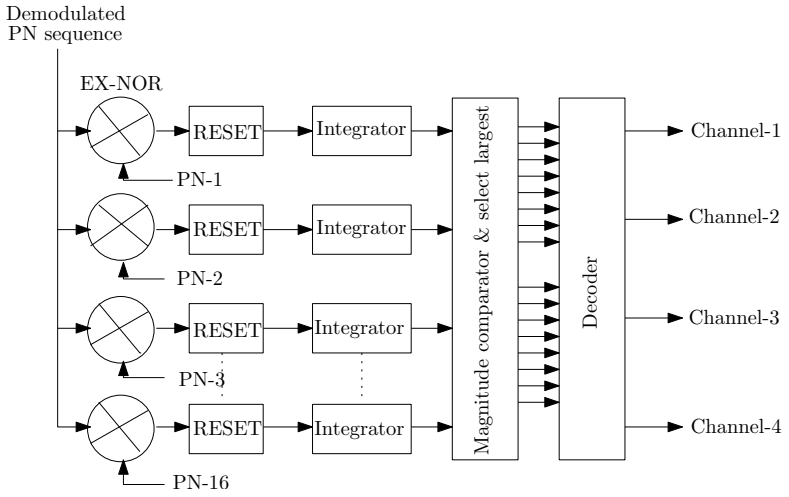


Figure 5-47: Block diagram of Correlator and Integrator

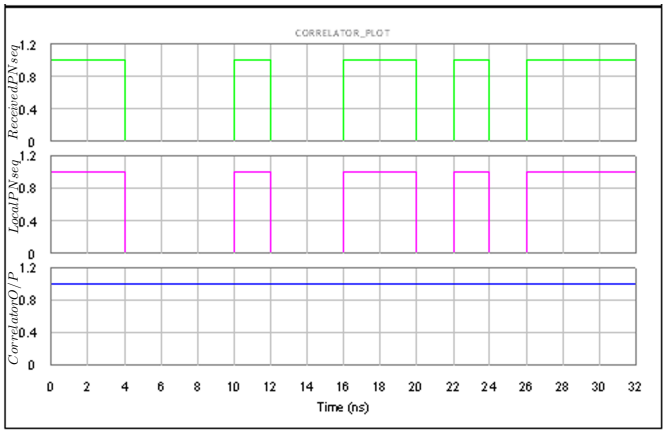


Figure 5-48: Correlator output for similar input PN sequence

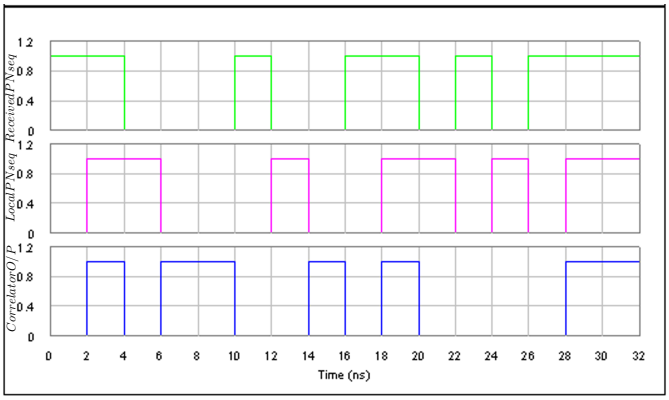


Figure 5-49: Correlator output for dissimilar input PN sequence

is reset to 0 after each integrator cycle. Each capacitor is reset to zero with the help of switching transistors triggered by a clock (Fig-5.21). It is observed during simulation of the circuit of Fig.5-50 that there exists a phase difference between the received PN sequence and the locally generated PN sequence.

This occurs due to the finite delay introduced by the different circuits through which

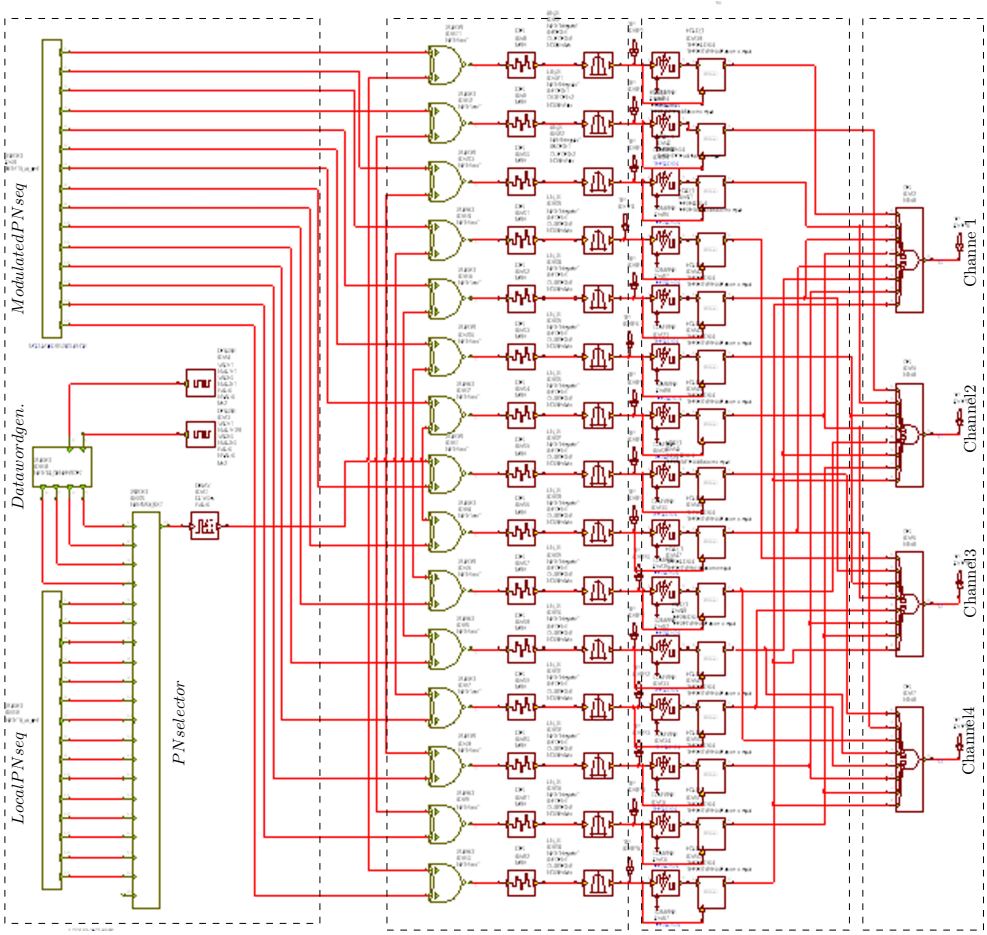


Figure 5-50: Circuit diagram of correlator, integrator and coding network

the signal propagates. This phase difference is removed by employing a delay device which introduces an appropriate delay to the locally generated PN sequence. Thus, the received PN sequence is correlated with all the 16 locally generated PN sequences and all the 16 outputs of the correlators are integrated simultaneously. The outputs of the integrators are then fed to magnitude comparator and 'select largest' circuit. The selected largest signal is fed to 16:1 decoder as shown in the Fig.5-50. The output waveforms of the integrator stage are shown in Fig.5-51 while Fig.5-52 presents the data outputs of the coding network corresponding to the four channels.
The decoder circuit was used to decode the largest output of the correlator-integrator stage into 4-bit data word. The decoder circuit receives all the 16 outputs of the magnitude comparator and select largest module simultaneously and decodes it into 4-bit data as per the truth table shown in Table 5.4. The decoding function was achieved by connecting the outputs of the magnitude comparator module to four 8-input OR gates as shown in Fig.5-50. The input and output combinations of each of the four OR gates are shown in Table 5.5.

The outputs of the four OR gates are the digital inputs of the four channels of the transmitter system. Fig.5-52 shows the outputs of the four OR gates for the time

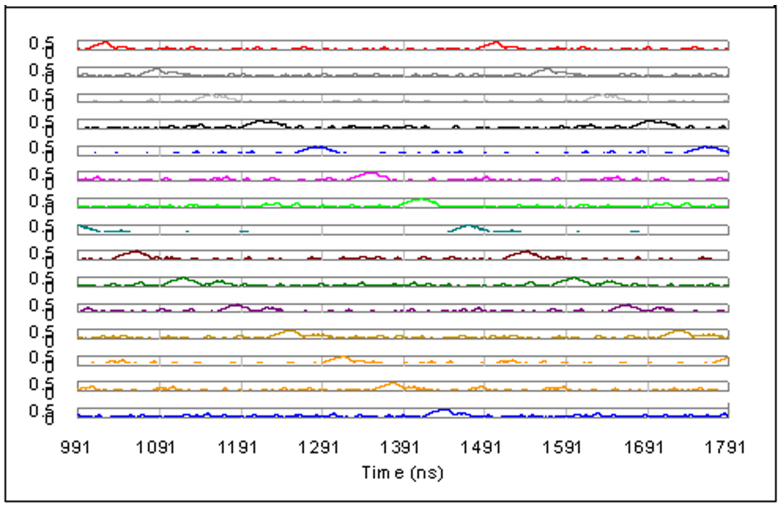


Figure 5-51: Outputs of the correlator and integrator stage

Table 5.4: Truth table of 16:4 decoder

A_0	$\dot{A}_1$	$\dot{A}_2$	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Table 5.5: Input and output combination of the 8-input OR gates

Input combination	OR gate no.	Output
$A_1A_3A_5A_7A_9A_{11}A_{13}A_{15}$	OR gate-1	Channel-1
$A_2A_3A_6A_7A_{10}A_{11}A_{14}A_{15}$	OR gate-2	Channel-2
$A_4A_5A_6A_7A_{12}A_{13}A_{14}A_{15}$	OR gate-3	Channel-3
$A_8A_9A_{10}A_{11}A_{12}A_{13}A_{14}A_{15}$	OR gate-4	Channel-4

duration 1–31ns which corresponds to the transmitted data by the four channels during that time duration.

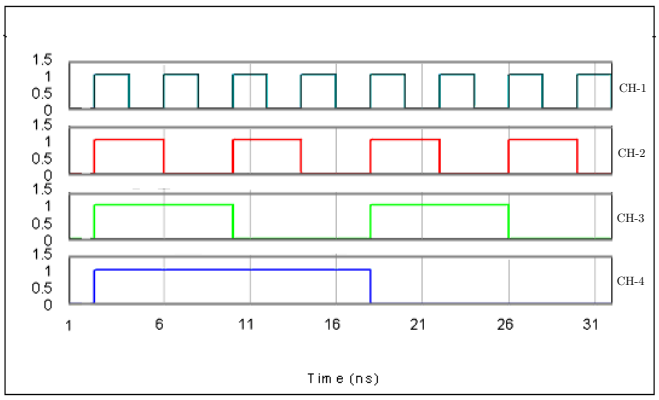


Figure 5-52: Output of the coding network for the time duration (1–31) ns

Integration of the receiver subsystems is described in chapter 6 where the simulation results of the overall receiver system performance as well as noise performance are also discussed.

Chapter 6

System Integration and Performance Analysis

6.1 Introduction

The overall transmitter system design was accomplished in chapter 4 while the receiver system design is described in chapter 5. Chapters 3 and 4 separately conceptualize the analog, digital and mixed signal subsystems proposed for the transmitter and receiver respectively. These chapters also serve to integrate the analog and digital subsystems to verify if the required system specifications are met. This chapter integrates both the transmitter and receiver designed and simulated in chapter 4 and 5 respectively. Performance analysis of the overall transceiver is also presented in this chapter.

6.2 Overview of the transceiver setup

The overview of the transceiver is depicted in Fig.6-1. At the transmitter side the data is coded with the spreading sequence which is then transmitted after further processing as described in chapter 4. In the receiver, the received signal is decoded by despreading the received sequence (as described in chapter 5).

6.3 FHSS/FSK based transceiver analysis

Transceiver analysis depends on the type of modulation scheme adopted. In this thesis, FSK modulation was employed which is described in section 2. A 15 chip per data bit

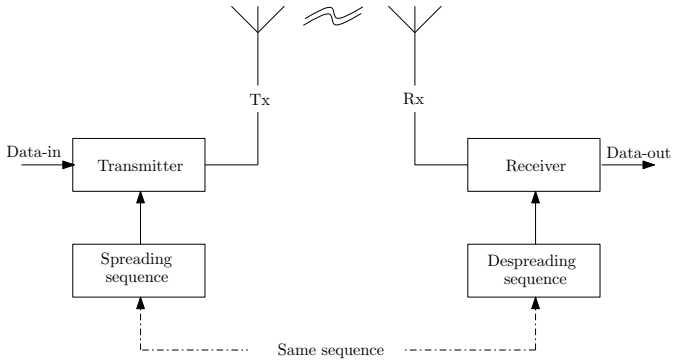


Figure 6-1: Overview of transceiver system

PN sequence was used which is described in chapter 4.
The functional analysis of the proposed transceiver can be done based on the functional schematic representation of the system as depicted in Fig.6-2 where, FU means Functional Unit.

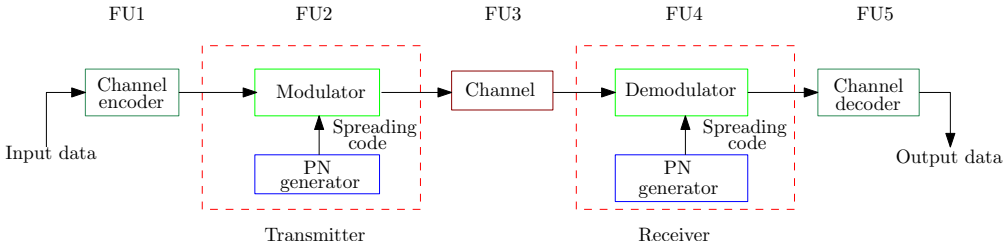


Figure 6-2: Functional analysis of the FHSS transceiver

6.4 Simulation Results of the Integrated System

Integration of the transceiver system is achieved as depicted in Fig.6-3 which may be summarized as follows:

Transmitter:

Inputs:

- digital data signal
- PN sequence
- external clock signal (required for digital subsystems)
- analog voltage source

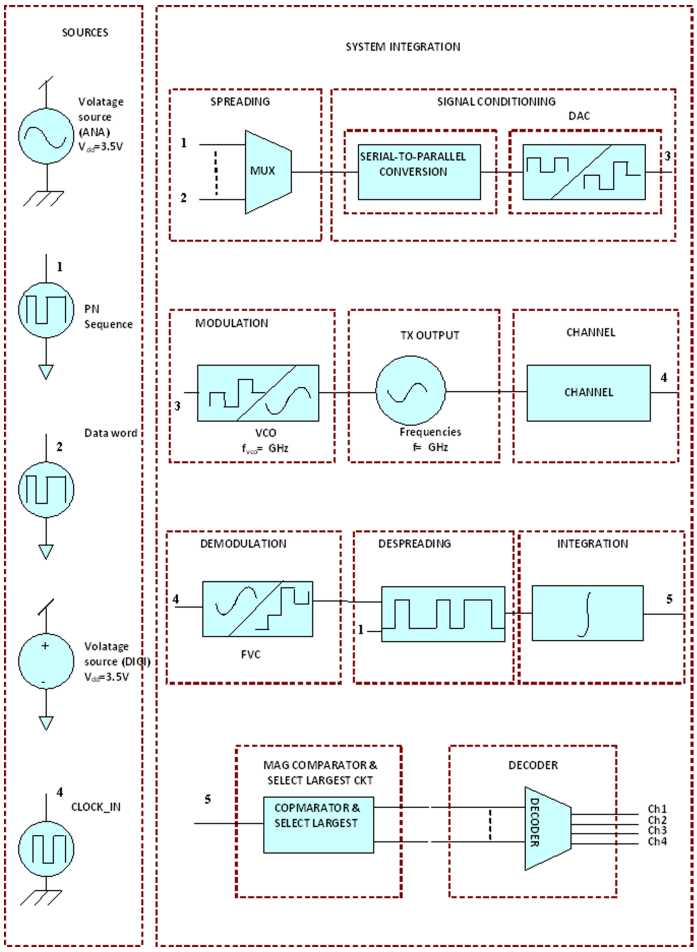


Figure 6-3: Test signals for simulation of the proposed transceiver

- digital voltage source

Outputs:

- 50Ω antenna (to be connected to the power amplifier output, not form part of this thesis)

Receiver:

Inputs

- PN sequence
- 50Ω antenna connected to LNA input (not part of this work)
- Synchronization clock signal (same as data rate)
- analog voltage source (used for analog subsystems)

- digital voltage source used for digital subsystems
- external clock signal (required for digital subsystems)

Outputs

- received data signal

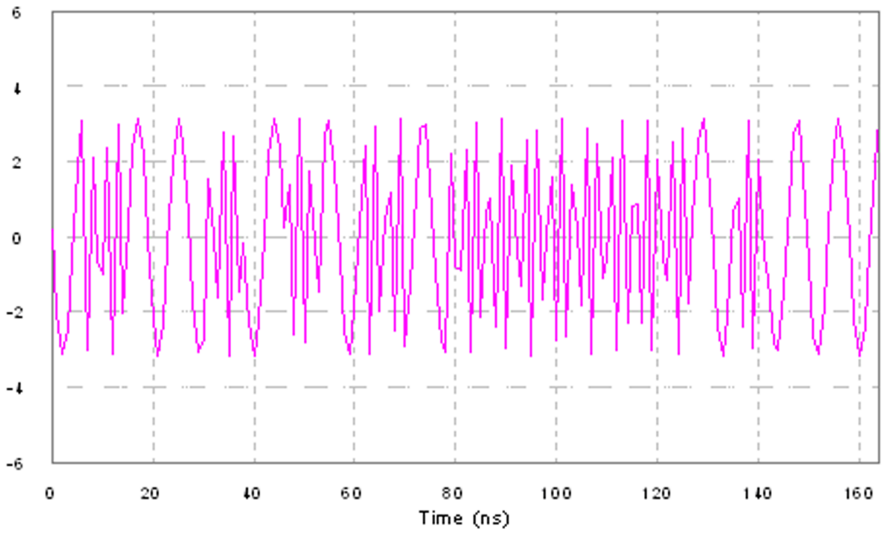


Figure 6-4: Time domain output of the transmitter

The time domain output of the transmitter is shown in Fig.6-4. It may be noticed here that altogether four different frequencies are generated by the VCO based on the analog input voltage for onward amplification by power amplifier prior to transmission by transmitting antenna.

6.5 Performance analysis

The performance of a communication system is typically measured by BER versus SNR. SNR estimation is thus an essential function for analyzing the performance of any communication system. The following sections describe the performance analysis methodology adopted for the proposed communication system.

6.5.1 Noise in communication systems

In communication systems information transmission is accomplished through communication medium. The information is processed through the transmitter circuitry and finally radiated to the atmosphere with the help of antenna. The antenna acts as a

source of information since it radiates the information in the form of electromagnetic (EM) wave. In wireless communication, these waves propagate through the atmosphere and reach the receiving antenna. The receiving antenna picks up the radiated wave and converts it into voltage form which is processed in the receiver circuit blocks and the transmitted information is recovered.

As the signal propagates through the atmosphere, it is corrupted or contaminated by various other signals which vary with time in unpredictable manner. This unpredictable signal which is a random process is called 'noise'. In digital communication systems, the major source of noise is the analogue channel. The performance of a receiver depends on how well it recovers the desired information from the noisy signal.

The presence of noise in communication channels tends to superimpose on the signal and limits the receiver's ability to correctly recover the intended information which subsequently adversely affects the rate of information transmission. Noise in communication systems arises out of a variety of man-made and natural sources. Most of the noises can either be eliminated or its undesirable effects can be reduced by good engineering design except the thermal or Johnson noise which is caused by [150,151] thermal motion of electrons in components like resistors, wires, semiconductor devices etc.

Thermal noise can be described as a zero-mean Gaussian random process [152] where a Gaussian process $n(t)$ is a random function whose value n at any time t is characterized by the Gaussian probability density function

$$p(n) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{n}{\sigma}\right)^2\right] \tag{6.1}$$

where, σ^2 is the variance of n.

It is common to represent a random signal as the sum of Gaussian noise random variable and a d.c. signal as follows:

$$z = a + n \tag{6.2}$$

where, z is the random signal, a is the d.c. component and n is the Gaussian noise random variable. The probability distribution function given in equation(6.1) now can be expressed as

$$p(z) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{z-a}{\sigma}\right)^2\right] \tag{6.3}$$

Gaussian distribution is very often used as system noise model because of the existence of a theorem known as central limit theorem [153], which states that under general conditions, the probability distribution of the sum of j statistically independent random variables approach the Gaussian distribution as $j \to \alpha$, irrespective of the type of individual distribution functions. Therefore, even if the individual noise mechanisms might have other than the Gaussian distributions, the aggregate of many such mechanisms will tend toward the Gaussian distribution.

The primary spectral characteristic of thermal noise lies in the fact that its power spectral density is the same for all frequencies in most communication systems. Therefore,

it is assumed for all simple thermal noise models that its power spectral density is flat for all frequencies as given by

$$G_n(f) = \frac{N_o}{2}\text{watts/hetz} \tag{6.4}$$

where, the factor 2 indicates the two-sided power spectral density of $G_n(f)$. Noise with such uniform spectral density is referred to as 'white noise'.
The autocorrelation function of white noise is given by

$$\begin{aligned} R_n(\tau) &= \Im^{-}\{G_n(f)\} \\ &= \frac{N_o}{2}\partial(\tau) \end{aligned} \tag{6.5}$$

Equation (6.5) reveals that the autocorrelation of white noise is a delta function with weight $N_o/2$ occurring at $\tau = 0$. The value of $R_n(\tau) = 0 \text{for} \tau \neq 0$ and therefore, any two samples of white noise, no matter how close together in time, are uncorrelated. It is indicated by equation (6.5) that any two different samples of white noise are uncorrelated. Since thermal noise is a Gaussian process and the samples are uncorrelated, it can be concluded that the noise samples are also independent [154]. Therefore, the effect of noise in the detection process of a channel with additive white Gaussian noise (AWGN) is that the noise affects each individual transmitted symbol independently. Due to the presence of thermal noise in all communication systems, the thermal noise characteristics additive, white and Gaussian are commonly used to model noise in communication systems. Also zero-mean Gaussian noise is completely characterized by its variance and hence it is simple to use in the detection of signals and optimum receiver design.

6.5.2 Noise Analysis of the proposed FSK based FHSS System

Noise signal is always associated with communication channels and therefore, information always reaches the receiver with noise. At the input of the receiver, the received signal can be given by

$$r(t) = s(t) + n(t) \tag{6.6}$$

where, $r(t)$ is the received signal, $s(t)$ is the transmitted or desired signal and $n(t)$ is the noise signal. In order to perform the noise analysis in the present context, we consider the presence of additive white Gaussian noise (AWGN) which is prominent in FSK system of communication. For m^{th} symbol, the symbol error rate is given as

$$P_s(m) = \sum_{\substack{i=1 \\ i \neq m}}^{M} P(S_m(t), S_i(t)) \tag{6.7}$$

where, $P\left(S_m\left(t\right), S_i\left(t\right)\right)$ is the probability of the receiver mistaking $S_i\left(t\right)$ for $S_m\left(t\right)$ and it is given as

$$P\left(S_m\left(t\right), S_i\left(t\right)\right) = \int_{d_{mi}/2}^{\alpha} \frac{1}{\sqrt{\pi N}} \exp\left(-\frac{v^2}{N}\right) dv \tag{6.8}$$

where d_{mi} is the Euclidean distance between $S_i\left(t\right)$ and $S_m\left(t\right)$ given by $\|S_m\left(t\right) - S_i\left(t\right)\|$. Considering complementary function, equation (6.2) can be written as

$$P\left(S_m\left(t\right), S_i\left(t\right)\right) = \frac{1}{2} erfc\left(\frac{d_{mi}}{2\sqrt{N}}\right) \tag{6.9}$$

From equation (6.7) and (6.9), we can write

$$P_s\left(m\right) = \frac{1}{2} \sum_{\substack{i=1 \\ i \neq m}}^{M} erfc\left(\frac{d_{mi}}{2\sqrt{N}}\right) \tag{6.10}$$

The probability of symbol error of CFSK signaling is given as

$$P_s = \sum_{m=1}^{M} p_m P_s\left(m\right) \tag{6.11}$$

where, p_m is the probability of transmitting m^{th} symbol. Considering $p_1 = p_2 = ... = p_m = ... = \frac{1}{2^k}$, we can rewrite equation (6.11) as

$$P_s = \frac{1}{2^{k+1}} \sum_{m=1}^{M} \sum_{\substack{i=1 \\ i \neq m}}^{M} erfc\left(\frac{d_{mi}}{2\sqrt{N}}\right) \tag{6.12}$$

6.6 Noise analysis setup for the proposed transceiver

The block diagram shown in Fig.6-4 shows the noise analysis setup for 4-FSK/FH spread spectrum system employed for BER measurement. As seen in the figure, the setup consists of the data generator employed in the transmitter, comparator and signal generator. The data generator generates the signals for different channels and the signals are modulated with QFSK transmitter. The QFSK signals are mixed with AWGN source and fed to the QFSK receiver. The QFSK receiver demodulates and decodes back the signal with noise. The output of the receiver is the PN sequence that was transmitted. Both the signals are compared with the help of EX-OR gate. The received signal thus obtained is the delayed version the PN sequence transmitted which can be overcome by introducing the same amount of delay to the EX-OR gate input through a clock and an AND gate. If a HIGH output from the EX-OR gate is obtained then we get an error bit

and if we get a LOW output, the bit is the correct one. By counting the total number of HIGH bits at the output of EX-OR gate, total error bit is determined. Bit Error Rate (BER) is estimated by dividing the total number of error bits by total number of bits transmitted.

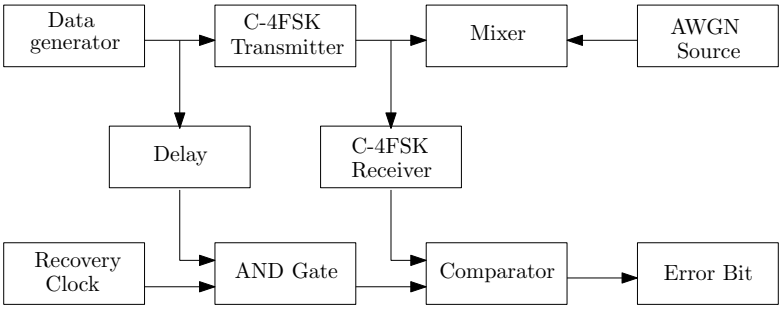


Figure 6-5: Block diagram of noise analysis setup.

6.6.1 Measurement of BER

Bit error test is a test performed in digital communication circuits that uses predetermined bit patterns comprising a sequence of logical ones and zeros. Using the BER simulation setup shown in Fig.6-5, we have measured the BER performance of the designed MFSK based FHSS system. The measured BER performance of the receiver under AWGN is plotted in Fig.6-6. Fig.6-7 shows BER performance of the 4-FSK

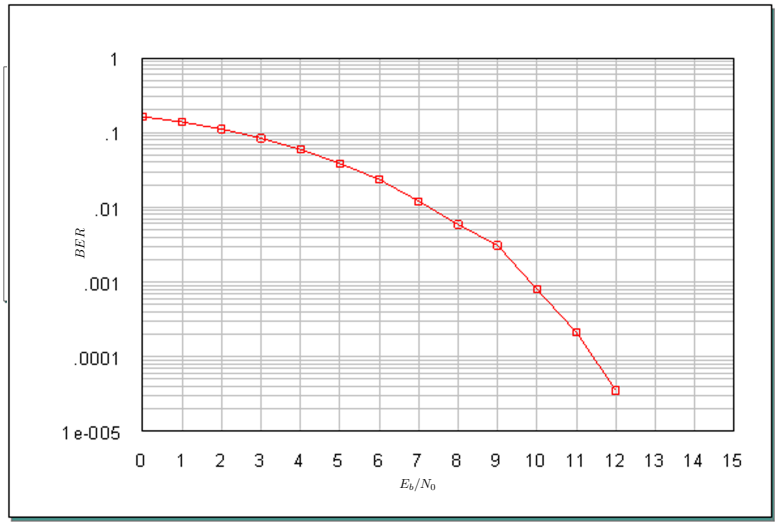


Figure 6-6: BER performance of the proposed transceiver

FHSS system with different hop sizes of f_m = 50 MHz, 100 MHz, 300 MHz, and 500 MHz. It is observed in the figure that for $f_m \approx$ 50 MHz, BER performance is worst while for f_m = 500 MHz, BER performance is best among all the hop sizes, that were considered for simulation. BER performance of the circuit is thus degraded as f_m reduces. For better BER performance we can consider higher hop size at the cost of higher

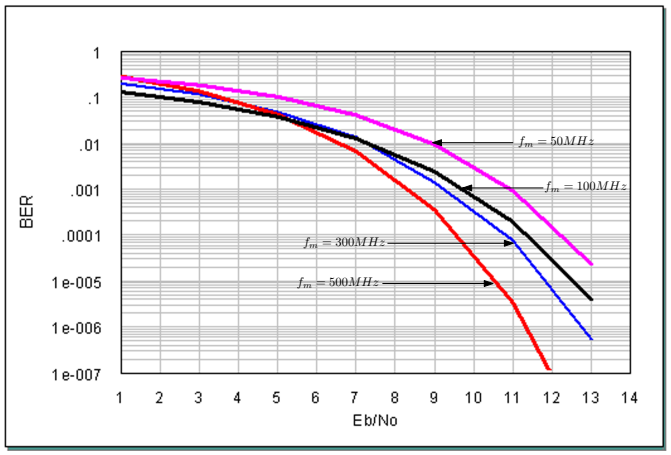


Figure 6-7: BER performance of the proposed transceiver for different hop sizes

bandwidth requirement. Actually, the bandwidth is formulated in terms of frequency hope size for K number of channels as:

$$Bandwidth = \left(2^K - 1\right) f_m \tag{6.13}$$

In case of f_m = 50 MHz, 100 MHz, 300 MHz, and 500 MHz, the bandwidth required for four channel FSK/ FHSS system obtained by using the equation (6.13) are 150 MHz, 300 MHz, 900 MHz, and 1500 MHz respectively. As f_m increases, the bandwidth requirement increases.

6.6.2 Performance analysis using eye diagram

The eye diagram is a methodology used to represent and analyze the quality of high speed digital signals. The eye diagram is constructed from a digital waveform by folding the parts of the waveform corresponding to each individual bit into a single graph with signal amplitude on the vertical axis and time on horizontal axis. By repeating this construction over many samples, the resultant graph will represent the average statistics of the signal and will resemble an eye.
Several system performances can be derived by analyzing an eye diagram [155]. Whether the signals are too long, too short, poorly synchronized with system clock, too low, too high, too noisy, too slow to change, too much undershoot or overshoot, can be observed from the eye diagram. An open eye pattern corresponds to minimal signal distortion while distortion of the signal waveform due to inter-symbol interference [156] and noise appears as closure of the eye pattern. The performances that the eye diagram mainly defines can be summarized as follows:

- *Eye opening (peak-to-peak height)*: measure of the additive noise in the signal
- *Eye overshoot/ undershoot*: measure of the peak distortion

- *Eye width*: measure of timing synchronization and jitter effects.

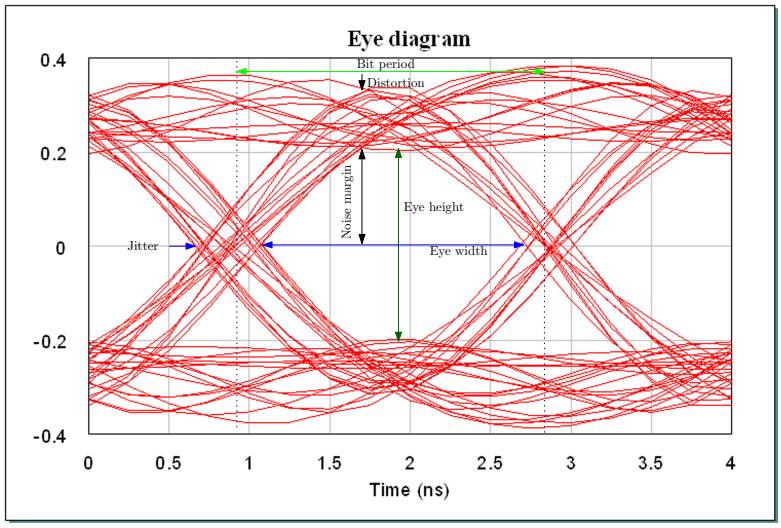


Figure 6-8: Eye diagram of FHSS receiver at 10dB SNR

Fig.6-8 shows the eye diagram under the AWGN condition for the proposed FHSS system based on FVC. Using this simulated eye diagram shown in Fig.6-8, we have estimated the noise margin, distortion and time variation at zero crossing which is a measure of jitter from the eye pattern. It is observed that with increase in SNR, distortion due to ISI decreases and noise margin increases. From the eye diagram we have also computed the noise margin and distortion as 0.21 volts and 0.12 volts for a signal-to-noise ratio(SNR) of 11 dB and a jitter of 0.42ns.

6.6.3 Adjacent channel interference

The effects of adjacent channel interference were simulated employing a simple model in which other users occupy adjacent channels to the left and right of desired channels. Since neighboring channels are the dominant interferes,a scenario with up to six users (four desired slots and two adjacent slots)were simulated. Because of the absence of explicit transmit shaping filter in the system, spectrum leakage from the neighboring channels slightly degrades performance. With two other adjacent channels, the simulated SNR degradation is about 0.63 dB which is minimal, probably due to orthogonality of the FSK tones (Fig.6-9).

6.6.4 Transmitter power

The time domain simulation result of Fig.6-4 shows that the peak voltage is approximately 5 volts. For a short time duration, if we consider the signal to be sinusoidal,

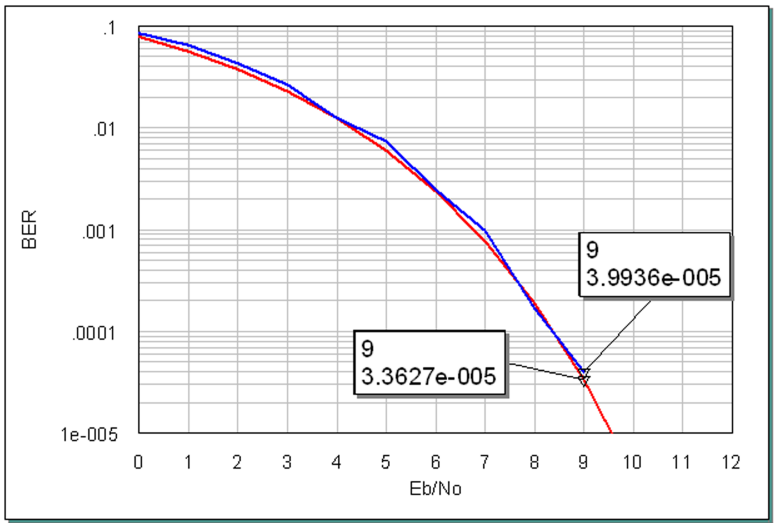


Figure 6-9: Adjacent channel simulation

the use of the equation, $V_{RMS} = \frac{V_{PEAK}}{\sqrt{2}}$ to compute the RMS voltage is justified. The maximum transmitted power is thus computed to be 62 mW over 50Ω load.

Chapter 7

Conclusions and Future Scope

7.1 Introduction

The research contributions of this thesis are summarized in this chapter. The future research scope is also outlined in order to provide some possibilities of extension of this research.

7.2 Technical summary and Contributions

Frequency Hopping Spread Spectrum systems are spread spectrum systems in which spreading is achieved by direct modulation of the data modulated carrier by a wideband spreading signal or spreading code. The spreading signal is chosen in order to facilitate demodulation at the receiver intended for as well as to make demodulation the most difficult for an unintended user [157]. The information signal was spread by the spreading sequence and then modulated on a carrier to get the resulting spread output [158]:

$$s(t) = d(t)\, c(t) \cos(2\pi f_{RF} t) \tag{7.1}$$

During the dispreading process in the receiver auto-correlation (AC) and cross-correlation (CC) functions are performed.
A custom chip design of this transceiver is a complex work and this thesis is a first attempt towards an on chip implementation.
To enable an effective and functional transceiver design, the relationship of the sub-systems to the integrated system was conceptualized and validated by simulation using Microwave Office . Some of the subsystems had to be designed from first principles and others were designed by referral to extensive research conducted elsewhere. The

following are the highlights of some of the achievements:

- **Voltage controlled oscillator**
  A current starved voltage controlled ring oscillator was conceptualized, designed and simulated. The VCO architecture provides high linear relationship between oscillation frequency ranging from $0.7-1.75$GHz with a tuning range of 75%. The phase noise achieved is -88 dBc/Hz at an offset frequency of 1MHz. The linear frequency sweep is obtained without employing additional compensation circuitry and hence less circuit complexity, die area and less power consumption.

- **Low noise amplifier**
  A wideband low noise amplifier has been designed in CMOS technology and was simulated with a large operating bandwidth of $0.6-9$GHz. L-type input matching network was employed to fix the Q-factor and p-type output matching network was employed to achieve extra degree of freedom to adjust the operating bandwidth. A gain of $\sim$ 27dB was obtained for the frequency range of $0.9-6$GHz and a noise figure (NF) of $<$ 2.5dB was obtained which are reasonably good compared to the reported works.

- **RF operational amplifier**
  A radio frequency operational amplifier was designed using the standard two-stage topology to achieve a unity gain bandwidth of 10GHz and a gain of around 22 dB with a phase margin of $\sim 45^0$. Power supply rejection ratio of 30 dB (PSRR+) and 60 dB (PSRR-) and a CMRR of 80 dB was achieved. The choice of the amplifier topology was attributed to improved gain, better noise performance and operating bandwidth.

- **Log and Anti-log Amplifier**
  A logarithmic and an anti-logarithmic amplifier were designed employing the pre-designed RF op amp around the op amp based classical architectures of log and ant-log amplifiers.

- **Differentiator and Integrator**
  A differentiator and an integrator circuit was constructed around the RF op amp based on classical op amp based architecture. The external passive component values were so chosen that the output voltages of both the circuits remain at the input voltage levels.

- **Subtracting circuit**
  A subtracting circuit was also designed around the standard op amp based architecture.

- **Square rooting circuit**
  A CMOS square rooter was designed to achieve square root of analog voltages.

- **Precision rectifier**
  A new precision rectifier circuit capable of rectifying very low input signals, below the diode knee voltages was conceptualized and simulated. Discrete implementation of the circuit at low frequencies was validated by experimental results. The architecture was extended to RF regime using CMOS subcircuits and simulated. The architecture was further modified to remove the frequency dependency. The modified circuit was simulated and the results satisfied the theoretical expectations.

- **Frequency-to-voltage converter**
  A new architecture for frequency-to-voltage conversion was conceptualized and developed. The innovation lies on the utilization of the transition band of a high pass filter over which the gain and the input signal frequency has a linear relationship over a good bandwidth compared to reported works. The filter output was further rectified by the precision rectifier to a dc voltage which is proportional to the input signal frequency.

- **Comparator**
  A 3-bit comparator which is the building block of the flash ADC circuit employed for conversion of analog-to-digital conversion was designed using high speed CMOS transistors. As we need a 2-bit ADC hence we need three comparators which were designed using the RF op amp described in section .The comparator generates a high when the input voltage exceeds a reference voltage and acts as a one-bit ADC. The outputs of the comparator is in the form of thermometer code (TC) which are to be converted to 2-bit binary using a digital encoder to obtain the transmitted digital signal.

- **Digital sub-systems**
  Several digital sub-systems were designed from first principle (albeit that they are conventional circuits). Some design simplifications were done wherever possible. Most of the digital sub-systems were achieved by using high speed CMOS devices described in chapter 4.

7.3 Future Scope

This thesis has laid the foundation for integration of a simplified direct conversion frequency hopped spread spectrum transceiver. Despite the extensive work that have been presented, there are some area pertaining to the transceiver design that are not dealt with in this work and is left for future work.
For further improvement of the proposed work, following iterations can be made.

- each sub-system can be further optimized independently
- reduce the number of op amps used in the FVC by custom-designed circuits for functions like squaring, log and anti-log conversion, differentiation and integration in order to reduce circuit complexity and power consumption.
- Investigate the deployment of alternative architecture for the analog sub-systems such as LNA, VCO and FVC.
- Investigate the designs in low power and ultra low power CMOS technology such as 180nm or 90nm CMOS technology for ultra-low power applications of the proposed transceiver.
- more detailed investigations may be made for multi-user analysis.
- a fully integrated transceiver can be designed and fabricated by integrating the transmitter with the receiver and deploying a power amplifier, an on-chip antenna and a RF duplexer to switch between transmit and receive modes.

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