ABSTRACT

Downscaling of MOS devices has offered new dimensions to the CMOS technology. But in the nanometer regime several effects degrades the performance of the MOS transistors, which are popularly known as short channel effects. Though researchers have tried to solve this problems completely or partially by material property improvement or employing different structure, but this is a fact that the downscaling of MOS devices cannot continue forever, thereby motivating the researchers to search for new technology which can be a proper substitute of CMOS technology.

As a predecessor of CMOS technology several alternative technologies have been under investigation for last two decades. These candidate technologies include, amongst others, Single Electron Device (SED), Carbon Nanotubes, Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Diodes (RTD), and Magnetic Spin devices. Single electron tunneling Technology is the most deserving future technology to meet the required increase in density and performance and decrease in power dissipation. The research work on single electron tunneling technology can be divided into two catagories. The first category consists of device research and is mainly focused on device fabrication and fabrication technology aspects. This is an expensive area of research and hence our country is lacking in this area of research. The second category of research focuses on the modeling and application of

single electron devices. We need a proper simulation environment to explore this novel technology. Though we had some established simulation software, what we actually lack is an efficient model which can represent the characteristics of a single electron transistor (SET) very well. Initially, we proposed a macro model of single electron transistor, which can be applied for symmetric as well as asymmetric SET. Here we have modified the existing macro model by incorporating a voltage controlled current source, to improve the coulomb blockade part of the characteristics. A comparison with other modeling and simulation approaches is given to verify the simulation result. A single electron inverter is designed using the proposed model to check the validity of the model. Then the applicability of the model is tested by designing a multi-peak NDR circuit. Also a Integrator circuit is designed to check the linearity of the device. So, the harmonic distortion and inter modulation distortion is investigated in the course of testing the linearity. To improve the accuracy of the simulation process we proposed a compact analytical model of SET, considering eleven island states. The proposed analytical model can be applied for symmetric, asymmetric devices and considers background charge issues. The model also provide some degree of freedom in terms of the no of island states and the value of n_{opt}. Various basic circuits are designed and simulated using the proposed analytical model. Next an error probability independent delay model is proposed for multiple

tunneling events. Two different delay model is derived considering same tunneling rates and different tunneling rates. Finally to prove its accuracy, the delay of an inverter and universal logic gates are calculated using the model and compared with the existing model and monte carlo method.

Next we explored a type of single electron device, known as threshold logic gates, which reduces the size and the power consumption of the designed circuits compared to SET based circuits by reducing the number of tunnel junctions. First a 4:1 multiplexer is designed and its simulation results are verified. We also checked the reliability and stability of the designed multiplexer. A general logic function is implemented using the programmable logic array architecture. Then we proposed the threshold logic gate as a neuron cell. The proposed neuron cell is used to design a 3 cell shadowing CNN circuit. Finally the reliability and stability of the designed CNN circuit verified.

Though threshold logic approach reduces the size and power consumption of the circuits, still it is unable to solve the inherent problems of SET, which are low gain, very low temperature operation and background charges. It is also worthy to mention that OS devices have also some limitations. So the SET and MOS devices can be combined to come up with SET-MOS hybrid technology, which will take up the advantages of both the technologies and will mitigate the drawbacks as well. A pass transistor logic based universal logic gates

are designed using hybrid SET-MOS approach. Then the same logic function that was implemented using threshold logic approach is designed and simulated. A comparison is laos given between the threshold logic approach and hybrid SET-MOS approach in terms of simulation results, delay and power consumption. We also proposed an approach to analyze the reliability and stability of the hybrid SET-MOS circuits. The proposed approach is applied to universal logic gates designed following hybrid SET-MOS approach.

Thus the present thesis contains a brief detail about the basics of SETs alonf with some proposed models of SET and subsequent applications of those models. SET-MOS hybrid concept together with threshold logic gates (TLG) and hybrid pass transistor based logics are focused. Some important circuits are realized using those concepts. Circuit stability and reliability analysis are also investigated in the present thesis.