Single Electron Transistor and its Hybridization with MOSFET for Increasing Density of Integration and Reducing Power Consumption

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CERTIFICATE FROM THE SUPERVISORS

This is to certify that the thesis entitled ***"Single Electron Transistor and its Hybridization with MOSFETs for Increasing Density of Integration and Reducing Power Consumption"*** *submitted by* **Shri**. ***Amit Jain,*** *who got his name registered on* ***08/10/2013*** *[****D-7/E/812/13****] for award of Ph.D. (Engg.) degree of Jadavpur University is absolutely based upon his own work under the supervision of* ***Prof. Subir Kumar Sarkar and Dr. N. Basanta Singh*** *and that neither his thesis nor any part of the thesis has been submitted for any degree/ diploma or any other academic award anywhere before.*

1.

2.

ABSTRACT

Downscaling of MOS devices has offered new dimensions to the CMOS technology. But in the nanometer regime several effects degrades the performance of the MOS transistors, which are popularly known as short channel effects. Though researchers have tried to solve this problems completely or partially by material property improvement or employing different structure, but this is a fact that the downscaling of MOS devices cannot continue forever, thereby motivating the researchers to search for new technology which can be a proper substitute of CMOS technology.

As a predecessor of CMOS technology several alternative technologies have been under investigation for last two decades. These candidate technologies include, amongst others, Single Electron Device (SED), Carbon Nanotubes, Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Diodes (RTD), and Magnetic Spin devices. Single electron tunneling Technology is the most deserving future technology to meet the required increase in density and performance and decrease in power dissipation. The research work on single electron tunneling technology can be divided into two catagories. The first category consists of device research and is mainly focused on device fabrication and fabrication technology aspects. This is an expensive area of research and hence our country is lacking in this area of research. The second category of research focuses on the modeling and application of

single electron devices. We need a proper simulation environment to explore this novel technology. Though we had some established simulation software, what we actually lack is an efficient model which can represent the characteristics of a single electron transistor (SET) very well. Initially, we proposed a macro model of single electron transistor, which can be applied for symmetric as well as asymmetric SET. Here we have modified the existing macro model by incorporating a voltage controlled current source, to improve the coulomb blockade part of the characteristics. A comparison with other modeling and simulation approaches is given to verify the simulation result. A single electron inverter is designed using the proposed model to check the validity of the model. Then the applicability of the model is tested by designing a multi-peak NDR circuit. Also a Integrator circuit is designed to check the linearity of the device. So, the harmonic distortion and inter modulation distortion is investigated in the course of testing the linearity. To improve the accuracy of the simulation process we proposed a compact analytical model of SET, considering eleven island states. The proposed analytical model can be applied for symmetric, asymmetric devices and considers background charge issues. The model also provide some degree of freedom in terms of the no of island states and the value of n_{opt}. Various basic circuits are designed and simulated using the proposed analytical model. Next an error probability independent delay model is proposed for multiple

tunneling events. Two different delay model is derived considering same tunneling rates and different tunneling rates. Finally to prove its accuracy, the delay of an inverter and universal logic gates are calculated using the model and compared with the existing model and monte carlo method.

Next we explored a type of single electron device, known as threshold logic gates, which reduces the size and the power consumption of the designed circuits compared to SET based circuits by reducing the number of tunnel junctions. First a 4:1 multiplexer is designed and its simulation results are verified. We also checked the reliability and stability of the designed multiplexer. A general logic function is implemented using the programmable logic array architecture. Then we proposed the threshold logic gate as a neuron cell. The proposed neuron cell is used to design a 3 cell shadowing CNN circuit. Finally the reliability and stability of the designed CNN circuit verified.

Though threshold logic approach reduces the size and power consumption of the circuits, still it is unable to solve the inherent problems of SET, which are low gain, very low temperature operation and background charges. It is also worthy to mention that OS devices have also some limitations. So the SET and MOS devices can be combined to come up with SET-MOS hybrid technology, which will take up the advantages of both the technologies and will mitigate the drawbacks as well. A pass transistor logic based universal logic gates

are designed using hybrid SET-MOS approach. Then the same logic function that was implemented using threshold logic approach is designed and simulated. A comparison is laos given between the threshold logic approach and hybrid SET-MOS approach in terms of simulation results, delay and power consumption. We also proposed an approach to analyze the reliability and stability of the hybrid SET-MOS circuits. The proposed approach is applied to universal logic gates designed following hybrid SET-MOS approach.

Thus the present thesis contains a brief detail about the basics of SETs alonf with some proposed models of SET and subsequent applications of those models. SET-MOS hybrid concept together with threshold logic gates (TLG) and hybrid pass transistor based logics are focused. Some important circuits are realized using those concepts. Circuit stability and reliability analysis are also investigated in the present thesis.

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Chapter 1

Introduction and Organization of The Thesis

1.1 Introduction

The first integrated circuit have been created by Jack Kilby [1.1]. After that six decades have been elapsed and during this period researchers have witnessed enormous improvement which have changed the fate of semiconductor industry. The continuous scaling of the MOSFETs have been the main motivation towards the growth of the modern semiconductor industry. The first MOSFET scalling methodology was proposed by Dennard et al, based on constant electric field theory [1.2]. Later these scaling methodologies have been revised depending on the state of the art demand. The down scaling of MOSFETs were going on smoothly following Moore's law [1.3], until the device dimension reached sub 100 nm regime. In the sub 100nm regime MOSFET device first faces a series of problems called the short channel effects (SCEs), Drain induced barrier lowering (DIBL), gate leakage, punch through, high field mobility degradation and static leakage. These issues are being handled by the researcher by material property and device

structure improvement [1.4]-[1.6]. High K dielectric is used as the gate material to nullify the gate leakage. SOI structure has been proposed to cope with DIBL and SCEs [1.7]. Though these solutions seems to work well but the fact is the downscaling of CMOS technology cannot continue forever. So researchers around the world are looking for novel nanotechnology devices which can efficiently replace the CMOS technology. Single electron tunneling technology is one of the most promising candidate for future nanotechnology solutions.

As the name implies single electron devices offers the control of electronic charge at the level of one electron. The device operates by transferring electrons across the tunnel junctions onto the nanometer scaled islands. The first concept of single electron charging energy was proposed by C. J. Gorter in relation to granular metal films [1.8]. In mid 70's the single electron effect on granular films was more clear by the work of Kulik and Sekhtar [1.9].

In mid 80's K. K. Likharev and co-workers investigated the single electron charging effects in tunnel junctions [1.10]. This work was well extended by the observation of coulomb blockade effect in granular films [1.11]. By the late 1980's, due to advancement in technology it was possible to fabricate nanoscale island and tunnel junctions. Which led to the fabrication of the first single electron device, single electron transistor by fultan and dolan [1.12]. After that various research work was performed to improve the fabrication process as well as inserch of

different single electron devices. In 1994 ali and ahmed proposed that the single electron device can also be fabricared using silicon on insulator (SOI) material [1.13]. The major break through came at 1995 whem Takahashi et al fabricated the first room temperature operated single electron transistor [1.14] in SOI material using electron beam lithography and oxidation.

To explore any technology we need good analytical models as well as efficient simulation methodologies. N. Bakhalov et al [1.15] were the first to use Monte Carlo approach for single electronics case. Later this approach is used to design the most popular single electronics simulation software, SIMON [1.16]. The master equation method was first proposed by E. Ben-Jacob et al [1.17]. All the compact analytical model proposed so far in the literature are based on master equation approach. The first analytical model of single electron transistor was proposed by Uchida et al [1.18]. After that a few analytical model was being reported in the literature. Some of them are suitable for both symmetric and asymmetric SET whereas some model incorporated large number of island states to increase the value of applicable supply voltage. Also a third method is also used to simulate single electronics circuits which is SPICE macro modeling approach [1.19]. The macro model [1.20] are designed using different microelectronic components like voltage sources, current sources, resistors and capacitors. So in today's research work a single electronics circuit is simulated either

incorporating the analytical or macro models in SPICE environment or using nanoelectronics simulation softwares like SIMON.

In last fifteen years several novel research work have been reported in the literature which have lifted the single electron tunneling technology to the next level. Apart from implementing logic gates several other important digital circuits like encoder [1.21], quantizer circuit [1.22] was implemented by the rsesaerchers. Also some research work was reported on converter circuits [1.23]-[1.24]. In 2001 Lageweg et al implemented a novel single electronics device known as threshold logic gate [1.25]. After that a lot of work has been done to explore this novel approach [1.26] – [1.27].

Threshold logic gates reduces the number of tunnel junctions used to design a circuit compared to single electron transistor based design, hence the total area and the power consumption is reduced. But the inherent problems like low gain and background charge issue is still there in threshold logic based circuits. So researchers have come up with an idea of combining the single electron tunneling technology and CMOS technology to combine their respective features in a new technology [1.28]. Here either the nmos or pmos of a circuit are replaced with single electron transistor. All the basic gates and different logic circuits have already been implemented using SET-MOS hybrid technology [1.29]. A PLL circuit and nano recongirable logic cells are also been designed using hybrid SET-MOS approach [1.30]-[

1.31]. Recently M. Abutaleb et al proposed a differential logic style for hybrid SET-MOS logic circuits [1.32]. Also some important aspects of this approach was repored by R. Parekh et al. [1.33].

The macro model reported in the literatute lacks accuracy. Also no analytical model is reported which considers a large number of states and at the same time can be applied for symmetric and asymmetric SET as well. Which motivated us to develop efficient macro model and compact analytical model so that single electron tunneling technology can be explored in all regime of circuits. The dealy calculation used for single electronics circuits was dependent on arbitary value of probability of error. So we tried to come up with a proposal where the dealy calculation will be indepenedent of the probability of error value. At the same time we tried explore some important threshold logic based circuits and hybrid SET-MOS circuits. Till now there was no means to analyze the reliability and stability of hybrid SET-MOS circuits. That actuated us to work on finding some way so that the reliability and stability of hybrid circuits can be analyzed.

1.2 Organization of the Thesis

In this work we have tried to explore various possibilities of single electron tunneling technology starting from analytical modeling to designing various benchmarked circuits. A delay model is proposed

for multiple tunneling events. We have designed different circuits using single electron threshold logic gates. Finally different hybrid SET-MOS circuits are designed, simulated and verified. In this section a brief overview of all the chapters are given.

In chapter 2, an analytical model of SET is proposed that considers eleven island states. The proposed model is applicable for symmetric as well as asymmetric SET. It incorporates background charge problem and can be applied for multi gate SET. A brief investigation is given on the accuracy of the proposed model. The V-I characteristics of the designed SET is thoroughly studied. Finally different benchmarked circuits are designed using the proposed SET model and simulated in SPICE environment. Also a comparison with the other existing model is given to verify the accuracy of the model.

In capter 3 a brief description of different modeling approaches and simulation methodologies are given. A macro model suitable for simulating single electronics circuits is proposed. The significance of different macro model parameters are explained clearly. The V-I characteristics of the device is thoroughly investigated. A comparison with other modeling and simulation approaches is given to verify the validity of the proposal. Finally a single electron inverter is designed using the proposed model. The static and dynamic characteristics of the invereter is studied to observe the effect of the macro model parameters. As the negative differential circuits are very useful in

designing various circuits so a multi peak NDR circuit is designed using the macro model. An integrator circuit is designed to check the responses of the proposed macro model. The harmonic distortion is performed to check the linearity of the integrator crcuit. Also a total difference frequency distortion (TDFD) test is performed to analyze the intermodulation distortion.

The dealy model available in the current literature considers only single tunnel event which is suitable for threshold logic based circuits. In chapter 4 an error probability independent delay model is proposed which can takes into account multiple tunneling event. Here two different models are proposed, one for constant tunnel rate events and other considering variable tunnel rate events. The derivation of both the proposed model is briefly given to improve the readability of the text. An inverter circuit is taken and its delay is calculated using the proposed model and finally delay calculations is extended for universal logic gates also. Finally a comparison is made with the existing model and the monte carlo method considering variable number of tunneling events.

In chapter 5 intially a brief description of the threshold logic approach is provided. The general structure of a threshold logic gate is thoroughly explained. The basic logic gates using threshold logic approach are already been designed by the researchers. So we started with designing a 4:1 multiplexer using threshold logic gates and

inverters. The total design flow is clearly explained along with analysis of reliability and stability of the designed circuit is analyzed. Next a general logic function is implemented using programmable logic array architecture. Parallel distributed processing architectures are gaining importance due to its huge processing capabilities. As large number of devices are involved, so area and power consumption becomes real issues in this kind of architectures. We have proposed threshold logic gate as a neuron cell which can be used to design cellular neural network (CNN) based designs. A 3 cell shadowing CNN circuit is implemented using the proposed neuron cell. Finally the design circuit is thoroughly analyzed with an emphasis on its reliability and stability issues.

In chapter 6 different SET-MOS hybrid circuits are designed and implemented. Here the universal logic gates are implemented employing pass transistor logic. the design circuit is simulated in SPICE environment using BSIM model for MOS transistos and MIB model for SET. The simulation results are plotted to verify the operation. Then the same logic function that was implemented using threshold logic approach is implemented using hybrid SET-MOS approach so that a comparison can be made between thses two approaches. The design circuit is also implemented using our proposed model for variable number of island states. Finally a comparison is given between threshold logic approach and hybrid SET-MOS

approach with respective number of devices involved, different parameter values, delay and power consumption. The reability and stability of the hybrid SET-MOS circuits cannot be analyzed using the general approach as the MOS transistors can not be simulated in single electronics software. We have proposed an approach to analyze the reliability and stability of the hybrid SET-MOS circuits. Then this approach is applied to the universal logic gates and the results are verified.

In the last chapter we have concluded the work. Some concluding remarks are given on the design issues of the respective approaches. The advantage and disadvantage of theses approaches are clearly explained. Some comments are made on the realiabilty and stability analysis of the designed circuits.

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Chapter 2

Basics of Single Electron Devices

2.1 Introduction

Single electron tunneling technology is all about the possibility of controlling the movement of a single electron or a small number of electrons. To be more specific we can add precisely one electron to a electrically neutral grain which means we have control over the movement of a single electron [2.1]. Till now various single electron devices have been reported in the literature. Single electron box, single electron transitor, pumps, transtiles, threshold logic gates, one and two dimensional array of tunnel junctions are the single electron devices proposed so far. The simplest single electron device that exhibits single electron charging effects is single electron box [2.2]. In this device a metal granule is connected to a tunnel junction. The first single electron device, single electron transistor was proposed and fabricated by fultan and dolan [2.3]. It is also the most studied single electron device. After this various single electron devices was proposed and demonstrated. this includes single electron transtile [2.4], pump [2.5]-[2.6], and multiple tunnel junction (MTJ) [2.7]-[2.10]. Some single

electron memory circuits [2.11]-[2.14] are also been proposed in the literature.The concept of threshold logic gate was first proposed by Lageweg et al [2.15]. After that it is being used to design various logic circuits as it reduces the size of the circuits. Due to their importantce and contribution to the single electron tunneling technology we have concentrated mainly on single electron transistors and threshold logic gates.

2.2 Basics of Single Electron Tunneling Technology

The energy required to charge a island or granule with equivalent capacitance C is known as the charging energy or coulomb energy, given as [2.16]

$$E_C = \frac{e^2}{2C} \tag{2.1}$$

If the thermal energy becomes greater than the charging energy then the the thermal fluctuation in energy suppresses the coulomb blockade phenomena and the circuit becomes unstable. This condition can be expressed as

$$E_C = \frac{e^2}{2C} > k_B T \tag{2.2}$$

Another condition for the stable operation of single electronics circuits is that the quantum fluctuation in the number of electrons on the island

should be negligible i.e electrons need to be localized on the islands. To validate this condition the resistance of the tunnel junctions must be greater than the quantum of resistance (25.8KΩ).

The charge transport phenomena of single electronics circuit is well described by the orthodox theory of single electron tunneling. Following this theory the tunneling rate is calculated as [2.16]

$$\Gamma = \frac{\Delta E}{e^2 R_j \left(e^{\Delta E/k_B T} - 1\right)} \tag{2.3}$$

Here ΔE is the change in electrostatic energy of the system due the tunneling of an electron. There are some assumptions regarding orthodox theory, which are

1. The electron energy of the island is quantized.
2. The tunnel junction traversal time of electrons is much smaller than any other time constant in the system.
3. Co-tunneling is ignored.
4. Electrons are localized on the island.

2.3 Single Electron Transistor

Initially the single electron charging effect was observed in single island double tunnel junction system as shown in Fig. 2.1 [2.1]. It can be seen that an island is sandwiched between two tunnel barrier or tunnel junctions. Now if the width of the tunnel junctions are very

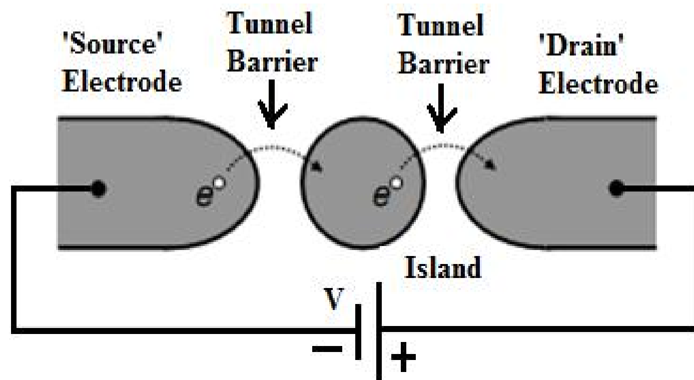

Fig. 2.1 Schematic Diagram of a Single Island, Double junction system

small, on the order of 10nm or less, then the voltage applied across the island can transfer electron on to or off the island through quantum mechanical tunneling. Now electron can tunnel across the junction if the applied voltage is equal to or greater than the charging energy associated to adding the electron to the respective island [2.17]. If the equivalent capacitance of the island is C then the charging energy required for an electron to tunnel on to the island is $e^2/2C$. Now the electrodes of Fig. 2.1, is referred as the drain and source electrodes, where the bias is applied across the drain electrode and the source electrode is grounded. If the values of Vds becomes greater than the charging energy then electrons tunnel across the junction on to the island. the same process happens for negative values of Vds. For lower values of Vds electron cannot tunnel and this is known as coulomb blockade effect as shown in Fig. 2.2. After the first electron tunneling

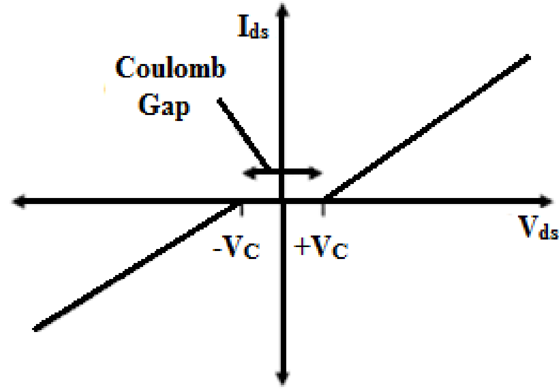

Fig. 2.2 Coulmb Blockade Characteristics of Symmetric SET

blockade effect as shown in Fig. 2.2. After the first electron tunneling the charging energy required for the second electron to tunnel is e^2/C. If the drain to source voltage overcomes this charging energy then one more electron tunnel across the junction and two electrons exist in the island. In this way the number of electron in the island increases one by one. If the tunnel rates across the two junctions are different then current increases in the step wise manner as observed in Fig. 2.3. There are some assumptions to be made based on the orthodox theory of single electron tunneling [2.16]. The most popular single electron device is single electron transistor. This is formed by adding a third terminal, gate to the double junction system explained in Fig. 2.1. The circuit diagram of the single electron transistor (SET) is shown in fig. 2.4, where the gate terminal is connected to the island by capacitor Cg [2.3].

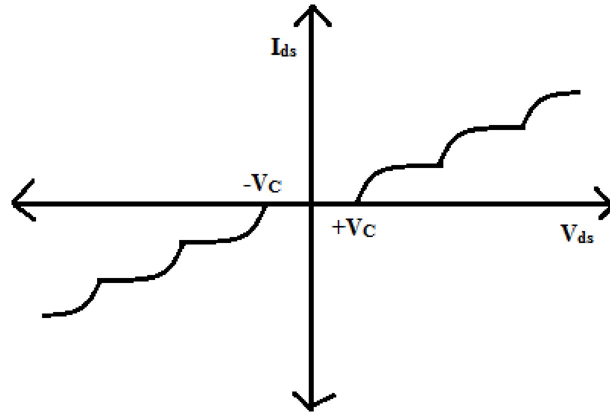

Fig. 2.3 Coulmb Blockade Characteristics of Asymmetric SET

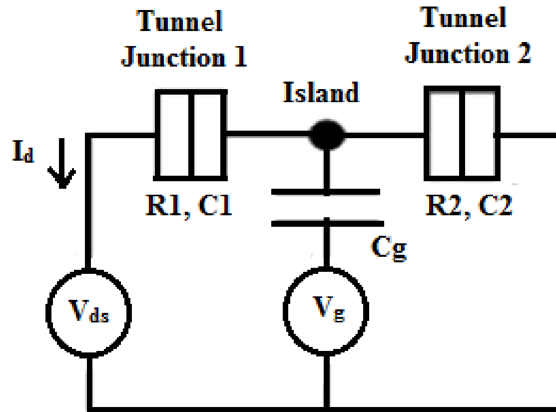

Fig. 2.4 Schematic of Single Electron Transistor

The gate terminal added extra functionality to the system by controlling the Fermi level of the system. The Id-Vgs characteristics of the SET is shown in Fig. 2.5. It is observed from the Fig. 5 that for a fixed value of vds, Id-Vgs oscillates periodically, which is known as the coulomb oscillation characteristics.

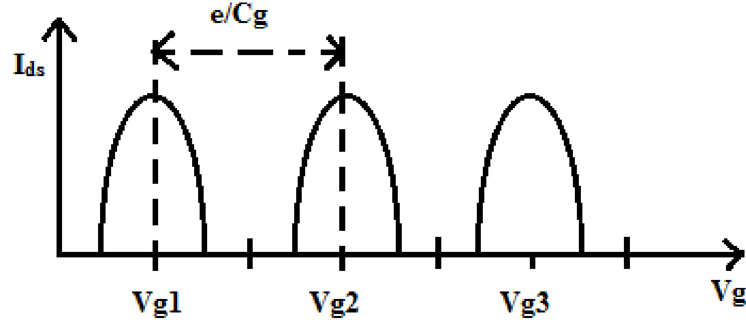

Fig. 2.5 Coulomb Oscillation Characteristics

2.4 Threshold Logic Gate

Other than single electron transistors there is one more popular single electron device, which is called single electron threshold logic gate (TLG) [2.15]. In a TLG the logic '1' and '0' values are interpreted by the presence or absence of the unit charge. So TLG can be thought as an alternative to Boolean logic gates. It operates on the principle of comparing between the wighted sum of the inputs and a threshold value. If the wighted sum of the inputs is greater than the threshold value, the output will be logic '1' else the output is logic '0'. The working function is represented as

$$\mathrm{F(X)} = sgn\{\mathrm{Y(X)}\} = \begin{cases} \text{if} \quad F(\mathrm{X}) < 0 \\ \text{if} \quad F(\mathrm{X}) \geq 0 \end{cases} \tag{2.4}$$

$$F(X) = \sum_{i=1}^{n} w_i x_i - T \tag{2.5}$$

Where X_i are the inputs and W_i are corresponding integer weights. The structure of the TLG is shown in Fig. 2.6. Here the input voltages V_p, weighted by their input capacitors C_p are added to the node x and inputs V_n, weighted by their input capacitors C_n are subtracted from voltage across the tunnel junction. The bias voltage V_b is used to adjust the critical voltage of the junction.

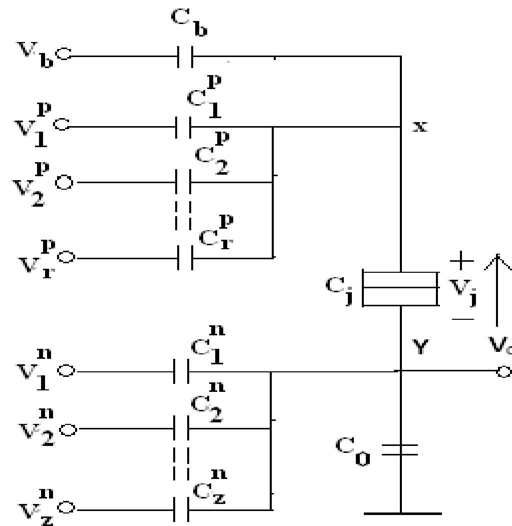

Fig. 2.6 threshold logic gate structure

The function F(X) can also be written as

$$F(X) = C_{\sum}^{n} \sum_{k=1}^{r} C_K^P V_K^P - C_{\sum}^{P} \sum_{l=1}^{S} C_l^n V_l^n - T \tag{2.6}$$

Where

$$T = \frac{1}{2}(C_{\sum}^{P} + C_{\sum}^{n}) - C_{\sum}^{n} C_b V_b \tag{2.7}$$

$$C_{\sum}^{p} = C_b + \sum_{k=1}^{r} C_k^P \quad (2.8)$$

$$C_{\sum}^{n} = C_0 + \sum_{l=1}^{S} C_l^n \quad (2.9)$$

We will consider the logic '0' value as 0V. The logic '1' value is calculated as logic '1'=0.1*q_e/CV, considering the capacitance value as 1 aF we get the logic '1' value as 16 mV.

All the basic types of digital circuits have been implemented using threshold logic gates. Threshold logic gates reduces the number of tunnel junctions used to design a circuit compared to single electron transistor based design, hence the total area and the power consumption is reduced. But the inherent problems like low gain and background charge issue is still there in threshold logic based circuits. So researchers have come up with an idea of combining the single electron tunneling technology and CMOS technology to combine their respective features in a new technology [2.18]. Here either the nmos or pmos of a circuit are replaced with single electron transistor. A SET-MOS hybrid inverter circuit is shown in Fig. 2.6. All the basic gates and different logic circuits have already been implemented using SET-MOS hybrid technology . As MOS transistors cannot be simulated in single electron software, SET-MOS hybrid circuits are simulated in SPICE environment by using the analytical or macro model of single electron transistor.

In fabrication process trapped charges are formed in the tunnel junctions and in the substrate around the island [2.19]. Thses trapped charges influences the total charge of the island and makes the circuit unreliable. Several experiments have been performed to observe the effect of background charge fluctuations [2.20]-[2.21] and to locate their sources. Some researchers suggested that the noise generated from the tunnel barriers have the maximum contribution to the background charge noise [2.22]. Where as the substrates surrounding the island is also been reported as the main contributor [2.23]-[2.24].

If the thermal energy becomes greater than the charging energy of the circuit, electron tunneling occurs due to thermal fultuation in energy, which causes for the instability of the circuit. The stability of single electronics circuits is analyzed using stability plots, ahich are plotted by simulating the circuit in SIMON software. But we cannot analyze the stability of a hybrid SET-MOS circuit using SIMON, as the MOS devices cannot be simulated in ant single electron based software.

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Chapter 3

Macro Model of Single Electron Transistor

3.1 Introduction

Single electron transistor is one of the most promising candidate for future VLSI/ULSI solutions[3.1]-[3.2]. A lot of works have been reported in the literature on single electron transistor [3.3]-[3.5] and SET-MOS based circuit design [3.6]. To explore any new technology we need a proper simulation environment where different types of circuits can be designed and analyzed efficiently. Being a new technology single electron tunneling technology was in need of a simulation environment where devices and circuits can be analyzed and which will make it able to compete with other existing technologies. Basically there are three different approaches for simulation of single electronics circuits, SPICE macro modeling, Monte Carlo approach and master equation approach [3.7]. The Monte Carlo method is a probabilistic approach which is based on stochastic integration [3.8]. In this method random tunnel times are calculated for all the possible tunneling events and the correlation in these pseudo random number can affect the result drastically [3.9]. Due to stochastic sampling, Monte Carlo

method takes a long time to simulate circuit with large number of nodes. In master equation approach a set of transport equations which represent the tunneling events are solved to calculate the probability of occupancy of different island states[3.7]. So in this method we need to know the number of relevant island states which is obviously a tedious job to perform. Macro model approach is the simplest of all these three approaches. Here we designed an equivalent circuit of the device using basic circuit components such as voltage and current sources, diodes and resistors [3.10]. In this approach we are not concerned about the probability of tunneling events rather we are interested only in KCL and KVL equations. As a fact the computation time for macro model approach is lesser compared to other methods. For small circuits master equation approach is faster than the Monte Carlo method. But for larger circuits the master equation method becomes complex due to involvement of large number of nodes, and macro model approach takes much lesser time.

In SPICE simulation it is always assumed that only the terminal characteristics of devices affects each other. But this assumption may not not hold in case single electron transistor as for single electron transistor the current is calculated considering the possible charge states of all island together. We consider the interconnection between adjacent SETs is so large that it actually acts as a reservoir for the

adjacent SET, which makes us able to simulate SET in SPICE environment. So if the interconnection is very large SET shows same characteristics whether it is isolated or a part of a large circuit. It is reported that if CL>6.25Cj then SET performs well, where Cl and Cj are the load capacitance and tunnel junction capacitance respectively.

3.2 Literature Review

Over the years several macro models [3.11]-[3.13] have been reported in the literature which can be used to design single electronics circuits. The first macro model of single electron transistor was proposed by Yu et al [3.11], which is build using resistors, diodes and voltage sources as shown in Fig. 3.1. Later Wu et al [3.12] modified this model by incorporating two back to back diodes in the model to make the gate current negligibly small. Karimian et al further included a switch capacitor circuit in the existing model [3.13]. The switch capacitor circuit which works as a quantizer circuit is incorporated to calculate the timing of electron tunneling. In this work we have incorporated a voltage control current source in Yu's model to improve the accuracy. The main disadvantage of Yu's model is that it is unable to predict the coulomb blockade characteristics as the current in the coulomb blockade region is not zero rather it increases linearly with the drain to source voltage. Though in case of Wu and Lin's model, the current is zero for a particular value of Vds, it doesn't provide any plots for other

values of drain voltage so it provides incomplete information regarding coulomb blockade characteristics.

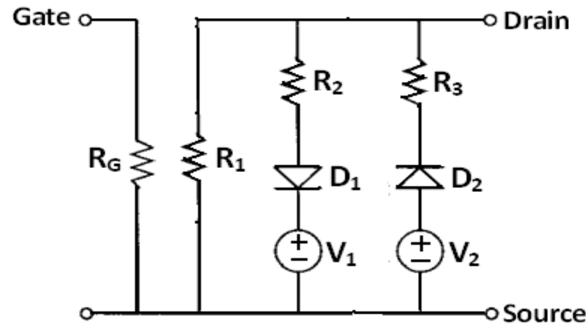

Fig. 3.1 The macro model of Yu et al.

3.3 The Macro Model

The proposed macro model is shown in Fig. 3.2. It can be observed by comparing Fig. 3.1 and Fig. 3.2 that resistor R1 of Yu's model is replaced by a voltage controlled current source g1 in the proposed

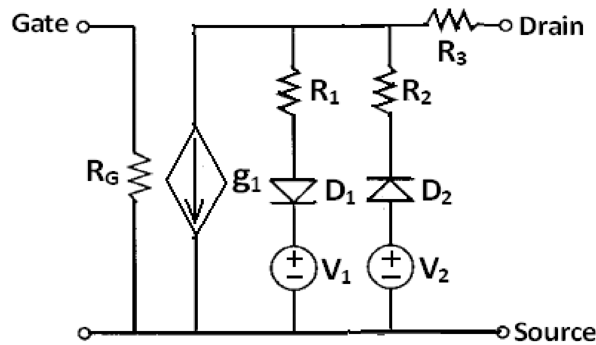

Fig. 3.2 The proposed macro model, where R_1 of Yu's model is replaced by a voltage controlled current source g_1

```
*D=Drain
*G=Gate
*S=Source

.option
.macro SET D G S
.param
+pi=3.14
+CF1=40
+CI2=0.2e-9
+CR1=300e+6
+CR2=220e+6
+CR3=0.5e-9
+CR4=0.5e-9
+CVp=0.02
V2 5 S DC 0.02
V3 7 S DC -0.02
RG G S 100G
RR1 1 4 R='(CVp/ (CI2-2*CVp/ (2*CR1+CR2*cos (CFl *pi*V (G, GND)))))/K1'
RR2 1 6 R='(CVp/ (CI2-2*CVp/ (2*CR1+CR2*cos (CFl *pi*V (G, GND)))))/K1'
RR3 1 D 1
D1 4 5 DIODE
D2 7 6 DIODE
g1 1 S cur='(CR3*sin (pi*V (G, GND)))/K2'
.MODEL DIODE D (N=0.01)
.eom
```

Fig. 3.3 SPICE macro model code of the proposed model.

model. The symmetric features of SET on both side of the coulomb blockade characteristics are predicted by a combination of diodes, resistors and voltage sources, denoted by D1, R1, V1 and D2, R2, V2 respectively. D1, R1, V1 and D2, R2, V2 controls the current in positivce and negative directions respectively assuring a bidirectional current flow. If the value of the critical voltage is greater than V1, the diode D1 gets On and current flows through resistor R1 and when it is less then V2, D2 gets ON and current flows through R2. The voltage controlled

current source g1 takes care of the coulomb blockade part of the characteristics. The resistor RG is used to isolate the gate terminal from the source terminal by restricting the current flow through it. The value of Rg is chosen very high compared to other resistors in the circuit so that it acts like an open circuit. A very small resistor R3 is also included in the circuit for measuring the overall drain current. This resistor contributes nothing in the operation of the macro model but helps in plotting the drain current. The SPICE code for the macro model is given in Fig. 3.3. Several parameters and scaling factors have been included in the macro model code to efficiently capture the characteristics of the device. In this code CF1, CI2, CR1, CR2, CR3, CR4 and CVp are macro model parameters and K1, K2, K3 are the scaling factors. The main three design components of the proposed macro model are R1, R2 and g1which are actually cosine function of the gate bias. The resistors R1 and R2 are expressed as

$$R1 = \left(\frac{CVp}{CI2 - \frac{2 * CVp}{CR1 + CR2 * Cos\left(CF1 * \pi * Vgs\right)}} \right) \Big/ K_1 \tag{3.1}$$

$$R2 = \left(\frac{CVp}{CI2 - \frac{2 * CVp}{CR1 + CR2 * Cos\left(CF1 * \pi * Vgs\right)}} \right) \Big/ K_2 \tag{3.2}$$

We can efficiently control the characteristics of the device, by controlling the values fitting parameters properly. It can be observed from (3.1) and (3.2) that two scaling factors K1 and K2 have been included in the expression of R1 and R2 respectively. Here K1 and K2 changes the range of drain current without affecting the I-V characteristics of single electron transistor. It is apparent that the values of R1 and R2 depends on K1 and K2, so to maintain the symmetry of the device, same values have been chosen for K1 and K2. As there are some significant disadvantages of asymmetric SET, in this work we have focused only on symmetric SET.

From the ideal characteristics of SET it can be observed that the gate to source voltage mainly have two functions. First, it acts like a parameter for Id-Vds curve for different values of Vgs keeping the nature of the curve same. It acts as a function for Id-Vgs curve which is oscillatory in nature. Keeping these facts in mind the expression for g1 is expressed as

$$g1 = \left(CR3 * Sin\left(\pi * Vgs \right) \right) / K_3 \tag{3.3}$$

Here the sine term is responsible for the oscillatory nature of Id-Vgs curve and the overall value of this expression gives a dc value to uplift the Id-Vds curve. The scaling factor K3 has been included in this expression to control the vertical shift of the Id-Vds curve for a fixed value of Gate to source value.

3.4 Simulation Results

The proposed macro model of single electron transistor is simulated in SPICE environment. For simulation purpose the following parameter values has been used: the gate capacitance Cg = 3.2aF, the junction capacitance Cj = 1.6 aF and the temperature T= 30K [3.11]. The values of the fitting parameters are chosen as CF1 = 40 [3.5], CVp = 0.02, CI2 = $0.2X10^{-9}$, CR1 = $300X10^{6}$ and CR2 = $220X10^{6}$. Id-Vds characteristics of the proposed model is shown in Fig. 3.4. The coulomb blockade and non coulomb blockade part of characteristics are clearly distinguishable in the figure. It can be observed that with increase in Vgs the grapgh shifts in upward direction. Thugh the same vertical shift is observed in Yu's model, but the nature of shifting is not fixed there. To prove the accuracy of the model a comparison has been shown in Fig. 3.5, between SIMON [3.14], MIB model [3.15], Yu's model, Wu's model and our model for coulomb blockade as well as non coulomb blockade regions. It can be observed that results obtained from our model closely matches with that of the Monte Carlo simulator SIMON. It is also observed that among all these models our proposed model covers the maximum drain current range which can be controlled by choosing suitable values of the respective scaling factors.

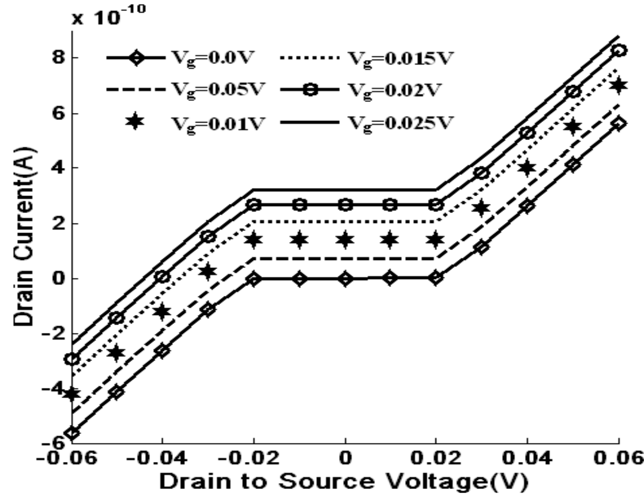

Fig. 3.4 Current-voltage characteristics of the designed SET where the gate biases is varied from V_g=0.0V to V_g=0.25V with an increment of 0.05V. For simplicity we have assumed K_1=K_2.

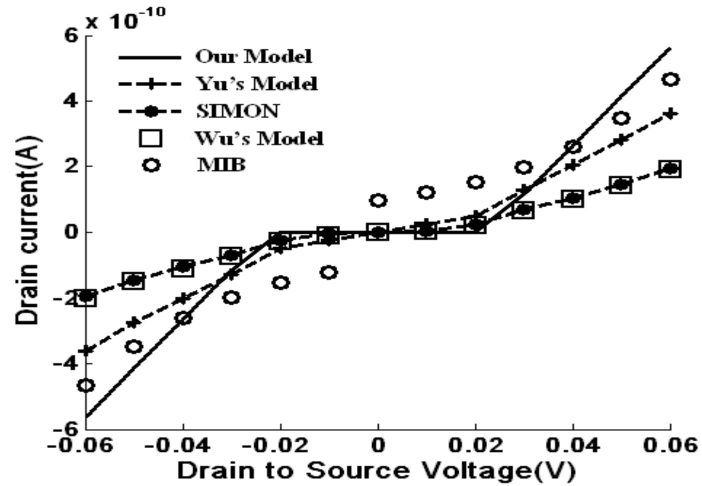

Fig. 3.5 Comparison of the I_{ds}-V_{ds} characteristics for zero gate to source voltage obtained from Yu's model, Wu and Lin's model, SIMON 2.0 and verilog-A model MIB under the condition R_D= R_S =100MΩ, C_{TD}= C_{TS} =1.6 aF, and T=30K. The parameters for our macro model areCF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=300*10^{+6} , CR2=220*10^{+6}. The value of RG is taken as 50*10^{9}Ω.

The Id-Vgs characteristics for different values of Vds is shown in Fig. 3.6. The coulomb oscillation characteristics is efficiently captured by the proposed model. It is observed that with increase in drain to source voltage the peak value of the oscillation characteristics curve increases and the curve look more prominent. So it can be said that the proposed SET gives better result for higher values of Vds compared to lower values. Fig. 3.7 demonstrates the transconductance characteristics of the model. It is a decreasing function of gate to source voltage and for values greater than 0.07V, most of the transconductance values lie between 0 and 10us. Here we have shown positive part of the transconductance characteristics considering positive values of Vgs only, whereas the negatice counter part of the characteristics can also be shown considering negative values of Vgs.

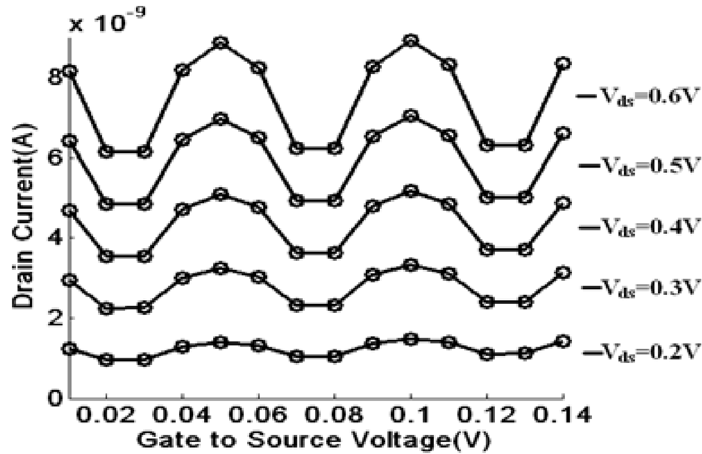

Fig. 3.6 Coulomb oscillation characteristics of the proposed SET for various drain to source voltage.

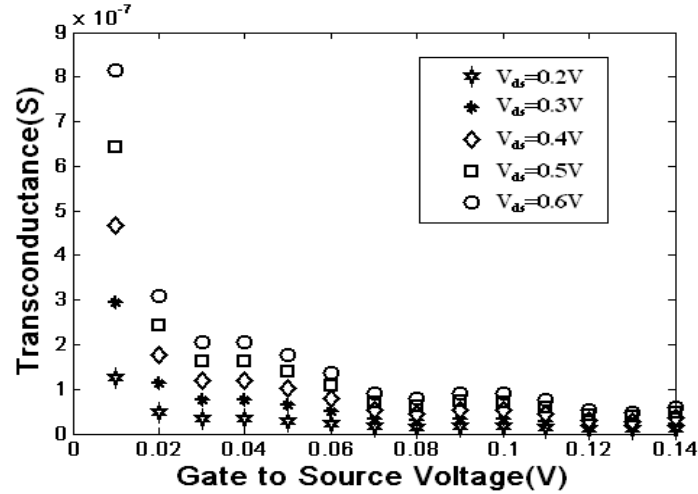

Fig. 3.7 Transconductance characteristics of the proposed macro model. Here V_{ds} has been chosen as the parameter whose values are varied from 0.2V to 0.6V, with an increment of 0.1V.

Table 3.1
Comparison of computational time for different circuits using Monte Carlo based, SPICE macro model and master equation based approach

Logic Circuit (Simulated in a Intel core i3 processor)	No. of devices	Monte Carlo method (Sec)	Master Equation based approach (Sec)	Macro model approach (Sec)
Inverter	2	1.0	3.63	0.9
NAND gate	3	2.0	3.97	1.22
Master-slave JK flipflop	8	3.0	4.3	1.6

Time consumption is the most important parameter which put the macro model approach in the best position compared to the existing approach of simulation of SET. So we have designed various basic logic circuits and compared their simulation time consumption with the

other simulation methodologies. A comparison regarding computational overhead for each simulation approach has been given in Table 3.1. It can be verified that logic circuits designed using our proposed model takes lesser time compared to other approaches.

3.5 Single Electron Inverter

To verify the validity of the proposed model, a single electron inverter is designed as shown in Fig. 3.8. The voltage transfer characteristic of the designed inverter is compared with that obtained from SIMON and Verilog-A [3.16] based MIB model as sown in Fig. 3.9. The simulation parameters used for SIMON and MIB model are R_S=R_D=1MΩ, C_{TD} = C_{TS} =1aF, C_{G1}=3aF and the output load capacitor is C_L=1 aF. The parameters used for our model are CF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=300*10^{+6}, CR2=220*10^{+6} and the value of RG is taken as 50*10^{9}Ω. The static characteristics obtained using our model closely resembles with that of the ideal one. In case of our model the logic '1' and logic '0' values are clearly distinguishable and the gain is greater than unity. The simulation results obtained from MIB model and SIMON are almost same and their output range is between -0.1V and 0.01V which is much lesser compared to our model. In inverter design the value of the load capacitor is taken very large to ensure that each SET can work independently.

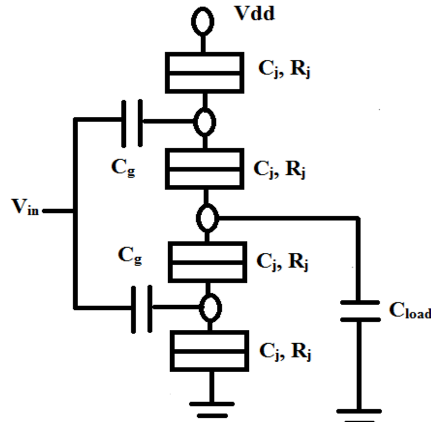

Fig. 3.8 Single electron transistor based inverter Circuit. C_{load} is the output load capacitance, Cj and Rj are tunnel junction capacitance and resistance respectively.

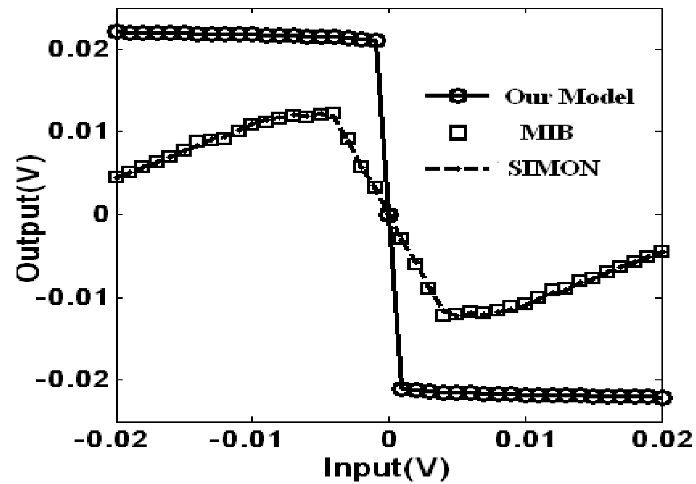

Fig. 3.9 Static chracteristics of an SET inverter cell, as predicted by MIB, SIMON and our model. The SET parameters for SIMON and MIB are R_S=R_D=1MΩ, C_{TD} = C_{TS} =1aF, C_{G1}=3aF, the output load capacitor is C_L=1 aF, and the parameters for our macro model is CF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=300*10^{+6}, CR2=220*10^{+6}. The value of RG is taken as 50*10^{9}Ω.

The transient characteristics of the designed inverter along with the results obtained from MIB model and SIMON is shown in Fig. 3.10. For our model the output pulse is an exact opposite replica of the input pulse and the better performance of our model compared to other approaches can be witnessed observing the figure. So our model shows sufficient accuracy both in static and dynamic regimes. The effect of model parameters on the noise margin of the inverter circuit is thoroughly investigated. We observed that gate resistance RG affects the robustness of SET logic significantly compared to other parameters. The effect of RG on the transfer characteristics of the inverter is shown in Fig. 3.11. With the increase of RG value the characteristic curve moves toward the ideal one and the best result is obtained for RG = 50GΩ. Further increase in RG value does not affect the characteristic curve. Noise margin as a function of RG has been shown in the inset of Fig. 3.11. It can be observed that for all the values of RG, $NM_L = NM_H$, so instead of using the ratio form we have represented it in absolute form. For RG equal to 10GΩ to 20GΩ the noise margin increases rapidly and after that the slope decreases. So the minimum noise margin ($NM_L = NM_H = 0.25$V) is obtained for RG = 10GΩ and the maximum noise margin is obtained ($NM_L = NM_H = 0.286$ V) for RG = 50GΩ.

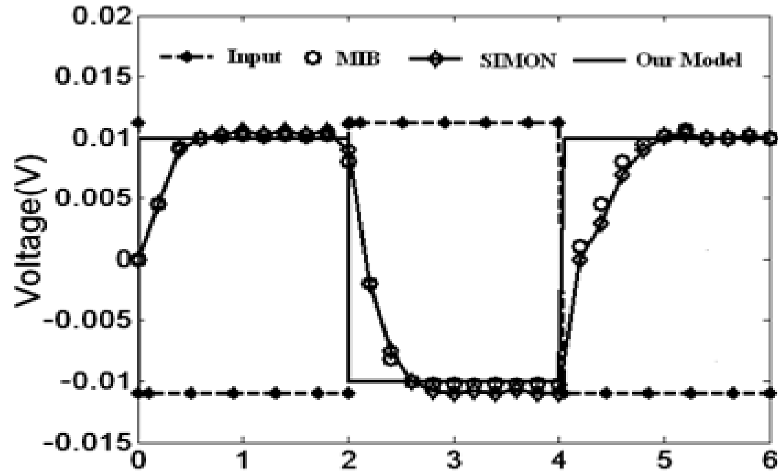

Fig. 3.10 Transient characteristics of an SET inverter cell, as predicted by MIB, SIMON and our model. The SET parameters for SIMON and MIB are R_S=R_D=1MΩ, C_{TD} = C_{TS} =1aF, C_{G1}=3aF, the output load capacitor is C_L=1 aF, and the parameters for our macro model is CF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=300*10^{+6}, CR2=220*10^{+6}. The value of RG is taken as 50*10^{9}Ω.

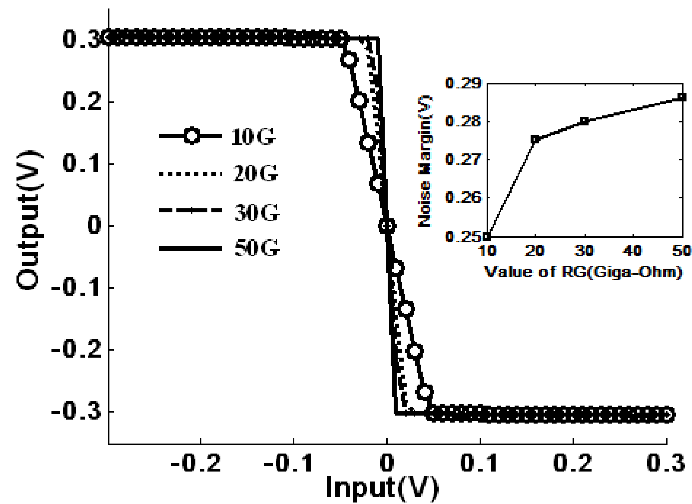

Fig. 3.11 Effect of RG on the static characteristics of the inverter circuit.

3.6 Multiple Peak NDR Circuit

The negative differential resistance (NDR) circuit has a wide range applications such as in analog-to-digital converter [3.17], memory circuit [3.18], logic circuit, oscillators and cellular neural network [19, 20]. The first SET based NDR circuit was proposed by Heji et al [3.21]. Later Mahapatra et al proposed a architecture with improved dynamic range of NDR region [3.19]. Multiple peak NDR circuit has been used in multiple valued logic circuits , frequency synthesizer [3.22] and in multiple valued memory circuits [3.23]-[3.25] due to its capability of ultra high speed and reducing circuit complexity. A SET-MOS hybrid multiple peak NDR circuit has been proposed by Inokawa et al. but till now nothing has been reported in the literature on SET based multiple peak NDR circuit. In this work we have designed a multiple peak NDR circuit based on SET as shown in Fig. 3.12. The transistor T1 is biased using current source IBias. Here a feedback loop is created by T1 which controls the current Iin flowing through T2. The I-V characteristics of the multipeak NDR circuit is shown in Fig. 3.13, considering bias current as a parameter. It is clearly seen that the input current is increasing with increase in input voltage showing a negative differential characteristics. We further investigated the effect of other parameters on the characteristics of NDR cell. The parameter CR2 affects the peak value for different NDR regions whereas CR1 helps in

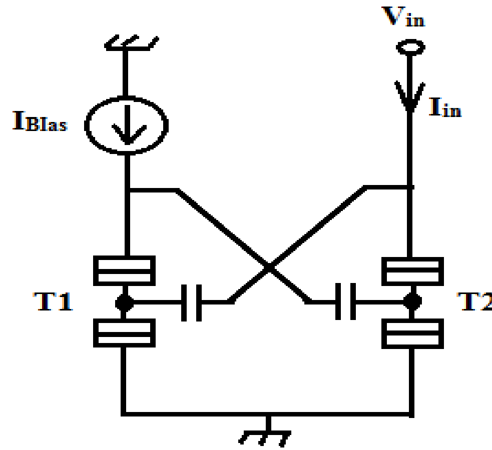

Fig. 3.12 Schematic diagram of the multi peak NDR circuit with two cross coupled single electron transistors and one current source used for biasing the transistor T1. The parameter values used are CF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=300*10^{+6}, CR2=220*10^{+6} (for T1) and CR1=300*10^{+6}, CR2=220*10^{+6} (for T2), The value of RG is taken as 10*10^{6}Ω.

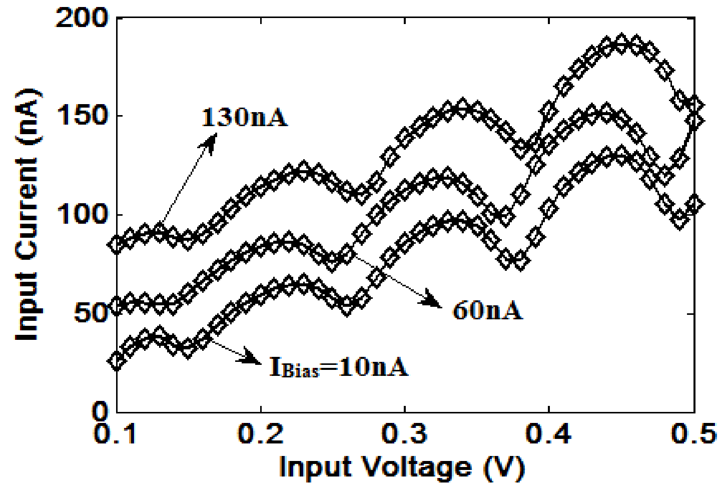

Fig. 3.13 Characteristics of the designed multi peak NDR circuit for different bias current simulated in SPICE environment. The parameter values used are CF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=420*10^{+6}, CR2=5*10^{+6} (for T1) and CR1=330*10^{+6}, CR2=330*10^{+6} (for T2), the value of RG is taken as 10*10^{6}Ω.

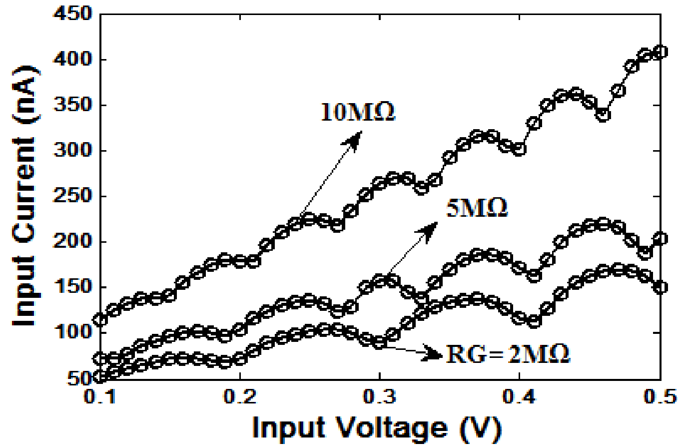

Fig. 3.14 Effect of Rg on the characteristics of the multi peak NDR circuit. The parameter values used are CF1=40, C_{VP}=0.02, CI2=0.2*10^{-9}, CR1=420*10^{+6}, CR2=5*10^{+6} (for T1) and CR1=330*10^{+6}, CR2=330*10^{+6} (for T2). The value of the bias current is 60nA.

increasing the NDR regions. among all the parameters RG affect the circuit most. It controls the number of NDR regions for a fixed range of input voltage. As the value of RG increases the number of NDR regions also increases as depicted in Fig. 3.14.

3.7 Integrator

We have also designed an integrator circuit to validate the versatility of the proposed macro model [3.26]. The designed two SET based integrator circuit is shown in Fig. 3.15. The transistor T1 is biased using voltage Vdd and T2 is biased using Vgs. The positive terminal of incremental input voltage Vin is connected to gate terminal of T1 and drain terminal of T2. Therefore the transistor T2 works as a pass transistor in this circuit. Finally the output is taken across the load

capacitor C_L. The transient characteristic of the designed integrator circuit is depicted in Fig. 3.16. The input is a sine waveform and the corresponding output is a cosine waveform which proves that the designed integrator circuit is working efficiently. We further analysed the linearity of the designed integrator circuit by analysing the harmonic and intermodulation distortion [3.27]. In SPICE simulator the harmonic distortion analysis is performed using '.four' command. The command instructs the simulator to perform a harmonic decomposition by calculating the fourier coefficients of the input waveform and finally calculates the total harmonic distortion (THD) [3.28]. Harmonic distortion analysis is performed considering the fundamental frequency as 10KHz and number of hermonics as nine. The harmonic distortion is plotted in Fig. 3.17, where the power is normalized into dBm. The maximum power of -15.95 dBm is obtained for the fundamental frequency. For other frequencies the power obtained is around -200 dBm whch is much lower comparerd to the fundamental frequency. Finally the total harmonic distortion is calculated as 2.94% which proves that the dsigned integrator circuit is highly immune to harmonic distortion. Intermodulation distortion is another important parameter to analyse the linearity of the circuit. SPICE doesn't provide any direct command to analyse the intermodulation distortion. So the intermodulation is analysed using total difference frequency distortion (TDFD) test [3.29]. The TDFD test

uses the same .four command but here all frequencies of interest have to be the multiple of fundamental frequency or the fundamental frequency is chosen as the submultiple of stimulating frequencies [3.30]. In TDFD analysis we perform a two tone test where fundamental frequency is 2KHz and stimulating frequencies are 8KHz and 10KHz. The output of this analysis is depicted in Fig. 3.18. It can be observed from the figure that the power of the stimulating frequencies are much higher compared to the second order and third order intermodulation frequencies of 2 KHz and 12 KHz respectively. Finally the intermodulation distortion is estimated as 1%. So it can be concluded that the design integrator circuit is highly linear and shows sufficient immunity to the harmonic and intermodulation components.

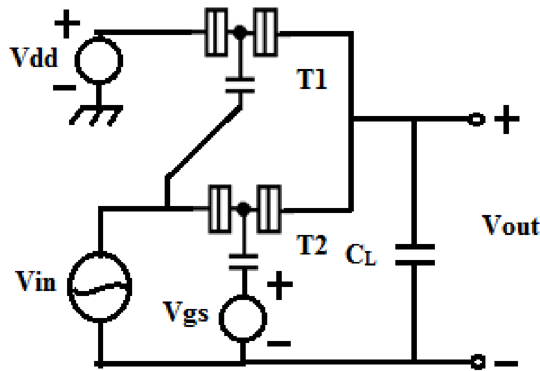

Fig. 3.15 Schematic diagram of the integrator circuit. The parameter values used are CF1=40, C_{VP}=0.02, CI2=$0.25*10^{-9}$, CR1=$420*10^{+6}$, CR2=$5*10^{+6}$, CR3=0.29e-5 (for T1) and CI2=$0.15*10^{-9}$, CR1=$330*10^{+6}$, CR2=$3*10^{+6}$, CR3=0.7e-7 (for T2), the value of RG is taken as $2*10^{6}\Omega$.

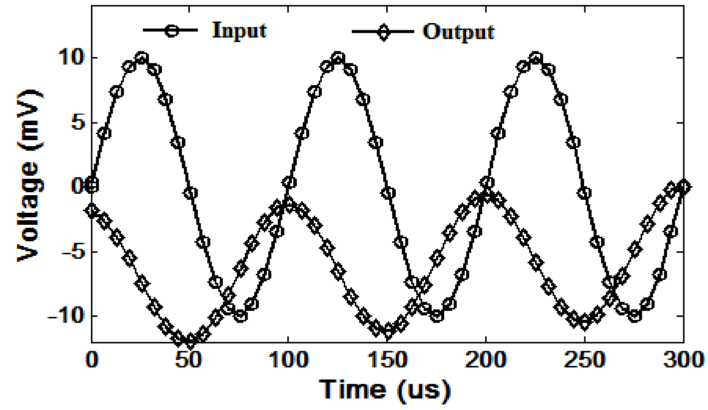

Fig. 3. 16 Transient characteristics of the designed integrator circuit.

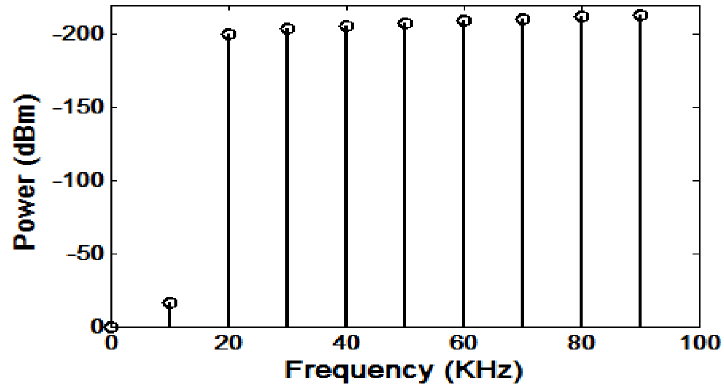

Fig. 3. 17 Plot of the harmonic distortion of the designed circuit.

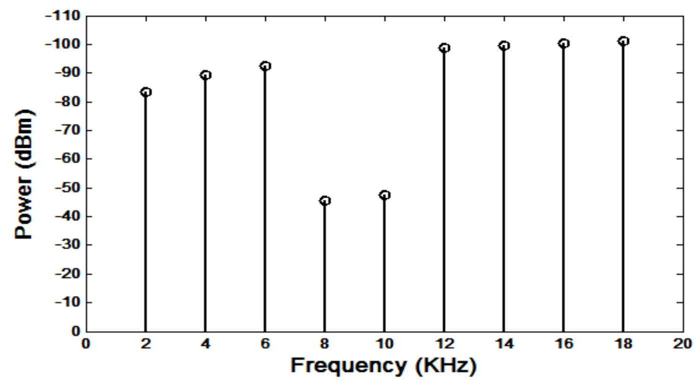

Fig. 3. 18 Plot of the intermodulation distortion of the designed circuit.

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Chapter 4

Compact Analytical Model of Single Electron Transistor

4.1 Introduction

Scalling of MOS devices faces limitations in the nanometer region due to different short channel effects. A Significant research has been carried out in the last decade to mitigate these effects in the material level as well as considering different device structures. But it is a fact that moore's law cannot continue forever and the downscaling of MOS devices are about to reach its physical limits. So researchers around the globe had started to look for new nano sized devices which will take care of the future of nanotechnology. Single electron tunnelling technology (SETT) is one of the most promising candidate for future VLSI/ULSI design because of its nano-scale size, ultra low power dissipation and unique characteristics of coulomb blockade oscillation [4.1]-[4.6]. But single electron transistor suffers from some serious drawbacks, which are low gain, high output impedance, very low temperature operation and background charge problem [4.7]-[4.10]. On the other hand MOS devices are very good in voltage gain and high speed driving which can compensate the intrinsic drawbacks of single

electron transistor. So it is very likely that in near future rather than replacing the CMOS technology by a new technology, a combination of both will give us a good solution[4.11, 4.12]. So by combining MOS with SET, a hybrid technology will evolve which will have new properties and functionalities in its bucket. Most of the analytical models reported in the literature considered few numbers of electron in the island to keep the model simple but it definitely limits the accuracy of these models. These models are good for SET based circuits only where the biasing voltage is very low. But the MOS transistors are generally biased at relatively higher voltage compared to SET [4.13]. So for SET-MOS hybrid circuits the value of Vds for SET will be higher than that used in case of SET based circuits, which creates a necessity of developing a new analytical model of SET that considers higher number of island states to accommodate large values of Vds.

In this work, a new compact analytical model has been proposed which considers eleven island states. The proposed model can accommodate the drain to source voltage of as large as 6e/Csum. Our model can efficiently express the characteristics of symmetric and asymmetric SET for wide range of temperatures and voltages. The proposed model is developed in the Verilog-A language [4.22] and can be implemented in any SPICE environment. To prove the validity of the model,the results are compared with those obtained from the monte carlo based simulator SIMON [4.23]. Also the effect of

temperature on the device characteristics is thoroughly investigated. Finally the model is applied to implement the SET-MOS hybrid inverter and NAND gates.

4.2 Literature Review

The first compact analytical model of SET was proposed by Uchida et al [4.14]. The model showed sufficient accuracy even at very high temperature. But this model doesn't consider the background charge effect and also not applicable for muti-gate and asymmetric SET. Innokawa and Takahashi [4.15] extended the model proposed by Uchida et al to asymmetric cases. But their model also lacks the practicality due to the ignorance of the background charge effect. Lee et al for the first time proposed a practical model of single electron transistor [4.16]. This model was developed in relation to the fabricated SET proposed by Kim et al [4.17]. So the model proposed by Lee at al provides the realistic parameters of SET. The MIB model [4.18] proposed by Mahapatra et al can be used for multi-gate as well as asymmetric deices. This model considers only four number of island states (-1, 0, 1, 2), which limits the range of drain to source voltage to 3e/Csum. this voltage range is sufficient for usual operation of SET. But as the temperature increases the probability of involving higher charge states increases [4.19] which in turn increases the drain voltage and the above voltage range becomes insufficient for hybrid SET-MOS circuit

operation. Also the model proposed by Mahapatra et al considers only the unidirectional electron flow and it doesn't show the staircase like characteristics for asymmetric SET. Lientschnig et al proposed [4.20] a model which considers a large number of island states but not suitable for asymmetric SET. Hasaneen et al proposed an approach [4.21] to calculate the most probable island states by using the master equation approach and the recursion method. They included the most probable island states in their model to improve the accuracy of the model. But this model also doesn't provide good results for asymmetric SET. So far most of the models [4.15, 4.18] have considered only four states and they have shown good results either for symmetric SET or Asymmetric SET.

4.3 The Model

schematic diagram of the single electron transistor is shown in Fig. 4.1. It consists of one island sandwitched between two tunnel junctions and two gates coupled to the island. The analytical model is derived based on orthodox theory and master equation method. The proposed model has been derived following three important steps:

- Calculation of the change in electrostatic energy.
- Then, calculation of the tunnelling rates across the two junctions.
- Finally the calculation of the I-V characteristics of the SET.

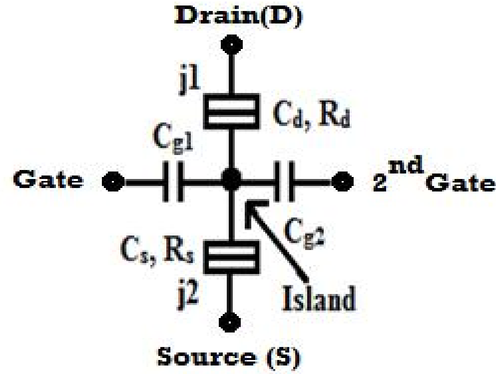

Fig. 4.1 Schematic diagram of SET

To derive the proposed model we need to make some assumptions:

- The drain and source terminal are connected to a large reservoir whose capacitance is much larger than the total equivalent capacitance of the island. This ensures that SET characteristics depends only on the nodal voltages, which ensures quasi steady state condition to enable transient analysis.
- To ensure suppression of electron tunnelling by quantum fluctuation The junction resistance is kept much larger than the quantum resistance [4.24].
- The co-tunneling is neglected.
- The quantum energy is assumed to be continuous.

4.3.1 Calculation of Change in Electrostatic Energy

To calculate the change in electrostatic energy we followed the approach proposed by Ingold and Nazarov [4.25]. The circuit diagram

of a double junction SET, biased with a supply voltage V is shown in Fig. 4.2, the capacitances associated with the island are shown in Fig. 4.3. Now the change in electrostatic energy is calculated for an electron tunnels on or off the island. By observing Fig. 4.3 the island charge –ne can be derived as

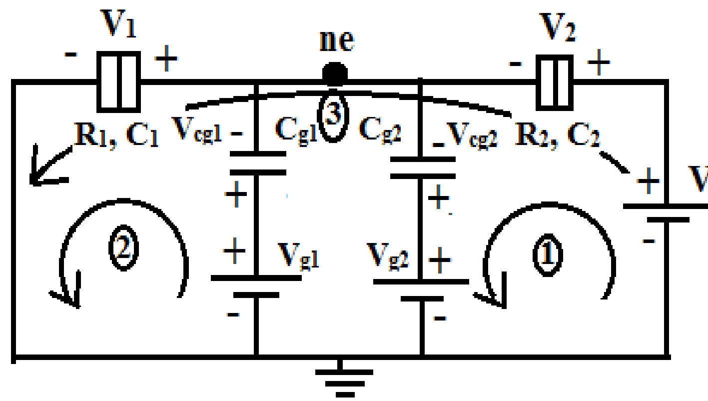

Fig. 4.2 Circuit diagram a Single Electron Transistor with a supply voltage V.

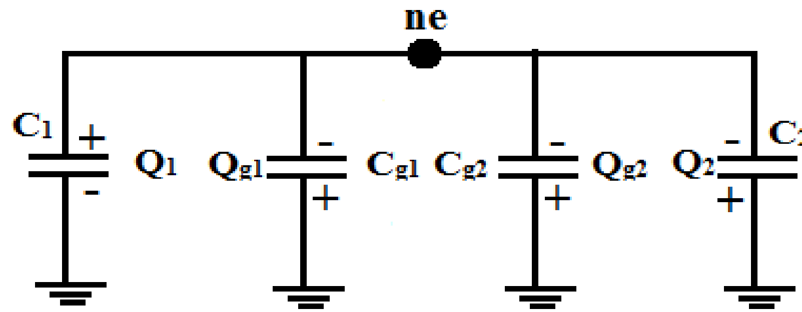

Fig. 4.3 Capacitance C1, Cg1, Cg2 and C2 looking from the island.

$$-ne = Q_2 + Q_{g_1} + Q_{g_2} - Q_1 \tag{4.1}$$

Applying Kirchhof's voltage law to the loops shown in the Fig. 4.2 we get,

Loop 1:

$$V + \frac{Q_{g2}}{C_{g2}} = \frac{Q_2}{C_2} + V_{g2} \quad (4.2)$$

Loop 2:

$$V_{g1} = \frac{Q_1}{C_1} + \frac{Q_{g1}}{C_{g1}} \quad (4.3)$$

Loop 3:

$$V = \frac{Q_1}{C_1} + \frac{Q_2}{C_2} \quad (4.4)$$

By solving the eqs. (4.1)-(4.4), we can the expressions for Q1, Q2, Qg1 and Qg2 in terms of ne, V, Vg and Vg2

$$Q_1 = \frac{C_1}{C_\Sigma}(ne + VC_2 + V_{g1}C_{g1} + V_{g2}C_{g2}) \quad (4.5)$$

$$Q_2 = \frac{C_2}{C_\Sigma}\left\{V(C_1 + C_{g1} + C_{g2}) - (ne + V_{g1}C_{g1} + V_{g2}C_{g2})\right\} \quad (4.6)$$

$$Q_{g1} = \frac{C_{g1}}{C_\Sigma}\left\{V_g(C_1 + C_2 + C_{g2}) - (ne + VC_2 + V_{g2}C_{g2})\right\} \quad (4.7)$$

$$Q_{g2} = \frac{C_{g2}}{C_\Sigma}\left\{V_{g2}(C_1 + C_2 + C_{g1}) - (ne + VC_2 + V_{g1}C_{g1})\right\} \quad (4.8)$$

Where $C_\Sigma = C_1 + C_2 + C_{g1} + C_{g2}$

Now we consider one electron is tunnelling onto the island from left hand side to the right hand side, thereby changing the island charge from –ne to –(n+1)e. The corresponding change in the other charges are calculated as

$$\Delta Q_1 = e\frac{C_1}{C_\Sigma}; \Delta Q_2 = -e\frac{C_2}{C_\Sigma};\ \Delta Q_{g_1} = -e\frac{C_{g1}}{C_\Sigma};\ \Delta Q_{g2} = -e\frac{C_{g2}}{C_\Sigma};$$

Where ΔQ_1, ΔQ_2, ΔQ_{g1} and ΔQ_{g2} reperesents the charges on C1, C2, Cg1, and Cg2 respectively.As one electron is transferred across C1 the change in charge across C1 is calculated as ΔQ_1+e.

The change in the electrostatic energy of the overall circuit for an electron tunnelling onto the island across tunnel junction 1, can be calculated as

$\Delta E_{1,add} = E_{final} - E_{initial}$ + Work done by the voltage source

$$\Rightarrow \Delta E_{1,add} = \frac{e}{C_\Sigma}\left\{ne + \frac{e}{2} - V_g C_{g1} - V_{g2}C_{g2} - VC_2\right\} \tag{4.9}$$

Similarly, the change in the electrostatic energy for an elcton tunnling of the island across tunnel junction 1 can be obtained as

$$\Delta E_{1,sub} = \frac{e}{C_\Sigma}\left\{-ne + \frac{e}{2} + V_g C_{g1} + V_{g2}C_{g2} + VC_2\right\} \tag{4.10}$$

This procedure of calculating the electrostatic energy can be applied for events across tunnel junction 2 and the corresponding expressions are given as

$$\Delta E_{2,add} = \frac{e}{C_\Sigma}\left\{ne + \frac{e}{2} - V_g C_{g1} - V_{g2}C_{g2} + V(C_\Sigma - C_2)\right\} \tag{4.11}$$

$$\Delta E_{2,sub} = \frac{e}{C_\Sigma}\left\{-ne + \frac{e}{2} + V_g C_{g1} + V_{g2}C_{g2} + V(C_2 - C_\Sigma\right\} \tag{4.12}$$

4.3.2 Tunneling rates across tunnel junctions

The tunnelling rates across the tunnel junctions is calculated as [4.24]

$$\Gamma = \frac{1}{e^2 R_j} \times \frac{-\Delta E}{1 - \exp(\Delta E / k_B T)} \tag{4.13}$$

Here Rj is the tunnel junction resistance and Δ E is the corresponding change in the electrostatic energy when an electron tunnels on or off the island. Depending on the direction and the tunnel junction of the electron flow any of the four expressions (4.9)-(4.12) can be used to calculate the respective tunnel rate. So we will get four tunnelling rates namely R1L(tunnelling left through tunnel junction 1), R2L (tunnelling left through tunnel junction 2), R1R (tunnelling right through tunnel junction 1) and R2R (tunnelling right through tunnel junction 2).

4.4 Calculation of V-I Characteristics

The maximum applicable voltage depends on the number of charge states of the island. Depending on the supply and input voltage, there is a probability of occupancy for each island state. The charge state with highest probability of occupancy is an important parameter for calculating the drain current of SET and it is estimated as [4.20]

$$n_{opt} = floor\left[-\left(\frac{C_2 V + C_{g1} V_{g1} + C_{g2} V_{g2} + Q_0}{e} \right) + \frac{C_\Sigma}{e} \frac{V R_1}{R_1 + R_2} \right] \tag{4.14}$$

Here the function “floor” estimates the value in the brackets to its nearest integer value. Q0 represents the background chare value. We Consider the value of V, Vg1, C2, Cg1, Cg2, R1 and R2 as 0.6V, 0.6V, 2.7aF, 1aF, 1aF, 1MΩ, 1MΩ respectively. The value of n_{opt} is calculated

as 0, if we ignore the background charge effect. But to make the model more realistic the background charge effect has been considered in the model and the value of Q0 is taken as 0.2e [4.26]. After considering the background charge effect the value of nopt is obtained as -1. We have considered eleven charging state for the proposd model which can be chosen either by considering the most probable states [4.21], or by taking five states on either side of the n_{opt} value. Though both the approaches gave same result yet the second approach is simpler and symmetric. The general recursion relation [4.27] is used to calculate the probability distribution function. The probability value for island states opt+1 is calculated as

$$PN_{opt+1} = \frac{R1R_{opt} + R2L_{opt}}{R1L_{opt+1} + R2R_{opt+1}} \tag{4.15}$$

The probability value for other charge states occupying the positive side of n_{opt} value is expressed as

$$PN_{opt+i} = PN_{opt+i-1} \frac{R1R_{opt+i-1} + R2L_{opt+i-1}}{R1L_{opt+i} + R2R_{opt+i}} \quad \text{for i=2,3,4,5} \tag{4.16}$$

Now the value with island states opt-1 is calculated as

$$PN_{opt-1} = \frac{R1L_{opt} + R2R_{opt}}{R1R_{opt-1} + R2L_{opt-1}} \tag{4.17}$$

The probability value for charge states occupying the negative side of n_{opt} value is expressed as

$$PN_{opt-i} = PN_{opt-i+1} \frac{R1L_{opt-i+1} + R2R_{opt-i+1}}{R1R_{opt-i} + R2L_{opt-i}} \quad \text{for i=2,3,4,5} \tag{4.18}$$

The value of P_{sum} is calculated as

$$P_{sum} = \sum_{i=1}^{5} P_{opt+i} + \sum_{i=-1}^{-5} P_{opt-i} + 1 \tag{4.19}$$

Finally the drain current is calculated as

$$I = \frac{e}{P_{sum}} \sum_{i=-5}^{5} PN_{opt+i} \left(R1R_{opt+i} - R1L_{opt-i} \right)$$

$$\Rightarrow \frac{e}{P_{sum}} \begin{bmatrix} PN_{opt+1}\left(R1R_{opt+1} - R1L_{opt+1}\right) + PN_{opt+2}\left(R1R_{opt+2} - R1L_{opt+2}\right) + \\ PN_{opt+3}\left(R1R_{opt+3} - R1L_{opt+3}\right) + PN_{opt+4}\left(R1R_{opt+4} - R1L_{opt+4}\right) + \\ PN_{opt+5}\left(R1R_{opt+5} - R1L_{opt+5}\right) + \left(R1R_{opt} - R1L_{opt}\right) + \\ PN_{opt-1}\left(R1R_{opt-1} - R1L_{opt-1}\right) + PN_{opt-2}\left(R1R_{opt-2} - R1L_{opt-2}\right) + \\ PN_{opt-3}\left(R1R_{opt-3} - R1L_{opt-3}\right) + PN_{opt-4}\left(R1R_{opt-4} - R1L_{opt-4}\right) + \\ PN_{opt-5}\left(R1R_{opt-5} - R1L_{opt-5}\right) \end{bmatrix} \tag{4.20}$$

4.5 Simulation Results

The proposed analytical model of SET is written in hardware description language, Verilog-A. This model is then incorporated in SPICE environment through Verilog-A interface. The V-I characteristics of the symmetric SET are simulated over a wide range of temperature and bias voltage. The I-V characteristics of the symmetric SET has been shown in Fig. 4.4 as a function of Vgs. The coulomb

blockade characteristics can be clearly observed in the shown figure. Fig. 4.4 also shows the comparison between the simulation results and the results obtained from the Monte Carlo simulator SIMON.

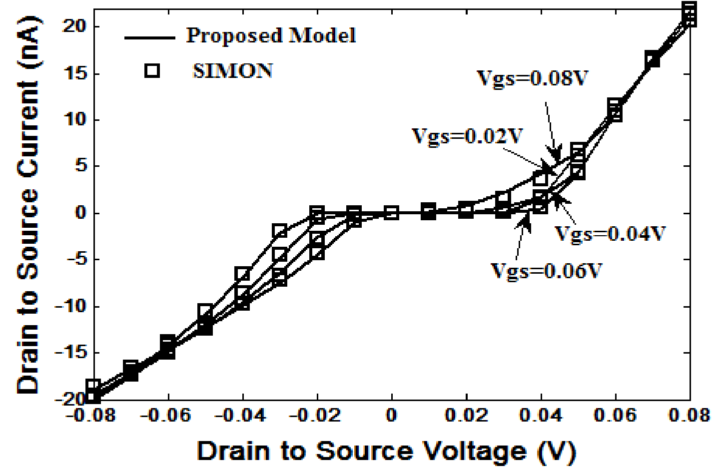

Fig. 4.4 I_d-V_{ds} characteristics for symmetric SET (R_d=R_s=1MΩ, C_d=C_s=1aF, C_{g1}=1aF, C_{g2}=2aF and T=15K)

Temperature is a great factor for a stable operation of single electron transistor. If the thermal energy of the system becomes greater than the charging energy, the coulomb blockade vanishes and the electrons starts to tunnel through the junctions. The I-V characteristics of the proposed SET for different temperatures is shown in Fig. 4.5. To prove the accuracy of the proposed model the result obtained from the proposed model is compared with that of another analytical model [4.20]. It can be observed that for very low temperature of 4.2K the coulomb blockade region clearly exists. As the temperature increases the coulomb blockade region gradually vanishes. For higher

temperatures (77K and 300K) the coulomb blockade region completely vanishes.

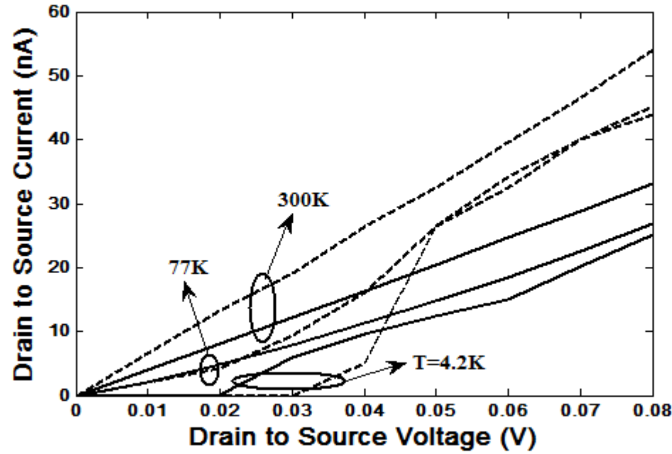

Fig. 4.5 I_d-V_{ds} characteristics for symmetric SET as a function of temperature (R_d=R_s=1MΩ, Cd=C_s=1aF, C_{g1}=1aF and C_{g2}=2aF)

The I-V characteristics for asymmetric SET is demonstrated in Fig. 4.6. The I-V characteristics of the asymmetric SET is analyzed for three different ratios of the tunnel junction resistance. The staircase characteristics of the asymmetric SET can be clearly observed in Fig. 4.6. With increase in the junction resistance mismatch ratio the staircase property becomes more prominent but at the cost of reduced drain to source current. As the tunneling rate depends on the junction resistance so as the mismatch ratio increases the higher junction resistance reduces the tunneling rate which finally dominates the drain to source current.

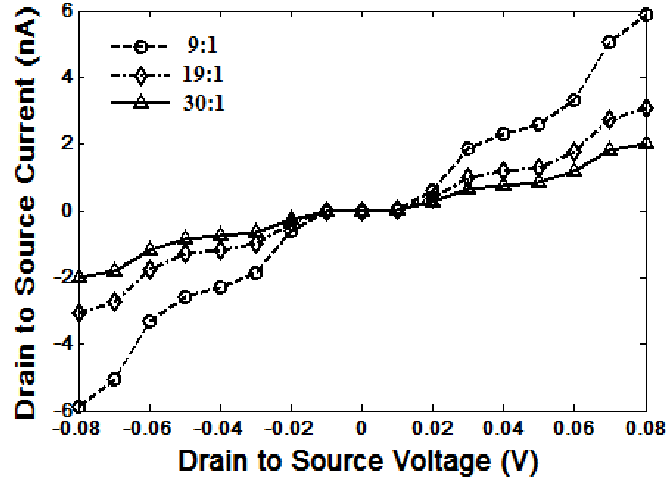

Fig. 4.6 Coulomb staircase (Id-Vds) characteristics for Asymmetric SET considering different tunnel junction ratios (R_d=R_s=1MΩ, C_d=C_s=1aF, C_{g1}=1aF, C_{g2}=2aF and T=15K).

The Id-Vgs characteristics for a symmetric SET considering drain to source voltage as a parameter is shown in Fig. 4.7. Here the empty square box represents the Monte Carlo simulation and the solid line represents the proposed model. The proposed model efficiently captures the coulomb oscillation characteristics. Also a good agreement is observed between the proposed analytical model and reference Monte Carlo simulator SIMON over the entire range of drain to source voltages. The I-V characteristics for an asymmetric SET is also being analyzed using the proposed model. The Id-Vgs characteristics for an asymmetric SET is shown in Fig. 4.8, where the source and drain tunnel junction resistance ratio is considered as 12:1. Like staircase property in

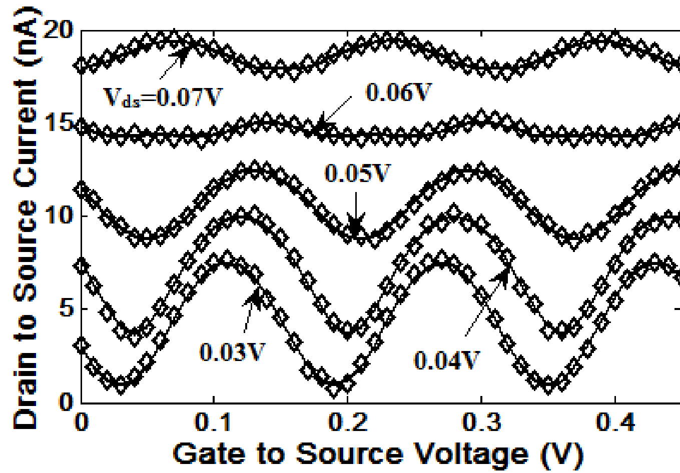

Fig. 4.7 The I_d-V_{gs} characteristics for symmetric SET(R_d=R_s=1MΩ, C_d=C_s=1aF, C_{g1}=1aF, C_{g2}=2aF and T=15K). In the figure, □ represents the Monte Carlo simulation (SIMON) and the solid line represents the proposed model.

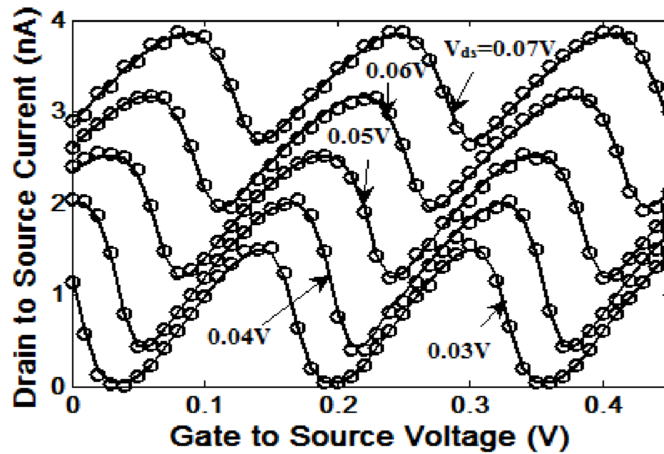

Fig. 4.8 The I_d-V_{gs} characteristics for Asymmetric SET (R_d=R_s=1MΩ, C_d=C_s=1aF, C_{g1}=1aF, C_{g2}=2aF and T=15K). In the figure, o represents the Monte Carlo simulation (SIMON) and the solid line represents the proposed model.

case of Id-Vds characteristics, there is no distinguishable part in the Id-vgs characteristics for an asymmetric SET only plots for the later is a bit

tilted compared to the symmetric counterpart. Also unlike symmetric SET no discrepancy is located in the coulomb oscillation characteristics for different drain to source voltage.

4.6 Accuracy of the proposed model

We further investigated the accuracy of the proposed model considering different number of island states and different values of n_{opt} value. Different level numbers has been assigned to the model depending on the number of states considered. Total four levels has been considered to analyze the accuracy of the model. Level 1considers 10 states with highest probability of occupancy [4.21]. Level 2 considers 11 states as 5 states on both side of the n_{opt} value. Level 3 considers 7 states as 3 states on both side of the n_{opt} value and in the same way level 4 with 3states has been considered. Regarding n_{opt} value, we have considered total three values as 0, 1 and -1 to test the accuracy. For each n_{opt} value all the four levels have been considered and the simulation results are checked. When n_{opt}=1, simulation results for levels 1 and 2 are satisfactory. for n_{opt}= 0, starting from level 1 up to level 3 the results are satisfactory. with the value of nopt= -1, all the considered levels give satisfactory results.

Now the level is kept fixed and for each considered level the whole range of n_{opt} is investigated and the following results are obtained:

- For level 1, the range of n_{opt} is $-5 \leq n_{opt} \leq 3$
- For level 2, the range of n_{opt} is completely same as above
- For level 3 the range of n_{opt} is $-3 \leq n_{opt} \leq 1$
- Lastly for level 4, only two values of n_{opt} (-1 and 0) are seen to work satisfactorily

It is observed that levels 1 and 2 gave maximum coverage for n_{opt} values with both giving the same result. As both gave the same results it can be concluded that for single electron transistor the symmetric consideration in choosing the states gave the same result as that of the best 10 states. Now combining the above discussed analysis finally it can also be concluded that level 1 and nopt= -1 will provide the best simulation results.

4.7 SET-MOS hybrid circuits and applications

The main goal of proposing this model is to be able to simulate SET-MOS hybrid circuits. We successfully implemented the co-simulation of SET and MOSFET by incorporating the proposed model in SPICE environment through its Verilog-A interface. Verilog-A is the analog platform of the hardware description language by which SPICE device models and verilog-A modules can be mixed in the same netlist. In the verilog-A module SET is defined as a four terminal device comprising of voltage controlled current sources and controlled by two gate

terminals. The parameter values of SET used for simulation are given as Rd=Rs=1MΩ, Cd=Cs=1aF, C_{g1}=1aF, C_{g2}=2aF, Vdd= 0.5V, Cout=2aF and T=15K. We have used 65nm technology for MOSFET (BSIM). The corresponding parameter value for MOSFET is w=150nm. We have applied the proposed model to simulate different hybrid SET-MOS circuits as discussed below.

4.7.1 Inverter circuit

An inverter is a logic gate that coverts a low input signal to a high output signal and vice versa. A circuit diagram of a hybrid inverter consists of a SET and MOSFET is shown in the inset of Fig. 4.9. As a design strategy the value of the load capacitance is kept high to suppress the single electron tunneling effect on the output node. The voltage transfer characteristic of the designed hybrid inverter is shown in Fig. 4.9. The figure also shows the comparison between the proposed model and SIMON. As SIMON is a simulator for single electron devices we cannot simulate hybrid SET-MOS devices directly in this simulator. So a different approach ,whch will be explained later, has been used for this purpose. Here as a replacement of CMOS logic Pseudo NMOS logic is used and the MOSFETs are replaced with an equivalent ON resistance. Then the hybrid SET-MOS circuit is successfully simulated in SIMON. It can be observed from Fig. 4.9 that

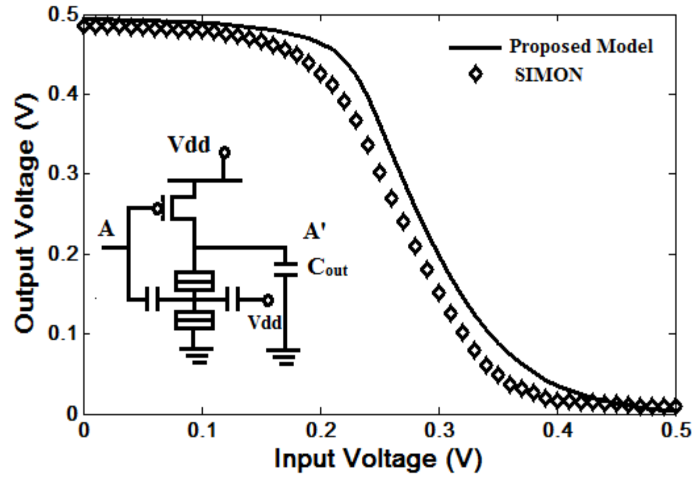

Fig. 4.9 Static characteristics of the designed inverter cell. The parameter values are Rd=Rs=1MΩ, Cd=Cs=1aF, C_{g1}=1aF, C_{g2}=2aF, Vdd= 0.5V, Cout=2aF and T=15K for SET and L=65nm W=150nm for MOSFET. The solid line represents the results of the proposed model and the symbols represent the results of the reference simulator.

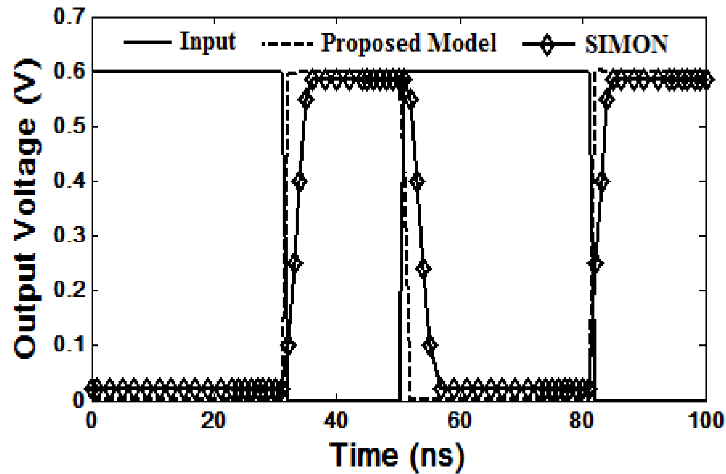

Fig. 4.10 Dynamic characteristics of the designed SET-MOS hybrid inverter cell. The SET parameters are Rd=Rs=1MΩ , Cd=Cs=1aF, C_{g1}=1aF, C_{g2}=2aF, Vdd= 0.5V, Cout=2aF and T=15K for SET and L=65nm W=100nm for MOSFET.

the simulations result of the proposed model agrees with that of the Monte Carlo simulations. The transient response of the designed hybrid inverter is shown in Fig. 4.10. The output waveform is an exact opposite replica of the input waveform. The proposed model also performs better than SIMON in this respect. So a overall good agreement with the Monte Carlo simulations proves the accuracy of the proposed model in both static and dynamic regimes.

4.7.2 NAND gate

A two input SET-MOS hybrid circuit is shown in Fig. 4.11. The pull-up network is constructed using MOSFETs and the pull-down network is formed using SETs. The transient characteristics of the designed NAND gate is demonstrated in Fig. 4.12. It is observed that the designed hybrid NAND gate works satisfactorily and shows good agreement with the Monte Carlo simulations. The proposed analytical model performed very well when applied for hybrid inverter and NAND gate, which demonstrates the validity of the proposed model for simulation of hybrid SET-MOS circuit using a general circuit simulator package such as SPICE.

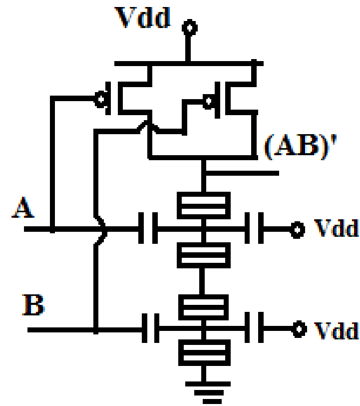

Fig. 4.11 Schematic circuit of the Hybrid SET-MOS two input NAND gate

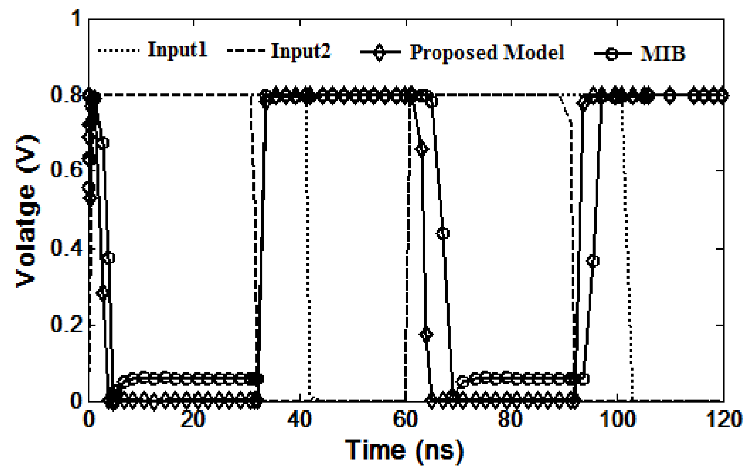

Fig. 4.12 Input and output waveforms simulated in SPICE environment (Rd=Rs=1MΩ , Cd=Cs=1aF, C_{g1}=1aF, C_{g2}=2aF, Vdd= 0.5V, Cout=2aF and T=15K for SET and L=65nm W=150nm for MOSFET).

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Chapter 5

Delay Analysis of Single Electronics Circuits

5.1 Introduction

Being a novel technology it's been a challenge for researchers to develop a proper simulation environment for single electronics circuits. The simulation software SIMON has been used extensively to simulate single electron devices [5.1]-[5.4]. Few analytical models have also been used to simulate circuits in SPICE environment. Due to lower gain single electron devices are mostly used in digital applications [5.5]-[5.8]. So the delay analysis is very much required for proper designing of practical integrated circuits. Electron transport phenomena in single electron devices are stochastic in nature, which implies that we need to include a probability distribution process in our analysis. Among all the popular distribution process the poison distribution process predicts the characteristics very well [5.9]. As we are using poisson process so we need to keep in mind some assumptions

1) The tunneling events are independent of each other.
2) The tunneling rates are independent of time.

3) Electron tunneling is a rare event.

5.2 Literature Review

The logic transition for threshold logic based gates is very simple as it depends on single tunnel event. The delay model for single electron threshold logic gates are already there in the literature [5.10]. But single electron transistor based circuits which covers the majority of single electronics involves multiple tunneling event. Still there is no established delay model for multiple tunneling events. Recently a research work was proposed where the delay is calculated based on some estimation methods [5.11]. These estimation methods estimates equivalent tunnel rates based on some assumptions and does not provide accurate result. These results deviate largely from the result obtained from Monte Carlo approach. Also these methods uses a fixed value of error probability which is actually probabilistic in nature. Monte Carlo method also uses the error probability value but it estimates this value through a random generator which works based on algorithms and also repeats itself for every tunneling event. But its not a good practice to uses error probability value for analytical models. So, we proposed a delay model which is independent of error probability value. Other than the assumptions already made regarding the poisson process there are a few more assumption which needs to be keep in mind,

1) The effect of temperature is neglected.
2) The quantum resistance [5.12] is considered to be high enough to ignore the co-tunneling events.
3) The tunneling time through a junction is negligible compared to the time interval between tunneling events.
4) The input signals are ideal with zero rise and fall time.

5.3 Delay Model for constant Tunneling Rate

The probability of K number of electrons tunneling in time interval t can be denoted as P (k, t). In a Poisson process the number of tunneling in disjoint time intervals are independent. Now consider a small interval δ, where maximum one electron can tunnel in this time, the probability mass function for electron tunneling is expressed as [5.13]

$$P(k,\delta) = \begin{cases} 1-\Gamma\delta & if \;\; k=0 \\ \Gamma\delta & if \;\; k=1 \\ 0 & if \;\; k>1 \end{cases} \tag{5.1}$$

The expected value of the number of electron tunneling for the interval δ can be calculated using (5.1) as

E [no. of tunneling in interval [0, δ]] = $\sum_k k.P(k,\delta)$ = $\Gamma\delta$

Here Γ is tunneling rate of the electrons tunneling across the junctions. But we are interested in multiple tunneling events. So, the total time span t is divided into same time interval δ, where the number of

intervals are n=t/δ and for each interval the probability for electron tunneling is $\Gamma\delta$. This is actually a kind of Bernoulli trial where for each trial $P=\Gamma\delta$ So the probability mass function for k number of tunneling in n time intervals is calculated as

$$\text{P (k number of tunneling)} = \binom{n}{k}\left(\frac{\Gamma t}{n}\right)^k\left(1-\frac{\Gamma t}{n}\right)^{n-k} \quad (5.2)$$

But we are interested in poisson process, which can be derived from (5.2) for $\delta \to 0$, and we get

$$\text{P (k, t)} = \frac{(\Gamma t)^k e^{-\Gamma t}}{k!} \quad \text{where k= 0, 1, 2} \quad (5.3)$$

We have assumed that total K number of tunneling has occurred in t+δ time. For very small δ it can be assumed that (k-1) tunneling has happened in t time and one electron has tunneled in interval [t, t+δ]. The probability that the kth electron has been tunnelled between time interval t and t+δ is expressed as

$$\begin{aligned} &P(t \le Y_k \le t+\delta) = f_{y_k}(t).\delta \\ &\Rightarrow P((\mathrm{k}-1) \text{ tunneling in } [0,\ \mathrm{t}]).\Gamma\delta = f_{y_k}(t).\delta \end{aligned} \quad (5.4)$$

Where $f_{y_k}(t)$ is the corresponding probability density function. Replacing the expression for the probability of (k-1) tunneling, from (5.1), we finally get

$$f_{y_k}(t)=\frac{\Gamma^k.t^{k-1}.e^{-\Gamma t}}{(k-1)!} \tag{5.5}$$

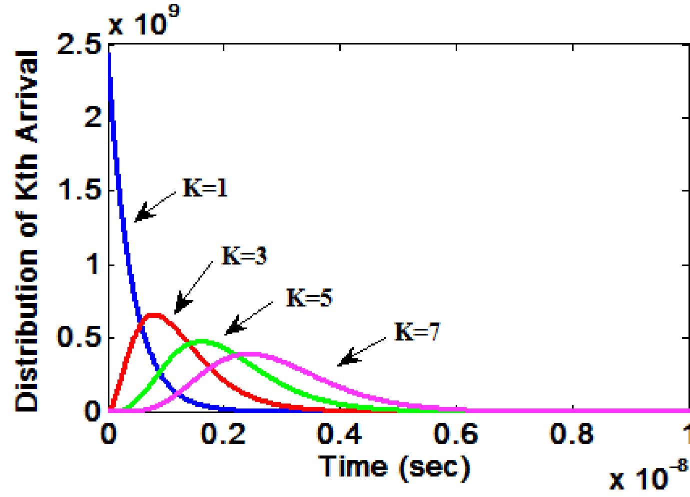

Fig. 5.1 The distribution of the kth electron arrival with constant tunneling rate for each event.

Using (5.5) the distribution of kth no. of electron tunneling in time domain is plotted in Fig. 5.1. It is observed that for K=1 the distribution function reduces to an exponential function. Being a density function the area under these curves is unity. Finally the expected time for k^{th} number of tunneling can be calculated as

$$E(t_d)=\int_0^\infty t.f_{y_k}(t)dt \tag{5.6}$$

Using (5.6) and after simplifying the solution we get

$$t_d = \frac{k}{\Gamma} \tag{5.7}$$

So the delay depends on the number of tunnel events and tunneling rate of the events.

5.4 Delay Model for Variable Tunneling Rate

Here we consider the total time t is divided into different length of intervals, δ_1, δ_2,…… δ_n. As the intervals are very small so rather than representing them by different term they can also be represented by a single term δ_{avg} where,

$$\delta_{avg} = \frac{\delta_1 + \delta_2 + \dots\dots + \delta_n}{n} \tag{5.8}$$

For this Bernoulli trial the probability of electron tunneling is given by

$P_i = \Gamma_i \delta_{avg}$ where i=1, 2,….n

Finally the probability of k electron tunneling in n time intervals is calculated as

$$\text{P (k electron tunneling)} = \binom{n}{k} \prod_{i=1}^{k} \left(\frac{\Gamma_i t}{n} \right) \prod_{j=1}^{n-k} \left(1 - \frac{\Gamma_j t}{n} \right)$$

(5.9)

Again as discussed previously we are more intended towards poisson process, which can be derived from (5.9) by $\delta_{avg} \to 0$. So the probability

of k electron tunneling with variable tunneling rates (Γ_1, Γ_2,....Γ_n) in time t is calculated as

$$P(k,t) = \frac{t^k}{k!} e^{-\Gamma_{equ} t} \prod_{i=1}^{k} \Gamma_i \tag{5.10}$$

where Γ_{equ} is the average of the k number of electron tunneling rates. Finally the probability distribution function for k electron tunneling with different tunneling rates can be expressed as

$$f'_{y_k}(t) = \frac{t^{k-1} e^{-\Gamma_{equ} t} \prod_{i=1}^{k} \Gamma_i}{(k-1)!} \tag{5.11}$$

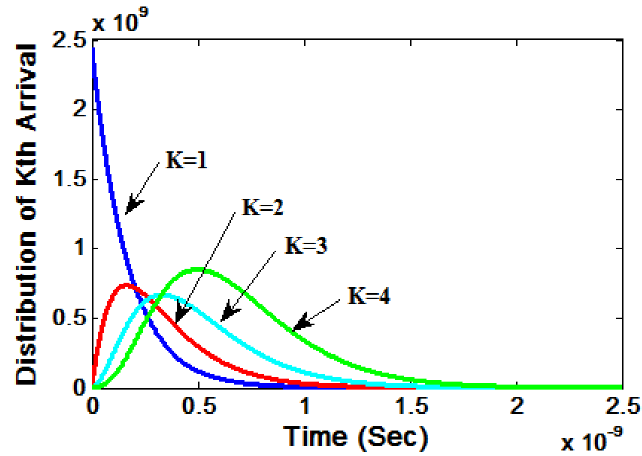

Fig. 5.2 The distribution of the Kth electron arrival with different tunneling rate for each event.

The distribution of kth electron arrival for variable tunneling rate is shown in Fig. 5.2. The variable tunneling rates considered for this plot are taken from events of logic "0" to "1" transition of inverter

explained in section 5.6. The delay of k electron tunneling with variable tunneling rates is expressed as

$$t_d = \sum_{i=1}^{k} \frac{1}{\Gamma_i} \tag{5.12}$$

So for variable tunneling rates the delay calculation depends on the individual tunneling rates of the events.

5.5 Tunnel Rates of The Junctions:

Tunneling rate is the most important parameter for single electron devices and circuits. It is calculated as [5.12]

$$\Gamma = \frac{\Delta E}{e^2 R_t \left[1 - \exp\left(-\Delta E / k_B T\right)\right]} \tag{5.13}$$

where e is charge of an electron, $k_B T$ is the thermal energy of the system, R_t is the tunnel junction resistance and ΔE is the change in the electrostatic energy for a tunnel event. The change in the electrostatic energy can be calculated following a local view or a global view of the associated tunnel junction. The local view, as the name implies takes into consideration only the junction involves in the tunneling and ignores its connection to the rest of the world. Whereas the global view takes the effect of the ideal sources connected to the tunnel junction to reestablish the equilibrium which has been disturbed by the tunneling process. Actually both the local and global view of the junction is just

the limiting cases of the orthodox theory. The change in electrostatic energy following the local view is calculated as

$$\Delta E = e\left(V_j - V_C\right) \tag{5.14}$$

Where V_j is voltage across the junction and V_c is the critical voltage of the junction. Most of the recent works [5.10, 5.11] on delay analysis calculates ΔE following the local view of the tunnel junction. Also in case of delay analysis we are concerned with individual electron tunneling which gives effect to the logic transition at the output node. So, in this work for calculation purpose the local view of the tunnel junction has been considered.

5.6 Delay Analysis of Different Logic Gates

5.6.1 Inverter

The first inverter using capacitively coupled single electron transistor was proposed in [5.14], as shown in Fig. 5.3. Though a complementary inverter with resistive coupling was proposed before tucker's inverter, but that discusses nothing on the quantitative optimization of the device. The parameter values for the inverter is given in Fig. 5.3, where C=1 aF (lowest capacitance available depending on the fabrication technology), the value of the tunnel junction resistance Rt=1MΩ. The value of the supply voltage Vdd is calculated as [5.14],

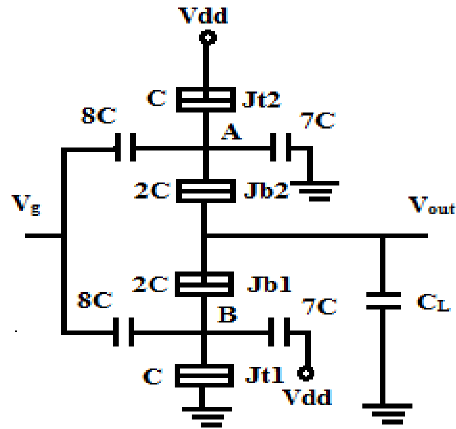

Fig. 5.3 Inverter circuit schematic

$$Vdd = \frac{1.5e}{2C'}$$

Where e is the charge of an electron and C' is the equivalent capacitance of the island. The value of the load capacitance is chosen as 360 aF [5.11]. Now, there are two possible cases, either the output of the inverter will transit from logic "0" to logic "1" or it will transit from logic "1" to logic "0".

When output transits from logic "0" to logic "1", a number of electrons will tunnel through the junctions Jb2 and Jt2 following the path, node Vout to node A and then node A to node Vdd. If the voltage across the junctions is greater than the critical voltage, the electron will keep tunneling giving rise to the output voltage. As we are considering unidirectional electron flow and only one electron tunnels at a time so the critical voltage of the respective junctions is calculated as

$V_C=e/2C_B=4.4$ mV, where C_B is the equivalent capacitance of the island 'B'. If an electron tunnels from output node to node B, the output voltage increases by $\Delta V_{out} = e/C_L$ =0.44mV. It is assumed that initially the potential of node B is V_B. After the first tunneling through Jb2, the voltage across it changes to $(V_B - e/C_B + \Delta V_{out}/9)$. This causes the tunnel event through Jt2 and the voltage across Jb2 changes to $(V_B + \Delta V_{out}/9)$ which triggers the next tunnel event through Jb2 and this process goes on until the voltage across the tunnel junctions becomes less than the critical voltage. The difference in tunnel rates between two consecutive tunneling through Jb2 is estimated as $\Gamma_{B2} = -(8/9)\Delta V_{out}$ which means the tunneling rate decreases with increase in tunneling event.

TABLE 5.1
Average Propagation Delay for the inverter circuit with different values of C_L (aF)

C_L (aF)	No. of tunnel events	Propagation delay for logic "0" to "1" transition t_{PLH} (ns)	Propagation delay for logic "1" to "0" transition t_{PHL} (ns)	Average Propagation delay (ns)
360	9	1.36	1.25	1.3
720	18	2.42	2.25	2.34
1440	36	4.35	4.05	4.2
2880	72	8.49	7.96	8.23

This can also be justified analytically, the voltage across Jb2 depends on the output voltage and with increase in output voltage the difference between the potential of node B and output node decreases

and so the tunneling rates across this junction. The difference in tunnel rates between two consecutive tunneling through Jt2 is estimated as $\Gamma_{T2} = -(\Delta V_{out}/9)$. As we already know the difference in consecutive tunneling rates for the tunnel junctions Jb2 and Jt2 so, if we can calculate the tunneling rate for the last tunnel event and total number of tunneling event we will be able to calculate the tunneling rates for all the tunnel events. The tunneling event for the last event for output transition of logic "0" to logic "1" is calculated following the procedure used in [11]. The tucker's inverter is simulated in SIMON [5.15]. The simulation result shows that the stable output voltage (V_0) and the output swing (V_{SW}) are 5.35 V and 4 mV respectively. The voltage of node B right before the last event in junction Jt2 is estimated as 0.95V. So, the voltage across this junction for the last tunnel event is (Vdd-0.95) =5.72V. The tunnel rate for the last event through Jt2 is calculated as $\Gamma_{T2,Last} = (V_{J2} - V_C)/(eR_t) = 8.2G/s$ (assuming operating temperature T=0K). The total number of tunneling event is estimated as $N = V_{SW}/\Delta V_{out} \simeq 9$. So the sequence of tunnel rates through Jt2 is given by 10.6G/s, 10.3G/s,……. 8.5G/s, 8.2 G/s. The voltage of node B right before the last tunnel event across junction Jb2 is estimated as $(0.95 + e/C_B - \Delta V_{out}/9) = 9.7V$. The voltage across this junction for the last event is given by $(9.7 - V_{out} + \Delta V_{out}) = 4.79V$. Finally the tunnel rate for the last tunnel event through Jb2 is calculated as $\Gamma_{B2,Last} = (V_{J2} - V_C)/(eR_t) = 2.44G/s$ and the

corresponding tunnel rates through Jb2 are given as, 22.04G/s, 19.59G/s,…… 4.89G/s, 2.44G/s. For each consecutive tunnel events through Jb2 and Jt2, the tunnel event with lower tunnel rate will have the dominant effect on the propagation delay. So the nine tunnel rates that will be considered for delay calculation are given as 10.6G/s, 10.3 G/s, 10.0G/s, 9.7G/s, 9.4G/s, 9.1G/s, 7.34G/s, 4.89G/s, 2.44G/s.

It is assumed that after logic "0" to "1" transition the output voltage is stable at 5.35mV.The potential of node A can be approximated as $\left(V_{out}/9 + 2V_g/9 + 7V_{DD}/18\right) = 6.15mV$. The tunnel rate for the 1st tunneling through Jt1 is calculated as 10.9G/s. Now, again following the same procedure explained earlier, the difference in the tunnel rates between two consecutive tunneling through Jt1 and Jb1 are calculated as $-(\Delta V_{out}/9)$ and $-(8\Delta V_{out}/9)$ respectively. The sequence of tunnel rates through Jt1 is given by 10.9G/s, 10.6G/s, …….8.5G/s. After the first tunneling the potential of node A changes to $2.65 - 6 + (e/C_A) = 5.45mV$, which causes the next possible tunnel event through Jb1. The tunnel rate for the first tunneling through Jb1 is approximated as 22.5G/s. The sequence of tunnel rates through Jb1 is given by 22.5G/s, 20.05G/s……….2.9G/s. As, among the two consecutive tunneling through Jb1 and Jt1, the tunnel rates for Jt1 is always less than that of Jb1, so only the tunneling through Jt1 will be considered for propagation delay calculation of logic "1" to logic "0" transition. The

average propagation delay for different load capacitance is given in Table 5.1.

5.6.2 NAND Gate

Fig. 5.4 shows the complementary C-SET based NAND gate designed by conventional CMOS design methodology. The parameter values are same as that used in inverter circuit design. High voltage fluctuations occurs in the central transistor due to the series connection of two single electron transistors in the pull down network of the designed NAND gate. To solve this issue a large capacitor of value same as the output capacitor has been connected between series connected transistors [5.16]. It can be observed that pull down network has the dominant effect on the overall propagation delay of the NAND gate. due to two series connected transistors in the pull down network, the logic 0 increases from 1.3V(in case of inverter) to 2.7V resulting in the new output voltage swing from 2.7V to 4V. Therefore the total no of tunneling event is estimated as $N = V_{SW} / \Delta V_{out} \simeq 6$. Initially the potential of node A, V_A is calculated as $(8V_{g2}/18 + 7V_{DD}/18) = 5.56mV$. The tunnel rate for the first tunneling through Jt1 is 7.25G/s. after this tunneling the potential of node A changes to -3.28V.

The potential of node C is estimated as $(8V_{g1}/18 + 7V_{DD}/18 + V_{out}/9) = 6.15mV$. So the tunnel rate through the junctions Jt2 and Jb2 is same as that of

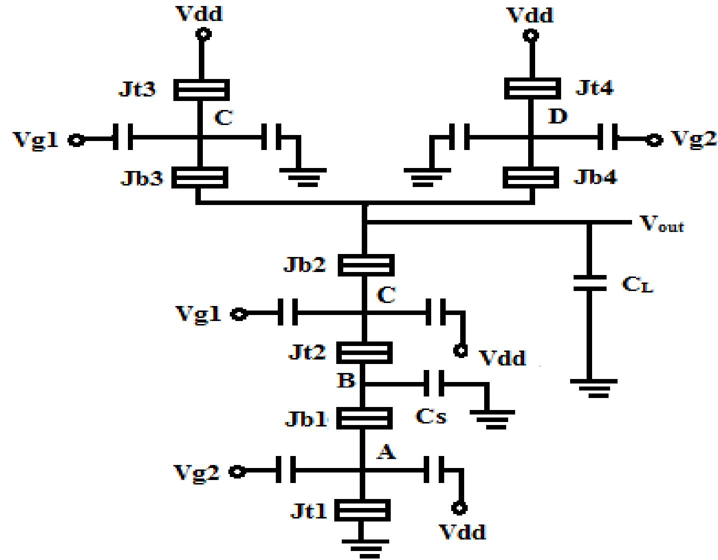

Fig. 5.4 Single Electron Transistor based two input NAND gate schematic.

the through Jt1 and Jb1 of the inverter cell. After tunneling through Jt2 the potential of node B changes to 8.8V. so the tunnel rate for the first tunneling through Jb1 is estimated as 48G/s. for the NAND gate the tunnel rates for the 1st tunneling for logic 1 to 0 transition are $\Gamma_{Jt1} = 7.25G/s$, $\Gamma_{Jb1} = 48.0G/s$, $\Gamma_{Jt2} = 10.9G/s$, and $\Gamma_{Jb2} = 22.5G/s$. The difference of the tunnel rates for junctions Jt1, Jb1 and Jt2, Jb2 is same as that of the Jt1, Jb1 of the inverter cell (as the difference in tunnel rates depends on the output capacitor value which is same as that used in case of inverter cell). Finally considering the six tunnel events the average propagation delay for logic "1" to logic "0" transition is estimated as 1.0 ns.

If any of the input is at logic "1", then the delay calculation for logic "0" to logic "1" transition at the output will be same as that of the inverter. But when both the input are at logic "0", all the transistor in the pull up network will help in the logic transition at the output. As both the transistors in the pull up network are working simultaneously and also independently so the number of tunnel events involved will reduce by half. The value of ΔV_{out} gets doubled which in turn makes the value of the difference in tunnel rates across the junctions Jb3, Jt3 and Jb4, Jt4 double. Finally the average propagation delay is calculated for different load capacitance and given in Table 5.2.

TABLE 5.2
Average Propagation Delay for NAND gate with different values of C_L (aF)

C_L (aF)	No. of tunnel events	Propagation delay for logic "0" to "1" transition t_{PLH} (ns)	Propagation delay for logic "1" to "0" transition t_{PHL} (ns)	Average Propagation delay (ns)
360	6	1.07	0.93	1.0
720	12	1.83	1.9	1.87
1440	24	3.17	3.98	3.58
2880	48	6.12	7.96	7.04

5.7 SIMULATION RESULTS

There are three different approaches to the simulation of single electronics circuits, spice macro-modeling, monte carlo based and

master equation approach. The master equation based model can be simulated in SPICE environment or for more accurate result it can be simulated using cadence tool. The SIMON simulator uses the monte carlo method. Here the results obtained from cadence tool and SIMON simulator is compared with the results of the proposed method as given in Table 5.3. The results obtained from ref. [5.15], are also included in the table to justify the validity of the proposal. It can be observed that for both inverter cell and NAND gate our results closely follows the results of the SIMON simulator.

TABLE 5.3
Comparison of propagation delay for logic "0" to logic "1" transition using Cadence tool, SIMON Simulator, ref [5.15] and proposed method

Logic circuits	Cadence tool	SIMON simulator	Ref [15]	Proposed method
Inverter	0.95ns	1.2ns	4.23ns	1.36ns
2-input NAND gate	0.85ns	1.1ns	4.28ns	1.0ns

Reference

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Chapter 6

Single Electron Threshold Logic Circuits

6.1 Introduction

Till now we have discussed on single electron transistor based circuit. The key property of single electronics is to control the transport of individual electrons. This property can be used to encode Boolean values directly as single electron charges. Lagweg et al first implemented a threshold logic gate where logic '1' and '0' values are interpreted by the presence and absence of single electron charge [6.1]. So, Threshold logic gate(TLG) can be a good alternative to Boolean logic gates in terms of logic functions.

Reliability is a very important issue for any single electronics circuits. Among all the parameters the background charge is the most important one which affects the reliability of single electronics circuits. So in this work we have analyzed the reliability of the designed multiplexer circuit. With increase in temperature if the thermal fluctuation in energy becomes greater than the charging energy then it electron can tunnel without any inputs and therefore causes for unstable operation of the designed circuit.

There are certain issues in nanoelectronic circuits like input-output limitations and interconnect constraints which can be solved using cellular network architecture by incorporating local processing capabilities. Due to its parallel architecture cellular neural network is capable of performing important task in image processing applications. The properties and features of single elcteon devices makes them a suitable candidate for cellular neural network design. A CNN is a PDP architecture which can be used for a range of applications including image processing, robotics and biological vision [6.2].

6.2 Literature Review

A number of research work have been reported in the literature regarding the threshold logic based designs and implementation of useful Boolean logic functions [6.3]-[6.8] J. F. Ramos et al implemented a threshold logic based clocked coupled inverters [6.4]. A N-bit binary encoder circuit is designed by S. E. Rehan [6.5]. Then Bahrepur et al implemented a high speed full adder using thresolg logic approach and applied that to design a compressor circuit [6.6]. Also a threshold logic based RAM cell has been reported in the literature [6.7]. The design and simulation of single electron 4:1 multiplexer have been reported in literature [6.8] but nothing have been reported on the threshold logic based design of the same. So here we have worked on

the design and reliability analysis of 4:1 multiplexer using threshold logic gates.

C. Chen and J. Mi proposed a method to analyze the reliability analysis of threshold logic gates [6.10]. Later C. Chen proposed a statistical reliability model for threshold logic gates and quiet efficiently analyzed the reliability of an AND gate [6.11]. We further extended this work to analyze the reliability analysis of threshold logic circuits. The stability analysis of single electronics circuits have been performed by several researchers using SIMON. So we have also perfomed the stability analysis of the designed circuits .

6.3 Proposed 4:1 Multiplexer Circuit

The designed multiplexer circuit is shown in Fig. 6.1. which consists of 101 nodes, 59 tunnel junctions and 104 capacitors. It has been reported that strong feedback effect occurs in the circuits consists of threshold logic gate so a buffer is included after each of the gate. Single electron transistor based inverter has been used as the buffer. Therefore buffered logic gates has been used to design the multiplexer. So theoretically two buffers should be added after each gate to get the correct result. To solve this issue top-down approach has been used while designing the circuit and finally one inverter has been added after each gate. Though it is a fact that incorporation of buffers

increases the size of the circuit but at the same time it increases the stability. It as been seen that a three input or four input threshold logic gate does not work very well so only two input threshold logic are used in the circuit. In this work only two different voltage sources has been used as given in Table 6.1 while six different voltage sources is used in [6.9].

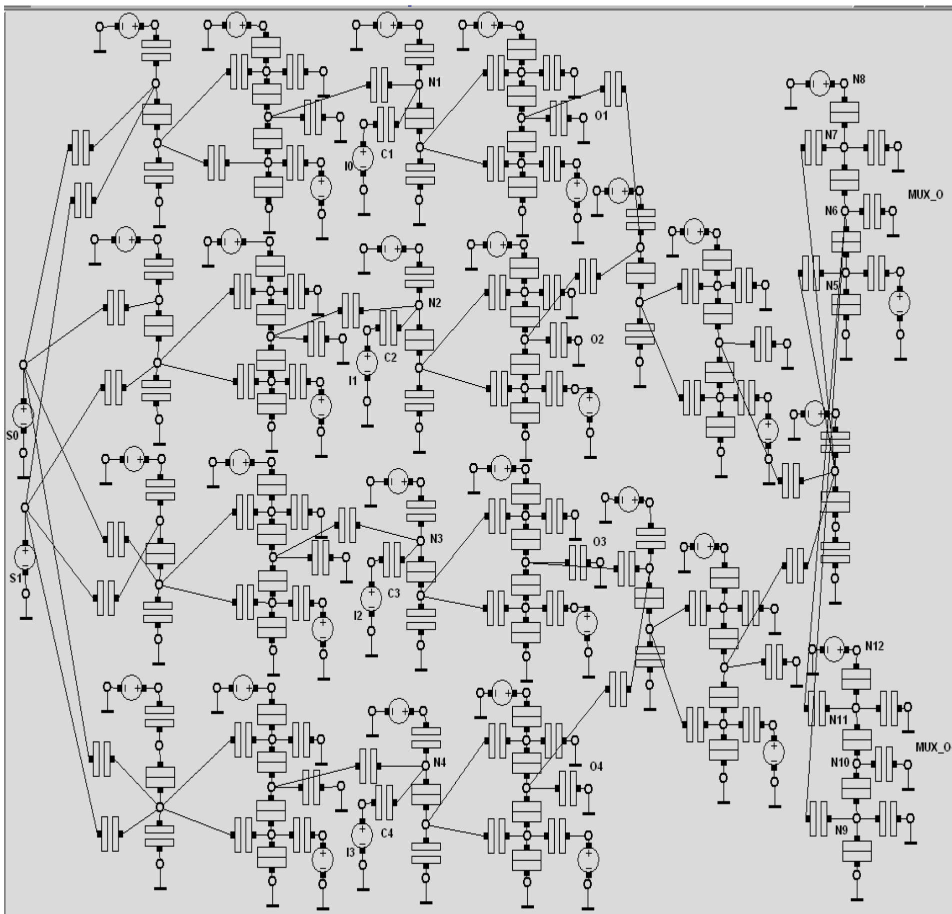


Fig. 6.1 The proposed multiplexer circuit

Table 6.1
Different voltage sources

Voltage sources	V1(V)	V2(V)	V3(V)	V4(V)	V5(V)
Proposed Circuit	0.0160	0.0171			
[13]	0.115	0.113	0.110	0.1	0.083

S0 and S1 are two control signal input and I0, I1, I2 and I3 are the four input of the circuit as denoted in Fig. 6.1. To design the buffer/inverter the parameters are taken from [6.12]. The inputs are applied to nodes N1, N2, N3, and N4 through the capacitors C1, C2, C3 and C4 respectively. The output is taken from node N6. An electron tunneling from node N6 to node Vdd1 corresponds to logic '1' as it leaves a positive charge in the output node. The absence of the positive charge in the island corresponds to logic '0'.

6.3.1 Simulation Results and Discussions

The designed circuit is simulated in SIMON [6.13], a nano structure simulation software. The control signals are pulse inputs which gives total four combinations required for selecting four input of the multiplexer. So depending on the control signal vector we will get the respective input as output. All the four possible outputs O1, O2, O3 and O4 has been shown in Fig. 6.2 and the final output, MUX_O has been shown in Fig. 6.4. The inputs corresponding to the control signal

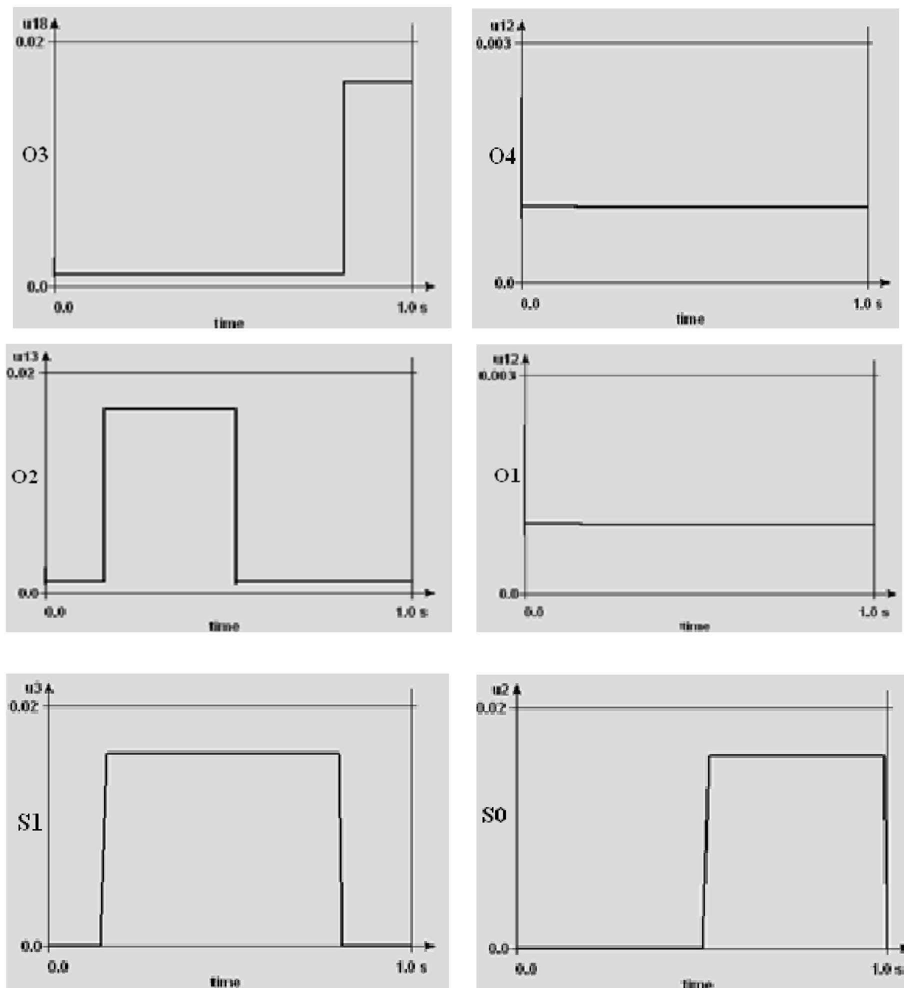


Fig. 6.2 Two control signals (S0 and S1) and four possible outputs (O1, O2, O3 and O4 corresponding to [S0, S1]=[0, 0], [0, 1], [1, 0] and [1, 1] respectively).

combination are given in Table 6.2. Here we have used pulse waveform form control signal rather than using DC values. If we would have used DC values we would have needed eight different signals, four for each of the control input. But with the proposed

approach we need only one variety for each of the control input which obviously increases the readability of the circuit. The time variation of charge at the output node N5 has been shown in Fig. 6.4. By comparing Fig. 6.4 and 6.5 it can be observed that the output is logic 1 if there is a positive charge at the output and the output is 0 if there is no charge present at the output node. So it can be concluded that in threshold logic based circuits only one electron is allowed to leave the output node for getting a logic '1' value.

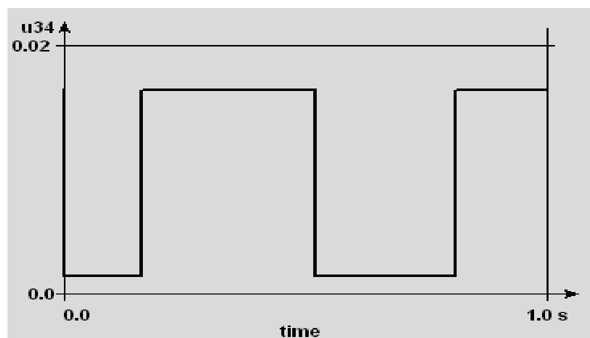


Fig. 6.3 Final Output of the Multiplexer

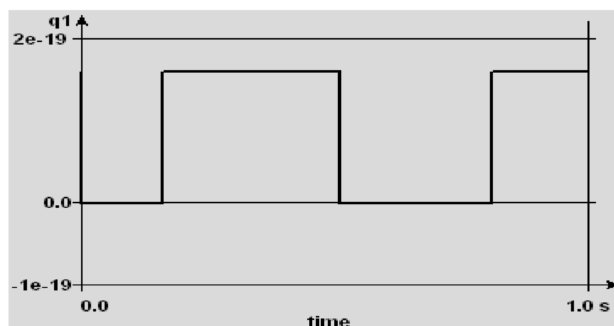


Fig. 6.4 Time variation of the charge at the output node N5 ofthe designed circuit

Table 6.2
Control signal and input's Values

S0	S1	INPUT(V)	Logic Value	Designation
0	0	0.0	'0'	I0
0	1	0.016	'1'	I1
1	0	0.0	'1'	I2
1	1	0.016	'0'	I3

6.3.2 Reliability Analysis

Reliability is one of the most important issue in single electronics technology. During fabrication of single electron devices random charges or trapped charges are formed on the nodes of single electron devices which is popularly known as background charges [6.14]. As these charges are randomly distributed in the substrate near the island or near the tunnel junction so it is impossible to describe them microscopically. Researchers have come up with different model of background charges, considering different approximations to analyze the effect of these charges on single electron devices [6.15]-[6.17]. Abramov et al proposed three models which can be incorporated in 2D numerical models to capture the effect of these charges [6.16]. The most commonly used model of background charges represents them as constant, $Q_0 = N^{0\prime}e$, where e is elementary charge. This model of background charge has been accepted by semi classical model and also by the well established analytical model [6.18].

The trapped charges creates extra voltage which actually changes the total voltage across the junction. If this change in voltage makes the junction voltage overcome the critical voltage of the junction then it forces an electron tunnel across that junction which eventually causes the unreliable operation of the circuit. As these charges are random in nature so we have considered two very commonly used distributions namely uniform distribution and normal distribution to characterize them.

Assume the background charges are uniform distributed over all the nodes in the designed circuit, given by

$$p\left(\frac{z}{q_e}\right) = \begin{cases} \frac{1}{2\eta}, -\eta \le \frac{z}{q_e} \le +\eta \\ 0, otherwise \end{cases} \tag{6.7}$$

Here Z is the random variable, qe is unit charge and η is the variation factor. The range of the random variable is $\pm\eta q_e$ Here η represents the extent of variation so it is known as variation factor. The random data with uniform distribution are generated using MATLAB's random number generation toolbox. The distribution of random data corresponding to η =0.04 has been shown in Fig. 6.5.

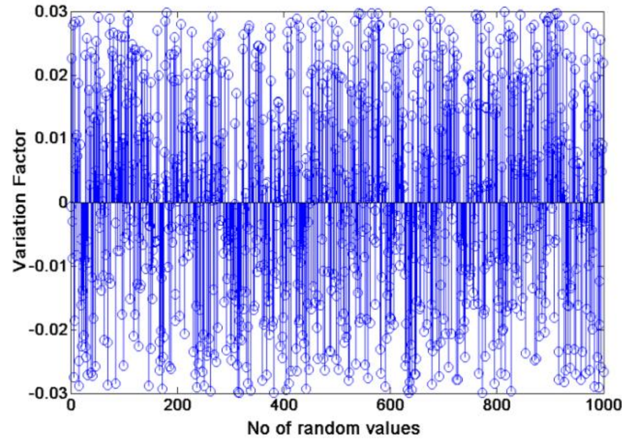


Fig. 6.5 Uniform distribution of random data

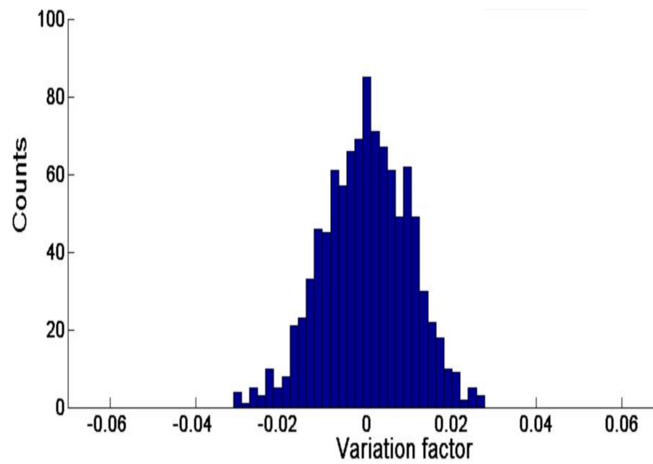


Fig. 6.6 Normal distribution of random data

The random charges can also take normal distribution with standard deviation σ, represented as

$$p(z1) = 1/(\sqrt{2\pi}\sigma)e^{-\frac{Z_1^2}{2\sigma^2}}) \tag{6.8}$$

Here Z1=Z/qe, and Z is the random variable. According to three sigma rule or empirical rule of statistics for normal distribution 99.7% of the area lie within three standard deviation of the mean [6.19]. So following this rule the value of the standard deviation is considered as $(\sigma / q_e) = \eta / 3$. The normally distributed data corresponding to η = 0.03 has been shown in Fig. 6.6.

The reliability of the circuit is analyzed following the steps given below

1) Random uniformly distributed data are generated using MATLAB with η=0.01.
2) These random data are distributed among all the 104 nodes and then the circuit is simulated in SIMON to check the operation.
3) Step 1-2 is repeated for T=100 times with new randomly generated data.
4) If the number of correct outputs is S then the reliability r of the designed circuit is calculated as

   $$r = \frac{s}{t} \times 100$$

5) Step 1-4 is repeated with η =0.02, 0.03 and 0.04.
6) Step 1-5 is repeated for normal distribution.

The effect of background charges for different distribution is shown in Fig. 6.7. It can be observed that normal distribution provides better

reliability than uniform distribution. Up to the value of η =0.01, both the distribution gives same result and the corresponding reliability is close to 100%. In case of uniform distribution a sudden fall is noticed after η =0.02 which reduces the circuit reliability from 76% to 25%, and after η =0.035 the circuit becomes almost unreliable. In case of normal distribution a large fall is noticed after η =0.03, but it goes down to 40% which is the lowest reliability. The data corresponding to various variation factor and distribution is given in table 6.3.

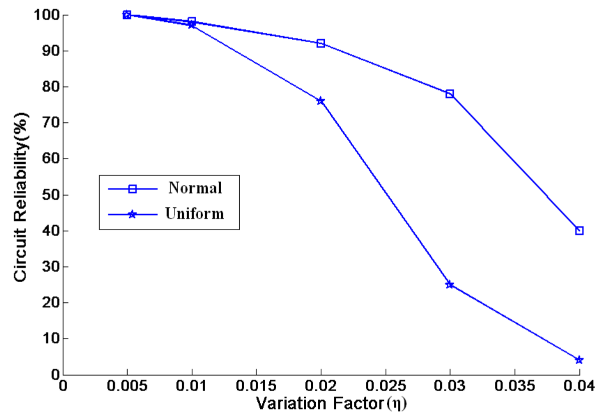


Fig. 6.7 Reliability of the circuit with normal and uniform distribution of background charges

Table 6.3
Details of circuit reliability with variation factor

Variation Factor(η)	Circuit reliability (%)	
	Normal Distribution	Uniform Distribution
0.01	98	97
0.02	92	76
0.03	78	25
0.04	40	4

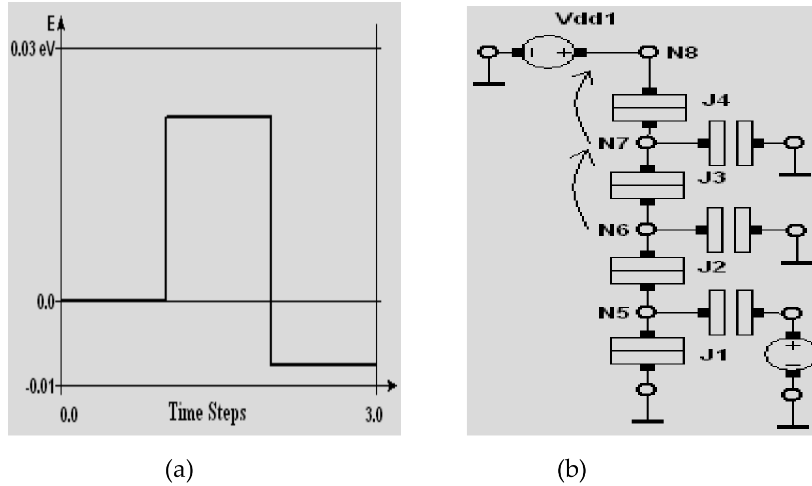
6.3.3 Stability Analysis

The stability of the designed multiplexer circuit is tested using SIMON. The free energy history diagram for the output transition of logic '0' to logic '1' is depicted in Fig. 6.8(a). The transportation of electron in the output buffer from node N6 to node Vdd1 for this transition is shown in Fig. 6.8(b). In the first time step of Fig. 6.8(a) no charge is present on the island. In the second time step an electron tunnel from node N6 to N7 through J3. Finally the third step belongs to the electron travelling from node N7 to Vdd1 through J4 which causes the system to reach a local minima as shown in Fig. 6.8(a). The free energy of the system is calculated as [6.12]

$$E_f = \sum_{i=1}^{3} E_{t_1} \qquad (6.9)$$

Where E_{t_i} is the free energy corresponding to each time step. The free energy is calculated as 0.044eV.

The stability of the designed multiplexer circuit is demonstrated in Fig. 6.9. SIMON works on the principle of calculation the free energy for each combination of considered two inputs. The local minima of circuit's free energy denotes a stable point and are coloured in white. And the local maxima of circuit's free energy corresponds to unstable point and are represented as black coloured points. The rest of the points are coloured grey which justifies for the small current that runs



(a) (b)

Fig. 6.8 (a) Free energy history diagram (b) Electron tunneling phenomena in the output buffer

through the junctions. The points correspond to the input control signal vectors [0, 0], [0, 1], [1, 0], [1, 1] are presented as A, B, C and D respectively as shown in Fig. 6.10. The input signal vectors [0, 0], [0, 1], [1, 0], [1, 1] are presented as A, B, C and D respectively as shown in Fig. 6.9. It can be observed from the figure that all the four points are in stable regions. The main concern regarding the stability of any single electronics circuit is temperature. The first condition to observe a single electron effect is that the charging energy must be greater than the thermal energy [6.14]

$$E_C = \frac{e^2}{2C} >> K_B T \tag{6.10}$$

Here E_C the charging energy of the system, C is the equivalent capacitance of the island and K_BT is the thermal energy. So the

charging energy increases linearly with temperature. If the thermal energy becomes greater than the charging energy, electron starts tunneling due to thermal fluctuations in energy, which finally results in instability of the circuit. It can be observed from (6.9), that the charging energy depends on the equivalent capacitance of the island. To observe the effect of temperature on the stability of the multiplexer circuit the stability of the design is again plotted with increase in temperature. The stability plot for higher temperature is shown in Fig. 6.10, where all the four points lies in the unstable region. This clearly signifies that with in increase in temperature the stability of the circuit reduces. Also the value of the changes on free energy increases from $1.84X10^{-10}$ to $2.76X10^{-8}$ which justifies that with increase in temperature the tunnel events increases which in turn increases the free energy maxima.

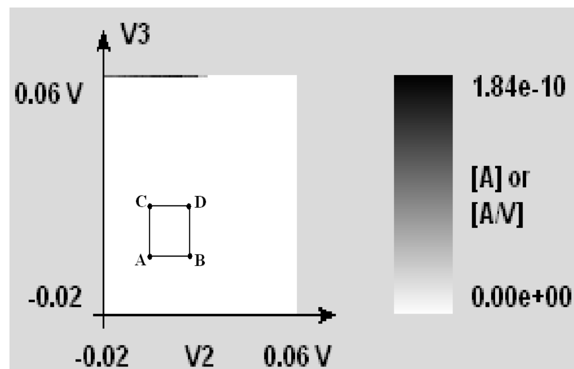


Fig. 6.9 Stability plot of the circuit with: A= [0, 0], B= [0, 1], C= [1, 0], D= [1,1] and T= 0 K.

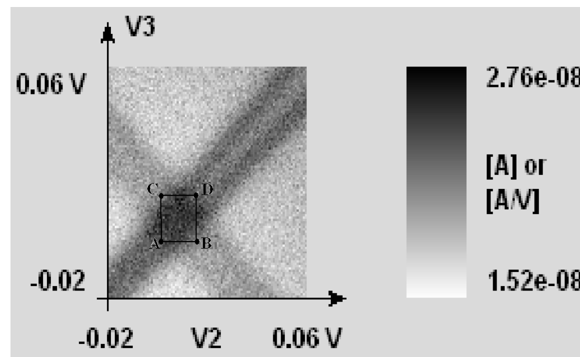


Fig. 6.10 Stability plot of the circuit with: A= [0, 0], B= [0, 1], C= [1, 0], D= [1, 1] and T=2 K

6.4 Threshold Logic Based Neuron Cell

In the previous sections we have explored the application of single electron threshold logic gates. Here we have shown a different application of single electron threshold logic gates. How a single electron threshold logic gate can be think as a basic neuron cell and can be applied for designing a neural network is explored in this section. In recent times different strategies and architecture have been explored to improve the quality of image processing. It has been observed by the researchers that neural network offer better performance compared to the existing technologies in different image processing applications like shadowing, pattern recognition etc [6.20]. The properties of single electron devices and its quantum mechanical behaviour made them suitable for neural network based applications. Recently due to its massively increased computational efficiency single electron devices

has gained considerable attention for neural computing. But to fulfil our goal first we need to have proper fabrication methodologies [6.21]-[6.24]. Recent improvement in fabrication methodologies have made it possible to fabricate single electron devices.

The existing approach for real-time image processing has become inefficient, whereas neurobiological systems can efficiently perform this kind of tasks. So people are trying to adapt the basic strategy of our nervous system so that this approach can be used for our beneficial. Cellular neural network first proposed by Chua et al is the most promising architecture which network follows a massively parallel architecture [6.2]. The processing elements of a cellular neural network are a neuron cell that are arranged in a locally interconnected array. Single electron devices have some serious drawbacks in terms of co-tunneling events and background charges. These issues can be resolved by using parallel distributed processing (PDP) architectures [6.25]. Cellular non linear network is one of the most attractive PDP architecture which offers robustness against local fluctuation and redundancy. As we know that today's complex signal processing systems involves large number of devices with large connectivity so, the device size and the power consumption has become a very crucial issue. Therefore the use of single electron threshold logic gate as a basic neuron cell for cellular neural network not only offers a good platform

but also helps it to compensate for his own drawbacks. Researchers have already been working on the design of single electron device based neuron cell. Goosens et al shown designs based on single electron synapses and neurons [6.26]. A novel neuron structure with n inputs and 6n+2 SET was proposed by Kirihara and Taniguchi et al [6.27]. But this structure was more complex than that was proposed by Goosens et al. Later Gerousis et al proposed a new architecture but the problem is it cannot consider negative weights [6.19]. This problem was solved by Flak et al., who proposed a programming version of the neuron cell where a binary programming scheme has been used to accommodate the positive and negative values but includes a separate circuit to perform this operation [6.28]. To the best of our knowledge the proposed threshold logic based cell is the smallest of all neuron cell proposed so far, which can take positive and negative values on either side of a tunnel junction without adding any extra circuitry in the system.

6.4.1 Threshold Logic Gate as A Neuron Cell

The basic structure of a single electron threshold logic gate is already discussed in chapter 2. The proposed single electron threshold logic based neuron cell is shown in Fig. 6.11. Here X and Y points resembles with the same point of the Fig. 2.6. It can be seen that all the capacitors

corresponding to positive and negative weights are connected to node X and Y respectively.

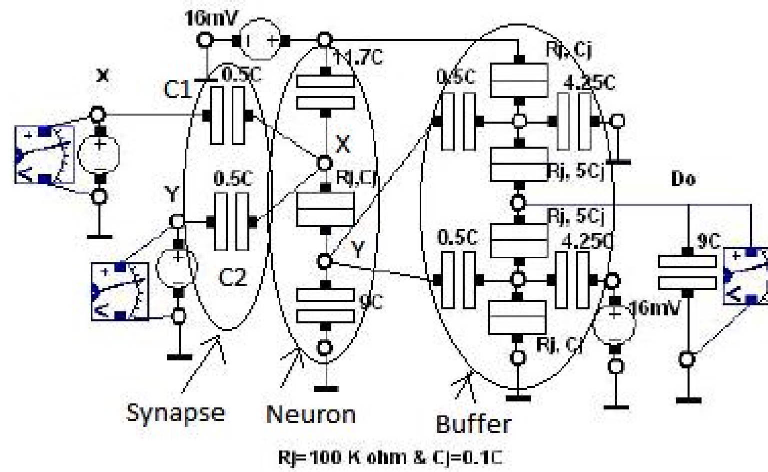


Fig. 6.11 The proposed Neuron cell

Here the capacitors C1 and C2 works as synapses. It can be observed that the synapse is represented by capacitors only without adding any extra circuitry to the circuit. Value of the output capacitance depends on the number of negative weights attached to node Y. A buffer is added to the output of the neuron cell to improve the reliabilty of the circuit.

6.4.2 Activation Function

In a neural network the ouput to a given input depends on the activation funcion of the neuron cell. If a neuron cell is sufficiently activated then it gives the ouput as logic '1' else the output is logic '0'.

Considering all the voltages of Fig 2.6 as 0 volt, it can be viwed as a series connection of three capacitors C_{Σ}^{P} , C_{Σ}^{n} , Cj. The value of the critical voltage Vc is estimated as [6.1]

$$V_c = \frac{qe}{2(C_j + \frac{C_{\Sigma}^{p} C_{\Sigma}^{n}}{C_{\Sigma}^{p} + C_{\Sigma}^{n}})} = \frac{(C_{\Sigma}^{p} + C_{\Sigma}^{n})qe}{2C_{\tau}} \quad (6.11)$$

The volatge of node X is denoted as Vx and it is calculated as

$$V_x(V_b, V^P) = \frac{(C_j + C_{\Sigma}^{n})(C_b V_b + \sum_{k=1}^{r} C_k^p V_k^p)}{C_{\tau}} \quad (6.12)$$

Finally the output of the designed threshold logic gate is calulated as

$$V_0(V_b, V^p, V^n) = \frac{C_j(C_b V_b + \sum_{k=1}^{r} C_k^p V_k^p)}{C_{\tau}} + \frac{(C_j + C_{\Sigma}^{p}) \sum_{l=1}^{s} C_l^n V_l^n}{C_{\tau}} \quad (6.13)$$

The ouput of the threshold logic gate is the input for the designed tranistor. The tunnel rates for the single electron transistor is calculated as [6.29]

$$\Gamma = \frac{1}{e^2 R_j} \times \frac{-\Delta E}{1 - \exp(\Delta E / k_B T)} \quad (6.14)$$

Where ΔE is the change in the electrostatic energy. We are assuming the tunneling across junction 1 only. The change in electrostatic energy for tunneling across junction 1 is estimated as

$$\Delta E_{1,add} = \frac{e}{C_{\Sigma}}\left\{ne + \frac{e}{2} - V_{out}C_{g1} - V_{g2}C_{g2} - VC_{2}\right\} \tag{6.15}$$

$$\Delta E_{1,sub} = \frac{e}{C_{\Sigma}}\left\{-ne + \frac{e}{2} + V_{out}C_{g1} + V_{g2}C_{g2} + VC_{2}\right\} \tag{6.16}$$

The change in the electrostatic energy for tunneling across tunnel junction 2 is calculated as

$$\Delta E_{2,add} = \frac{e}{C_{\Sigma}}\left\{ne + \frac{e}{2} - V_{g}C_{g1} - V_{g2}C_{g2} + V(C_{\Sigma} - C_{2})\right\} \tag{6.17}$$

$$\Delta E_{2,sub} = \frac{e}{C_{\Sigma}}\left\{-ne + \frac{e}{2} + V_{g}C_{g1} + V_{g2}C_{g2} + V(C_{2} - C_{\Sigma}\right\} \tag{6.18}$$

Here $\Delta E_{1,add}$, $\Delta E_{1,sub}$ and $\Delta E_{2,add}$, $\Delta E_{2,sub}$ denotes the addition and subtraction of one electron to the island across junction 1and Junction 2 respectively. Considering three island states of the island, -1, 0 and 1, the current through the transistor is calculated as

$$I = e\sum_{n=-1}^{n=+1} P_{n}\left(R1R_{n,l-r} - R1L_{n,r-l}\right) \tag{6.19}$$

Here P_n is the probability that n electrons will occupy the island. R1R and R1L are the tunneling rates for tunneling through tunnel junctions 1, across right and left side respectively. The probability corresponding to island states of -1 and +1 are calculated as [6.30]

$$PN_1 = PN_0 \frac{R1R_0 + R2L_0}{R1L_1 + R2R_1} \tag{6.20}$$

$$PN_{-1} = PN_0 \frac{R1L_0 + R2R_0}{R1R_{-1} + R2L_{-1}} \tag{6.21}$$

The value of PN_0 is estimated through a recursive process. The current is calculated as

$$I = \frac{2}{R_j C_\Sigma}\left\{\begin{array}{l}\left(\begin{array}{l}\dfrac{C_j(C_bV + \sum_{k=1}^{r} C_k^p V_k^p) + (C_j + C_\Sigma^p)\sum_{l=1}^{s} C_l^n V_l^n}{C_\tau} C_{g1} \\ +V_{g2}C_{g2} + VC_2\end{array}\right)\left(P_{-1} + P_0 + P_1\right) \\ +e\left(P_{-1} - P_1\right)\end{array}\right\} \tag{6.22}$$

So, it can observed from (6.22) that the ouput current depends on the capacitances values and supply voltage.

6.4.3 Basics of A CNN Architecture

In a CNN architecture the neuron cell is represented by inputs, outputs and a state which depends on the dynamical laws. Each cell in a CNN is connected to its neighbour cells through inputs u_{kl}, and outputs y_{kl}. For a cell the connection are valid which lies in the sphere of influence s_{ij} of radius r [6.20]. Each neuron cell receives a weighted feed forward signal ($b_{kl}u_{kl}$) and a weighted feedback signal ($a_{kl}y_{kl}$) from its neighbouring cells. The state equation of a CNN cell is given by

$$\frac{dx_{ij}}{dt}(t) = -x_{ij} + z_{ij} + \sum_{kl \in S_{ij}} a_{kl} y_{kl} + \sum_{kl \in S_{ij}} b_{kl} u_{kl} \tag{6.23}$$

Here Xij is the state variable of the cell which may be current or voltage and Zij is corresponding threshold value. The output of the cell is expressed as

$$y_{ij} = f\left(x_{ij}\right) = \frac{1}{2}\left(\left|x_{ij}+1\right| - \left|x_{ij}-1\right|\right) = \begin{cases} 1........x_{ij} \geq 1 \\ x_{ij}.....\left|x_{ij}\right| \geq 1 \\ -1.....x_{ij} \leq 1 \end{cases} \tag{6.24}$$

A CNN architecture is basically characterized by three templates namely A, B and Z. Template A and B defines the modulation of input signals and feedback signals from the neighbouring cells respectively. Template Z represents the threshold value. Template A can never take a null value but depending on situations template B and Z can take null values.

6.4.4 Shadowing CNN Circuit

In a shadowing CNN right of a cell with high input are shadowed. A threshold logic based shadowing CNN circuit is depicted in Fig. 6.12. Earlier a single electron transistor based shadowing CNN circuit was proposed by Gerousis et al [6.20], which uses feedback connections from the output to the input of individual cell. We simplified that

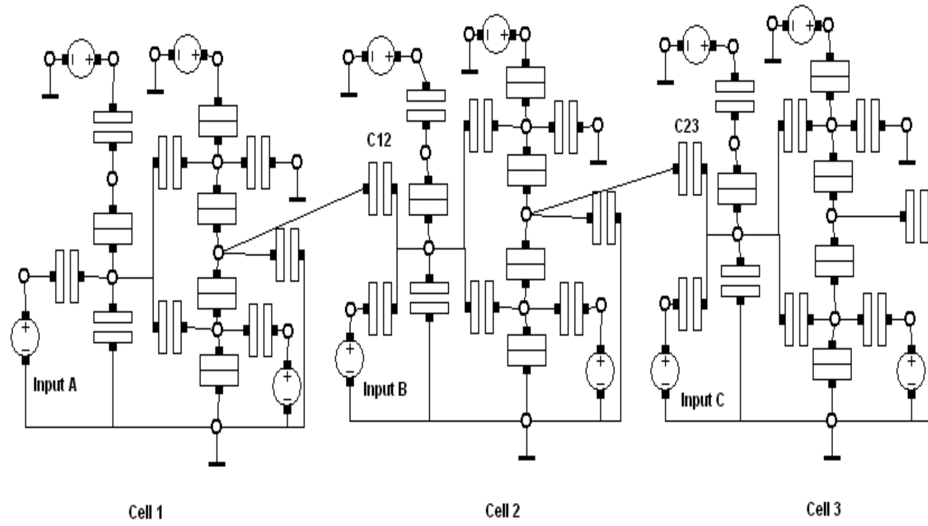
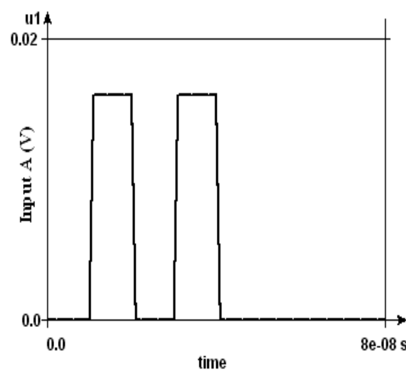
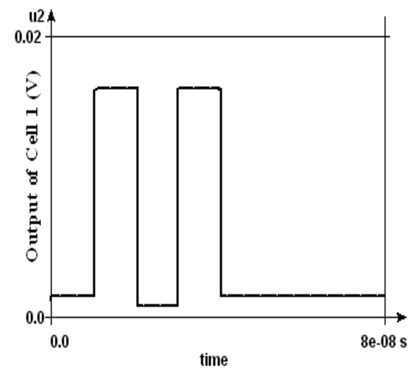


Fig. 6.12 Schematics of the single electron threshold logic based 3 cell shadowing CNN. Here C_{12} and C_{23} are the intercell capacitors.



(a)



(d)

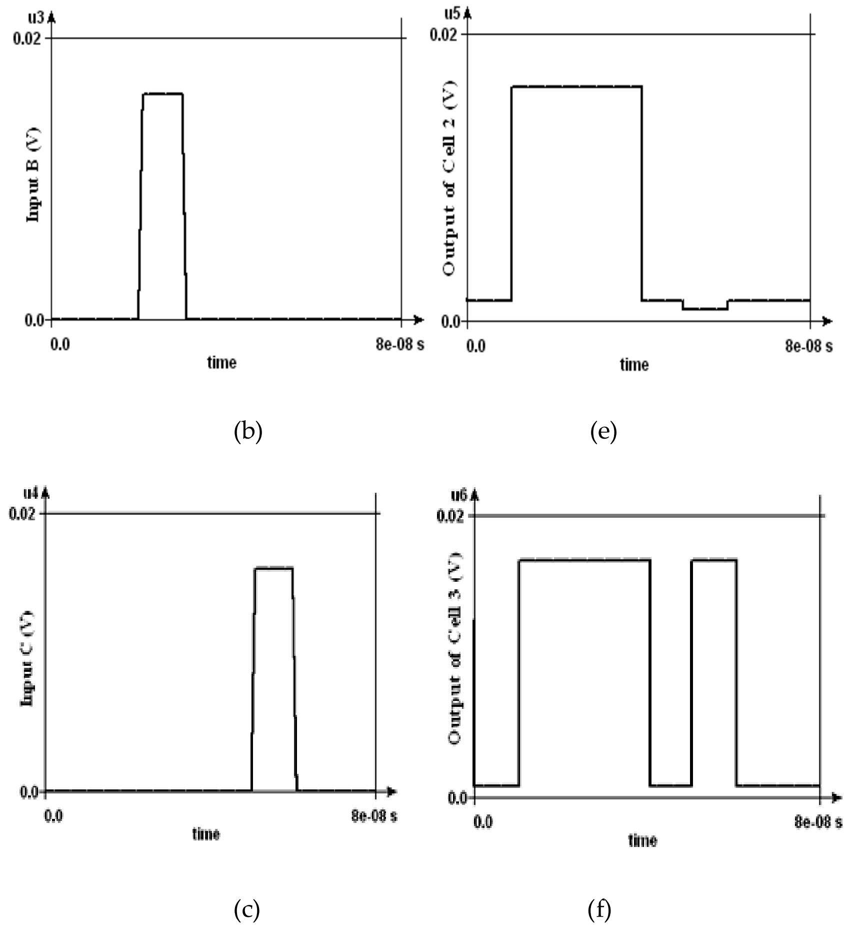


Fig. 6.13 Transient simulation results of the proposed 3 cell shadowing CNN where the input bits are represented by (a) Input A (b) Input B (c) Input C, and the outputs, (d) output of cell 1, (e) output of cell 2, (f) output of cell 3, clearly justifies the accuracy of the proposed architecture.

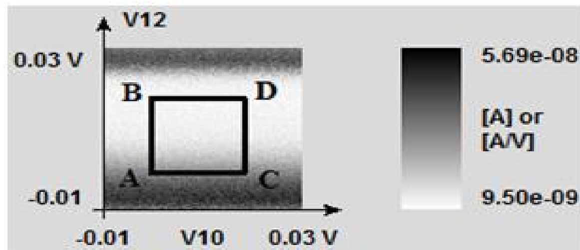
design by removing feedback connections which implies that for our design the template B=0. It is also to be observed that in our design the capacitance template is also very simple as the same capacitance values

has been used by the input capacitors representing synapses and the interconnect capacitors. If there is a high input to a logic cell then all the cell to the right of that cell along with that cell itself will give a high output which is known as the shadowing of the output bits by the input bits. The designed circuit is simulated in SIMON and the corresponding simulation results are shown in Fig. 6.13. It can be verified through the simulation results that the proposed circuit is working with sufficient accuracy.

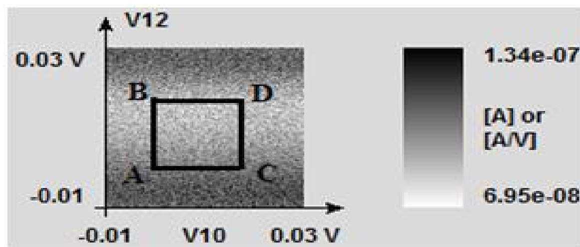
6.4.4.1 Stability Analysis

As there are three inputs (V1, V2 and V3) to the circuit so the stability analysis are performed taking any of the two inputs at a time. The stability plots for the designed circuit considering different temperatures are demonstrated in Fig. 6.14. The input vectors are represented as A [0, 0], B[0, 1], C[1, 0] and D[1, 1] respectively. It can be observed that for Fig. 6.15(a) points B and D lies in the stable region whereas for other points a very small current flows through the circuit. In case of Fig. 6.14(b), Points B and D lies in the grayish area which implies a very small leakage current and other points lies in the unstable region. For Fig. 6.14(c) all four points are in unstable region. This clearly explains that with increase in temperature the fluctuation in energy increases which results in instability of the circuit. The

fluctuation in energy increases from 5.69X10^{-8} for temperature 5K to 3.21X10^{-7} for 30K. To neglect the co-tunneling events, due to quantum fluctuations in energy the value of junction resistance has been chosen much higher compared to the quantum resistance [6.31] value.



(a)



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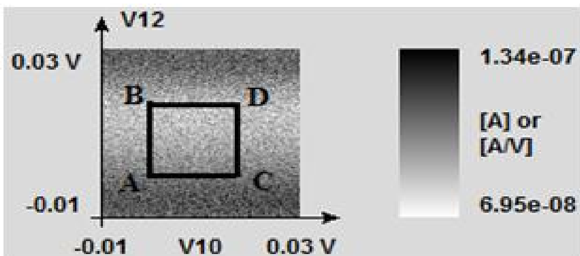

(c)

Fig. 6.14 Stability plot of the designed circuit using SIMON for different temperature (a) 5K (b) 15K (c) 30K with A [0, 0], B [1,0], C [0,1], D [1,1], points represents the four input signal vectors.

6.4.4.2 Reliability Analysis

The reliability of the designed circuit is analyzed considering normal and uniform distribution as shown in Fig. 6.15. The reliability of the designed circuit is analyzed considering a single cell and the complete circuit to observe the effect of individual neuron cell. For a single cell the reliability degrades in a linear nature with the lowest reliability as 80%. In case of the complete circuit the slope increases after variation factor of 0.1 and reduces to a value of 60% for the variation factor of 0.4. It can also observed that normal distribution shows better result compared to uniform distribution.

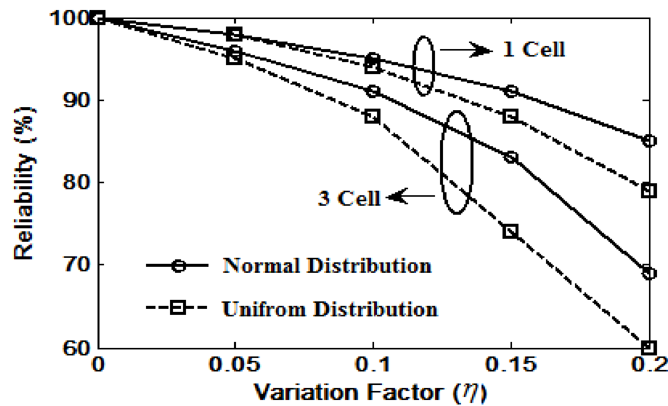

Fig. 6.15 Reliability analysis of the designed 3 cell shadowing circuit for different values of the background charges. Here solid line represents the uniform distribution and dashed line represents the normal distribution of random variable.

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Chapter 7

Design and Simulation of Hybrid SET-MOS Circuits

7.1 Introduction

Till now we have been quiet able to follow the moor's law efficiently by minimizing the device size. But in near future we would hit a point where further miniaturization of the device dimension would not be possible as MOS devices would face a number of limitations such as quantum effect, increased gate oxide leakage and increased subthreshold leakage. So researchers are looking for alternative technologies which can be a replacement of the CMOS technology. Single electron tunneling technology is one of the most promising candidate for future VLSI solutions due to its nano feature size and ultra low power dissipation. Though single electron transistor has some important advantages it has some disadvantages too like lower gain, very low temperature operation and background charge problem. So, single electron tunneling technology and CMOS technology are rather complementary to each other which justifies that in near future CMOS have to share its domination over semiconductor industry with single electron tunneling technology [7.1]. In the last chapter we have

discussed the reliability ans stability analysis of single electronics circuits. Single electron transitor being an integral part of the hybrid SET-MOS circuits, the reliability and stability analysis of SET-MOS circuits have the same importance as that of single electronics circuits. But till now nothing has been reported on this issue. So, we have proposed an approach to analyze the reliability and stability of hybrid SET-MOS circuits.

7.2 Literature Review

Basic digital circuits have already beed designed using hybrid approach [7.2]. In the middle of the last decade some very important circuits had been designed and implemented using this technology which includes Phase locked loop [7.3] and voltage controlled oscillators [7.4]. B. Sui et al implemented hybrid nano reconfigurable logic cells [7.5]. In 2011 A. A. Prager et al successfully fabricated the first hybrid SET-MOS circuit [7.6]. Apart from basic single electron transitor, a multi gate or a multiple tunnel junction SET have also been used to desing hybrid circuits [7.7]. Then W. Wei et al designed a hybrid memory cell [7.8]. R. Parekh et al discuused the fabrication aspect and capabilities of hybrid SET-MOS circuits [7.9]. Recently M. M. Abutaleb proposed a static differential design style for SET-MOS hybrid circuits [7.10].

Pass transistor logic is an alternative to CMOS logic which reduces the number of transistors involved to implement a particular logic function. In case of pass transistor logic the input signal is not only applied to the gate terminal but can be applied to the source/drain terminal as well [7.11]. Yokinori et al first proposed single electron transistor based pass transistor logic which can be used to implement different logic gates [7.12]. In this work we have proposed a hybrid SET-MOS pass transistor logic and implemented universal logic gates with a gain almost equal to 1.

7.3 Hybrid Pass Transistor Logic

The basic circuit of hybrid SET-MOS pass transistor logic is shown in Fig. 7.1. When A = 1 the NMOS is On and current flows following the path P1. For A=0, SET is ON and current flows through the path P2. Finally we will get the output as the combined effect of these operations. Here it has been assumed that the source terminal of NMOS and drain terminal of SET is connected to a logic '1' value. According to previous works, for satisfactory performance the value of the input should be greater than the supply voltage. This problem has been solved in our design and same values has been used for both the input voltage and supply voltage. So our proposed approach definitely reduces the complexity of the design.

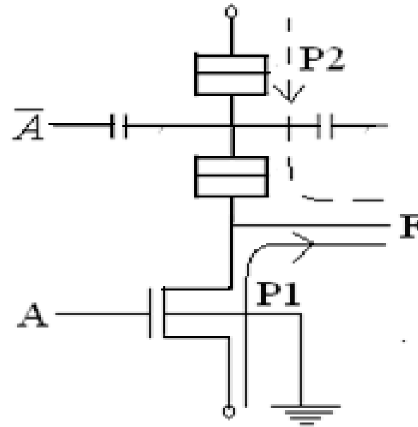


Fig. 7.1 The elemental circuit of the hybrid SET-MOS pass transistor logic.

7.3.1 Universal Logic Gates Design

We have implemented NAND and NOR logic gate using the proposed hybrid SET-MOS pass transistor logic as shown in Fig. 7.2. Here we have applied different input in their original and complemented form to get the desired output. The corresponding logic operations are implemented indirectly by following De Morgan's law. In case of NAND gate, if $\overline{A}$ =1, the MOS is ON and current flows from VDD to node F and output is logic '1'. When A =1, the output is $\overline{B}$. So the output is obtained as

$$F = \overline{A} + \overline{B} = \overline{A.B} \quad (7.1)$$

Which is the expression of a NAND gate with inputs A and B. In Fig. 7.2(a), if $\overline{A}$ =1, the MOS transistor is ON and the output is $\overline{B}$. Again if

A=1 then output current discharges through the SET giving the overall output as

$$F = \overline{A}.\overline{B} = \overline{A+B} \tag{7.2}$$

Therefore the logic circuit of Fig. 7.2(b), works as a NOR gate. To design the logic gates MIB model of single electron transistor [7.13] and BSIM model of SET has been used. The parameters of both the models used in the simulation process is given in Table 7.1. As can be observed from the table 65nm CMOS technology has been used for MOSFET. The threshold voltage of the MOSFET is taken as 220 mV. In case of

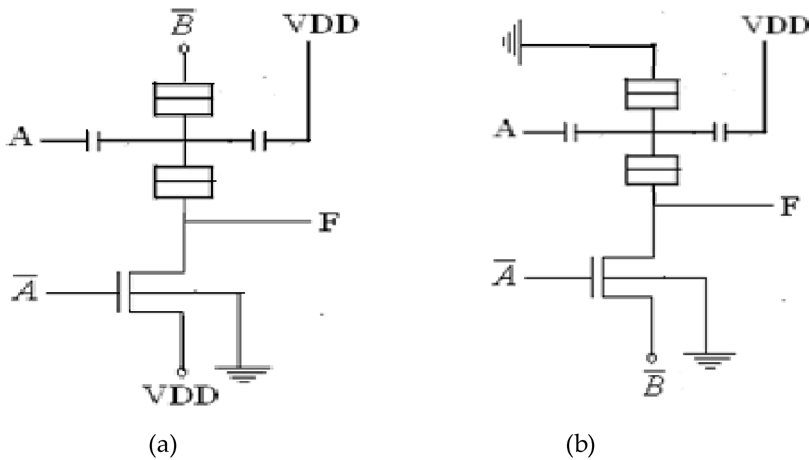


Fig. 7.2 Designed hybrid (a) NAND logic gate (b) NOR logic gate, Here input A is applied directly to the gate of the SET and in complemented form to the gate of the NMOS transistor.

SET same values of resistances and capacitances have been used for both the logic gates which reduces the complexity of the design. For

the accuracy of the orthodox theory the value of the tunnel junction resistance is taken as 1MΩ [7.14]. The values of capacitances are tried to kept as small as possible so that the design logic gates can work for a good range of temperature. The different value of the parameters are chosen following parametric analysis.

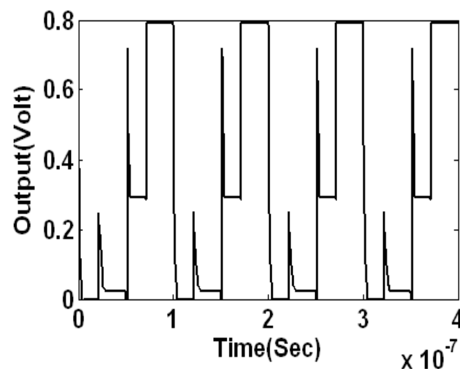
Table 7.1
Parameter values of the designed universal logic gates

Device	Parameters	NAND	NOR
NMOS	W(nm)	65	65
	L(nm)	100	100
	V_{th}(V)	0.22	0.22
SET	C_{TS}, C_{TD}(F)	1.0×10^{-19}	1.0×10^{-19}
	R_{TS}, R_{TD}(Ω)	1.0×10^{6}	1.0×10^{6}
	C_{G1}	2.75×10^{-19}	2.75×10^{-17}
	C_{G2}	1.3×10^{-19}	1.3×10^{-19}

7.3.2 Simulation Results

The designed logic gates are simulated in SPICE simulation environment, where the analytical model of SET is incorporated through its verilog-A interface. In SPICE the accuracy of the simulation result depends on the value of relltol and abstol. Giving the accuracy much priority compared to the simulation time we have chosen the value of the abstol and reltol as 0.2 nanoamps and 0.005% respectively. The value of the supply voltage is taken as 0.8 V which also represents the logic '1' value and 0V denoted the logic '0' value. The output of the NAND gate is shown in Fig. 7.3(c). It is observed that for input

combination of [0, 0] the output is 0.8 V, but for the combination of [0, 1] or [1, 0] the output is not 0.8 V rather it is around 0.7V. the simulation result of the NOR gate is shown in Fig. 7.3(d). In case of NOR gate it is observed from the Fig. 7.3(d) that the output for the input vector [A,B]=[1,0] is not 0 volt rather it is roughly equal to 280mv. As the logic '1' is equal to 800mV so we can consider 280mV as logic '0' value. For other input combination the logic '0' or logic '1' value can be clearly visualized. So it is observed that both the logic gate gives almost satisfactory performance if the glitch that is observed in some part of the output can be ignored. The reason for this inaccurate result is attributed to the inability of single electron transistor to pass a logic '0' value.



(d)

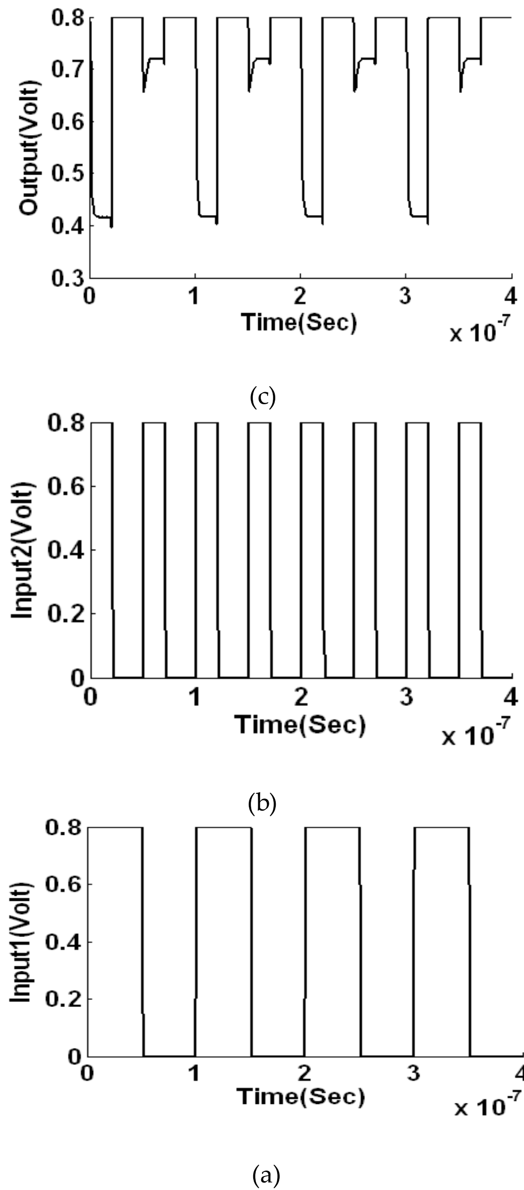


Fig. 7.3 Inputs and outputs of the transient analysis of the designed Hybrid SET-MOS pass transistor logic based Universal logic gates.(a) Input1 of the logic gates (b) Input2 of the logic gates (c) Output of the NAND gate (d) Output of the NOR gate.

7.4 Logic Function Implementation

We will implement some logic functions using hybrid SET-MOS approach. The implementation of hybrid SET-MOS logic gates using CMOS design style are already reported in the literature [7.2]. Generally the pull up network is formed using SETs and pull down network is comprises of MOSFETs. One of the very important property of SET is that we can get a n-type device (nSET) or a p-type device (pSET) depending on the back gate connection. If the back gate or popularly known as 2nd gate is connected to ground then it works as a pSET and if it connected to the power supply then it will work as nSET. We have implemented the same logic function as that was implemented using threshold logic gate so that a comparison can be drawn between these two approaches. So for reader's convenience here we are again writing the logic functions which are

F1=B′C′+A′C

F2=A′B+A′C+AB′

The complete schematic of the implementation of these two logic functions using hybrid SET-MOS approach is shown in Fig. 7.4. Three distinguished layers are clearly observed in the schematic as it is based on the programmable logic array architecture. The first layer is consists of three inverters which provides the complemented form of the

inputs. The second layer is made of four 2-input NAND gates. Finally One 3-input NAND and one 2-input NAND gates are used in the third layer. The truth table corresponding to the implemented logic functions are given in Table 7.2.

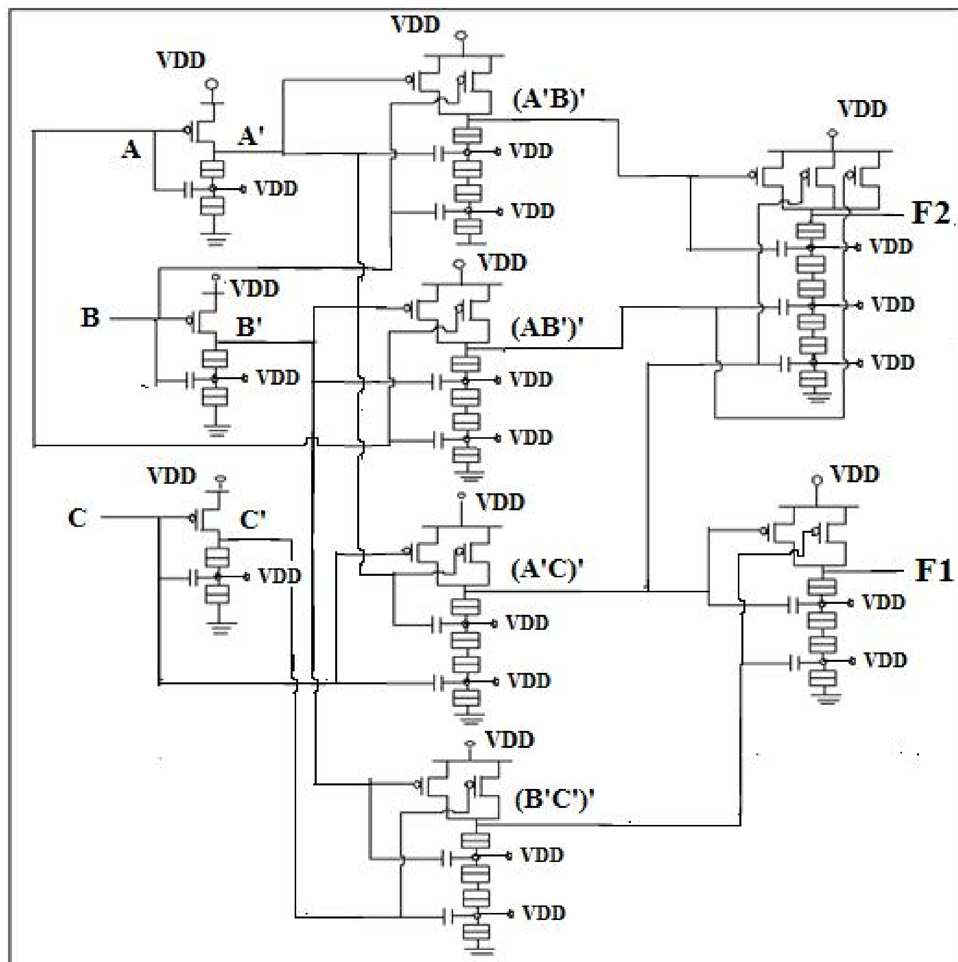
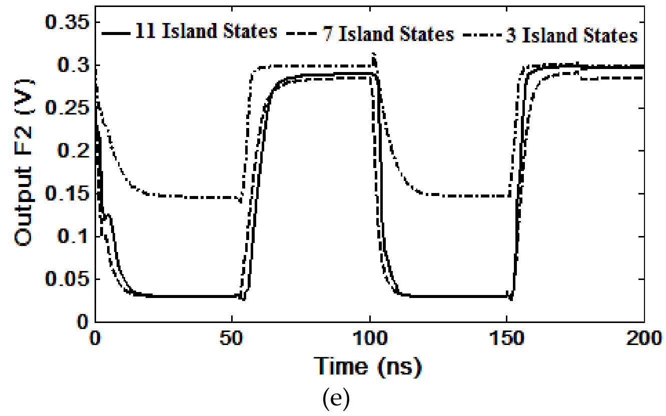


Fig. 7.4 The designed hybrid SET-MOS circuit with programmable logic array architecture implementing the logic functions F1 and F2.

Table 7.2
Truth table of the designed logic circuit with the combinational logic output functions F1 and F2, having inputs A, B and C

A	B	C	F1	F2
0	0	0	1	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

The designed logic circuit is simulated in SPICE environment, where the BSIM model of MOSFET has been used. For SET our proposed model with eleven island states have been used by incorporating it in the SPICE netlist through its verilog-A interface [15]. The proposed analytical model provides three degree of freedom regarding number of island considered during for simulation. So, simulations have been performed considering three different island states, namely level 1, level 2 and level 3 with 11 island states, 7 island states and 3 island states respectively. The simulation results have been shown in Fig. 7.5. It can be observed that the results corresponding to 11 island states and 7 island states provides are quite satisfactory. Whereas the simulation results for 3 island states are very poor for F1, even the logic '0' value may not be detected properly. This is due to the stacked architecture of three SETs in pull down network of 3-input NAND gate, which restrict



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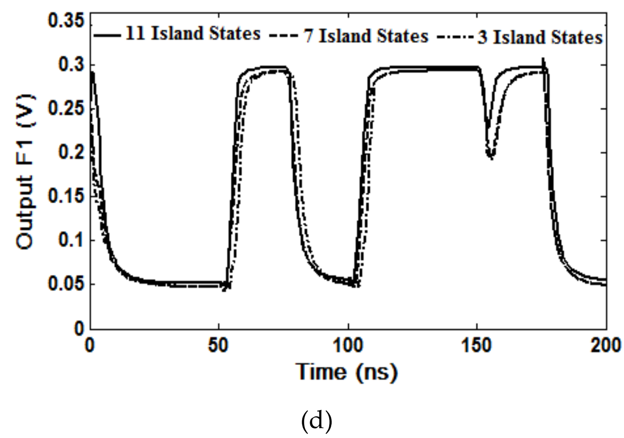

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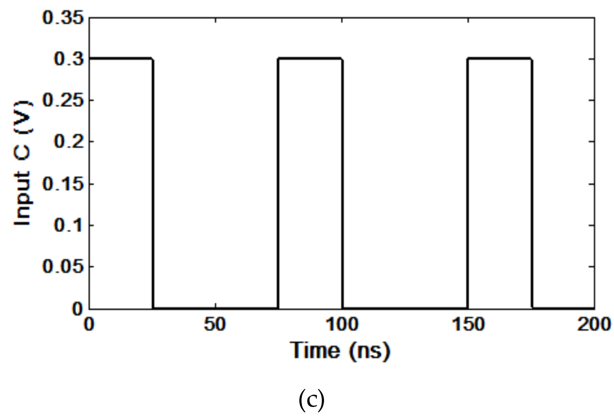

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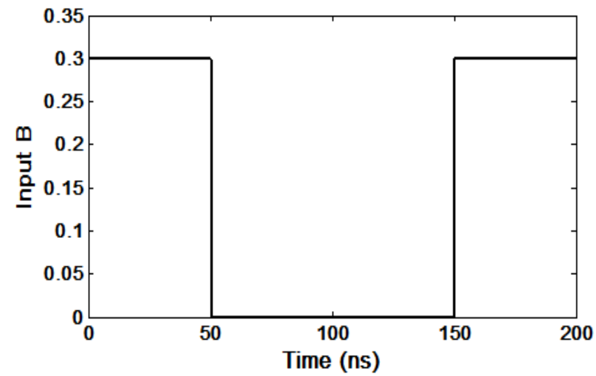

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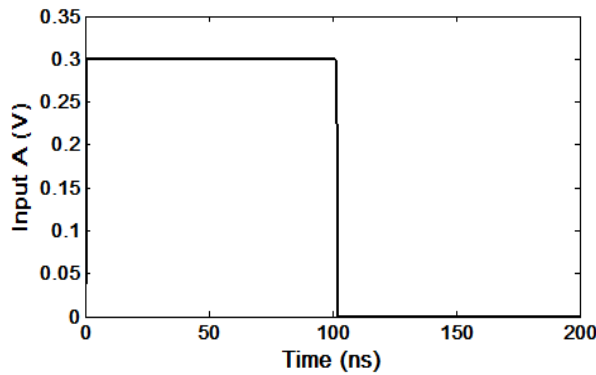


(a)

Fig. 7.5 Inputs and outputs of the designed hybrid SET-MOS circuit (a) Input A (b) Input B (c) Input C (d) Output logic function F1 (e) Output logic function F2

the logic '0' level to go more lower. Through analysis it has also been observed that with increase in the supply voltage the performance of the device with 7 island states degrades. And with 3 island states it is impossible to implement the logic functions if we increase the supply voltage.

7.5 Power and Delay Analysis

Static power consumption in single electron tunneling technology is of the order of 100pW/gate which is 4/5 decades lower than that of CMOS technology [7.16]. In single electron devices the leakage current is due to co-tunneling and thermal enhancement normal tunneling. In single electronics with increase in temperature thermal fluctuation increases but the co-tunneling events is suppressed. With increase in operating temperature the device dimension need to be scaled down but the current and voltage values increases which is in contrast to the CMOS technology [7.17]. Therefore in case of single electron devices the power delay product increases with reduction in feature size. Now for hybrid SET-MOS technology as both SET and MOSFET are present so the scenario will be a bit different. The average power dissipation is obtained as 144uw, 134uw and 89uw for 11 island states, 7 island states and 3 island states respectively. So the power dissipation increases with increase in no of island states.

Regarding the propagation delay of single electron devices the most important parameter is tunnel rate which depends on the value of the tunnel junction resistance. In case of threshold logic gate the delay is calculated considering single tunnel event which will not be applicable for hybrid SET-MOS circuits as this case multiple tunnel events occurs. Though there is a model reported in the literature for N tunnel events

[7.18] but it is not valid for hybrid SET-MOS circuits. Like CMOS technology the delay for single electron logic is not the summation of the delay of individual logic gate rather it is dominated by the logic gate with lowest equivalent tunnel rate. The average propagation delay estimated for the designed logic circuit is 3.2ns, 3.16ns and 3.3ns for 11 island states, 7 island states and 3 island states respectively. So the observable fact is though the static power dissipation varies depending on the number of island states, there is no such considerable effect is observed in delay calculation of different island states.

7.6 Performance Comparison

Finally we have made a comparison between threshold logic approach and hybrid SET-MOS approach to quantify their respective advantages and disadvantages. Table 7.3 summarizes the features of both the approaches. In case of threshold logic approach the number of basic elements is 32 whereas for hybrid SET-MOS it is 48, so threshold logic approach reduces the size of the circuit. One of the most important advantage of threshold logic approach that the supply voltage can be as low as 16mV whereas, in case of hybrid SET-MOS approach it is 300mV. As the power consumption of MOSFET is much higher compared to single electron devices so the power consumption for hybrid approach is almost 3 decades higher than the threshold logic approach. The island causes for the unreliable operation of any

Table 7.3

Comparison of threshold logic gate and hybrid SET-MOS based approaches

Logic Function implementation using PLA architecture	Based on threshold Logic Gates	Based on hybrid SET-MOS approach
Tunnel junctions	42	32
Number of islands	39	16
Number of MOSFETs	N/A	16
Total number of capacitors	70	16
Supply voltage (mV)	16	300
Temperature (K)	0	0
Voltage input for HIGH logic (mV)	16	300
Voltage input for LOW logic (mV)	0	0
Voltage output for HIGH logic (mV)	16	300
Voltage output for LOW logic (mV)	0	50
Logic levels for inputs and outputs	Active-high	Active-high
Tunnel junction resistance (Ω)	Not fixed	10e6
Tunnel junction capacitance (aF)	Not fixed	1
Gate capacitance(aF)	0.5	1
Overall circuit elements	151	80
Bias capacitor capacitance (aF)	Depends on that particular gate	N/A
Load capacitor capacitance (aF)	9	1-10
Power consumption(nW)	0.038	144(11 island states)
		134 (7 island states)
		89 (3 island states)
Average propagation delay (nS)	2.72	3.2 (11 island states)
		3.16 (7 island states)
		3.3 (3 island states)

single electronics circuits. Now as the hybrid approach reduces the number of island size to almost half of the threshold logic approach so the former provides a more reliable and stable circuit. For threshold logic based design the value of the load capacitance is fixed to 9 aF but for hybrid approach we have the freedom to chose the value between 1 aF and 10 aF. The hybrid approach shows a bit higher propagation delay compared to threshold logic approach.

7.7 Reliability and Stability Analysis of Hybrid SET-MOS Circuits: A New Approach

It has already been discussed how the reliability and stability of single electronics circuits can be analyzed using SIMON simulation software. But the same procedure cannot be applied for hybrid SET-MOS circuits. As the operating principle of MOS transistors are different than SET, so with normal approach hybrid SET-MOS circuits cannot be simulated in SIMON [7.19] or COSEC or any other single electron simulation software. The hybrid SET-MOS circuits are simulated in SPICE using macro model or analytical model of SET, but the stability analysis cannot be performed in SPICE as it depends on tunneling events. Till now to the best of our knowledge no work has been reported in the literature on the stability and reliability analysis of hybrid SET-MOS circuits. In this work an approach for stability and reliability analysis of hybrid SET-MOS circuits has been proposed.

7.7.1 Theory

In CMOS logic approach the pull up network (PUN) comprises pMOSFETs and pull down network (PDN) consists of nMOSFETs. In case of ratioed logic the entire pull up network is replaced by a load device keeping the rest of circuit same. This new logic obviously reduces number of devices used compared to CMOS logic approach. Pseudo NMOS logic is an example of ratioed logic where a PMOS transistor is used as a load [7.20] as shown in Fig. 7.6(b). The disadvantage of Pseudo NMOS logic is that as the pMOS device always remains on so there is always a current flowing through the load device which causes for static power dissipation and reduced noise margin. Now if we replace the load device by an equivalent resistor and the pull down network comprises single electron transistors only then this approach can be used for simulation of hybrid SET-MOS circuits in SIMON and for stability and reliability analysis as well.

The pMOS of the PUN can also be replaced by its large signal model, but for large circuits this approach will increase the complexity of the overall circuit. Again MOSFET can be replaced by equivalent 'ON' resistance in the linear region of operation. As the MOSFET works as a load in the proposed approach therefore it can be surely replaced by an equivalent ON resistance rather than the large signal model. The

proposed approach employing Pseudo NMOS logic where the pull up network is formed using a resistor and pull down network comprises of SETs is shown in Fig. 7.6(c).

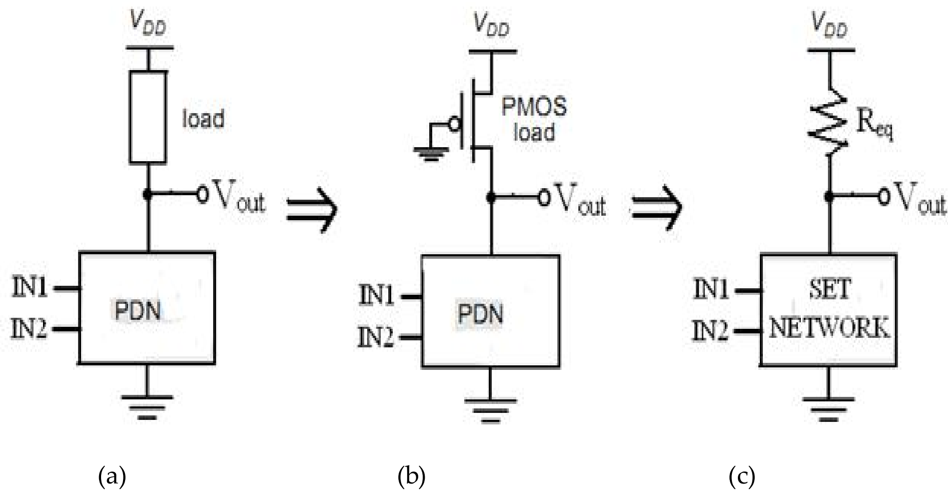


Fig. 7.6 The design approach (a) Generic (b) Pseudo NMOS logic (c) Hybrid SET-MOS equivalent circuit employing resistor R_{eq} as the equivalent circuit model.

The most important part of this proposed approach is to calculate the value of the equivalent value of the resistor which will predict the characteristics of the load device. Generally the value of this resistor denoted by Req depends on the operating point of the device. So we calculated the average value of the resistance over the operational region of interest. The value of Req is estimated as [7.21]

$$R_{eq} = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} R_{ON}(t)\,dt = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)}\,dt \tag{7.3}$$

The PMOS load will be in saturation if

$$V_{sd} \geq V_{sg} + V_T$$

This expression can be written as

$$V_S - V_D \geq V_S - V_G + V_T$$

From Fig. 7.6(b) we get, V_G=0 V and V_D=V_{out}. Considering the parameters of generic 0.25μm CMOS process [7.21] we get

$$V_{out} \leq 0.4V \tag{7.4}$$

As the supply voltage for our design is 0.1V so the PMOS load always remains in saturation. Now considering the channel length modulation (7.3) Can be written as,

$$R_{eq} = \frac{1}{V_{OH} - V_{OL}} \int_{V_{OL}}^{V_{OH}} \frac{V}{I_{DSAT}(1+\lambda V)} dV \tag{7.5}$$

Assuming V_{OH}=V_{DD} and V_{OL}= 0V, we get

$$\frac{1}{V_{DD}} \int_{0}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)} dV = \frac{1}{V_{DD} \times I_{DSAT}} \int_{0}^{V_{DD}} \frac{V}{(1+\lambda V)} dV \tag{7.6}$$

Integrating this expression we get

$$R_{eq} = \frac{1}{V_{DD} \times I_{DSAT} \times \lambda^2} \left[\lambda V_{DD} - \log\left(1 + \lambda V_{DD}\right) \right] \tag{7.7}$$

So for a specific technology the value of the equivalent resistor depends only on the supply voltage. The theoretical value calculated

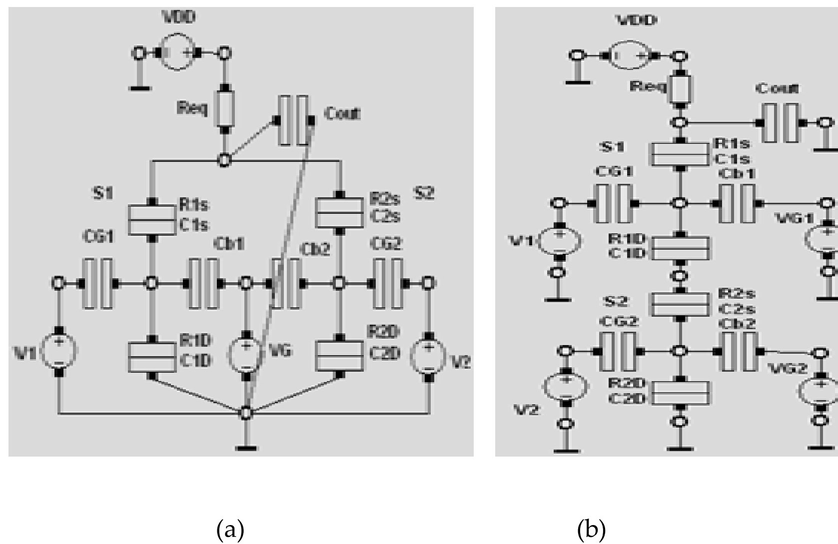
by (7.7) is a good approximation if the circuit comprises of MOS transistors only. But as our circuit comprises of single electron transistors also, we need to consider the constraints imposed by them. Following the proposed approach in case of designing a logic gate we can get two stable outputs depending on the whether the SET network in ON or OFF. If the ON resistance of the PDN is RON and OFF resistance is ROFF then the value of the Req will be limited as [7.22]

$$R_{ON} << R_{eq} << R_{OFF} \tag{7.8}$$

According to orthodox theory of single electron tunneling to localize electrons in the island the value of the tunnel junction resistance should be greater than the quantum of resistance, which is roughly equal to 26KΩ. For the accuracy the limiting value of the tunnel junction resistance is taken as 200KΩ [7.23].

Finally we have designed universal logic gates using the proposed approach as shown in Fig. 7.7. The hybrid NOR gate consists of two single electron transistors connected in parallel and one resistor representing the load device. If one or both the transistors in PDN are ON we will get a logic '0' value, which corresponds to the ON resistance of the SET network RON. As a single electron transistor is basically a connection of two tunnel junctions connected through an island, ignoring the capacitance part of the tunnel junctions SET can be roughly considered as a series connection of two tunnel junction

resistances. So for a NOR gate the value of RON is approximately equal to $4X10^5\Omega$. In case of NAND gate the SET network is formed by two SETs connected in series as shown in Fig. 7.2(b). As one single electron transistor is made of two tunnel junctions so in case of NAND gate the SET network can be seen as series connection of four tunnel resistances. the value RON for NAND gate is estimated as 1MΩ. The capacitance of the tunnel junctions are kept as small as possible [7.23] so that the design logic gates can be operated for a wide range of temperature.



(a) (b)

Fig. 7.7 (a) Hybrid NOR Gate (b) Hybrid NAND Gate

Table 7.4
Parameters of SET-MOS universal logic gates

GATE	POWER SUPPLY (V)	VALUE OF THE $R_{EQ}(\Omega)$	PARAMETERS OF SET	
NAND	0.1	2x10^{7}	S1	S2
			C_{G1}=3.2x10^{-19}F	C_{G2}=3.2x10^{-19} F
			C_{B1}=1.15x10^{-19} F	C_{B2}=1.15x10^{-19} F
			C_{1S}=5x10^{-20} F	C_{2S}=2.5x10^{-19} F
			C_{1D}=3.5x10^{-19} F	C_{2D}=8.0x10^{-20} F
			R_{1S}=3 x10^{5} Ω	R_{2S}=4.6 x10^{5} Ω
			R_{1D}=1 x10^{5} Ω	R_{2D}=8.5 x10^{5} Ω
			V_{G1}= 3.4x10^{-1}V	V_{G2}=1.9x10^{-1}V
NOR	0.1	9.75x10^{5}	C_{G1}=C_{G2}=2.9x10^{-19} F C_{B1}=C_{B2}=1.18x10^{-19} F C_{1S}= C_{1D} =C_{2S}= C_{2D}=1.0x10^{-20} F R_{1S}= R_{1D} =R_{2S}= R_{2D}=2.6 x10^{4} Ω V_G=4.5x10^{-1}V	

To compensate the operating window shrinking with increase in temperature, the ration of R_{eq}/R_{ON} have been increased [7.23]. The different parameters of the single electron transistors are selected through parametric analysis keeping in mind that the designed NAND and NOR gates can be operated between 0K and 77K. The values of different parameters are given in Table 7.4.

7.7.2 Results and Discussions

The designed NAND and NOR gates are simulated in SIMON. The outputs of both the logic gates operated at 0K and 77K are shown in Fig. 7.8. It can be observed that both the logic gates gave good results at 0K and at 77K the output of NAND gate gets slightly distorted. Even though the output is a bit distorted the overall results is satisfactory. It can be observed from table 7.2, that in case of NOR gate both the transistors have same parameter values which is attributed to the simple parallel architecture of NOR gate. But in case of NAND gate due to its stacked architecture most of the parameters of the SETs have different values.

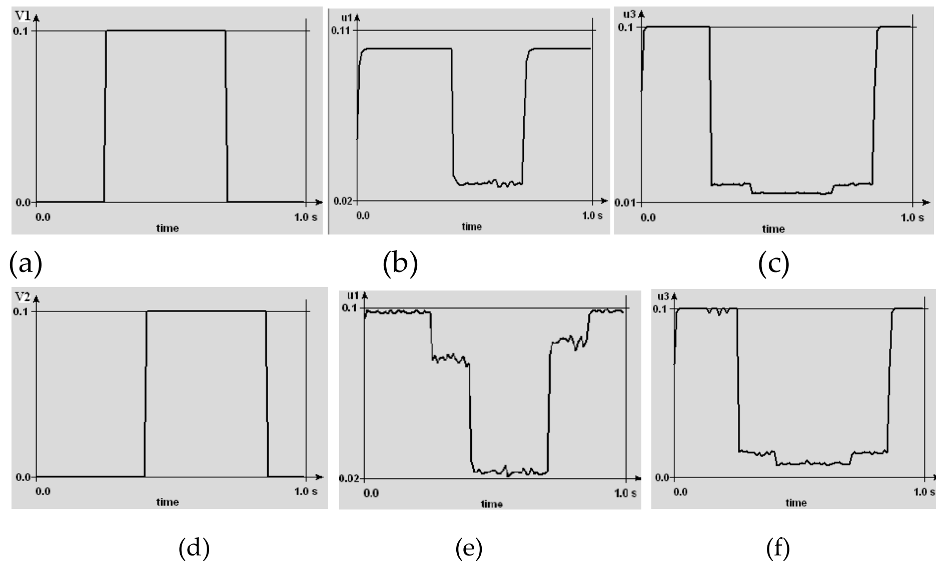


Fig. 7.8 Inputs and outputs of the designed logic gates(a) Input V1 (b) Input V2 (c) Output of the NAND gate at 0K (d) Output of the NAND gate at 77K (e) Output of the NOR gate at 0K (f) Output of the NOR gate at 77K.

7.7.3 Stability Analysis

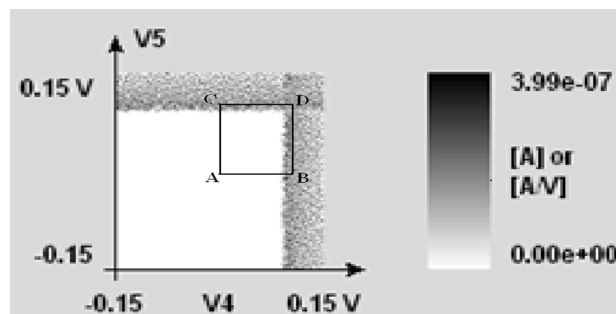
The stability of the designed universal logic gates are tested using SIMON. The main concern regarding the stability of any single electronics circuit is temperature. The first condition to observe a single electron effect is that the charging energy must be greater than the thermal energy

$$E_C = \frac{e^2}{2C} >> K_B T \tag{9}$$

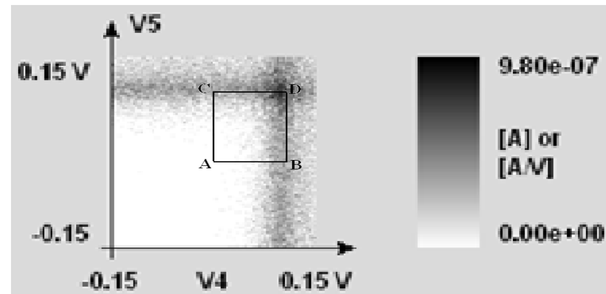
Here E_C the charging energy of the system, C is the equivalent capacitance of the island and KBT is the thermal energy. So the charging energy increases linearly with temperature. If the thermal energy becomes greater than the charging energy, electron starts tunneling due to thermal fluctuations in energy, which finally results in instability of the circuit. It can be observed from (7.9), that the charging energy depends on the equivalent capacitance of the island. So to observe a stable single electron effect at the temperature of liquid nitrogen (77K) the capacitance of the island must be smaller than 12 aF, which requires grains with a diameter smaller than 15 nm [7.24]. Therefore by keeping the value of the island capacitance below a specified value the stability of the single electronics circuits can be guaranteed. The second condition to observe a single electron charging effect is that the electron should be localized in the island so

that the quantum fluctuations on the island can be neglected. As already explained to solve this issue we have considered tunnel junction with resistance much higher compared to quantum resistance so that co-tunneling can be neglected.

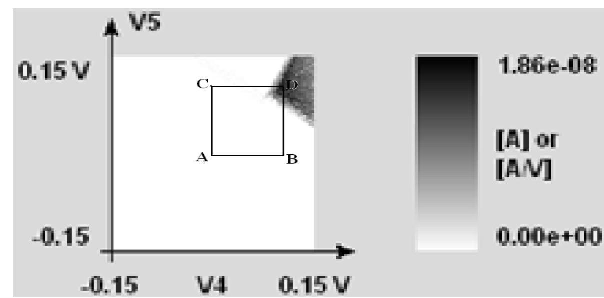
The effect of temperature on the stability of SET is investigated at 0K and 77K and the corresponding stability plots are shown in Fig. 7.9. The local minima of circuit's free energy represents a stable condition and these points are coloured in white. Whereas local maxima of circuit's are free energy corresponds to unstable condition and are coloured black. The rest of the points are coloured in grey which denotes a very small current flowing through the junctions. The four points corresponds to input control signal vectors [0, 0], [0, 1], [1, 0] and [1, 1] are marked as A, B, C and D respectively. It can be observed that for both Fig. 7.9(a) and (b), point A [0, 0] lies in the stable region whereas for rest of the points, B [0. 1], C[1, 0] and



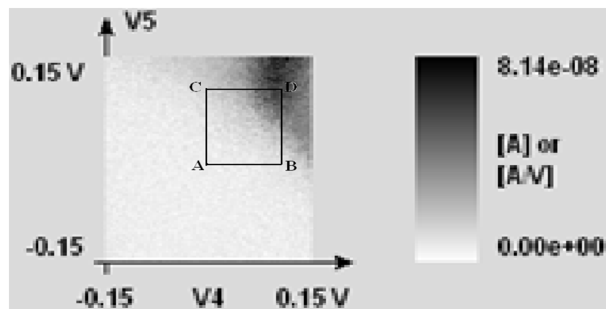
(a)



(b)



(c)



(d)

Fig. 7.9 Stability Plots using SIMON with A[0, 0], B[0,1], C[1,0], D[1,1] points corresponding to four input signal vectors for (a) NOR gate(0K) (b) NOR gate(77K) (c) NAND gate(0K) (d) NAND gate(77K).

D [1, 1] a very small current flows through the circuit. It is also observed that for Fig. 7.9(a) to 7.9(b) the free energy of the black coloured points increases from $3.99X10^{-07}$ to $9.80X10^{-07}$ which indicates that the tunneling event increases with increasing in temperature and thereby decreasing the stability of the circuit. As observed from Fig. 7.9(c), in case of NAND gate at 0K all the points except point D are in stable region. Almost same is observed at 77K also but some grey point are observed near points B and C as seen in Fig. 7.9(d). So finally it is concluded that for the designed logic gates only point A [0, 0] represents stable point both at 0K and 77K. For other combination of inputs the designed circuits are not completely stable and a very low current flows through the circuit. The maximum free energy for NOR gate is $9.80X10^{-07}$ which is higher compared to the maximum free energy of NAND gate, $8.14X10^{-8}$. So the number of tunneling events is higher in case of NOR gate which is attributed to the simple parallel structure of NOR gate compared to the stacked architecture of NAND gate.

7.7.4 Reliability Analysis

Reliability is one of the most important issue in single electronics technology. During fabrication of single electron devices random charges or trapped charges are formed on the nodes of single electron devices which is popularly known as background charges. As these

charges are randomly distributed in the substrate near the island or near the tunnel junction so it is impossible to describe them microscopically. Researchers have come up with different model of background charges, considering different approximations to analyze the effect of these charges on single electron devices. Abramov et al proposed three models which can be incorporated in 2D numerical models to capture the effect of these charges [7.25]. The most commonly used model of background charges represents them as constant, $Q_0 = N^{0\prime}e$, where e is elementary charge. This model of background charge has been accepted by semi classical model [7.26, 7.27] and also by the well established analytical model [7.28].

The trapped charges creates extra voltage which actually changes the total voltage across the junction. If this change in voltage makes the junction voltage overcome the critical voltage of the junction then it forces an electron tunnel across that junction which eventually causes the unreliable operation of the circuit [7.29]. As these charges are random in nature so we have considered two very commonly used distributions namely uniform distribution and normal distribution to characterize them.

Assume the background charges are uniform distributed over all the nodes in the designed circuit, given by

$$p\left(\frac{z}{q_e}\right)=\begin{cases}\frac{1}{2\eta}, -\eta \le \frac{z}{q_e} \le +\eta \\ 0, otherwise\end{cases} \tag{7.10}$$

Here Z is the random variable, qe is unit charge and η is the variation factor. The range of the random variable is $\pm\eta q_e$.

2. the random charges can also take normal distribution with standard deviation σ, represented as

$$p(z1) = 1/(\sqrt{2\pi}\sigma)e^{-\frac{Z_1^2}{2\sigma^2}}) \tag{7.11}$$

Here Z1=Z/qe, and Z is the random variable. According to three sigma rule or empirical rule of statistics for normal distribution almost all the values lie within three standard deviation of the mean. So following this rule the value of the standard deviation is considered as $(\sigma / q_e) = \eta / 3$. The reliability of the designed NAND and NOR gates are analyzed at 77K considering different background charge values as shown in Fig. 7.10 and 7.11 respectively. The results of both the distribution are plotted in the same Figure So that a comparison can be drawn. It is observed that with increase in variation factor the reliability of the logic gates decreases almost linearly. The uniform distribution provides better reliability compared to normal

distribution. Both the logic gates shows almost same reliability characteristics with the lowest reliability as 60%.

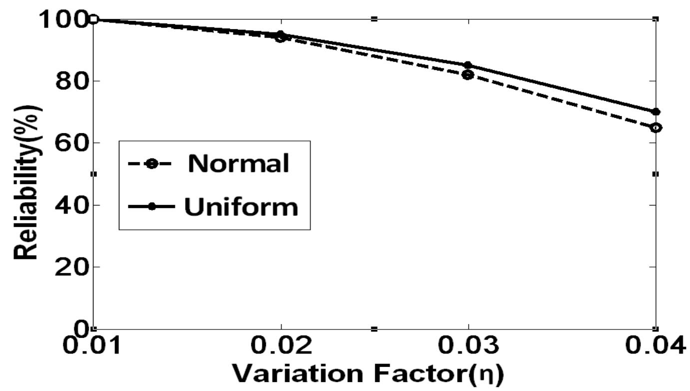


Fig. 7.10 Reliability of NAND gate at 77K with normal and uniform distribution of background charges.

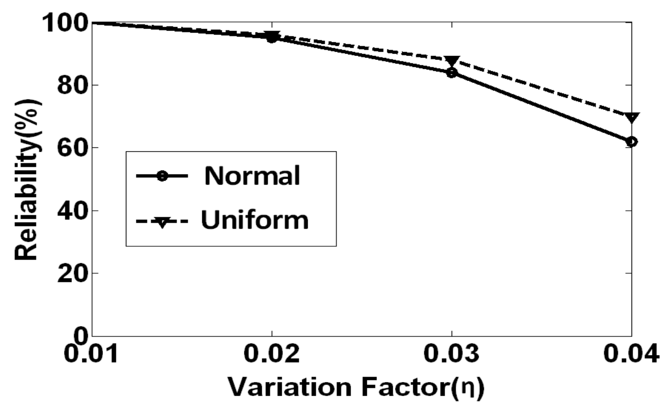
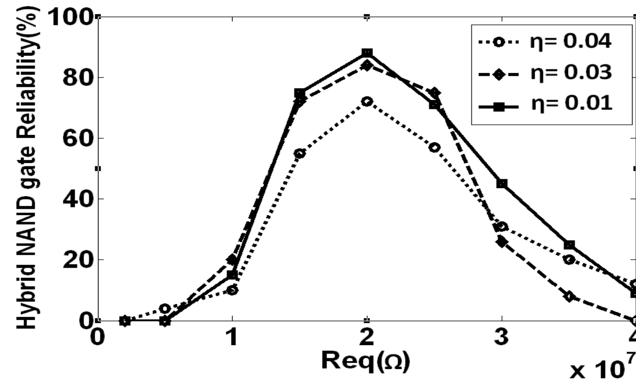
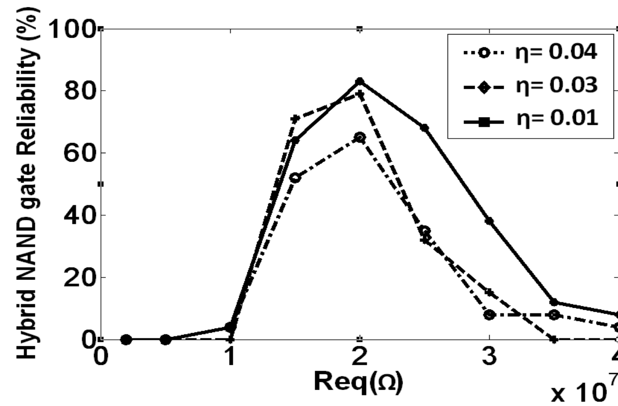


Fig. 7.11 Reliability of NOR gate at 77K with normal and uniform distribution of background charges



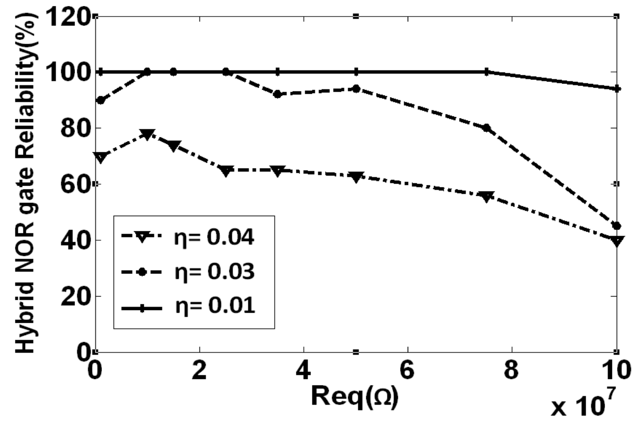
(a)



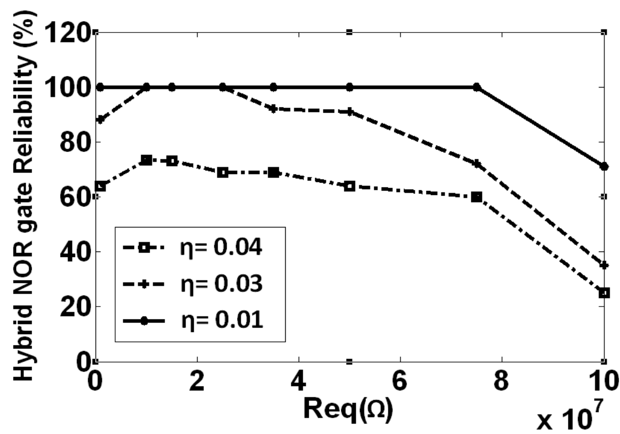
(b)

Fig. 7.12 Reliability Vs R_{eq} curves for Hybrid NAND gate with (a) normal (b) uniform distribution of background charges for the values of variation factor 0.04, 0.03 and 0.01.

We have further investigated the effect of Req on the reliability of the designed logic gates. The effect of Req on the reliability of NAND gate is plotted in Fig. 7.12. It can be observed that initially the reliability is very low, which starts to increases with increase in Req, attains a peal value and again starts to decrease. So to get good results for NAND



(a)



(b)

Fig. 7.13 Reliability Vs R_{eq} curves for Hybrid NOR gate with (a) normal (b) uniform distribution of background charges for the values of variation factor 0.04, 0.03 and 0.01.

gate the value of Req should be in the middle of the range. It is observed that for NAND gate the best reliability is obtained at Req = $2X10^7\Omega$ which is used in our design purpose. Also the reliability of

more than 50% can be obtained if the value of Req is kept between $1.7X10^7\Omega$ and $2.4X10^7\Omega$. The NOR gate shows a much simpler reliability characteristics as shown in Fig. 7.13. For NOR gate with variation factor 0.01 the reliability is almost 100% for the entire range of operation. For other values of variation factor up to Req = $8X10^7\Omega$ the reliability doesn't change much, but after that it decreases drastically.

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Chapter 8

Concluding Remarks and Future Scope

8.1 Concluding Remarks

In the present work we have explored the capabilities of single electron tunneling technology by designing and implementing various single electronics circuits. we have proposed different model for single electron transistor and verified them by using these models to design different circuits. Reliability and stability of the designed circuitis thoroughly analyzed. Finally different hybrid SET-MOS circuits are designed and implemented. In this chapter we have concluded the wotk.

In this work an improved macro model is reported for efiicient simulation of single electronics circuits. The novelty in the work lying with the incorporation of a voltage controlled current source to imrove the couomb blockade part of the characteristics. Various fitting parameters are included in the model to make it more accurate. Also some scalling factors are included which works as a degree of freedom to switch between symmetric and asymmetric SET and helps to scale the drain current. the comparison with other simulation methodologies

shows that the results of our model closely matches with that of the popular simulation software SIMON. Finally a inveter is designed using the proposed model. It was found that amonf all the parameters RG affects the noise margin of the inver most. The noise margin improves with increase in the value of RG, and the best result is obtained for RG=50GΩ. the designed multi peak NDR circuits work well under the bias conitions. The parameters CR1, CR2 and RG have the maximum effect on the characteristics of the designed NDR circuit. While CR1 and CR2 affects the shape of the characteristics curve, RG controls the number of NDR regions. the integrator ciruit also work fine. The harmonic distortion and intermodulation distortion is measured as 2.94% and 1% respectively. So it can be concluded that the designed circuits are highly immune to any kind of distortion.

A compact analytical model for single electron transistior is developed using master equation method, based on the orthodox theory of single electron tunneling. Total eleven island states have been considered in the proposed model to imrove its accuracy. From the simulation results the coulomb blockade effect and coulomb oscillation characteristics are clealy observed for both symmetric and asymmetric single electron transistors. the simulation results are verified by comparing it with the results obtained from the Monte Carlo simulator SIMON. The model with n=1 and level 1 (five states on both side of the

optimum value) gives the best result. the coulomb blockade effect gradually disppaers with increase in temperature. The model is written in verilog-A language so that it can be incorporated in the SPICE environment to cosimulate SET-MOS devices. The proposed compact analytical model with eleven island states works very well for the designed inveter and NAND gate. The comparison with other existing simulation approaches shows that our model gives the best result with the maximum drain current coverage.

In the existing model for delay analysis the calculation is based on the error probability value, which is a probablistic value and no standard value for this is yet reported in the literature. In this work we proposed a method for error probability independent delay analysis of single electronics circuits that considers multiple tunneling events. Based on the orthodox theory and poison distribution, initially the probability distribution function and then the equation to calculate the delay is thoroughly derived. The delay for inverter and universal logic gates are completely analyzed. It is found that the propagation time for logic high to low transition is different from low to high transition. The comparison with other approaches clearly shows that the proposed method outperforms the existing approaches in both simplicity and accuracy.

A 4:1 multiplexer has been designed using threshold logic approach. Buffer threshold logic gates are used in the design to reduce feedback effect and to increase the stability. The circuit remains highly reliable for both of the distribution upto the variation factor value of 0.2. After that the circuit becomes unreilble for uniform distribution of background charges. Stability plots have been shown for different temperatures and it is observed that the stability degrades with increase in temperature. Then design, implementation and analysis of some logic functions are presented using this approach. Programmable logic array architecture is used to implement the circuit. The logic operation is verified using SIMON. The stability plots for different input combinations shows that the design circuit is stable for the specified voltage range. The power consumption is measured as 0.038nW. the average propagation delay is estimated as 2.72ns. a neuron cell based on threshold logic gate is proposed. It has been shown how the capacitive weight can work as synapses without adding any extra circuitry to the design. The activation function for the design neuron cell is thoroughly derived. Then the proposed neuron cell is used to design a 3 cell shadowing CNN circuit. It is investigated that the designed shadowing circuit works well upto temperature of 15K, after thet the stability degrades due to increase in thethermal fluctuations of energy. The reliability analysis reveals that the circuit is

more reliable for uniform distribution of background charges compared to the uniform distribution.

To compensate for the drawbacks of the single electron tunneling technology, a novel SET-MOS hybrid technology is used to design and implement various circuits. Universal logic gates are designed, implemented and analyzed using hybrid SET-MOS based pass transistor logic. Higher values of tunnel junctions are used to increase the range of operative temperature. The designed logic gates are found to work satisfactorily. Next the same logic functions that are implemented using threshold logic approach are designed using hybrid SET-MOS approach. The performance of the circuit is analyzed for different number of island states. It is observed that the circuit with 11 island states performs better than the 7 and 3 island states. Also it is realized that with increase in temperature the number of island states need to be increased for proper operation of the circuit. The power consumption is three decades higher than that of threshold logic circuit.

8.2 Future Scope

Some significant improvement have reported thorough our research work, but still threre are room for improvement and challenges in

single electron tunneling technology as well as in hybrid SET-MOS technology. following future scopes are proposed for further progrees:

1. Though we have developed macro model or analytical model of single electron transistor for better simulation of single electronics circuits but we need to modify this model or proposed new models which can be used to simulate circuits in room temperature.
2. The proposed delay model is suitable for single electronics circuits but we also need delay model for hybrid SET-MOS circuits as well.
3. Till now we have mostly concentrated on the digital applications of single electron tunneling technology but to think of it as a successor of CMOS technology we need to explore the applicability of this technology for analog circuits also.