PERFORMANCE IMPROVEMENT FOR FUTURE NANO DEVICES AND EXPLORE SOME OF THEIR APPLICATIONS

THESIS

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[2]. Analytical Model for performance comparison of a nano scale dual material double gate Silicon on insulator SOI and Silicon on nothing SON

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CERTIFICATE FROM THE SUPERVISOR

This is to certify that the thesis entitled " ***Performance Improvement For Future Nano Devices and Explore Some of Their Applications*** *" submitted by Shri* ***Pranab Kishore Dutta,*** *who got his name registered on 30.04.2013 for the award of Ph.D (Engineering) degree of Jadavpur University is absolutely based upon his own work under the supervision of* ***Prof.(Dr) Subir Kumar Sarkar*** *and that neither his thesis nor any part of the thesis has been submitted for any degree / diploma or any other academic award anywhere before.*

[Subir Kumar Sarkar]

Signature of the Supervisor

and date with Official Seal

Dedicated to

My Parents

Kamal Chandra Dutta,

Saroj Kumari Dutta

For their motivation

&

My Wife

Purabi Tamuli Dutta

For her support and cooperation

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ABSTRACT

Continuous demand for performance improvement of the device haves shepherd semiconductor industry to miniaturization of the MOS device. After more than forty decades of scaling of the device it comes to its limitation. To continue the process of scaling urgent innovation for new and innovative device structure with new material for MOS is required. Short channel effect is the main hinder for further scaling of bulk MOSFET. Development of crystal growth technique has provide Silicon-on-Insulator (SOI) MOSFET to semiconductor technology. It is a new innovative device which use buried oxide layer in between the channel and the substrate to overcome the different type of parasitic capacitance effect. The use of double gate and then enhance by dual metal double gate allow to reduce the size of the device to thin level. Dual metal double gate use the concept of gate engineered to have a precise control of gate over the channel. The performance of the device is further enhance by using air as a buried layer which will reduce the capacitance of the buried layer and make it more efficient in terms of speed, size and power consumption. The new device is Silicon-on-Nothing (SON) MOSFET. The implementation of work function engineered DMDG SON MOSFET transform the size of the device to level of ultra thin dimension. The ultra thin device dimension will generate some critical issues for the recent semiconductor device, such as increase of source drain region, quantization of carrier and gate oxide breakdown. A proper analysis and modeling of device is required with reference to the above critical issues to provide a better

performance in terms of low threshold voltage, drain current, further scaling and its application to VLSI circuit.

This thesis work incorporate different novel DMDG SON device structure with analytical modeling for potential profile, threshold voltage and drain current considering the increase of source/drain resistance, quantization of carrier and gate oxide breakdown for performance improvement of nano device.

In order to meet the future demand for nano device, researcher has to look beyond CMOS. Single Electron Transistor (SET) is such a device which can control the flow of single electron. MOS the most regularly use present semiconductor device is complementary to SET. So use of the hybrid SET-MOS circuit utilizing the benefit of both SET and MOS will be one of the future generation nano circuit. So the thesis also consist an application of hybrid SET-SOIMOS circuit.

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List of Abbreviations

VLSI	Very Large Scale Integration
ULSI	Ultra Large Scale Integration
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
SCE	Short Channel Effect
DIBL	Drain Induced Barrier Lowering
SG	Single Gate
DG	Double Gate
DMG	Dual Material Gate
DMDG	Dual Material Double Gate
DGFET	Double Gate Field Effect Transistor
DMGFET	Dual Material Gate Field Effect Transistor
SOI	Silicon on Insulator
FD SOI	Fully Depleted Silicon on Insulator
PD SOI	Partially Depleted Silicon on Insulator
SON	Silicon on Nothing
BL	Buried Layer
BOX	Buried Oxide
SOV	Silicon on Void
ESS	Empty Space in Silicon
SED	Single Electron Device
SET	Single Electron transistor

RTD	Resonant Tunneling Diode
Si	Silicon
SiO	Silicon Oxide
ZO	Zirconium Oxide
NWFET	Nano Wire Field Effect Transistor
WFEG	Work Function Engineered Gate
2D	Two Dimensional
3D	Three Dimensional
2DEFG	Two Dimensional Electron Gas
EOT	Equivalent Oxide Thickness

Chapter 1

INTRODUCTION AND ORGANIZATION OF THE THESIS

1.1 Introduction.

Semiconductor industry can sustain in the state-of-the-art device for its ability to distinguish itself by the fast pace of improvement of its product. The quadruple increase of transistor per chip every two years, the famous Moore's law predict by Gordon Moore [1.1] is taken as a benchmark for the semiconductor industry and followed for more than four decades. The modern silicon based electronic gadgets like personal computer, mobile, high-definition digital TV, high speed internet can be realized due to striking progress in Ultra-Large-Scale Integration (ULSI) technology. The feature of scalability in complementary metal oxide semiconductor (CMOS) device [1.2]-[1.5] act as a catalyst for the tremendous improvement of microelectronics technology. Reducing gate length, gate dielectric thickness and increasing the channel doping in the conventional scaling technique used for planner metal oxide field effect semiconductor (MOSFET) may not be sufficient to maintain the frantic pace imposed by Moore's law. To control the short channel effect (SCE), planner MOSFET requires high channel doping, and the results are degradation in carrier mobility and high leakage power consumption. Advanced and new device

structure should replace the planner MOSFET to maintain the pace of development in the semiconductor industry. Multigate gate device, ultra thin fully depleted silicon on insulator (FDSOI) and silicon on nothing (SON), high-k are some of the new and innovative research which leads to new device structure [1.6]. New development in semiconductor industry always push the researchers to go for new innovative approach and sometimes force to look beyond CMOS[1.7].

Realization of small size, high speed and low power consumption device and system are the grail of our present research fraternity. Different modeling approaches are there to understand the performance improvement of the device due to ballistic or quasi-ballistic transport and technology booster which involve strain, thin Silicon On Insulator (SOI) architecture, SON, high-k dielectric [1.8]-[1.11]. Threshold sensitivity to channel length and drain induced barrier lowering (DIBL) for sub 100nm device can be reduced somewhat with the use of SOI double gate (DG) MOSFET model [1.12]. Double gate (DG) is a novel structure evolve from regular MOSFET structure with placing the second gate below the thin body channel. The two gate make the device more effective in preventing the drain electric field lines reaching the source. Hence reduce the short channel effect. Volume inversion in DG MOS enhance the number of minority carrier and increase in carrier mobility are some of the advancement in DG MOSFET. Increase in carrier mobility and enhancement of minority carrier will finally increase the drain current and transconductance [1.13],[1.14]. Dual Metal Gate (DMG) is another novel structure which evolves from using two metal gate with different work function placing side by side and considering as a single gate. The surface potential

profile will be in the form of step which will reduce the 2D charge sharing effect and in turn, will increase the carrier transport efficiency [1.15]. Incorporating DMG in SOI MOSFET will reduce the SCE in deep submicron regime. The Dual Metal Double Gate (DMDG) MOSFET [1.16] include the benefit of both DG and DMG MOSFET and becomes most prominent device structure in sub 100nm range. The everlasting requirement of improved electronics gadgets in terms of speed, cost, power and compactness of the product forces the semiconductor industry for miniaturization of the device. According to ITRS 2013 [1.17] anticipation, the physical dimension of the transistor will be around 10nm threshold by the year 2020-2025 and to support this the physical gate length will be changed from 32nm(2008) to 5nm (2028). The MPU/ASIC half pitch and gate length trends in ITRS 2013 have been representing by figure 1.1. Novel device structure with new methodologies and material can be a possible solution for the above consequence as predicted by ITRS 2013.

As the dimension reduces an important phenomenon called quantization of carrier will prevail in the device characteristics [1.18],[1.19]. So quantum effect consideration becomes an important parameter in the analysis of the device characteristics. The miniaturize of the device structure will also scale down the oxide layer and its start the breakdown of the oxide layer. Reliability concerns [1.20] and tunnel leakage current [1.21] are the some of the problems arises due to the breakdown of the oxide layer. These problems can be somewhat reduced by using new material. To meet the future demand of improved device performance in VLSI/ULSI circuit in terms of reduced power, device density and speed researcher has to explore in the field

combining device scaling with new non-classical device structure and/or new materials considering different functional limitation set up by manufacturing physics.

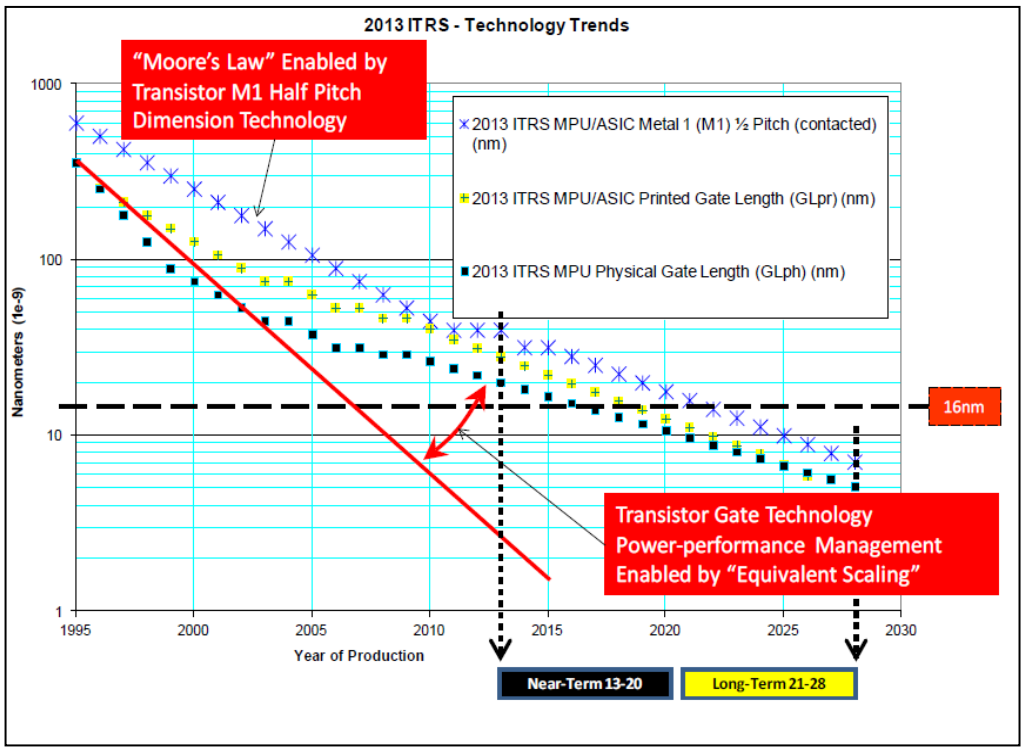

Fig. 1.1 The MPU/ASIC half pitch and gate length trends in ITRS-2013.

1.2 Recent work on the relevant area.

Modern days metal oxide semiconductor was first reported by E.H.Snow et al. [1.22]. Although it was first described by J.E Lilienfield [1.23] and later by D.Kahng et al [1.24] with silicon, but this was not viable due to the absence of routinely growing reliable oxide. Scaling down the size of the MOS device and increasing the number of

transistor in a single chip is the simple concept of semiconductor technology to satisfy Moore's law [1.1]. The advances in low temperature annealing and lithography has scaled down the MOS transistor from several microns to less than 100nm in last three decades. Short channel effect such as drain-induced-barrier-lowering, surface scattering, threshold voltage roll off, velocity saturation and hot electron effect [1.25] limits the scalability of planner bulk MOSFET. Recent advances in crystal growth technology has opened up new possibilities in the field of non-classical structure such as Silicon-On-Insulator (SOI) MOSFET, Silicon-On-Nothing (SON) MOSFET, FinFET or nanowire MOSFETs that overcome the device scaling difficulty [1.26]-[1.28].

Scaling of the conventional planner CMOS device suffers from various SCE and other drawbacks such as gate tunneling, boron penetration, reliability issues of the device, etc. SOI MOSFET is a non-conventional MOSFET structure which can reduce the problem of SCE in the deep submicron regime. Superior electrical characteristics, compatibility with bulk MOSFET, easier fabrication feasibility, and progress in the separation of implantation of oxygen technology make it much sought after device in early 2009 [1.9]. Reduce junction capacitance, high radiation tolerance, lower propagation delay, improved sub-threshold characteristics, suppressed short channel effect, etc. are some of the advantage of FDSOI [1.29]-[1.31] which makes it a prominent device for 16nm technology. Structural modification on FDSOI will innovate it to new generation silicon MOS transistor. Analytical modeling of the device is very much important before going for fabrication of the device. A current-voltage model for

FDSOI was proposed by Tommy C. Hsiao et al considering the effective depleted charge on the drain bias, source drain series resistance, voltage drop in the substrate region, DIBL [1.32],[1.33]. The threshold voltage roll-off is reduced in FDSOI [1.34], and the saturation current is enhanced which will reduce the static power consumption [1.35]. Dual-Material Gate Field Effect Transistor (DMGFET) generic structure [1.36] will provide rapid acceleration of charge carriers and suppressed short channel effect due to the difference in work function of the material with a more positive voltage near the source than the drain. DMGFET was designed based on the earlier research of dual gate [1.37], split gate [1.38] and Hetero Material Gate Field Effect Transistor [1.39]. Scaling of the device to ultra-short channel SOI MOSFET will have a problem related to self-heating series resistance, velocity overshoot, etc. J.B.Roldan et al. [1.40] provide analytical current voltage expression for circuit simulation. The concept of the asymmetric gate to source side and symmetric gate to the drain side was proposed by Zhou [1.41] for the first time. The utilization of n^+ and p^+ polysilicon as gates materials in asymmetrical double-gate (DG) CMOS for better performance in terms of symmetrical- gate counterparts was first proposed by Keunwoo Kim and Jerry G. Fossum [1.42]. The use of two metal with different wok function will control the electric field near the drain region [1.16],[1.43]. This rise the concept of DMDG MOSFET. The rise in the difference of work function in the two metal will decrease the electric field near the drain which will, in turn, decrease the electron velocity at the drain end, and that reduces the hot electron effect. The basic idea for the internal design of a tri-material gate FD SOI MOSFET can be obtained by a solution of 2D

Poisson's equation for the two-dimensional potential profile, sub-threshold conduction, threshold voltage [1.44]. The concept of graded channel misaligned double gate FDSOI MOSFET was reported by Rupendra Kumar [1.45] with two dimensional analytical sub-threshold model used for accurate prediction for different parameters of the device. Several analysis and model are proposed for unphysical behaviors near the flat band voltage, silicon junctionless MOSFET, suppression of floating-body effect for improvement of SOI MOSFET device [1.46]-[1.48]. Further improvement of the SOI MOSFET device in terms of performance can be achieved, if the buried layer of SiO_2 is replaced by a dielectric layer of low permittivity normally of '1' (air). A new device will exist with nomenclature Silicon-On-Nothing (SON) [1.28],[1.49]. The lower permittivity of buried layer will reduce the buried capacitance of SON and effectively reduce the coupling between drain and the source through the buried layer. This phenomenon will reduce the DIBL. The sub threshold behavior of the ultra thin SON device is improved which provide a high speed low voltage and low power device. SON from St-Microelectronics [1.50], Silicon-On-Void (SOV) [1.51], Empty space in Si (ESS) [1.52] fabrication shows the practical feasibility of SON device. To improve the threshold voltage model B.Svilicic et al. [1.53] use the fringing field lines between source/drain and channel region through the buried oxide layer to develop a novel vertical fully depleted SON MOSFET. The concept of work function engineering gate in terms of mole fraction variation of the binary metal gate electrode of DMDG has been implemented in SON device to control the threshold voltage of the device [1.54]-[1.56]. S.Deb et al [1.57] proposed the idea of continuous

mole fraction variation in a binary metal alloy gate for SOI MOSFET. This idea was implemented in SON structure by Bibhas et al. [1.58], which shows that there is an improvement in the performance of the device in compared to SOI MOSFET. Scaling down the device to the deep 100nm regime will create ultra thin source/drain region which results in larger series resistance effects. Larger series resistance will reduce the drain current driving capability. The problem arises because of ultra thin drain/source region can be overcome by using recessed source/drain structure [1.59],[1.60]. The dominance of SON MOSFET over the other counterpart, motivate us to apply recessed source/drain structure deeper into a buried layer in SON structure.

Reduction of device dimension excessively will provide a low dimensional device, but it will come along with different short channel effect and other parasitic effect. To reduce the short channel effect and improve the performance of the device, the channel doping should be increased with reducing oxide thickness. The consequence of this in MOSFET will have a very high vertical electrical field [1.61]. The high electric field in an ultrathin Silicon layer will rise to carrier quantization. Quantization of carrier will generate quantum well at Si/SiO_2 interface, and quantum confinement effect comes into the present. The constraint in the analysis by classical approach will be evident when the gate leakage increases on the decrease of oxide thickness below 1.2nm [1.21], [1.62]-[1.64].

The classical theory says that the carrier density is in peak value at the Si/SiO_2 interface, but quantum mechanics explanation is antilogous to it, i.e. carrier density at Si/SiO_2 interface is forced to vanish. So by the influence of quantization effect, the carrier

distribution will be displaced towards the substrate. Hence the electric characteristics are modified by the classical approach, and these changes should be envisaged to the analysis in the deep sub-micron regime. The impact of quantum effect can be seen on the threshold voltage, mobility of the carrier, capacitance and drain current. This also put a limit in the scaling of the device [1.64]-[1.66]. The introduction of new material along with new architecture are required to break the scaling barriers [1.67]. DMDG MOSFET is one of the prominent candidatures to overcome the barrier [1.16]. As the device dimension can be compared with de Broglie wavelength heavy doping in the channel is required to reduce the short channel effect. The heavy doping in the channel will degrade the carrier mobility, and quantum mechanical effect comes into existing. This ultra thin device structure will be subjected to structural confinement along with transverse electric field induced quantum confinement. So quantum mechanical effect consideration on the drain current is quite important in the compact modeling of DMDG MOSFET.

The progress of device scaling has reduced the gate dielectric to an ultra-thin layer. The shrinking of the oxide layer will rise the leakage current due to quantum mechanical tunnel effect [1.21]. The electron tunneling between gate and channel can be reduced by increasing the potential barrier between channel and gate. This is achieved by making dielectric thicker in space or higher in energy. Conventional Silicon-di-oxide (SiO_2), because of its passivation, high insulation and process compatibility with Silicon has been used widely. But as it oxide layer becomes thinner, SiO_2 cannot withstand the leakage tunneling current. Further scaling of MOSFET device with SiO_2 as dielectric reaches it

limits. The high-k dielectric material is a possible solution to break the limit of scaling [1.68],[1.69]. The improvement in the oxide thickness will be equivalent to the ratio of the permittivity of high-k dielectric to the permittivity of SiO_2. This means that a high-k dielectric of 'n' times larger dielectric constant than SiO_2 will have oxide capacitance n times larger for equivalent oxide thickness. The increase of the effective thickness of high-k dielectric will overcome the drawback of SiO_2 in terms of leakage current. Hafnium di-Oxide (HfO_2) with a high dielectric constant of 22-25[1.70], band offset larger than 1.4eV and band gap of 5.6eV[1.71] is a potential candidate to replace SiO_2. Moreover, its thermal stability when contact with silicon is quite satisfactory with lower trap density [1.72],[1.73]. The time for breakdown also increases in case of hafnium oxide due to its ability to withstand dynamic stress for long time in MOS device [1.74]. This motivate us to use HfO_2 as dielectric oxide layer and analysis the threshold voltage and drain current of an ultra thin DMDG SON MOSFET.

The performance improvement of the device will have practical importance if it is analysis from an application point of view. Scaling of the device deep below sub 100nm regime make CMOS device unfeasible [1.9].[1.21],[1.62],[1.64] due to different SCE, gate leakage and drain resistance. Single Electron Transistor (SET) a nano feature size [1.75],[1.76] device beyond CMOS which can be endorsed for future nanodevice [1.7],[1.76],[1.77]. Low power dissipation and compatible with CMOS [1.78] makes its most prominent candidate to replace CMOS. But due to its deprive of some important MOS feature like voltage gain, current drive, high speed and high temperature operation it cannot completely replace MOS from CMOS structure. A

hybrid of SET-MOS [1.79],[1.80] will utilize the advantage of both SET and MOS structure. The modification of MOS in terms of SOI MOS in hybrid SET-MOS architecture can further improve the performance of the circuit.

The above relevant work, motivate us to explore for the new innovative model in nanodevice dimension which will take care the problem of series source/drain resistance, quantization and gate oxide breakdown of conventional SiO_2.

1.3 Organization of the thesis.

The thesis has been organized in four different work related to performance improvement of nano device along with brief literature to nanodevice and end with a conclusion. The conventional scaling of the device takes place in three dimensions, gate length, gate dielectric thickness and Silicon film thickness. Scaling of the device in this dimension will make the device ultra thin. The ultra thin device will arise different problem which limits the bar of scaling. The problem is due to the increase of series source/drain resistance, quantization of the carriers and leakage through the gate dielectric. This also forces us to think something beyond CMOS. The thesis is organized based on the above parameter which tries to provide a solution for future nanodevice.

Chapter 2 introduces the concept of basic of nanodevices structure. The theory of quantum consideration, high-k dielectric, SET are discussed in this chapter.

The device performance increases if the size of the device dimension reduces to ultra thin level. Reducing the width of the device will increase the series source/drain resistance which will reduce the drain current. The increased resistance of the device can be reduced if the source is recessed deep inside the buried layer of the structure. Moreover if instead of dividing the gate metal with two metal of different work function, the gate metal is linearly varied along the channel with different work function, the steep change of potential profile of the device can be avoided. This two concept of device engineering is merged in a DMDG SON MOSFET structure which is explained in **chapter 3**. This will combine the benefit of both the structure and provide a more scalable and improved device structure in the form of surface potential and electric field.

When the device dimension is comparable to de Broglie wavelength, the quantization of carriers takes place. The maximum inversion charge which is present in the interface of Si/SiO_2 in classical mechanics are now shifted to the middle of the substrate and produce a volume inversion. This volume inversion is due to the quantum mechanical effect. So to determine the drain current appropriately the Schrödinger and Poisson's equation should be solved self-consistently. **Chapter 4** contain the analytical modeling and analysis of drain current for DMDG SON MOSFET considering the quantum mechanical effect. A comparison of drain current is made between classical and quantum approach.

The scaling of a device will scale down the gate oxide with same proportion The ultra-thin gate oxide layer of SiO_2 will start breakdown when its thickness approach to 2nm range and provide a leakage

current path from the gate metal to the channel through the gate oxide. The leakage current will increase and gate will lose control over the channel. The effective gate oxide thickness can be increased by using a high-k dielectric material. The analytical modeling of the threshold voltage and drain current for a DMDG SON MOSFET using HfO_2 as a high-k dielectric is covered in **chapter 5** and try to give a solution for replacing SiO_2 as a gate dielectric.

Chapter 6 demonstrate the application of hybrid SET- SOI MOS circuit. This circuit utilizes the benefit of both SOI MOS and SET and provide a solution for future nanodevice application.

The outcome of the present work and the conclusion are summarized in **chapter 7**.

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Chapter 2

BASICS OF NANODEVICES

2.1 Introduction.

Electronics components have become imperative part of human in the current era of human civilization. The rapid growth in the field of electronic is attributed to constant device miniaturization. Increase in circuit speed, reduction in cost and increase in integration density are the standard to miniaturization of the device [2.1]. Increasing demand for downscaling of the device to quasi-nanometer level, improvement of speed and power [2.2] has allowed the researcher to adopt single chip complex integrated system. The evolution of nano-electronics from microelectronics scale down the physical dimension of the semiconductor device. Downscaling will double the number of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) integrated into a chip every two years. The densely packed chip and high drive current are the natural advantages of nanoscale device make it faster and multifunction operational on a single chip. The prediction of Moore's law [2.3] facilitated the continuous downscaling of the semiconductor device and to explore the development in nanometer range with new method and materials. Rapid progress in Complementary Metal Oxide Semiconductor (CMOS) has given a boost in downscaling of the semiconductor device which eventually effect in the tremendous

increase in functionality and speed of the device. In a nano-dimensional device, the excessive leakage current will act as a barrier for the further shrinking of the device. The performance analysis of the evolution of transistor structure with scaling size is shown in figure 2.1.

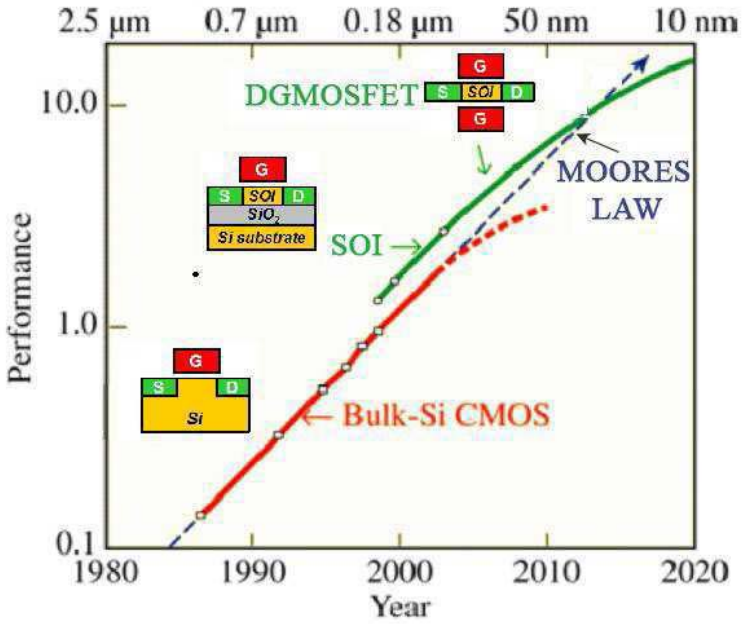

Fig. 2.1. Evolution of transistor structure with scale size

The conventional Scaling trend of the device will not be able to maintain the performance and reliability of the device. So researchers are being pursued to look for new device structure with new material [2.4]. Maintaining the same or improve functional efficiency of further miniaturization of the device is possible through novel device structure and enhanced material property. Reliability issues, gate depletion, direct tunneling, boron penetration and different short channel effect (SCE) becomes constrain for miniaturization of the device from micro

to nanometer regime. These challenges associated with CMOS regime can be somewhat assuaged by adopting nonconventional Metal Oxide Semiconductor (MOS) structure. Multiple gate strain silicon, Silicon on Insulator (SOI), Silicon on Nothing (SON) structure are some of the innovative MOS structure in nano dimensional regime which exhibit improved performance. Carbon Nanotube FETs, Nanowire Field-Effect Transistors (NWFETs), Graphene Nanoribbon FETs, III-V channel replacement devices, etc. are some of the alternative devices which can be shrunk to 22nm range [2.4].

The further reduction of size in the semiconductor device will lead to quantization of the carriers. Quantum mechanical law which comes into present limit the downscaling of the device along with fabrication technique and cost limitation [2.5]. According to recent studies [2.6] size of the transistor will be shrink to 10nm with a span of 10 to 15 years make it more difficult to fabricate and realize the operation of the nano size device. So we have to look for the alternative device. The alternative device will either go for quantum mechanical phenomena or adjust themselves to perform in the nanometer regime [2.7]. Two type of device come into existence one is the revolutionary nano electronic device which works on the quantum mechanical phenomena principles such as Resonant Tunneling Diode (RTD), Spintronics, HEMT, SET, etc. And the second is evolutionary nano electronic devices which work in the existing semiconductor technology to satisfy the downscaling of the device such as carbon nanotube FETs, NWFETs, Graphene Nanoribbon FETs, unconventional geometries for FETs etc. Moreover to minimize the leakage current some exploration has to do on the different material

used for a conventional transistor. One such is the use of high permittivity dielectric material to reduce the leakage current. The primary issues of further scaling and parameter optimization of non-conventional nanodevice and bulk devices have been focused in this chapter.

2.2 Nano Devices

Simple structure, low power consumption and low cost of fabrication make MOSFETs a promising semiconductor device in early 1970. The exponential rise in the number of transistors as predicted by Moore's law [2.3] in integrated circuit has focused the semiconductor industry from micro to nanometer regime. The nano dimensional device will increase the structural complexity and pursue device physicists to explore various ways to keep pace with the race of device scaling. Challenges arise from the miniaturization of the device compelled the microelectronics engineer to search for new material or new innovative device structure for the transition from bulk MOSFET to future nanodevice. Based on the above issues here we try to give an enlight the transition from bulk MOSFET to nanodevice.

2.2.1 Metal Oxide Semiconductor Field Effect Transistor

The modern MOSFET is based on the principle set by Julius Edgar Lilienfeld [2.8] in 1925. Signal amplification and electronic switching are the two purpose for its design. The operation of MOSFET is based on the MOS capacitor. The MOS capacitor is designed by sandwiching a thin layer of oxide between the silicon (Si) substrate and

the gate metal layer. The state of the silicon surface is controlled by the voltage applied to the gate. The control can be of accumulation or inversion. The attraction of the holes due to the application of negative gate voltage in a 'p' type silicon is accumulation state and application of a positive voltage greater than the threshold voltage in an 'n' type silicon surface from the inversion state. The basic n channel MOSFET is shown in figure 2.2. [2.9]. The MOSFET comprise of four section, the heavily doped source and drain, lightly doped substrate and separated by oxide layer gate. n-type and p-type are the two MOSFET available based on the type of substrate.

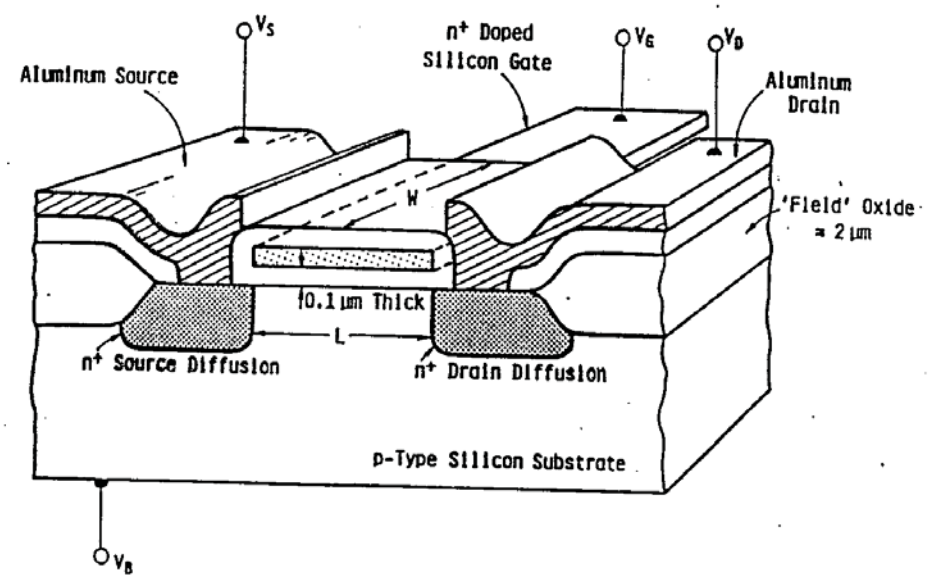

Fig. 2.2 Cross section of MOSFET

N-channel is formed by n^+ source and drain with p substrate, and it names as n-channel MOSFET. The electron is the majority carrier in n-channel MOSFET. Similarly for p-channel MOSFET the channel is

formed with p^+ source and drain with n-type substrate. The hole is the majority carrier here. The channel length 'L' is the distance between drain and source and the lateral extension perpendicular to length is the width 'W' of the channel. There is no current flow between the gate and the channel due to the presence of oxide dielectric layer which makes the device as voltage operated device [2.10]. The symmetry of drain and source is maintained by completely interchangeable drain and source according to the flow of the carriers.

MOSFET can be classified as depletion mode and enhancement mode MOSFET. It is further individually categorized as n channel and p channel [2.11]. In the depletion mode MOSFET the channel, source and drain are diffused with the same impurity. A conducting path exist between source and drain due to inherent doping in the channel even at zero gate voltage. This makes it normally ON device. Application of negative gate voltage in the n-channel depletion mode will induce positive charge through the dielectric layer and make the channel deprive of drain current. Finally, further increase of gate voltage will make the drain current zero and move the device into OFF state. The circuit symbol and structural representation of depletion mode MOSFET are shown in figure 2.3 and figure 2.4 respectively.

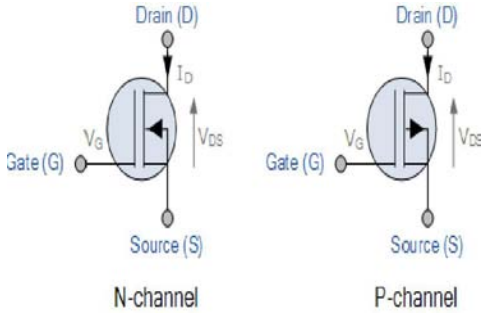

Fig. 2.3 Depletion-mode MOSFET circuit symbol

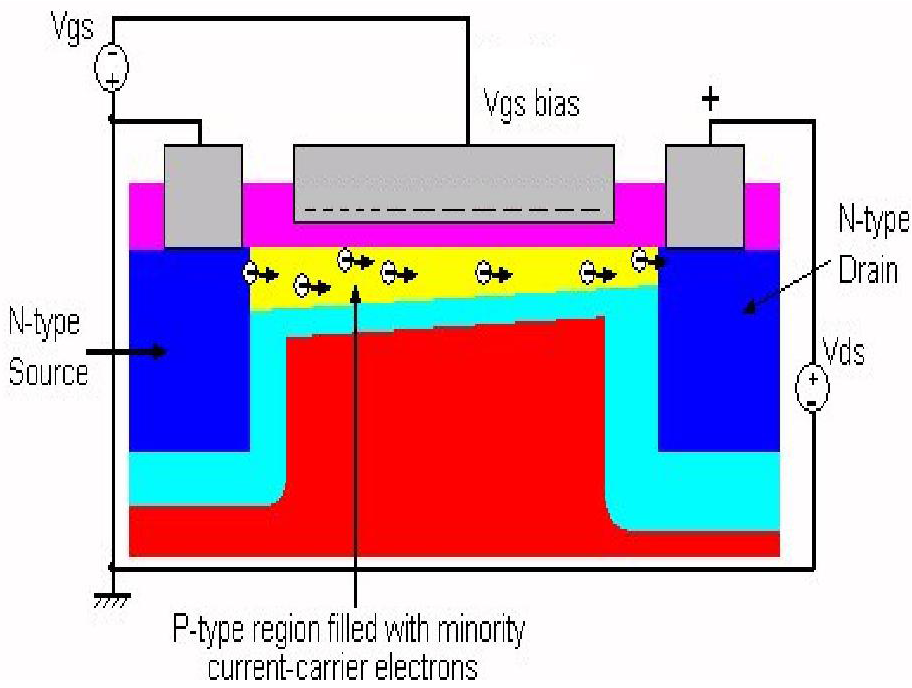

Fig. 2.4 Depletion-mode MOSFET structure

The channel of the enhancement mode MOSFET is lightly doped or even undoped in compared to source and drain to make the device void of conducting channel between source and drain in the absence of gate voltage. This makes the device in OFF state. The application of gate voltage (positive voltage for n channel and negative voltage for p channel) greater than threshold voltage will attract the minority carrier of the substrate to form a conducting channel. The increase of the gate voltage will increase the carrier concentration. The increase of carrier concentration will reduce the channel resistance which will enhance the current following through the channel. Thus the device will move to ON state, and it will work like a transconductance

device. The structure and symbol of the enhancement mode MOSFET is shown in figure 2.5 and figure 2.6 respectively.

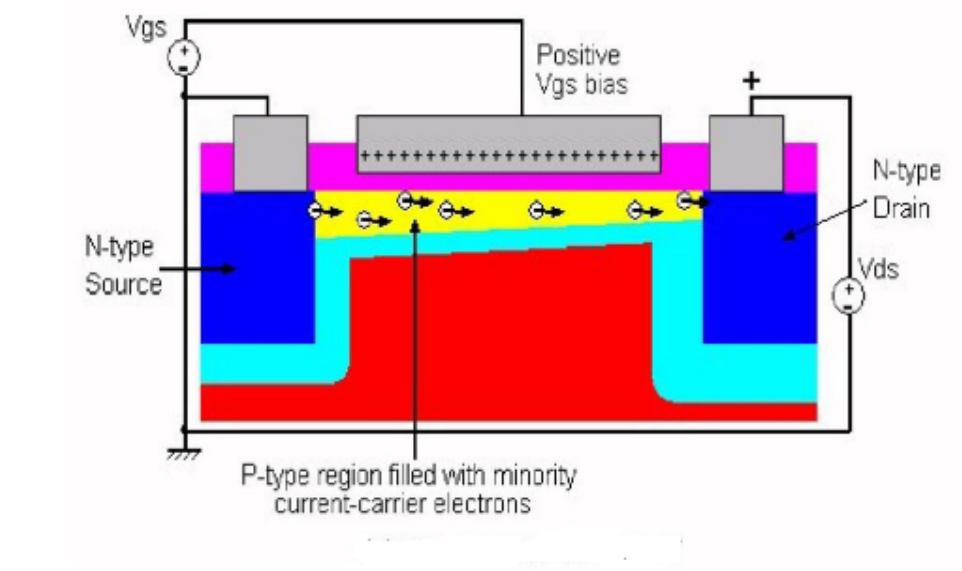

Fig. 2.5. Enhancement mode MOSFET structure.

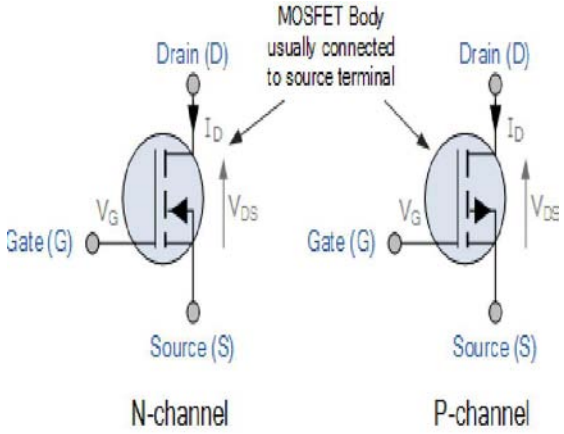

Fig. 2.6. Enhancement mode MOSFET circuit symbol

The current voltage relation of a MOSFET will define the three types of region which MOSFET can operate. The three region of operation in the characteristics graph as shown in figure 2.7. are

(i) Cut Off region.

(ii) Linear or ohmic region.

(iii) Saturation region.

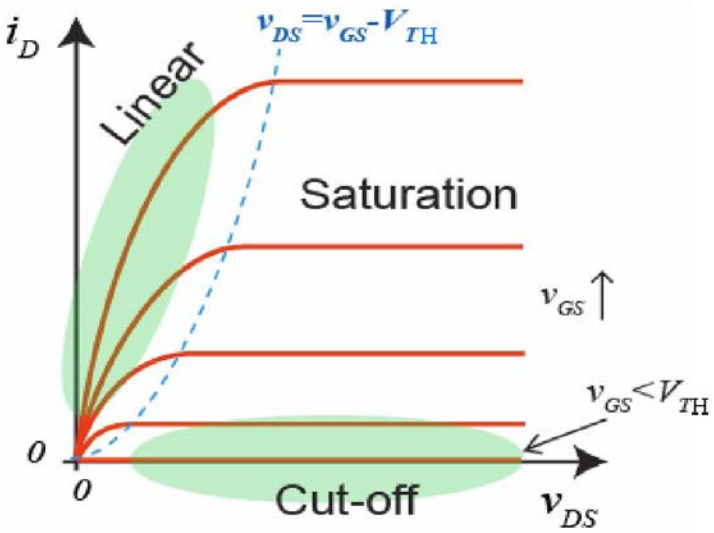

Fig. 2.7 Drain current characteristics curve of n channel enhancement MOSFET

In the cut off region, the gate voltage is less than threshold voltage . Hence there will be no conducting channel formed between source and drain. The current following through the device is zero and the device is in OFF state.

In the linear or ohmic region the gate voltage is greater than threshold voltage but less than drain to source voltage. The transistor will move to conduction region, and the channel will behave like a variable resistance. Gate voltage will control the resistance.

In saturation region, the gate voltage is greater than the threshold voltage but less than the difference between drain to source voltage and threshold voltage. The device is fully in ON state, and the drain current is maximum and its acts like constant current region.

2.2.2 Complementary Metal Oxide Semiconductor.

CMOS (Complementary metal oxide semiconductor) is evolved from incorporating both PMOSFET and NMOSFET in complementary mode [2.12]. CMOS technology is used for constructing integrated circuit. Here both the MOS are not ON at the same time due to its complementary nature. Complementary nature of the MOSFET will make only OFF state leakage current loss effective for steady state. Low static power consumption and noise immunity make the technology effective for an integrated circuit. The structural view of CMOS and connection for a CMOS inverter is shown in figure 2.8 and figure 2.9 respectively.

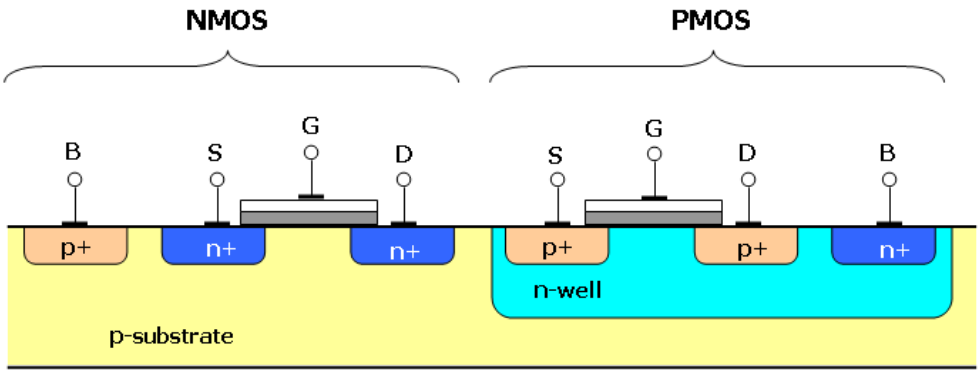

Fig. 2.8 CMOS structural view

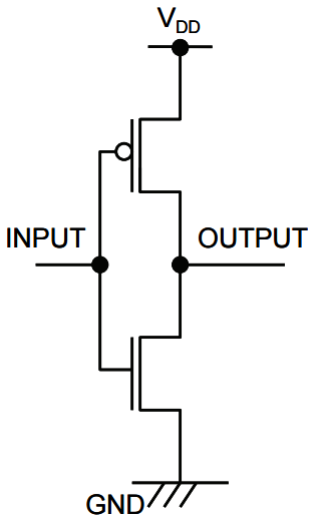

Fig. 2.9. CMOS inverter connection

2.2.3 Silicon on Insulator MOSFET.

Reduction of channel length due to scaling down of MOSFET give rise to various short channel effect. The Classical conventional device structure is unable to give a solution by which we can further scale down the device. Innovative non-classical device structure can have a panacea to the various short channel effect. Silicon on Insulator (SOI) MOSFET is one such innovative alternative with lower short channel effect which allows further scaling of the semiconductor device.

The concept of housing a thick layer of silicon-di-oxide in between the silicon layer beneath the gate and the substrate is used for SOI structure. The thick oxide layer is known as Buried Oxide (BOX) fabricated between the channel and the substrate makes it different from the conventional MOSFET. The BOX is fabricated by oxidation of silicon or implantation of oxygen in silicon. The presence of

dielectric as buried layer will restrict the extension of the depletion region to the substrate thereby decreasing parasitic capacitance and leakage current. Low leakage current and parasitic capacitance will make the device less electrical power consumption device, high speed, and support miniaturization. Constant innovation in SOI MOSFET structure expands the device from single gate to multiple gates and surrounding gate structure [2.13]-[2.16]. The cross sectional view of SOI MOSFET structure is shown in figure 2.10.

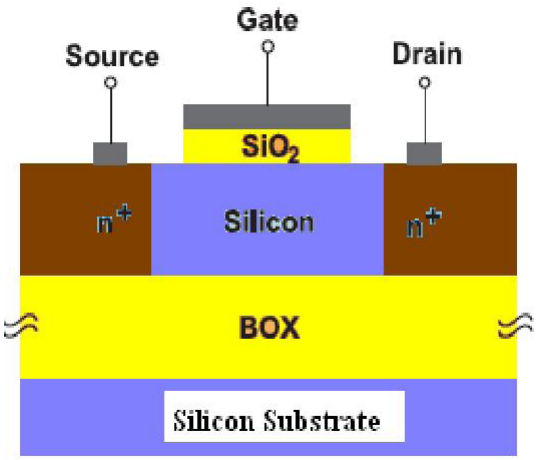

Fig. 2.10. Silicon on Insulator (SOI) Stucture

The thickness of silicon layer of SOI MOSFET will classify it into two different modes of operation, Partially-Depleted (PD) SOI and Fully-Depleted (FD) SOI. The cross sectional view of both the SOI structure is shown in the figure 2.11. The body region of the FDSOI is thinner in compare to PDSOI making the gate depletion width higher than silicon thickness. Hence for both ON and OFF state the entire body region will be under depletion. Whereas in PDSOI the thickness

of the silicon is larger than the gate depletion width so that the surface potential in the channel region is not uniform. Floating body is more pronounced in the PDSOI due to the presence of a undepleted region in the back interface.

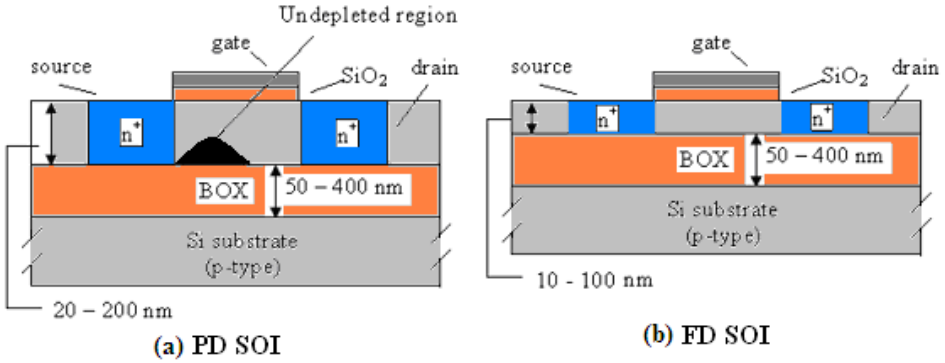

Fig. 2.11 Cross section of (a) PD-SOI (b) FD-SOI

2.2.3.1 Characteristics of SOI.

SOI structure has many advantages in compared to bulk CMOS. The glimpse of it can be seen through its characteristics.

(i). Kink Effect.

The electron for a fixed gate voltage with supplied drain to source voltage will move towards the drain region. The flow of electron will get momentum due to the gaining of kinetic energy which will create additional hole electron pair because of impact ionization. The generated electron will enhance the drain current. The extra generated hole will move towards the source and starts accumulated there. The accumulated hole will reduce the threshold voltage which further increase the drain current. This is reflected in the sharp rise of drain

current for a particular drain voltage. And the sharp of drain current phenomena is known as kink effect [2.17]-[2.19].

(ii). Improved Subthreshold slope.

The steep Subthreshold slope is the another characteristics of SOI MOSFET with a slope of 60mv/decade. Due to less SCE in FDSOI, FDSOI will have better subthreshold slope than PDSOI [2.18],[2.19].

(iii) Threshold voltage Roll Off.

The presence of SCE in a MOSFET will reduce the threshold voltage as the channel length decreases. This effect is also present in SOI MOSFET. But due to the reduce SCE in SOI MOSFET in compare to bulk MOSFET the threshold voltage roll-off is less in SOI MOSFET.

(iv) Parasitic bipolar effect.

The parasitic bipolar transistor created with n^+ source, drain and body region due to the accumulation of hole in the source region(because of impact ionization) will adversely affect the threshold voltage, subthreshold slope and breakdown voltage between the drain and the source. The presence of undepleted body region in PDSOI will make it more prominent in PDSOI.

(v) Dynamic floating body effect.

The body potential of a SOI MOSFET varies with different changes in the device behavior. This is due to the complete isolation of channel to the body. This phenomenon of having different body potential for different induce effect is known as dynamic floating body effect. Majority carrier redistribution and impact ionization are the main

reason of changes of body potential. FDSOI is more immune to floating body effect than PDSOI.

(vi) Self-heating effect.

The BOX layer which is used for better performance of SOI device will also act as thermal insulation between the channel and the substrate. So heat generated by drain current will be thermally insulated to release through the substrate and the device become hotter. This is known as self-heating. The effect of self-heating will reduce the performance of the device. Reduced drive current, turning on the bipolar parasitic transistor, low breakdown voltage, excess generation of hot carrier current are some of the negative effects of self-heating.

2.2.3.2 Advantage of SOI MOSFETS.

(i). Reduce parasitic capacitance.

The presence of SiO_2 (with lower dielectric constant than silicon) buried oxide layer in SOI device will reduce the capacitance between the substrate and drain/source. The reduction in parasitic capacitance will effectively reduce the switching speed of the device and in turn increase the performance by 20 to 25 percentage faster for same power consumption. Moreover for the same supply voltage the power consumption of SOI device is less than bulk MOSFET.

(ii). Smaller layout and ideal device isolation.

The device placement for a SOI device can be made more compact by using a thin insulation film for lateral isolation between two device and thick BOX layer for vertical isolation for channel and

substrate. This makes the perfect device isolation. The CMOS inverter output can be connected directly to p^+ and n^+ diffusion making the device more compact than bulk MOSFET.

(iii). No latch up.

The buried layer prevent the formation of n-p-n-p (or p-n-p-n) thyristor in SOI MOSFET. So no latch-up occur as in bulk MOSFET.

(iv). Small p-n junction leakage current.

The thinner top silicon layer reduces the p-n junction leakage current due to a small area. So low standby power is required [2.20],[2.21].

(v). Improvement of stack gate speed.

The threshold voltage and fall time increase for a NAND gate designed by MOSFET. The presence of negative body bias in connecting the both pull down transistor to ground will generate this drawback. But in SOI MOSFET due to the presence of buried layer, a positive body bias is obtained which will reduce the threshold voltage and fall time and increase the drain current.

(vi). Reduce short channel effect.

The gate has better control over the potential profile of the channel due to miniaturization of the device in compared to MOSFET. The better control of gate over the channel will reduce the SCE drastically.

2.2.3.3 Disadvantage of SOI MOSFETs.

The SOI MOSFETs becomes most sought after device after having many advantages over bulk MOSFET. But it also suffer from

some disadvantage [2.22]-[2.25] because of SCE. Some of the disadvantages are

- High drain voltage will produce a high off current because of forward bias body source junction.
- The design of ultrathin films to support fully depleted device have realization problem.
- Floating body effect of PDSOI will give rise to kink effect and overshoot of drain current in DC circuit and switching circuit respectively
- Ultra thin structure are more prone to parasitic bipolar transistor effect and dynamic floating body effect.
- Self-heating of SOI device is a critical issue for circuit realization.
- To reduce the interface scattering buried oxide should be of high quality.

2.2.3.4 Improve SOI MOSFETs.

SOI structure has many advantages over normal conventional MOS structure in the range of submicron level. But when the device moves to the deep sub 100nm regime it cannot mitigate the different issues of SCE. So we have to look for some innovative engineering on SOI device to get a better performance SOI device [2.26].

(i). Recessed Source/Drain ultra thin SOI MOSFET

The FD-SOI use the concept of ultrathin silicon films to suppressed the sub-surface leakage path by having good gate control

over the channel. To avoid the mobility degradation problem and fluctuation of threshold voltage it does not completely rely on heavy doping of channel. Although it reduces the SCE, due to ultra-thin nature of the source/drain, it will increase the series resistance and thereby have a poor current driving capability. This problem of higher series resistance can be overcome by using recessed source/drain extending deep into the buried layer [2.27],[2.28] as shown in the figure2.12.

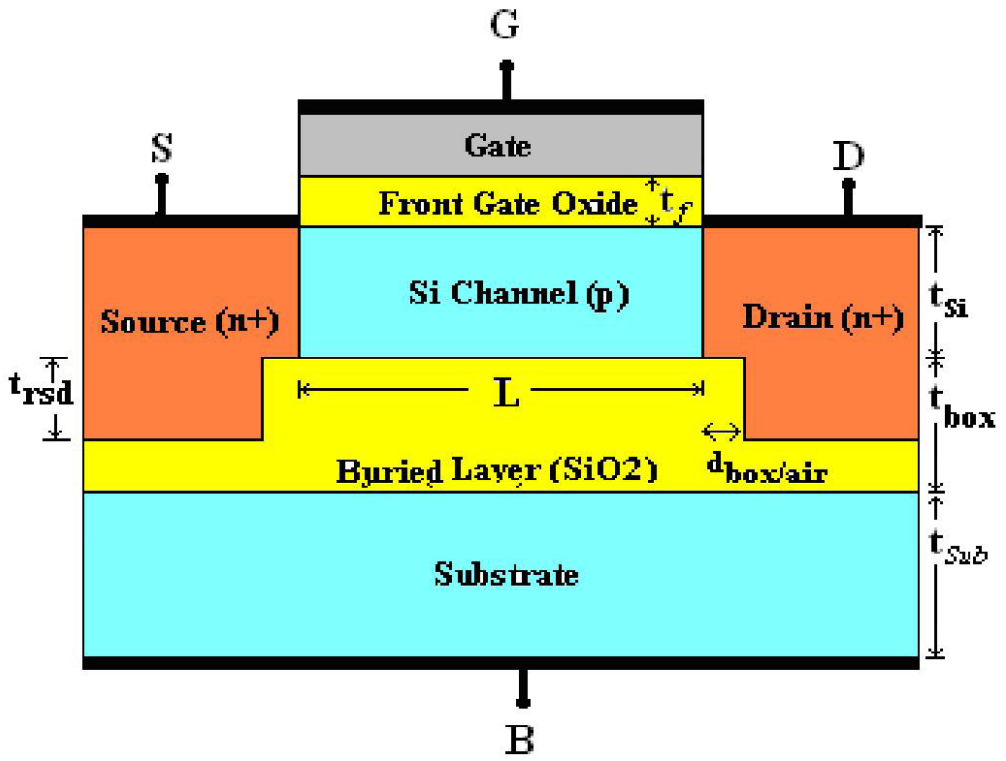

Fig.2.12 Recessed source/drain ultra thin SOI structure

(ii). Metal source and drain SOI MOSFET

The ultra-thin SOI MOSFET will have a higher value of series resistance due to the small cross-sectional area of source and drain.

The high resistance will decrease the drain current. The resistance of the device can be decreased by using metal drain and source. The metal source/drain will form a Schottky barrier between source/drain and channel. So proper emphasis should be given to reduce the Schottky barrier

(iii) Metal Gate SOI MOSFET.

Boron penetration, high gate resistance, and poly-Si gate depletion are some of the issues arise from miniaturization of MOS device. Metal gate SOI MOSFET can overcome this problem. The metal gate SOI MOSFET use the work function of the gate instead of thin film doping concentration to modify the threshold voltage. [2.29]-[2.31]. Moreover the use of metal gate instead of the polysilicon gate also mitigate the problem of polysilicon gate depletion.

(iv). Multiple gate SOI MOSFET.

The intrusion of electric field from the drain to the channel can be reduced by using multiple gate SOI structure. The volume inversion in a multiple gate will provide better conductance and better control of gate over the channel. It has the benefit of reducing SCE. Double gate, quadruple gate, π gate, gate all around transistor etc are some of the examples of multiple gate SOI MOSFET structure [2.26].

(V). Dual material gate SOI MOSFET.

Dual material gate structure used two material of different work function side by side in a single gate. The concept of gate engineering introduce a step potential in the potential profile of the channel to

reduce the short channel effect. There is an improvement of source side electric field which will have the impact of carrier transport efficiency in the positive note [2.32]. The structure of dual material gate is shown in the figure 2.13.

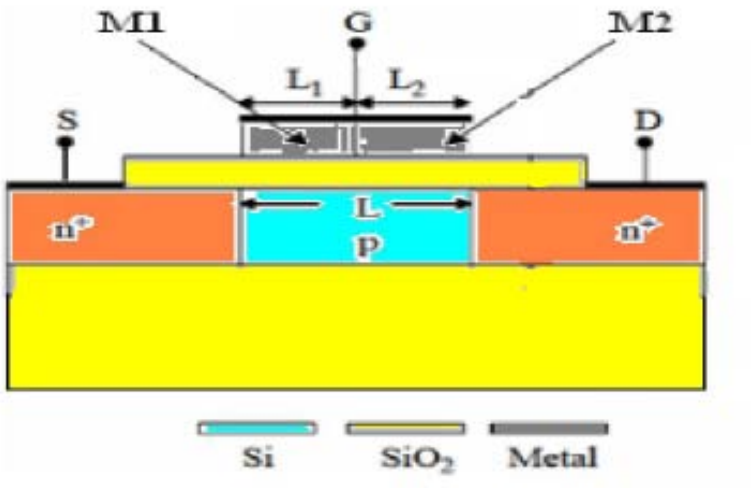

Fig. 2.13 Dual material gate SOI MOSFET structure

2.2.4 Silicon on Nothing MOSFET.

The performance of the SON structure can be improved further by replacing the buried oxide of the SOI structure with low permittivity material of permittivity one. The new innovative device is known as Silicon on Nothing (SON) MOSFET. The SON structure embodied the benefit of both bulk MOSFET and SOI MOSFET and provided a better performance in terms of reduce short channel effect, reduce floating body effect and hot carrier effect. Immunity to short channel effect will support further miniaturization of the device. The ultra-thin nature of the SON structure with less permittivity of the buried oxide will remove the resistance for heat release from the generated heat from the channel

region to substrate [2.33]-[2.35]. The concept of the dual metal gate of SOI structure can also be extended to SON MOSFET. The steep variation of work function in dual metal gate can be overcome by implementing the concept of linearly graded mole fraction variation of work function in dual metal gate engineering SON MOSFET [2.36].

The SON MOSFET structure has many advantages over SOI MOSFET structure. Some of them to the SOI counterpart are

- The buried air layer will provide high dielectric isolation of active channel region.
- The electrostatic coupling through the buried layer is reduced.
- The parasitic capacitances effects is less, that ensure high circuit speed.
- The power consumption, noise, short channel effect are reduce in SON MOSFET which ensures further scaling capability and s faster switching speed.

2.2.5 Single Electron Transistor.

Scaling down the device below 100nm range arises series of problem related to different type of short channel effect, drain induced barrier lowering, punch through, static leakage, etc. An innovative structure like SOI MOSFET and SON MOSFET, a material with high-k dielectric are some of the way by which these issues can mitigate up to a certain level. But downscaling of the device cannot continue forever with the same technology. So researcher is looking for another novel approach which can replace the existing CMOS technology. Single electron tunneling technology is one of such novel approaches which

gives us to look beyond CMOS. Single electron tunneling technology is one that control the flow of single electron [2.37].The first single electron device is the Single Electron Transistor (SET) proposed and fabricated by Fultan and Dolan [2.38].

The tunnel junction is the basic element of single electron device (SED). The conduction of current in SED is due to quantum mechanical tunneling of an electron through the tunnel barrier. The basic concept of SET is where a conductive island is sandwich between two tunnel junction. The tunnel junction is a thin dielectric layer which will act like a leaky capacitor as shown in the figure 2,14. The charge transport between the terminal is discrete in nature as one electron can transport at a time. The addition of the third terminal coupled to the island through a dielectric will form a SET as shown in figure 2.15.

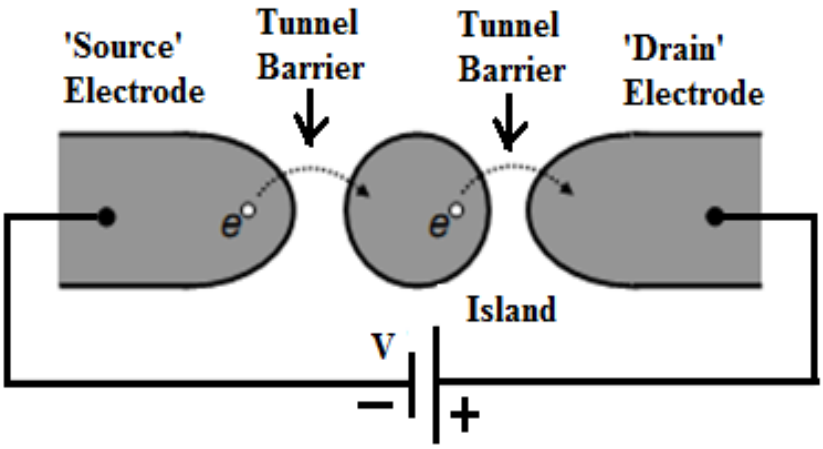

Fig. 2.14 Single island double junction device.

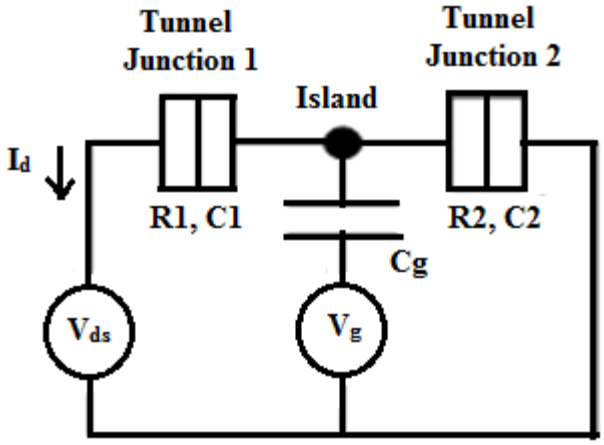

Fig 2.15 Single Electron Transistor

2.2.5.1 Operation of SET.

The tunneling of an electron in SET is depended upon coulumb blockade effect. If the width of the tunnel junction is too small, then the applied voltage will cause the quantum mechanical tunneling of the electron. Now if C is the junction capacitance than tunneling of an electron can take place if the energy provided by external biasing is greater than the charging energy ($E_c=e^2/2C$) [2.39]. If the energy is below the charging energy, the electron cannot tunnel through the junction and the device goes to OFF state. This phenomenon is known as a Coulomb blockade. The smaller value of capacitance will make the charging energy more significant, and it helps in control of electron in one electron level. This effect is referred as single electron charging effect. For a micrometer regime the single electron device will not be effective as nanometer regime since the capacitance value is too high making the charging energy very small to control electron in single electron level. To tunnel an electron the applied energy should be

greater than charging energy which is shown in the figure 2.16. After tunneling of the first electron the energy required to tunnel the second electron should be greater than e^2/C and it goes on. If the tunneling rate across the junction is same, the tunneling will be as shown in the figure 2.16. If the tunneling rate across the junction is different than the current increase in stepwise as shown in the figure 2.17. The tunneling of electron takes place based on the assumption of orthodox theory of SET [2.40]

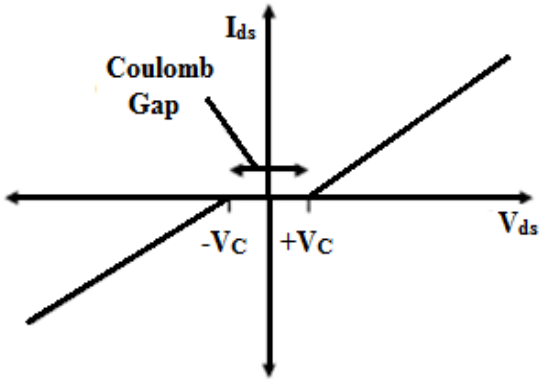

Fig 2.16 Symmetric SET coulomb blockade phenomena

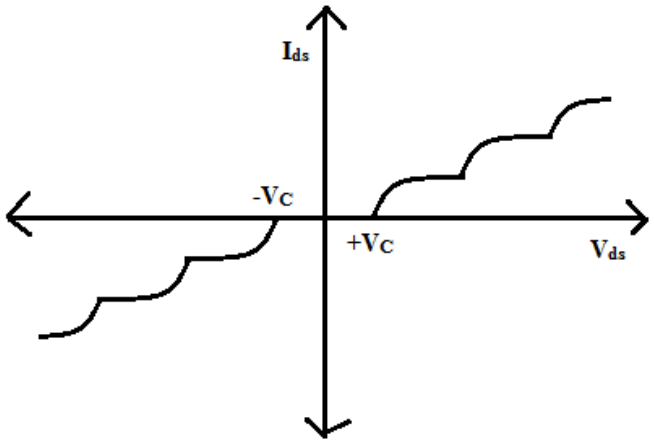

Fig.2.17 Asymmetric SET Coulomb blockade phenomena

The circuit diagram shown in the figure 2.15 is a single electron transistor (SET) where the gate terminal is incorporated to the island through capacitor Cg [2.38]. R_1,C_1 and R_2,C_2 are the resistance and capacitance parameter for tunnel junction 1 and junction 2 respectively. The gate terminal added to the system will control the Fermi level of the system. Figure 2.18. Shows the Id-Vgs characteristics of the SET. For a fixed value of vds, Id-Vgs oscillates periodically and is known as the Coulomb oscillation characteristics.

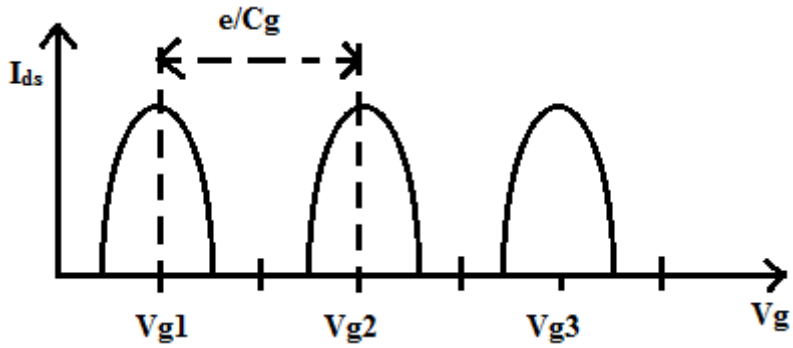

Fig. 2.18 Coulomb Oscillation.

2.2.5.2 Orthodox Theory of Single Electron Effect.

The charge transport phenomena of single electronics circuit is well described by the orthodox theory of single electron tunneling.

- The charging energy E_c must be very high in compared to the thermal energy k_BT, to overcome the effect of tunneling of the electron due to thermal fluctuation. [2.38][2.39].
- The tunnel resistance R_T should be relatively high to localize the electron in the island.

  $\boldsymbol{R_T \gg R_K = \hbar/e^2 = 25.9K\Omega}$ where R_K is the quantum of resistance and h is the Plank's constant

2.2.5.3 Hybrid SET MOS.

The unique feature of nanoscale size, coulumb blockade oscillation, and ultra low power dissipation make SET as a most fascinating device. But due to low drive current and temperature dependability of the device put a question mark on its application. If the feature of the SET can be exploited to increase the functionality of the CMOS it will become a better and improves device. SET and MOS are rather complementary to each other which is shown in Table 2.1.

Table 2.1 Pros and cons of SET and MOS

Technology	Advantage	Disadvantage
SET	• Nanoscale feature size • Unique Coulomb blockade • Ultra low power dissipation	• Low current drive • Lack of room temperature operable technology • Background charge effect
MOS	• High gain and current drive • High speed • Matured fabrication technology	• Sub 10nm physical limit • Power density

The advantage of low power consumption and new functionality (Coulomb blockade) of SET is complement by high voltage gain and high drive current of CMOS. So by combining SET and MOS, a new functionality can obtain which will utilize the benefit of both MOS and SET [2.41]. A new architecture i.e. hybrid CMOS-SET architecture is obtained which will offer the Coulomb blockade oscillation of SET and

high drive current of MOS. The architecture and circuit symbol of hybrid SET MOS is depicted in figure 2.19 [2.41]. A constant current source is used to biased the SET, gate of the MOSFET is connected to the drain of the SET, the output of the device is obtained from the drain terminal of the MOSFET.

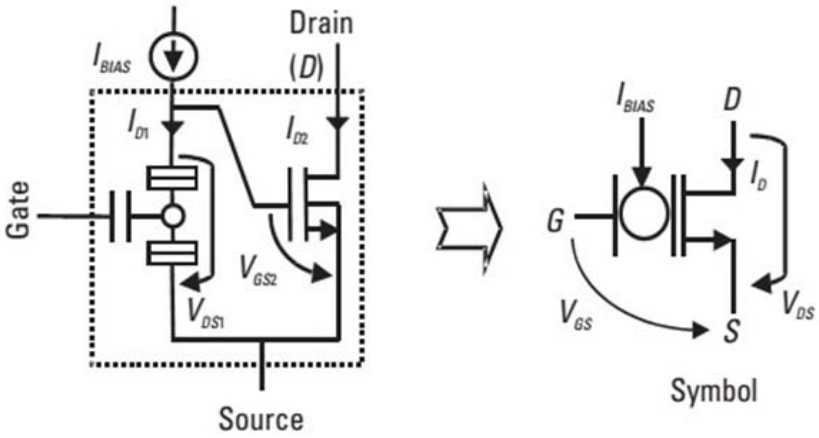

Fig. 2.19 SET MOS architecture and symbol

2.3 High K Dielectric

Integrated circuit development for the last decade has been driven by scaling of the MOSFET. The requirement for circuit speed, the range of power supply, off state static power consumption, output voltage [2.42] varies according to the field of operation of the circuit. The circuit speed can be improved by improving the drive current of the device. So the effect of scaling is an important aspect of research. The saturation current of the MOSFET is given as [2.43],[2.44]

$$I_{Dsat} = \frac{W}{L}\mu C_{ox}\left(\frac{V_G - V_T}{2}\right)^2 \tag{2.1}$$

Where

W = Width of the MOSFET channel

L = Length of the MOSFET channel

μ = Effective mobility

V_G =Gate voltage

V_T = Threshold voltage

C_{ox} =Gate oxide capacitance

The increase of gate oxide capacitance which is inversely related to dielectric oxide thickness will increase the saturation current. The gate oxide capacitance is defined as

$$C_{ox} = \frac{k\varepsilon_0}{t_{ox}} \tag{2.2}$$

where

k = Dielectric constant of the gate oxide

ε_0 = permittivity of the vacuum

t_{ox} = Gate oxide thickness

So scaling down of the gate oxide will increase the effective oxide capacitance which finally enhance the saturation current.

Some of the properties that make the Silicon di-Oxide (SiO_2) as a perfect dielectric in micrometer range of MOSFET are

- Dielectric constant of approximately 3.9 sufficient for micrometer range
- Band gap of 9eV.
- Band offset in the conduction band and valence band for Silicon is sufficient.
- Si-SiO_2 interface is perfect

- Thermal stability even at high temperature with Si.
- Boron penetration from p^+ poly-silicon gate is well insulated.
- Oxide breakdown protection with good dielectric strength.

Reducing the oxide thickness will increase the oxide capacitance to enhance the drain current. But it will raise some critical gate leakage issue if the thickness of the oxide is brought down less than 3nm [2.45]. The gate leakage current increases exponentially with a decrease of gate oxide. This mechanism is due to quantum mechanical tunneling of an electron through the gate oxide [2.46]. Moreover boron penetration from the p^+ poly-silicon gate will exist [2.47],[2.48]. The carrier mobility of channel also starts degrading when the oxide thickness is reduced below 1.3nm [2.48]-[2.50] due to a different type of scattering effects. These technical issues of gate leakage current make the MOSFET eventually unusable when the device is scaled down below 45nm. So to maintain the scaling trend of Moore's Law, an alternative gate oxide is required to replace SiO_2. The replace gate dielectric should have high permittivity so that the effective oxide thickness in comparison to SiO_2 increases. This will make the gate oxide physically thick to suppressed the tunneling current and electrically thin to provide higher oxide capacitance to improve the drive current.

2.3.1 Properties of High-k Dielectric Material.

Various high-k dielectric material with high permittivity are there to replace SiO_2 as dielectric gate oxide. To replace the SiO_2, a dielectric material along with high permittivity and high gate oxide capacitance should satisfy the following requirement.

(i) Dielectric constant should be sufficient.

Use of innovative high-k material as a gate dielectric oxide in the existing CMOS process will increase the production cost of the semiconductor industry. So the material that is going to replace the SiO_2 should support the industry for coming generation. The dielectric having large band gap thermal stability with Silicon, large band offset with silicon, etc. [2.51] but with lower permittivity should not be considered for future generation gate oxide. Moreover, the actual value of the dielectric constant varies according to the deposition parameters, deposition technique and the composition of a component in the material.

(ii). Thermal stability.

Fabrication of CMOS technology exposes the dielectric material to high-temperature crystallization and formation of silicate which are the concerns at very high temperature for high-k dielectric. Crystallization of high-k material will provide additional gate leakage path for the leakage current, so crystallization of gate should be avoided. Same is the case if silicate (metal-Si-oxide) is formed at high-k/silicon interface. This is one of the reasons why Hafnium Oxide (HfO_2) is preferred over Zirconium Oxide (ZO_2) after having a lower permittivity[2.52],[2.53].

(iii). Band gap.

Band gap and band offset are other two parameters should be considered while selecting the high-k material. High band gap will decrease the leakage current [2.54],[2.55]. Smaller barrier height has an effect on Schottky thermionic emission which will degrade the mobility of the carrier in the channel. ZrO_2 and HfO_2 are preferred

because of high band offset and band gap among other high-k dielectric material.

(iv). Low interface trap density.

The scattering effect in the channel will be increased if some defects remain in the Si/gate oxide interface. The increase of scattering will have a negative effect on the carrier mobility of the channel. The interface trap density should be of low value. Normally it is high for high-k material in compared to SiO_2 due to the difference of work function between the substrate and the gate. So the interface quality of high-k dielectric with silicon should also be taken into account to find out an efficient high-k dielectric material.

HfO_2 is a high-k dielectric candidate which satisfy a maximum of the requirement to replace SiO_2. According to ITRS road map 2013 the effective of HfO_2 can be scale down as low as 0.8 nm [2.56]

2.4 Quantum Consideration Relevant to Nanodevices.

Miniaturization of the device around 10nm range will bring the channel length equal to depletion region of source/drain which will result different type of short channel effect. So to overcome the effect of the short channel, the gate oxide should be reduced with high channel doping. The high vertical electric field generated because of heavy doping in the channel will create a potential well in the interface of Si/SiO_2. Under this condition as shown in the figure 2.20 the energy of the electron starts quantized [2.57] which will lead to quantum

confinement effects. This effect is more prominent if wavelength of electron wave function and device dimension are of same order. Classical mechanical states that if an electron is confined in a box, the exact position and momentum of the electron can be determined, but quantum mechanics contradict it. It states that probability of finding an electron in a particular position can be determined instead of exact position. So if a device comes in the range of quantum consideration, then analysis of the device considering quantum effect is very much necessary.

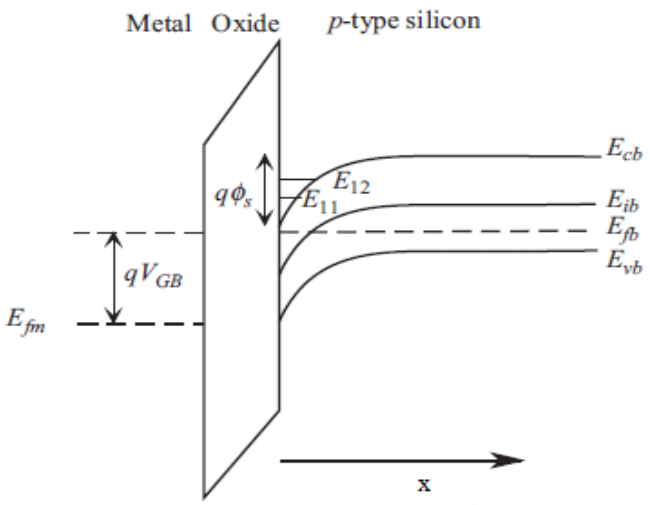

Fig. 2.20. Quantization of carrier energy at Si-SiO_2 interface.

2.4.1 Effect of Quantum Confinement in MOSFET.

Two types of confinement are present in an ultra thin MOSFET structure, electrical and structural confinement. The strong electric field because of high doping will create electric field induce quantum confinement. And the structural quantum confinement is due to the ultra-thin nature of silicon film. The operation of the MOSFET will be

influenced by quantum confinement of the carrier, and its impact will be on:

(i). Threshold Voltage.

Ionized impurity density of a top silicon layer decreases with decreasing thickness of top silicon layer. According to classical mechanics, it will reduce the threshold voltage [2.58]. These classical mechanics hold good as long as top silicon layer thickness of a SOI MOSFET can support bulk (3-D) transport. Quantum mechanics says that the threshold voltage will increase with the decrease of silicon thickness. This is due to the quantum mechanical effect which will shift a maximum of the inversion charge to the middle of the silicon substrate and produce volume inversion [2.59]-[2.61]. The critical dimension at which quantum consideration come into present is 10nm. So as the dimension of device reduces below 10nm, both Schrodinger and Poisson's equation should be solved self-consistently to interpret the volume inversion correctly. Moreover, the concentration of the carrier for same Fermi level will be less as compared to the small density of states in the corresponding classical 2D system. Hence more gate voltage is required to have the same number of carriers in 2D inversion layer, which will ultimately increase the device threshold voltage [2.62].

(ii). Mobility.

In a MOSFET structure if the size of the silicon film is very thin and it can be compared with de Broglie wavelength then the quantum size have an influential impact in the mobility of carrier even at low inversion charge concentration. Confinement of electron in thinner layer increases as the size of the silicon layer is reduced. This will

increase the charge concentration [2.63]. Large charge concentration has a negative effect on phonon scattering i.e. phonon scattering increases significantly. The increase of phonon scattering will degrade the mobility of the carrier in the channel. Increasing gate voltage will increase the number of sub-bands and confinement of carrier will have inter-sub band scattering which will also degrade the carrier mobility.

(iii). Capacitance.

The capacitance of MOSFET will play an important part in measuring the performance of MOSFET. Capacitance which is related to gate delay will influence the speed of the circuit. The total capacitance of device comprises of gate capacitance (C_G) and parasitic capacitance (C_{par}). The gate delay of the MOS depends upon the factor '$1+C_{par}/C_G$'. To have a high speed circuit, the value of gate capacitance should be as high as possible in comparison to parasitic capacitance. In a strong inversion region, the gate capacitance consists of two type of capacitance, gate oxide capacitance (C_{ox}) and inversion layer capacitance (C_{inv}).The inversion capacitance also noted as C_{si} is related to the distance between the channel electron and Si/SiO_2 interface. Now as the device size reduce to 10nm an additional capacitance called quantum capacitance come in to present (C_q). The gate capacitance can be defined as

$$C_G = \left[\frac{1}{C_{ox}} + \frac{1}{C_{si}} + \frac{1}{C_q} \right]^{-1} \tag{2.3}$$

When gate oxide capacitance is less than inversion layer capacitance, then the gate capacitance is equivalent to gate oxide

capacitance. But the reduction of device size will increase the gate oxide capacitance and this increase the influence of inversion layer capacitance on gate capacitance. Influence of inversion layer can be reduced by making the channel film thinner. But thinner silicon film will increase the sub band splitting which will finally reduce the quantum capacitance [2.64]. So the gate capacitance will also have the influence of quantum capacitance. So when the device is miniaturized, and quantum confinement effect is present the effect of quantum capacitance should also be considered while finding the performance of the device.

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Chapter 3

MATERIAL ENGINEERED GATE RECESSED ULTRA THIN BODY SOURCE/DRAIN SON MOSFET FOR BETTER PERFORMANCE

3.1 Introduction.

Downscaling of the device into deep-sub micrometer regimes for enhancing performance and for higher integration densities [3.1] degrade the characteristics of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Silicon-on-insulator (SOI) which has its inherent functional advantages and easier fabrication technology employs a thin layer of silicon isolated from a silicon substrate by a relatively thick layer of silicon oxide. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures. It has many advantages over bulk silicon Complementary-metal-oxide-semiconductor (CMOS) technology, such as higher speed, lower power dissipation, high radiation tolerance, lower parasitic capacitance, low short channel effects, high subthreshold voltage swing. Transistors with 25nm gate length do not perform well in bulk silicon while SOI devices are more tolerant to the constraints of scaling-down rules. The performance of SOI MOSFET can be further improved if the buried oxide is replaced with air, we get a structure known as Silicon-On-Nothing (SON). The basic advantages

of SON MOSFET are radiation immunity in an extreme environment, lower power consumption, further scaling capability, low noise, higher short channel immunity, faster-switching action due to lowest parasitic capacitance and low cost. Higher insulation of channel from the substrate with lowest dielectric constant material 'air' at box region, makes it suitable for a device for hot, cold and other extreme climatic condition. Analytical modeling of SON MOSFET is extremity important as this structure is considered as a probable candidate for next generation ultra low dimensional MOSFET. Nanoscale SOI/SON MOSFET suffer from degradation of threshold voltage with decreasing channel length and DIBL effects at higher drain biases. Calculation of threshold voltage is the most important part of analytical modeling of SON MOSFET as the basic difference between SON and conventional SOI structure come from significantly different threshold voltage. This chapter includes extensive literature study related to the different types of development taken place in gate engineering of SOI/SON MOSFET structure and study the characteristics and performance of the device. This will be followed by proposing a suitable analytical model which will be having better performance with respect to the existing structure.

3.2 Literature Survey.

Ever increase demand for miniaturization of semiconductor device [3.2] leads to shrinking of channel length which will lead to short channel effect, such as steep threshold voltage roll-off, off-state leakage current and drain induced barrier lowering [3.3]. Moreover,

effects of source/drain and dominance of parasitic capacitance have reduced the control of gate in planner bulk CMOS technology [3.4],[3.5]. To overcome these problems, different solution are evolved [3.6]- [3.10]. Double gate MOSFET is one such structure where instead of single two gates, front gate and back gate is used. Due to the presence of a double gate, it will have more control over the channel. The dual gate will prevent the drain electric field from reaching the source. And hence reduce the short channel effect. The volume inversion in the dual gate is also increased which enhances the carrier mobility. It is further improved to DUAL Metal Double Gate (DMDG) MOSFET. Here two material with different work function is used side by side for the single front gate. The work function of the metal connected to the source is higher than that connected to the drain. Due to this charge carrier are accelerated and in turn, reduce the short channel effect. Further reduction of device size has forced the researchers for some non conventional structure and concept and FDSOI MOSFET come into the picture [3.7]. Fully depleted Silicon on Insulator (FDSOI) MOSFET Double gate structure provides a better candidate for the future device due to its inflate performance in terms of short channel effect, current drivability, subthreshold swing, high radiation immunity, high speed of operation, etc. [3.11]-[3.14]. The presence of the buried layer (BL) reduces the coupling effect which in turns reduces the short channel effect makes SOI device a better candidate for a future device. As the device structure reduce further the control of the FDSOI device on basic ingredients of advanced scalability such as silicon film thickness, series resistances, and the fringing fields [3.15]-[3.16] are

reduced. Replacing the buried layer with air a new device SON is formed with lower parasitic and junction capacitance. This device has better control over those parameter [3.4],[3.17]-[3.19]. Reducing the permittivity of the buried layer will reduce the buried oxide capacitance, which will increase the operation speed of the device. Moreover, the self heating problem of SOI MOSFET can also be overcome. The degradation of threshold voltage and Drain Induced Barrier Lowering (DIBL) effect in high drain bias are some of the drawbacks arises in nanoscale SOI MOSFET structure due to a decrease in channel length. Dual metal double gate work function engineered gate SOI MOSFET as proposed by Deb at al. [3.20] will reduced some of the drawbacks. The uneven transition of surface potential and surface electric field at the junction position of the dual metal gate [3.9],[3,21],[3.22] is overcome by lateral mole function variation of the dual metal double gate. This concept can be extended to the SON structure also. Scaling of dual metal SOI/SON MOSFET to the ultra thin body to deep sub 100nm era will lead to ultra thin drain and source region. The ultra thin structure has the advantages of smaller threshold voltage, more control of gate over the channel and further scaling. But due to ultra thin source and drain region the series resistance of the device increase. The increase of source/drain region will lower the drain current driving capability. Zhang et al. and Long et al. [3.23], [3.24] proposed recessed source/drain (Re S/D) structure which extends deeper into buried layer of SOI MOSFET can overcome the problem.

From the above research work it has motivate to used the concept of recessed structure and linearly graded mole function

variation of dual metal double gate SOI/SON in a single device structure. The present research work combines the benefit of work function engineered gate (WFEG) [3.25] and recessed source/drain SOI/SON MOSFET. An analytical model for work function engineering gate recessed source/drain SOI/SON MOSFET (WFEG Re S/D SOI/SON MOSFET) is proposed and two dimensional surface potential distribution has been modeled at the front and back channel which is used to examine the behavior of surface potential and threshold voltage.

3.3 Analytical Modelling.

A schematic cross sectional view of our proposed WFEG Re-S/D SOI/SON MOSFET is shown in the figure Fig 3.1. The proposed structure consists of Tantalum(Ta)-Platinum(Pt) binary alloy system as a gate electrode with linearly varying work function from 100%Pt (at source side) to 100%Ta(at drain side). The buried layer of Silicon di oxide (SO_2) of SOI structure is replaced by air when SON structure is considered. The device is a dual metal double gate structure with metal M1 (Pt with a work function of 5.3 eV) and M2 (work function of 4.4eV). The work function is linearly graded along X axis of the channel. The thickness of the front gate oxide, buried layer (t_{box} for SOI and t_{air} for SON MOSFET), channel silicon film and silicon substrate are represent by t_f, $t_{box/air}$, t_{si} and t_{sub} respectively. The source/drain overlap region over buried layer and the recessed thickness of source/drain are depicted by $d_{box/air}$ and t_{rsd} respectively. The proposed model has a channel length of L.

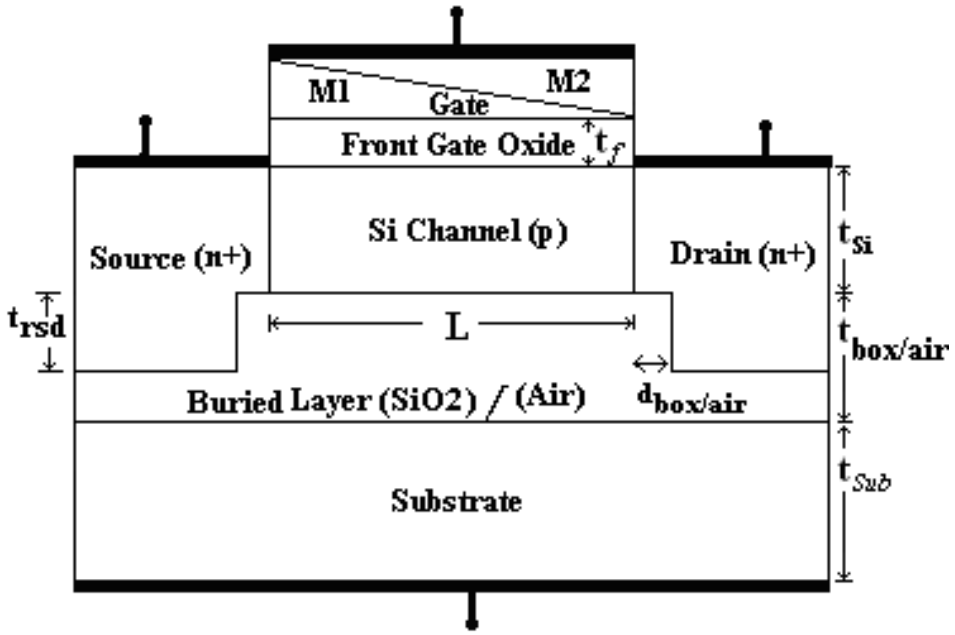

Fig. 3.1 Schematic cross-sectional view of layered recessed S/D SOI/SON MOSFET

T. Nabatame et. al. [3.26] define approximately the work function of arbitrary metal alloy $A_\alpha B_{1-\alpha}$ as

$$\phi_m(\alpha) = \alpha\phi_b + (1-\alpha)\phi_a + \alpha(1-\alpha)\left[\frac{(\phi_b-\phi_a)(\rho_b-\rho_a)}{\lambda\rho_b+(1-\alpha)\rho_1}\right] \quad (3.1)$$

ϕ_a = pure constituent work function of metal A

ϕ_b = pure constituent work function of metal B

α = mole fraction

ρ_a and ρ_b = pure constituent total densities of states for metal A and B respectively.

In the proposed model metal A and B are replaced by Pt and Ta respectively. Effective work function for our proposed model with horizontal channel position along x coordinate for ρ_a equal ρ_b can be defined as

$$\phi_{meff}(\alpha) = (x / L)\phi_b + (1 - x / L)\phi_a \tag{3.2}$$

3.3.1 Surface Potential Distribution

The surface potential distribution of SOI/SON structure is obtained by solving the two dimensional Poisson's equation. The channel doping and influence of the charge carriers on electrostatics in the thin silicon film region are considered to be uniform. The 2D's Poisson's equation before the strong inversion is [3.7],[3.27]

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_a}{\varepsilon_{si}} \; for(0 \le x \le L, 0 \le y \le t_{si}) \tag{3.3}$$

$\phi(x,y)$ = 2D potential profile of the silicon channel.

N_a = Doping concentration of p type channel.

q = Electron charge

ε_{si} = Permittivity of silicon.

The potential profile of the channel is parabolic in nature. This equation can be solved by using Young [3.28] parabolic potential approximation. The 2D potential profile Φ (x,y) is

$$\phi(x,y) = \phi_f(x) + C_1(x)y + C_2(x)y^2 \quad for \quad (0 \le x \le L, 0 \le y \le t_{si}) \qquad (3.4)$$

$\phi(x,y)$ is the front interface surface potential. $C_1(x)$ and $C_2(x)$ are arbitrary constant.

Using the following four boundary condition[3.7],[3.28], along the channel the Poisson's equation can be solved.

(i) The electric field is continuous at the gate, and front oxide interfaces i.e.

$$\varepsilon_{si} \left. \frac{d\varphi(x,y)}{dy} \right|_{y=0} = \varepsilon_{ox} \frac{\varphi_f(x) - (V_{gs} - V_{fbf}(x))}{t_f} \qquad (3.5)$$

Where

The front channel interface flat band voltage $V_{fbf}(x) = \phi_{meff} - \phi_S$

relative permittivity of Silicon = ε_{Si} and

relative permittivity of Silicon di-oxide = ε_{ox}.

(ii) The electric field is continuous at silicon channel and buried layer interface.

$$\varepsilon_{Si} \frac{d\phi(x,y)}{dy} = C_b(V_{Sub1} - \phi_b(x)) + C_{rsd1}(V_{S1} - \phi_b(x)) + C_{rsd2}(V_{D1} - \phi_b(x)) \qquad (3.6)$$

Where the effective bias voltage for substrate(V_{Sub1}), Source(V_{S1}) and Drain(V_{D1}) are given as

$V_{Sub1}=V_{Sub}-V_T \ln(N_{Sub}/N_i)$,

$V_{S1}= V_S - V_T \ln(N_A N_D/N_i^2)$ and

$V_{D1}= V_D - V_T \ln(N_A N_D/N_i^2)$.

$C_b=\varepsilon_{box/air}/t_{box/air}$ is the buried layer capacitance.

The C_{rsd1}, C_{rsd2} are the two modified recessed Source/Drain capacitance of source and drain respectively of our proposed model as Svilic˘ic´ et. al[3.29]

$C_{rsd1}= C_{rsds2}= C_{rsd}$

$$C_{rds} = \frac{\varepsilon_{box/air}}{L(\frac{\pi}{2}+\frac{\pi}{2}\sec h(\frac{t_{rsd}}{d_{box/air}}))}\ln(1+\frac{L}{2d_{box}}) \text{ for } L/2 < t_{rsd} \text{ or } t_{rsd}=0. \quad (3.7)$$

$$C_{rds} = \frac{\varepsilon_{box/air}}{L(\frac{\pi}{2}+\frac{\pi}{2}\sec h(\frac{t_{rsd}}{d_{box/air}}))}\ln(1+\frac{t_{rsd}}{d_{box}}) \quad \text{for } L/2 > t_{rsd} \quad (3.8)$$

(iii) The potential at the source end is built in potential of the channel

$$\phi(0,y) = \phi_f(x) = V_{bi} \quad (3.9)$$

V_{bi} is the built in potential

(iv) The potential at the drain end is the summation of built in potential and drain to source voltage.

$$\phi(L,y) = \phi_f(L) = V_{bi} + V_{DS} \quad (3.10)$$

Now

$$\phi(0,y) = \phi_f(x) \quad (3.11)$$

and

$$\phi(x,t_{si}) = \phi_b(x) = \phi_f(x) + C_1(x)t_{si} + C_2(x)t_{si}^{\ 2} \quad (3.12)$$

Using the equation no (3.4), (3.5) and (3.6) the Poisson's equation(3.3) can be solved

From boundary condition (i) eq. (3.5)

$$\frac{C_f(\phi_f(x)-V_{gs1})}{\varepsilon_{si}} = \left.\frac{d\phi(x,y)}{dy}\right|_{y=0}$$

$$\frac{d\phi(x,y)}{dy} = 0 + C_1(x) + 2yC_2(x)$$

$$\left.\frac{d\phi(x,y)}{dy}\right|_{y=0} = C_1(x) = \frac{C_f(\phi_f(x)-V_{gs1})}{\varepsilon_{si}} \tag{3.13}$$

From boundary condition (ii), equation (3.6) we have

$$\left.\frac{d\phi(x,y)}{dy}\right|_{y=t_{si}} = \frac{C_b}{\varepsilon_{si}}(V_{Sub1}-\phi_b(x)) + \frac{C_{rsd1}}{\varepsilon_{si}}(V_{S1}-\phi_b(x)) + \frac{C_{rsd2}}{\varepsilon_{si}}(V_{D1}-\phi_b(x)) \tag{3.14}$$

and from equation (3.12)

$$\left.\frac{d\phi(x,y)}{dy}\right|_{y=t_{si}} = C_1(x) + 2t_{si}C_2(x) \tag{3.15}$$

From equation (3.12),(3.14) and (3.15) we have

$$2C_2(x) = -\left[\frac{C_f}{\varepsilon_{Si}t_{Si}}\frac{\left(1+\frac{C_b}{C_{Si}}+\frac{C_{rdsl1}}{C_{Si}}+\frac{C_{rds2}}{C_{Si}}\right)}{\left(1+\frac{C_b}{2C_{Si}}+2\frac{C_{rdsl1}}{C_{Si}}+\frac{C_{rds2}}{2C_{Si}}\right)} + \frac{\left(\frac{C_b}{\varepsilon_{Si}}+\frac{C_{rdsl1}}{\varepsilon_{Si}}+\frac{C_{rds2}}{\varepsilon_{Si}}\right)}{t_{Si}\left(1+\frac{C_b}{2\varepsilon_{Si}}+\frac{C_{rdsl1}}{2\varepsilon_{Si}}+\frac{C_{rds2}}{2\varepsilon_{Si}}\right)}\right]\phi_f(x)$$

$$+(V_{GS}+\phi_S-\phi_a)\left[\frac{C_f}{\varepsilon_{Si}t_{Si}}\frac{\left(1+\frac{C_b}{C_{Si}}+\frac{C_{rdsl1}}{C_{Si}}+\frac{C_{rds2}}{C_{Si}}\right)}{\left(1+\frac{C_b}{2C_{Si}}+2\frac{C_{rdsl1}}{C_{Si}}+\frac{C_{rds2}}{2C_{Si}}\right)}\right] + \left[\frac{\left(\frac{C_b}{\varepsilon_{Si}}V_{Sub1}+\frac{C_{rdsl1}}{\varepsilon_{Si}}V_{S1}+\frac{C_{rds2}}{\varepsilon_{Si}}V_{D1}\right)}{\left(1+\frac{C_b}{2C_{Si}}+\frac{C_{rdsl1}}{2C_{Si}}+\frac{C_{rds2}}{2C_{Si}}\right)L}\right] \tag{3.15}$$

$$-\left(\frac{\phi_b-\phi_a}{L}\right)\left[\frac{C_f}{\varepsilon_{Si}t_{Si}}\frac{\left(1+\frac{C_b}{C_{Si}}+\frac{C_{rdsl1}}{C_{Si}}+\frac{C_{rds2}}{C_{Si}}\right)}{\left(1+\frac{C_b}{2C_{Si}}+2\frac{C_{rdsl1}}{C_{Si}}+\frac{C_{rds2}}{2C_{Si}}\right)}\right]x$$

C_{si} is the capacitance of the silicon substrate.

Putting $\phi(0,0)$ in equation (3.4)

$$\frac{d\phi(x,y)}{dx} = \frac{d\phi_f(x)}{dx}$$

$$\frac{d^2\phi(x,y)}{dx^2} = \frac{d^2\phi_f(x)}{dx^2} \tag{3.17}$$

$$\frac{d\phi(x,y)}{dy} = C_1(x) + 2C_2(x)y$$

$$\frac{d^2\phi(x,y)}{dy^2} = 2C_2(x) \tag{3.18}$$

Putting the value of equation (3.16) and (3.18) in the equation (3.3)

$$\frac{d^2\phi_f(x)}{dx^2} + 2C_2(x) = \frac{qN_a}{\varepsilon_{si}} \tag{3.19}$$

The surface potential equation can be obtained by putting the value of $2C_2(x)$ from equation (3.16) in equation (3.19)

$$\frac{d^2\phi_f(x)}{dx^2} - \alpha\phi_f(x) - \delta x = \beta \tag{3.20}$$

Where $\alpha = P_1 + P_2$

$$P_1 = \frac{C_f}{\varepsilon_{Si} t_{Si}} \frac{\left(1+\frac{C_b}{C_{Si}}+\frac{C_{rds1}}{C_{Si}}+\frac{C_{rds2}}{C_{Si}}\right)}{\left(1+\frac{C_b}{2C_{Si}}+2\frac{C_{rds1}}{C_{Si}}+\frac{C_{rds2}}{2C_{Si}}\right)},$$

$$P_2 = \frac{\left(\frac{C_b}{\varepsilon_{Si}}+\frac{C_{rds1}}{\varepsilon_{Si}}+\frac{C_{rds2}}{\varepsilon_{Si}}\right)}{t_{Si}\left(1+\frac{C_b}{2\varepsilon_{Si}}+\frac{C_{rds1}}{2\varepsilon_{Si}}+\frac{C_{rds2}}{2\varepsilon_{Si}}\right)},\ \delta = \left(\frac{\phi_b-\phi_a}{L}\right)P_1$$

And $\beta = \frac{qN_A}{\varepsilon_{Si}} - (V_{GS}+\phi_S-\phi_a)P_1 - \left[\frac{\left(\frac{C_b}{\varepsilon_{Si}}V_{Sub1}+\frac{C_{rds1}}{\varepsilon_{Si}}V_{S1}+\frac{C_{rds2}}{\varepsilon_{Si}}V_{D1}\right)}{\left(1+\frac{C_b}{2C_{Si}}+\frac{C_{rds1}}{2C_{Si}}+\frac{C_{rds2}}{2C_{Si}}\right)L}\right]$

The surface potential equation is a non-homogenous differential equation. Complete solution of front surface potential is obtained by using separation of variable method.

$$\phi_f(x) = A(x)\exp(\kappa x) + B(x)\exp(-\kappa x) - \frac{\delta}{\alpha}x - \frac{\beta}{\alpha} \qquad (3.21)$$

Where

$\kappa = \sqrt{\alpha}$.

This linear x dependent term is due to the consideration of work function engineering. If work function is not related to x then the term vanishes and Equation (3.21) will become a similar expressions as derived for surface potential by W.Long et al.[3.24]. The coefficients A(x) and B(x) are evaluated by using the boundary condition (iii) and (i) i.e. equation (3.9) and (3.10) respectively.

$$A(x)=\frac{\left[V_{DS}+V_{bi}(1-\exp(-\kappa L))+\frac{\beta}{\alpha}(1-\exp(-\kappa L))+\frac{\delta}{\alpha}L\right]}{2\sinh(\kappa L)} \tag{3.22}$$

$$B(x)=\frac{\left[\left(V_{bi}+\frac{\beta}{\alpha}\right)\exp(-\kappa L)-V_{DS}-\frac{\delta}{\alpha}L\right]}{2\sinh(\kappa L)} \tag{3.23}$$

In the recessed source/drain SOI/SON MOSFET, due to the recessed structure there will be a coupling of source/drain to the back channel through buried layer. So the study of the back channel surface potential is also important as front channel surface potential [3.30]. Applying the same procedure for back channel surface potential as used for front channel surface potential with appropriate boundary condition for silicon film and buried layer interface the differential equation obtained is

$$\frac{d^2\phi_b(x)}{dx^2}-\eta\phi_b(x)-\lambda x=\gamma \tag{3.24}$$

Where

$$\eta=\left[\frac{C_b}{\varepsilon_{Si}t_{Si}}+\frac{C_{rds1}}{\varepsilon_{Si}t_{Si}}+\frac{C_{rds2}}{\varepsilon_{Si}t_{Si}}+\frac{C_b}{\varepsilon_{Si}t_{Si}}\left(\frac{1+\frac{C_b}{2C_{Si}}+\frac{C_{rds1}}{2C_{Si}}+\frac{C_{rds2}}{2C_{Si}}}{\left(1+\frac{C_f}{2C_{Si}}\right)}\right)\right]$$

$$\lambda = \left(\frac{\phi_b - \phi_a}{L}\right)\left[1 - \frac{\frac{C_f}{2C_{Si}}}{1+\frac{C_f}{2C_{Si}}}\right]\frac{C_f}{\varepsilon_{Si}t_{Si}}$$

$$\gamma = \frac{qN_A}{\varepsilon_{Si}} - \left(V_{GS} + \phi_S - \phi_a\right)\frac{\frac{C_f}{\varepsilon_{Si}t_{Si}}}{\left(1+\frac{C_f}{2C_{Si}}\right)} - \left[\frac{\left(\frac{C_b}{\varepsilon_{Si}t_{Si}}V_{Sub1} + \frac{C_{rds1}}{\varepsilon_{Si}t_{Si}}V_{S1} + \frac{C_{rds2}}{\varepsilon_{Si}t_{Si}}V_{D1}\right) + \left(\left(\frac{C_b}{2C_{Si}}V_{Sub1} + \frac{C_{rds1}}{2C_{Si}}V_{S1} + \frac{C_{rds2}}{2C_{Si}}V_{D1}\right)\frac{C_f}{\varepsilon_{Si}t_{Si}}\right)}{\left(1+\frac{C_f}{2C_{Si}}\right)}\right]$$

Again using the proper boundary condition at back channel interface, the solution of equation (3.24) can be obtained as

$$\phi_b(x) = A(x)\exp(\chi x) + B(x)\exp(-\chi x) - \frac{\lambda}{\eta}x - \frac{\gamma}{\eta} \qquad (3.25)$$

Where $\chi = \sqrt{\eta}$ and other coefficients are same as previous value.

3.3.2 Threshold voltage modeling.

The minima of the surface potential is used for WFEG ReS/D MOSFETs device to calculate the threshold voltage. When the recessed structure cross a certain limit there is a chance of creating an inversion layer at the back channel interface[3.30] before front channel interface. Here come the necessaties of analutical modeling of the threshold voltage for both front and back channel interface.

Equation (3.21) and (3.25) can be used to calculate the position of the minimum of the surface potential as

$$\left.\frac{d\phi_f(x)}{dx}\right|_{x=x_0} = 0$$

and

$$\left.\frac{d\phi_b(x)}{dx}\right|_{x=x_0} = 0$$

Where, x_0 =position where front interface potential is minimum. and limiting value of x_0 should be between x=0 to x=L

The analytical expression of threshold voltage of front channel using strong inversion condition is

$$V_{thf} = \left[\left\{\frac{qN_A}{\varepsilon_{Si}} - \frac{\alpha}{K_1}\left(2\Psi_b - K_2\right) - K_3\right\}\frac{\varepsilon_{Si}t_{Si}}{C_f} - (\phi_S - \phi_a)\right] \tag{3.26}$$

Where K_1, K_2 and K_3 are constant and given as

$$K_1 = \left[2\left\{(1-\exp(-\kappa L))\sinh(\kappa x_{0f})\right\} - (1-\exp(-\kappa x_{0f}))\right]$$

$$K_2 = \left[\left(V_{bi}\exp(-\kappa x_{0f}) - \frac{\delta}{\alpha}x_{0f}\right) + 2\sinh(\kappa x_{0f})\left(V_{DS} + \frac{\delta}{\alpha}L + V_{bi}(1-\exp(-\kappa L))\right)\right]$$

$$K_3 = \frac{\left(\frac{C_b}{\varepsilon_{Si}}V_{Sub1} + \frac{C_{rds1}}{\varepsilon_{Si}}V_{S1} + \frac{C_{rds2}}{\varepsilon_{Si}}V_{S1}\right)}{\left(1 + \frac{C_b}{C_{Si}} + \frac{2C_{rds}}{C_{Si}}\right)t_{Si}}$$

Similarly, the back interface threshold voltage is

$$V_{thb} = \left[\left\{ \frac{qN_A}{\varepsilon_{Si}} - \frac{\eta}{m_1}\left(2\Psi_b - m_2\right) - m_3 \right\} \frac{\varepsilon_{Si} t_{Si}}{C_f} - (\phi_S - \phi_a) \right] \tag{3.27}$$

Where m_1, m_2 and m_3 are the constants and can be expressed by the modified K_1, K_2 and K_3 with x_{0f} and x_{0b} are the minimum value of front and back channel surface potential respectively.

3.4 Results and explanation.

The characterization and analytical modeling of our proposed Work function engineered Gate (WFEG) Recessed S/D SOI and SON MOSFETs structures are considered to show the superiority of the existing structure. The comparison and the superiority of WFEG structures over the Single gate (SG) and Dual Metal Gate (DMG) MOSFETs have already been carried out [3.25]. The comparison of our proposed structures is carried out with the observation of the normal WFEG SOI/SON MOSFETs. The gate electrode for our model for both SOI and SON structure is a Ta-Pt binary alloy material. The work function is linearly varied with increasing discrete compositions from 100% Pt (from source side) to 100% Ta (at drain side). 2D MEDICI device simulator is used to simulate the model, and the results are used to validate the analytical result [3.31]. The simulations parameters for the model are shown in Table 3.1.

Figure3.2 represents the front surface potential distribution of proposed WFEG Re S/D SOI/SON MOSFET structure concerning different position of channel length. Excessive scaling of the device will

impact in the symmetric nature of the surface potential. The surface potential profile becomes asymmetric in nature, and the minima of the parabola will gradually shift to the drain side instead of remaining middle of the channel length. But our model satisfies the symmetry of the potential profile with gradual reducing of channel length. This shows the device is more immune to DIBL and other charge sharing effects.

Table3.1: Simulation Parameters for Re S/D WFEG SOI/SON structure

Parameters	Values
N_A	10^{21} m^{-3}
N_{SUB}	10^{21} m^{-3}
$N_{S/D}$	10^{26} m^{-3}
t_{Si}	40 nm
t_f	1.5 nm
$t_{box/air}$	200 nm
$d_{box/air}$	3nm
t_{rsd}	30nm
t_{sub}	200nm
V_S	0V

Moreover, the presence of the recessed structure will shift the surface potential minima upward, thereby reducing the threshold voltage and in turn increase the current driving capability. SON structure has lower source to drain barrier potential which will engender lower threshold voltage than SOI device. This property is exhibit in the graph showing

the SON structure surface potential profile minima is above than SOI device structure.

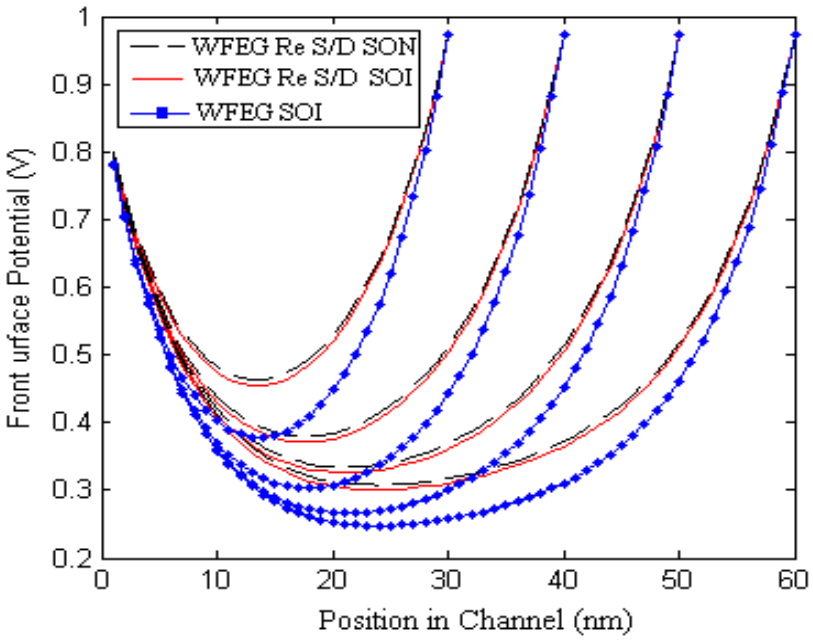

Fig.3.2 Variation of front Surface potential along the channel position of WFEG recessed S/D SOI/SON structures. Vgs=Vds=0.1V

Figure 3.3. depicts the variation of surface potential for different value of drain to source voltage. It shows that the surface potential minima is almost same for different value of drain to source voltage. The model is almost immune to DIBL effect. When this comparison is made with SOI and SON device structure, SON device structure has better performance with comparison to SOI device structure. The analytical result are validate with simulated results from 2D MEDICI TCAD tools. The simulated data are shown as a dot in all the graph where ever it is required. The inversion of the back or front channel can be done by controlling the recessed layer [3.30], which is shown in figure 3.4.

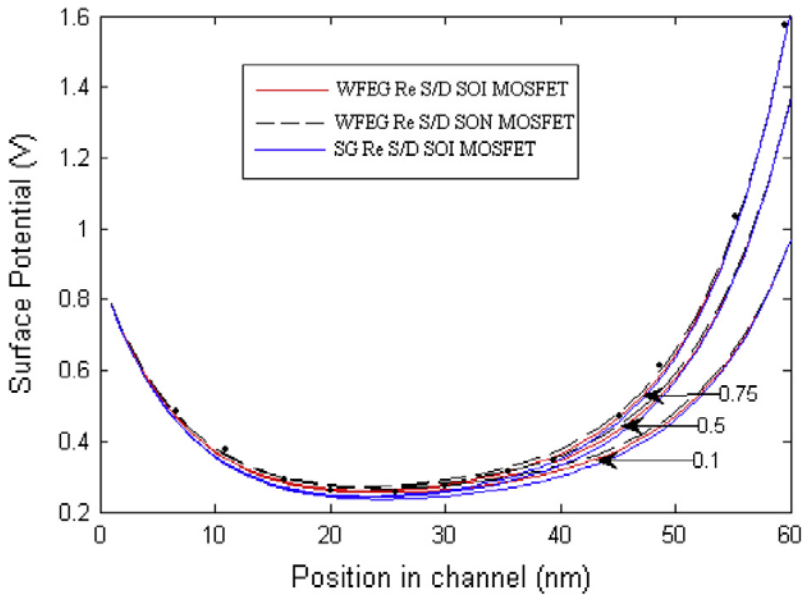

Fig.3.3 Variation of surface potential along the channel position of the single gate (SG) Re S/D SOI, WFEG Re S/D SOI and SON MOSFETs for different values of VDS (0.1V, 0.5V, 0.75V)and VGS =0.1V. Dot indicates TCAD Data for WFEG Re S/D SOI structure for V_{DS}=.75V

Here the recessed layer of t_{rsd}=30nm will invert the back channel before the front channel. This is reflected in the figure where the minimum of the front surface potential deeps below the back surface potential. The continuous work function adjustment in the channel region of a device instead of having a constant work function can reduce the electric field. So a WFEG device will have a less electric field than a device having a constant work function such as single gate SOI, single material double gate SOI [3.25]. If a recessed structure is present in the continuous WFEG then the peak value of the electric

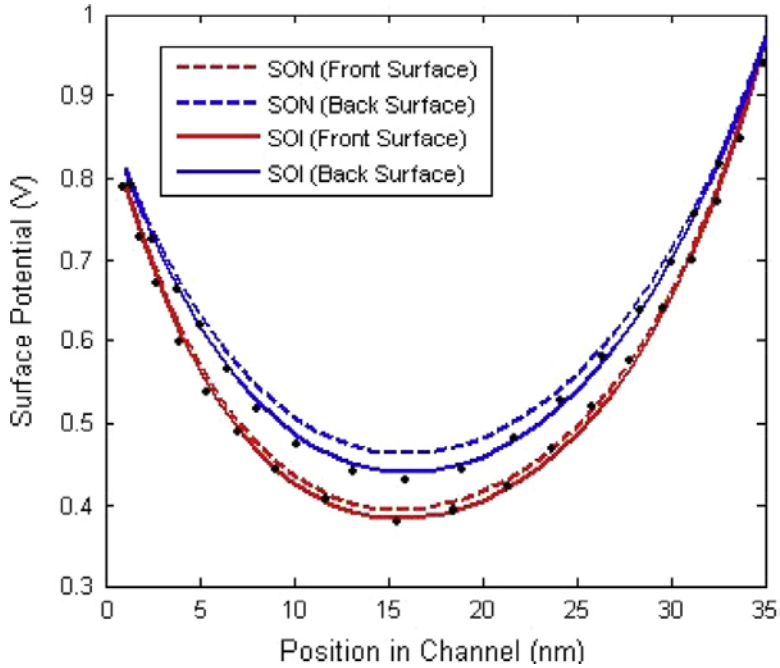

Fig. 3.4 Surface potential variation along the channel position of WFEG Re S/D SOI and SON MOSFETs at Si/Sio_2 and Si/Box interface for V_{GS}= V_{DS}=0.1V. Dot has the same significance as Fig.3.3

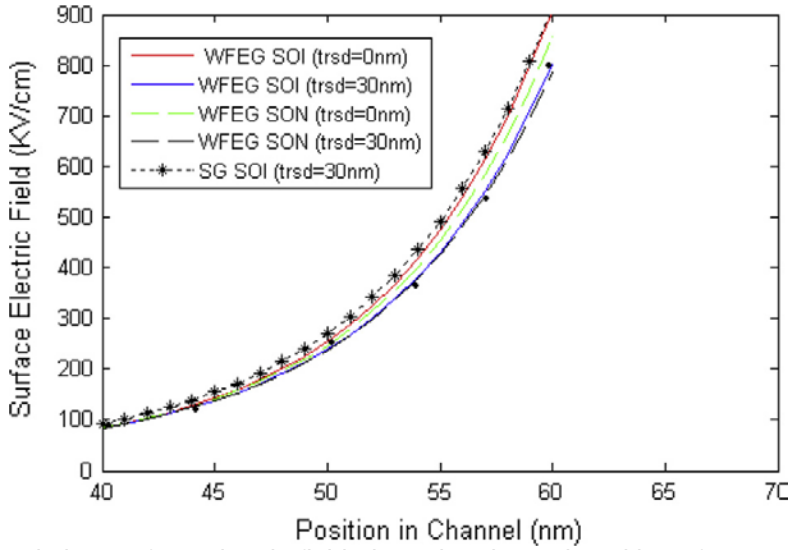

Fig. 3.5 Variation surface electric field along the channel position of SG SOI, WFEG SOI/SON MOSFETs for V_{DS}=V_{GS}=0.1 V with channel length of 60nm. Dot indicates TCAD simulated data.

field reduces further. This condition is pictorially represented in figure 3.5. of our proposed model. This make the device more immune to Hot carrier effect (HCE). The performance is more improve in SON structure as shown in the figure. Here t_{rsd} =0nm indicates a device without recessed structure.

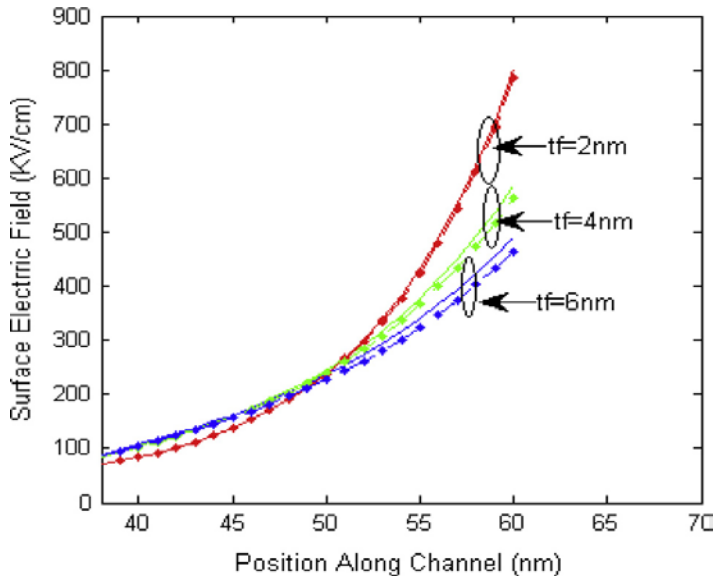

Fig. 3.6 Surface electric field along the channel position of SOI and SON MOSFET for different values of front oxide thickness. Vds=0.1V and Vgs=0.1V with channel length L = 60 nm.

The variation of the surface electric field for various level of front oxide thickness is shown in figure 3.6. The front oxide thickness is inversely proportional to the gate oxide capacitance. As front oxide thickness increases gate oxide capacitance reduces which in turn shift the potential upward thereby reducing the electric field. Variation of threshold voltage along the channel length of WFEG RE-S/D SOI/SON MOSFET device is shown in the figure 3.7. The figure satisfy the condition explained for figure 3.3 where minima of surface potential

shifted upwards will have a low threshold voltage. This figure also satisfies the condition of the low threshold voltage and high driving capability of SON device with SOI device. The dot in the figure indicates the simulated data.

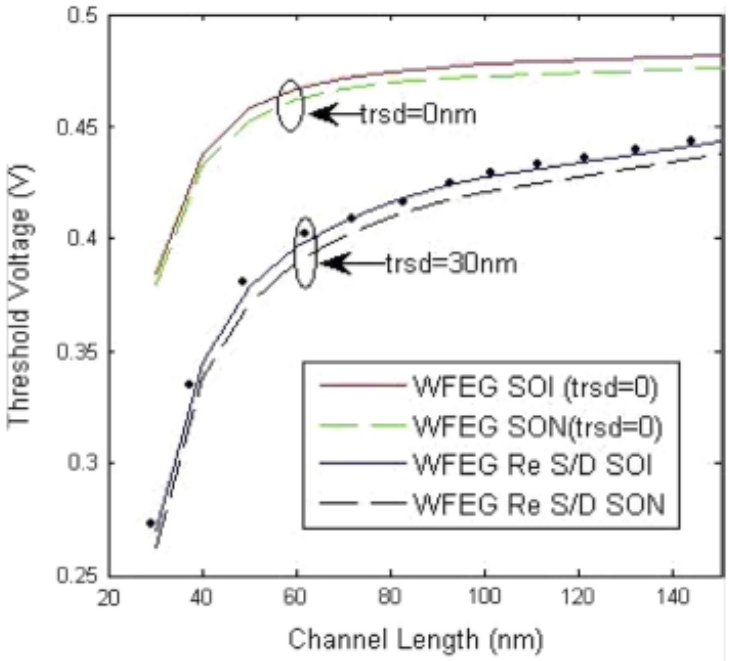

Fig.3.7. Variation of threshold voltage along the channel length of SOI and SON MOSFETs at V_{DS}=0.1V. Dot indicate the TCAD data for WFEG SOI at t_{rsd}=30nm

In a short channel length device, when the device is scaling down the increase in gate oxide thickness will decrease the oxide capacitance. The lower value of capacitance will increase the coupling of the gate voltage to the channel which will decrease the device threshold voltage. This phenomenon is pictorially represented in figure 3.8. Here variation of the threshold voltage is shown for various front oxide thickness. The analysis for effect on threshold voltage due to the variation of buried layer and silicon film thickness are carried out, and it is represented by figure 3.9 and figure 3.10 respectively. Buried layer

capacitance C_b decreases with the increase of the thickness of the buried layer which will reduce the voltage drop at the BOX layer beneath the channel. The effect of the drop in voltage at the BOX layer will decrease the threshold voltage for both the SOI and SON structures. As the channel length decrease the threshold voltage decreases rapidly, and its value increases with the increase in silicon film capacitance. So, to minimize the variation effects of changes in the threshold voltage due to shorter channel length, the channel is kept thin as evince from figure 3.10

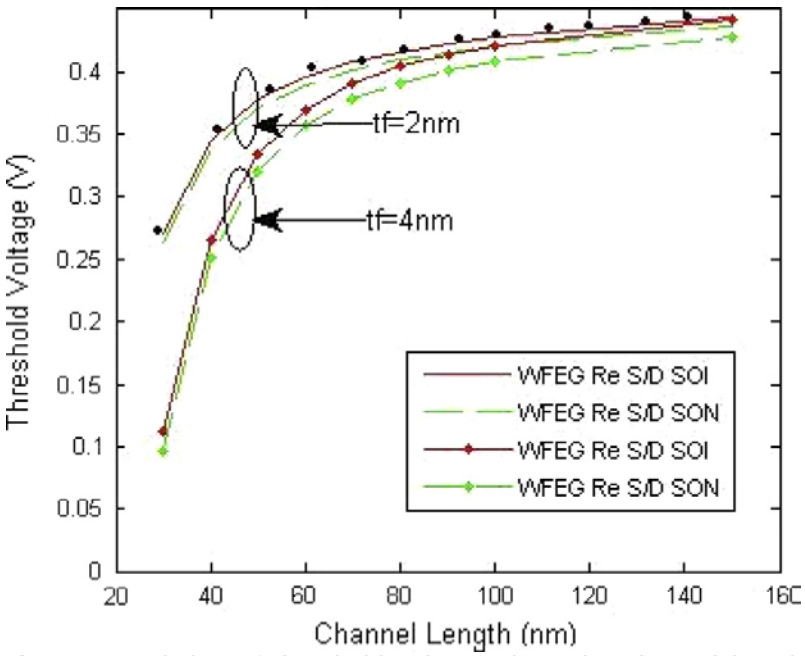

Fig. 3.8. Variation of threshold voltage along the channel length for various front oxide thickness, t_f at V_{DS}=0.1V.

The overall analysis has shown that the DIBL which is the difference between the threshold voltage at linear and saturation region has been reduced in our proposed model. Figure 3.11 shows the

calculated value of DIBL with respect to channel length. DIBL value decreases with increase in the recessed thickness. So the proposed structure is capable of reducing the drain induced short channel effect.

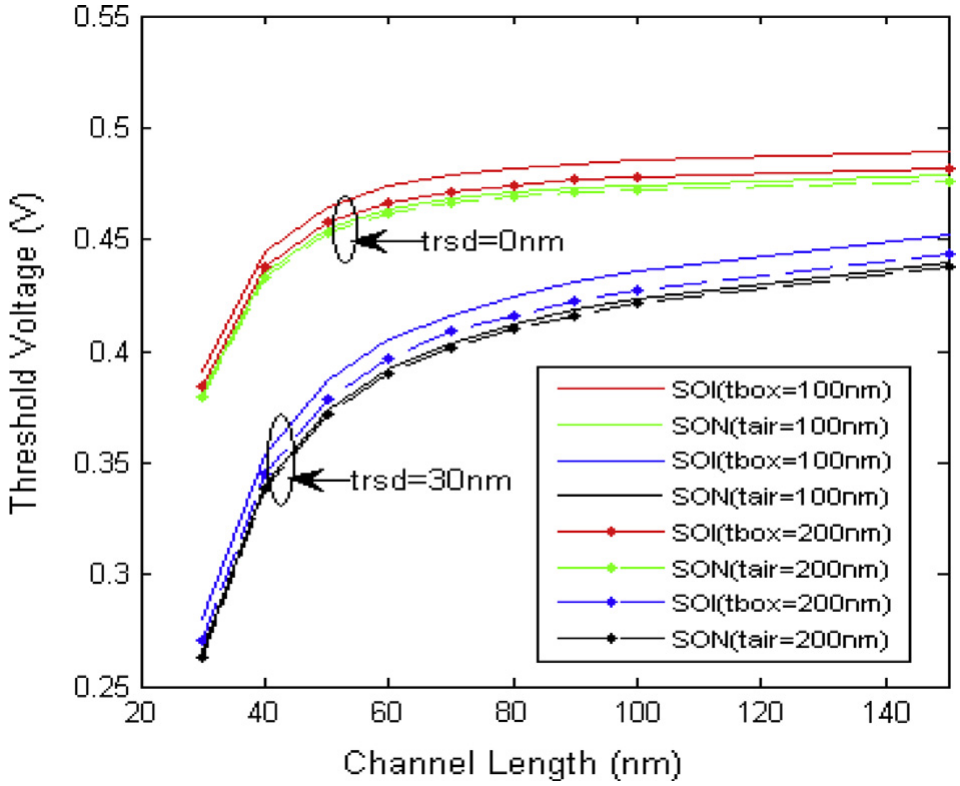

Fig. 3.9. Variation of threshold voltage along the channel length for various buried layer thickness, $t_{box/air}$ at V_{DS}=0.1V.

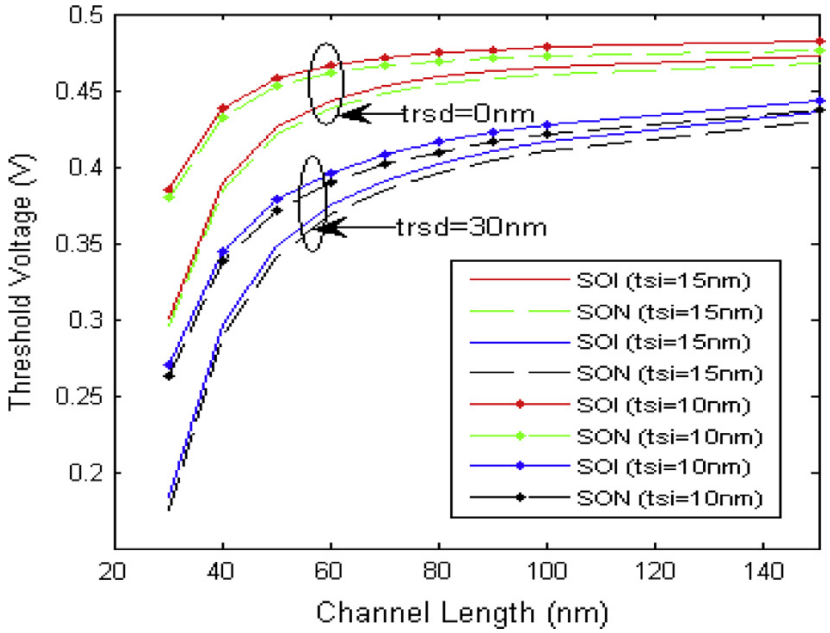

Fig. 3.10. Variation of threshold voltage along the channel length for different silicon film thickness, $t_{Si.}$

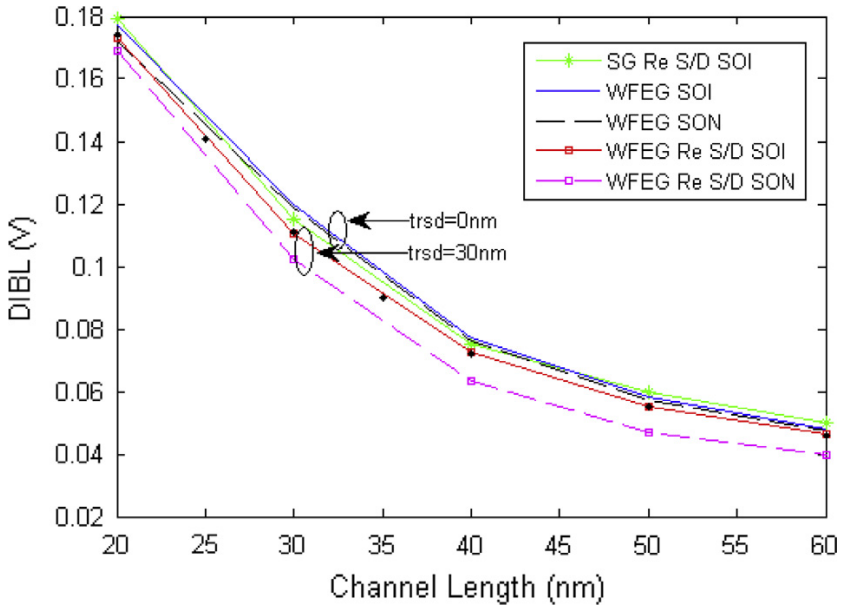

Fig. 3.11. Variation of DIBL with the channel length of WFEG Re S/D SOI and SON MOSFETs at V_{DS}=0.5V.

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Chapter 4

QUANTUM CONFINEMENT EFFECTS ON DMDG SON MOSFET AND THEIR EFFECTS ON DEVICE PERFORMANCE

4.1 Introduction.

Everlasting demand for miniaturization of semiconductor device leads to rapid downscaling of MOSFET in the deep submicrometer region[4.1]. This downscaling will be in the form of [4.2] gate length, gate dielectric thickness, and silicon film thickness. The reduction in the device dimension engendered into several short channel effects which force the researchers to explore a different type of non-conventional geometry of Metal Oxide Semiconductor (MOS) structure both practically and theoretically. The performance of the ultra thin device can be maximized by reducing the short channel effects (SCE) by using ultra thin oxide thickness and high channel doping concentration. This high channel doping and ultra thin oxide generate a very high vertical electric field [4.3]. When the dimension of the channel length approach to the mean distance between carrier collisions i.e. wavelength of electron wave function and thickness of oxide layer reaching few atomic layer, it will create potential well at Silicon(Si)-Silicon di-Oxide($Si0_2$) interface [4.4]]. The potential well will induce quantization of carrier energy. The quantized electron will form Two-Dimensional Electron Gas (2DEG) in double gate device. The

quantization effects will result in different energy levels in the surface potential as shown in figure 4.1 [4.4] and Figure 4.2. The figure shows the electron distribution for quantum and classical model in the perpendicular direction to the interface. Here come the concept of quantum confinement which can be explained by quantum theory [4.5]-[4.8].

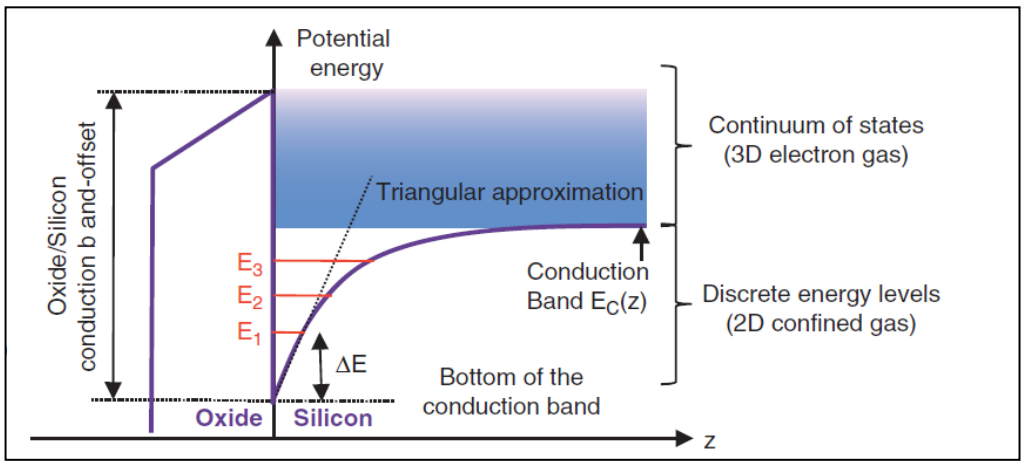

Fig. 4.1 2DEG in a MOSFET

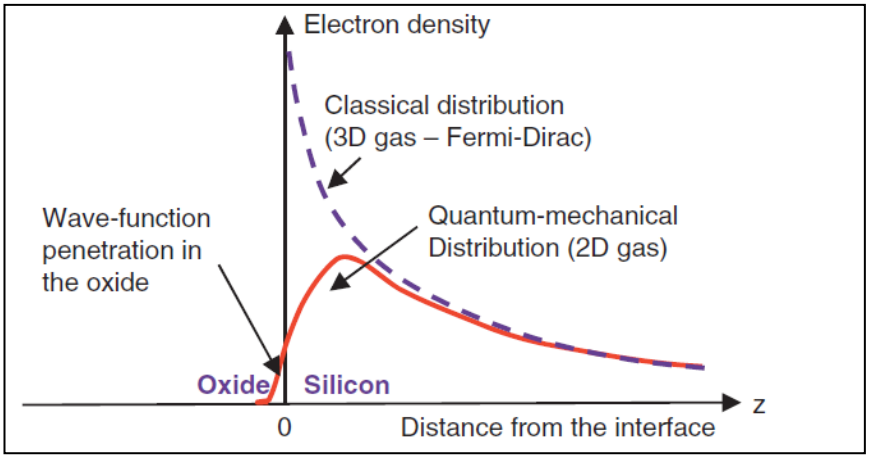

Fig. 4.2 Electron distributions in the direction perpendicular to the interface for the classical and quantum-mechanical models.

In this thesis work, we have incorporated the physics-based analysis of the quantum mechanical effect on Dual Metal Double Gate Silicon on Nothing MOSFET (DMDG SON MOSFET). The analysis is carried on the current-voltage characteristics of the device. The 1-D Schrodinger equation for structural confinement and 2-D Poisson's equation for vertical and horizontal electric field are solved self-consistently in the inversion region[4.9] to derive the charge model and current model. The benefit of the research compared with that of the classical model of semiconductor physics.

4.2 Focus on the research work in the relevant area.

State of the art devices forces the researcher to realize higher speed and higher packing density of MOS devices and give rise to the relentless scaling of device dimension. Downscaling of the device will degrade the MOSFET current driving capability and produces different types of short channel effect, Drain Induced Barrier Lowering (DIBL), Hot carrier effect, leakage current, etc. [4.9]-[4.13]. The increase of charge sharing from source to drain due to a decrease in channel length and DIBL are some of the issues are needed to be considered for ultra thin devices. Scaling of devices less than 45nm regime has given the researchers ample scope to explore in the field of the metal gate electrode, high k dielectric and fully depleted SOI devices. In comparison to bulk CMOS the SOI MOSFET have higher immunity to short channel effect [4.14],[4.15]. It also has reduced junction capacitance, reduce coupling effect, high radiation tolerance, lower

propagation delay and improved subthreshold characteristics [4.16],[4.17]. The introduction of step function in channel position by using two metal gate with different work function suppressed the short channel effect and enhanced the transconductance in the MOS device [4.18]-[4.20]. This brings the new concept of Dual Metal Gate (DMG) SOI MOSFET. G.Reddy et. al [4.21] proposed a new structure Dual Metal Double Gate (DMDG) SOI MOSFET which incorporates the benefits of both DMG and Dual Gate[4.22]. DMDG SOI MOSFET structure has excellent property in suppressing SCE, but it has a limitation in threshold voltage roll off and reduction in subthreshold slope [4.23]. M. Jurczak et. al [4.24] and J. Pretet et. al. [4.25] proposed improved SOI structure with a dielectric material of dielectric constant of one. Air having the dielectric constant of one will replace the buried layer of SOI structure. This new structure is known as Silicon on Nothing (SON). The parasitic capacitance between the substrate and the source/drain is reduced, and this leads to improvement in reduction of SCE and high speed device [4.25]-[4.27]. As the downscaling of the device continue and when the device dimensions can be compared to electron de Broglie wavelength then the classical model [4.27],[4.28] is not sufficient to delineate charge inversion phenomena and potential profile of the device. Here quantum size become relevant and quantization of electron take place [4.29],[4.30]. However reducing the device dimension by the extreme measure will build up different short channel effect and parasitic effect. Quantization of carrier is one such effect. Structural confinement for low dimensional size and electrical confinement for high doping shows up quantization of carrier, which will split carrier energy into different

levels [4.31]. Quantization deviates the characteristics of the device significantly from the classical model which can be explained by the quantum theory The new compact structure developed, has challenges to describe its physical phenomena with reference to the device integration[4.5].[4.6]. Lots of work has been done on classical approach of analytical modeling on Double Gate structure. But very few or limited exploration have done on device structure based on quantum effect. Yatao Ma et al [4.32] first work on quantum mechanical effect on analytical charge and current model for deep submicrometer MOSFET. Analytical modeling of DG MOSFET with arbitrary Si thickness based on quantization and volume inversion was done by Lixin Ge et al [4.33]. It is a physic based quantum model considering electric field dependence and gate-gate charge coupling. D. Munteanu et al [4.34] has proposed a quantum model for drain current and demonstrated its application in circuit simulation. The first model incorporating quantum effect and short channel effect was proposed by D. Munteanu [4.35]. This model work fine for both asymmetric and symmetric structure of Double Gate Field Effect Transistor (DGFET) for film thickness less than 10nm and dielectric permittivity greater than 10nm. Later in 2011 the same author [4.36] proposed a quantum drain current model for Independent DG MOSFET. The model explain the drift diffusion transport of the carrier and its application to the various circuit. Quantum analytical threshold voltage model for DMDG SON MOSFET was proposed by Sourav Naskar et al [4.37]. The model present a physics base description of short channel effect and quantum effect on DMDG SON structure. Hence quantum confinement effect has to be

considered in the modelling of the MOSFET device. The 2-D Poisson and 1-D Schrodinger equation has to be solved in the weak inversion region to obtain the potential and charge distribution.

4.3 Analytical Modeling and Simulation

4.3.1 Device Structure.

The proposed model for DMDG SON MOSFET structure is shown in Figure 4.3. It consists of two gate front and back gate. The front gate comprises of two metal, M_1 of length L_1 (with p^+ polysilicon and work function of 5.25 eV) and M_2 of length L_2 (with n^+ polysilicon and the work function of 4.17 eV).The back gate consists of metal M_2. t_f,t_{si} and t_b are the thickness of the front gate oxide (SiO_2), thin-film Si and back gate buried air layer (air) respectively. The front gate consists of both asymmetric (metal M_1) and symmetric (metal M_2) double gate in a single structure. The metal M_1 is asymmetric because of two different work function with respect to back gate and M_2 is symmetric because of same work function with respect to back gate. Due to the downscaling of the device, it becomes ultra thin, and quantization of carrier take place. So we are trying to incorporate quantum effect in obtaining the current and charge distribution for symmetric and asymmetric double gate structure. This analysis is done in a single structure instead of doing separately for the symmetric and asymmetric gate as done earlier [4.38],[4.39].

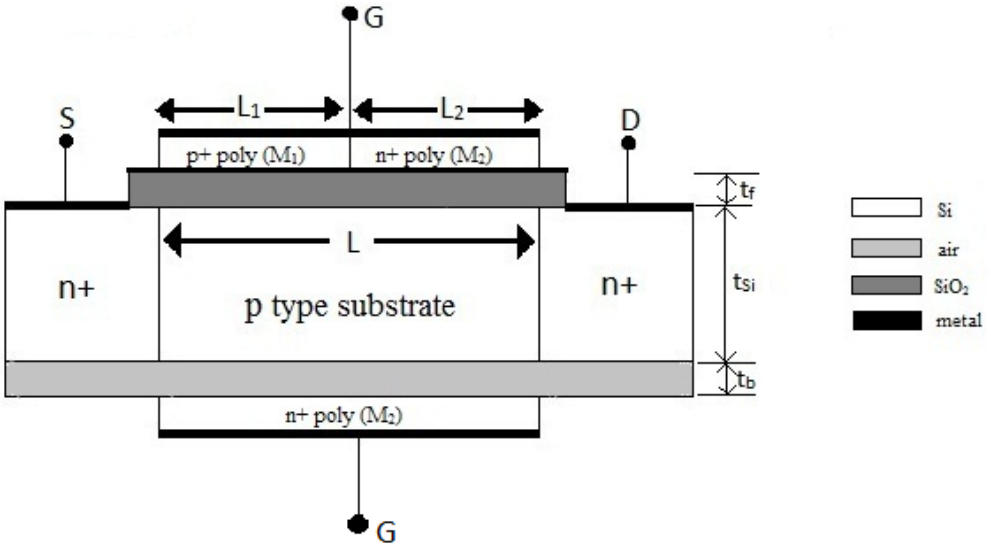

Fig. 4.3 DMDG SON MOSFET device structure.

4.3.2 Inversion Charge Model.

Ultra thin devices give rise to quantization of carriers due quantum confinement. Confinement can be of structural or electrical. Structural confinement is due to ultra-thin nature of the film, and electrical confinement of carriers is due to the transverse electric field [4.40]. So 2D Poisson's equation and 1D Schrödinger equation have to be solved self-consistently to analyze the structure shown in figure 4.3. [4.39],[4.41],[4.42].

In the inversion charge model, there are two types of well within the structure, rectangular and structural well as shown in figure 4.4 [4.43]. For the region $0<x<L_1$ it will be rectangular well with perturbation ofΔE due to asymmetric nature of the gate and for the region $L_1<x<L_2$ it will be triangular well due symmetric nature of the gate.

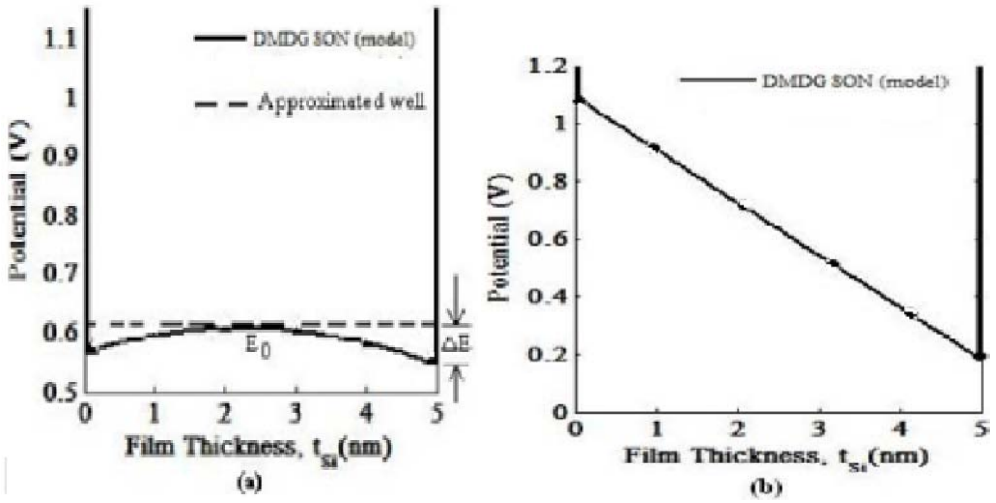

Fig. 4.4 Potential well in the channel along film thickness. (a)Rectangular well with perturbation ΔE in gate M_1 (b) Triangular well under gate M_2

The total inversion charge across the channel is calculated by solving the Schrodinger equation for rectangular well and triangular well [4.44] separately. The final inversion charge for the silicon's six energy valley comprising of two longitudinal and four transverse in nature[4.4],[4.38],[4.43].[4.44] will be

$$Q_i(x) = \frac{qkT}{\pi\hbar^2}\sum_i \left[m_l^* g_l \ln\left[1+\exp\left(-\beta\left(\tilde{E}_l^{\,i} + \frac{E_g}{2} - \phi_S(x) + V_F(x)\right)\right)\right] + \sqrt{m_l^* m_t^*}\, g_t \ln\left[1+\exp\left(-\beta\left(\tilde{E}_t^{\,i} + \frac{E_g}{2} - \phi_S(x) + V_F(x)\right)\right)\right]\right] \quad (4.1)$$

where $V_F(x)$ is the Quasi-Fermi level given by [4.21]

$$V_F(x) = -\frac{kT}{q}\left(\frac{m}{n}\right) \times \ln\left[\exp\left\{\left(-\frac{V_D\left(m/n\right)^{-1}}{kT/q}\right)-1\right\}\left(\frac{x}{L}\right)^{\frac{C}{V_g - V_{FB}}}+1\right]\left(at_{si}\right)^{\frac{V_D}{3c}} \quad (4.2)$$

where
m/n=2+bx(V_G-V_{FB}), a=0.2nm^{-1}, b=0.05V^{-1}, C==1V^{-1}.

$\hbar$ =h/2π, h is the planks constant

E= Energy of the electron

m_l^*= Longitudinal effective mass

m_t^*= Transverse mass

i= natural positive number

Now for the region 0<x<L_1 in the rectangular well, the inversion charge will be

$$Q_{il}(x) = \frac{qkT}{\pi\hbar^2}\sum_i \left[\begin{array}{l} m_l^* g_l \ln\left[1+\exp\left(-\beta\left(\tilde{E}^{\,i}_{rec,l} + \frac{E_g}{2} - \phi_{S1}(x) + V_{F1}(x)\right)\right)\right] \\ +\sqrt{m_l^* m_t^*}\, g_t \ln\left[1+\exp\left(-\beta\left(\tilde{E}^{\,i}_{rec,t} + \frac{E_g}{2} - \phi_{S1}(x) + V_{F1}(x)\right)\right)\right] \end{array}\right] \quad (4.3)$$

Where $\tilde{E}^{\,i}_{rec,l,t} = E_{rec,l,t} + \Delta E^i$

$E_{rec,l,t}$ is the overall energy level of the electron and can be calculated by solving the 1-D Schrodinger equation using separation of variable method [4.43],[4.44]

$$\frac{\partial^2\psi}{\partial y^2}+\frac{2qm_{l,t}^*}{\hbar^2}(E-E_0)\psi=0$$

$E_0=E_{g/2}$ -Φ(x-t_f/2), and Ψ is the electron wave function.

$$E_{rec,l,t}^i=E_0+\frac{\hbar^2\pi^2 i^2}{2qm_{l,t}^* t_{si}^2}$$

ΔE^i is present due to the 1st order perturbation for external electric field.

$\Delta E^i=\left\langle\psi_i^*\left|H\right|\psi_i\right\rangle$, H is the Hamiltonian operator and is given as H=-q(C_{11}y+$C_{12}$$y^2$) and ψ_i^* is the complex conjugate of electron wave function

$\Delta E^i==\frac{C_{22}t_{si}^2}{6}\left[1+\frac{3}{\pi^2 i^2}\right]$ i=1,2,3.....; are side band index

for the model all the electron are confined to the first sideband only with decreasing channel width and hence we consider i=1.

The value of the C_{11},C_{12} and C_{22} can be calculated by solving 2D Poisson equation of DMDG structure.

For the region L_1<x<L_2 the potential profile is triangular in nature, hence the total inversion charge is

$$Q_{i2}(x)=\frac{qkT}{\pi\hbar^2}\sum_i\left[\begin{array}{l}m_l^* g_l\ln\left[1+\exp\left(-\beta\left(\tilde{E}_{trian,l}^{\,i}+\frac{E_g}{2}-\phi_{S2}(x)+V_{F2}(x)\right)\right)\right]\\+\sqrt{m_l^* m_t^*}\,g_t\ln\left[1+\exp\left(-\beta\left(\tilde{E}_{trian,t}^{\,i}+\frac{E_g}{2}-\phi_{S2}(x)+V_{F2}(x)\right)\right)\right]\end{array}\right] \quad (4.4)$$

The solution of the Eigenvalue gives the Airy function which is the solution of Schrodinger equation in the triangular potential well. The Eigenvalue is given [4.43] as

$$E^{i}_{trian,l,t} = \left(\frac{\hbar^2}{2qm^*_{l,t}} \right)^{1/3} \left(\frac{3\pi q \left| \xi_{s2} \right|}{2} \left(j - \frac{1}{4} \right) \right)^{2/3}$$, j=1,2,3.... are

subband's index. The surface electric field under M_2 is given by

$$\xi_{s2} = -\frac{d\left(\phi_{s2}(x) + C_{21}(x)y + C_{22}(x)\right)}{dx}\bigg|_{y=0} = -C_{21}(x)$$

$\phi_{s2}(x)$ is the surface potential under the gate M_2.

The surface potential distribution of SON structure and constant C_{11},C_{12},C_{21} and C_{22} are obtained by solving the two-dimensional Poisson's equation [4.43].

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}} \tag{4.5}$$

$\phi(x,y)$ = 2D potential profile of the silicon channel.

N_a = Doping concentration of p-type channel.

ε_{si} = Permittivity of silicon.

According to Young [4,15] the 2D potential profile Φ (x,y) can be expressed as is

$$\phi(x,y) = \phi_s(x) + C_1(x)y + C_2(x)y^2 \tag{4.6}$$

$\phi_s(x)$ is the surface potential. $C_1$and C_2 are arbitrary constant.

The front gate of the DMDG SON MOSFET comprises of two metal of different work function. So the potential under the two region [4.21]

$$\phi_1(x,y) = \phi_{s1}(x) + C_{11}(x)y + C_{12}(x)y^2, \quad for 0 \le x \le L_1, 0 \le y \le t_{si} \tag{4.7}$$

$$\phi_2(x,y) = \phi_{s2}(x) + C_{21}(x)y + C_{22}(x)y^2, \quad for L_1 \le x \le L, 0 \le y \le t_{si} \tag{4.8}$$

where C_{11},C_{12},$C_{21}$and C_{22} are function of x and are arbitrary coefficient. These unknown value can be found out by applying the following boundary condition [4.43]

(i) The electric field is continuous at the gate, and front oxide interfaces i.e.

$$\varepsilon_{si} \left.\frac{d\phi_1(x,y)}{dy}\right|_{y=0} = \varepsilon_{ox} \frac{\phi_{s1}(x) - V'_{G1}}{t_f} under M_1 \tag{4.9}$$

$$\varepsilon_{si} \left.\frac{d\phi_2(x,y)}{dy}\right|_{y=0} = \varepsilon_{ox} \frac{\phi_{s2}(x) - V'_{G2}}{t_f} under M_2 \tag{4.10}$$

(ii) The electric field is continuous at silicon channel and buried layer interface.

$$\varepsilon_{si} \left.\frac{d\phi_1(x,y)}{dy}\right|_{y=t_{si}} = \varepsilon_{air} \frac{V'_{GSb} - \phi_B(x)}{t_b} under M_1 \tag{4.11}$$

$$\varepsilon_{si} \left.\frac{d\phi_2(x,y)}{dy}\right|_{y=t_{si}} = \varepsilon_{air} \frac{V'_{GSb}(x) - \phi_B(x)}{t_b} under M_2 \tag{4.12}$$

(iii) The potential at the source end is built in potential of the channel

$$\phi_1(0,0) = \phi_{s1}(0) = V_{bi} \tag{4.13}$$

V_{bi} is the built in potential

(iv) The potential at the drain end is the summation of built in potential and drain to source voltage.

$$\phi_2(L_1 + L_2, 0) = \phi_{s2}(L_1 + L_2) = V_{bi} + V_{DS} \tag{4.14}$$

where

ε_{OX}= dielectric constant of the oxide layer

$V_{G1}^{'}$ = V_{GS} -V_{FB1}, $V_{G2}^{'}$ = V_{GS} -V_{FB2} , V_{Gs}= Gate to source bias voltage.

ε_{air}= dielectric constant of the back gate oxide layer (air)

$\phi_B(x)$ = potential function along the back gate oxide -silicon interface.

$V_{GSb}^{'}$ = V_{GS}-V_{FBb}, V_{FBb} is the back gate flat -band voltage.

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - V_{GS1}^{'}}{t_f} \tag{4.16}$$

$$C_{12}(x) = \frac{V_{GSb}^{'} - \phi_{s1}(x)\left[1 + \frac{C_{ox}}{C_{air}} + \frac{C_{ox}}{C_{si}}\right] + V_{GS1}^{'}\left[\frac{C_{ox}}{C_{air}} + \frac{C_{ox}}{C_{si}}\right]}{t_{si}^2\left[1 + 2\frac{C_{si}}{C_{air}}\right]} \tag{4.17}$$

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\phi_{s2}(x) - V_{GS2}^{'}}{t_f} \tag{4.18}$$

$$C_{22}(x)=\frac{V_{GSb}^{'}-\phi_{s2}(x)\left[1+\frac{C_{ox}}{C_{air}}+\frac{C_{ox}}{C_{si}}\right]+V_{GS2}^{'}\left[\frac{C_{ox}}{C_{air}}+\frac{C_{ox}}{C_{si}}\right]}{t_{si}^{2}\left[1+2\frac{C_{si}}{C_{air}}\right]} \tag{4.19}$$

Surface potentials are obtained by substituting these coefficients in the Poisson equation (4.5) and solving it

$$\phi_{S1}(x)=Ae^{\eta x}+Be^{-\eta x}-\frac{\beta_1}{\alpha} \tag{4.20}$$

$$\phi_{S2}(x)=Ce^{\eta(x-L_1)}+De^{-\eta(x-L_1)}-\frac{\beta_2}{\alpha} \tag{4.21}$$

where the constant as per [4.43] are

$$A=\left(V_{bi}+V_{DS}+\sigma_2\right)-\left(V_{bi}+\sigma_1\right)e^{-\eta L}+\left(\sigma_1-\sigma_2\right)\cosh\left(\eta L_2\right)\left\{\frac{e^{-\eta L}}{1-e^{-2\eta L}}\right\}$$

$$B=\frac{\left(V_{bi}+\sigma_1\right)-\left(V_{bi}+V_{DS}+\sigma_2\right)e^{-\eta L}-\left(\sigma_1-\sigma_2\right)\cosh\left(\eta L_2\right)e^{-\eta L}}{1-e^{-2\eta L}}$$

$$C=Ae^{\eta L_1}-\frac{\left(\sigma_1-\sigma_2\right)}{2},\sigma_1=\frac{\beta_1}{\alpha},\sigma_2=\frac{\beta_2}{\alpha}$$

$$D=Be^{-\eta L_1}-\frac{\left(\sigma_1-\sigma_2\right)}{2},\eta=\sqrt{\alpha}$$

$$\alpha=\frac{2\left[1+\frac{C_f}{C_{Si}}+\frac{C_f}{C_b}\right]}{t_{Si}^{2}\left(1+\frac{2C_{Si}}{C_b}\right)}\qquad \beta_1=\frac{qN_A}{\varepsilon_{Si}}-\frac{2V_{G1}^{'}\left[\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right]}{t_{Si}^{2}\left(1+\frac{2C_{Si}}{C_b}\right)}-\frac{2V_{GSb}^{'}}{t_{Si}^{2}\left(1+\frac{2C_{Si}}{C_b}\right)}$$

,

$$\beta_2 = \frac{qN_A}{\varepsilon_{Si}} - \frac{2V_{G2}^{'}\left[\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)} - \frac{2V_{GSb}^{'}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}$$

4.3.3 Drain Current model.

Drift and diffusion are the two component of the drain current in MOSFET device. The drift current is due to the motion of the charge because of the external electric field and diffusion current is due to the concentration gradient. When quantization of carries start due to scaling down of the device both in length and thickness, the carriers are residing in the first subband instead of 3D bulk [4.43]. The energy will be close to rectangular well for 0nm to L_1nm and triangular well for L_1nm to Lnm.

The Quasi Fermi potential [4.4],[4.21],[4.39] will be

for the region $0<x<L_1$

$$V_{F1}(x) = -\frac{kT}{q}\left(\frac{m}{n}\right)_1 \times \ln\left[\exp\left\{\left(-\frac{V_D\left(m/n\right)_1^{-1}}{kT/q}\right)-1\right\}\left(\frac{x}{L}\right)^{\frac{C}{V_g-V_{FB1}}}+1\right]\left(at_{si}\right)^{\frac{V_D}{3c}} \quad (4.22)$$

where $(m/n)_1=2+bx(V_G-V_{FB1})$

for the region $L_1<x<L$

$$V_{F2}(x) = -\frac{kT}{q}\left(\frac{m}{n}\right)_2 \times \ln\left[\exp\left\{\left(-\frac{V_D\left(m/n\right)_2^{-1}}{kT/q}\right)-1\right\}\left(\frac{x}{L}\right)^{\frac{C}{V_g-V_{FB2}}}+1\right]\left(at_{si}\right)^{\frac{V_D}{3c}} \quad (4.23)$$

The current densities is express as [4.45]

$$J_n(x) = -Q_i(x) \times \mu \times \frac{dV_F(x)}{dx} \tag{4.24}$$

Where,

$J_n(x)$ = Current density

$Q_i(x)$ = Charge density of electrons

μ = Effective mobility of electrons in the channel

$V_F(x)$ = Quasi-Fermi level

So for the region $0<x<L_1$ the current density is

$$J_{n1} = -Q_{i1}(x)\mu \times \frac{dV_{F1}(x)}{dx} \tag{4.25}$$

and for the region $L_1<x<L$

$$J_{n2} = -Q_{i2}(x)\mu \times \frac{dV_{F2}(x)}{dx} \tag{4.26}$$

Now the total drain current

$$I = W\int_0^L J_n(x)dx$$

$$= W\left[\int_0^{L_1} J_{n1}(x)dx + \int_{L_1}^{L} J_{n2}(x)dx\right]$$

$$= \left[I_1 + I_2\right]$$

so by using equation (4.25) and (4.26) we can have

$$\int_0^{L_1} I_{d1}dx = -\mu W \int_0^{V_{F1}} Q_{i1}(x)dV_{F1}(x) \tag{4.27}$$

$$\int_{L_1}^{L} I_{d2}dx = -\mu W \int_{V_{F1}}^{V_D} Q_{i2}(x)dV_{F2}(x) \tag{4.28}$$

Now for the region $0<x<L_1$

$$\int_0^{L_1} I_{d1}(x)dx = -\mu W \frac{qKT}{\pi\hbar^2} \times \left[\left[\int_0^{V_{F1}} m_l^* \times g_l \times \ln\left[1+\exp\left\{ -\beta \left(\begin{matrix} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} + V_{F1}(x) \end{matrix} \right) \right\} \right] dV_{F1}(x) \right] + \left[\int_0^{V_{F1}} \sqrt{m_l^* m_t^*} \times g_l \times \ln\left[1+\exp\left\{ -\beta \left(\begin{matrix} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} + V_{F1}(x) \end{matrix} \right) \right\} \right] dV_{F1}(x) \right] \right] \tag{4.29}$$

and for the region $L_1<x<L$

$$\int_{L_1}^{L} I_{d2}(x)dx = -\mu W \frac{qKT}{\pi\hbar^2} \times \left[\left[\int_{V_{F1}}^{V_D} m_l^* \times g_l \times \ln\left[1+\exp\left\{ -\beta \left(\begin{matrix} E_{l,trian}^i \\ +\frac{E_g}{2} - \phi_{s2,\min} + V_{F2}(x) \end{matrix} \right) \right\} \right] dV_{F2}(x) \right] + \left[\int_{V_{F1}}^{V_D} \sqrt{m_l^* m_t^*} \times g_l \times \ln\left[1+\exp\left\{ -\beta \left(\begin{matrix} E_{l,trian}^i \\ +\frac{E_g}{2} - \phi_{s2,\min} + V_{F2}(x) \end{matrix} \right) \right\} \right] dV_{F2}(x) \right] \right] \tag{4.30}$$

For inversion region ln(1+x) is approximately equal to ln(x), hence equation (4.29) and (4.30) can be written as

$$\int_0^{L_1} I_{d1}(x)dx = -\mu W \frac{qKT}{\pi\hbar^2} \times \left[\begin{array}{l} \left[\int_0^{V_{F1}} m_l^* \times g_l \times \left[\left\{ -\beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} + V_{F1}(x) \end{array} \right) \right\} \right] dV_{F1}(x) \right] + \\ \left[\int_0^{V_{F1}} \sqrt{m_l^* m_t^*} \times g_l \times \left[\left\{ -\beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} + V_{F1}(x) \end{array} \right) \right\} \right] dV_{F1}(x) \right] \end{array} \right] \quad (4.31)$$

$$\int_{L_1}^{L} I_{d2}(x)dx = -\mu W \frac{qKT}{\pi\hbar^2} \times \left[\begin{array}{l} \left[\int_{V_{F1}}^{V_D} m_l^* \times g_l \times \left[\left\{ -\beta \left(\begin{array}{l} E_{l,trian}^i \\ +\frac{E_g}{2} - \phi_{s2,\min} + V_{F2}(x) \end{array} \right) \right\} \right] dV_{F2}(x) \right] + \\ \left[\int_{V_{F1}}^{V_D} \sqrt{m_l^* m_t^*} \times g_l \times \left[\left\{ -\beta \left(\begin{array}{l} E_{l,trian}^i \\ +\frac{E_g}{2} - \phi_{s2,\min} + V_{F2}(x) \end{array} \right) \right\} \right] dV_{F2}(x) \right] \end{array} \right] \quad (4.32)$$

Integrating equation (4.38) and (4.39) we get the drain current for the two region (0 to L_1 as I_{d1} and L_1 to L as I_{d2}) of the DMDG structure as

$$I_{d1} = -\mu \times \frac{W}{L_1} \times \frac{qKT}{\pi\hbar^2} \times \left[\begin{array}{l} m_l^* \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} \end{array} \right) \times V_{F1}(x) + \frac{V_{F1}^2}{2} \right\} + \\ \sqrt{m_l^* m_t^*} \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} \end{array} \right) \times V_{F1}(x) + \frac{V_{F1}^2}{2} \right\} \end{array} \right] \quad (4.34)$$

$$I_{d2} = -\mu \times \frac{W}{L - L_1} \times \frac{qKT}{\pi \hbar^2} \times \left[\begin{array}{l} m_l^* \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ + \dfrac{E_g}{2} - \phi_{s2,\min} \end{array} \right) \times (V_D - V_{F1}) + \dfrac{V_D^2 - V_{F1}^2}{2} \right\} + \\ \sqrt{m_l^* m_t^*} \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ + \dfrac{E_g}{2} - \phi_{s2,\min} \end{array} \right) \times (V_D - V_{F1}) + \dfrac{V_D^2 - V_{F1}^2}{2} \right\} \end{array} \right] \quad (4.35)$$

Total drain current for the device is

$$I_d = I_{d1} + I_{d2}$$

Substituting the value of the drain current from the equation (4.41) and (4.42), we get total current as

$$I_d = -\mu \times \frac{W}{L} \times \frac{qKT}{\pi \hbar^2} \times \left[\begin{array}{l} m_l^* \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ + \dfrac{E_g}{2} - \phi_{s1,\min} \end{array} \right) \times V_{F1}(x) + \dfrac{V_{F1}^2}{2} \right\} + \\ \sqrt{m_l^* m_t^*} \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ + \dfrac{E_g}{2} - \phi_{s1,\min} \end{array} \right) \times V_{F1}(x) + \dfrac{V_{F1}^2}{2} \right\} \\ + m_l^* \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ + \dfrac{E_g}{2} - \phi_{s2,\min} \end{array} \right) \times (V_D - V_{F1}) + \dfrac{V_D^2 - V_{F1}^2}{2} \right\} + \\ \sqrt{m_l^* m_t^*} \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ + \dfrac{E_g}{2} - \phi_{s2,\min} \end{array} \right) \times (V_D - V_{F1}) + \dfrac{V_D^2 - V_{F1}^2}{2} \right\} \end{array} \right] \quad (4.36)$$

4.4 Result and Discussion

The work consists of both the features of the symmetrical and asymmetrical gate in a single DMDG SON MOSFET structure. Figure 4.1 is used for doing the analytical analysis. Here we have tried to incorporate the quantum mechanical effect while in the analysis of drain current. The analytical modeling is represented pictorially in the form of graph and has made a comparison with the existing classical model [4.21] to show the benefit of our work. Table 4.1 Shows the parameter used to do the analysis for the DMDG structure. Figure 4.5 shows the drain current vs drain voltage for different value of gate to source voltage. It seems that increasing of gate voltage will increase the drain current this is due to the increase of gate voltage will increase the inversion process which will increase in conductance, in turn, the drain current.

Figure 4.6 shows the variation of drain current with respect to variation of drain voltage for different channel length of 16nm, 20nm and 30nm. As the channel length reduces the drain current increases, this is because of quantum confinement effect. Quantization of carrier increases as channel length shrinks hence drain current increases. Moreover, scattering probability also decreases with the decrease of channel length which moves the electron transport through the channel to quasi-ballistic transport which will also increase the drain current. For a shorter length, the decrease of scattering will increase the carrier

mobility. Drain current in logarithmic scale is plotted for gate voltage for different value of drain to source voltage in figure 4.7. Comparison between a classical and quantum model for drain current is shown in figure 4.8. In the quantum model, the degree of freedom of the carrier is reduced due to quantization of the carrier which will reduce the drain current in comparison to the classical approach. Moreover in the ultra thin structure to reduce the short channel effect heavy doping is required this will quantize the carrier due to electric field induced carrier quantization. The inversion charge which is present in the interface of Si/SiO_2 in classical approach will be shifted to the middle of the substrate, and this will reduce the drain current. There is also a negative effect on the drain current because of phonon scattering and inter subband scattering which will reduce the mobility of the carrier current.

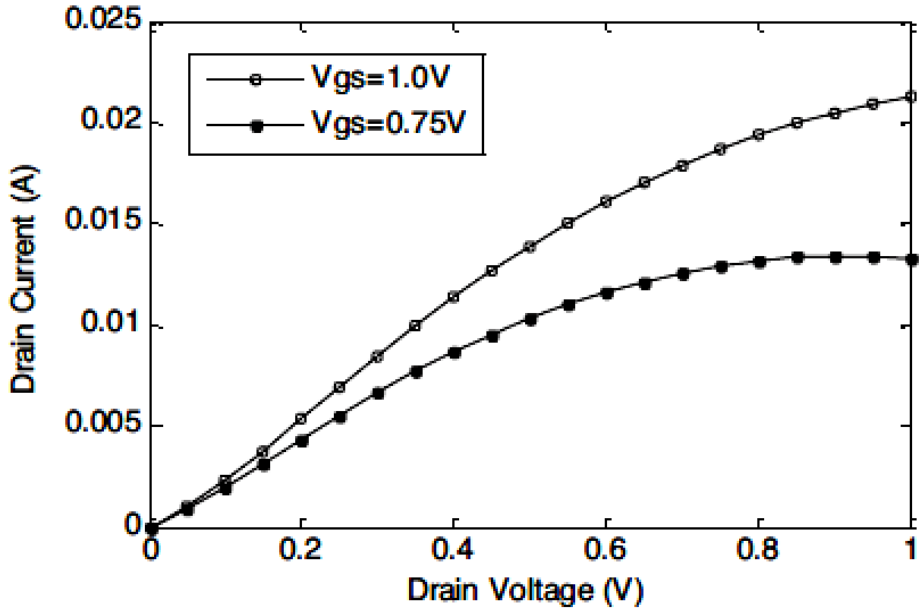

Fig. 4.3 Drain current vs drain voltage for DMDG SON MOSFET

Table 4.1: Physical Parameters for DMDG structure

Parameters	Values
Doping Concentration (N_A)	$2x10^{21}$ m^{-3}
Source/Drain Concentration($N_{S/D}$)	$5x10^{26}$ m^{-3}
Work function of p^+ Polysilicon	5.25eV
Work function of n^+ Polysilicon	4.17eV
Front gate Oxide (t_f)	1 nm
Back gate oxide ($t_{box/air}$)	1nm
Film thickness (t_{si})	5nm
Total Channel length (L)	20nm
Channel length under p^+ Polysilicon (L_1)	10nm
Channel length under n^+ Polysilicon (L_2)	10nm
Channel Width	50nm

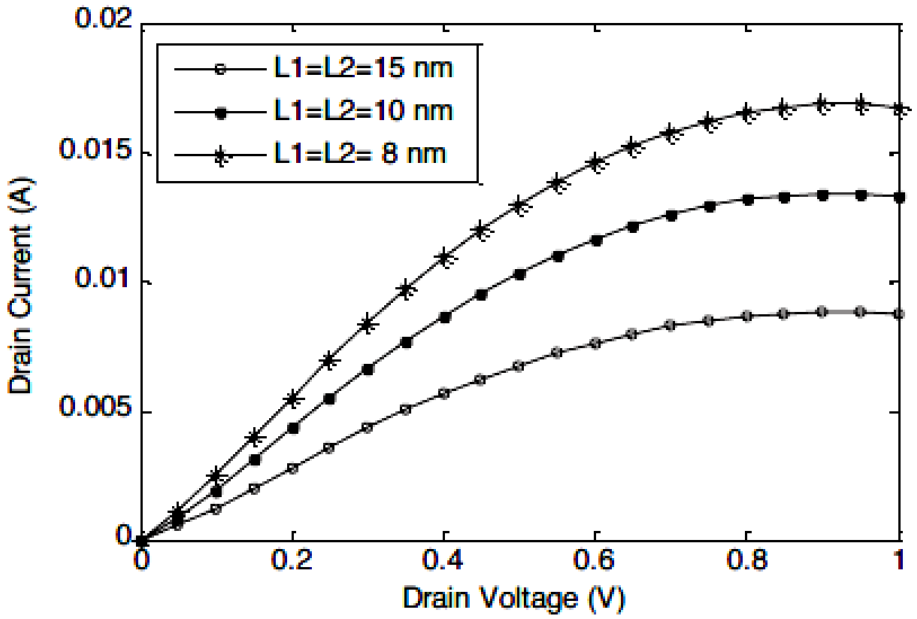

Fig. 4.4 Drain current vs drain voltage for different channel length

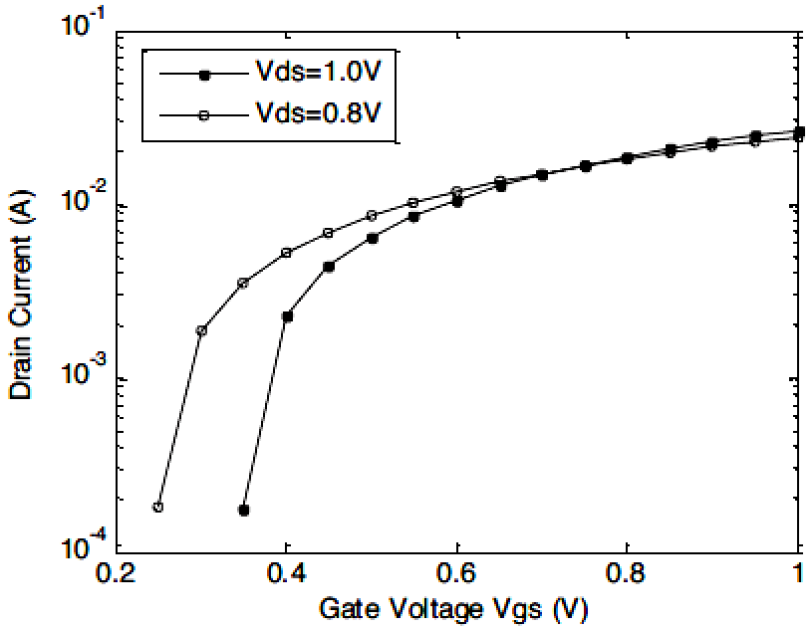

Fig. 4.5 Drain current vs gate voltage for different drain to source voltage

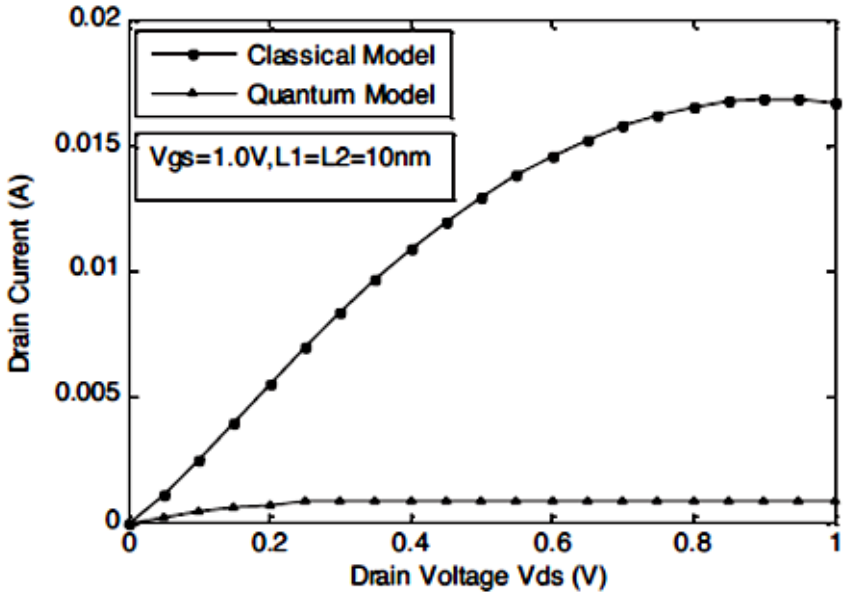

Fig: 4.6 Drain current vs drain voltage for classical and quantum model

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Chapter 5

A COMPARATIVE ANALYSIS OF NANO SON DMDG MOSFET USING HIGH-K DIELECTRIC FOR IMPROVED PERFORMANCE

5.1 Introduction.

CMOS technology has been used from early 1970 for its excellent high speed performance due to its adaptability to improve the innovative design, scalability, and better control. The aggressive downscaling of the MOS device improves the productivity and the performance of microelectronics devices. However, this also leads to many challenges such as lowering the gate control over the channel resulting in an increase of different types of short channel effect and high off current. Moreover, scaling of the channel will force to scale down the conventional oxide dielectric silicon-di-oxide (SiO_2) layer in the equal proportion which results in ultra thin SiO_2 layer. This ultra-thin SiO_2 layer when scale down to the range of 1nm will break down due to direct tunneling of current. The gate leakage current increase exponentially with a decrease of gate oxide due to quantum mechanical tunneling of the electron through the gate oxide. Moreover, the insulation provided by SiO_2 in micrometer range for boron penetration from p^+ polysilicon gate also breakdown, which further degrade the mobility of the carrier in the channel. The effect of this is

seen in degradation of the threshold voltage and drain current. So an alternative material with high permittivity is required to resist the gate leakage current, oxide breakdown, boron penetration, etc. that exist in when SiO_2 is used as a gate oxide. In this chapter, we try to give a solution to this problem by using high-k dielectric material Hafnium Oxide (HfO_2). Two different DMDG SON MOSFET structure are used to evaluate the performance of the device. The front gate oxide of both the structure are replaced with HfO_2 whose permittivity is higher than the permittivity of SiO_2 . Analytical modeling for threshold voltage and drain current for linearly graded work function variation DMDG SON MOSFET and DMDG SON MOSFET are carried out, and comparison analysis have been made with respect to the conventional SiO_2 gate oxide.

5.2 Literature Survey.

The current between the source and drain in a MOSFET will determine the performance of a modern device how fast the transistor can operate. Two voltages are controlling this parameter. First is the gate voltage and the second is the drain source voltage. The gate voltage is responsible for the inversion or accumulation of charge carrier density in the semiconductor channel. This is done by charging the gate insulator. Hence to generate more carrier, a large capacitance is required for same applied voltage. The induced charge in the channel is driven by the other voltage i.e. voltage between the source and the drain. Gate dielectric, source/drain capacitance are some of the issues, if not controlled, will increase the short channel effect, drain induced

barrier lowering, poly gate depletion, gate oxide tunneling and quantization effect in the inversion layer [5.1][5.2]. Scaling down the semiconductor device will also scale down the oxide dielectric layer by the same proportion [5.2] to maintain the control over short channel effect. So for the ultra thin device of sub 45nm the effective oxide thickness should be in the range of 1nm[5.1]. The high energy electron i.e. hot electron will tunnel through the ultra thin oxide layer and increase the charge which will ultimately cause the failure of the device [5.3]. The direct tunneling current [5.2] and reliability concern[5.5] are two parameters which will make SiO_2 as a not competent dielectric layer for modern MOSFET device. So we have to look for high permittivity material (high-K) for the dielectric layer. So in the setup of high K dielectric, a comparison of capacitance charge of the insulator for high K and SiO_2 has to be done. The area(A), permittivity (ε) of the insulator and the insulator thickness (t_{ox}) will determine the oxide capacitance C_{0X}. The oxide capacitance is directly proportional to the permittivity of the dielectric and inversely to the thickness of the dielectric layer. A term equivalent oxide thickness (EOT) [5.5] is defined as the thickness of the silicon dioxide which will generate the same capacitance as generate by high K dielectric oxide layer. The drain source current (I_{ds}) will mainly depend upon three parameters as describe by Sah[5.6], the mobility (μ), the geometry (W/L) of the channel and the induced charge density (Q_{si}). The induced charge density is directly proportional to the oxide capacitance and inversely to the area. The current drawn by a transistor can be increased if EOT is around 0.5nm. The value of EOT of around 0.5nm can be achieved by

controlling the three parameters of drain current i.e. thickness of the oxide layer (t_{ox}), permittivity (ε) and the mobility(μ), which can be obtained by scaling the device, having high-K dielectric layer, and high mobility. The performance of the conventional MOSFET can be increased by scaling the device. As the device is scaled down the threshold voltage decreases with decreasing channel length and the drain voltage increases which results in different short channel effect and DIBL effect. The double gate MOSFET(DG MOSFET) [5.7].[5.8] improve the scalability of the MOSFET. But for sub 100nm DG MOSFET it shows considerable DIBL effect and threshold voltage roll off. Moreover as the scaling increase different types of SCE, DIBL, sub-threshold conduction hot carrier effect come into presents [5.9],[5.10]. A new Fully Depleted Silicon-on-Insulator (FDSOI) MOSFET has get much attention due to its improve SCE, less junction capacitance, low propagation delay and reduced junction capacitance [5.11],[5.12] The problem of reduction of subthreshold slope and immunity to threshold voltage roll off still persist in the FDSOI device [5.13]. So the buried BOX layer of SOI device is replaced with air (relative dielectric constant of one) to reduce the parasitic capacitance value between substrate and source/drain. This will increase the speed of the device, and the device is known as Silicon-on-Nothing(SON) MOSFET. A Chaudhry et al [5.14] implemented the concept of gate engineering and proposed new structure with dual metal double gate (DMDG) MOSFET which modified the vertical field of a single gate. The DMDG MOSFET is having two gate metal of different work function. The metal near the source will have higher work function than the metal near the drain for n channel DG MOSFET.[5.16],[5.17]. The

gate transport efficiency is increased due to the sudden increase of electron velocity and electric field in the interface of the two metal gate. Moreover due to two different threshold voltage because of different work function metal gate, the increase in drain saturation voltage will not allow the drain field to enter into the channel. The structure also provide immunity to mobility degradation and will have higher transconductance [5.17]. S. Deb et al [5.18] proposed an improved linearly graded work function engineered binary metal gate electrode DMDG MOSFET structure. This structure will provide less DIBL effect, and it is more immune to SCEs due to the linearly variation of work function. With the continuous miniaturization of the device will transform the gate dielectric thickness to an ultra thin level [5.18]. The ultra thin gate dielectric cannot withstand gate applied voltage and as such leakage current will increase [5.2]. This leakage current will increase the power consumption and also create reliability problem [5.4]. The presence of trap charges in the gate oxide, and the surface will result significant amount of surface and Coulomb scattering. Due to this scattering, it will hamper the effective mobility of the carrier. To mitigate these challenges the researcher look for different type of dielectric material of high K with metal gate [5.19],[5.20]. Among the various properties, the gate dielectric should have the properties such as high permittivity, reduce leakage current, lower direct tunneling effect, high barrier height, lower the power consumption, compatible with the gate metal and stable over a silicon substrate. Good insulating properties and high capacitance are the most important properties that should be present in the good dielectric material. The off current of the

device decreases exponentially with the rise in dielectric parameter which will reduce the direct tunneling of the current. Moreover, DIBL also reduces exponentially with the rise of a dielectric constant which reduces SCE [5.20],[5.21]. Transconductance, gain, and output resistance increases if dielectric layer of SiO_2 is replaced by the high-k dielectric material. Hafnium di-Oxide (HfO_2) with a high dielectric constant of 22-25[5.22], band offset larger than 1.4eV and band gap of 5.6eV[5.23] is a potential candidate to replace SiO_2. Moreover, its thermal stability when contact with silicon is quite satisfactory with lower trap density [5.24],[5.25]. The time for breakdown also increases in case of hafnium oxide due to its ability to withstand dynamic stress for a long time in MOS device [5.26].

The present research work tries to utilize the benefit of using Hafnium dioxide dielectric layer in linearly graded DMDG SON MOSFET structure and analysis the structure in terms of change in threshold voltage and surface potential. As the device is scaled down and dielectric layer thickness reach around 1nm, the quantum confinement effect comes into present [5.27]. An analysis of charge density, electric field, and drain current has also been done considering quantum effect in hafnium oxide dielectric DMDG SON MOSFET.

5.3 Analytical modeling.

The proposed analytical modeling of the semiconductor device is divided into two parts. First analytical modeling for surface potential and threshold voltage has been done on linearly graded DMDG SON MOSFET without considering the quantum effect. Secondly, DMDG

SON MOSFET structure is used for analysis of charge density, electric field and drain current considering quantum effect. For both the case hafnium dioxide is used as a dielectric layer instead of SiO_2.

5.3.1 Linearly graded DMDG SON MOSFET

The proposed structure consist of linearly graded double gate dual metal SON MOSFET with hafnium dioxide (HfO_2) as a dielectric material in place of SiO_2 is shown in figure 5.1. Here binary alloy metal over the gate is used. The idea of continuous mole fraction variation of the binary metal gate [5.28] is used here. Two metal, Metal M1 platinum(Pt) with a work function of 5.25eV and Metal M2 titanium (Ta) with work function of 4.17eV are used. The front gate is linearly graded.

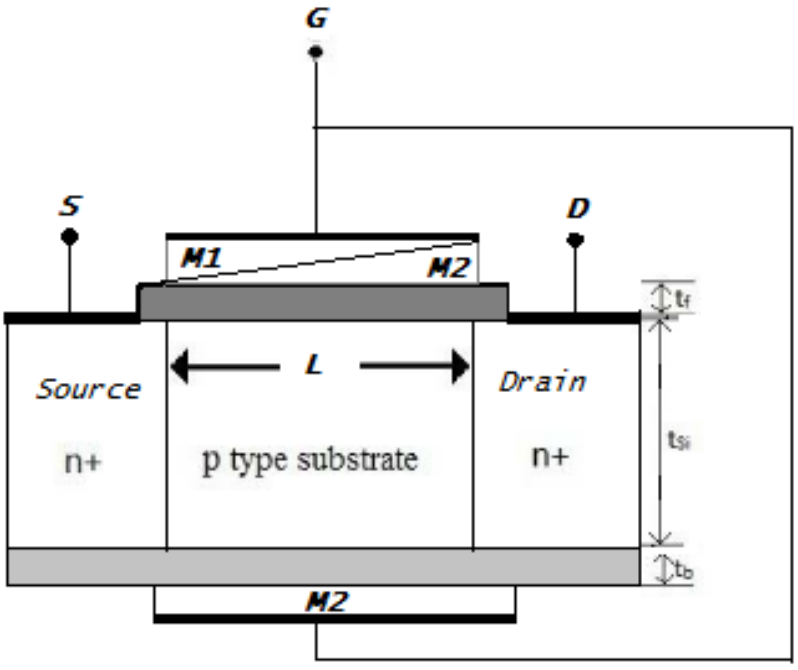

Fig. 5.1. Linearly graded DMDG SON MOSFET

The back gate comprises of metal M2. The front and back gate oxide thickness is represent by t_f and t_b respectively. The dielectric layer of front gate is of HfO_2. Since it is SON structure the back gate oxide is consist of air. t_{si} is the body thickness and L is the length of the channel.

For an arbitrary metal $A_\lambda B_{1-\lambda}$ alloy the work function can be expressed as [5.29]-[5.31]

$$\phi_m(\lambda) = \lambda\phi_2 + (1-\lambda)\phi_1 + \lambda(1-\lambda)\left[\frac{(\phi_2-\phi_1)(\rho_2-\rho_1)}{\lambda\rho_2+(1-\lambda)\rho_1}\right] \tag{5.1}$$

where

ϕ_1 = work function of metal M1

ρ_1 = Total densities of states of M1

ϕ_2 = work function of metal M2

ρ_2 = Total densities of states of M2

If total densities of states of the metal are equal, then the effective work function of the gate is given as

$$\phi_m(\lambda) = \lambda\phi_2 + (1-\lambda)\phi_1 \tag{5.2}$$

Normalizing the work function with length of the channel (L)

$$\phi_m(x) = (x/L)\phi_2 + (1-x/L)\phi_1 \tag{5.3}$$

The potential distribution of a short channel device is 2-D in nature [5.32]. Threshold voltage and potential profile expression can be obtained by solving the Poisson's equation in the channel region[5.33]. The 2D Poisson's equation for $0 \le x \le L$, $0 \le y \le t_{si}$

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{q N_d}{\varepsilon_{si}} \tag{5.4}$$

where

$\phi(x,y)$ = Potential distribution in x and y-direction,

ε_{si} =The permittivity of silicon channel and

Na =Doping concentration of channel.

the potential distribution according to Young [5.34],

$$\phi(x,y) = \phi_s(x) + C_1(x)y + C_2(x)y^2 \tag{5.5}$$

$\phi_s(x)$ = Front interface surface potential

$C_1(x)$ and $C_2(x)$ are arbitrary coefficient.

Now using the four boundary condition of [5.28], i.e.

i). Electric flux at the gate/front oxide interface is continuous.

ii) Electric flux at the interface of buried oxide and the back channel is Continuous.

iii) The potential at the source end is built in potential in the channel.

iv). The potential at the drain end is summation of built in potential and drain to source potential.

the value of $C_1(x)$ and $C_2(x)$ can be obtained as

$$C_1(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_s(x) - V_{gs}^{'}}{t_f} \tag{5.6}$$

$$C_2(x) = \frac{V_{sb}^{'}\alpha}{2} - \frac{(\alpha+\beta)\phi_s(x)}{2} - \frac{\beta\phi_m(x)}{2} + \frac{\beta(V_{gs}+\phi_{si})}{2} \tag{5.7}$$

where

$V_{gs}^{'} = V_{gs} - V_{FB}$ and

$V_{sb}^{'} = V_{gs} - V_{FBB}$

V_{gs} is the gate to source applied bias,

V_{FB}, V_{FBB} is the flat band voltage of front and back oxide.

$V_{FB} = \phi_m(x) - \phi_{si}$ and $V_{FBB} = \phi_2 - \phi_{si}$

ϕ_{si} = Work function of the silicon and is given by

$$\phi_{si} = \chi + \frac{E_g}{2q} + \phi_F \tag{5.8}$$

where

$\phi_F = \frac{KT}{q}\ln\left(\frac{Na}{ni}\right)$ is the bulk potential

E_g = Band gap of silicon

q = Electron charge

n_i = Intrinsic concentration of silicon

K = Boltzmann constant

T = Room temperature

$$\alpha = \frac{2}{t_{si}^2(1+{}^{2C_{si}}\!/_{C_b})}, \quad \beta = \frac{2({}^{C_f}\!/_{C_b} + {}^{C_f}\!/_{C_{si}})}{t_{si}^2(1+{}^{2C_{si}}\!/_{C_b})}$$

$$C_f = \frac{\varepsilon_{hfox}}{t_f}, \quad C_b = \frac{\varepsilon_{air}}{t_b} \text{ and } C_{si} = \frac{\varepsilon_{si}}{t_{si}}$$

where

ε_{hfox} = relative permittivity of hafnium dioxide

ε_{air} = relative permittivity of the air.

Putting the constant term derived above and using the boundary condition the surface potential can be defined as

$$\phi_s(x) = Ae^{\eta x} + Be^{-\eta x} + K_1 x + K_2 \tag{5.9}$$

Where, $K_1 = \frac{\beta(\phi_1 - \phi_2)}{L\eta^2}$,

$$K_2 = \frac{-qNa}{\eta^2 \varepsilon_{si}} + \frac{V_{sb}^{'}\alpha}{\eta^2} + \frac{\beta(V_{gs} + \phi_{si})}{\eta^2} - \frac{\beta\phi_1}{\eta^2},$$

$$A = V_{bi} - B - K_2$$

V_{bi}=built in potential

$$= \frac{KT}{q} \ln\left(\frac{NaNd}{n_i^2}\right).$$

Nd is the Donar concentration of source and drain region.

$$B = \frac{V_{bi}e^{\eta L} + K_2(1 - e^{\eta L}) + K_1 L - (V_{bi} + V_{ds})}{2\sinh \eta L},$$

V_{ds}=Drain to source voltage

Now when the minima of the surface potential is equal to $2\Phi_f$ that value of gate to source voltage is called the threshold voltage [5.35]. Equating

$$\frac{d\phi_s(x)}{dx} = 0$$

$$x_{\min} = \frac{A\eta + B\eta + K_1}{B\eta^2 - A\eta^2} \tag{5.10}$$

Threshold voltage can be defined as

$$V_{th} = \frac{1}{r}\left\{\begin{array}{l} 2\phi_F + \dfrac{\sinh \eta x_{\min}}{\sinh \eta L}\left[V_{bi}e^{\eta L} + K_1 L - (V_{bi} + V_{DS})\right] \\ -K_1 x_{\min} - V_{bi}e^{\eta x_{\min}} \\ -\left[(1-e^{\eta x_{\min}}) - \dfrac{\sinh \eta x_{\min}}{\sinh \eta L}\right]\left[\dfrac{-qN_a}{\varepsilon_{si}\eta^2} + \dfrac{V_{sb}'\alpha}{\eta^2} + \dfrac{\beta(\phi_{si}-\phi_1)}{\eta^2}\right] \end{array}\right\} \quad (5.11)$$

where $r = \dfrac{\beta}{\eta^2}\left[(1-e^{\eta x_{\min}}) - \dfrac{\sinh \eta x_{\min}}{\sinh \eta L}\right]$

5.3.2 DMDG SON MOSFET with Quantum Effect.

Downscaling of the device to deca-nanometer scale deviates the characteristics of the device from classical model. This is because of the quantum confinement of electron. So while doing the analysis of the device quantum effect should also be considered [5.36][5.37]. Here we are using the same device structure as used in chapter 4 to analysis the drain current behavior of the device. The drain current, charge density, and electric field are analysed using HfO_2 as a high-k dielectric layer. The proposed DMDG SON MOSFET device structure is shown in figure 5.2. It consists of two gate metal in the front gate. The gate metal M_1 (p^+ polysilicon) is having a work function of 5.25eV and gate metal M_2 (n^+ polysilicon) is having a work function of 4.17eV with the length of L_1 and L_2 respectively. The back gate consists of the same material M_2 of the work function of 4.17eV. The front gate oxide, silicon substrate and back gate oxide thickness are represented by t_f, t_{si} and t_b respectively. The front gate oxide material is of HfO_2. For an ultra thin short channel structure carrier quantization appears and the potential and carrier distribution is 2D in nature.

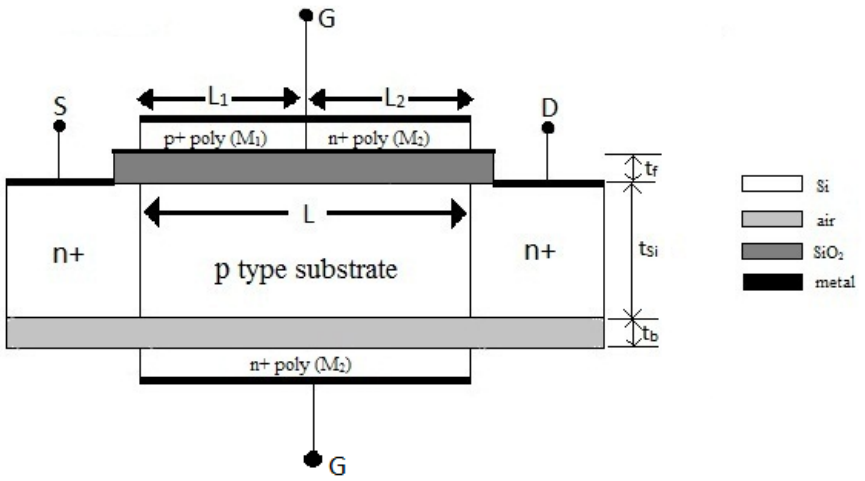

Fig. 5.2 DMDG SON structure

To find the potential profile of such structure Poisson and Schrodinger equation should be solved self-consistently [5.38],[5.39].

The 2D poisons equation for the structure is

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}} \tag{5.12}$$

where

$\phi(x,y)$ = 2D potential profile of the silicon channel.

N_a = Doping concentration of p type channel.

ε_{si} = Permittivity of silicon.

2D potential profile can be expressed as [5.34]

$$\phi(x,y)=\phi_s(x)+C_1(x)y+C_2(x)y^2 \tag{5.13}$$

$\phi_s(x)$ is the surface potential. $C_1$and C_2 are arbitrary constant.

The front gate of the proposed structure consists of two metal of different work function. So from chapter 4 equation no (4.7) and (4.8) the potential profile under the two region can be expressed as

$$\phi_1(x,y) = \phi_{s1}(x) + C_{11}(x)y + C_{12}(x)y^2, \quad for\, 0 \le x \le L_1, 0 \le y \le t_{si} \tag{5.14}$$

$$\phi_2(x,y) = \phi_{s2}(x) + C_{21}(x)y + C_{22}(x)y^2, \quad for\, L_1 \le x \le L, 0 \le y \le t_{si} \tag{5.15}$$

From chapter 4 using the boundary condition equation from (4.9) to (4.19) the surface potential can be expressed as

$$\phi_{S1}(x) = Ae^{\eta x} + Be^{-\eta x} - \frac{\beta_1}{\alpha} \tag{5.16}$$

$$\phi_{S2}(x) = Ce^{\eta(x-L_1)} + De^{-\eta(x-L_1)} - \frac{\beta_2}{\alpha} \tag{5.17}$$

The constant A, B, C, D, α, β_1 and β_2 have the same value as in chapter4. Differentiating the surface potential we can obtained the electric field of the proposed structure. Moreover the capacitance C_{OX} and relative permittivity ε_{OX} shown in the equation (4.16) to (4.19) are due to high-k dielectric layer hafnium oxide.

The total inversion charge across the channel is calculated by solving the Schrodinger equation for rectangular and triangular well separately. So from [5.40] -[5.42] and chapter 4 equation (4.1) to (4.4), the inversion charge for the two regions is given as

For the region $0 \le x \le L_1$

$$Q_{il}(x)=\frac{qkT}{\pi\hbar^2}\sum_i\left[\begin{array}{l} m_l^* g_l \ln\left[1+\exp\left(-\beta\left(\tilde{E}_{rec,l}^{\,i}+\frac{E_g}{2}-\phi_{S1}(x)+V_{F1}(x)\right)\right)\right] \\ +\sqrt{m_l^* m_t^*}\, g_t \ln\left[1+\exp\left(-\beta\left(\tilde{E}_{rec,t}^{\,i}+\frac{E_g}{2}-\phi_{S1}(x)+V_{F1}(x)\right)\right)\right]\end{array}\right] \quad (5.18)$$

For the region $L_1 \le x \le L_2$

$$Q_{i2}(x)=\frac{qkT}{\pi\hbar^2}\sum_i\left[\begin{array}{l} m_l^* g_l \ln\left[1+\exp\left(-\beta\left(\tilde{E}_{trian,l}^{\,i}+\frac{E_g}{2}-\phi_{S2}(x)+V_{F2}(x)\right)\right)\right] \\ +\sqrt{m_l^* m_t^*}\, g_t \ln\left[1+\exp\left(-\beta\left(\tilde{E}_{trian,t}^{\,i}+\frac{E_g}{2}-\phi_{S2}(x)+V_{F2}(x)\right)\right)\right]\end{array}\right] \quad (5.19)$$

The total drain current considering channel length modulation is given as

$$I=\frac{W}{L}\left[\int_0^{L_1} J_{n1}(x)dx+\int_{L_1}^{L} J_{n2}(x)dx\right] \quad (5.20)$$

where

$J_{n1}(x)$ and $J_{n2}(x)$ are the current density for the regions $0 \le x \le L_1$ and $0 \le x \le L_2$ respectively. The current equation is obtained as shown in equation (4.36) of Chapter 4

$$I_d = -\mu \times \frac{W}{L} \times \frac{qKT}{\pi\hbar^2} \times \left[\begin{array}{l} m_l^* \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} \end{array} \right) \times V_{F1}(x) + \frac{V_{F1}^2}{2} \right\} + \\ \sqrt{m_l^* m_t^*} \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s1,\min} \end{array} \right) \times V_{F1}(x) + \frac{V_{F1}^2}{2} \right\} \\ + m_l^* \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s2,\min} \end{array} \right) \times (V_D - V_{F1}) + \frac{V_D^2 - V_{F1}^2}{2} \right\} + \\ \sqrt{m_l^* m_t^*} \times g_l \times \left\{ \beta \left(\begin{array}{l} E_{l,rec}^i \\ +\frac{E_g}{2} - \phi_{s2,\min} \end{array} \right) \times (V_D - V_{F1}) + \frac{V_D^2 - V_{F1}^2}{2} \right\} \end{array} \right] \quad (5.21)$$

the symbolic notation has same meaning as in chapter 4.

5.4 Result and Discussion

The work tries to analysis the benefit of using high-k hafnium dioxide material as a front gate dielectric oxide for DMDG SON MOSFET structure. The work is divided into two parts. Firstly we considered linearly graded mole function variation DMDGSON MOSFET structure, which is quite immune to short channel effect [5.28]. But when the device structure is reduced to ultra thin level the conventional SiO_2 layer cannot act as a proper dielectric layer. So to overcome the drawback of SiO_2 it is replace by high-k dielectric material HfO_2. Surface potential and threshold voltage parameters are analysis for the device considering high-k dielectric layer. Secondly, we

try to incorporate quantum confinement effect in a DMDG SON MOSFET structure while analyzing the electric field, charge density and drain current due to high-k dielectric material on the device. For both the case, the simulation is done with Atlas 2D simulator. The parameters used for simulation of figure 5.1 (linearly graded DMDG SON MOSFET) and figure 5.2 (DMDG SON MOSFET) is shown in table 5.1 and table 5.2 respectively.

Table 5.1 Physical parameter for linearly graded DMDG SON MOSFET

Parameters	Values
Doping Concentration (N_A)	$2x10^{21}$ m^{-3}
Source/Drain Concentration($N_{S/D}$)	$5x10^{25}$ m^{-3}
Work function of metal M_1, Pt	5.25eV
Work function of metal M_2, Ta	4..17eV
Front gate Oxide (t_f)	2 nm
Back gate oxide t_b	2nm
Film thickness (t_{si})	10nm
Total Channel length (L)	20nm
Permittivity (SiO_2)	3.9
Permittivity (HfO_2)	25
Channel Width	50nm

Table 5.2 DMDG SON MOSFET parameters

Parameters	Values
Doping Concentration (N_A)	$2x10^{21}$ m^{-3}
Source/Drain Concentration($N_{S/D}$)	$5x10^{26}$ m^{-3}
Work function of p^+ Polysilicon	5.25eV
Work function of n^+ Polysilicon	4.17eV
Front gate Oxide (t_f)	1 nm
Back gate oxide ($t_{box/air}$)	1nm
Film thickness (t_{si})	5nm
Total Channel length (L)	20nm
Channel length under p^+ Polysilicon (L_1)	10nm
Channel length under n^+ Polysilicon (L_2)	10nm
Channel Width	50nm
Permittivity (SiO_2)	3.9
Permittivity(HfO_2)	25

The physical thickness of the gate oxide is given as

$$t_{ox}^{physical} = \frac{k_{high-k}}{k_{ox}} t_{ox} \tag{5.22}$$

where k_{high-k} and k_{OX} represent the permittivity of high-k and SiO_2 respectively. t_{Ox} is the equivalent oxide thickness. It seems that the physical thickness of the gate oxide is approximately increased by four times if we use hafnium dioxide in place of SiO_2. The increase in the physical thickness will reduce the barrier height between channel and source which will increase the termination of the electric field in the drain and source region. Moreover, the increase in the effective gate oxide thickness will avoid the breakdown of the gate oxide which in turn

reduce gate oxide leakage current. So the gate will have more control of the carrier in the channel and the threshold voltage of the device reduced. Again the increase of gate oxide capacitance with high permittivity material will act as a catalyst to reduce the threshold voltage. This reduction of the threshold voltage is reflected in figure 5.3. The reduction of threshold voltage will rise the minima in the potential surface graph which is evident for both analytical as well as ATLAS 2D simulated data as shown in figure 5.4 for using HfO_2 in place of SiO_2 as dielectric oxide. Figure 5.5 shows a variation of surface potential for different values oxide thickness. Figure 5.3 to figure 5.5 are graph obtained for the figure 5.1

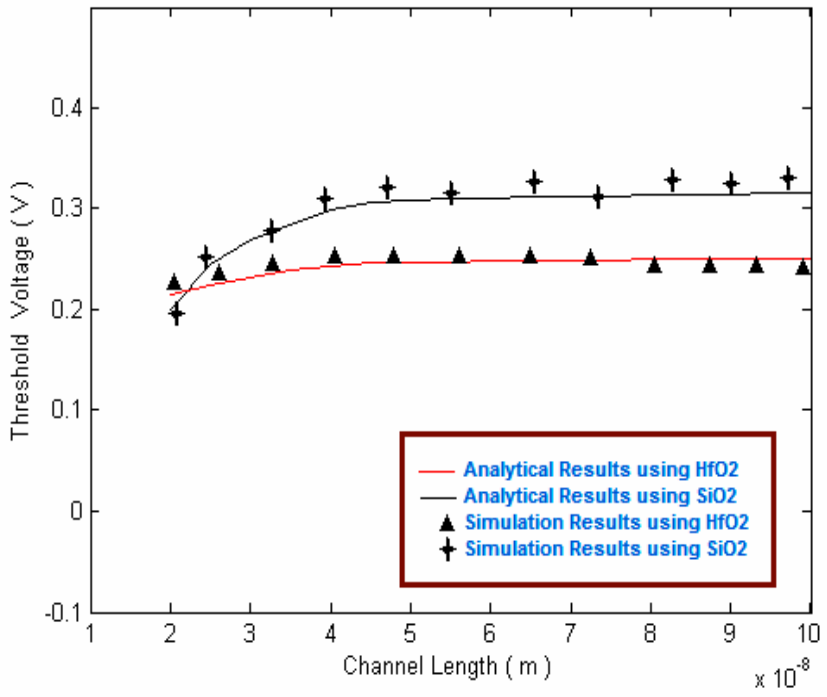

Fig. 5.3. Variation of threshold voltage with channel length (V_{gs}=0.2 V and V_{ds}=0.4 V).

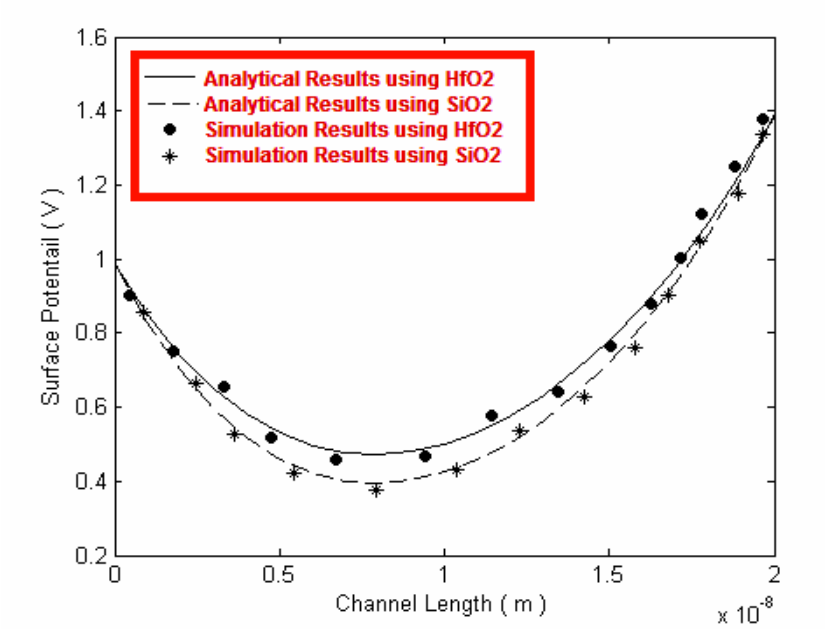

Fig. 5.4. Variation of surface potential with channel length

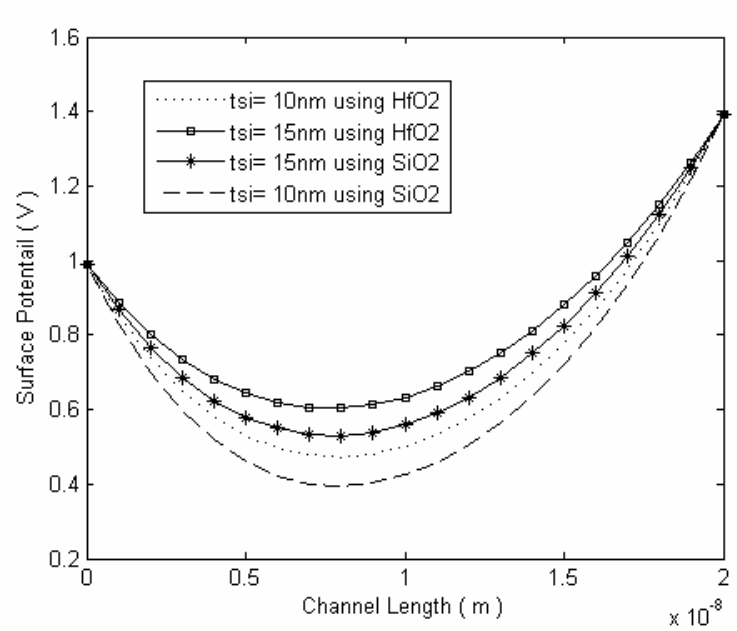

Fig. 5.5. Variation of surface potential with channel length for t_{si}=10nm and t_{si}=15nm

The charge density of the MOSFET is directly proportional to the relative permittivity, in turn to the permittivity of the oxide dielectric. This is shown in figure 5.6. Where the charge density for HfO_2 dielectric is above the SiO_2 as the permittivity of HfO_2 is more than the SiO_2. The figure 5.7. explain the relation between electric field and normalized channel position. As the effective physical oxide thickness increases with increase in the permittivity, the gate leakage current which exists due to the positive gate voltage in SiO_2 dielectric reduces when HfO_2 is used as gate oxide dielectric. The reduction of leakage current will reduce the hot carrier effect. There is a steep rise in electric field in the middle point of the channel, that is the point where the two metal gate with two different work function interface. At this point the conduction band energy changes abruptly which cause a step in the potential profile [5.41]. As the oxide capacitance is inversely proportional to drain source resistance. The drain current increase when HfO_2 is used as an

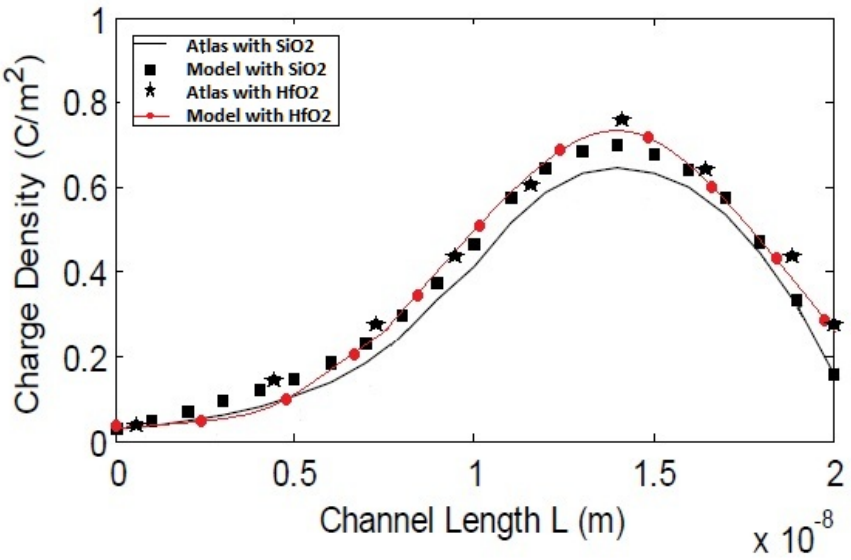

Fig.5.6 Charge density vs channel length

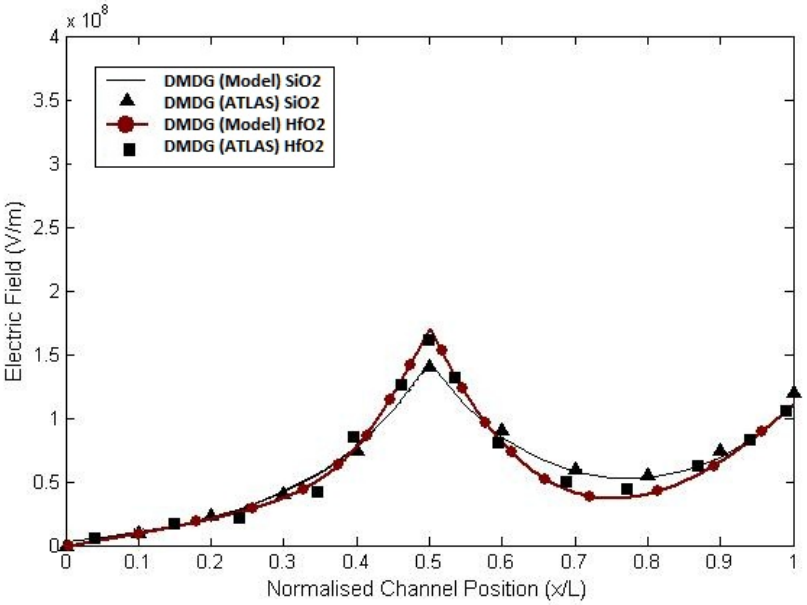

Fig 5.7 Electric Field vs normalized channel position

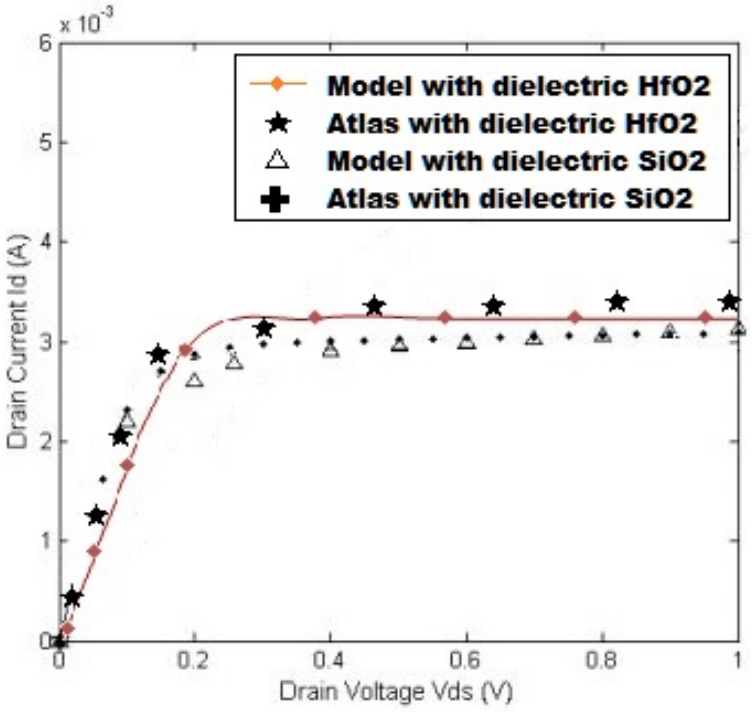

Fig 5.8. Drain Current vs Drain Voltage

dielectric oxide in place of SiO_2. The reduction of boron penetration through the oxide layer will reduce the scattering effect. So mobility of the charge carrier increase. This will also enhance the drain current. Figure 5.8 resembles it. ATLAS-2D simulator is used to verifies the analytical model results. Here we have used ATLAS -2-D mobility models concentration dependent mobility mode, FLDMOB for simulation of the device. Figure 5.6 to figure 5.8 are obtained for the DMDG SON MOSFET structure shown in figure 5.2.

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Chapter 6

DESIGN AND IMPLEMENTATION OF AN ASYNCHRONOUS ARBITER CIRCUIT : AN APPLICATION USING IMPROVED HYBRID SET SOI MOSFET

6.1 Introduction.

Rapid progress of semiconductor device has force and motivate the researchers for new innovative device to satisfy the international technology road map for semiconductor device [6.1] In a ultra thin device below sub 100 nm range a MOSFET device face a series of problem such as quantum effect in the inversion layer, short channel effect, gate leakage, source and drain resistance etc.[6.2]-[6.6]. Silicon-on-Insulator (SOI), Silicon-on-Nothing (SON), high-k dielectric, Dual Metal Double Gate (DMDG) are some of the unconventional technique develop to utilize the enchanting performance of MOSFET in low dimension level. But it cannot further miniaturize the device below 10nm. An alternative approach should be endorsed in order to continue with the alluring properties of CMOS device. Single electron transistor (SET) which control the flow of the carrier in single electron level is one of the candidate to replace CMOS device due to its nano feature size [6.7],[6.8]. The power dissipation of SET is approximately four to five times lower than advanced CMOS [6.8]-[6.10]. Moreover the fabrication of SET is CMOS compatible [6.11]. Although after having lots of advantages in SET, it is deprive of having some important advantages

of MOS like voltage gain, back ground charge and high temperature operation. It is unlikely that CMOS can be completely replace. Merits and demerits of SET and MOS reflected that CMOS and SET are self complementary to each other. So in near feature CMOS has to sacrifice or share its domination over semiconductor technology with SET to maintains its superiority [6.12] . Here comes the concept of hybrid SET-MOS circuit which utilize the new principles of coulomb blockade and low power consumption of SET and high speed and high drive current of MOS. Now if conventional MOS in SET-MOS circuit is replaced by SOI MOS device, than the benefit of SOI device such as low short channel effect can be incorporate in the MOS circuit of hybrid SET-MOS circuit. This provide the flexibility of reducing the supply voltage further due to the low threshold voltage of the MOS circuit. The work in this chapter is related to exploring benefit of SET-SOIMOS circuit from application view point. We have used a SET-SOI MOS hybrid circuit to show its advantage from the conventional CMOS circuit. MIB model of SET [6.13] and BSIM SOI model of MOS are used and the circuit is simulated in Tanner EDA environment..

6.2 Research Background

The introduction of MOSFET by Dennard [6.14] has made a revolutionized changes in the semiconductor industry. The dominance of MOSFET is maintain in the industry by scaling down the device drastically. this reduction of MOSFET size deep into nano scale region has introduce different types of challenges such as in terms of SCE, DIBL, subthreshold conduction, hot carrier effect and junction lekage

[6.15][6.16]. These forces researchers to approach in some non conventional innovative method geometry MOS structure. Fully Depleted Silicon On Insulator (FDSOI) MOS device is one of the product which have superior electrical characteristics such as reduced coupling effect, lower propagation delay, reduced junction capacitance, suppressed SCE, high, improved subthreshold characteristics and radiation tolerance over bulk CMOS technology [6.17],[6.18]. Further scaling down of the device below sub 20nm range leads to loss of gate control over the channel [6.19],[6.20] due to short channel effect, which will increase different type of leakage current. To overcome such problem we have to look beyond CMOS. SET is one such promising candidate. The detail review of which is discuss in chapter 2. The basic concept of SET is where a conductive island is sandwiched between two tunnel junction. The tunnel junction resistance should be greater than the quantum resistance [6.21]-[6.23] and single electron charging energy should be greater than the thermal energy [6.20],[6.24] are the two basics requirement of SET. The SET is having lots of advantages, such as nano feature size, low power dissipation, CMOS compatible fabrication process [6.7]-[6.11]. But it is deprive of some of the feature of MOS device such as high voltage gain and current drive, low output impedance, high speed. Here come the idea of hybrid SET MOS device [6.25],[6.26], so that it can utilize the advantage of both SET and MOS technology. Different types of logic circuit are realize using hybrid approach. Phase locked loop[6.27] and voltage control oscillator [6.28] are some of the hybrid circuits which shows the advantage of hybridization of SET and MOS circuit. Hybrid nano reconfigurable logic

cells [6.29]. was first implemented by B. Sui et al in 2010. Real life application of the device can be justified if the device is fabricated. The first hybrid SET MOS circuit is fabricated by A. A. Prager et al in 2011 [6.30]. Hybrid SET-MOS approach is extended to multi gate or multiple tunnel junction and memory cell, which is design and implemented by G. Deng et al.[6.31] and W.Wei et al [6.32] respectively. Research work on hybrid SET-MOS circuit from fabrication aspect is discussed by R. Parekh et al [6.33]. Exploration in the field of differential design style of hybrid circuit is also going on as proposed by M. M. Abutaleb[6.34]. In our proposed work we have design a hybrid SET-MOS arbiter circuit. The concept of SOI MOS circuit is used in the hybrid SET-MOS approach so that the advantage of SOI can be utilize in hybrid approach.

6.3 Design of hybrid SET SOI MOSFET Arbiter circuit

A multiprocessor digital system sharing global resources requires a digital system or circuit that will help in sharing the resources to the individual processor. Arbiter is the device which will help in sharing the resources to the processor one at a time [6.35]. Here in this chapter we are trying to design and implement two input arbiter circuit which will give control of the resource as a master to any one of the processor out of the two processor connected to the system. This two input arbiter can be extended to any input arbiter circuit according to the requirement.

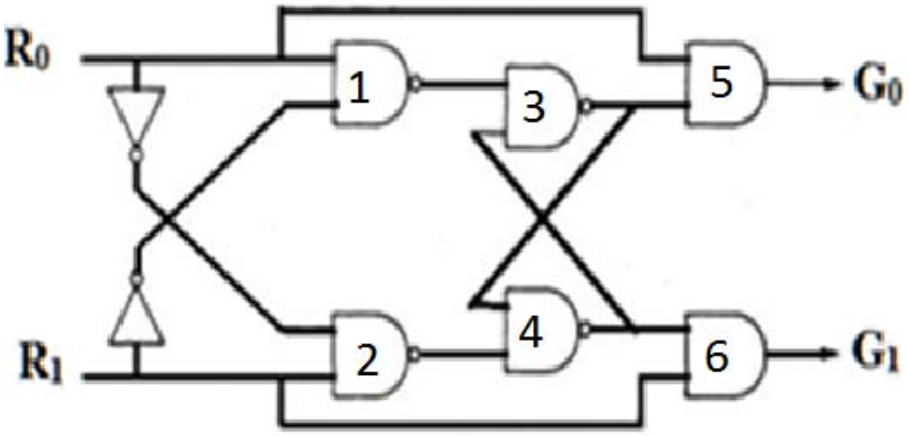

Fig. 6.1 Conventional Digital circuit for two bit arbiter

The circuit is implemented with the help of hybrid SET MOS design concept. The MOS device circuit used here is of SOI MOSFET. The conventional digital circuit for a two bit arbiter is shown in the figure 6.1. The arbiter circuit will generate the grant signal either G_0 or G_1 for the processor 1 or processor 2 based on the request signal generated from R_0 and R_1 of processor 1 or 2 respectively. The arbiter is generating the request grant signal G_0 or G_1 for processor connected to R_0 and R_1 of processor 1 and 2 respectively based on first come first serve basis. The truth table for the operation of the circuit is shown in the table 6.1. The previous record granted of the arbiter are stored in the set reset flip-flop consist by four NAND gate 1 to 4. The request line R_0 and R_1 are crosscouple to the flipflop circuit, so that a request line cannot change the state of the flip flop when the previous request line from the other processor is already high. The request line will be acknowledge when the previous request is deactivated i.e. the request

line go low. If a continous overlapping request are made then the request will be granted alternatively.

Table 6.1 Two input arbiter truth table

INPUT		**OUTPUT**	
R_0	**R_1**	**G_0**	**G_1**
0	**0**	**No Request**	
0	**1**	**0**	**1**
1	**0**	**1**	**0**
1	**1**	**Request granted on alternate basis**	

The implementation of logic gate using hybrid SET-MOS concept in CMOS design style is discussed by A. Jana et al. [6.36]. In this any one of the pull up network or pull down network of CMOS is replaced by SET and other by MOS or vise versa. The connection of the back gate (second gate) determine whether we are having pSET (p-type device) or nSET(n-type device). The connection of back gate to ground will make it pSET and if it is connected to supply (normally VDD) it will be nSET. In our design the pull up network is implemented with pmos and pull down network by nSET to get the hybrid SET-MOS circuit. The design circuit for two input arbiter is shown in the figure 6.2. The signal from the R_0 and R_1 are inverted by the two inverter as shown in the figure 6.2. These signals are cross coupled to the four SET-MOS NAND gate. This four SET-MOS inverter will act as an SR latch. The AND operation of the latch output and the input is implemented by hybrid SET-MOS NAND and a inverter circuit to get the final output G_0 and G_1.

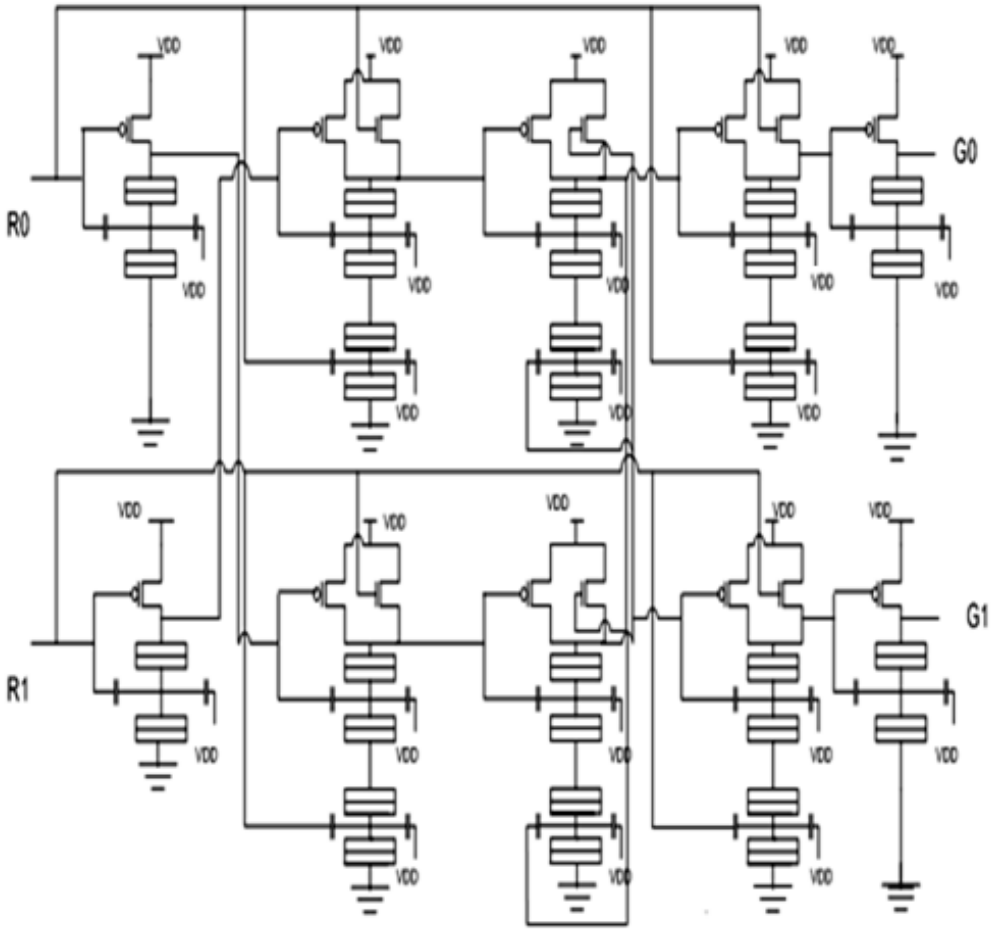

Fig. 6.2 SET MOS hybrid model for two bit arbiter

6.4 Result and Discussion

Spice macro modeling, Master equation approach and Monte Carlo approach [6.37] are the three approach by which a single electronics can be simulated. The Monte Carlo approach is based on stochastic integration [6.38] is a probabilistic approach. For a larger number of nodes, Monte Carlo approach will take long time due to stochastic sampling. In Master equation method the tunnel events are

represent by a set of transport equation and these equation are solved to calculate the probability of occupancy of different island [6.37]. Finding the relevant island is a tedious job. In Macro model approach stress is given in Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) equation instead of finding the probability of tunnelling event [6.39]. The common circuits components such as current, voltage, resistors and diode are used to design the equivalent circuit of the device. So the computation time for the macro model is less in compared to the other two model. Moreover it is the simplest model. The design of two bit arbiter is simulated in spice simulation environment where BSIMSOI MOSFET model is used. The verilog-A interface is used to incorporate the SET model. The SET circuit is designed based on MIB model [6.13]. Tanner spice environment is used to simulate the circuit. The various parameter used for the parametric analysis are shown in the table 6.2. The tunnel junction resistance are considered as 1M Ω [6.40] to satisfy the accuracy of orthodox theory. The capacitance values are kept as small as possible to make the circuit operationable for a wide range of temperature [6.40]. 0.8V is taken as supply voltage which also represent logic 1 and logic 0 represent 0V.

Figure 6.3 shows the simulated output of the arbiter circuit which resembles with the truth table shown in the table 6.1. In case of single electron device the current and voltage level increases when device is scaled down this is contrast to the MOS device [6.41]. The threshold voltage of hybrid SET-MOS circuit is lower than when PMOS and NMOS are used in CMOS. This is because of use of SET. The SET control the flow of charge in single electron level. So less voltage will

be required to control the flow of electron. Moreover use of SOI will also reduce the threshold voltage. The lower threshold voltage will reduce the requirement of current and supply voltage and in turn consume less power. The average power consumption for the arbiter circuit is 0.67µW for 0.8V power supply. Time delay another parameter which will give the operation speed of the circuit. It is the difference between the initial and 50% of the final value. Delay for MOS device depends upon the parasitic capacitance and load capacitance but for SET device it depends upon tunnel rate of the respective junction which in turn also depend upon source and drain capacitance. So switching speed of MOS device is high than SET circuit. Due to the use of SET in hybrid circuit the switching speed of hybrid circuit is less than CMOS circuit. But the overall performance parameter i.e. power delay product of hybrid SET-MOS arbiter circuit is less than CMOS arbiter circuit which is shown in the table 6.3.

Table 6.2 Parameter used for two bit arbiter circuit

Device	Parameters	Value
PMOS	W(nm)	65
	L(nm)	100
	Vth (v)	0.22
SET	$C_{TS,}$, C_{TD}(F)	$1.0X10^{-19}$
	R_{TS},R_{TD} (Ω)	$1.0X10^{6}$
	C_{G1}(F)	$2.75X10^{-19}$
	C_{G2}(F)	$1.3X10^{-19}$

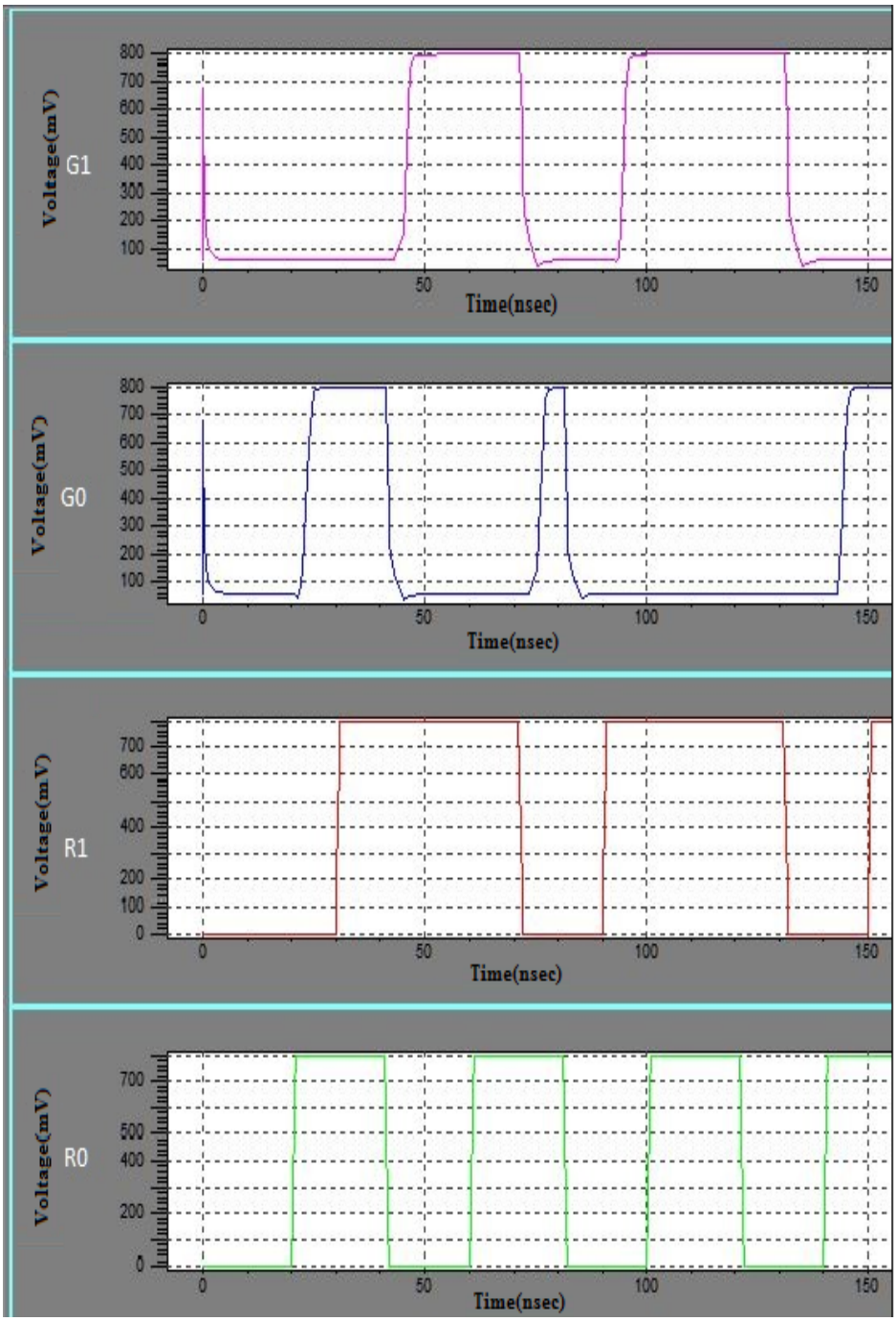

Fig. 6.3 Two bit arbiter simulation results

Table 6.3 Performance Analysis of two bit arbiter

	Average Power(μW)	**Delay (nS)**	**Power delay Product**
SET-MOS	$0.67X10^{-6}$	$2.35 X 10^{-9}$	$1.57X10^{-15}$
CMOS	$2.18X10^{-6}$	$1.57X10^{-9}$	$3.42X10^{-15}$

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Chapter 7

CONCLUDING REMARKS AND FUTURE SCOPE.

7.1 Concluding Remarks.

This thesis embodied the theoretical studies of the characteristics of low dimensional semiconductor structures and some of its application. The theoretically computed results are compared with simulated data wherever possible. The observation of the work is summarized in this chapter.

Miniaturization of the device deep below 100nm regime creates different short channel effects. The Short channel effects in terms of threshold voltage roll-off, subthreshold slope, DIBL, Hot Carrier Effects(HCEs) etc. present in bulk CMOS, single and double gate SOI MOSFET can be somewhat subjugate by the concept of work function engineering gate electrode of MOSFET as explored by earlier researchers. The ultra thin nature of the source/drain results larger series resistance. The larger series resistance will significantly reduce the current driving capability of the device and in turn, will have high threshold voltage and DIBL effect. In chapter 3 a new model for SOI/SON device has been proposed to give a better performance for future nanodevice. The proposed WFEG Re S/D SOI and SON MOSFET structure performance depiction has been made based on analytical modeling. The simulated data are obtained by simulating the

device in 2D MEDICI TCAD simulator. The concept of recessed source/drain in the buried layer and linearly graded work function in binary metal gate alloy SOI/SON MOSFET are used. Due to the presence of recessed source/drain along with work function engineered gate structure it has been observed that the threshold voltage and total series resistance are reduced as evident vide figure 3.7. Along with reduced threshold voltage, the device also maintains its symmetry along the channel as shown in figure 3.2. The reduction of the electric field vide figure 3.5 will also reduce the hot carrier effect. Hence incorporating the advantage of Recess S/D regions of 30nm deeper inside the buried layer and continuous mole fraction variation on the gate electrode, can provide better device performances in terms of threshold voltage (vide figure 3.7) surface electric field (vide figure 3.5), DIBL(vide figure 3.11) in deep nanometer regime. Analysis of SOI and SON MOSFETs device structure are carried out, and its performance are mannered in terms of front and back surface potential distribution, threshold voltage behavior and Electric field profile. This contrastive perusal provides WFG ReS/D SOI/SON MOSFET with higher immunity against SCEs and thereby providing its further scope of device miniaturization.

The use of work function engineered gate recessed source/drain SON MOSFET structure improves the performance of the device. But further scaling of the device will results quantization of the carrier. So the effect of quantization of the carriers in performance analysis become an important aspect of analytical modeling. In chapter 4 carries out the drain current analytical modeling of DMDG SON MOSFET incorporating quantum mechanical effect. Minimum surface

potential will achieve the maximum inversion charge in the channel concept is used to derive the drain current expression. Although SCE tries to warp the potential, but it will have little effect on the quantization[4.33]. The drain current of the device increase if the device length is reduced vide figure 4.4 which support further scaling of the device. The observation of lower drain current in quantum approach than the classical approach (vid fig 4.6) due to quantization of carrier reflected the actual value of drain current. This will help in future modeling of DMDG SON structure to reduce the different types of scattering in the device. So that drain current can be increased. Zhou[4.40] shows that dual metal gate can be fabricated. So if the present analysis is implemented in nanodevice of 20nm regime, it will provide a more accurate current voltage characteristics of future DMDG structure.

The conventional SiO_2 cannot withstand the influence of gate voltage, and it starts break drown when the thickness of dielectric gate oxide layer is reduced to less than 2nm. This will raise the gate leakage current and reliability issues. Chapter 5 analyzed the performance of DMDG SON MOSFETs considering high-k HfO_2 as a gate dielectric in place of SiO_2. The use of HfO_2 will reduce the threshold voltage and threshold voltage roll off of the device vide figure 5.3. This allows us for further scaling of the device. Miniaturization of the device to ultrathin level will have carrier quantization. Quantization of the carrier will reduce the drain current. The drain current of the device can be increased if HfO_2 is used as oxide dielectric which is evident from figure 5.8. The increase of the effective physical thickness of gate dielectric due to the use of high-k HfO_2 dielectric layer will reduce the oxide

breakdown and hence reduce the gate oxide tunneling current which will in turn reduce the leakage current. So the gate will have more control over the channel and drain current will increase. Further incorporating the feature of gate engineering will enhance the performance of the device. ATLAS-2D simulator verifies the analytical model results. The reduction of the threshold voltage and improve in drain current gives the flexibility of using lower supply voltage due to low power consumption. The analysis shows that if HfO_2 is used as gate oxide, then we can have a more power efficient and compact nanodevice.

Chapter 6 discusses the application of nanostructure MOS device in hybrid SET-MOS circuit for an arbiter circuit. According to Moore law in near future, the size of the device will come down to less than 10nm. Due to ultra thin device feature, MOS device will face a lots of issue due to a different type of short channel effects. So we have to look for a device beyond CMOS. Single electron transistor is one such technology which can sustain below 10nm. But the superior feature of the MOS device are also a significant assets to the semiconductor industry. So a hybridization of SET and MOS will be a boost to the industry. So in chapter 6 we try to design and implement a hybrid SET-MOS arbiter circuit and compare its performance with the existing CMOS circuit. The MOS device used here is a SOI MOS device based on BSIMSOI 4.4 model. SET is designed based on MIB model. The functionality of the circuit is verified with simulated results vide figure6.3 using Tanner SPICE. The hybridization of SET and SOIMOS device will give better performance in comparison to CMOS circuit vide Table 6.3. The power delay product of hybrid circuit obtained here is

approximately two times less than CMOS circuit. Moreover, the use of innovative SOI device will provide a new way of research to incorporate the present development in SOI and SON device in application to a hybrid circuit which helps to further scaling down of semiconductor device in the future application. So we can suggest that if innovative SOI MOS-SET device are used in place of CMOS circuit, the performance of a system can be improved.

The above study gives a considerable impact in future nanodevice research, and such study will open numerous new areas of research in low dimensional electronic device applications

7.2 Future Scope.

Our research has delineated some significant improvement, but always there is some room for improvement and challenges for future low dimensional nanodevice modeling and application. Following future aspects can be proposed for further progress:

- Quantum confinement effects can be incorporated in the material engineered gate recessed ultra thin body source/drain SON MOSFET model for better performance analysis.
- The drain current expressions in the quantum model for DMDG structure have been derived using 2D Poisson equation and 1D Schrödinger equation. The overall potential charge determined more accurately if 3D Poisson equation and 2D Schrödinger equation are solved self-consistently.

- The application of hybrid SET-SOIMOS can be extended in exploring analog circuit also to prove it superiority over CMOS technology.