Ref. No.: Ex/Prod/ET/T/125/2019(Old)

**B.E. PRODUCTION ENGINEERING**
**FIRST YEAR SECOND SEMESTER (Old) EXAM 2019**

Subject: **Basic Electronics Engineering**

**Time : Three hours** **Full Marks: 100**

*All parts of the same question must be answered at one place only*

I. Answer any **two(2)** from Q. 1 **(a), (b) and (c)** in this block:

**1. (a)** i Cut-in voltage of silicon and germanium PN junction diode is____ and ____.
ii. In P type semiconductors, the majority carriers are ____ and, in N type semiconductors, the majority carriers are _____.
iv. Differentiate semiconductor, conductor and insulator.
v. Define hole and electron in a semiconductor.

[4+3+3]

**(b)** i. An ideal diode offers _____ resistance when forward biased, and _____ resistance when it is reverse biased.
ii. Draw and explain the VI characteristics of a PN junction diode.
iii. What is an intrinsic semiconductor?
iv. What are the majority carrier and minority carrier of p type and n type semiconductor.

[2+4+2+2]

**(c)** i. What is doping? Why it is needed?
ii. Name the elements which are used as N-type impurities and P-type impurities.
iii. Explain the operation of a PN junction diode under no bias condition.
iv. What is meant by the term "Barrier potential"? What is it value for Germanium diode? [3+2+3+2]

II. Answer any **three(3)** from **2 (a), (b), (c) and (d)** in this block:

**2. (a)** i. Draw the circuit diagram of centre tap half-wave rectifier and explain its operation.
ii. Discuss the working of full-wave rectifier circuit and give the output voltage waveform.
iii. Define breakdown voltage. [4+4+2]

**(b)** i. State whether the statement is true or false:
i.i A transistor has two PN junction.
i.ii The emitter of a transistor is heavily doped.
i.iii Base has the biggest size in a transistor.
i.iv The value of $\alpha$ of a transistor is less than 1.
ii. Draw and explain a fixed bias circuit. [4+6]

**(c)** i. Explain the CE configuration of BJT with circuit diagram, input and output characteristics.
ii. Derive the relation between $\alpha$, $\beta$.
[6+4]

**(d)** i. State whether the statement is true or false:
i.i In P-type semiconductor, the majority carriers are hole.
i.ii A full-wave rectifier utilizes only positive half cycle.
i.iii For a half-wave rectifier : PIV = $2V_m$.

[ Turn over

ii. Distinguish between zener breakdown and avalanche breakdown.
iii. What is Q point? [4+4+2]

III. *Answer* **3 (a) OR (b)** *in this block::*

**3. (a)** i. Compare class A, class B and class C amplifier.
ii. Define cross over distortion and how it can be overcome?
iii. What do you mean by efficiency in power amplifier? [4+3+3]

**(b)** i. Explain the working of schmit trigger with proper circuit diagram
ii. Describe the working of astable multivibrator with a neat circuit diagram
[3+3+4]

IV. *Answer any* **three (03)** from **4 (a), (b), (c) and (d)** *in this block:*

**4. (a)** i. Convert base of the following numbers:
i.i. $(64.5)_{10} \equiv (?)_2$
i.ii. $(7CA3)_{16} \equiv (?)_8$
i.iii. $(742.46)_8 \equiv (?)_2$
ii. Obtain 2's complement of $(1010100)_2$ and $(1101001)_2$.
iii. Subtract (i) $(1110)_2$ from $(10101)_2$ and (ii) $(10011)_2$ from $(11101)_2$ (without converting base).
[6+2+2]

**(b)** i. State De-Morgan's theorem. Show its logic implementation.
ii. Simplify the following Boolean expression:
$f = \left(A + \overline{B}C\right) + \left(\overline{A + \overline{B}C}\right)$ and $f = AB + ABC + \overline{A}B + A\overline{B}C$ [4+6]

**(c)** i. Realize the following two Boolean expressions using basic gates $f = \left(C\left(A + B\right) + D\right)$ and $f = \left(\overline{AB} + + \overline{C}\right)$
ii. Add (a) $(38)_{10}$ and $(17)_{10}$ and (b) $(84)_{10}$ and $(53)_{10}$ using BCD numbers. [6+4]

**(d)** i. Draw the symbols of universal gates. Write their truth table (for 2-input gate).
ii. Realize AND, OR and NOT using only NAND gates. [4+6]

V. *Answer* **5.(a) OR (b)** *from this block:*

**5. (a)** i. Distinguish between combinational circuit and sequential circuits.
ii. What is a flip-flop?
iii. Describe the working of SR flip-flop with circuit diagram and truth table. [3+3+4]

**(b)** i. What is the difference between latch and flip-flop?
ii. What is a clock? What is the purpose of the clock signal?
iii. Draw the circuit diagram of JK flip-flop.
iv. What is race around in JK flip-flop? [2+2+3+3]