Ref No. Ex/EE/5/ET/T/123/2019

B. E. ELECTRICAL ENGINEERING (PART TIME) 1ST YEAR 2ND SEMESTER EXAMINATION, 2019

Subject: Electronics-II **Time: 3.0 Hours** **Full Marks: 100**

No. of questions	Answer any **Five (5)** question: 5×20	Marks
1.	(a) Convert the following numbers: (i) $(1101.1011)_2 = ()_{10}$ (ii) $(75.15)_{10} = ()_2$ (iii) $(125)_{10} = ()_8$ (iv) $(68)_8 = ()_{10}$ (v) $(3A.2F)_{16} = ()_2$ (b) Represent $(-17)_{10}$ in (i) Sign-magnitude, (ii) 1's complement and (iii) 2's complement representation. (c) Explain how an OR gate can be implemented with AND and NOT gates. (d) Implement the Boolean function $X=AB+A'C$ with NAND gates. (e) Design a two input XOR gate exclusively with the help of (i) NAND gates (ii) NOR gates	(5x1)+3+3+4+5
2.	(a) (i) Simplify the following Boolean function in product of sums: $F(A, B, C, D) = \Sigma (0, 1, 2, 5, 8, 9, 10)$ (ii) What is the simplified sum of products form of F? (b) (i) Implement the expression using a multiplexer $F (A, B, C, D) = \sum m (0, 2, 3, 6, 8, 9, 12, 14)$ (ii) Implement the following multi-output combinational logic circuit using a 4-to-16-line decoder $F_1 = \sum m (1, 2, 4, 7, 8, 11, 12, 13)$	(5+5)+(5+5)
3.	(a) What is meant by race-around condition? How can it be avoided by using master-slave *JK* flip-flops? (b) Show that a T flip-flop can be used as a divide by 2 circuit. (c) How can you design a 4-to-1 multiplexer using basic gates? (d) Show that a *JK* flip-flop can be converted into a *D* flip-flop and a T flip-flop.	(2+3)+5+5+5
4.	a) Give the expression of diode current. What do you meant by diode dynamic resistance? Draw and explain the diode I-V characteristic. (b) Calculate the efficiency and ripple factor of a full wave diode rectifier circuit. (c) Draw a suitable circuit with diode to reduce the ripple factor and explain how this circuit reduces the ripple? (d) Why Zener diode provides a constant voltage across it?	(2+2+3)+(3+2)+(3+3)+2

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5.	(a) Explain clearly the Early effect and punch through condition of a BJT. (b) Give a comparative study of CB, CE and CE configuration of BJT for the following parameters. Input and output impedance, current and voltage gain. (c) Explain with a suitable circuit the BJT can be used as a switch. (d) Derive the expression for current gain of a Darlington Pair transistor. (e) Differentiate between current source and current mirror.	(2+2)+4+4+4+4
6.	(a) Mention the advantages of potential divider bias scheme compared to the other biasing scheme. Derive the expression for stability factor for this circuit with respect to I_{CEO}. (b) Give the circuit of a BJT CE amplifier. Sketch and explain the gain versus frequency response curve. Derive the expression for input impedance, output impedance, current gain and voltage gain.	(2+5)+(2+3+8)
7.	(a) Describe how a ***transistorised shunt voltage regulator*** provides a steady state output voltage against the input voltage fluctuation? Write down the output voltage expression for this circuit. (b) Derive the condition of oscillation for a circuit. (c) Classify the different oscillator in accordance with the frequency range. Explain how the condition of oscillation of a COLPITTS oscillator using OPAMP is satisfied. How the frequency of oscillation for this circuit is determined.	(6+2)+4+(2+4+2)
8.	(a) Explain how the output of a 2 input TTL NAND gate becomes high. (b) Give the schematic diagram of CMOS. Mention the areas of application of CMOS. Explain the operation of a CMOS Inverter. (c) Give the operation of an astable multivibrator using 555 IC.	5+(3+2+4)+6

** The symbol $'$ indicates the complement.