ANALYTICAL MODELING OF NEGATIVE CAPACITANCE MOSFETS: EFFECTS OF CHANNEL DOPING AND FERROELECTRIC LAYER THICKNESS WITH DERIVATION OF LANDAU COEFFICIENTS

A Thesis

Submitted for the partial fulfilment of the requirement for the Degree of ***Masters of Engineering*** *in the* ***Dept. of Electronics and Tele-Communication Engineering*** *under the Specialization of* ***Electron Devices***

Jadavpur University

By

SOUMITRA CHAKRAVORTY

Registration Number: 163533 of 2022-23

Class Roll No.: 002210702007

Under the Guidance of

Dr. CHANDRIMA MONDAL

Department of Electronics & Telecommunication Engineering

Jadavpur University, Kolkata- 700032

India

August, 2024

FACULTY OF ENGINEERING AND TECHNOLOGY

JADAVPUR UNIVERSITY

CERTIFICATE

This is to certify that the thesis entitled , **"Analytical Modeling of Negative Capacitance MOSFETS: Effects of channel doping and ferroelectric layer thickness with derivation of Landau coefficients"** submitted by Soumitra Chakravorty (Class Roll No.: **002210702007**, Examination Roll No.: **M4ETC24005**, University Registration No.: **163533 of 2022-23**) of Jadavpur University, Kolkata is a record of bonafide research work under my supervision and can be accepted in partial fulfilment of the requirement for the degree of Master of Engineering in Electronics and Tele-communication Engineering under the specialization of Electron Devices of the institute. The research results represented in this thesis are not included in any other paper submitted for the award of the degree to any other university or institute.

Dr. Chandrima Mondal

Supervisor

Dept. of Electronics and Telecommunication Engineering

Jadavpur University, Kolkata-700032

Prof. Sudhabindu Ray

Head of the Department

Department of Electronics & Telecommunication EngineeringJadavpur University, Kolkata-700032

Prof. Dipak Laha

Dean

Faculty of Engineering & Technology

Jadavpur University, Kolkata-700032

FACULTY OF ENGINEERING AND TECHNOLOGY

JADAVPUR UNIVERSITY

CERTIFICATE OF APPROVAL*

The foregoing thesis is hereby approved as a credible study of an engineering subject and presented in a manner satisfactory to authorization acceptance as a pre-requisite to the degree for which it has been submitted. It is understood that by this approval the undersigned do not necessarily endorse or approve any statement made, opinion expressed or conclusion drawn there in but approve the thesis only for which it is submitted.

Committee on Final Examination

For the Evaluation of the Thesis

_____

Signature of Examiner

_____

Signature of Supervisor

*Only in the case thesis is approved

FACULTY OF ENGINEERING AND TECHNOLOGY

JADAVPUR UNIVERSITY

DECLARATION OF ORIGINALITY AND COMPLIANCE OF AN ACADEMIC THESIS

I hereby certify that this thesis entitled, **"Analytical Modeling of Negative Capacitance MOSFETS: Effects of channel doping and ferroelectric layer thickness with derivation of Landau coefficients"**

- Is original and has been done by me under the guidance of my supervisor
- This work has not been submitted to any other institute for any degree
- All the information have been obtained and presented in accordance with academic rules and the ethical Code of Conduct of the institute

I also declare that, as required by the rules and conduct, wherever I have used materials that are not original to this work, I have given proper credit by citing them in the text of the thesis and giving their details in the list of references.

Soumitra Chakravorty

Class Roll No.: 002210702007

Examination Roll No.: M4ETC24005

University Registration No.: 163533 of 2022-23

Thesis Title : Analytical Modeling of Negative Capacitance MOSFETS: Effects of channel doping and ferroelectric layer thickness with derivation of Landau coefficients

SOUMITRA CHAKRAVORTY

(Signature with date)

ACKNOWLEDGEMENT

I had been working on this project since the month of July, 2023 and by completing this work, my two year journey in Jadavpur University will come to an end. There were a number of hurdles throughout the work but ultimately I have been able to cross them and also been able to reach my goal. At this moment, I feel it needful to express my acknowledgements to many persons for whom I am now in a position to submit this project.

I feel myself fortunate to express my deep sense of gratitude to my project supervisor **Dr. Chandrima Mondal**, Dept. of Electronics & Telecommunications Engineering, Jadavpur University, Kolkata for providing me the opportunity to carry out my thesis work and helping me throughout every inch of this project. I am really grateful to her for the valuable insights she has given me on the concepts revolving my work, the utmost motivation and mental support throughout my research and finally the valuable suggestions for the successful completion of my thesis.

I also convey my heartiest appreciation to **Prof. Sudhabindu Ray**, Head of the Department of Electronics & Telecommunication Engineering, Jadavpur University, Kolkata for his constant support and encouragement. I would also like to thank all the other professors of this department for their opinions and guidance.

I am grateful to my senior **Mr. Sanket Mitra** for his unconditional assistance and support which has smoothened my work very much. I also thank all of my senior lab mates for their moral support towards the fulfilment of this thesis work.

I would also like to extend my sincere thanks to my parents for their love, care, support and guidance throughout my life and finally thank God who has been kind enough to me thus making me able to perform this work.

CONTENTS

CHAPTER 1

INTRODUCTION 9

1.1 Literature Survey 9
1.2 Ferroelectric Materials 19
1.3 Negative Capacitance of a Ferroelectric 23

CHAPTER 2

STRUCTURE OF OUR DEVICE 24

CHAPTER 3

MODEL FORMULATION 26

3.1 Development of semiconductor charge model 27

3.2 Development of threshold voltage model 32

3.3 Development of subthreshold swing model 34

3.4 Development of expressions of Landau coefficients 35

CHAPTER 4

RESULTS

4.1 Threshold Voltage Vs Ferroelectric Thickness at different doping levels 38

4.2 Threshold Voltage Vs Doping with and without β 41

4.3 Subthreshold Swing Vs Doping of both normal and MFIS FET 43

4.4 Subthreshold Swing Vs Ferroelectric Thickness 45

CHAPTER 5

LIST OF REFERENCES 46

ABSTRACT

In this paper, we consider a surface-potential based 1D analytical model for a long-channel negative capacitance (NC) silicon-based Metal Oxide Semiconductor (MOS) transistor. We firstly derive the expressions for the Landau coefficients i.e α and β for the ferroelectric material utilized and further proceed to calculate the threshold voltage (V_T) and subthreshold swing (SS) exploiting the potential balance equation. We finally observe the characteristics of V th and SS with variation in channel doping concentration (N_a) and ferroelectric layer thickness (t_{FE}). We additionally report a study to highlight the non-scalability of ferroelectric parameters with t_{FE} by consulting some experimental results.

CHAPTER 1

INTRODUCTION

Literature Survey

Early days people used to work in the land under sun. That was the only source of intense light those days. They used to calculate using their brain because there was no such device which can do the calculation for them. It was the work of mighty Alessandro Volta who discovered an electric cell that can act as a source of electrical energy. That discovery created a milestone for a new domain. Various discoveries were done after that and it was the mighty work of Thomas Alva Edison who discovered the electric bulb which can be switched on or off as per our wish. But what about the calculator? There was only a mechanical device invented by Charles Babbage that can do the calculation. But how it can be done electrically? Sir Flemming came up with a device called the vacuum tube where the motion of charged particles inside the tube was also a matter of concern in addition to its charge. This created another milestone in the history of Physics. Thus Electronics was born where electron is a charged particle.



Fig 1. Vacuum tubes. These were earlier used to implement electronic circuits

The invention of the tube created a facility for implementation of a variety of functions. It can be used as a switch and as an amplifier. Its switching property led to the discovery of calculators, memory and many things. But it consumed a lot of power and occupied a lot of space and were not reliable. An entire building was needed to house a calculator which contained lots of vacuum tubes and lots of trained people were employed to operate the tube. This wasted a lot of money and situation was tough. Circumstances demanded a small solid-state device which can do the work of vacuum tube. That came up with the honorable work of John Bardeen, Walter Brattain under the supervision of Dr. William Bradford Shockley and that device was named as the transistor. It was a point contact device, more efficient than its vacuum tube in terms of space, power, reliability etc.

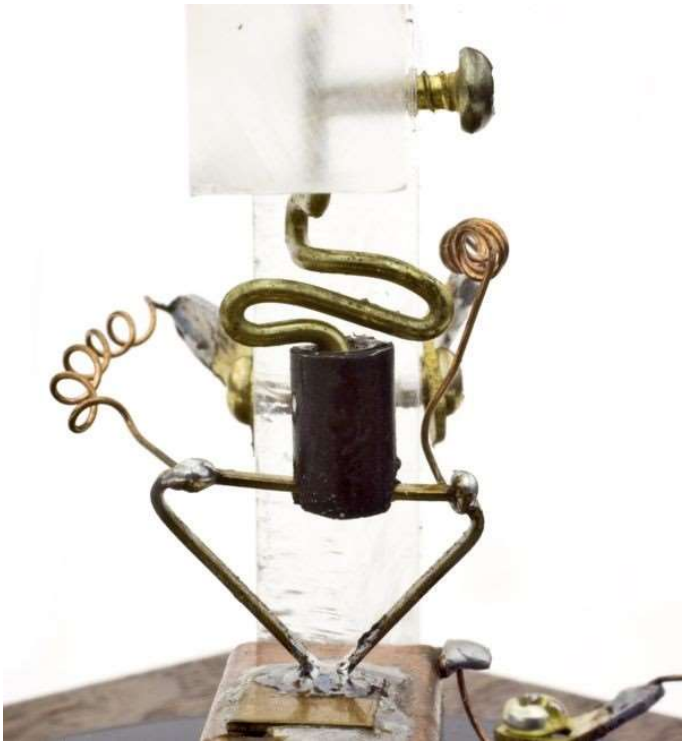


Fig 2. First transistor proposed by Shockley which marked the beginning of solid state electronics

After the discovery of the transistor, many applications became easier and economical compared to the vacuum tube. But still the work of calculation demanded a lot of such transistors which again gave rise to a problem associated with space. In 1952, a British radio engineer Geoffrey Dummer suggested that if a calculator demanded a lot of such devices, then the problem could be solved if we can pack a lot of such devices in a single package. After his idea, in 1958 planar transistors came into picture. These transistors could be manufactured in a single substrate or a slice of semiconductor. The invention of the planar

transistors triggered Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Semiconductors with an idea of manufacturing more than one transistors on a single slice of silicon and connecting them by depositing metal on top of the slice and connecting the devices so that it looks similar to a printed conductors of a printed circuit board. This technology was named integrated circuit and it was developed by them in 1960.

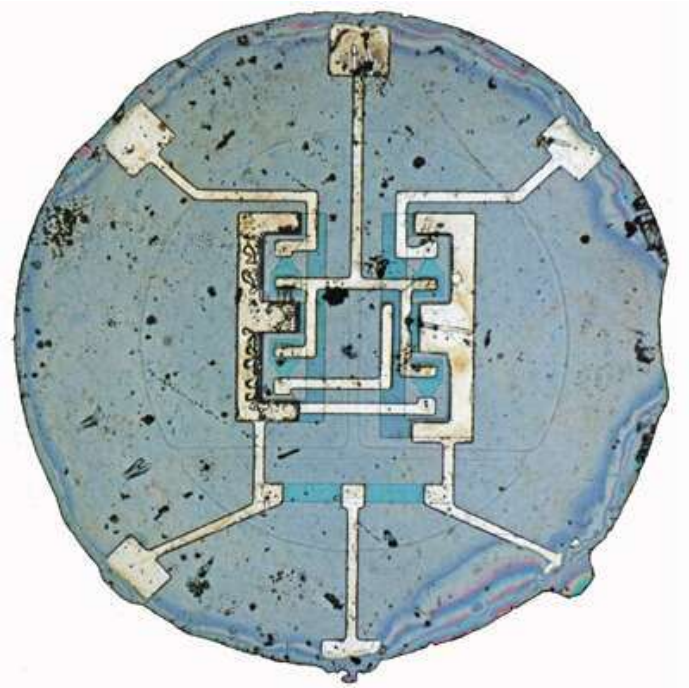


Fig 3. First Integrated Circuit proposed by Noyce of Fairchild Semiconductors

After the development of the integrated circuit, it became easy to fabricate devices in a single slice of silicon. This idea triggered Gordon Moore of Intel Corporations to device a law that states the number of components in an integrated circuit would double after every 18 months. This idea led to the discovery of various sophisticated electronic devices that we see today in our daily life.

Parallel to this development, another transistor structure was also proposed where the control terminal is insulated from the semiconductor. In that device, silicon dioxide was used as the insulator and silicon was used as the semiconductor. The control terminal was made of metal. This gave the device the name Metal Oxide Semiconductor Field Effect Transistor (in short MOSFET). That device had a symmetric structure that made it easier for fabrication in an integrated circuit and it also occupied less space compared to the transistor proposed in 1948. This slowly made MOSFET a patent device for integrated circuits.

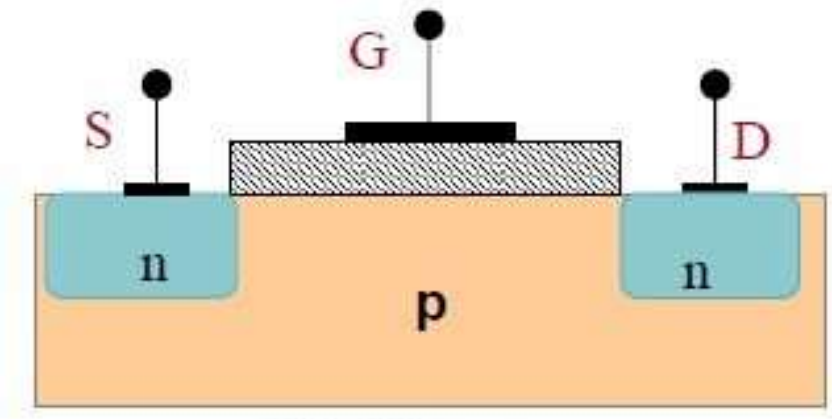


Fig 4.This is the structure of a MOSFET. It has two n-type regions inside the p-type structure. The left side n-region is called the source and the right side n-region is called the drain. There is a layer of insulator above p-type structure which is grey here. Above the insulator is a layer of metal which is shown by a black colour. It is called the gate of the MOSFET. From the source, drain and the gate, wires come out which is required for providing the desired electric potential. Normally current does not flow through this device even if potential difference is applied between source and drain because there is a barrier field of pn-junction which prevents the carriers from entering the p-region. When desired potential is applied at the gate, a layer of n-type region develops below the insulator in the p-region and then the device allows current to flow between source and drain if there is a potential difference between source and drain. So without proper potential at the gate, the device remains non-conducting and with it, the device starts to conduct. So the device can be used as a switch. This switching property makes it useful as logic devices of computer processors. Since the layer here developed here is n-type, it is n-channel MOSFET because this layer of electrons act as a channel for charge low from source to drain.

Keeping pace with Moore's law, the number of components per slice increased. This increase occurred by scaling down the size of MOSFETs. As their size became smaller, their response became faster. They also consumed lesser power. Thus high speed, low power, high functionality integrated circuits started appearing in the market.

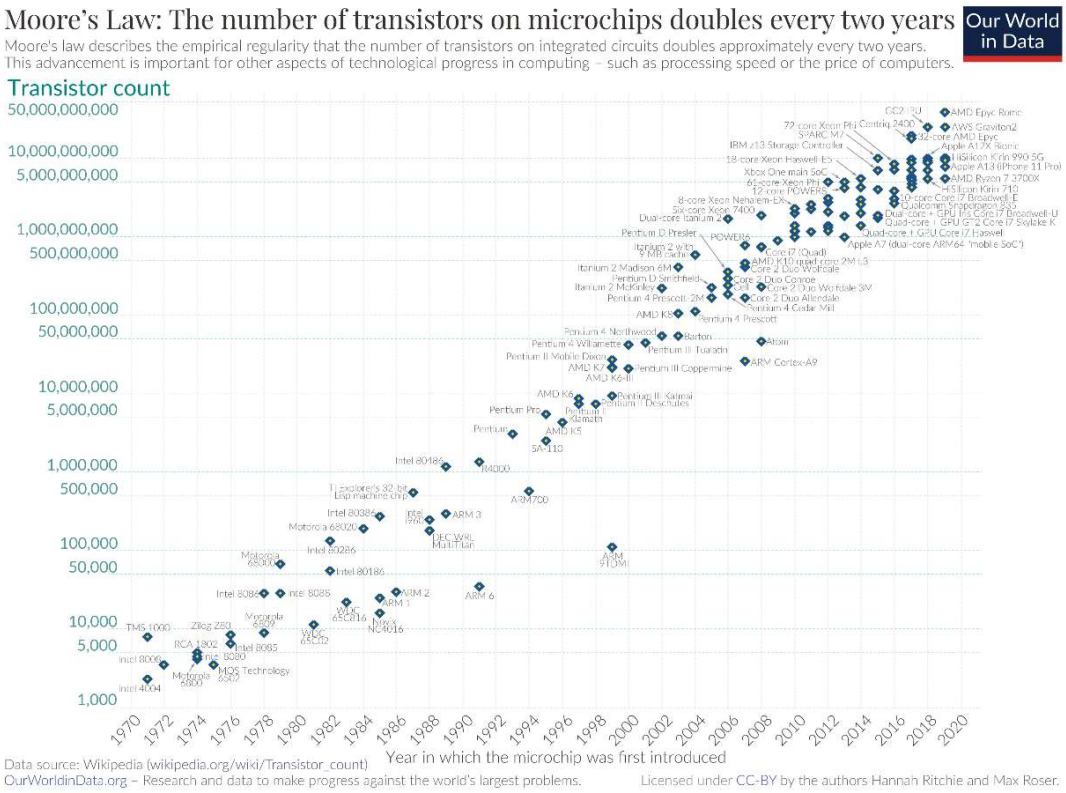


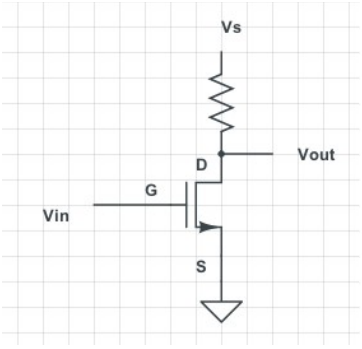
Fig 5. Moore's Law showing increase in the number of transistors in processors till 2020

Increase in the number of devices in a chip though permitted more functions to be implemented on the same chip but it posed various problems. The fabrication of components became more difficult in maintaining the correct precision in their dimensions and shape and they also started showing some undesirable effects which hampered their performance.

As the transistors are made smaller, their source and drain come closer. As they come closer, the oppositely doped region between the source and drain becomes comparable to the base width of a bipolar transistor of the same dimensions as the MOSFET where the source acts as the emitter and the drain acts as the collector. So when potential difference is applied between the source and drain, significant current starts to flow due to transistor action even if the gate voltage is below the threshold voltage. So if the device is desired to be off even if there is a potential difference between the source and drain, the device can't be made off due to this current flow and the device remains on. This creates a severe problem in digital switching operation.

Moreover, since the number of components increased in the chip power dissipation in the chip also increased which made the chip hot and reduced the age of the chip if heat sinks were not properly used. So low power dissipation capability of the chip reduced.

The power dissipation in the chip mainly occurs due to current flow through various components in the chip. But this power dissipation also varies between various configurations of the components. For example, when logic circuits are implemented using MOSFETs in resistor-transistor logic mode, power dissipation occurs more than the case where logic circuits are implemented with MOSFETs where they are used in complementary mode.



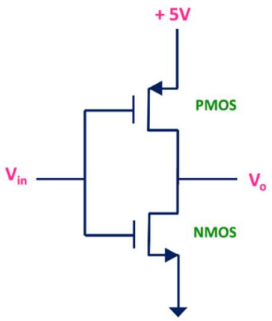


Fig 2(a) Fig 2(b)

Fig 6. It gives the implementation of NOT logic using a) Resistor-Transistor mode using MOSFET and b) Complementary mode where both n-channel and p-channel MOSFETs are used

In resistor-transistor NOT gate, when 0V is applied to the gate of the transistor as input, the transistor does not conduct current. We get the entire supply voltage at the output. When input voltage to the gate is high, the transistor conducts current and current flows from supply voltage to the ground through the resistor and the transistor. As a result low voltage appears at the output and the circuit behaves like an inverter of logic level. Now, in the case where we see that the input voltage is high, current is continuously flowing through the circuit. So there is power dissipation. In the complementary mode, when the input voltage is low, the p-channel MOSFET is in conducting mode, whereas the n-channel MOSFET is in non-conducting mode. So the entire supply voltage appears at the output terminal. When the input voltage is high, the p-channel transistor is off and the n-channel transistor is on, so the ground potential appears at the output terminal. Here, in this case we observe that in both the cases, when one transistor is on, the other transistor is off. So, there is no path for current flow from the supply to the ground. So there is no current and hence power dissipation is zero here. So we see that resistor-transistor logic consumes power during operation whereas the

complementary case does not consume any power. This made complementary MOSFET technology an accepted choice for integrated circuits.

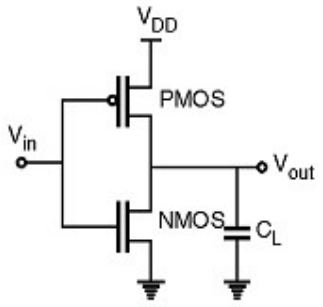


Fig 7. CMOS inverter with a load capacitor

Though complementary MOSFET technology had the advantage of zero power dissipation, but it consumed power when logic level at the input changed. This happened because any logic family has a load capacitor C_L at the output node. Considering that the load capacitor was initially uncharged, when the input voltage goes high, the p-channel transistor turns on and the n-channel transistor turns off. The p-channel transistor provides a path for current to flow to the load capacitor to charge it and the load capacitor gets charged to high voltage to give logic high at the output. During the charging process due to flow of current, power dissipation occurs in the circuit. It occurs till the capacitor is fully charged to power supply voltage. When the input voltage goes low, the p-channel transistor turns off and the n-channel transistor turns on.

The n-channel transistor provides a path to the ground for the capacitor to discharge. So the capacitor discharges through the n-channel transistor and the voltage across it decreases so that output logic becomes low and current flows. This current flows till the capacitor is fully discharged. So during this time, there is power dissipation. So as a result power dissipation occurs in complementary MOSFET technology inverter when there is a transition in logic level. Since this power dissipation occurs during transition, this power dissipation will occur the number of times transitions occur. So, this power dissipation is proportional to the frequency of transitions. Since the load capacitor charges and discharges during transition, it has to store that much amount of energy proportional to the square of the voltage across it and its capacitance and discharge the same amount of it. So it stores energy proportional to the square of the supply voltage and its capacitance and discharges the same amount of it. So if the supply voltage is high, the capacitor has to store a lot of energy and as a result of it lot

of power will be dissipated for its charging and same goes for discharging. So if there are millions of transistors in a chip, then during transitions, lots of power will be dissipated and lot of heat will be generated. So, to reduce the power dissipation, in addition to keeping the number of transitions as low as possible for the job, we have to reduce the supply voltage.

Reducing the supply voltage reduces the amount of stored charge in the load capacitor by a large amount since stored charge in the capacitor is proportional to square of the voltage across it. So reducing supply voltage is a good practice to reduce power dissipation. But it is found that the trend to reduce the supply voltage cannot be continued fully. This is because if we want to reduce the supply voltage, we need to reduce the threshold voltage of the MOSFET. If we reduce the threshold voltage of the MOSFET beyond a certain limit, significant amount of leakage current is found to flow from the drain to source of NMOSFET (source to drain for PMOSFET) for a small applied potential difference between the source and drain even if the gate voltage is less than the threshold voltage. This leakage current can significantly impact the performance of the circuit if there are millions of transistors. Moreover if the source and drain comes closer along with this impact, the structure becomes like an npn or a pnp bipolar transistor and current starts to flow between source and drain due to transistor action because source and drain acts like emitter and collector of bipolar transistor and since current now flows due to transistor action, the leakage current is significantly large which may adversely affect the performance of the circuit. To avoid this problem attention is needed to be focused on a parameter called subthreshold swing which determines the change in gate voltage for a decade change in current. Since this parameter detects the change in gate voltage for a decade change in current, we can detect the change of gate voltage for orders of magnitude change in current. This makes our detection of off-current to on-current ratio more easily because on-current and off-currents vary by orders of magnitude.

Suppose current I is flowing between the source and drain of the MOSFET. The potential difference between the source and drain is V_D. Let the potential at the gate of the MOSFET be V_G with respect to source assuming both the source and the body are grounded.

So subthreshold swing is given as change in gate voltage Vg with respect to decade change in current as shown below.

$$\text{SS} = \frac{d(V_G)}{d(\log(I))}$$

where logarithm is to the base 10

$= \frac{d\Psi_S}{d(\log(I))} . \frac{d(V_G)}{d\Psi_S}$

where Ψ_S is the surface potential

The term $\frac{d\Psi_S}{d(\log(I))}$ is the change of surface potential per decade change of current.

The term $\frac{d(V_G)}{d\Psi_S}$ is the change of gate voltage per volt change of surface potential.

If this subthreshold swing is small, then a very small amount of voltage changes for order of magnitude change in current. So if threshold voltage is small, a device with small subthreshold swing has a very less subthreshold leakage current. So that device will be much more efficient in performance.

To reduce this subthreshold swing, various works have been done to reduce the term $\frac{d\Psi_S}{d(\log(I))}$. Various transistor structures have been proposed in the literature which have low value of subthreshold swing. These are tunnel FETs, I-MOS and feedback FETs. These structures made the subthreshold swing small but they either did not produce any current enhancement or limited the supply voltage scaling since they relied on high electric field within the structure. So this created a problem.

Then focus was shifted to the reduction of the term $\frac{d(V_G)}{d\Psi_S}$. On focusing on it, it was found that it was impossible to reduce the subthreshold swing beyond a certain limit. This can be shown as follows:

$\frac{d(V_G)}{d\Psi_S}$ is given by the capacitance voltage divider relation as

$\frac{d(V_G)}{d\Psi_S} = 1 + \frac{C_s}{C_{ins}}$

where C_s is the semiconductor capacitance per unit area and

C_{ins} is the insulator capacitance per unit area.

To make the term smaller the insulator capacitance is needed to be made large by using high dielectric constant materials and keeping the insulator thickness thin. Lowering the thickness of the insulator though increased the capacitance but at the same time, it increased the

tunnelling current from semiconductor to the gate. Moreover the term $\frac{d(V_G)}{d\Psi_S}$ was not possible to be made lesser than 1 practically. So the subthreshold swing was found impossible to be made lower than 60 millivolt per decade change of current.

It was the honorable work of Sayeef Salahuddin who proposed an idea of replacing the insulator by a ferroelectric material which lowered the $\frac{d(V_G)}{d\Psi_S}$ value than 1 by a mechanism called negative capacitance. This opened up a new idea where we can further lower the supply voltage and have circuits operating with lower power.

Ferroelectric Materials

Solids can be classified into broadly four categories based on their ability to conduct electric current when potential difference is applied across their ends. They are conductors, insulators, semiconductors and superconductors. Conductors are materials which allow electric current to flow through them easily when potential difference is applied across its ends. Insulators are materials that do not allow current to flow through them when potential difference is applied across their ends. Semiconductors are materials which allow electric current to flow through them not so good like conductors and they also do not block current to flow through them like insulators. But they have a peculiar characteristic that their ability can be tuned in such a way that under certain conditions they will allow no current to flow through them and in other conditions they will allow easy flow of current through them. Superconductors are materials that allow easy flow of current through them with no loss when potential difference is applied across their ends.

When potential difference is applied across the ends of an insulator, there is no current conduction but there is other thing that happens. The thing that happens depends on the nature of the atoms or molecules present in them. This nature of atoms and molecules classifies them into two categories: polar and non-polar. Polar atoms and molecules are those whose centres of positive and negative charges are not the same. Non-polar atoms and molecules are those whose centres of positive and negative charges are the same. When potential difference is applied between an insulator containing non-polar molecules, the negative charge centre of the molecule shifts towards the direction of high potential and positive charge centre moves towards the direction of low potential. As a result, there is a displacement of the centers of positive and negative charges. This constitutes a dipole and it has an associated dipole moment. So the atom or molecule has become polar and there is a polarization vector associated with the substance which is dipole moment per unit volume of the material which depends on the strength of the electric field. These materials are also called dielectrics because there is a development of dipole moment of an atom or a molecule which we can use for various purposes. When electric field is removed, all the polarization is lost in the material and the material again returns to its initial state.

For a dielectric, the polarization **p** of an atom is given as

$\mathbf{p} = \alpha\varepsilon_0\mathbf{E}$

where ε_0 is the permittivity of vacuum

E is the applied electric field

and α is the atomic polarizability

The polarization **P** of the substance is the dipole moment per unit volume of the material.

It is given as $\mathbf{P} = N\,\alpha\varepsilon_0\mathbf{E}$

where N is the number of atoms or molecules per unit volume.

Here polarization and electric field are vectors, so they are mentioned in bold.

In the case of insulators containing polar molecules, the atoms or molecules have permanent dipole moments. The dipole moments have some random orientation. The nature of their random orientation further classifies the polar insulators into various types. In one type all the dipoles are randomly oriented. In other type one group of dipoles have a fixed orientation, another group has a fixed orientation and so on. Here since a group of dipoles have a fixed orientation, in this material we will find a region where all the dipoles are oriented in the same direction. This region has a directed dipole moment and is called a domain. So we will find domains in this material and all of the domains have a random direction of dipole moment. These materials which have domains of dipoles directed randomly are called ferroelectric materials because they have electric dipole domains analogous to the magnetic domains of a ferromagnetic material. These materials may or may not have a resultant non-zero polarization in the absence of an external electric field.

When potential difference is applied between the ends of an insulator containing polar molecules, the negative charge center moves towards the direction of high potential and the positive charge center moves towards the direction of low potential. Since they are polar molecules and they have a dipole moment, they experience a torque due to this opposite movement of two charge centers. This torque tents to align the dipoles in the direction of the electric field. As a result the polarization of the material increases from the value of zero electric field if present.

When potential difference is applied across the ends of a ferroelectric material, the domains tend to align themselves in the direction of the electric field. Moreover, like normal polar

insulators, the dipoles in other domains also experience a torque which tends to align themselves in the direction of the electric field. As a result if these dipoles are near a domain which is aligned already in the direction of the electric field, these dipoles together with the domain get added together to give resultant dipole moment which makes the domain oriented in the direction of the electric field grow in size. So here the domains align themselves in the direction of the electric field and they also grow in size to give a resultant dipole moment and polarization. So the polarization of the material has increased from the value that was initially present when no electric field was applied.

When the potential difference across the ferroelectric is removed, the polarization of the ferroelectric does not become zero. Some amount of polarization remains even after the removal of the external electric field. This polarization is called the remnant polarization.

Ferroelectrics do not show polarization verses electric field curve like other insulators containing polar atoms and molecules. Rather it shows a hysteretic behavior like magnetic induction verses magnetic field curve of a ferromagnet. This can be explained as follows:

Initially we assume that the domains in the ferroelectric are oriented in such a way that, the resultant polarization in the ferro-electric is zero. When potential difference is applied across the ends of the ferroelectric, the domains experience a torque and they grow in size so that there is a resultant polarization in the material. As the potential difference is increased, the polarization increases and finally it saturates to a value at some value of the potential difference. This value of polarization is called the saturation polarization. After attaining saturation, the value of polarization increases very less with applied potential difference. Now when we start decreasing the value of applied potential difference, the value of polarization decreases. But when the value of potential difference is made less than the value at which the polarization saturated, the polarization decreases with decrease in potential difference but does not follow the path with which it increased initially. It decreases less compared to its increase earlier. As a result when the potential difference is made equal to zero, the polarization has decreased but not became zero as expected normally. So at zero applied potential difference, we see a polarization in the material. This polarization is called the remnant polarization denoted by P_r. When the potential difference is made lesser than zero(increased in the opposite direction), the polarization further decreases and becomes zero at some value of the potential difference. This potential difference or the electric field is called the coercive field denoted by E_C. When the electric field is further increased in the opposite

direction, polarization increases in the opposite direction and again saturates to saturation polarization in the opposite direction and increases less with increase in potential difference. Again, when the potential difference of opposite direction is decreased the polarization decreases flowing the same path till the potential difference where the polarization almost saturated and again follows different path of decrease. So when the applied potential difference is again zero, there is some polarization left in the material in the opposite direction called remnant polarization. When the potential difference is again increased above zero, the opposite polarization decreases and again goes to zero at some value of potential difference called coercive field for negative remnant charge. When the potential difference is increased further, the polarization increases above zero and again saturates to the same value forming a loop same as the magnetic induction verses magnetic field curve of a ferromagnetic material. That's why its is called a ferroelectric material. This curve can be traced from experiments where we want to test the material as an isolated entity, free from other passive elements connected to it in series.

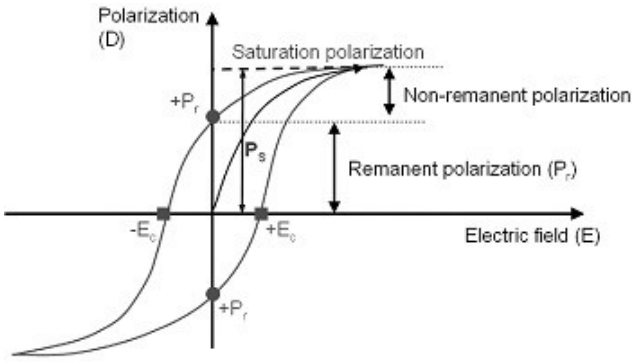


Fig 8. Hysteretic Polarization verses Electric Field Curve of a ferroelectric material

Negative Capacitance in Ferroelectric Materials

Another important property of ferroelectric materials is that when they are connected in series with a capacitor made of normal dielectric material, they show a peculiar property that the charge stored in the material or the polarization in the material increase with decrease in the value of external potential difference across it. This is called negative capacitance effect since the charge stored in the material or the polarization in the material increase with decrease in the value of external potential difference across it. Since the potential difference across it decreases, since it is in series with a normal capacitor the charge stored in each of them is the same the potential difference across the normal capacitor is more and allows more charge to be stored in it.

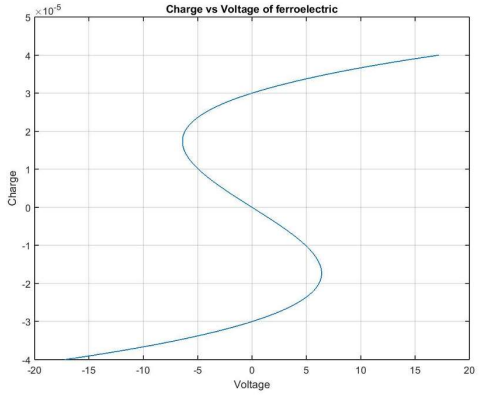


Fig 9. S-curve of a ferroelectric material

The negative capacitance principle can be explained by Landau-Devonshire theory which states that the total energy in a ferroelectric is given as $U = \alpha P^2 + \beta P^4$[7]where α and β are anisotropic constants and P is the polarization inside the ferroelectric. This can also be shown from the S-curve of ferroelectrics.

CHAPTER 2

STRUCTURE OF OUR DEVICE

In the literature, two device structures have been proposed. One is the Metal Ferroelectric Insulator Semiconductor Field Effect Transistor or MFIS FET and the other one is the Metal Ferroelectric Metal Insulator Semiconductor Field Effect Transistor or MFMIS FET. Both the structures have relative advantages and disadvantages. The MFIS structure is more stable compared to the MFMIS structure because in MFMIS structure, there is more chance of leakage compared to the MFIS structure[8]. Moreover, the MFIS structure is relatively easy to fabricate compared to the MFMIS structure because in MFMIS structure, we have to deposit an extra layer of metal above the insulator and then deposit the ferroelectric above it and then the gate which increases the complexity of fabrication. Moreover after fabrication many interface trapped charges exist between various interfaces due to discontinuity of the material which reduces the performance of the device.

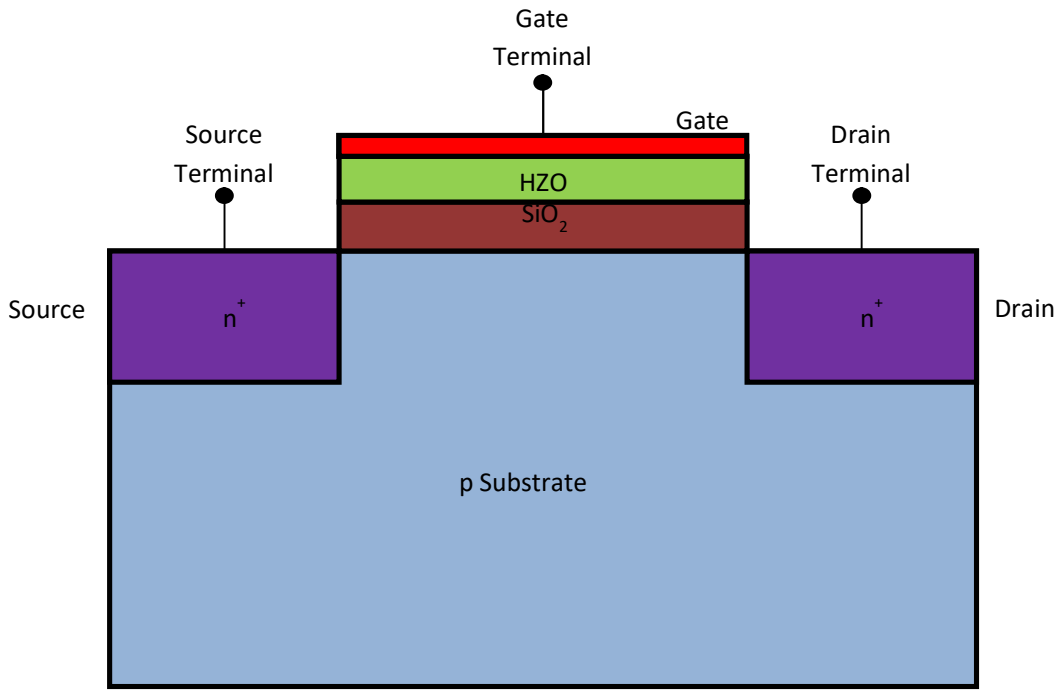


Fig 10. MFIS structure

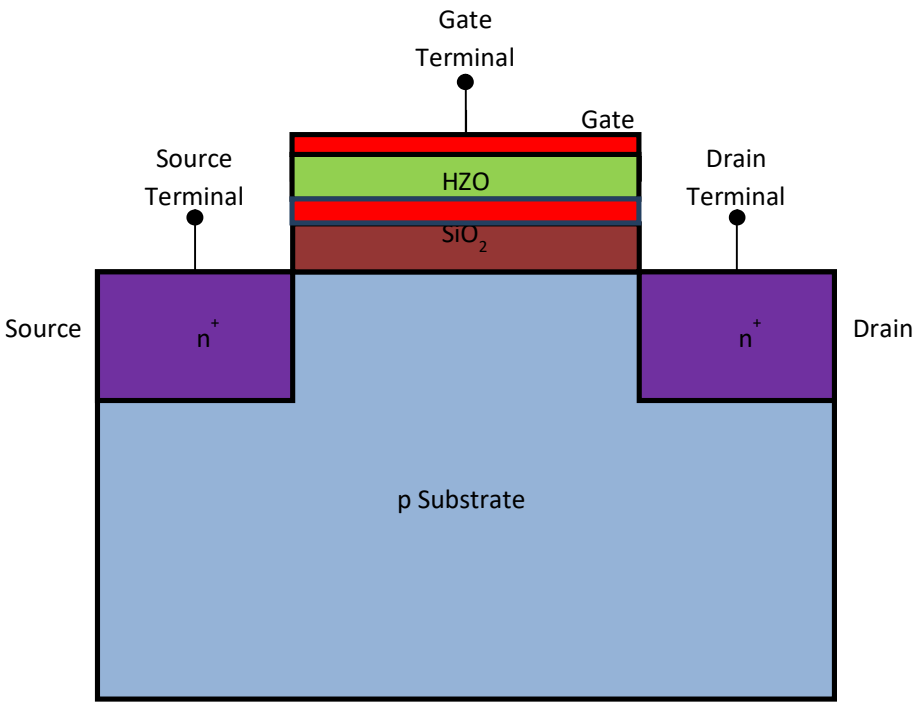


Fig 11. MFMIS Structure

In our work we have considered some constant parameters to develop and simulate our model. These are listed below.

Table 1. List of constant parameters

Sl No.	Parameter	Value
1.	Permittivity of free Space	8.854×10^{-14} $C^2kg^{-1}cm^{-3}s^2$
2.	Dielectric Constant of silicon	11.7
3.	Dielectric Constant of silicon Dioxide	3.9
4.	Charge of Electron	1.6×10^{-19} coulomb
5.	Work Function of metal	5.2 eV
6.	Work function of oxide	4.7 eV
7.	Thermal Voltage	26 mV
8.	Oxide thickness	2 nm
9.	Channel Length	200 nm
10.	Channel Width	1000 nm

The other parameters used in our work include the ferroelectric anisotropy constants α,β, ferroelectric thickness, doping concentration which are variable and they are mentioned in the results along with their corresponding tables.

CHAPTER 3

MODEL FORMULATION

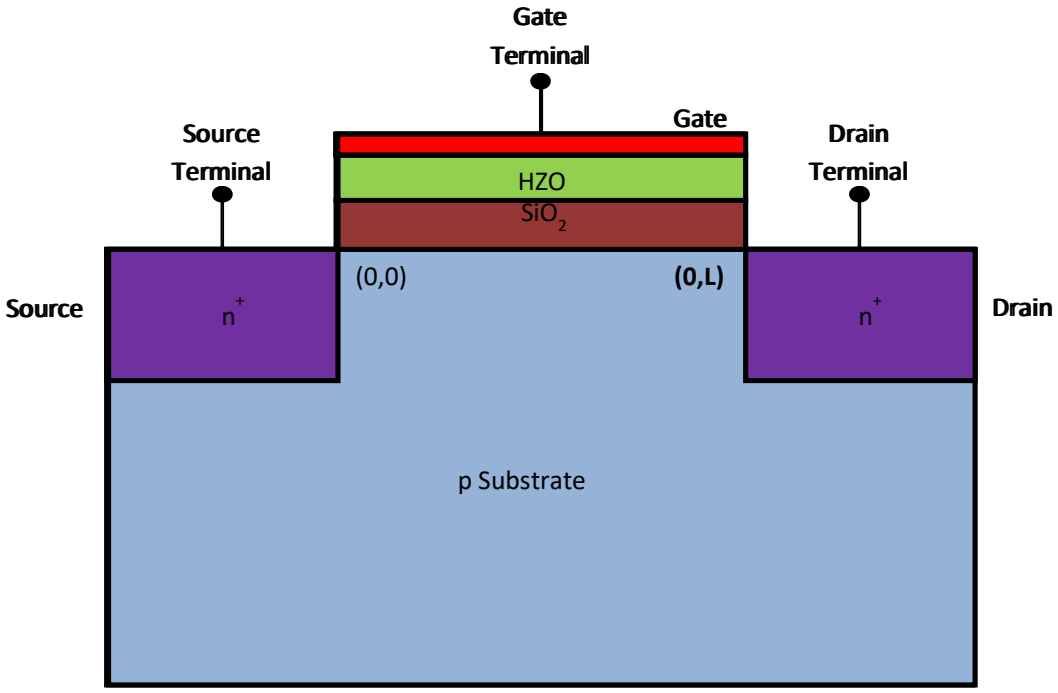
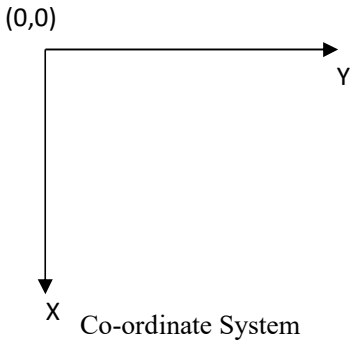


Fig 12. MFIS structure



Co-ordinate System

Here we have chosen Cartesian co-ordinate system with x-axis pointing vertically downwards and y-axis pointing horizontally rightwards. Here the semiconductor surface is at the interface between oxide and semiconductor. At the semiconductor surface, the x co-ordinate is 0. The y co-ordinate varies from 0 to channel length L from source end to drain end. We have assumed here source to be grounded and all voltages are measured with respect to source.

Development of semiconductor charge model

When the gate and the body are shorted, there is electron flow in the wire till a condition of equilibrium is reached where the Fermi Level of the metal and the semiconductor line up. In this condition, there is an electric field developed at the surface of the semiconductor and potential difference exists between the body and the surface of semiconductor. This potential difference causes variation of concentration of charge carriers from surface to body. The concentration of charge carriers at the surface is given as follows:

In equilibrium, the diffusion and drift components of currents of electrons and holes balance individually[1],[9].

So for electrons,

$J_{drift} + J_{diffusion} = 0$

where J_{drift} is the drift current density and $J_{diffusion}$ is the diffusion current density

J_{drift} for electrons is given as $q\mu_n nE$, where q is the electronic charge in coulombs, μ_n is the mobility of electrons, n is the density of electrons per centimetre cube and E is the electric field.

$J_{diffusion}$ for electrons is given as $qD_n\frac{dn}{dx}$, where q is the electronic charge in coulombs, D_n is the diffusion coefficient for electrons and $\frac{dn}{dx}$ is the concentration gradient of electrons.

So, $q\mu_n nE + qD_n\frac{dn}{dx} = 0$

or, $\mu_n nE + D_n\frac{dn}{dx} = 0$

or, $-\mu_n n\frac{dV}{dx} + D_n\frac{dn}{dx} = 0$

where electric field is the negative gradient of potential, $E = -\frac{dV}{dx}$

So, $-\mu_n n\frac{dV}{dx} + D_n\frac{dn}{dx} = 0$

or, $-\mu_n n(dV) + D_n(dn) = 0$

or, $dV = \frac{D_n}{\mu_n}\frac{dn}{n}$

or, $dV = V_t\frac{dn}{n}$

where V_t is the thermal voltage we get using Einstein's relation

Integrating both sides using proper limits, we get

$\int_0^{\Psi_S} dV = \int_{n_0}^{n_S} \frac{dn}{n}$

where Ψ_S is the surface potential, n_S is the surface electron concentration and n_0 is the electron concentration in the bulk

So, $\Psi_S = V_t \ln(\frac{n_S}{n_0})$

To get the equation with respect to bulk doping concentration, we replace n_0 by n_i^2/N_a where n_I is the intrinsic carrier concentration and N_a is the doping concentration.

So, $\Psi_S = V_t \ln(\frac{n_S}{\frac{n_i^2}{N_a}})$

or, $\Psi_S = V_t \ln(\frac{\frac{n_S}{N_a}}{\frac{n_i^2}{N_a^2}})$

or, $\Psi_S = V_t \ln(\frac{n_S}{N_a}) - V_t \ln(\frac{n_i}{N_a})^2$

or, $\Psi_S = V_t \ln(\frac{n_S}{N_a}) + 2V_t \ln(\frac{N_a}{n_i})$

or, $\Psi_S = V_t \ln(\frac{n_S}{N_a}) + 2\phi_F$

where $\phi_F = V_t \ln(\frac{N_a}{n_i})$

or, $\Psi_S - 2\phi_F = V_t \ln(\frac{n_S}{N_a})$

or, $n_S = N_a e^{\frac{(\Psi_S - 2\phi_F)}{V_t}}$ …(1)

Similarly for holes we proceed in the same manner.

So for holes,

$J_{drift} + J_{diffusion} = 0$

where J_{drift} is the drift current density and $J_{diffusion}$ is the diffusion current density

J_{drift} for holes is given as $q\mu_p pE$, where q is the electronic charge in coulombs, μ_p is the mobility of holes, p is the density of holes per centimetre cube and E is the electric field.

$J_{diffusion}$ for holes is given as $-qD_p(\frac{dp}{dx})$, where q is the electronic charge in coulombs, D_p is the diffusion coefficient for holes and $\frac{dp}{dx}$ is the concentration gradient of holes.

So, $q\mu_p pE - qD_p\frac{dp}{dx} = 0$

or, $\mu_p pE - D_p\frac{dp}{dx} = 0$

or, $-\mu_p p\frac{dV}{dx} - D_p\frac{dp}{dx} = 0$

where electric field is the negative gradient of potential, $E = -\frac{dV}{dx}$

So, $-\mu_p p\frac{dV}{dx} - D_p\frac{dp}{dx} = 0$

or, $-\mu_p p(dV) - D_p(dp) = 0$

or, $-dV = \frac{D_p}{\mu_p}\frac{dp}{p}$

or, $-dV = V_t\frac{dp}{p}$

where V_t is the thermal voltage we get using Einstein's relation

Integrating both sides using proper limits, we get

$-\int_0^{\Psi_S} dV = V_t \int_{p_0}^{p_S} \frac{dp}{p}$

where Ψ_S is the surface potential, p_S is the surface hole concentration and p_0 is the hole concentration in the bulk.

So, $-\Psi_S = V_t \ln(\frac{p_S}{p_0})$

or, $-\Psi_S = V_t \ln(\frac{p_S}{N_a})$

because bulk hole concentration is equal to the bulk doping concentration.

Or, $p_S = N_a e^{\frac{-\Psi_S}{V_t}}$ …(2)

Now to get the electric field, we now apply the one-dimensional Poisson's equation inside the charged region.

So, $\frac{d^2\Psi}{dx^2} = -q\ \frac{p-n-N_a}{\varepsilon_s}$ [2],[4]

where ε_s is the permittivity of silicon.

Or, $\frac{d^2\Psi}{dx^2} = -q\frac{(N_a e^{-\frac{\Psi}{V_t}} - N_a e^{\frac{\Psi-2\phi_F}{V_t}} - N_a)}{\varepsilon_s}$ [From (1) and (2)]

or, $\frac{d^2\Psi}{dx^2} = -qN_a\frac{(e^{-\frac{\Psi}{V_t}} - e^{\frac{\Psi-2\phi_F}{V_t}} - 1)}{\varepsilon_s}$

or, $\frac{d}{dx}(\frac{d\Psi}{dx}) = -qN_a\frac{(e^{-\frac{\Psi}{V_t}} - e^{\frac{\Psi-2\phi_F}{V_t}} - 1)}{\varepsilon_s}$

or, $(\frac{d\Psi}{dx})d(\frac{d\Psi}{dx}) = -qN_a\frac{(e^{-\frac{\Psi}{V_t}} - e^{\frac{\Psi-2\phi_F}{V_t}} - 1)}{\varepsilon_s}d\Psi$

Now $\frac{d\Psi}{dx} = -E$,

So, $EdE = -qN_a\frac{(e^{-\frac{\Psi}{V_t}} - e^{\frac{\Psi-2\phi_F}{V_t}} - 1)}{\varepsilon_s}d\Psi$

Integrating both sides within proper limits, we get

$\int_0^{Es} EdE = (-\frac{qN_a}{\varepsilon_s})\int_0^{\Psi_S} Xd\Psi$

where $X = \frac{(e^{-\frac{\Psi}{V_t}} - e^{\frac{\Psi-2\phi_F}{V_t}} - 1)}{\varepsilon_s}$, E_S is the perpendicular electric field at the surface and Ψ_S is the surface potential

or, $\frac{E_S^2}{2} = \frac{qN_aX'}{\varepsilon_s}$ …(3)

where $X' = V_t((e^{\frac{-\Psi_S}{V_t}} - 1) + (e^{\frac{\Psi_S-2\phi_F}{V_t}} - e^{\frac{-2\phi_F}{V_t}}) + \Psi_S)$ …(4)

So, $E_S^2 = \frac{2qN_aX'}{\varepsilon_s}$

The electric field in a medium depends on the permittivity of the medium. When it is multiplied by the permittivity of the medium we get electric displacement density which is independent of the medium.

So, $\varepsilon_s^2 E_S^2 = D^2 = 2qN_a\varepsilon_sX'$ …(5)

Now from Gauss' law, electric displacement density is equal to the amount of charge enclosed within the closed surface per unit area of the closed surface. Now here if we consider the space charge region as the closed body, then

$D = Q_S$

where Q_S is the semiconductor charge per unit area.

So, $Q_S = (2qN_a\varepsilon_s X')^{\frac{1}{2}}$ …(6)

When $\Psi_S = 0$ and $2\phi_F$,

$Q_S = 0$ and $(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}}$

which we can easily get from the equation $Q_S = (2qN_a\varepsilon_s\Psi_S)^{\frac{1}{2}}$ which is obtained from depletion approximation equation. So the generalised equation converges to depletion approximation at flat-band and threshold point. It is also seen from simulations that the generalised equation and the approximated equations do not vary significantly. So we can take the depletion approximation as the equation for semiconductor charge in this range of values of surface potential.

So, $Q_S = Q_S = (2qN_a\varepsilon_s\Psi_S)^{\frac{1}{2}}$ …(7)

Development of threshold voltage model

Now, when we consider the voltage drop across the various layers, we use the potential balance equation as

$V_G = V_{FB} + V_F + \Psi_{ox} + \Psi_s$ ...(8)

where,V_G is the gate voltage, V_{FB} is the flat-band voltage, V_F is the voltage dropped across the ferroelectric, Ψ_{ox} is the voltage dropped across the oxide and Ψ_s is the voltage dropped across the semiconductor.

V_{FB} is given by the work-function difference between the metal and the semiconductor divided by the electronic charge. V_F is given by the Landau-Devonshire theory as

$V_F = 2\alpha t_{fe}Q + 4\beta t_{fe}Q^3$ ...(9)

where t_{fe} is the thickness of the ferroelectric, Q is the charge stored inside the ferroelectric per unit area and α and β are anisotropy constants dependent on the ferroelectric material.

Ψ_{ox} is the voltage drop across the oxide given by Q/C_{ox} where C_{ox} is the oxide capacitance given as $\frac{\varepsilon_{ox}}{t_{ox}}$ where ε_{ox} is the permittivity of the oxide and t_{ox} is the oxide thickness.

Ψ_S is the usual surface potential.

Now the surface potential with respect to the gate voltage can be calculated as follows:

$V_G = V_{FB} + V_F + \Psi_{ox} + \Psi_s$

or, $V_G = V_{FB} + 2\alpha t_{fe}Q + 4\beta t_{fe}Q^3 + \frac{Q}{C_{ox}} + \Psi_S$ [From (9)]

Here, the capacitance combination is a series one, so the charge stored in each of them is the same.

So, $V_G = V_{FB} + 2\alpha t_{fe}Q + 4\beta t_{fe}Q^3 + \frac{Q}{C_{ox}} + \Psi_S$

or, $V_G = V_{FB} + 2\alpha t_{fe}(2qN_a\varepsilon_s\Psi_S)^{\frac{1}{2}} + 4\beta t_{fe}(2qN_a\varepsilon_s\Psi_S)^{\frac{3}{2}} + \frac{(2qN_a\varepsilon_s\Psi_S)^{\frac{1}{2}}}{C_{ox}} + \Psi_S$ [Using (7)]

or, $V_G = V_{FB} + 2\alpha t_{fe}\gamma\Psi_S^{\frac{1}{2}} + 4\beta t_{fe}\gamma^3\Psi_S^{\frac{3}{2}} + (\gamma\frac{\Psi_S^{\frac{1}{2}}}{C_{ox}}) + \Psi_S$

where $\gamma = (2qN_a\varepsilon_s)^{\frac{1}{2}}$ is a constant.

If we let $\Psi_S^{\frac{1}{2}}$ = z, then the equation becomes

$V_{GB} = V_{FB} + 2\alpha t_{fe}\gamma z + 4\beta t_{fe}\gamma^3 z^3 + \frac{\gamma z}{C_{ox}} + z^2$

Now, this is a cubic equation in z. This can be solved by using Cardan's method but it made the problem very complex. Moreover, by calculation, the term $4\beta t_{fe}\gamma^3$ is found out to be very small. So, this cubic term is neglected.

The equation now becomes

$V_{GB} = V_{FB} + 2\alpha t_{fe}\gamma z + \frac{\gamma z}{C_{ox}} + z^2$

or, $V_{GB} = V_{FB} + Az + z^2$

where $A = 2\alpha t_{fe}\gamma + \frac{\gamma}{C_{ox}}$

or, $z^2 + Az + B = 0$

where $B = V_{FB} - V_G$

Solving this equation using Sreedharacharya's rule and including only the positive term, we get

$z = \frac{-A+\sqrt{A^2-4B}}{2A}$ ..(10)

Squaring z, we get the expression for surface potential Ψ_S.

Now, the expression for threshold voltage can be written as follows:

$V_T = V_{FB} + 2\alpha t_{fe}(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}} + 4\beta t_{fe}(2qN_a\varepsilon_s(2\phi_F))^{\frac{3}{2}} + \frac{(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}}}{C_{ox}} + 2\phi_F$ ..(11)

After extensive simulations, it is found that if we neglect the cubic term, this does not hamper the value of threshold voltage for a considerable range of doping.

So $V_T = V_{FB} + 2\alpha t_{fe}(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}} + \frac{(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}}}{C_{ox}} + 2\phi_F$ ..(12)

Development of Subthreshold Swing model

Now we calculate the subthreshold swing of this structure.

$V_G = V_{FB} + 2\alpha t_{fe}(2qN_a\varepsilon_s\Psi_S)^{\frac{1}{2}} + 4\beta t_{fe}(2qN_a\varepsilon_s\Psi_S)^{\frac{3}{2}} + \frac{(2qN_a\varepsilon_s\Psi_S)^{\frac{1}{2}}}{C_{ox}} + \Psi_S$

Differentiating V_{GB} with respect to Ψ_S, we get

$\frac{dV_G}{d\Psi_S} = 1 + (\frac{(2qN_a\varepsilon_s)^{\frac{1}{2}}}{\Psi_S^{\frac{1}{2}}})(\alpha t_{fe} + \frac{1}{2C_{ox}}) + 6\beta t_{fe}(2qN_a\varepsilon_s)^{\frac{3}{2}}\Psi_S^{\frac{1}{2}}$

Subthreshold swing = $2.3V_{th}(dV_{GB}/d\Psi_S)$

Which is lesser than 60 millivolt per decade.

But this expression does not give a good result.

So a new expression for subthreshold swing has been adopted in the literature[14]. It is given as:

Subthreshold swing = $2.3V_{th}$(Subthreshold Swing of Normal MOSFET)$(1-|\frac{C_{ox}}{C_{FE}}|)^{-1}$ (13)

Where Subthreshold swing of normal MOSFET is given as $\frac{1}{2C_{ox}}(\frac{2qN_a\varepsilon_s}{\Psi_S^1})^{\frac{1}{2}} + 1$ and

C_{FE} is given as $\frac{1}{2\alpha t_{fe} + 12\beta t_{fe}Q^2}$ where Q is given by …(7).

Development of expressions of Landau Coefficients

The negative capacitance principle can be explained by Landau-Devonshire theory which states that the total energy in a ferroelectric is given as $U = \alpha P^2 + \beta P^4$ where α and β are anisotropic constants and P is the polarization inside the ferroelectric. This can also be shown from the S-curve of ferroelectrics.

When there is some potential difference across the ferroelectric, there is some energy stored inside the ferroelectric due to the voltage.

The free energy inside the ferroelectric is given as:

$F = \alpha P^2 + \beta P^4 - PE$

where P is the polarization and E is the electric field across the ferroelectric.

Now, it is known that the free energy change with respect to charge is given as

$$\frac{dF}{dP} = -\rho\frac{dP}{dt} \quad (14)$$

where ρ is the frictional inertia of the system, P is the polarization, F is the free energy and t is the time.

Differentiating the expression for F with respect to P, we get

$\frac{dF}{dP} = 2\alpha P + 4\beta P^3 - E$

or, $-\rho\frac{dP}{dt} = 2\alpha P + 4\beta P^3 - E$

or, $E = 2\alpha P + 4\beta P^3 + \rho\frac{dP}{dt}$

Under steady state $\rho\frac{dP}{dt}$ is 0.

So, $E = 2\alpha P + 4\beta P^3$

When E = 0,

$P_R = \sqrt{\frac{-\alpha}{2\beta}}$ or $-\sqrt{\frac{-\alpha}{2\beta}}$ or 0.

Here $\sqrt{\frac{-\alpha}{2\beta}}$ is the remnant polarization.

Differentiating the equation of E with respect to P, we get

$\frac{dE}{dP} = 2\alpha + 12\beta P^2$

Now, from the hysteretic curve and the S-curve it is found that when $\frac{dE}{dP}$ is equal to 0, the value of E is approximately equal to the coercive electric field E_C. Conceptually when the electric field is equal to the coercive electric field, the polarization inside the material is 0. But here in this S-curve, the value of polarization is not equal to zero when $\frac{dE}{dP}$ is 0. So since the value of electric field at that point is approximately equal to the coercive electric field, we can call this polarization coercive polarization denoted as P_C.

So $2\alpha + 12\beta P_C^2 = 0$

or, $P_C = \sqrt{\frac{-\alpha}{6\beta}}$ or $-\alpha 6\beta$

Now, in the equation for steady state electric field verses polarization,

$E = 2\alpha P + 4\beta P^3$

or, $-E_C = 2\alpha P_C + 4\beta P_C^3$

Here E_C is greater than 0. We need negative E_C to make the positive remnant charge 0 and vice-versa. So, when E_C is positive P_C is negative and vice versa,

So, $-E_C = 2\alpha P_C + 4\beta P_C^3$

or, $-E_C = 2\alpha \sqrt{\frac{-\alpha}{6\beta}} - 4\beta(\sqrt{\frac{-\alpha}{6\beta}})^3$

or, $-E_C = 2\alpha \sqrt{\frac{-\alpha}{6\beta}} - \frac{2}{3}\alpha \sqrt{\frac{-\alpha}{6\beta}}$

or, $-E_C = \frac{4}{3}\alpha \sqrt{\frac{-\alpha}{6\beta}}$

or, $-E_C = \frac{4}{3\sqrt{3}}\alpha \sqrt{\frac{-\alpha}{2\beta}}$

or, $-E_C = \frac{4}{3\sqrt{3}}\alpha P_R$

or, $\alpha = -\frac{3\sqrt{3}}{4}\frac{E_C}{P_R}$

Now, $P_R = \sqrt{\frac{-\alpha}{2\beta}}$

or, $P_R = \sqrt{\frac{\frac{3\sqrt{3}}{4}\frac{E_C}{P_R}}{2\beta}}$

or, $P_R^2 = \frac{3\sqrt{3}}{8\beta}\frac{E_C}{P_R}$

or, $\beta = \frac{3\sqrt{3}}{8}\frac{E_C}{P_R^3}$

So the expressions for anisotropy constants α and β are derived.

This negative capacitance mechanism of a ferroelectric is utilized in our work as an insulator in MOSFETs for the amplification of the surface potential of MOSFETs which helps to reduce the subthreshold swing below the Boltzmann limit.

CHAPTER 4

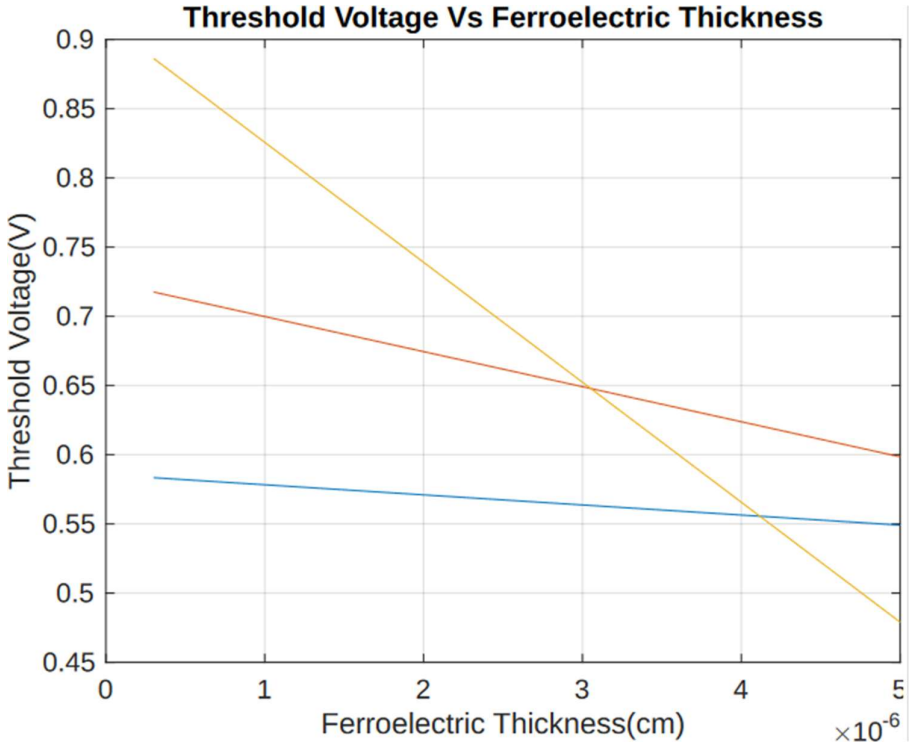
RESULTS

Threshold Voltage Vs Ferroelectric Thickness at different doping levels

Here we vary the ferroelectric thickness keeping other parameters constant and plot the threshold voltage with respect to ferroelectric thickness.

Table 2. List of constant and variable parameters

Sl No.	Parameter	Value
1.	Ferroelectric Thickness(nm)	3 to 50
2.	Doping concentration(cm^3)	10^{15},10^{16},10^{17}
3.	Coercive Field(MV/cm)	1.45
4.	Remnant Polarization($\mu C/cm^2$)	7.15

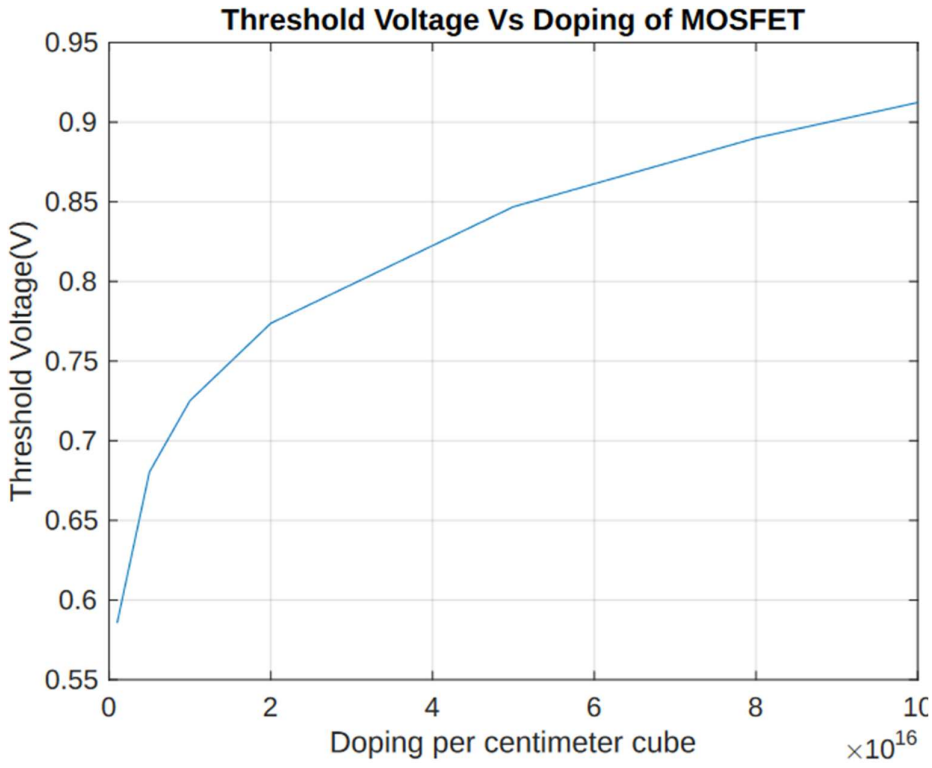


Graph 1. Plot of Threshold Voltage with varying ferroelectric thickness at different doping concentrations

Here we have plotted three graphs with different doping concentrations and assumed flat-band approximation.

1. **The blue graph indicates doping concentration 10^{15} cm^{-3}.**
2. **The orange graph indicates doping concentration 10^{16} cm^{-3}.**
3. **The yellow graph indicates doping concentration 10^{17} cm^{-3}.**

Here we observe that for all the curves the threshold voltage decreases with increase in ferroelectric thickness for a fixed doping concentration. For classical MOSFETs without ferroelectric, the threshold voltage increases according to the relation that at threshold voltage, the voltage drop along the semiconductor vertically is the difference between the intrinsic Fermi potential and Fermi potential multiplied by 2. The difference between the Fermi potential and intrinsic Fermi potential increases with doping concentration. So more voltage drop occurs for higher doping. Here we observe that for low ferroelectric thicknesses, the threshold voltage increases with doping, following classical MOSFETs. But as the thickness of ferroelectric increases, the threshold voltage decreases because the ferroelectric's effect increases with increase in thickness. We see that as the doping is increased, the decrease of threshold voltage with respect to ferroelectric thickness is more severe. We see that the threshold voltage for a MOSFET with ferroelectric of thickness 50 nm is much less for doping concentration of 10^{17} per centimetre cube than 10^{15} or 10^{16} per centimetre cube which is even less than the surface potential at threshold of 10^{17} per centimetre cube. This shows that a thick ferroelectric internally amplifies the voltage so that the surface potential of that high value is reached with very low threshold voltage. We have also done it at flat-band approximation because if we considered it, then the threshold voltage might would become negative for high ferroelectric thicknesses and it should become impossible for use in logic circuits. This flat-band approximation has an advantage that it gives the threshold voltage of the MOSFET ideally so that now we can select the gate metal so that the device gets properly adjusted in our circuit.



Graph 2 showing the variation of threshold voltage with respect to doping of a normal MOSFET

Threshold Voltage Vs Doping with and without β

With β, the expression for threshold voltage is

$$V_T = V_{FB} + 2\alpha t_{fe}(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}} + 4\beta t_{fe}(2qN_a\varepsilon_s(2\phi_F))^{\frac{3}{2}} + \frac{(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}}}{C_{ox}} + 2\phi_F$$

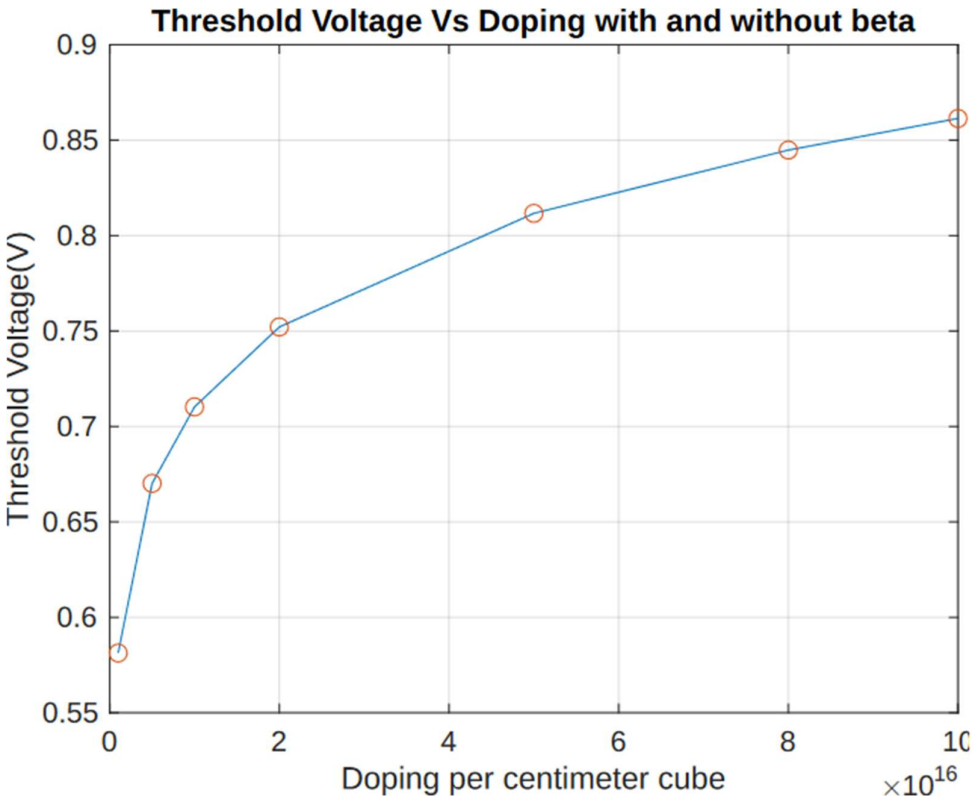
and without β, its expression is

$$V_T = V_{FB} + 2\alpha t_{fe}(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}} + \frac{(2qN_a\varepsilon_s(2\phi_F))^{\frac{1}{2}}}{C_{ox}} + 2\phi_F$$

Both these equations are plotted using the below given parameters and others mentioned in Chapter 2.

Table 3. List of constant and variable parameters

Sl No.	Parameter	Value
1.	Ferroelectric Thickness(nm)	20
2.	Doping concentration(cm^3)	10^{15}, $5X10^{15}$,10^{16} ,$2X10^{16}$ $5X10^{16}$, $8X10^{16}$, 10^{17}
3.	Coercive Field(MV/cm)	0.93
4.	Remnant Polarization($\mu C/cm^2$)	15.6



Graph 3 Showing the variation of threshold voltage with and without beta term of a ferroelectric

Here we have plotted the threshold voltage term with and without beta term by varying doping concentration and assuming flat-band approximation.

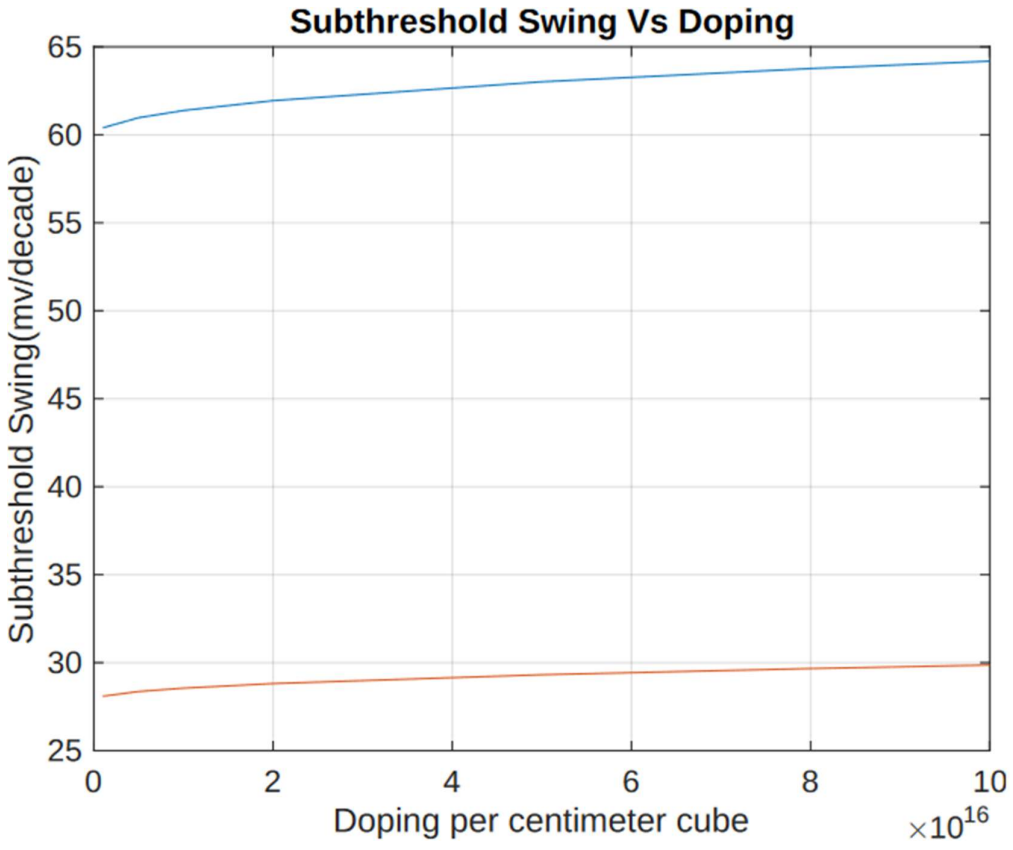
1. **The continuous line is without β term.**
2. **The circles show the variation of threshold voltage of NCFET with beta term.**

From the graph we see that if we include or replace beta term from the expression of threshold voltage, it makes no difference.

Subthreshold Swing Vs Doping of both normal and MFIS FET

Table 4. List of constant and variable parameters

Sl No.	Parameter	Value
1.	Ferroelectric Thickness(nm)	20
2.	Doping concentration(cm^3)	10^{15}, $5X10^{15}$,10^{16} ,$2X10^{16}$ $5X10^{16}$, $8X10^{16}$, 10^{17}
3.	Coercive Field(MV/cm)	0.93
4.	Remnant Polarization($\mu C/cm^2$)	15.6



Graph 4 showing the variation of subthreshold swing with respect to doping of both normal and MFIS FET

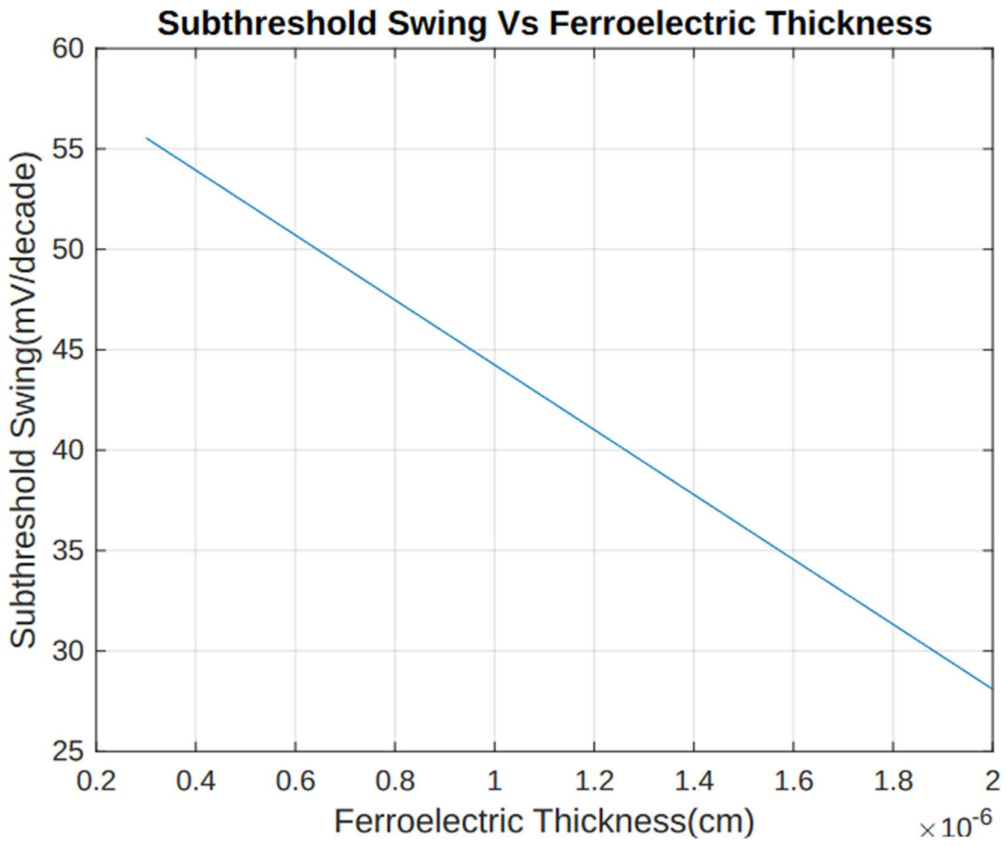
1. **The blue curve shows the variation of subthreshold swing with respect to doping of a normal MOSFET.**
2. **The orange curve shows the variation of subthreshold swing with respect to doping of MFIS FET.**

From the graph it is seen that the subthreshold swing of the device increases with doping for both normal and MFIS FETs. MFIS FETs have a much lower subthreshold swing compared to normal MOSFETs which makes them useful for low power VLSI circuits.

Subthreshold Swing Vs Ferroelectric Thickness

Table 5. List of constant and variable parameters

Sl No.	Parameter	Value
1.	Ferroelectric Thickness(nm)	3 to 20
2.	Doping concentration(cm^3)	10^{15}
3.	Coercive Field(MV/cm)	0.93
4.	Remnant Polarization($\mu C/cm^2$)	15.6



Graph 5 shows the variation of subthreshold swing with respect to ferroelectric thickness with constant doping

This graph shows that the subthreshold swing decreases with increase in ferroelectric thickness because ferroelectric effect increases with thickness. But ferroelectric parameters like coercive field, remnant polarization and thickness are non-scalable parameters. They depend on each other.

CHAPTER 5

REFERENCES

1. Ben G.Streetman, Sanjay Kumar Banerjee, Solid State Electronic Devices, 6th Edition Printice Hall India Publication, Chapter 5, pp.5.2.1
2. Ben G.Streetman, Sanjay Kumar Banerjee, Solid State Electronic Devices, 6th Edition Printice Hall India Publication, Chapter 6, pp.6.4.2
3. Comprehensive Physics Class XII Volume 1, Laxmi Publications, Chapter 4, pp.4.19
4. Operation and modelling of the MOS Transistor by Yannis Tsividis and Colin McAndrew, Third Edition, Oxford University Press, Chapter 2, pp,2.4.4
5. Compact Model for Ferroelectric Negative Capacitance Transistor with MFIS structure by Girish Pahwa, Tapas Dutta, Amit Agarwal and Yogesh Singh Chauhan, IEEE Transactions on Electron Devices, Vol 64, No. 3, March 2017
6. A New Surface Potential-Based Analytical Model for MFIS NCFETs by Anuj Pahariya and Aloke K. Dutta, IEEE Transactions on Electron Devices, Vol 69, No 2. February 2022
7. Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices by Sayeef Salahuddin and Supriyo Dutta Nano Letters 2008, Vol. 8, No. 2 405-410
8. Negative Capacitance Behavior in a Leaky Ferroelectric by Asif Islam Khan, Ujwal Radhakrishna, Korok Chatterjee, Sayeef Salahuddin and Dimitri A. Antoniadis, IEEE Transactions on Electron Devices, Vol. 63, No. 11, November 2016
9. Electronics Fundamentals and Applications 12th Edition by D. Chattopadhyay and P. C. Rakshit, New Age International Private Limited Publishers, pp.5.5
10. Microelectronic Circuits Theory and Applications 7th Edition by Adel. S. Sedra and Kenneth C. Smith by Oxford
11. CMOS Digital Integrated Circuits Analysis and Design by Sung-Mo Kang and Yusuf Leblebici, 2nd Edition, McGraw-Hill publishers
12. Semiconductor Physics and Devices, 3rd Edition by Donald A. Neaman by Tata McGraw-Hill
13. Fundamentals of Modern VLSI Devices, 2nd Edition, Yuan Taur and Tak H. Ning, Cambridge University Press
14. Short-Channel Effects in 2D Negative-Capacitance Field-Effect Transistors by Wei-Xiang You, Chih-Peng Tsai and Pin Su IEEE Transactions on Electron Devices, Vol. 65, No. 4, April 2018