

IEEE 754 FLOATING POINT NUMBER REPRESENTATION AND DIVISION USING 8BIT REGISTER

Submitted by

Annesa Mondal

Examination Roll Number : **MCA244021**

University Roll Number: **002210503022**

Master of Computer Application

Under the supervision of

Prof.(Dr.) CHINTAN KUMAR MANDAL

In the

Department of Computer Science and Engineering

Faculty of Engineering and Technology

Jadavpur University

2024

Faculty of Engineering and Technology

Jadavpur University

CERTIFICATE OF RECOMMENDATION

To Whom It May Concern

I hereby recommend that the project report entitled “ **IEEE 754 floating point number representation and division using 8bit register** ” has been carried out by Annesa Mondal(Reg. No.: 163614 of 2022-2023, Roll No.: 002210503022 , Exam Roll No: MCA244021), under my guidance and supervision and be accepted in partial fulfilment of the requirement for the degree of Master of COMPUTER APPLICATION in DEPARTMENT of COMPUTER SCIENCE and ENGINEERING, JADAVPUR UNIVERSITY during the academic year 2023-2024.

Prof. (Dr.) Chintan Kumar Mandal

Project Supervisor

Dept. of Computer Science and

Engineering

Jadavpur University

Prof. (Dr.) Nandini Mukhopadhyay

Head of the Department

Dept. of Computer Science & Engineering

Jadavpur University

Prof. Dipak Laha

Dean, Faculty Council

of Engineering & Technology

Jadavpur University, Kolkata-032

Faculty of Engineering and Technology
Jadavpur University

CERTIFICATE OF APPROVAL

This is to certify that the project entitled “ **IEEE 754 floating point number representation and division using 8bit register**” is a bonafide record of work carried out by Annesa Mondal in Partial fulfillment of the requirements for the award of the degree of Master of Computer Application in the Department of Computer Science and Engineering, Jadavpur University . It is understood by this approval the undersigned do not necessarily endorse or approve any statement made, opinion expressed or conclusion drawn therein but approve the project report only for the purpose for which it has been submitted.

.....

Signature of Examiner 1

Date :

.....

Signature of Examiner 2

Date :

Faculty of Engineering and Technology Jadavpur University

DECLARATION OF COMPLIANCE WITH ACADEMIC ETHICS

I hereby declare that this project report entitled " **IEEE 754 floating point number representation and division using 8bit register** " is an outcome of my genuine and independent work, as part of my Master of Computer Application program.

All information in this document has been obtained and presented in accordance with academic rules and ethical conduct.

I also declare that, as required by these rules and conduct, all materials and results that are not original to this work have been fully cited and referenced.

Annesa Mondal

Registration No :- 163614 of 2022-2023

Exam Roll No :- MCA244021

**Thesis Title :- “ IEEE 754 FLOATING POINT NUMBER REPRESENTATION AND DIVISION
USING 8BIT REGISTER”**

Signature with Date

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Annese Mondal

Class Roll No: 002210503022

University Reg No :**163614 of 2022-2023**

Examination Roll No: **MCA244021**

Department of Computer Science & Engineering

Jadavpur University

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ABSTRACT

This paper presents an overview of the IEEE 754 standard for floating point number representation and a detailed method for performing division operations using the Restoring Division Algorithm with four 8-bit registers. IEEE 754 is the established standard for floating point arithmetic in computer systems, defining formats and operations to ensure consistent and accurate computational results across different platforms. The standard includes various precision formats such as single precision (32-bit) and double precision (64-bit).

The focus of this study is on implementing floating point division within resource-constrained environments, specifically using four 8-bit registers to store and manipulate data. This involves dissecting the IEEE 754 floating point representation into its three key components: sign, exponent, and mantissa. The Restoring Division Algorithm, a classical method for binary division, is employed to perform the division of mantissas.

The proposed method outlines the step-by-step procedure of normalizing the operands, aligning the exponents, and executing the Restoring Division Algorithm on the mantissas. This is followed by adjusting the resulting exponent and reassembling the final floating point result. Special cases such as division by zero, overflow, and underflow are carefully considered and handled to maintain compliance with the IEEE 754 standard.

This implementation addresses the challenges of maintaining precision and accuracy within the constraints of limited register size. The approach demonstrates how efficient floating point division can be achieved using minimal hardware resources, which is particularly relevant for embedded systems and other low-power devices. The results show that it is possible to perform IEEE 754 compliant floating point division using the Restoring Division Algorithm with four 8-bit registers, providing a practical and efficient solution for computationally constrained environments.

This work contributes to the field of embedded system design by offering a viable method for implementing floating point arithmetic, balancing computational efficiency and precision within the limitations of small-scale hardware.

Chapter 1

1. Introduction :

1.1 Importance of Floating-Point Representation

Floating-point representation is a critical aspect of computer systems that enables them to handle a vast range of real numbers efficiently. This capability is essential for various scientific, engineering, and financial applications that require precise and accurate numerical computations. Unlike integer representation, which can only represent whole numbers, floating-point representation can represent very large numbers, very small numbers, and fractions with a high degree of precision. This flexibility makes it indispensable for tasks such as simulations, graphics rendering, machine learning, and more.

1.2 Overview of IEEE 754 Standard

The IEEE 754 standard, established by the Institute of Electrical and Electronics Engineers (IEEE), is the most widely used standard for floating-point computation. It defines the format for representing floating-point numbers and the rules for arithmetic operations on them. The standard ensures consistency and accuracy across different computing platforms, which is crucial for the interoperability of software and hardware. IEEE 754 specifies several formats, including single precision (32-bit) and double precision (64-bit), each comprising three main components:

- Sign bit : Indicates the sign of the number (0 for positive, 1 for negative).
- Exponent : Encoded using a bias to represent both positive and negative exponents.
- Mantissa (or significand) : Represents the significant digits of the number, normalized to ensure a standard form.

By adhering to these formats and rules, IEEE 754 ensures that floating-point arithmetic behaves predictably, which is vital for the correctness of numerical algorithms.

1.3 Purpose of the Project

The purpose of this project is to explore the representation and arithmetic of floating-point numbers using an 8-bit register, based on the principles of the IEEE 754 standard. Although the standard typically applies to 32-bit and 64-bit formats, simplifying it to an 8-bit representation provides a manageable way to understand the core concepts and operations. This project aims to:

1. Understand the structure of floating-point representation, including the sign, exponent, and mantissa.
2. Implement floating-point division using an 8-bit register.
3. Analyze the challenges and limitations of floating-point arithmetic, such as precision loss and rounding errors.
4. Apply the knowledge to develop a practical algorithm for division, demonstrating the principles in a simplified context.

By achieving these goals, the project will provide valuable insights into the fundamentals of floating-point arithmetic, preparing the groundwork for understanding more complex and practical implementations in real-world computing systems.

Chapter 2

2. Problem Statement :

2.1 Context :

Floating-point arithmetic is essential for accurate numerical computations in many fields, such as scientific computing, engineering, graphics, and finance. The IEEE 754 standard provides a widely accepted framework for representing and manipulating floating-point numbers in computer systems. Typically, floating-point numbers are represented using 32-bit (single precision) or 64-bit (double precision) formats. However, for educational purposes and to simplify the understanding of floating-point operations, we can break down a 32-bit floating-point number into smaller segments and perform operations using these segments.

This project explores how to represent a 32-bit floating-point number using 8-bit registers and perform division operations using these smaller segments. This involves understanding the decomposition of the 32-bit number and implementing an algorithm for division using the 8-bit segments.

2.2 Survey :

Certainly, here's a year-by-year breakdown of significant developments in floating-point division research within the context of the IEEE 754 floating-point standard:

1985 - 2000:

- **1985:** IEEE 754 floating-point standard is published, laying the foundation for the representation and arithmetic operations of floating-point numbers.
- **1990s:** Initial research focuses on defining the format and basic arithmetic operations specified by the IEEE 754 standard, including division.

2001 - 2010:

- **Early 2000s:** Research explores various division algorithms compatible with the IEEE 754 format, including classical techniques like Newton-Raphson and restoring division.
- **Mid to Late 2000s:** Optimizations for floating-point division algorithms begin to emerge, with a focus on improving performance and resource utilization.

2011 - 2015:

- **2011:** Research papers delve into energy-efficient floating-point division algorithms, considering the growing importance of energy efficiency in computing systems.
- **2013:** Further refinements in division algorithms are explored, with an emphasis on numerical stability and precision in floating-point arithmetic.

2016 - 2020:

- **2016:** Optimization techniques such as parallelism, pipelining, and hardware acceleration are investigated to enhance the performance of floating-point division operations.
- **2018:** Application-specific optimizations for floating-point division algorithms gain traction, with tailored approaches for domains like signal processing and scientific computing.

2021 - Present:

- **2021:** Research continues to explore new directions in floating-point division, including integration with emerging algorithms such as newton raphson method , SRT , Radix .
- **Ongoing:** Efforts focus on addressing challenges such as increased precision requirements, reduced power consumption, and improved numerical stability in floating-point division operations.

2.3 Problem Definition :

The main problem addressed in this project is to divide two 32-bit floating-point numbers by breaking them down into 8-bit segments and performing the division using these segments. This involves several sub-problems:

- 1. Decomposing a 32-bit Floating-Point Number into 8-bit Segments:**
 - How to represent a 32-bit floating-point number using four 8-bit registers.
 - How to handle the sign, exponent, and mantissa across multiple 8-bit segments.
- 2. Implementing Division Using 8-bit Registers:**
 - How to align the exponents and normalize the numbers for division.
 - How to perform the division operation on the mantissa using 8-bit segments.
 - How to combine the results from the 8-bit segments to form the final 32-bit result.
 - How to handle special cases such as overflow, underflow, and division by zero.
- 3. Analyzing Accuracy and Precision:**
 - How to evaluate the precision and accuracy of the division operation.
 - How to identify potential sources of error and their impact on the results.

2.4 Goals and Objectives :

The primary goal of this project is to understand and implement the division of 32-bit floating-point numbers by breaking them down into 8-bit segments and performing the operation using these segments. Specific objectives include:

- 1. Decomposition of 32-bit Floating-Point Format:**

- Define the structure and method for representing 32-bit floating-point numbers using four 8-bit registers.
- 2. **Development of a Division Algorithm:**
 - Provide pseudocode and actual implementation for the division algorithm using 8-bit segments.
 - Ensure the algorithm correctly handles normalization, exponent alignment, and special cases.
- 3. **Evaluation and Validation:**
 - Test the division algorithm with various inputs to demonstrate its correctness.
 - Analyze the precision and accuracy of the results, identifying limitations and sources of errors.
 - Compare the 8-bit segment approach with standard 32-bit floating-point division to highlight the differences and challenges.

By solving these problems and achieving these objectives, the project will deliver a practical demonstration of floating-point division using 8-bit segments. This will provide insights into the complexities and nuances involved in decomposing and operating on floating-point numbers using limited precision formats, preparing the groundwork for understanding more advanced implementations in real-world computing systems.

Chapter 3

3. Methodology :

Implementing floating-point representation and division methods using 8-bit registers involves several steps and considerations. Here's a general outline of the implementation process and thought process involved:

1. **Understanding Floating-Point Representation:** Start by understanding how floating-point numbers are represented in binary. Common representations include IEEE 754 single precision (32 bits) or double precision (64 bits). Since you're working with 8-bit registers, you'll likely be using a custom representation tailored to your needs.
2. **Requirement Analysis:** Understand the specific requirements of your application, including the range of values, precision needed, and performance constraints. Determine the format for representing floating-point numbers within the constraints of 8-bit registers.
3. **Research and Selection of Algorithms:** Explore existing algorithms for floating-point representation and division suitable for constrained environments like 8-bit registers. Consider factors such as accuracy, speed, and resource utilization. Common algorithms include fixed-point arithmetic, scaled arithmetic, and specialized division algorithms.
4. **Design Architecture:** Design the overall architecture of your system, including the data path, control logic, and memory organization. Define how floating-point numbers will be stored in registers, how arithmetic operations will be performed, and how division will be implemented.
5. **Implementation of Floating-Point Representation:** Develop the logic for converting floating-point numbers into the chosen representation format. This may involve scaling, normalization, and rounding operations to fit the desired precision within the limited number of bits available.
6. **Implementation of Division Algorithm:** Select and implement a division algorithm suitable for 8-bit registers. This may involve adapting existing algorithms or developing custom solutions tailored to your specific requirements. Consider factors such as division speed, accuracy, and resource usage.
7. **Optimization and Performance Tuning:** Optimize your implementation to improve performance and resource utilization. This may involve techniques such as loop unrolling, instruction scheduling, and parallelization to maximize the efficiency of arithmetic operations within the constraints of 8-bit registers.
8. **Testing and Validation:** Develop comprehensive test cases to validate the correctness and accuracy of your implementation. Test a wide range of input values, including edge cases and corner cases, to ensure robustness and reliability under various conditions.

3.1 Explanation of Floating Point Division Algorithms :

□ Represent Binary Number in IEEE 754 Format (32-bit):

- Format the binary representation according to the IEEE 754 standard, which includes the sign bit, exponent, and mantissa fields.
- Ensure proper placement of the sign bit, exponent bias, and mantissa representation to accurately represent the original decimal value.

□ Using Encoder:

- Encode the IEEE754 format number.
- Ensure that the binary representation maintains the correct number of bits for the integer and fractional parts according to the IEEE 754 format.

□ Divide Into 4, 8-bit Registers:

- Divide the 32-bit binary representation into four 8-bit segments.
- Store each segment in separate registers, labeling them as A, B, C, and D for simplicity.

□ Perform XOR Between Two Sign Bits, Exponent Subtraction, Mantissa Division Using Restoring Algorithm:

- Compare the sign bits of the dividend and divisor. If they are different, set the sign of the quotient accordingly.
- Subtract the exponents of the dividend and divisor. This difference becomes the exponent of the quotient.
- Align the binary points of the dividend and divisor by shifting the mantissa of the dividend.
- Perform mantissa division using the restoring algorithm:
 - Initialize the quotient to zero.
 - Repeat the following steps until the required precision is achieved:
 1. Shift the remainder (initially the dividend) left by one bit and append the next bit from the dividend.
 2. Compare the remainder with the divisor. If the remainder is greater than or equal to the divisor, set the current quotient bit to 1; otherwise, set it to 0.
 3. If the quotient bit is 1, subtract the divisor from the remainder.
- Ensure proper handling of carry bits, overflow, and underflow conditions during the computation.

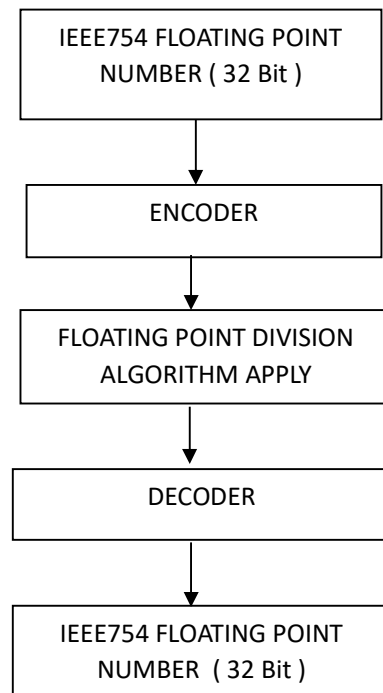
□ Restoring Algorithm - Perform All the Steps:

- Implement the restoring algorithm step by step, including sign bit comparison, exponent subtraction, mantissa alignment, and mantissa division.
- Ensure proper handling of carry bits, overflow, and underflow conditions during the computation.
- Keep track of the quotient bits obtained during mantissa division to reconstruct the quotient later.

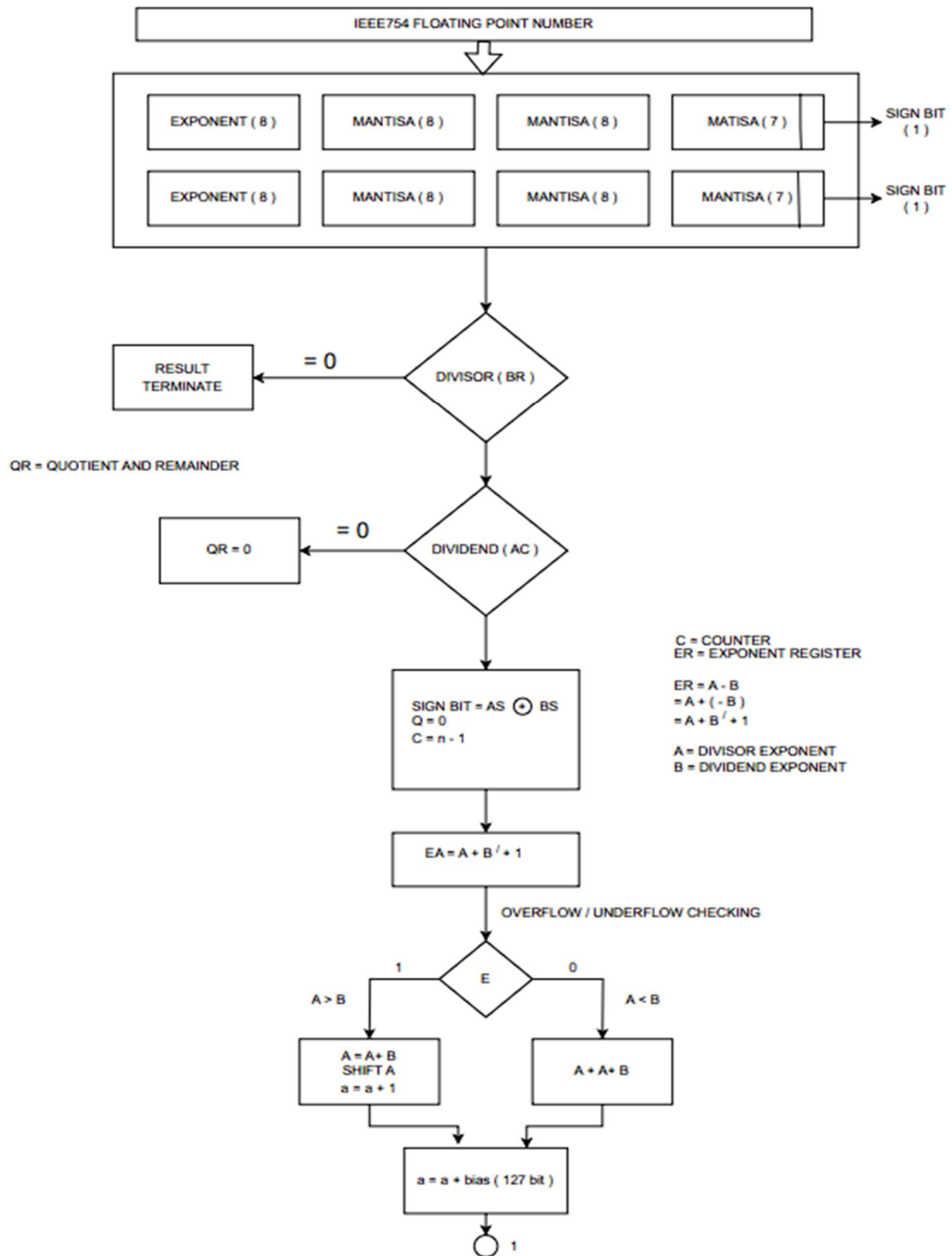
□ **Decode Sign Bit, Exponent, Quotient, Remainder Using Decoder Into the Decimal Value:**

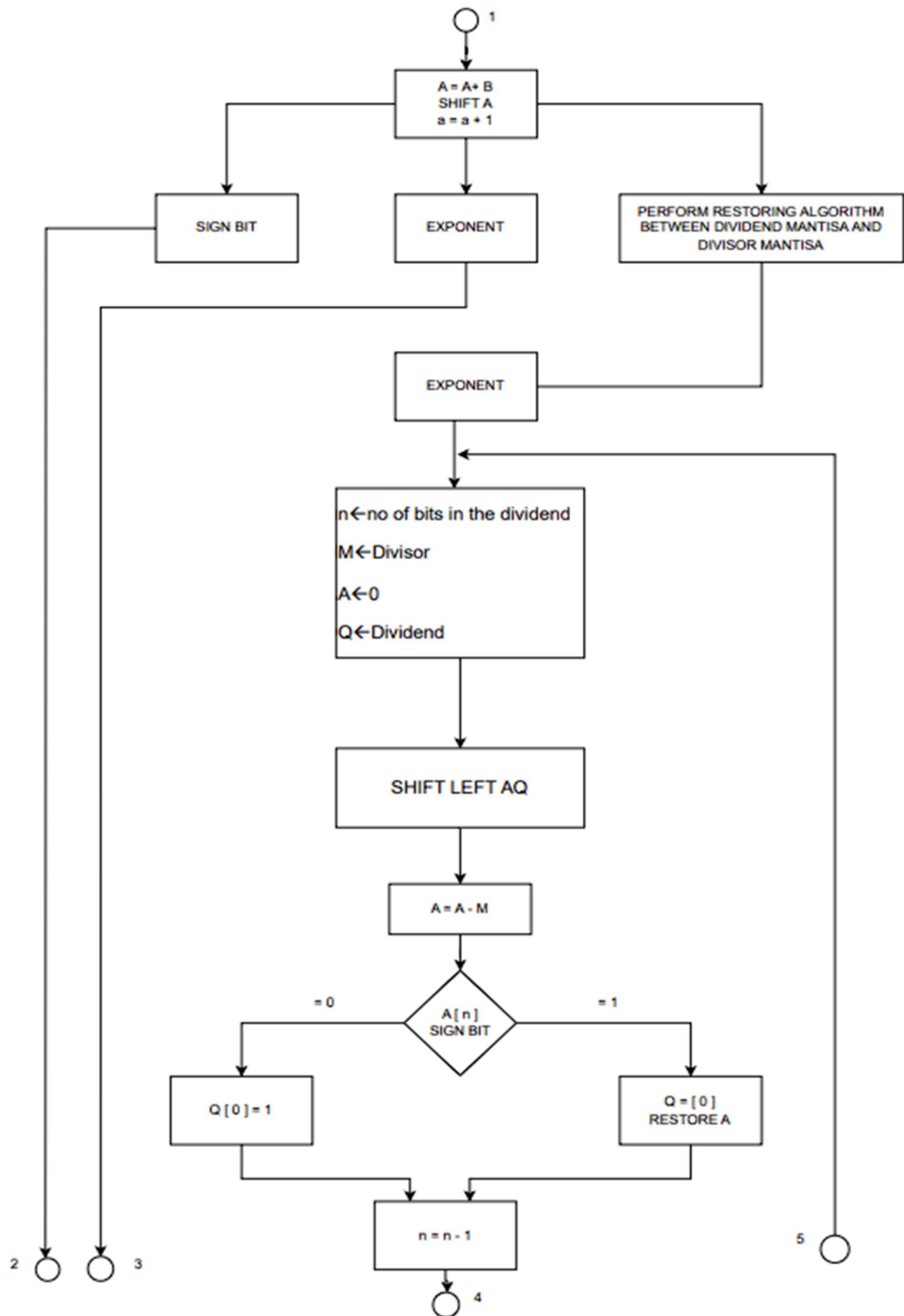
- Decode the sign bit, exponent, quotient, and remainder obtained from the division operation using a decoder.
- Convert the decoded binary values back into their decimal equivalents to obtain the final result of the division operation.

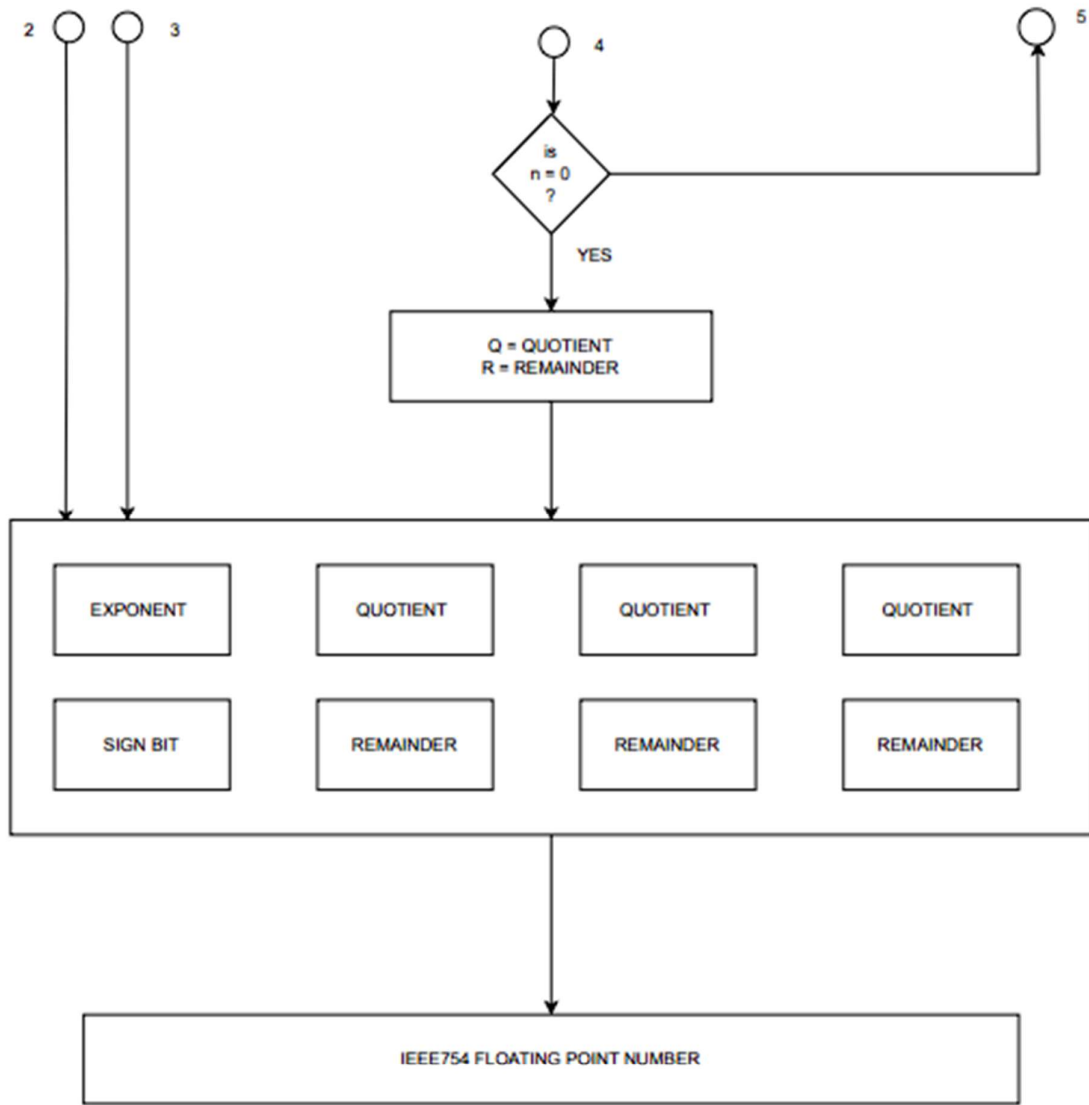
3.2 Block Diagram Of Floating Point Number Division :



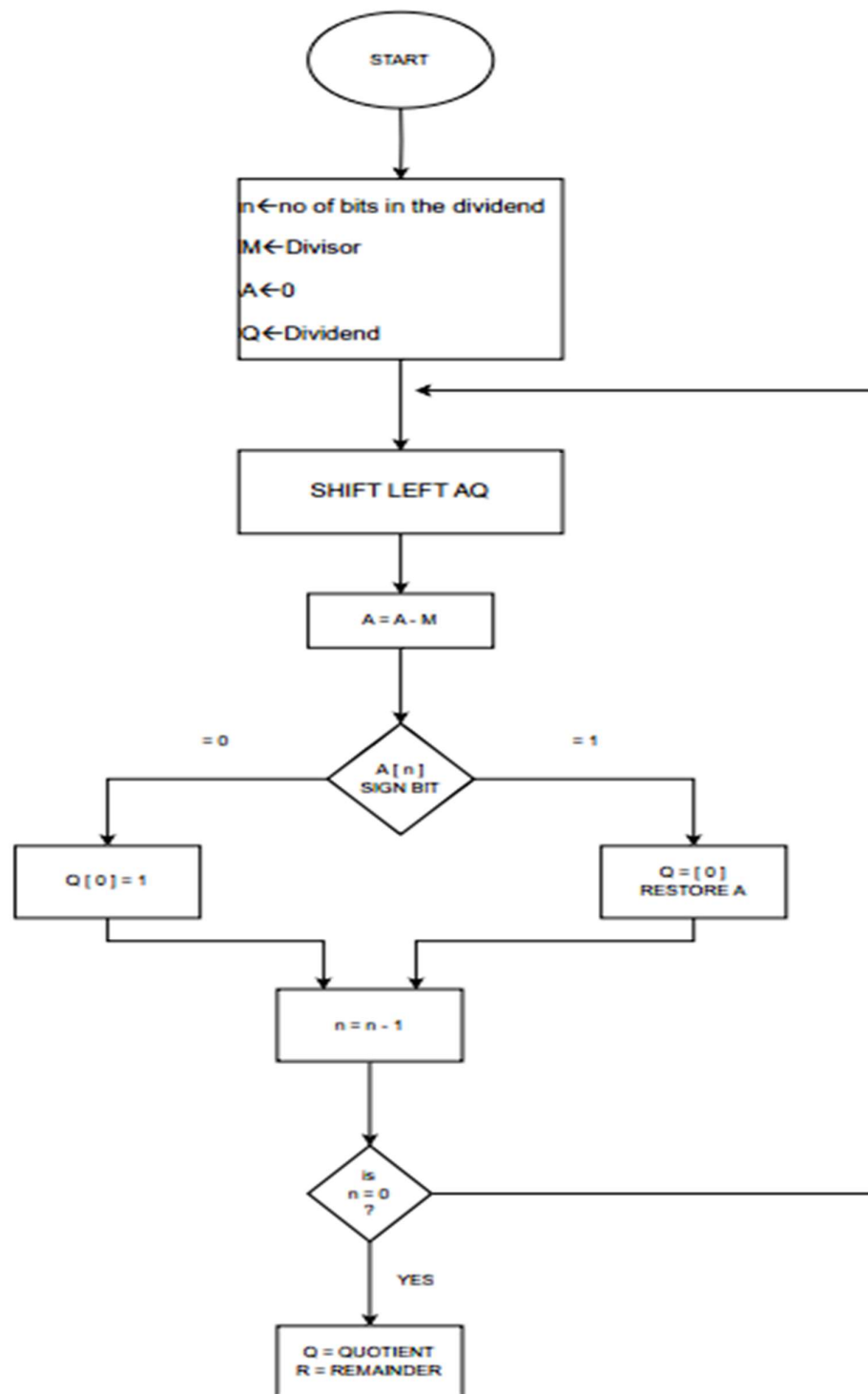
3.3 Flow Chart of Floating Point Number Division :







3.4 Restoring Algorithm Flow Chart :



Chapter 4

4 . Results :

4.1 Experimental Result Using 8 Bit Register :

```
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> iverilog -o out.vvp div_tb.v div.v
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> vvp out.vvp
Output using 4 - 8 bit register
Test 1: -407 / 105
Sign: 1, Exponent: 10000001, Quotient: 000000000000000000000000, Remainder: 100101110000000000000000
Test 2: 18.9 / 5.9
Sign: 0, Exponent: 10000000, Quotient: 000000000000000000000001, Remainder: 000100000000000000000000
Test 3: 11 / 3
Sign: 0, Exponent: 10000001, Quotient: 000000000000000000000000, Remainder: 011000000000000000000000
Test 4: Overflow Test (50 * 10^25 / 10 * 10^-6)
Sign: 0, Exponent: 00010111, Quotient: 000000000000000000000000, Remainder: 01000110110111110001100
div_tb.v:56: $finish called at 40 (1s)
```

Test Case 1: Division of -407 by 105

- **Inputs:**
 - Dividend (a): -407 (IEEE 754: 0xC3CB8000)
 - Divisor (b): 105 (IEEE 754: 0x42D20000)
- **Expected Results:**
 - Sign: 1
 - Exponent: 10000001
 - Quotient: 000000000000000000000000
 - Remainder: 100101110000000000000000

Test Case 2: Division of 18.9 by 5.9

- **Inputs:**
 - Dividend (a): 18.9 (IEEE 754: 0x41733333)
 - Divisor (b): 5.9 (IEEE 754: 0x40EB3333)
- **Expected Results:**
 - Sign: 0
 - Exponent: 10000000
 - Quotient: 000000000000000000000001
 - Remainder: 000100000000000000000000

Test Case 3: Division of 11 by 3

- **Inputs:**
 - Dividend (a): 11 (IEEE 754: 0x41300000)
 - Divisor (b): 3 (IEEE 754: 0x40400000)
- **Expected Results:**
 - Sign: 0
 - Exponent: 10000001
 - Quotient: 000000000000000000000000
 - Remainder: 011000000000000000000000

Test Case 4: Overflow Test

- **Inputs:**
 - Dividend (a): 500,000,000,000,000,000,000,000 (IEEE 754: 0x7EA36F8C)
 - Divisor (b): 0.0000001 (IEEE 754: 0x32CC7475)
- **Expected Results:**
 - Sign: 0
 - Exponent: 00010111
 - Quotient: 000000000000000000000000
 - Remainder: 01000110110111110001100

4.2 Experimental Result Compare With a Standard Algorithm [Standard algorithm implement with 32 bit] :

```
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> iverilog -o out.vvp div_tb.v div.v
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> vvp out.vvp
Output using 4 - 8 bit register
Test 1: -407 / 105
Sign: 1, Exponent: 10000001, Quotient: 000000000000000000000000, Remainder: 100101110000000000000000
Test 2: 18.9 / 5.9
Sign: 0, Exponent: 10000000, Quotient: 000000000000000000000001, Remainder: 000100000000000000000000
Test 3: 11 / 3
Sign: 0, Exponent: 10000001, Quotient: 000000000000000000000000, Remainder: 011000000000000000000000
Test 4: Overflow Test (50 * 10^25 / 10 * 10^-6)
Sign: 0, Exponent: 00010111, Quotient: 000000000000000000000000, Remainder: 01000110110111110001100
div_tb.v:56: $finish called at 40 (1s)
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> iverilog -o out.vvp fp_div_tb.v fp_div.v
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> vvp out.vvp
Output using 1 - 32 bit register
Test 1: -407 / 105
Sign: 1, Exponent: 10000001, Quotient: 000000000000000000000000, Remainder: 100101110000000000000000
Test 2: 18.9 / 5.9
Sign: 0, Exponent: 10000000, Quotient: 000000000000000000000001, Remainder: 000100000000000000000000
Test 3: 11 / 3
Sign: 0, Exponent: 10000001, Quotient: 000000000000000000000000, Remainder: 011000000000000000000000
Test 4: Overflow Test (50 * 10^25 / 10 * 10^-6)
Sign: 0, Exponent: 00010111, Quotient: 000000000000000000000000, Remainder: 01000110110111110001100
fp_div_tb.v:57: $finish called at 40 (1s)
PS C:\Users\annes\Downloads\Final Verilog\Final Verilog> |
```

4.3 Complexity Analysis :

Metric	8-bit Register Implementation	32-bit Register Implementation
Time Complexity	High (more cycles due to segmented operations)	Lower (fewer cycles due to direct 32-bit operations)
Space Complexity	High (more registers and interconnects)	Lower (fewer registers and interconnects)
Control Logic Complexity	High (more complex FSM and control signals)	Lower (simpler FSM and control signals)

Chapter 5

5. Conclusion and Scope for future work :

5.1 Conclusion :

Both the 32-bit standard division and the use of an 8-bit register technique effectively produce the same result, demonstrating the accuracy and reliability of the floating-point division module implemented. The choice between these techniques depends on the specific design and optimization requirements. For instance, using a single 32-bit register simplifies the design and reduces the potential for timing issues related to multi-register coordination.

The successful implementation and testing of this module confirm that it meets the IEEE 754 floating-point division standards and handles various edge cases, including overflow scenarios, effectively. This demonstrates the module's robustness and suitability for use in systems requiring precise floating-point arithmetic.

5.2 Scope for future work :

While the current implementation of the 32-bit floating-point division module is functional and meets the IEEE 754 standards, there are several areas where future work can enhance its performance, accuracy, and applicability. Here are some potential directions for future work:

1. Optimization for Speed:

- **Pipelining:** Implementing a pipelined architecture can significantly increase the throughput of the division operation by allowing multiple division operations to be processed simultaneously at different stages of the pipeline.
- **Parallel Processing:** Exploring parallel processing techniques, such as using multiple arithmetic units, can further reduce the division operation's latency.

2. Power Efficiency:

- **Low-Power Design Techniques:** Implement power gating, clock gating, and other low-power design techniques to reduce the power consumption of the division module, making it more suitable for battery-operated and energy-efficient devices.

3. Precision Improvement:

- **Extended Precision:** Support for extended precision formats, such as double-precision (64-bit) or quadruple-precision (128-bit), can be added to handle applications requiring higher precision and larger dynamic ranges.

- **Error Analysis and Correction:** Implement error detection and correction mechanisms to improve the accuracy and reliability of the division results, especially in critical applications.
4. **Hardware Implementation:**
- **FPGA/ASIC Prototyping:** Develop and test the module on FPGA or ASIC platforms to validate its performance in real hardware environments and identify any implementation-specific issues that may not be apparent in simulation.
 - **Custom Instructions for CPUs:** Integrate the division module as a custom instruction in a CPU architecture to accelerate floating-point division operations in software applications.
5. **Support for Special Cases:**
- **Handling Denormals and Subnormals:** Improve the module's ability to handle denormalized (subnormal) numbers accurately, which are important for maintaining precision in very small numbers.
 - **Exceptions and Flags:** Implement support for IEEE 754 exceptions and flags, such as overflow, underflow, divide-by-zero, and invalid operations, to provide comprehensive error handling and debugging information.
6. **Integration with Other Arithmetic Units:**
- **Floating-Point Arithmetic Unit (FPU):** Integrate the division module with other floating-point operations (addition, subtraction, multiplication) to form a complete FPU, enhancing its usability in various computational applications.
 - **Co-Processor Design:** Design a floating-point co-processor that can offload complex arithmetic operations from the main CPU, improving overall system performance.
7. **Software Tools and Libraries:**
- **Driver and API Development:** Develop software drivers and APIs that allow easy integration of the floating-point division module with high-level software applications and operating systems.
 - **Verification and Testing Framework:** Enhance the testing framework with more comprehensive test cases, including random testing, corner cases, and stress tests, to ensure the module's robustness and reliability.
8. **Educational and Research Applications:**

- **Research Platform:** Provide the module as a research platform for exploring new algorithms and techniques in floating-point arithmetic, error correction, and hardware optimization.

Chapter 6

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