EX/IEE/PC/B/IT/T/322/2025

B.E. INSTRUMENTATION AND ELECTRONICS ENGINEERING EXAMINATION

THIRD YEAR SECOND SEMESTER EXAM - 2025

COMPUTER ORGANIZATION, ARCHITECTURE AND NETWORKING

Time : 3 hours **Full Marks : 100**

Answer any five from the following questions:

1. Define pipelining in processor design. Describe the purpose of a register file. Explain in detail the stages of a 5-stage instruction pipeline. What are the challenges associated with pipelining? A 5-stage pipeline has a cycle time of 2 ns. If 100 instructions are executed, calculate the total execution time assuming no pipeline stalls.Differentiate between hardwired and microprogrammed control. [3+3+5+3+3+3] [CO1]

2. What is a shift register? Name its four types.Compare and contrast parallel processing and serial processing.Compare and contrast SIMD and MIMD architectures. What is throughput in pipelining? How is it calculated? Explain the Hybrid Vector Processor Architecture and discuss its advantages.[3+2+3+3+3+6] [CO2]

3. Define static routing and list its advantages. What is dynamic routing and how does it work?What are adaptive routing algorithms? Give examples.Differentiate between bus topology and ring topology.Given a token ring with 5 nodes and a data frame circulation time of 20 ms, calculate the token passing delay if each node holds the token for 2 ms. [5+5+3+3+4] [CO3,CO4]

4. What is a Process Control Block (PCB)? List its components and explain.Describe the difference between Preemptive and Non-Preemptive Scheduling. What is Context Switching? Explain its steps.Define Long-Term Scheduler, Short-Term Scheduler, and Medium-Term Scheduler.[2+3+3+2+4+6] [CO2]

5. What is the difference between a program and a process? Explain the various process states with the help of a diagram. Given the following set of processes with their arrival time and burst time, draw the Gnatt chart and calculate: Completion time (CT), Turnaround time (TAT) and Waiting time (WT). Find out the average turnaround time and waiting time using FCFS, SJF, and Round Robin (Quantum = 3)

Process	Arrival Time	Burst Time
P1	0	8

P2	1	4
P3	2	9
P4	3	5

[3+5+12] [CO2]

6. i) For the reference string **[1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5]**, calculate the number of page faults using FIFO, LRU, and Optimal page replacement algorithms for 3 page frames and compare the results. [3+3+3+1] [CO2]
   ii) In a 5-stage pipeline, a branch instruction causes 3 stall cycles if mispredicted. Calculate the average instruction execution time if 20% of instructions are branches and 10% of them are mispredicted.[5][CO1]
   iii) Consider the following memory partitions: **100 KB, 500 KB, 200 KB, 300 KB, 600 KB (in order)**. A process of size **212 KB**, 417KB, 112KB and 426KB (in order) needs to be allocated. Find out First fit, Best fit and Worse fit. [CO2][5]

7. What are the major advantages and disadvantages of pipelining? Discuss the Johnson Counter and its advantages over a Ring Counter. If a branch predictor correctly predicts 85 out of 100 branches, what is its accuracy? What is the penalty in cycles if each misprediction costs 2 cycles? Explain how cache memory interacts with the processor.[6+(3+2)+6+3][CO1]

8. .What is flooding in networking?What is tree topology? Discuss its structure, advantages, and disadvantages. Discuss how network topology affects network performance and security.[3+3+9+5][CO3,CO4]