Department of Instrumentation and Electronics Engineering
3rd year, 1st semester Examination, 2025
Subject: VLSI Design

Full Marks-100 **Time-3hrs**

MODULE-1

(Answer any three) **$6\times 3 = 18$**

1. What are the advantages and disadvantages of IC? What are the different steps a typical IC fabrication process consists of? 3+3

2. Write the use of SiO2 as a passivating layer. For a controlled doping in a narrow gate region, which doping technique should be used and why? 2+4

3. What is the function of photoresist in the fabrication process? State differences between positive and negative photoresist. 3+3

4. Describe the basic steps in MOS fabrication process with suitable diagram. 6

MODULE-2

(Answer any six) **$12\times 6 = 72$**

5. Consider a CMOS inverter circuit with the following parameters: V_{DD}=3.3V, $V_{TO,n}$=0.6V, $V_{TO,p}$=−0.7V, k_n=200uA/V^2,k_p=80uA/V^2. Calculate the noise margins of the circuit. 12

6. a) " It is not customary to shuffle the NMOS and PMOS in pull-down and pull-up network in a CMOS inverter "-Justify your answer. 6

   b) State advantages of CMOS inverter over depletion load NMOS inverter configuration. Draw a neat diagram for both inverter configurations. 6

7. a) Show that in a CMOS inverter for symmetric switching requires, $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_p$ for all practical purposes, where, $\mu_p = 230\ cm^2/V.s$ and $\mu_n = 580\ cm^2/V.s$. 6

   b) How the switching threshold in a CMOS inverter shifts when $\frac{k_n}{k_p} > 1$. Show using suitable voltage-transfer characteristics curve. 6

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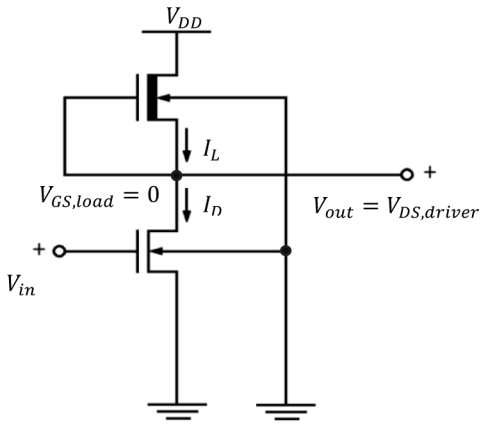
8. Calculate the critical voltages $V_{OL}, V_{OH}, V_{IL}, V_{IH}$ and find the noise margins of the following depletion-load inverter circuit: 12



$\boldsymbol{V_{DD} = 5V}$

$\boldsymbol{V_{T0,driver} = 1.0V}$

$\boldsymbol{V_{T0,load} = -3.0V}$

$\boldsymbol{(W/L)_{driver} = 2, (W/L)_{load} = 1/3}$

$\boldsymbol{k_{n,driver}{}' = k_{n,load}{}' = 25\mu A/V^2}$

$\boldsymbol{\gamma = 0.4V^{1/2}}$

$\boldsymbol{\emptyset_F = -0.3V}$

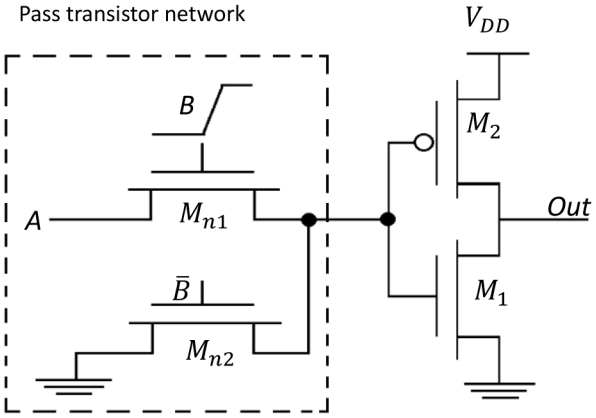
9. Consider the following Boolean Expression:

$$Z = A\,(B + C) + DE$$

a) Calculate equivalent driver $\left(\frac{W}{L}\right)$ ratio of the pull-down network if $\left(\frac{W}{L}\right)_n = 10$ for all NMOS transistors. 5

b) Suggest a design technique for large fan-in circuits to reduce propagation delay in a CMOS inverter with a suitable example. 7

10. Consider the circuit of the given figure:



$V_{DD} = 2.5V$

$(W/L)_2 = 1.5um/0.25um$

$(W/L)_1 = 0.5um/0.25um$

$(W/L)_{ni} = 0.5um/0.25um$

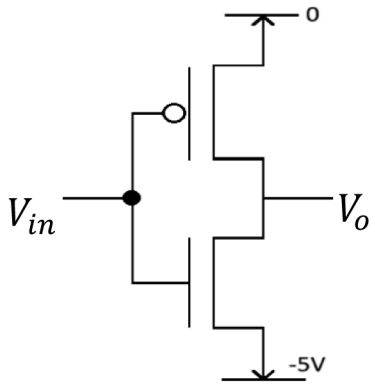
$k_n{}' = 115uA/V^2, kp' = -30uA/V^2$

Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem. Consider Vtn=0.43V and Vtp=0.4V for the network.

a. What is the logic function performed by the circuit? 6+6

b. Explain why this circuit exhibits non-zero static dissipation.

11. Consider the circuit of the given figure:



The threshold voltage $|V_T|$ for each transistor = 2V. What should be the range of input voltage V_{in} , for the circuit to work as an inverter. Analyse the operation of the circuit to estimate the output voltage Vo.

MODULE-3

(Answer any one) **$10\times 1 = 10$**

12. a) Discuss different physical defects in a chip. How are they translated into electrical and logical faults? 5
    b) Explain the relationships between physical defects, electrical faults and logical faults using a simple NOR 2 logic. 5

13. Describe the essential circuit modules for built-in self-test design. 10