Ref. No: EX/IEE/PC/B/T/314/2025

BIEE 3rd YEAR EXAMINATION, 2025
(1st Semester)
SUBJECT: Microcontrollers

Time: Three hours | Full Marks 100

Question	Assume that the 8051 μC uses a 12 MHz crystal	Marks
	UNIT-I (Answer any two)	
1.	With suitable examples explain the bit-wise implementation of the PSW register of the 8051 microcontroller.	10
2.	Draw a functional block diagram of an I/O port line of the 8051 microcontroller and explain how it operates to input/output data.	10
3.	With suitable diagrams describe the on-chip memory organization of the 8051 microcontroller.	10
	UNIT-II (Answer any two)	
4.	Write an 8051 assembly language program that generates the integer average of the unsigned integers stored in memory locations 30h to 37h and stores the same in location 38h.	10
5.	Write an 8051 assembly language program that multiplies two numbers stored in memory locations 30h to 31h in sign-magnitude form and stores the result in 32h and 33h.	10
6.	Write an 8051 assembly language program that compares two unsigned 16-bit integers stored in R0-R1 and R2-R3 and sets the CY flag if the one in R0-R1 is greater than the one in R2-R3. Calculate the code execution time if the content of R0-R1 is greater than that in R2-R3.	7+3
	UNIT-III (Answer any three)	
7.	Using suitable block diagrams explain the 8051 timer operations in modes 1 and 2. Write down the advantages and disadvantages of the timer operation in mode 2.	7+3
8.	Write an 8051 assembly language program that uses the overflow interrupt of timer-1 configured in mode 2 to generate a 2 kHz, 20% duty cycle PWM waveform at port P1.0.	10
9.	What are the 8051 interrupt inputs and their vector addresses? How are the interrupt inputs enabled and prioritized? How does the microcontroller solve the conflict when two interrupt inputs occur at the same instant of time?	3+4+3
10.	Explain the serial port multiprocessor communication scheme involving on master and two slaves. (Write clearly the configurations and communication protocol followed by the master and slave devices)	10
11.	Write an 8051 assembly language program that executes the following tasks sequentially: • Configures the serial port in mode 1with the receiver enabled • Sets the baud rate to 19200 • Serially transmits the content of R1 to R7 registers • Waits in an infinite loop	10

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Question.	Assume that the 8051 μC uses a 12 MHz crystal	Marks
	UNIT-IV (Answer all questions)	
12.	Draw the complete connection diagram of a DAC0800 chip with an AT89C51 μC where: • P0 is used as the data-bus • The DAC uses a 10V V_{REF+}, V_{REF-} is grounded • The output swings between ± 10V (approximately) Generate the count values for a 20-point sawtooth waveform and list them in a tabular form. Write an 8051 assembly language program that repeatedly generates a 100 Hz sawtooth waveform at the output of the DAC.	5+2+8
13.	An ADC0808 is interfaced with an AT89C51 μC where: • P1 is used as the data bus • P0.6 drives the SC/ALE pin and P0.7 drives the OE pin • P2.0 reads the EOC pin Draw the complete connection diagram of a ADC0800 chip with the AT89C51 μC. Write an 8051 assembly language program that repeatedly reads the analog input connected to channel 0 at 1 kHz rate and saves the converted data to memory location 30h.	5+10

80C51 Instruction Set

Arithmatic operations		
mnemonic	byte	m/c cycle
ADD A, Rn/@Ri	1	1
ADD A, direct,#data	2	1
ADDC A, Rn/@Ri	1	1
ADDC A, direct/#data	2	1
SUBB A, Rn	1	1
SUBB A, direct	2	1
SUBB A, @RI	1	1
SUBB A, #data	2	1
INC A/Rn/@Ri	1	1
INC direct	2	1
DEC A/Rn/@Ri	1	1
DEC direct	2	1
INC DPTR	1	2
MUL AB	1	4
DIV AB	1	4
DA A	1	1
Logical operations		
mnemonic	byte	cycle
ANL A, Rn/@Ri	1	1
ANL A, direct/#data	1	1
ANL A, #data	2	1
ANL direct, A	2	1
ANL direct, #data	3	2
ORL A, Rn/@Ri	1	1
ORL A, direct/#data	2	1
ORL direct, A	2	1
ORL direct, #data	3	2
XRL A, Rn/@@Ri	1	1
XRL A, direct/#data	2	1
XRL direct, A	2	1
XRL direct, #data	3	2
RL A	1	1
RLC A	1	1
RR A	1	1
RRC A	1	1
SWAP A	1	1
Program branching		
mnemonic	byte	m/c cycle
ACALL addr11	2	2
LCALL addr16	3	2
RET	1	2
RETI	1	2
AJMP addr11	2	2
LJMP addr16	3	2
SJMP add8	2	2
JZ/JNZ rel	2	2
CJNE A, direct, rel	3	2
CJNE A, #data, rel	3	2
CJNE Rn, #data, rel	3	2
CJNE @Ri, #data, rel	3	2
DJNZ Rn, rel	3	2
DJNZ direct, rel	3	2
NOP	1	1
Data transfer		
mnemonic	byte	m/c cycle
MOV A, Rn/@Ri	1	1
MOV A, direct/#data	2	1
MOV Rn, A	1	1
MOV Rn, direct	2	2
MOV Rn, #data	2	1
MOV direct, A	2	1
MOV direct, Rn	2	2
MOV direct, direct	3	2
MOV direct, @Ri	2	2
MOV direct, #data	3	2
MOV @Ri, A	1	1
MOV @Ri, direct	2	2
MOV @Ri, #data	2	1
PUSH direct	2	2
POP direct	2	2
XCH A, Rn	1	1
XCH A, @Ri	1	1
XCHD A, @Ri	1	1
Boolean variable manipulation		
mnemonic	byte	m/c cycle
CLR C	1	1
CLR bit	2	1
SETB C	1	1
SETB bit	2	1
CPL C	1	1
CPL bit	2	1
ANL C, bit	2	2
ANL C, /bit	2	2
ORL C, bit	2	2
ORL C, /bit	2	2
MOV C, bit	2	1
MOV bit, C	2	2
JC/JNC rel	2	2
JB/JNB bit, rel	3	2
JBC bit, rel	3	2