Ex/IT/PC/B/T/215/2025

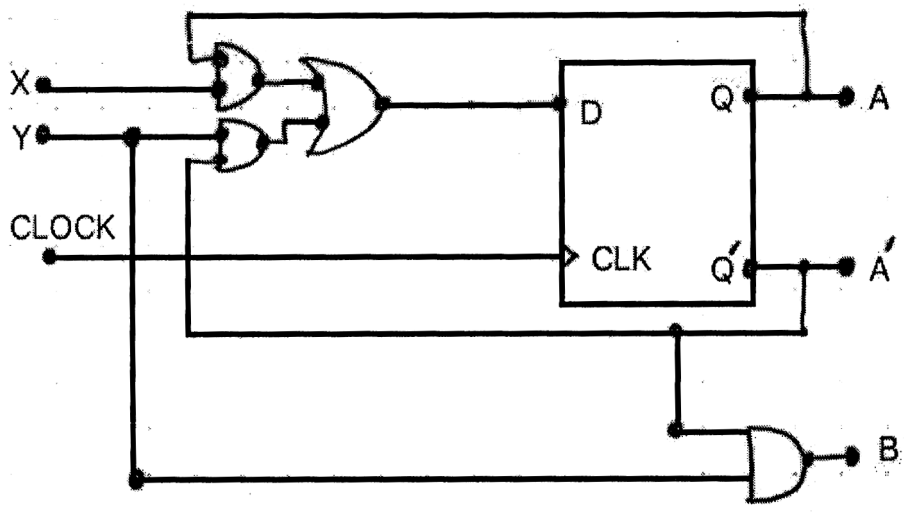
BE INFO TECH 2nd YEAR 1st SEMESTER EXAMINATION, 2025

Computer Organization and Architecture

Time: 3 Hours Full Marks: 100

Answer All 10 Questions

1.a) Study the following sequential circuit. Write down the Equation, State Table and State Diagram of this circuit.



b) Why are I/O Operations slower than Memory Operations? ((2+3+3)+2)[CO1]

2.a) Write down -15 and -17 in Two's Complement form of 6bits. Now add them and analyze the results.

b) Write down 147 in 8 bit binary format. Convert this number to Octal and Hexa-Decimal format. Now, sign-extend this number to 16 bit binary format.

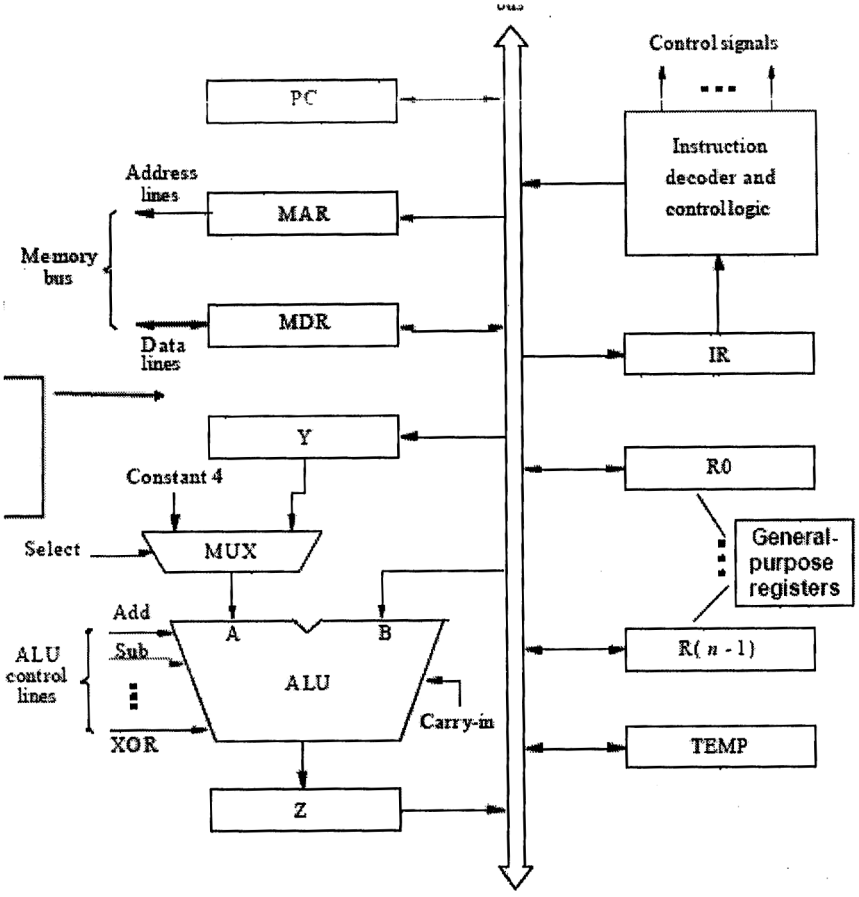
c) What are the differences between Ordinary Binary Multiplication and Booth Multiplication. (3+4+3)[CO2]

3.a) Using the IEEE 754 Rounding Mode 4, convert the following binary fractions to binary numbers.
100.11, 100.10, 100.01, 100.00, 101.11, 101.10, 101.01 and 101.00

b) Convert the decimal numbers 2267 & 58567 to IEEE 754 Floating Point Number (Half Precision). Now add these two floating point numbers and convert the result back to the decimal number. (4+(3+3))[CO2]

[Turn over

4.a) With respect to the diagram shown below, write down and explain the complete sequence of micro-operations performed by the CPU to execute the instruction "Sub (R4), R3, R2" [(R4)+R3 → R2].



b) List down the methods of generating control signals by the CPU to execute instructions. (8+2) [CO3]

5.a) Write down the sequence of instructions needed to evaluate the expression "X=(A+D)*(B*C)" for a Three-Address, Two Address, One-Address and Zero-Address instruction format CPU.

b) Out of the Condition Codes V, Z, N and C; specify which condition code will be set for the following Operation:-

ADD, SUB, MUL, XOR

c) Using proper examples, differentiate between Arithmetic Shift and Rotate Instruction. (4+4+2) [CO3]

6.a) List down the characteristics differences between a RISC CPU and a CISC CPU.

b) Out of the 4 different types of High Level Instructions (viz., Assignment, Loop, Call and If), which one is more expensive from the Memory Reference point of view and why?
(5+5) [CO3]

7.a) Differentiate among SRAM, DRAM, ROM, PROM, EPROM and EEPROM

b) Differentiate between Memory Access Time and Memory Cycle Time.

c) Using relevant diagrams, illustrate the concept of Memory Interleaving. (4+2+4) [CO4]

8.a) Using relevant diagrams, explain the structure of a typical Magnetic Disk Drive.

b) Using numerical examples, illustrate the concepts of Tracks, Sectors and Cylinders.

c) List down the cost of Disk Access. (5+3+2) [CO4]

9.a) List down the four Different criteria to evaluate processor interconnection matrix. Explain them using the example of 3-D Mesh Network.

b) Draw the complete diagram of UMA, NUMA and Multicomputer architecture with proper labeling. (5+5) [CO5]

10.a) With proper Numerical Examples, explain the concept of Speedup, Algorithmic Scalability and Architectural Scalability.

b) With proper examples, show how Matrix Multiplication can be done in parallel.
(5+5) [CO5]