ET/PC/B/T/214/2025

B. E. Electronics and Telecommunication Engineering 2nd Year 1st Semester Examination- 2025

Digital Logic Circuits

Time: 3 Hours **Full Marks: 100**

Answer all the parts of a question in the same place

Module-I [Answer question no. 1 (1×10) = 10] CO1

1. a) Convert $(11010111)_2$ to Gray code.
   b) Perform the subtraction +62 – (+29) using 8-bit 2's complement method.
   c) Convert the hexadecimal number $(A2B.3C)_{16}$ to Octal
   d) Write the importance of Gray code.
   e) Convert the decimal number $(8476.35)_{10}$ to hexadecimal.

(2+2+2+2+2)

Module-II [Answer *any three* questions (3×10) = 30] CO2

2. a) What do you mean by synchronous counter? Draw a 4-stage synchronous serial counter using J-K flip-flops and logic gates. Sketch the counter output waveform considering 0 propagation delay and write the maximum clock frequency expression considering non-zero propagation delay.

(1+4+5)

3. a) Write the truth table and output expressions of a full subtractor. Implement the full subtractor using minimum number of two input NOR gates.
   b) Draw a full subtractor circuit using two half subtractors and single OR gate.

(8+2)

4. a) What is an encoder? Write the truth table of a decimal-to-BCD encoder and draw corresponding gate level circuit.
   b) Draw the block diagram of a BCD adder and label corresponding inputs and outputs.

(7+3)

5. a) Draw the circuit of a master-slave D flip-flop using NAND gates only and explain its operation briefly.
   b) What do you mean by excitation table?
   c) write the excitation table of a J-K flip-flop.

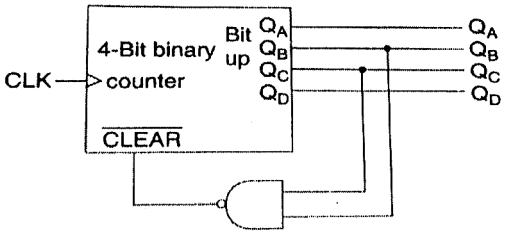
(6+2+2)

Module-III [Answer *any four* questions (4×10) = 40] CO3

6. a) Design a 4-input OR gate using one 4:1 multiplexer and one 2-input OR gate. Assume constants 0 and 1 are available.
   b) Implement the Boolean function F(x, y, z) = x′y + yz + xz′ using minimum number of 2:1 multiplexer and a single inverter only.
   c) Simplify the logic function F (w, x, y, z) = Σ m(0, 1, 3, 7, 8, 9, 11, 15) using Karnaugh map method.

(3+3+4)

7. a) Determine the MOD value of the synchronous counter shown in the following figure. Also write corresponding counter states.



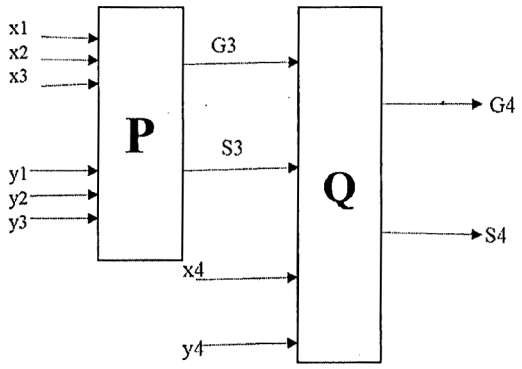
   b) Design a decade counter using direct reset inputs. Also, sketch the corresponding counter circuit using minimum number of J-K flip-flops and logic gates.
   c) What is lockout of a counter? How it can be removed?

(3+5+2)

8. a) Implement the following Boolean functions using a decoder and minimum number of 2-input OR gates.

   F_1 (A, B, C, D) = Σ (1, 3, 5, 6, 14, 15);
   F_2 (A, B, C, D) = Σ (4, 6, 7, 12, 14);
   F_3 (A, B, C, D) = Σ (1, 4, 5, 6, 15);

b) Given logic module P that compares the magnitudes of two 3-bit number X_3 = x1x2x3 and Y_3 = y1y2y3, where x3 and y3 are the least significant bits. Module P has two outputs G3 and S3, such that G3 = 1 if $X_3 > Y_3$; S3 = 1 if $X_3 < Y_3$; and G3 = S3 = 0 if $X_3 = Y_3$. Design the logic unit Q such that together with module P it will serve as a comparator for two 4-bit numbers X_4 = x1x2x3x4 and Y_4 = y1y2y3y4 as shown in the following figure. Find the expressions for G4 and S4 in terms of the inputs to unit Q and show a realization of these expressions using NAND gates only.



(4+6)

9. a) Define propagation delay and noise margin for a logic family.
   b) Draw a 2-input CMOS XNOR gate using minimum number of transistors.
   c) Why is the static power dissipation low in CMOS circuits?

(4+4+2)

10. a) Design a sequence generator to produce the output sequence 1110010.
    b) Draw the state diagram of a sequential circuit that detects three or more consecutive 1's in a string of bits coming through an input line.

(7+3)

Module-IV [Answer *any two* questions (2×10) = 20] CO4

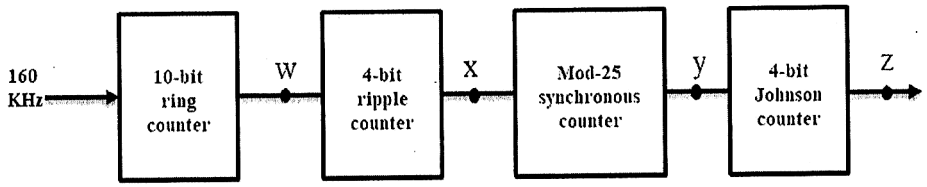
11. a) With a neat sketch, briefly explain the operation of a 4-bit R-2R ladder Digital to Analog Converter (DAC).
    b) The output of a three stage Johnson (switch-tail ring) counter is fed to a DAC. Assume that the counter initially at reset state. Draw the waveform at the DAC output.

(7+3)

12. a) With a neat sketch, briefly explain the operation of a 3-bit parallel (flash) type ADC.
    b) Draw a simplified logic diagram of a 12-hour digital clock, label each block of your design and mention their specifications.

(7+3)

13. a) What do you mean by resolution and settling time of a DAC? Write their importance for hardware based system design.
    b) An ADC has a total conversion time of 200 μs. What is the maximum frequency that its analog input should be allowed to contain?
    c) Determine the frequency of the pulses at points w, x, y and z in the following figure. Give logic in each case.



(4+2+4)