B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
SECOND YEAR SECOND SEMESTER EXAM 2024
DIGITAL CIRCUITS AND SYSTEMS

Time : Three hours Full Marks : 100

Use separate answer scripts for each Part
Answer all the sub-parts of a question altogether

PART I (50 Marks)
Module 1 (CO1 & CO2)

1. Design a sequential circuit:

You are tasked with designing a circuit breaker for a data center. A circuit breaker is placed to regulate the power flowing through the networking equipment and other sensitive infrastructures. A short or faulty ground connection could potentially result in damage to several hundred million dollars' worth of equipment and semiconductor chips.

When the circuit breaker detects a high current, it will trip and automatically break the circuit, saving the equipment in the data center. The moment the circuit detects a Trip, it will automatically go to the Maintenance state at the next clock cycle.

When the circuit breaker requires Maintenance, the system will output a warning signal to inform the system users to refrain from using the system. Once the maintenance has been completed, it will Reset and go back to its Closed state.

What type of finite state machine is this? Explain your reasoning.
The specifications are organized below:

Input	Description
x	Circuit breaker is tripped → logic '1'
y	Maintenance has been completed → logic '1'

Input	Description
Closed	The default state where the circuit is complete
Tripped	The circuit breaker is tripped
Maintenance	The circuit breaker requires inspection
Reset	The circuit breaker is being reset

Output	Description
z	System is in the Maintenance state → logic '1'

- The system always starts from Closed state and will reset back to Closed after Reset
- The system will always go to Reset after Maintenance
- The system cannot be tripped and complete maintenance at the same time

Marks: 20

2. You are part of an applied biosystems lab that requires you to design a circuit to do DNA sequencing. Consider the DNA sequence as a combination of one base pair: Adenine (A) and Thymine (T) in random order. The new DNA sequence is an array of either A's or T's where at each time step, the input is either A or T. For example, "TATAAT" is a sequence with 6 characters where the input at the 1st time step is T and input at the 2nd time step is A and so on. Your goal is to detect if the sequence "**TAAT**" occurs consecutively in the input DNA using a finite-state automaton and output a value "1" if the input DNA strand gives a continuous sequence of "**TAAT**."

   To make it more concrete, here is an example of an occurrence of a DNA sequence "TAAT" in a DNA strand: If the input is "TATTTTAATAATATATA," the state machine should output a value 1 after the 9th character input in the given sequence but should provide an output of value 0 otherwise.

   We could model the circuit as follows:

State Names	State Assignments (Q_1Q_0)	Description
START	00	Initial State
T_1	01	"T" detected
A_1	10	"TA" detected
A_2	11	"TAA" detected

   After the sequence "TAA" has been received, we're in state A2. If given the input "A," go to the START state and output "0." However, if the input is "T," go to the START state and output "1." Similarly, output the value "0" on all other inputs as well (as long as we haven't matched the "TAAT" pattern). Let X be the input, where "0" represents Adenine (A), while "1" represents Thymine (T). Also, let Z denote the output of the circuit.

   a. Would this DNA sequence be considered a Moore or Mealy machine?
   b. Draw the state transition diagram of this finite state machine. Write out the state transition table.
   c. Using K-maps, derive the equations of the next states and output.
   d. Design the sequential circuit using D flip-flops and draw the circuit diagram.

Marks: 20

OR

Answer any 4 of Qs. 3

3. a) Design a hazard-free circuit to implement the following function.

   $F(A, B, C, D) = \Sigma m(1, 3, 4, 5, 6, 7, 9, 11, 15)$.

   b) Minimize the following Moore machine using the implication table

PS	NS (X=0)	NS (X=1)	Output z
A	D	C	0
B	F	H	0
C	E	D	1
D	A	E	0
E	C	A	1
F	F	B	1
G	B	H	0
H	C	G	1

c) Design a synchronous sequential circuit that takes a one-bit stream $x_0x_1x_2$ ... as input, and outputs a one-bit stream $y_0y_1y_2$ .... The i-th output bit y_i is 1 if and only if the four most recently read input bits $x_i{-}3x_i{-}2x_i{-}1x_i$ have odd parity. Here is an example. At the beginning of the input, four bits are not read. Assume that the missing bits are 0 (that is, $x_{-3} = x_{-2} = x_{-1} = 0$).

Input: 0100110100111010...

Output: 0111000101001110...

d) Design a 4-bit binary ripple counter (asynchronous) that has one count-enable input and one control input. If the control input is 0, the counter increments by 1 modulo 16. If the control input is 1, the counter increments by 2 modulo 16. Use negative-edge triggered T flip-flops. The count-enable input is (negative) edge-sensitive, whereas the control input is level-sensitive.

e) Design a Mealy machine N that, given the output of M, produces the corresponding input for M. Specify the start state of N. (Treat M as a message-encoding circuit. Then, N is the corresponding message decoding circuit.)

Marks: 20

Module 2 (CO5)

Answer any 1 of Qs. 4

4. a) Implement a standard LFSR for the characteristic polynomial f(x) = x8 +x7 +x2 +1.
Multiply the two numbers (54) and (-7) by using the Booth's multiplication algorithm.
Multiply the two numbers (1 0 1 0) and (0 1 1 0) by using the Partial Sum Approach.

b) Briefly describe Booth's algorithm with a flowchart. Find BCD Addition of 974 and 599.

Marks: (4+3+3) / (8+2) = 10

Ref. No. : Ex/ET/PC/B/T/222/2025

B.ETCE 2nd Year 2nd Semester Examination 2025

DIGITAL CIRCUITS AND SYSTEMS

Time : Three hours | **PART II (50 Marks)** | Full Marks : 100

Use Separate Answer scripts for each part

Answer All Questions. Each Question has two options, choose one of them

Q. 1 A **10 x 2 =20**

a. Write a Verilog code of 8x1 using 4x1 and 2x1 MUX (Use Gate level programming for 4 x1 and 2x1. Use Structural level instances for 8x1 MUX using already developed 4x1 and 2x1 MUXs).Write its Test Bench

b. Write a Verilog code for state machine shown in Fig 1 . This FSM has eight states: idle, r1, r2, r3, r4, c, p1, and p2. Also, it has one input, mem, and one output, out1.

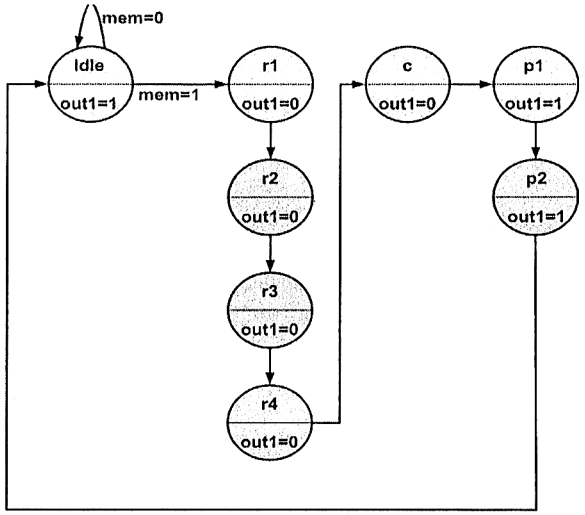


Fig.1

Or

Q. 1 B **10x 2=20**

a. Design a 4-bit signed comparator using Verilog (Gate level) that can compare two 4-bit signed numbers and output the greater, lesser, or equality status.Introduce a conflict scenario where the inputs A and B are extremely close in value (e.g., one is 0111 and the other is 1000), which could result in erroneous comparisons due to timing or signal propagation delays.

b. Following timing diagram in Fig 2 describes the specification given by user. The circuit component uses D flipflop and combinational logic gates. Draw the circuit and write its gate level / structural level verilog code.

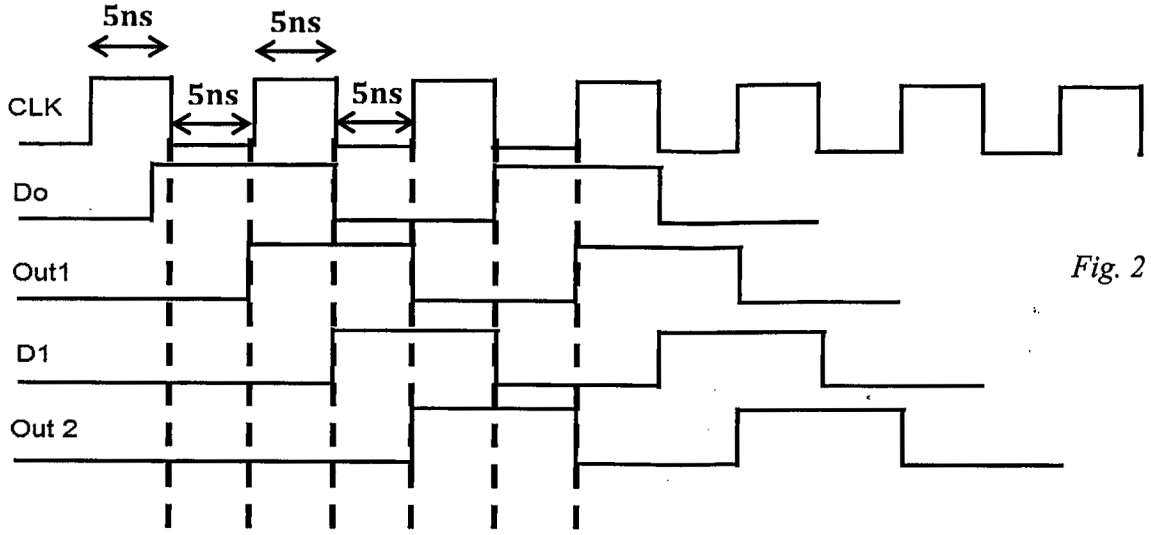


Fig. 2

Q. 2 A **6+8+2+4=20**

a. Explain the Unateness of two input NAND gate.

b. Write down the table of unateness for the gates in each level of the following circuit shown in Fig 3

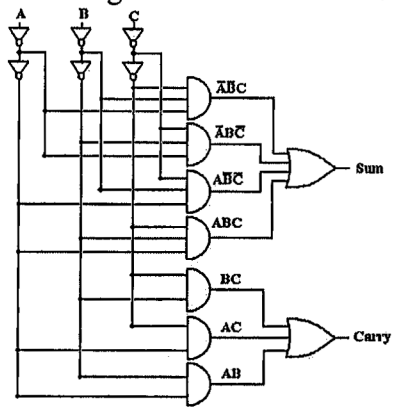


Fig. 3

c. What is clock gating path? Show the clock gating path in the circuit shown in Fig 4.

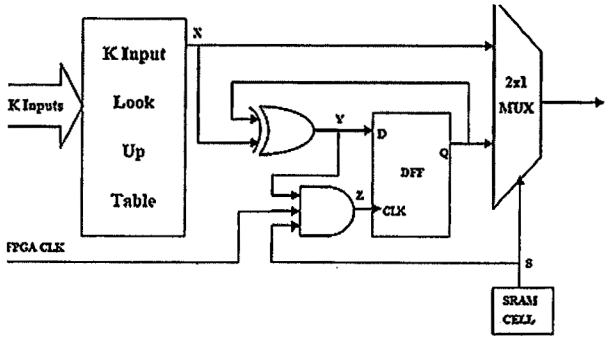


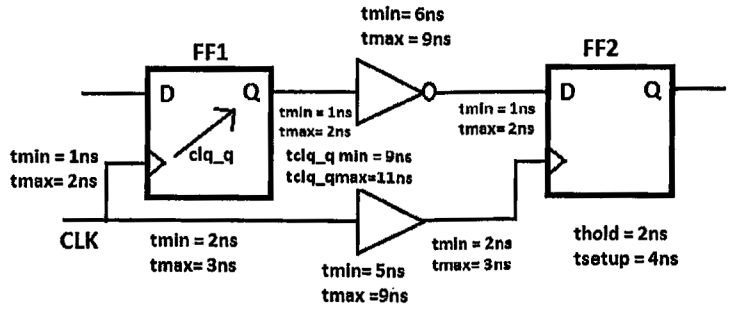
Fig. 4

Or

Q. 2 B **6+6+8=20**

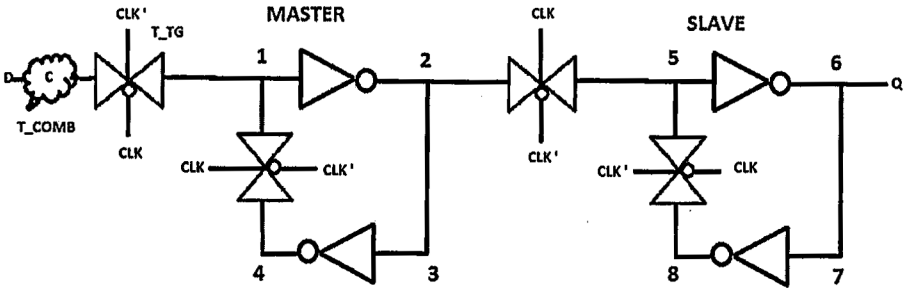
a. In the following circuit shown in Fig 5, find out if there is any hold violation?

Fig. 5



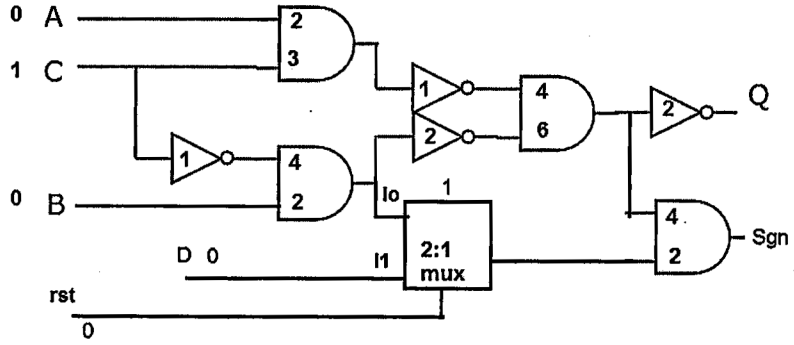
b. From the circuit shown in Fig 6, explain the concept of setup time and hold time. Clock pins are connected with transmission gates.

Fig. 6



c. Find out the critical path of the circuit shown in Fig 7 by calculating AT RAT table. Consider RAT as 13.

Fig. 7



Q.3 A **5+5=10**

a. From the expression F1(A,B,C)=A'B+BC Show the realization using PAL architecture.

b. Using PROM realize the following expression F1(a,b,c,d) = $\sum$ m(8, 4, 12, 14, 13) + d(10, 6).

Or

Q.3 B **10**

Design the Configurable logic block (CLB) based network to realize a two bit carry look ahead adder. Choose suitable LUTs to store the truth table values and finally draw with proper interconnection matrix the complete block. Justify what should be the Bit stream data for this CLB network