M.E. Electronics and Tele-Communication Engineering
First Year First Semester Examination, 2025

Analog VLSI Circuits (NV)

Time: **3 Hours** Full Marks: **100**

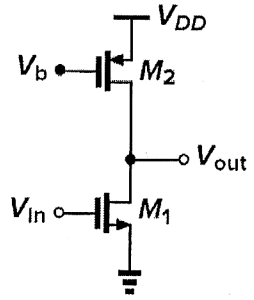
All parts of the same question must be answered together. Ensure neatness and clarity. Any approximation used in solving problems need to be justified.

Assume: $V_{DD} = 2$ V, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 50\ \mu A/V^2$, $\lambda_n = 0.1\ V^{-1} = 0.5\lambda_p$, $L = 0.5\ \mu m$, and $|V_{TH}| = 0.5$ V for all MOSFETs, if not specified otherwise.

Q1 Answer ***part (a)*** and ***any TWO*** from the rest: [PO1]

a) Draw the circuit diagram of a cascoded common-source amplifier and discuss on its advantages. 5

b) Derive the expression of the input-referred rms noise voltage of the following common-source amplifier, considering both thermal and flicker noise sources. 10



c) Explain the advantages of differential signaling in an integrated circuit. Can two common-source amplifiers be fed with differential input signal in order to realize a fully-differential amplifier? 10

d) In a PTAT cell, replace the diode-connected BJTs with diode-connected MOS transistors, and show that the MOSFETs maintain a constant-g_m. 10

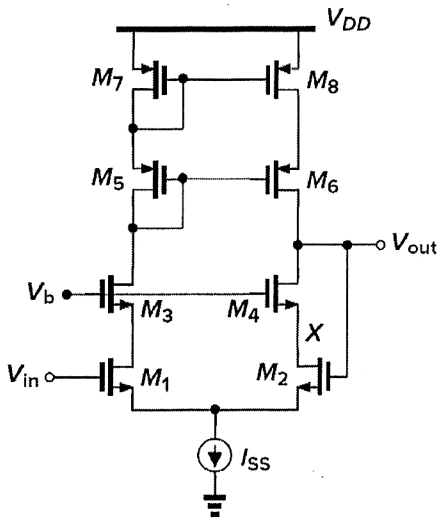
Q2 Answer ***part (a)*** and ***any TWO*** from the rest: [PO2]

a) Discuss on the realization of BJTs in CMOS technology. 5

b) For a quiescent current consumption of 10 μA in the NMOS-based input-pair of a fully-differential *Folded-Cascode OTA*, calculate the width of the input transistors for obtaining unity-gain frequency of 10 MHz (at load capacitance of 5 pF). Draw the corresponding circuit schematic. 10

c) Find the maximum permissible range of the output voltage for a *Telescopic Cascode OTA* being used to implement a unity-gain buffer (in figure below). 10

Derive the expression of the loop-gain (at low frequencies) of the negative-feedback loop involved in this circuit.

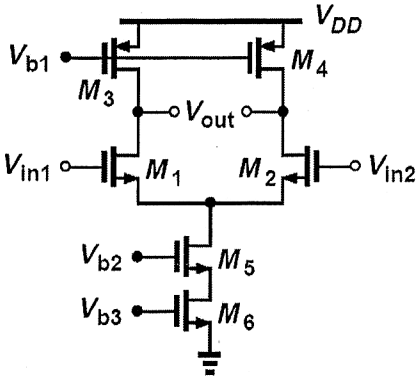


d) Draw the circuit diagram and derive expressions for the dc-gain, ICMR, and output voltage swing of a 5T OTA with PMOS input-pair. 10

Q3 Answer ***part (a)*** and ***any TWO*** from the rest: [PO3]

a) Discuss how frequency compensation is done for ensuring stability of a two-stage OTA in negative feedback. 5

b) Draw the CM half-circuit and hence derive the expression of the CM gain for low frequency operation of the following differential amplifier. Now assuming that $r_{o4} = (r_{o3} + \Delta r_o)$, derive the expression of its CM-to-DM gain. What might happen to the CMRR at higher frequencies due to the parasitic capacitance at the source node of M1/M2? 10



c) For a fully-differential 5T OTA, draw the circuit schematic including the CMFB with resistive CM detection. What will be the expression of the open-loop DM gain of this OTA circuit? Describe how many poles are present in its CMFB path. 10

d) Draw the circuit schematic of a Miller-compensated 2-stage OTA with single-ended output, where the first-stage is a folded-cascode stage with PMOS input pair and the second-stage is a common-source stage. Discuss about the poles 10

present in this circuit while deriving their approximate expressions.

Q4 Answer ***part (a)*** and ***any TWO*** from the rest: [PO4]

a) Discuss how resistors are practically realized in CMOS integrated circuits with proper diagram(s). 5

b) Explain how layout design must be done to enable proper transistor matching, together with a representative layout diagram (with clear labelling). 10

c) Draw the schematic of a *Low Dropout Regulator* (LDO) and design its pass-transistor branch having quiescent power dissipation of 100 μW, output voltage of 1.5 V, and negative feedback loop-gain of 75 dB. Consider that the input reference voltage is 1.2 V and open-loop gain of the constituent OTA is 40 dB. 10

d) Design a *Beta Multiplier Current Reference* for generating 10 μA output current (using any necessary assumption) and draw the final designed circuit. Discuss the necessity of a start-up circuit for this, using circuit diagram. Mention if there is any resultant limitation on the supply voltage range for the overall circuit. 10