M.E. Electronics and Tele-Communication Engineering
First Year First Semester Examination, 2025

Analog VLSI Circuits (NV)

Time: **3 Hours** Full Marks: **100**

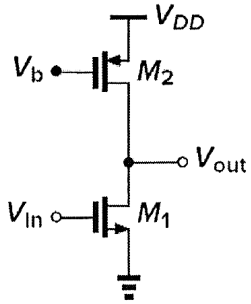
All parts of the same question must be answered together. Ensure neatness and clarity. Any approximation used in solving problems need to be justified.

Assume: $V_{DD} = 2$ V, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 50\ \mu A/V^2$, $\lambda_n = 0.1\ V^{-1} = 0.5\lambda_p$, $L = 0.5$ µm, and $|V_{TH}| = 0.5$ V for all MOSFETs; and x is the last digit of your exam roll number.

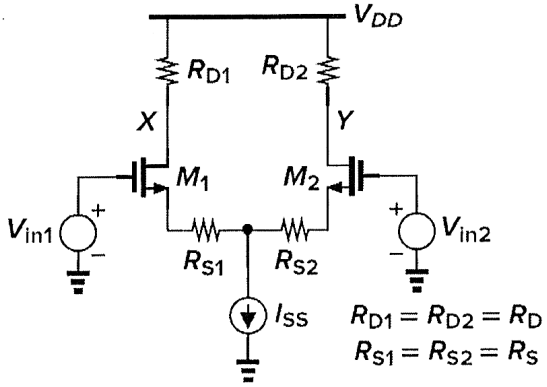
Q1 Answer ***part (a)*** and ***any TWO*** from the rest: [CO1]

a) Draw the circuit diagram of a common-source amplifier with cascoded input device and load, and derive the expression of its low frequency voltage gain. 5

b) Derive the expression of the rms noise voltage referred to the gate terminal of the transistor M2 of the following common-source amplifier, considering both thermal and flicker noise sources. 10



c) Explain the advantages of differential signaling in an integrated circuit. Find the expressions of differential and common-mode voltage gain of the following diff amp neglecting channel-length modulation and body effect. 10



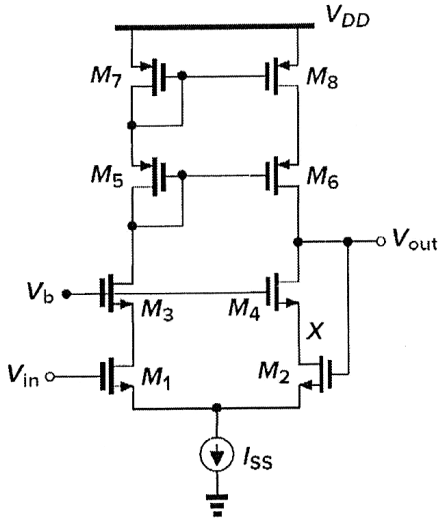
d) Draw the schematic of a PTAT cell by replacing the diode-connected BJTs with diode-connected MOS transistors. Explain if these MOSFETs would maintain a constant-g_m. 10

Q2 Answer ***part (a)*** and ***any TWO*** from the rest: [CO2]

a) Discuss on the realization of bipolar transistors in CMOS technology. 5

b) For a quiescent current consumption of (5+x) μA in the NMOS-based input-pair of a fully-differential *Folded-Cascode OTA*, calculate the width of the input transistors for obtaining unity-gain frequency of 12 MHz (at load capacitance of 6 pF). Draw the corresponding circuit schematic. 10

c) Find the maximum permissible range of the output voltage for a *Telescopic Cascode OTA* being used to implement a unity-gain buffer (in figure below). Derive the expression of the loop-gain (at low frequencies) of the negative-feedback loop involved in this circuit. 10

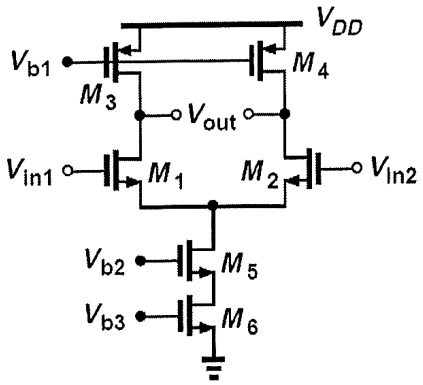


d) Draw the circuit diagram and derive expressions for the dc-gain, ICMR, and input referred noise voltage of a 5T OTA with PMOS input-pair. 10

Q3 Answer ***part (a)*** and ***any TWO*** from the rest: [CO3]

a) Discuss how frequency compensation is done for ensuring stability of a two-stage OTA in negative feedback. 5

b) Draw the CM half-circuit and hence derive the expression of the CM gain for low frequency operation of the following differential amplifier. Assuming that $r_{o4} = (r_{o3} + \Delta r_o)$, derive the expression of its CM-to-DM gain. What might happen to the CMRR at higher frequencies due to the parasitic capacitance at the source node of M1/M2, and at the output nodes? 10



c) For a fully-differential 5T OTA, draw the circuit schematic including the CMFB with resistive CM detection. What might happen if the CMFB circuit is not used? What will be the expression of the open-loop DM gain of this OTA circuit? 10

d) Draw the circuit schematic of a Miller-compensated 2-stage OTA with single-ended output, where the first-stage is a folded-cascode stage with NMOS input pair and the second-stage is a common-source stage. Derive the expressions of the poles and zeros present in this circuit. 10

Q4 Answer ***part (a)*** and ***any TWO*** from the rest: [CO4]

a) Discuss on the need of various design rules for integrated circuit layout with suitable diagram(s). 5

b) What are the reasons behind fabrication induced random mismatches? Explain how layout design can be done to enable proper transistor matching (with clear labelled diagram). 10

c) Draw the schematic of a *Low Dropout Regulator* (LDO) and design its pass-transistor branch having quiescent power dissipation of (50+5*x*) μW, output voltage of 1.5 V, and negative feedback loop-gain of 75 dB. Consider that the applied input reference voltage is 1.2 V and the open-loop gain of the constituent OTA is 42 dB. 10

d) Design a *Beta Multiplier Current Reference* for generating (10+0.5x) μA output current (using any necessary assumption) and draw the final designed circuit. Discuss the necessity of a start-up circuit for this. Explain if there is any resultant limitation on the supply voltage range for the overall circuit. 10