M.E. Electronics and Tele-Communication Engineering
First Year First Semester - 2025

Subject: Advanced Electronic Design Automation

Full Marks: 100 **Time : 3hrs**

Answer all questions. Q.1 to Q.3.have two options (choose any one)
Answer all the part of the question in same place. Different part of questions at different sections will carry no marks.

All the programme should follow proper syntax. Any kind of syntax error (semicolon , comma error, mismatch in identifier, wrong statement etc.) will carry no marks

Q.1A **4+4+6+6=20**

a. Briefly explain about Chiplet?
b. Explain the significance of PDK and its use.
c. What is logic synthesis and how it is carried out.
d. What is IP Core and write down their categories.

Or

Q.1 B **4+6+4+6=20**

a. Explain the significance of RTL Signoff in the IC design flow. What key aspects are checked before signoff?
b. Describe the importance of CDC (Clock Domain Crossing) checks during RTL Signoff.
c. Explain Back annotation
d. What is technology mapping and how technology mapping can affect delay.

Q.2A **8+5+7 =20**

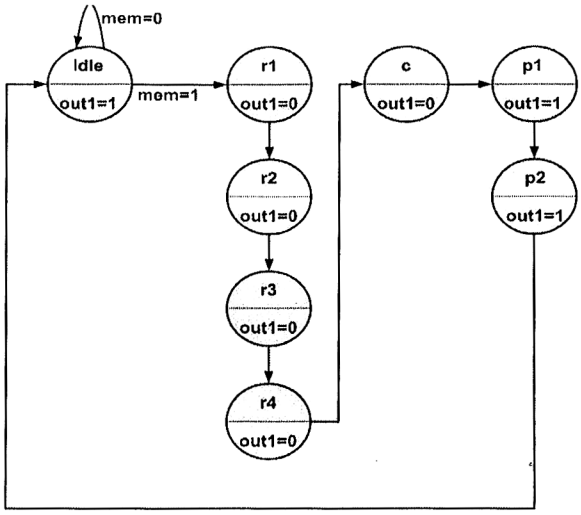
a. Write a Verilog code of 8x1 using 4x1 and 2x1 MUX. Write its Test Bench
b. Write a Verilog code on Moore Machine.

Or

Q.2 B **10 x 2= 20**

a. Design a parameterized Verilog module for anN-bit Carry Look-Ahead Adder. How would you modify the design to efficiently scale for large values of N?

b. Write a Verilog code for following state machine. This FSM has eight states: *idle*, *r1*, *r2, r3, r4, c, p1,* and *p2*. Also, it has one input, *mem*, and one output, *out1*.



Q.3A **8+6+6= 20**

a. What is the synthesized output of the following code?

```
module GrayToBinary (A, B, C, Bc0, Bc1, Bc2);
  input A, B, C;
  output Bc0, Bc1, Bc2;
  wire NotA, NotB, NotC;

  assign NotC = ~ C;
  assign NotB = ~ B;
  assign NotA = ~ A;

  assign Bc0 = (A & B & NotC) | (A & B & C) |
               (A & NotB & C) | (A & NotB & NotC);
  assign Bc1 = (NotA & B & C) | (NotA & B & NotC) |
               (A & NotB & C) | (A & NotB & NotC);
  assign Bc2 = (NotA & NotB & C) | (NotA & B & NotC) |
               (A & B & C) | (A & NotB & NotC);
endmodule
```

b. For a Sum of Product what kind of timing hazards is possible? Explain with a case study. How to create a hazards free circuit?

c. Discuss the impact of space complexity on the memory usage during synthesis, focusing on intermediate representations and lookup tables.

Or

Q.3 B **6+8+6= 20**

a. Draw the synthesized circuit of following code. Use OAI logic as technology library

```
module SelectOneOf (A, B, Z);
  input [1:0] A, B;
  output [1:0] Z;
  reg [1:0] Z;

  always @ (A or B)
    if (A > B)
      Z = A;
    else
      Z = B;
endmodule
```

b. Explain with example about Gate Merging, Sub expression elimination and Power Optimization in synthesis.

c. From the following porgramme write the gate level synthesis code in Verilog.

```
modulecritical_path_example (inputwireclk,input wire A, B, C, D,outputreg F);
        wire w1, w2, w3, w4;
// Logic implementation
        assign w1 = A & B;              // AND gate
        assign w2 = C ^ D;              // XOR gate
        assign w3 = w2 & w1;            // AND gate
        assign w4 = w1 | w3;            // OR gate

        always@(posedgeclk)
        F <= w4;
endmodule
```

Timing constraints are as follows

AND gate delay: 2 ns ; OR gate delay: 3 ns; XOR gate delay: 4 ns; Clock Period: 10 ns

Q.4 **5+5+10=20**

a. How zero bias threshold voltage is modeled in SPICE level 1? Draw clear diagram of equivalent circuit of MOSFET for AC noise analysis

b. The MOSFET has an initial channel length L of 1 μm and operates at a supply voltage VDD of 5V. The oxide thickness tox is 10 nm. To maintain reliability and avoid breakdown due to high electric fields, constant field scaling is applied with a scaling factor S=1.5.Determine the following:

1. The new values of channel length L′, supply voltage VDD′, and oxide thickness tox′ after scaling.
2. The impact of scaling on current density and power density in the MOSFET.

Q.5 **4+6+10 = 20**

a. Brief explains ANOVA and justifies the usage of ANOVA in Surface model

b. Draw the flowchart to generate response surface model (RSM) in comparison to SPICE model. Write down the multi variable equation for RSM with inner products.

c. In the following circuit X_4 has as-a-0. For a test vector 1001 that detects error simulate without and with fault