Ref. No.: Ex/PG/ETC/PE/115E/2025

Master of Engg. (Electronics & Tele-Comm. Engg.) Exam., 2025
(First Year, 1st Semester Exam. 2024-2025 Session)

PROGRAMMABLE LOGIC CONTROLLER
(Specialization: ML&IC)

Time: 3 Hours | Full Marks: 100

Answer All the **FIVE** Modules.
(All parts of the same question must be answered at one place only)

Module I (CO1)

1. (i) Differentiate PLC and PC, and List the advantages of PLC.
(ii) Illustrate the typical components of PLC with suitable diagrams and explain the same.

[5+15 Marks]

Module II (CO2)

2. (i) List the necessary steps in order to design Digital circuit with control objective and to develop the equivalent Ladder Diagram. Based on these steps, solve the Problem given below:
(ii) A Railway station has 3 Platforms A, B, and C. A train is coming to the Station. It is to be directed to Platform A if A is empty. The train is to be directed to Platform C, only if both Platforms A and B are Full. The train has to wait of all the Platforms are full. Develop the necessary Ladder Logic Diagram to implement the same. [5+15]

Module III (CO3)

3. (i) Differentiate Electronic Timers and PLC Timers.
(ii) Differentiate ON-Delay and OFF-Delay PLC Timers
(iii) Develop a Ladder Diagram for the Two Motor System satisfying the following conditions:
A. Start PUSH Button starts Motor-1
B. After 10 seconds, Motor-2 is ON
C. Stop Switch stops Motor 1 and Motor 2 [5+5+10]

Module IV (CO4)

4. (a) (i) Differentiate Microprocessor Unit (MPU) and Microcontroller Unit (MCU) with a simple Block Diagram.
(ii) State the Evolution and List the Features of MCS-48, MCS-51 and MCS-96 Family of MCUs.
(iii) Justify / State the Reason behind the Logical Separation of Data Memory (DM) and Program Memory (PM) in MCU. Draw the Memory of MCS-51 DM and PM. [2+3+5]
(b) (i) State the "Timer" Function mode of 8051 MCU.
(ii) Differentiate Mode-0 and Mode-1 operation of 8051 Timer with appropriate Block Diagrams.
(iii) State the Mode-2 operation of 8051 Timer and its application. [2+2+3]
(c) List the conditions that can block the generation of "LCALL 16-bit Address" instruction in the 8051 MCU interrupt process. [3]

Module V (CO5)

5. (a) (i) All the Conditional Branching Instructions in 8051 MCU specify the destination address by _____ addressing mode only. (ii) Identify the appropriate / optimal JUMP instruction if the offset of the Jump location is > 127 and is within the same 2K Block of the current instruction: _____
(iii) How many Program Fetches occur in a Machine cycle? _____
(iv) The addressing mode used in the "MOVC Instruction" is _____
(v) The example for the instruction that uses the "Indirect addressing mode" is _____ [5 X 2]

(b) A Look Up Table (LUT) with 6 Bytes are stored in Code Memory starting from 8000H onwards. Write an 8051 Assembly Language Program (ALP) to read the LUT, and to store them from the RAM location 30H onwards. [10]