Ex/PG/ETC/PE/T/115J/2025

M. ETCE FIRST YEAR FIRST SEMESTER EXAMINATION-2025

Subject: Low Power VLSI Design Time: 3 Hours Full Marks: 100

All parts of the same question must be answered in one place only

1. Answer **any Five** Questions: [Marks: 5×8=40]

A. Explain the concept of switching power dissipation and its significance in low-power circuit design.
B. Write a short note on system-level measures while designing low-power circuits.
C. Write about Drain-Induced Barrier Lowering (DIBL) and punch-through in short-channel MOSFETs.
D. Discuss the different sources of power dissipation in integrated circuits.
E. Explain the concept of glitch power dissipation and how it affects circuit performance.
F. Explain the role of supply voltage scaling in switching power reduction.
G. Discuss methods to minimize switched capacitance in low-power circuit design.
H. Explain a few leakage reduction techniques while designing low-power VLSI circuits.

2.

A. Explain the architecture and working principle of a **Ripple Carry Adder (RCA)** with a suitable schematic. Discuss the drawbacks of RCA in terms of delay and power consumption. Describe the **Carry Select Adder (CSA)** and how it improves over RCA. Compare RCA and CSA in terms of area, speed, and power efficiency for low-power applications.

[Marks: 5+5+5+5 = 20]

OR

B. Explain the working of a **Carry Look-Ahead Adder (CLA)** with a neat schematic. How does CLA reduce propagation delay compared to RCA? What is a **Carry Bypass Adder (CBA)**? Explain how it reduces carry propagation delay. Compare CLA and CBA in terms of speed and power consumption for low-power VLSI design. [Marks: 5+5+5+5 = 20]

3.

A. Explain the **Wallace Tree Multiplier** and how it reduces computation time. Describe the **Booth Multiplication Algorithm** with an example. Compare the delay, area, and power consumption of Wallace Tree and Booth Multipliers. Which multiplier is more power-efficient, and why? [Marks: 5+5+5+5 = 20]

OR

B. Explain the working principle of a **Booth Multiplier** and how it improves signed multiplication. What is a **Bit-Serial Multiplier**, and how does it function? Compare Booth and Bit-Serial Multipliers in terms of power, area, and delay for low-power VLSI applications. Discuss how **pipelining and clock gating** can be applied to Booth Multipliers to reduce power consumption. [Marks: 5+5+5+5 = 20]

4.

A. Define **clock skew**, **clock jitter**, and **clock grating**. Explain their impact on circuit performance and how they can be minimized. Describe the **clock distribution network** inside an IC. What are the challenges associated with clock distribution in large-scale integration? [Marks: 12+8 = 20]

OR

B. Explain different **on-chip clock generation techniques** used in modern VLSI circuits. Discuss their advantages and trade-offs. Define **clock latency** and **clock slew**. How do these parameters affect timing and power consumption in a digital system? What is a **clock tree**? Discuss its role in clock distribution and how it helps in reducing power consumption.
[Marks: 10+6+4 = 20]