M.E. Electronics and Tele-Communication Engineering
First Year Second Semester Examination, 2025

Advanced Analog IC Design (NV)

Time: **3 Hours** Full Marks: **100**

(Use Separate Answer Script for each part)

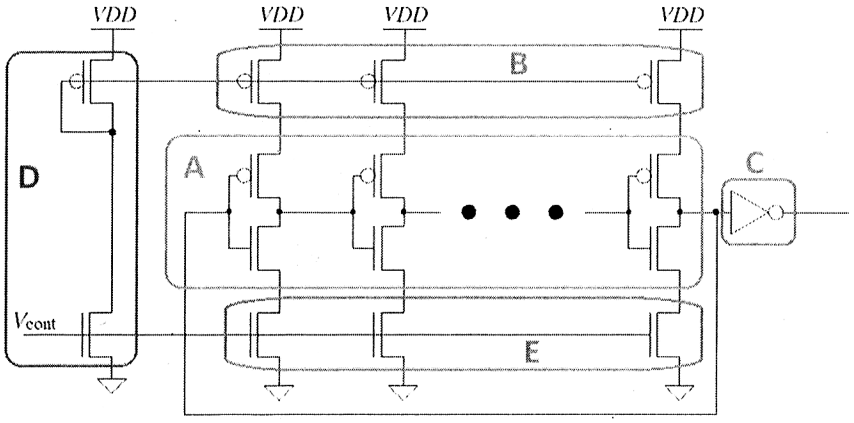
PART-I (70 marks)

Answer any 3 from the 4 questions [each comprises: CO1, CO2 & CO3]

*All parts of the same question **must** be answered together.*

Q1.a Discuss the main differences between an amplifier and an oscillator using Barkhausen's criteria together with representative diagrams. Discuss the mode of operation of a non-linear oscillator using representative schematic diagram. 10

Q1.b Identify the following circuit topology and describe the individual functionality of the highlighted constituent sections A to E. 10



Q1.c Explain how the o/p (at C) would be affected if the aspect ratio of the transistors in sections B and E are made 4× of that of the corresponding transistors in section D. 3

Q2.a Discuss on the applications of phase locked loops in electronic circuits. Why do we need a VCO within such a loop? 8

Q2.b Draw the circuit schematic of differential implementation of ring oscillator – both with an even and an odd number of stages, with proper justification. Assuming the transfer function of each stage is $-A_0/(1 + s/\omega_0)$ (with s, A_0 and ω_0 having the usual meanings), what is the minimum required voltage gain per stage if we have a four-stage differential RO? 15

Q3.a	Draw the schematic of a type-1 PLL implemented using XOR, RC-LPF, and LC VCO blocks.	7
Q3.b	Show a simple circuit implementation of a phase/frequency detector (PFD) with corresponding input and output waveforms.	6
Q3.c	How a PLL is affected due to jitter in the input signal? Using the small-signal model of a PLL, describe why the slow jitter components from the constituent VCO are suppressed, but fast jitter components are not?	10
Q4.a	Compare different ADC architectures (Flash, SAR, Sigma-Delta, and Pipelined) in terms of speed, power, resolution, and area.	16
Q4.b	Suggest suitable ADC types for a wireless sensor application with justification.	7

One (**01**) additional mark for neatness and clarity of the answers!

Ex/PG/ETC/PE/T/123J/2025

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PART-II (30 marks)

Answer any 2 from the 3 questions

*All parts of the same question **must** be answered together.*

1. Compare different ADC architectures (Flash, SAR, Sigma-Delta, Pipeline) in terms of speed, power, resolution, and area. Suggest suitable ADC types for a wireless sensor application and justify. 15

2. What are subthreshold analog circuits? Discuss their relevance in ultra-low power applications and compare them with strong-inversion analog designs in terms of performance and robustness. 15

3. Discuss the impact of process variations on analog circuit performance. Describe common techniques used to improve robustness, such as layout matching and trimming. 15