M.ETCE FIRST YEAR SECOND SEMESTER, 2025

Embedded and Cyber-Physical Systems

Time: 3 hours **Full Marks: 100**

Answer any 4 questions.

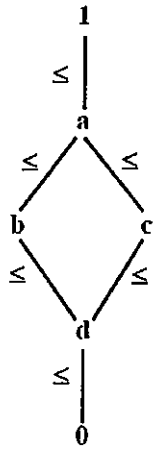
1. An output pulse z is to be coincident with the second of a sequence of consecutive x_2 pulses following an x_1 pulse. Draw the state diagram and hence design the state-machine for the given problem using J-K flip-flops.

[25]

2. a) Construct a hierarchical state machine for the elevator problem, operated from outside the elevator. Draw 3 state diagrams, one for elevator-control in normal mode, the second one for power-failure situation, and the last one for fire-extinguishing, in case the elevator is caught with fire.

   b) Justify the importance of the hierarchical design of the elevator.

   c) Given the lattice diagram of system input variables: *a,b,c,d,e* of an automaton, capable of recognising "*aabb*" sequence by at least 3 possible ways. Design the Lattice automaton, and hence evaluate the lattice belief to recognise the given sequence using the lattice diagram provided.



   d) What are the merits of lattice automaton over fuzzy and stochastic automaton?

[8+6+8+3]

3. a) Draw the PLA for the input output combinations listed in Table I. Use all-MOS realization.

Table- I

A_2	A_1	A_0	y_1	y_0
0	0	0	0	1
0	1	0	1	0
1	0	0	1	1
1	1	0	0	0

b) Construct the PAL for the following switching functions:

$$y_1 = x_2 x_1' + x_1 x_0$$
$$y_0 = x_1 x_2' + x_2 x_0.$$

c) Construct a PLD for the following switching function:

$$y_0 = x_1 x_2' + x_2 x_0 y_0.$$

[10+10+5]

4. a) Draw the schematic architecture of Fairchild corporation's p-ASIC configuration logic block/programmable logic device (PLD).
   b) Realise a half-adder by trials on a single p-ASIC PLD module.
   c) Suggest an automation to synthesise the half-adder on this PLD using evolutionary algorithm.
   d) What is a complex PLD (CPLD)?
   e) Develop a VHDL program of a full-adder using
      i) XOR-gates, AND-gate and OR-gate,
      ii) half-adders.

[3+6+4+3+9]

5. a) Develop an Assembly-level program for transfer of 10 characters from your microcomputer system to a dot-matrix printer. Also show the hardware interface between the printer and your microcomputer system. Draw the timing diagrams of the interfacing signals you have used in your system.
   b) The operating temperature of a plant needs to be adjusted under on-line condition (i.e., without shutting down the plant) by an operator. The operator should press the following 3 keys in sequence:- Vector Interrupt, x and y, where $x, y \in [1,9]$. Use interrupt-driven data-transfer to implement the above and write down an Assembly-Level-Program to perform the task.

[12+13]

6. a) Illustrate task-merging and splitting on a task graph. Also explain the importance of the above operations.

b) A big distributed embedded system needs to be realized using alternatives from hardware (power PC / FPGA board / ARM microcontroller) and software (Real-time MATLAB / Smart-C) to realize individual tasks. Draw a task graph, comprising 7 tasks. Prepare a table indicating possible computational time of each task on different hardware and software. Assuming communication overhead to be 3 seconds between 2 different hardware/software, determine one possible optimal choice of hardware/software to realize individual task of the embedded system. Also compute the minimum time required for complete execution of the tasks following the task graph and optimal choice of pure hardware/software for the individual tasks.

c) Construct a Petri net to handle the Dining Philosopher's problem, presuming 3 philosophers and 3 forks around/in the dinner table. How deadlock is avoided in your drawing?

d) Are the two transitions in Fig. 1 enabled? Can they fire synchronously? If no, what remedy do you suggest on the Petri net to handle the problem?

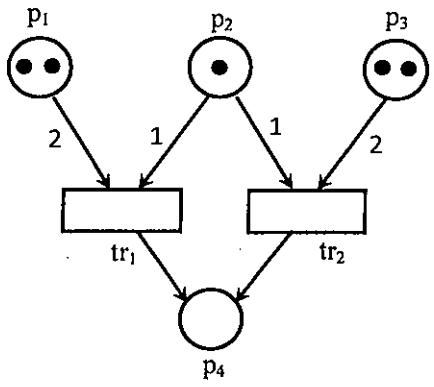


Fig.1

[5+10+5+5]

7. a) Draw the architecture of an ARM processor. List the 16 registers & their functions.

b) Show the instruction/data flow path involved in STR r_1, [r_0].

c) Write a note on:

Brain-Computer Interface for rehabilitative applications and its realizations,

OR

Cyber-physical systems: scope and importance.

[8+6+11]