M.E. Electronics and Tele-Communication Engineering
First Year Second Semester Examination, 2025

Digital VLSI Circuits (NV)

Time: 3 Hours **Full Marks: 100**

PART - I (70 marks)

All parts of the same question must be answered together

Answer 1 Question from each section, up to 5 sections MAX [14x5 =70]

Section 1: Logical Effort

1. Derive the expression for the delay of a logic gate using the Logical Effort Model. Clearly explain the role of: Logical Effort (g), Electrical Effort (h), Parasitic Delay (p). Also, define the assumptions under which the Logical Effort Model is valid.
2. Explain why the inverter has the minimum logical effort among all logic gates. Derive its logical effort from first principles, considering symmetric rise/fall times.

Section 2: Setup and Hold Time

1. Explain the concepts of **setup time** and **hold time** in flip-flops with the help of suitable timing diagrams. Why are these constraints critical in synchronous digital circuits? Also, explain the consequences of violating the setup and hold time requirements on circuit operation.
2. Describe the various techniques used to mitigate **setup time** and **hold time** violations in digital circuits. Discuss at least **three methods** in detail with examples, highlighting their advantages and limitations.

Section 3: Wire and interconnects

1. Explain the role of **interconnects (wires)** in digital VLSI circuits. Discuss how **wire resistance (R)**, **capacitance (C)**, and **inductance (L)** affect the performance of high-speed digital circuits. When can inductance be ignored in wire modeling?

[Turn over

2. Explain the concept of **crosstalk** in digital circuits. How do **interconnect parasitic** lead to crosstalk noise? Discuss at least **two techniques** to minimize crosstalk in VLSI design.

Section 4: Pipeline

1. Explain the principle of **pipelining** in digital circuits and computer architecture. Discuss the trade-offs between Throughput, Latency, and Hardware complexity. Also, explain why pipeline **hazards** occur and classify them with examples.
2. Describe the following pipeline hazards in detail with suitable examples: Structural Hazards, Data Hazards, and Control Hazards. Also, discuss **techniques** to resolve or minimize each type of hazard.

Section 5: FSM

1. Explain the differences between **Mealy** and **Moore** finite state machines. Draw a block diagram for each and explain their advantages and disadvantages with respect to: Speed, Complexity, and Output timing.
2. Design a **sequence detector FSM** that detects the sequence `1011` in an incoming serial bit stream (overlapping sequences allowed).(a) Draw the **state diagram**. (b) Write the **state transition table**. (c) Derive the minimized Boolean equations for the next state and output logic.

Section 6: Combinational Circuit Design

1. Explain the differences between **combinational** and **sequential** circuits with examples. Design a combinational circuit that takes a 3-bit input and outputs '1' if the number of 1's in the input is **odd**, otherwise outputs '0'. Draw the truth table, Karnaugh map, minimized Boolean expression, and logic diagram.
2. Design a **4-bit magnitude comparator** that compares two 4-bit numbers A and B, and generates the following outputs: A > B, A = B, and A < B. Provide the truth table, derive the logic expressions, and explain the design approach.

Section 7: Data path

1. Design a **4-bit magnitude comparator** using **carry lookahead** techniques for high-speed operation. (a) Derive the Boolean expressions for outputs A > B, A = B, and A < B. (b) Draw the circuit diagram. (c) Discuss how this design improves speed compared to traditional comparator designs.
2. Design a **4-input parallel adder** (i.e., sum of four binary numbers) optimized for speed. (a) Explain different design strategies such as **carry-save adders (CSA)** and **Wallace Tree structures**. (b) Derive the required logic expressions and show the block diagram. (c) Analyze the delay and area of your design.

Section 8: Power Distribution Network (PDN)

1. Explain the significance of power distribution networks (PDN) in large-scale digital circuits. Discuss the main challenges in PDN design, such as: IR drop, Electromigration, and L(di/dt) noise (dynamic voltage drop). Propose methods to mitigate each of these issues.
2. Describe the structure of an on-chip power grid in a modern VLSI chip. Derive the relationship between **metal width**, **resistivity**, and **voltage drop** in the power grid. Explain how **decoupling capacitors** help stabilize the PDN.

Section 9: Clock Distribution Networks

1. Define **clock skew** and **clock jitter**. Explain how these affect the performance and reliability of digital systems. Discuss at least two techniques for minimizing clock skew in large digital chips.
2. Explain the procedure of **Clock Tree Synthesis (CTS)** in the physical design flow of VLSI circuits. Given a netlist with 16 flip-flops, describe the steps for CTS to minimize: Clock skew, Insertion delay, and Power. Provide a block-level diagram of the synthesized clock tree.

Ex/PG/ETC/PC/T/122D/2025

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(Use Separate Answer Script for each part)

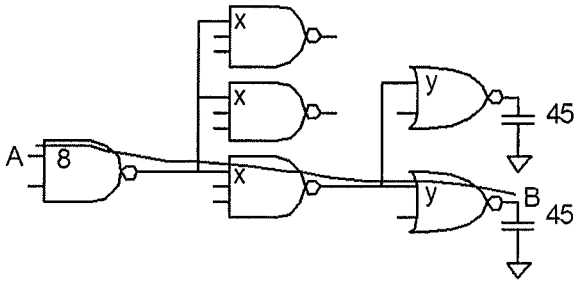
PART-II (30 marks)

Answer any 2 from the 3 questions [each comprises: CO1, CO2 & CO3]

*All parts of the same question **must** be answered together.*

Q1.a Discuss what is Branching Effort using a representative logic circuit diagram, and hence discuss how it is useful in computing the Path Delay. 5

Q1.b For the highlighted path in the circuit below, derive the estimated Minimum Path Delay using Logical Effort technique, and hence size the NAND3 and NOR2 gates. 10



Q2.a Discuss how Clock Gating and Dynamic Voltage Scaling might be used to reduce power consumption in digital VLSI. Why do we need Level Converters? – explain with suitable diagram. 8

Q2.b Estimate the dynamic power consumption of an IC chip comprising 500 million MOSFETs in a 1.1 V 65 nm process ($\lambda = 25$ nm and channel lengths=50 nm), having clock frequency of 1 GHz. Note that there are 50 million logic transistors with average width of 15 λ and activity factor of 0.15, and there are 450 million memory transistors with average width of 4 λ and activity factor of 0.04. Further, it is given that each transistor contributes 1 fF/μm of gate capacitance and 0.8 fF/μm of diffusion capacitance. Neglect wire capacitance and short-circuit current. 7

Q3.a Compute the Logical Effort of the following gates with suitable diagram and explanation: (a) NAND3, (b) NOR2, (c) XOR2, (d) INV_4x. Derive corresponding Parasitic Delays (p) of the gates? 10

Q3.b What are the various sources of Static Power Dissipation in digital circuits? 5