Ref No: Ex/PG/ELE/PE/T/115D/2025

MASTER OF ELECTRICAL ENGINEERING 1ST YR 1ST SEMESTER EXAMINATION, 2025

SUBJECT: - DESIGN & APPLICATION OF EMBEDDED SYSTEM

Use separate sheets for each part

Part-I (50)

Time: Three hours | Full Marks: 100

	Answer question:-1 any two questions from the rest	
1.	***Answer any four:-***	
	a) Explain the significance of (W/L) ratio and speed-power product parameter of typical CMOS logic gate in VLSI technology.	
	b) What is cross talks and explain how it affects the performance of wire in VLSI fabribation?	
	c) Explain the advantages of multiple threshold CMOS gate.	
	d) Discuss in brief the differences between Carry Look ahead adder and Carry Select adder, showing necessary function diagrams, computional complexity	
	e) Distinguish the operation between the permanently programmed and reconfigurable FPGA.	
	f) Explain the term 'Event driven simulation', 'Simulation time wheel'.	4 X 5=20
2.	a) Illustrate different methods of routing by programmable interconnect systems. Explain the basic difference between SRAM based and CMOS logic gate based Lookup table. Explain the operation of "Antifuse and Flash element which can be used for configuring logic elements in FPGA.	
	b) Given a two input lookup table with input a and b, write the lookup table contents for these Boolean functions: i) a AND b ii) NOT a iii) A XOR b	9+6
3.	a) What is meant by logic optimization phases in logic synthesis process?	
	b) What are the opbectives of technology-independent logic optimization? Illustrate logic suitable for factorizon method.	

[Turn over

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	c) Distinguish between technology-dependent and technology-independent logic optimization method. Doses FPGA based design provide technology-dependent logic optimization solution? Give reasons.	
4.		5+5=5
	a) Explain the performance of sequential logic circuits can be analyzed with important delay parameters, showing waveform.	
	b) Explain why two phase clocks are advantageous than single phase clock.	
	c) What does the clock skew mean? Explain why it is important.	
5.		5+5+5
	a) What is meant by critical path delay in logic network? How this delay can be minimized?	
	b) State the advantages for adding hierarchy and concurrency to the state machine model showing state diagram.	
	c) Write the sequential programming language pseudo code for elevator unit control system.	5+5+5

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M. E. ELECTRICAL ENGINEERING 1ST YEAR 1ST SEMESTER EXAMINATION, 2025

SUBJECT: - DESIGN AND APPLICATION OF EMBEDDED SYSTEMS

Full Marks 100
(50 marks for each part)

Time: **Three hours**

No. of Questions	PART II	Marks
1.	Present various methods of classifications of embedded systems.	10
	OR	
	a) Define MTBF and MTTR of embedded systems. How is availability of a system depend on MTBF and MTTR?	6
	b) What is NRE cost? How is this related to the types of processors?	4
	[CO1-K1]	
2.	Answer any TWO:	
	a) (i) Compare the architectures of datapath and controller for general purpose and single purpose processors.	7
	(ii) Which type of processors contain MAC operations? What is the benefit of using such operation?	1+2
	b) (i) How do you implement a basic AND gate using array of transistors placed over a substrate?	5
	(ii) What is an Antifuse? How does it work? Where is it used?	5
	c) Implement the Boolean expression $Y = \Sigma\, m(0, 5, 7)$ in Sum-Of-Product (SOP) form using a diode-based two-dimensional structure with programmable switch. Draw the schematic diagram neatly and explain your solution. **[CO2-K2]**	10

3.	Answer any ONE:	10
	a) What is an IP core? What are the variants of IP core found in the area of embedded systems? Explain each of them with their respective merits and demerits?	
	b) What is SoC? Explain the building blocks of SoC. In what ways are the SoCs different from a conventional IC-based structures?	
	[CO3-K3]	
4.	Write short note on (any ONE):	10
	a) Dynamic Power Management (DPM) and Dynamic Voltage Scaling (DVS) in the development of embedded system.	
	b) CAD based design flow for implementing a configurable hardware using SPLD/CPLD/FPGA	
	[CO4-K4]	