Department of Instrumentation and Electronics Engineering

1st year, 2nd semester M.Tech Examination, 2025

Subject: Design of Digital CMOS Integrated Circuits

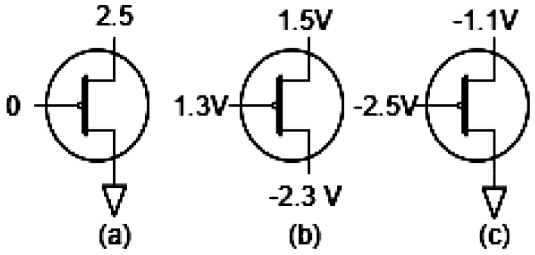
Time: 3 hours **Full marks:100**

MODULE-1

*Answer any **Four*** $4\times 10 = 40$

1. a) What are the different generations of IC? What are the different steps a typical IC fabrication process consists of ? 2+3
   b) Consider an NMOS transistor with Vth=1V is operated in the triode region with small value of Vds. With Vgs=1.5V it is found to have a resistance $R_{ds} = Ron = 1Kohm$. What value of Vgs is required to obtain R_{ds}=200 ohm? Find the corresponding resistance values obtained with a device having twice the value of W. 5

2. a) Write the use of SiO2 as a passivating layer. For a controlled doping in a narrow gate region, which doping technique should be used and why? 2+4
   b) Determine the bias state for PMOS transistors in the following diagram where Vth=-0.4V 4



3. a) What is the function of photoresist in the fabrication process? State differences between positive and negative photoresist. 2+2
   b) What are BiCMOS gates? Describe the basic steps in MOS fabrication process with suitable diagram. 6

4. a) In an n-channel MOSFET with a metal gate electrode, the original gate metal is replaced by a metal with a smaller work function. Explain qualitatively the effect on the threshold voltage. 3
   b) How do the gate-source capacitance of a MOSFET vary with gate to source voltage? Explain. 3
   c) What is channel pinch off? How does the drain current in a MOSFET vary beyond the pinch-off point? 4

5. a) What is interstitialcy? Give an example of a suitable dopant atom in Silicon lattice site. 4
   b) What is thermal diffusion? How it is carried out? 6

MODULE-2

*Answer any **five*** **5× 10 = 50**

5. a. It is not customary to shuffle the NMOS and PMOS in pull-down and pull-up network in a CMOS inverter "-Justify your answer 4

b. Show that in a CMOS inverter for symmetric switching requires, $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_p$ for all practical purposes, where, $\mu_p = 230\ cm^2/V.s$ and $\mu_n = 580\ cm^2/V.s$. 6

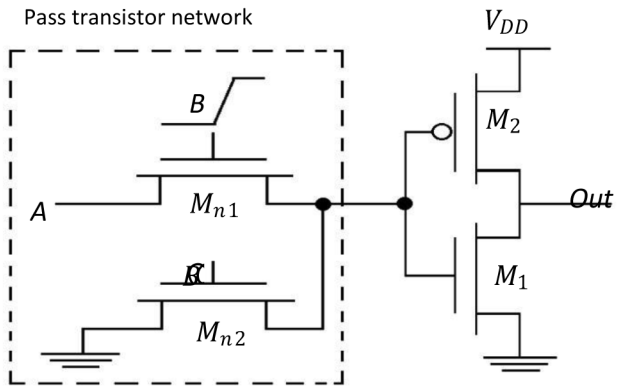
6. a) Consider a CMOS inverter circuit with the following parameters: V_{DD}=3.3V, $V_{TO,n}$=0.6V, $V_{TO,p}$=−0.7V, k_n=200uA/V^2,k_p=80uA/V^2. Calculate the noise margins of the circuit. 7

b) How the switching threshold in a CMOS inverter shifts when $\frac{k_n}{k_p} > 1$. Show using suitable voltage-transfer characteristics curve. 3

7. For a simple CMOS inverter with a power supply voltage of VDD= 5V, determine the fall time τ_{fall} , from $Vout = V90\% = 4.5$ to $Vout = V10\% = 0.5$. Use both the averngе-current method and the differential equation method for calculating τ_{fall}. The output load capacitance is 1pF. The NMOS parameters are given as; 10

$$\mu_n C_{ox} = \frac{20\mu A}{V^2}$$
$$\left(\frac{W}{L}\right)_n = 10$$
$$V_{r,n} = 1.0V$$

8. Consider the circuit of the given figure:



$V_{DD} = 2.5V$

$(WTL)_2 = 1.5um/0.25um$

$(WTL)_1 = 0.5um/0.25um$

$(WTL)_{ni} = 0.5um/0.25um$

$k_n' = 115uATV^2, kp' = -30uATV^2$

Assume the inverter switches ideally at V_{DD}/2, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem. Consider Vtn=0.43V and Vtp=0.4V for the network. 5+5

a. What is the logic function performed by the circuit?

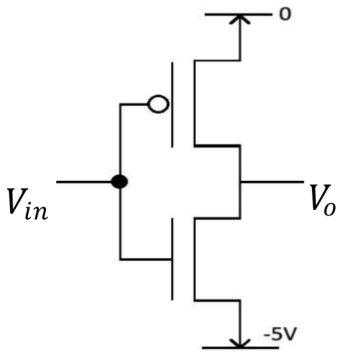
b. Explain why this circuit exhibits non-zero static dissipation.

9. a) Consider the following Boolean Expression: $\boldsymbol{Z = \overline{(A + B + C)\,(DE)}}$ 5

Calculate equivalent driver $\left(\frac{W}{L}\right)$ ratio of the pull-down network if for all NMOS transistors. $\left(\frac{W}{L}\right)_n = 10$. Draw a CMOS equivalent circuit for the expression.

b) Suggest a design technique for large fan-in circuits to reduce propagation delay in a CMOS inverter with a suitable example. 5

10. Consider the circuit of the given figure: 10



The threshold voltage $|V_T|$ for each transistor = 2V. What should be the range of input voltage V_{in}, for the circuit to work as an inverter. Analyse the operation of the circuit to estimate the output voltage Vo.

MODULE-3

*Answer any **one*** *10x1=10*

11. a) What are the various types of physical defects that can occur in a semiconductor chip? n what ways do these physical defects lead to electrical faults within the chip? How are these electrical faults further manifested as logical faults during chip operation? 5

b) Explain the relationships between physical defects, electrical faults and logical faults using a simple NOR 2 logic 5

12. Describe the essential circuit modules for built-in self-test design 10