# NANODEVICES AND THEIR APPLICATION IN CIRCUITS WITH EMPHASIS ON CIRCUIT RELIABILITY AND STABILITY

**THESIS**

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[2]. **Arpita Ghosh**, Amit Jain, S.Gharami and Subir Kumar Sarkar, "Small-signal model for Single electron transistor", *Jour. of Computa. Electro.*, Springer 2017, Vol. 16, Issue 2, pp 296–306, , June 2017,doi.org/10.1007/s10825-017-0971-1.

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[4]. **Arpita Ghosh**, Amit Jain, N.B. Singh and Subir Kumar Sarkar, "Design and Implementation of SET-CMOS hybrid half subtractor", *INDICON 2014*,Pune, doi: 978-1-4799-5364-6/14/$31.00 ©2014 IEEE**.**

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**Book Chapter**

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[2]. **Arpita Ghosh**, Amit Jain, N.B. Singh and Subir Kumar Sarkar ,"A Comparative Study of Single electron threshold logic based and SET-MOS hybrid based half subtractor", *Computational Advancement in Communication Circuits and Systems,Proc.of ICCACCS* 2014,*Lecture Notes in Electrical Eng.*vol. 335,Springer,pp 367-373,18 March 2015 ,ISBN 978-81-322-2273-6.

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7. Presented a paper entitled “Single Electron Threshold Logic Based Feynman Gate Implementation”, in 2nd*IEEE Int. Conf. on Research in Computational Intelligence and Comm. Net. (ICRCICN*) 23rd-25th September 2016, RCCIIT, Kolkata.

8. Presented a paper entitled “Comparative Study of Single electron Threshold Logic Based and SET-CMOS Hybrid Based 1 Bit Comparator” in *Int. conf. on Computational Science and Eng. (ICCSE*) 4th-6th October 2016,RCCIIT, Kolkata.

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11. Presented a paper entitled “3 to 8 Decoder Implementation using Single Electron Threshold Logic (SE-TL) for Low Power Computing”, in *ETAEERE,* SMIT, Sikkim.

12. Presented a paper entitled, “Five input majority gate implementation with Single electron Nanoelectronic Device.” in, *ICCDC*, Haldia Institute of Technology, Haldia.

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# CERTIFICATE FROM THE SUPERVISOR

*This is to certify that the thesis entitled* ***"Nanodevices and Their Application in Circuits with Emphasis on Circuit Reliability and Stability"*** *submitted by* ***Smt. Arpita Ghosh,*** *who got her name registered on* ***22/01/2016*** *[****D-7/E/36/16****] for award of Ph.D. (Engg.) degree of Jadavpur University is absolutely based upon her own work under the supervision of* ***Prof. Subir Kumar Sarkar*** *and that neither her thesis nor any part of the thesis has been submitted for any degree/ diploma or any other academic award anywhere before.*

_____

[Prof. Subir Kumar Sarkar]

*Dedicated to*

*My parents*

*Mrs. Swati Ghosh*

*Mr. Subrata Kumar Ghosh*

*For their constant love,support and motivation*

*&*

*My husband*

*Mr. Pritam Jana*

*For his cooperation and encouragement*

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*July, 2018* *(Arpita Ghosh)*

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# ABSTRACT

The ever increasing demand of miniaturization to support the advancement of the technological progress seeks attention towards the devices beyond the MOS technology as it is equipped with the different short channel effects in the sub-nanometer regime. Among the different nanodevices the Single Electron Device (SED) is being studied extensively by the researchers to utilize its unique features for replacing the conventional MOS completely or partially. Research work in this domain is mainly carried out by fabrication, characterization of the different SEDs and the circuit design aspect of the technology. The fabrication of the device is an expensive as well as a very time consuming affair. The circuit design area of Single electron Technology demands the equivalent models along with the simulation software platforms for testing. The aim behind doing so is the reduction of time constraints and predicting the circuit behavior under different parameter variations but in a cost effective way.

The simulation of the Single electron Transistor (SET) based circuit implementation necessitates equivalent model of the practical SET. Here in this thesis the structure and development of the Macro Model to support practical SET functionalities is portrayed with necessary simulation results and comparisons with previously proposed models. The model is established by designing two SET based benchmark circuits such as inverter and the Multi-peak negative-differential-resistor. The linearization of the input output relationship for a particular device is often required to properly characterize the designed circuits in presence of small-signal. The SET lacks of the development of any small-signal model. The investigation of the frequency dependence of associated intrinsic and extrinsic parameters is carried out. The effects of the parasitic components on the device small-signal parameters are also evaluated.

***Abstract***

The circuit design side of SED includes the details of the circuits constructed by the Threshold Logic Gates (TLGs) implemented with Single Electron Tunneling Technology (SE-TLG). The five input majority gate circuit and the function implementation using Programmable Logic Array is presented with SE-TLG approach. Both the circuits are simulated with the widely accepted SED simulator SIMON. The computation of the related power dissipation and delay is elaborated. These circuits facilitate with extremely low power consumption in the range of pico-Watts and nano-scale size. The partial replacement of the MOS in CMOS technology accommodates the strengths of MOS and SET both. The co-simulation of SET-CMOS based circuit is done with Tanner SPICE by using SPICE compatible equivalent model of both. Two circuits namely half subtractor and a two-bit binary multiplier are implemented with this hybrid approach and the simulated results, power consumption are furnished. Moreover a comparative analysis has been demonstrated between the conventional CMOS, SE-TLG and SET-CMOS based comparator implementation.

While designing a circuit with any technology the performance of that particular circuit is evaluated with the analysis of circuit reliability and stability. The reliability of a circuit is a severe issue to be taken care of as unreliable operation of a circuit leads to the erroneous output. For the SEDs the background charge results in circuit malfunction. The randomly distributed charges are taken into account for reliability determination of the designed SE-TLG based PLA circuit. The effect of the island shape and size on reliability of the same circuit is also investigated. Another method of reliability analysis is also deliberated for a SE-TLG combinational circuit using combined MC and Probability Transfer Matrix. The results of the combined method have been compared with the results of purely MC based method of reliability assessment. The stable operation of a SED indicates no tunneling of electrons which implies zero tunneling current or the Coulomb Blockade state, provided the temperature is 0K and co-tunneling is absent. The circuit stability of the SE-TLG based PLA and an inverter circuit is

studied with varied input combinations. The parametric variation effects on the circuit stability is also studied. Finally the stability analysis of the hybrid SET-CMOS based inverter circuit is elaborated.

As a whole the thesis familiarizes with the development of Macro model and small-signal model of SET, circuit design and testing of several important circuits with SE-TLG as well as SET-CMOS approach. The designed circuit performance is also examined with the corresponding reliability and stability analysis.

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# *LIST OF ABBREVIATIONS*

| | |
|---|---|
| BSIM | Berkeley Short-channel IGFET Model |
| CB | Coulomb Blockade |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| DIBL | Drain Induced Barrier Lowering |
| EDA | Electronics Design Automation |
| EKV | Enz-Krummenacher-Vittoz |
| KOSEC | Korea Single Electron Circuit Simulator |
| MC | Monte Carlo |
| ME | Master Equation |
| MIB | Mahapatra-Ionescue-Banerjee |
| MOS | Metal-Oxide-Semiconductor |
| MOSFET | Metal-Oxide-Semiconductor Field Effect Transistor |
| MP-NDR | Multi Peak NDR |
| NDR | Negative Differential Resistance |
| NM | Noise Margin |
| PLA | Programmable Logic Array |
| PTM | Probability Transfer Matrix |
| SCE | Short Channel Effect |
| SED | Single Electron Device |
| SE-TLG | Single Electron –Threshold logic Gate |
| SEEL | Single Electron Encoded Logic |
| SET | Single Electron Transistor |
| SET-CMOS | Single Electron transistor- Complementary Metal-Oxide-Semiconductor |
| SETT | Single Electron Tunneling Technology |
| SIMON | Simulation of Nano-Structure |

| | |
|---|---|
| SPICE | Simulation Program for Integrated Circuit Emphasis |
| TLG | Threshold Logic Gate |
| ULSI | Ultra Large Scale Integration |
| VCCS | Voltage Controlled Current Source |
| VTC | Voltage Transfer Characteristics |
| VLSI | Very Large Scale Integration |

# Chapter 1

# INTRODUCTION AND ORGANIZATION OF THE THESIS



## 1.1 Introduction

The technological up gradation is possible with improvement of operational speed, packing density and extremely low power consumption of the devices used for present electronic applications. The journey of the compact size in the form of Integrated Circuits (IC) started in 1959 by Jack Kilby [1.1]. Higher packing density is achievable through a continuous and rigorous reduction in the dimension of the conventional devices. The main catalyst behind the modern semiconductor industry's growth is the scaling [1.2]. The speed and the power consumption of the device increase with reduced dimensions, while production cost per unit is slashed down. The antagonistic scaling[1.3]-[1.4] of MOS devices underneath a certain limit of 100nm originates several kinds of Short Channel Effects (SCEs)[1.5]-[1.6], Drain Induced Barrier Lowering (DIBL)[1.7], Gate leakage[1.8], punch through, degradation of high field mobility, etc which in turn affects the operation of the MOS in an undesirable way. But according to Moore's law [1.9] the scaling down of MOS must go on to support the required double numbered transistors in every 18 months. The classical nano-CMOS approach with high-k dielectric materials[1.10], Silicon-on-insulator (SOI)[1.11] , metal gates and the different non classical approaches such as Dual Gate MOS [1.12], Fin-FET [1.13]may support MOS to go beyond

100nm but the limit is up to 10nm[1.14]-[1.15](known as the showstopper region of CMOS). It suggests that the life of the semiconductor technology beyond CMOS is going to be dominated by the emerging nanodevices. The Single-Electron Devices (SEDs)[1.16]-[1.19], Carbon Nanotubes (CNTs)[1.20]-[1.22], Resonant Tunnel Diodes (RTDs)[1.23], Rapid single quantum flux[1.24] are the different candidates of emerging nanotechnology .

In this thesis, the main focus has been given to the SEDs. The benefits of using Single Electron Tunneling technology(SETT) [1.25] are the low energy consumption using a countable number of electrons, compact size, high speed (can be reached in the order of 0.1fs to 1fs), high sensitivity, extremely high on-chip integration density, simplified circuit, simple principle of operation and straightforward hybridization with conventional CMOS circuits.

In 1951 Coulomb repulsion, well-known as Coulomb blockade (CB) due to low bias current suppression [1.26] was explained by C. J. Gorter. The 'Orthodox' theory of Single electron tunneling was introduced by D.V. Averin and K.K. Likharev [1.27] in 1985. Fulton and Dolan [1.28] in 1987 familiarized with the Single Electron Transistor (SET), whereas Nakazato et al. [1.29] in 1993 explained Single electron memory. The room temperature operability of SET was experimentally proved by Takahashi et al.[1.30] in 1995. The possibility of fabrication of SEDs on SOI was demonstrated by Ali and Ahmed [1.31] in 1994. Saitoh and Hiramoto [1.32] in 2002 explained that with reduction in dot size energy level separation increases. The review of coupled quantum dots was done by van der Wiel et al.[1.33] in 2002.

The SETT has several merits over the conventional CMOS technology starting with greater scaling which leads to higher integration. The implemented circuits with SETT consume a reduced amount of power dissipation than CMOS based circuits. Having the simple physical structure formed by mainly a quantum tunnel junction, the fabrication is

done in many ways. Unlike MOSFET, current conduction in SET is due to electron tunneling through the tunnel barrier. A tunnel junction is the elementary part of a SED. This tunnel junction is constructed by inserting an extremely thin insulating material in between the two conducting layers. The formation of SET is accomplished with two such tunnel junctions placed in series. The piece of the conductor in between the two tunnel junction actually works as the island. The discrete natured charge transportation takes place in these SED devices in place of continuous like MOSFETs. A third terminal coupled to the island through a thick dielectric is the gate. According to the coupling of gate, SET can be either Capacitive (C-SET) [1.34] or Resistive (R-SET). As R-SET fabrication has suffered from practical realization issues [1.35] the work presented in this thesis is limited to C-SET devices only.

The Orthodox theory regulates the rules of electron tunneling through the tunnel junction. The quantization of electron energy is ignored in this theory. According to it firstly, the junction resistance should be much larger than the quantum resistance ($R_Q \approx h/q_e^2$) shown in equation (1.1), where h is the Planck's constant ($6.62 \times 10^{-34}$ J-s) and $q_e$($1.602 \times 10^{-19}$Coulomb) is the elementary charge of the electron.

$$R_T >> R_Q \approx 25813\Omega \tag{1.1}$$

Secondly, the charging energy ($E_C = q_e^2/2C_{sum}$) should overcome the thermal energy $k_BT$ (presented in equation (1.2)) where $k_B$ is the Boltzmann's constant ($1.38 \times 10^{-23}$ J/K),

$$E_C >> k_BT \tag{1.2}$$

T is the temperature, $C_{sum}$ is the total capacitance of the circuit. If the above two conditions are followed then only the charging effects can be observed. The distinct properties of any SED are the Coulomb Blockade and the Coulomb oscillation.

Most of the popular simulation software for SED is Monte Carlo tool [1.36]-[1.38] based which requires a huge amount of time for circuit simulation. According to [1.39] if the load capacitor value is made sufficiently large then the current-voltage characteristics of a SET can be made independent of the adjacent SETs. The extensive probability calculations needed for the electron tunneling of entire circuit can be avoided with this condition. The formulation of compact models[1.40]-[1.43] is thus essential for SEDs. The flexible and accurate SET simulation tools[1.44] for quickly modifying and updating SET models makes possible the verification, characterization, and testing of new ideas of SET circuits.

The prototyping of a device is possible by studying the device characteristics in details. The nonlinear behavior of the drain current with respect to applied terminal voltages can be linearized for the specified low amplitude of the applied AC signal. By this, the higher order terms of the Taylor series expansion of the device characteristic equation is linearized. As a result, the different input-output voltage and currents are related by means of linear equations. The small-signal model[1.45]-[1.47] of a device is thus important for getting the linearized expressions of the device current-voltage parameters. The actual attributes of the device can be counterfeited by designing the equivalent small-signal model of the device. The frequency characteristics of the device can also be verified under the fluctuation of device small-signal model [1.48] intrinsic and extrinsic parameters.

Apart from the equivalent SET modeling, another aspect of the Single Electronics is the application domain in which different digital and analog circuit design and implementations are studied. The circuit design with SEDs in earlier days followed mainly CMOS-type SET design [1.49]-[1.50]style. This design style is easy to implement as it utilizes the prior CMOS based circuit design concept and the SETs are used in such a fashion that they imitate the behavior of conventional p-MOS and n-

MOS. For full utilization of the unique features, of SETT based Encoding Logic is used. Few of the formerly reported literature also suggested the applicability of threshold logic gate (TLG) concept for SEDs. The use of TLG concept[1.51] along with the SETT introduces a new set of logic gates which can be further used to form various kind of Single Electron-Threshold Logic Gate (SE-TLG)[1.52]-[1.55] based large circuits. But the switching activities of the TLGs introduce feedback and feedforward effects. The output of TLG behaves as an input to the next stage as in a network generally output of a TLG drives another TLG. Thus a portion of voltage level also affects the junction of the TLG and modifies the threshold value. This kind of erroneous behavior can be avoided by the addition of a static buffer [1.56] to the back end of all the TLGs. The extra capacitive load is added to the output node of TLG by adding a static buffer. The parameters are thus adjusted to reduce the feedback effect[1.57].

Hybridization of SET with conventional CMOS accommodates the functionalities of both the technologies. Using the enhanced features ,the drawbacks of both the technologies can be compensated. Different type of SET-CMOS based [1.58]-[1.61] hybrid structures and related circuit design styles are also reported here.

Whenever any circuit is designed, corresponding performance analysis becomes one of the prime concerns to accept the design style in future applications. The two prime factors for judging the performance of implemented circuits with SEDs are the reliability[1.62]-[1.65] and stability analysis [1.66]-[1.68]. Due to the sensitivity towards background charges (BC) [1.69] generated during the fabrication procedure, SED faces fluctuation in node charges and in turns in node voltages also. It affects the proper functioning of the SEDs. While determining the reliability of the designed circuits this background charge factor is to be accounted. On the other hand, the charge fluctuations in the circuit for a particular combination of bias voltages affect the change in free energy.

As the tunneling rate and the tunneling current of SED are associated with the change in free energy it also becomes a deciding factor for system stability.

A Modified Macro model [1.70] for SET is presented here with its detailed structure, response, and characteristics verification. Comparison with the existing models is also included in the work. Justification of the proposed model is also provided by furnishing the results of SET based circuit simulation using the model.

The thesis also comprehends the detailed structure of SET small-signal model linearized equations of terminal voltage and currents and different small-signal parameters. Frequency dependence of the related intrinsic and extrinsic circuit components are checked and illustrated.

The research progression on the field of SETT is mainly categorized into two types-

A. Fabrication of SEDs[1.71]-[1.75]

B. Circuit Design and Implementation with Single Electronics

The circuit design and realization aspect of the SETT is deliberated in this thesis with SE-TLG and SET-CMOS approach. For circuit design purpose mainly SED is combined with TLG concept to reveal the uniqueness of SEDs thoroughly. The design employment, and simulation results of the circuit a Majority Gate with five inputs and Programmable Logic Array (PLA) circuit is presented in this thesis. The constructional details and simulation issues of hybrid SET-CMOS based half subtractor and binary multiplier circuit is demonstrated in the work. The comparison of SET-CMOS based design approach with SE-TLG based approach is also furnished.

The performance assessment of the designed SE-TLG based circuits has been accomplished through the circuit reliability and stability analysis. The SET-CMOS circuit stability analysis is also demonstrated for the designed circuit.

## 1.2 Organization of the thesis

This thesis is organized in total six different works related to the SED based nanodevices. The motivation and the objective of the thesis are being elaborated in the first part. The application of SED in circuit realization needs attention towards different equivalent models. The establishment and technical details of the two such SET models are demonstrated in the next two chapters. After that the thesis moves on towards the circuit design aspect with SE-TLG and hybrid SET-CMOS approach. The performance analysis of the designed circuits by evaluating their corresponding reliability and stability are furnished in the next two chapters. Finally the conclusion is drawn as per the works done. The thesis is segmented into total eight numbers of chapters. The detail of the individual chapters is furnished below.

***Chapter 2*** introduces a new Macro Model circuit for SET. The simulation of SET circuits is possible by means of Master equation(ME) based Analytical model, Monte Carlo(MC) Method based approach and Macro Model-Based approach. For small circuits, it has been surveyed that the MC and analytical method both work well. But as MC method is based on the probability calculations of the different tunnel events, with circuit size the time complexity increases proportionately and moreover, it becomes unreasonably complicated. On the other hand, ME method does not include any probability calculation related to the individual tunnel event but a set of equations are generated and solved according to the considered system state. For smaller circuits, it consumes less time than the MC method of circuit simulation but for the larger circuit complexity due to a large number of equation increases and so the time requirement. As a promising solution Macro Models are introduced which can be easily used independent of the circuit size. The time requirement is also below the previous two methods. The Macro Model of

SET is formed with the basic micro-electronics components such as a resistor, capacitor, voltage and current sources. The previously reported Macro Models of SET are not perfect in all aspects. Moreover, most of them are designed keeping in mind the ideal characteristics of SET. So this chapter elaborates a modified Macro Model representing the practical SET capabilities along with proper circuit implementation support.

***Chapter 3*** elaborates the small-signal model of the SET for the first time. The small-signal modeling is a technique to analyze and approximate the behavior of a nonlinear electronic device using linear equations. The application of AC signal with sufficiently low magnitude, ensures that the SET is driven in the linear region of operation. By determining the two-port equivalent of the SET circuit the nonlinear nature of the drain current is represented by the linearized relationship between the terminal voltage and currents. The two-port network analysis is carried out on the equivalent small-signal model to find out the different associated parameters. The related impedance, admittance parameters are analyzed with frequency variation and model parameter variation for intrinsic-SET. The model is initially developed for the intrinsic-SET after that the several parasitic elements are also taken into account to form the complete circuit in the high-frequency domain. At high-frequency, the characteristic of a device is often defined with the scattering parameters (S-parameters). The related S-parameters and effects of different parasitic elements on the S-parameters are investigated. Finally, the technique of parasitic element extraction is also discussed in this section of the thesis.

*In* ***Chapter 4*** the circuit design using SED principle is discussed. The improvisation of the circuit with the use of threshold logic concept further reduces the consumption of power even from the SET based

circuit design which follows CMOS-like structure by cutting down the number of tunnel junctions. Design and implementation of SE-TLG based circuits such as five input majority gate and PLA circuits are presented. The first one requires a single tunnel junction, thus do not require any buffered logic but the later one is designed with buffered TLG to eliminate the feedback related problems for the larger circuit (which uses multiple numbers of SE-TLGs connected one after another). Power consumption being one of the major concerns for any designed circuit is calculated for both as well. Other performance parameters of the single electron tunneling based circuits such as tunneling rate and the time delay are also evaluated.

***Chapter 5*** introduces circuit implementation with the SET-CMOS hybrid technology. SET-CMOS is the combination of SET and CMOS technology which clubs the benefits of both the technologies. The co-simulation technique and required model types are also deliberated in this part of the thesis. The detailed implementation of hybrid SET-CMOS based half subtractor circuit and a binary multiplier circuit is explained and furnished here with result verification. Finally, the comparative analysis of the hybrid SET-CMOS based design is done with the typical CMOS based and SE-TLG based circuit implementation of a circuit.

***Chapter 6*** discusses the reliability issues of the SEDs. The estimation of circuit reliability for SED circuits with different approaches is explained. The proper operation of the SED is affected by the random background charge generated in the different nodes due to the fabrication process. The erroneous output of the SEDs is basically due to the generation of these background charges (BCs). Thus different approaches related to the BC-based SED reliability are investigated. Choosing a suitable method or tool for reliability analysis for circuits designed with SEDs is illustrated with an example in a step by step manner. The MC based

simulation method has been adopted in this thesis for evaluating the reliability of PLA circuit designed using the SE-TLG based method. Another approach of reliability which uses MC method for individual gate error percentage determination and Probability Transfer Matrix (PTM) for overall reliability is also elaborated to determine the reliability of a SE-TLG combinational logic circuit.

***Chapter 7*** encompasses another important parameter of SED based circuit performance evaluation i.e. circuit stability. The condition of stability for a SED circuit is explained in this chapter. At very low drain-to-source voltage the electron tunneling rate between the junction and the island is almost negligible as a result no current flow is there. The range of voltage for which the DC current suppression occurs is known as the Coulomb Blockade (CB) gap. The CB region for which there is no current flow is mainly indicated as the stable condition of the circuit. This stability of any SED circuit can be analyzed by plotting a stability plot. The stability of the SE-TLG based circuits, such as Single electron based Inverting Buffer and PLA are discussed in details in this part of the thesis. The procedure of SET-CMOS hybrid circuit stability analysis is also highlighted here.

In ***Chapter 8*** the concluding remarks for the overall work are provided. The future aspects and scopes of research in this domain of work are also illuminated in this last part of the thesis.

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# Chapter 2

# MACRO MODEL OF SINGLE ELECTRON TRANSISTOR



## 2.1 Introduction

The improvement of the electronic devices is possible with the introduction of novel device structures [2.1], new principle of operations, use of new material properties [2.2] and scaling down [2.3] the dimensions. Conventional MOSFET technology suffers from several unwanted Short Channel Effects (SCE)[2.4] due to tremendous scaling. SETT[2.5]-[2.7] being one of the emerging nanotechnologies with extremely low power consumption, very high packing density, can be used as a substitute for MOSFET. The SED [2.8] is based on the transportation of single or a few numbers of electrons and shows a completely different kind of electrical characteristics than the MOSFET. One of the main SEDs is the Single Electron Transistor (SET)[2.9]-[2.11]. SET fabrication is a time consuming and expensive affair which is the main reason behind the development of different computer-aided tool-

based design and simulation tools. These simulation tools [2.12] for SET circuit simulation are mainly used for testing and characterizing the new ideas cost-effectively and obviously in less amount of time.

Modeling of the SET is very important for predicting the characteristics of the circuits implemented with SET. To explore the applications of SET in different circuits, it is very important to simulate the circuit using the proper equivalent model of SET. Different reported compact model is available for the simulation of single-electron circuits. There are a few available simulation software for SED such as SENECA [2.13], MOSES [2.14] SIMON [2.15] etc. Among them, MOSES and SIMON are based on the Orthodox theory [2.16].

For simulation purpose of SET based circuits mainly three approaches are adopted

1) Macro-modeling,
2) Monte-Carlo method and
3) Analytical modeling

The Monte Carlo (MC)[2.17] approach for SET simulation relies on the calculation of probabilities related to all the tunneling events of electrons onto and from the island. The process is complicated and time-consuming. Moreover, the co-simulation of SET with CMOS needs the SPICE (Simulation Program for Integrated Circuit Emphasis) compatible model of SET. But the MC-based approach is not SPICE compatible at all. The MC-based simulators available for SET simulation are SIMON, KOSEC (Korea-Single-Electron-Circuit-Simulator) [2.18], MOSES etc. Another approach apart from MC method is the Master Equation (ME)[2.19] or analytical method[2.20]. According to this method, several numbers of system states are considered and a set of equations are generated with the state change. The characteristics curves of SET are achieved by solving those state equations. The accuracy of the model is proportionate to the number of considered states. But in turns, it

increases the computation complexity and time requirement both. For small circuits, the performance of ME method is better than the MC method but it takes more time than Macro model approach while applying to the larger SET based circuits.

On the other hand, a Macro Model is an equivalent circuit developed using the basic microelectronics components such as capacitors, resistors, voltage sources and current sources. The Macro Model is solely established by solving KCL and KVL equations. No probability calculation of related tunneling events or the system state considerations is required for this. The SPICE compatible feature enables the simulation of SET-CMOS [2.21] based circuits. This approach is much faster than the previously explained two methods as it reduces the time of computation. To use the Macro Model for any SET circuit simulation SET is substituted by its corresponding electrical circuit.

In multiple SET based environment, the Macro Model or the subcircuit needs to be called.

The assumptions related to the macro modeling are:

1) The SET equivalent model can be used in a whole circuit after determination of the parameters.
2) Only through the changes of terminal voltages,the current-voltage characteristic of the SET is affected by transistors in the neighborhood.

In earlier days several macro models of SET has been reported such as Yu's model [2.22], Wu and Lin's model [2.23], Karimian's model [2.24] etc. However, all the mentioned models suffer from different kind of drawbacks and none of them has reported the characteristics that suites practical SETs. For eliminating the drawbacks of the previously proposed models the Macro Model needs to be modified further. The section 2.4 of the work explains a modified Macro Model structure for SET. The characteristics of the said model are also analyzed to justify the claimed

output. The detailed construction and the requirement of each and every related elements are described in the model formulation part sub section 2.4.1. The comparison of the previous model results with the proposed one is also presented in this part of the literature. The validity of the circuit is justified with the design of benchmarked circuits using the model.

## 2.2 Literature Survey

The rapid progress in the nanodevice fabrication process expedites the integrated circuit implementation based on SEDs. For analyzing and designing single electron based integrated circuits the demand for accurate and compact SET model is also increasing. Several such compact SET models and SET specific simulation software are reported. Among them, Fonseca et al. developed SENECA[2.13], Chen et al. proposed MOSES [2.14] and Wasshuber et al. introduced SIMON[2.15] software tool based on quantum mechanics and tunneling technology. SEMSIM[2.25] was developed by Allec et al. and SECS(Single-Electron-Circuit-Simulator)[2.26] was demonstrated by Zaradalidis and Karafyllidis in 2008. Yu et al. first introduced the SET Macro Mode[2.22] with diodes, resistors and voltage sources. Later the model proposed by Yu et al. was modified by Wu et al.[2.23] by adding two face to face diodes to nullify the current leakage between gate-to-source terminals. Further modification to Wu's model was incorporated by adding a switched capacitor based quantizer[2.24] circuit by Karimian et al. In the year 2000,Wang et al. proposed an Analytical model of SET compatible with SPICE[2.27].A transient model for SET for SPICE was also reported in 2005 by Yu[2.28]. Boubaker et al.[2.29] designed a SET SPICE model for low temperature in 2008. An HSPICE model of Single-electron turnstile was proposed by Wei et al [2.30] in 2014.Recently Jain et al.[2.31] improved the Macro model by replacing the resistor with a

voltage controlled current source (VCCS) to match the SET model with ideal characteristics of SET. But practically the characteristic of SET differs a bit from the ideal one mainly in the Coulomb blockade (CB) [2.32] region. To incorporate this practical characteristic,the Macro Model has been further modified to make it appropriate for practical SET operations. The modified Macro Model presented in this thesis is designed with four branches of microelectronic components.Among them, two newly added branches are formed with resistor, diodes and VCCSs to provide the desired result in the CB region for the ideal SET.

## 2.3 Existing Macro Models of SET

There are four existing Macro Models of SET such as models proposed by Yu et al., Wu et al., Karimian et al. and Jain et al. The details of the circuits of a pre-existing Macro Model of SET are elaborated in this section. The detailed discussion of the benefits and shortcomings of all the models and the requirement to develop or modify the models is also elaborated in the next four subsections 2.3.1, 2.3.2, 2.3.3 and 2.3.4.

### 2.3.1 Yu's Model

Line fitting and parameter based modeling are used in the Macro Model proposed by Yu et al. In this model very large interconnection among the

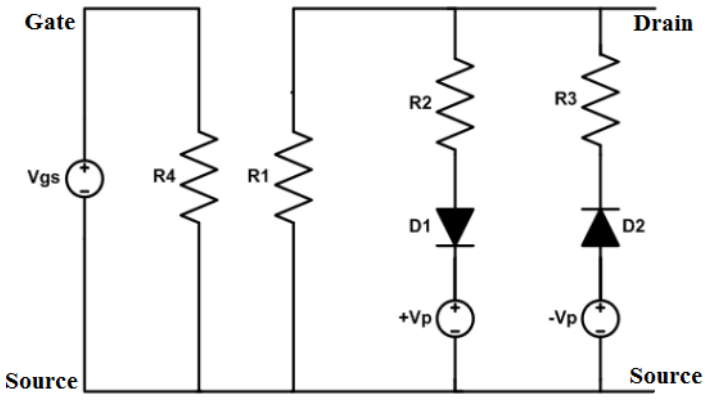


**Figure 2.1**: Macro model proposed by Yu et. al.

SETs have been assumed to treat SETs independently.

The results are obtained by simulating the equivalent circuit using KOSEC. The plotted drain characteristics of the Yu's model shows that for the different values of the gate-to-source voltages ($V_{gs}$), the $I_{ds}$ (drain-to-source current) versus drain-to-source voltage ($V_{ds}$) curves are not parallel in nature. The Yu's model is displayed in figure 2.1. It consists of two diodes D1 and D2, four resistors R1,R2,R3,R4 and the two voltage sources $+V_p$,$-V_p$.

The result of the model projected by Yu et al. has large dissimilarities between the results gathered from the well-accepted single-electron circuit simulator SIMON. According to this model, the $I_{ds}$ increases linearly with $V_{ds}$ in the CB region but it should have changed exponentially with $V_{ds}$. In the $I_{ds}$ versus $V_{gs}$ characteristics, the $I_{ds}$ baseline increases with the $V_{gs}$ value because of the leakage current between the gate and source terminal. This also enhances the amount of Coulomb oscillation [2.33].

## 2.3.2 Wu and Lin's Model

The above-mentioned drawbacks were partially removed in the model proposed by Wu and Lin. The problem related to the gate-to-source leakage current is handled in this model. This model used two ideal face

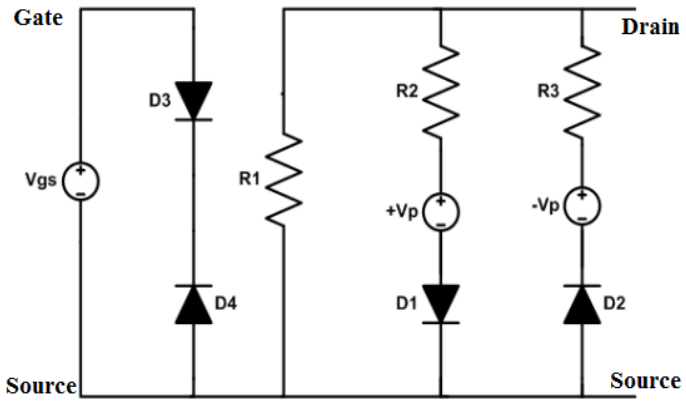


**Figure 2.2:** Macro Model of SET proposed by Wu and Lin.

to face connected diodes in place of the large valued resistor R4.

The results of the Wu & Lin's model are better than the previously proposed Yu's model. The circuit of Wu and Lin's model for SET is revealed in figure 2.2. The used model parameters are three resistors R1,R2,R3, four diodesD1,D2,D3,D4 and the two voltage sources for CB region $+V_p$,$-V_p$.

## 2.3.3 Karimian's Model

Further modification of the Macro Model was done by Karimian et al. In this model of Karimian et al., switched capacitors were used to determine the electron tunneling timing across the tunnel barrier. The proposed model of Karimian is represented in figure 2.3. The additional component is the quantizer part built with switches and a capacitor.

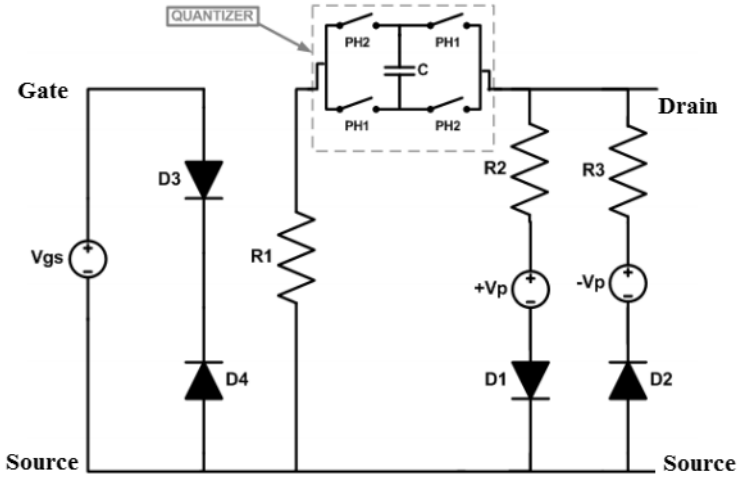


**Figure 2.3:** Macro Model of SET proposed by Karimian et al.

## 2.3.4 Jain et.al.

Recently proposed Macro Model by Jain et al. removes the shortcomings of the existing models. This model is suitable for the ideal SET. The model proposed by Jain et al. is illustrated in figure 2.4, where an extra

element g1 is added to the model in place of the resistor R1 of the previously reported model. Here g1 is the VCCS.

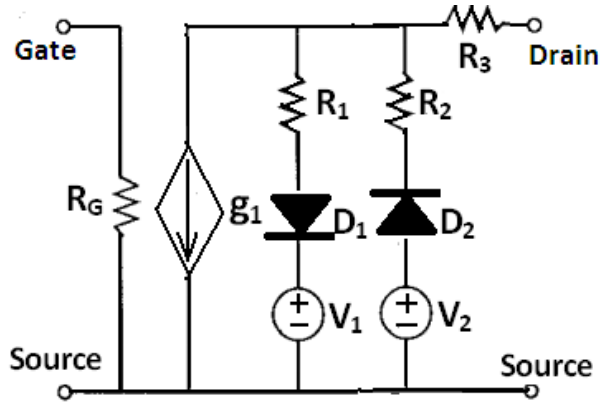


**Figure 2.4:** Macro model proposed by Jain et al.

Though several works are reported on Macro Modeling of SET none of the models generated the characteristics of practical SET. Therefore all the above-mentioned models still have some drawbacks and need further modification to achieve a more practical and accurate model.

## 2.4. New Modified Model

The modified Macro Model formulation is done with the target of making the existing SET Macro Models more practical and accurate.

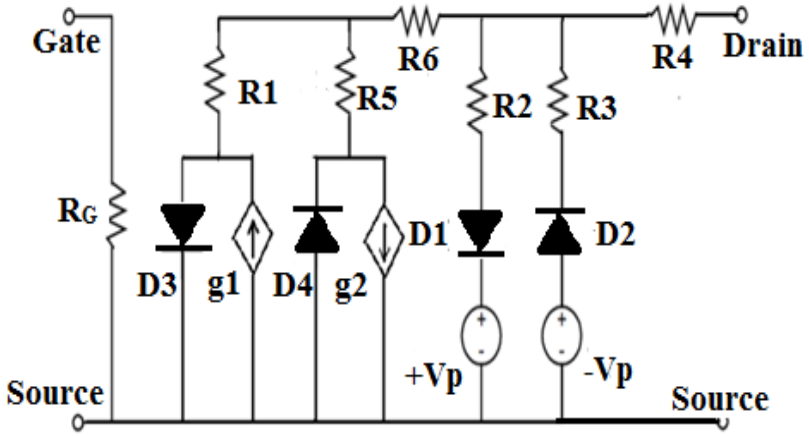


**Figure 2.5:**The proposed Modified Macro Model of SET designed with two voltage controlled current sources g1 and g2.

The structure of the newly proposed Macro Model is shown in figure 2.5. It includes total four numbers of diodes (D1,D2,D3, D4); seven numbers of resistors (R1,R2,R3,R4,R5,R6,$R_G$) and two VCCSs (g1 and g2). The detailed model structure, formulation, and working principle are discussed in the next sub-section.

## 2.4.1. Model Formulation

The formulation of the projected Macro Model of SET is done from the concept of SET drain-current characteristics. The characteristic is generally divided into two parts one is the CB region and another part is for the non-CB region. The non-CB part is designed with the D1 and D2 diodes, resistors (R2,R3) and voltage sources ($-V_p$, $+V_p$). This part designates the symmetric drain current nature which is a function of the $V_{ds}$. Whenever the value of critical voltage becomes greater than the $+V_p$ the diode D1 conducts and as a result current flows through the resistor R2. The negative part of the non-CB region of the characteristics is achieved with D1, R2, and $+V_p$. In a similar way when the critical voltage is below $-V_p$ the diode D2 conducts and current flows through the resistor R3, as a result, the positive portion of the non-CB region is attained. The main modification has been done in the CB region part. This part of the circuit is implemented using another branch comprising of D3, g1, R1 and D4, R5, g2. Here both VCCSs g1 and g2 are the functions of the $V_{gs}$. For the positive part of the CB characteristics, current flows through the resistance R5 and VCCS g1. Here D4 is bypassed. A negligible amount of current flows through resistor R1 and diode D3 of the other branch. The isolation of gate and the source is done by using a resistor $R_G$ having sufficiently high value compared to the rest of resistors present in the circuit. It restricts the current between gate and source terminal and works as an open circuit. The reverse thing happens in the negative part of the CB region. From the perspective of

the model design, the resistor R6 is not having any significance but it is required to plot the drain current. The range of CB voltage can be set using $V_p$.

The expression of the resistors R1 (denoted with RR1), R5 (denoted with RR5), R2(denoted with RR2) and R3(written as RR3) is represented below with equations (2.1)-(2.3).

$$RR1 = \left(CR1 + CR2 \times \cos(CF1 \times \pi \times V_{gs})\right) \tag{2.1}$$

$$RR5 = \left(CR1 + CR2 \times \cos(CF1 \times \pi \times V_{gs})\right) \tag{2.2}$$

$$RR2 = RR3 = \frac{CVp}{CI2 - \frac{2CVp}{\left(2 \times CR1 + CR2 \times \cos(CF1 \times \pi \times V_{gs})\right)}} \tag{2.3}$$

At different gate voltages, the parameters CVp, CF1, CR1, CR2,and CI2 are utilized to fit the drain characteristics curve of SET. The parameter CF1 is used for determining the Coulomb oscillation frequency in characteristics of $I_{ds}$-$V_{gs}$. CF1 is expressed in the equation (2.4).$C_g$ and $q_e$ are the gate capacitance and elementary charge of electron respectively in the expression (2.4).

$$CF1 = 2C_g / q_e \tag{2.4}$$

The newly added components g1 and g2 are expressed in the equation (2.5) considering the vertical shift of $I_d$-$V_{ds}$ curve with respect to the $V_{gs}$ keeping its nature intact.

$$g1 = g2 = \left(\frac{1}{(k1 \times CR1)} \times \sin\left(\pi \times V_{gs}\right)\right) \times k2 \tag{2.5}$$

CVp is the peak voltage representing the maximum range of CB region. The values of CR1 and CR2 are associated with the resistance of junction in the mega-ohm range whereas; CI2 is linked to the nano-ampere range current. The parametric values of the designed model are in accordance with reference [2.22].Through the curve fitting method, the basic equation is obtained. The approximate range of parameter values is

determined from the nomenclature of these fitting parameters as the direct calculation is not possible.

The sub-circuit code is displayed in figure 2.6, where k1, k2 are the scaling factors for adjusting the slope of drain characteristics and CVp, CR1, CR2, CF1 CR3, CR4, CI2 are the Macro Model parameters. The initialization part of the code has been done by defining the different parameter values. CR1 and CR2 are taken as $300x10^{+6}$ and $100x10^{+6}$ respectively. The CB gap is defined with CVp values i.e. starting from -0.02Volt to 0.02Volt.The value of CF1 is assumed as 40 and it is the temperature dependent parameter through $C_g$ value. Here $C_g$ is calculated as 3.2aF. The remaining resistance values are then defined.

```
.SUBCKT set 8 2 3
.param
+pi=3.14
+CF1=40
+CI2=0.2e-9
+CR1=300e+6
+CR2=100e+6
+CVp=0.02
V2 5 3 DC 0.02
V3 7 3 DC -0.02
RG 2 3 100G
RR1 13 9 R='(CR1+CR2*cos (CF1*pi*V (2, 3)))'
RR6 1 13 1
RR5 13 10 R='(CR1+CR2*cos (CF1*pi*V (2, 3)))'
RR2 1 4  R='(CVp/(CI2-2*CVp/(2*CR1+CR2*cos(CF1*pi*V(2, 3)))))'
RR3 1 6 R='(CVp/ (CI2-2*CVp/(2*CR1+CR2*cos(CF1*pi*V(2, 3)))))'
RR4 1 8 1
D1 4 5 DIODE
D2 7 6 DIODE
D3 9 3 DIODE
D4 3 10 DIODE
MODEL DIODE D (N=0.01)
g1 9 3 cur='((1/ (k1*CR1))*sin (pi*V (2, 3)))*k2'
g2 10 3 cur='((1 / (k1 *CR1))*sin (pi*V (2, 3)))*k2'
.ends
```

**Figure 2.6:** Code for New Macro-Model

## 2.4.2 Drain Characteristics of the Model

The drain characteristics of the SET are plotted according to the simulation of the designed model. For simulation purpose Tanner SPICE tool has been used and the selected model parameters are CR1=300x10$^{+6}$, CR2=220x10$^{+6}$, CI2=0.2x10$^{-9}$, CVp=0.02, Cj=1.6aF, $C_g$=3.2aF, CF1=40 and T=30K. The drain current ($I_{ds}$) is plotted with the $V_{gs,}$ for the constant $V_{ds}$ depicted in figure 2.7. The periodical oscillation of the constant $V_{ds}$ is observed from the same figure. From this drain characteristic, it can be justified that the model is producing one of the main features of SET i.e. Coulomb oscillation. If the $V_{ds}$ value is increased from 0.03Volt to 0.09Volt with an increment value of 0.02Volt, it can be seen that the amplitude of the current rises in the nano-Ampere range from 0.18 to 0.8. The range of $V_{gs}$ for the simulation purpose is taken as -0.08Volt to 0.08Volt with an increment of 0.02Volt.

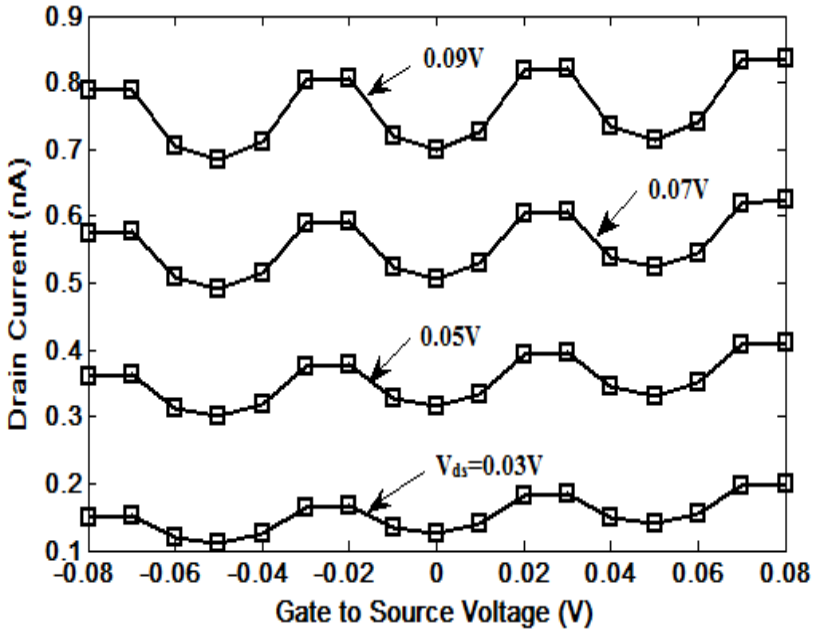


**Figure 2.7:**Drain current characteristics with $V_{gs}$ voltage for proposed macro-model.

Using the proposed Macro Model the $I_{ds}$-$V_{ds}$ characteristics has been plotted. The drain characteristics of the Macro Model with the $V_{ds}$ is

presented in figure 2.8. The range of the CB region can be easily recognized from the characteristics curve for the $V_{ds}$ value of -20mV to 20mV. The $I_{ds}$ apart from the CB region has a positive part and a negative part. According to the operation of the ideal SET, the drain current is zero in the CB region as the tunneling rate is almost zero in this region. But practically a negligible amount of current flows in the CB region as well. This current is because of the thermally activated carrier tunneling in presence of small finite temperature.

The $V_{gs}$ range considered in this simulation is from 0.0V to 0.5V.For the increasing values of $V_{gs}$, the graph moves along the Y-axis. The characteristics of the Yu's model also exhibits this kind of shift but the nature of shift was not fixed in that case. As the tunnel junctions are considered to be symmetric in nature i.e. both CR1 and CR2 have the same value, the drain current monotonically increases or decreases beyond the CB part.

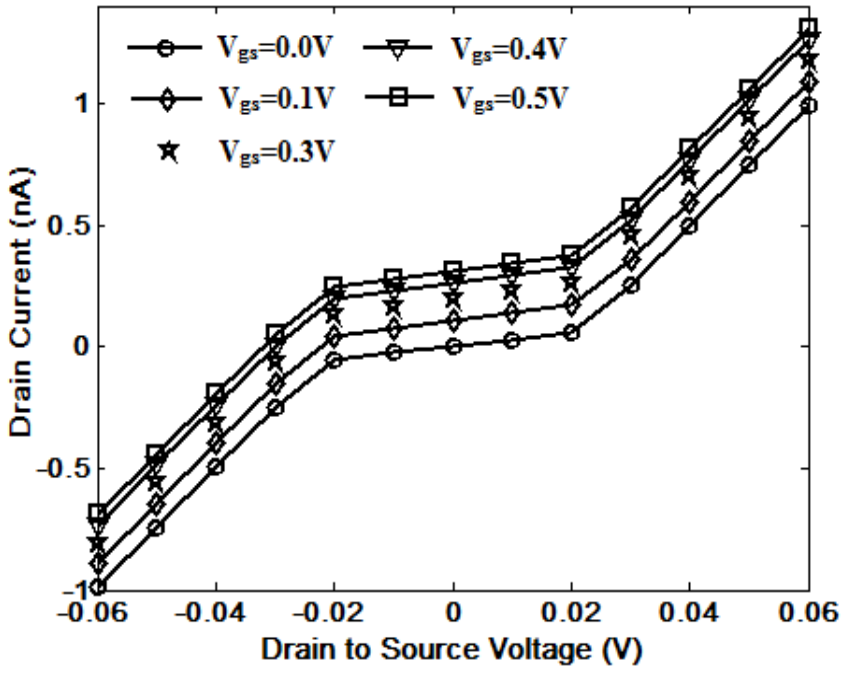


**Figure 2.8:** $V_{ds}$-$I_{ds}$ characteristics of the proposed macro-model for different gate biases varied from 0.0V to 0.5V with an increment of 0.1V.

## 2.4.3 Performance Comparison with other models

The comparative analysis of the performance of the presented model is accomplished by studying and comparing the $I_{ds}$-$V_{ds}$ characteristics in the CB region and the non-CB region with other models. In figure 2.9 drain current of all the Macro Models along with MIB [2.33], the popular analytical model of SET, and SIMON result is presented. The result of the present model is in close proximity with the popular MC single-electron simulation software SIMON. For the simulation purpose, the values of the model parameters are considered as follows- Rj and Cj are respectively 100MΩ and 3.2aF, T=30K. The temperature dependent parameter CF1 is set at 40. The CB region is defined with CVp=0.02. Rest of the parameters are considered as CR1=300x$10^{+6}$, CR2=220x$10^{+6}$, CI2=0.2x$10^{-9}$, $R_G$= 100x$10^{9}$Ω and $V_{gs}$=0V. It can be observed that the maximum range of $I_{ds}$ is achieved for the proposed model.

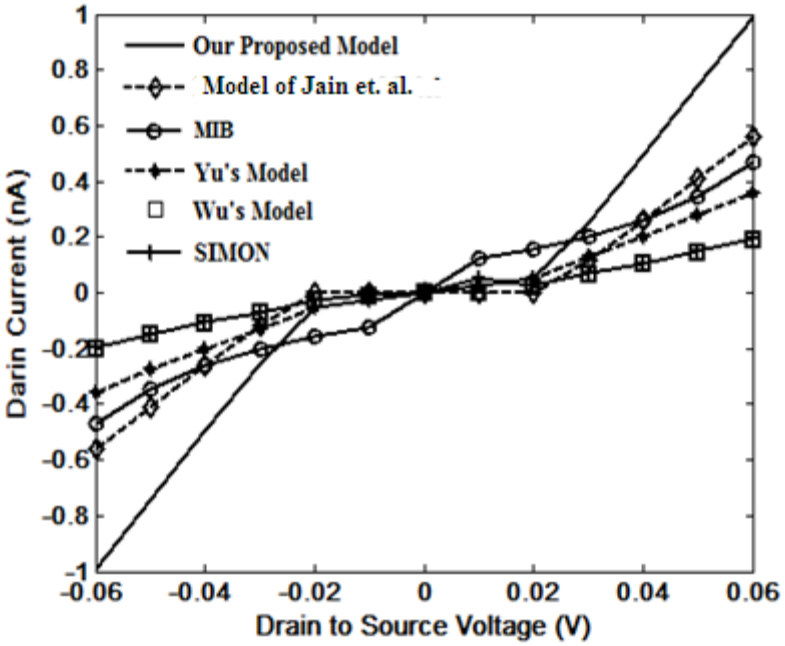


**Figure 2.9:** Comparative analysis of the $I_{ds}$ vs. $V_{ds}$ for $V_{gs}$=0V between the Yu's model, Wu and Lin's Model, the model proposed by Jain et al., MIB, SIMON and the proposed model.

## 2.5. Circuit Implementation with a new model

The verification and the validation of any model are possible if the designed circuits using the model behave in the desired way. For the justification and validation of the proposed model two benchmarked circuits are designed utilizing the same. The first circuit is one of the commonly used circuits of any digital logic application i.e. the inverter or the NOT gate and the second one is the SET based NDR (Negative-differential-resistance) circuit with multi-peak. In both the circuits the SETs are defined with the new modified Macro Model. The simulation of the circuits is done in the SPICE environment by including the designed model file.

### 2.5.1 Inverter circuit

The SET based circuit of NOT gate or inverter [2.34] is shown in figure 2.10. It is built with two identical SETs one working as p-SET another working as n-SET. They are connected in CMOS-like fashion [2.35] to give the inverted output as result.

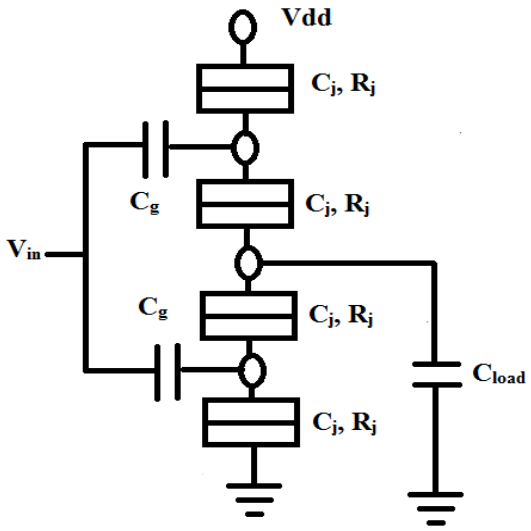


**Figure 2.10:** Schematic of the SET based inverter circuit.

The circuit parameters are junction capacitance ($C_j$), junction resistance ($R_j$), power supply voltage (Vdd), the input voltage (Vin) and the load capacitor ($C_{load}$).

The SET inverter circuit shown in the figure 2.10 is simulated by replacing the SETs with the subcircuit of the proposed Macro Model.

After the circuit is defined in the SPICE environment the terminal voltages are applied. According to the input applied signal, the output is checked which satisfies the logical requirement. The input and output signals are plotted with respect to time for the simulation of the SET based inverter. Figure 2.11 shows the result of the inverter design.

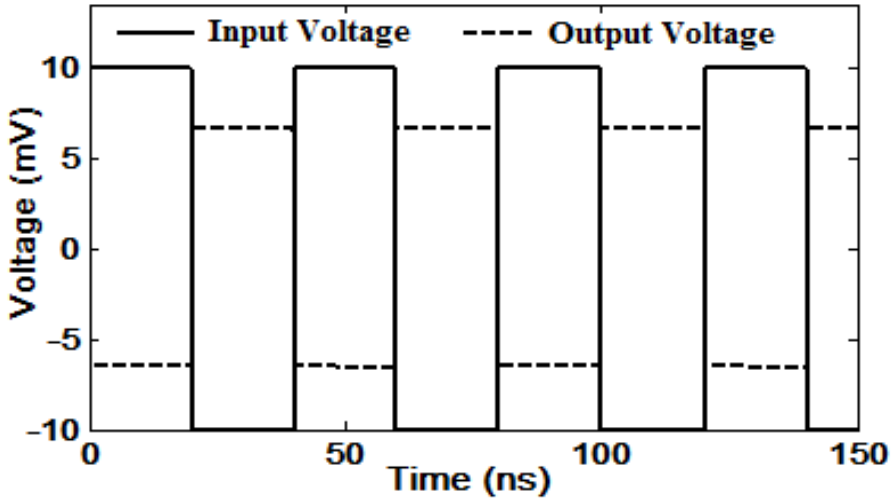


**Figure 2.11:** Input-output waveforms of the SET based inverter simulated with the proposed Macro model.

The solid line indicates the input signal waveform whereas the dashed line is for the output signal waveform. The parameter values used for the simulation purpose are as follows- $R_G$=100 GΩ,CR1=340x$10^{+6}$, CR2=100x$10^{+6}$, CVp=0.02, CF1=40 and CI2=0.2x$10^{-9}$.

The effect of the $R_G$ resistor on the voltage transfer characteristics (VTC) is analyzed with the figure 2.12. The different values considered for the $R_G$ resistor is 10GΩ, 20GΩ,30GΩ and 100GΩ. It can be observed that

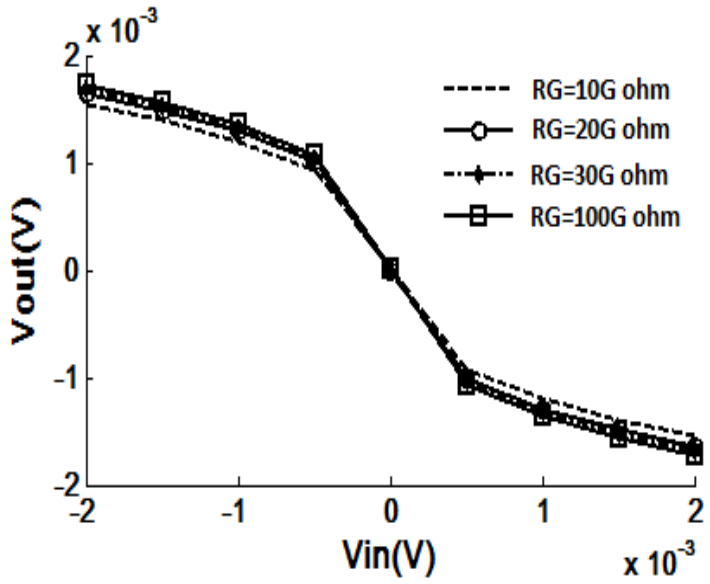


**Figure 2.12:** Effect of $R_G$ on the SET based inverter circuit voltage transfer characteristics simulated using proposed macro model where the $R_G$value is varied up to 100GΩ.

with the increase in the value of $R_G$ the voltage level of the output increases for the same input voltage value.This is because along with the increase in $R_G$ value, the probability of current leakage between the source and the gate terminal also gets diminished.

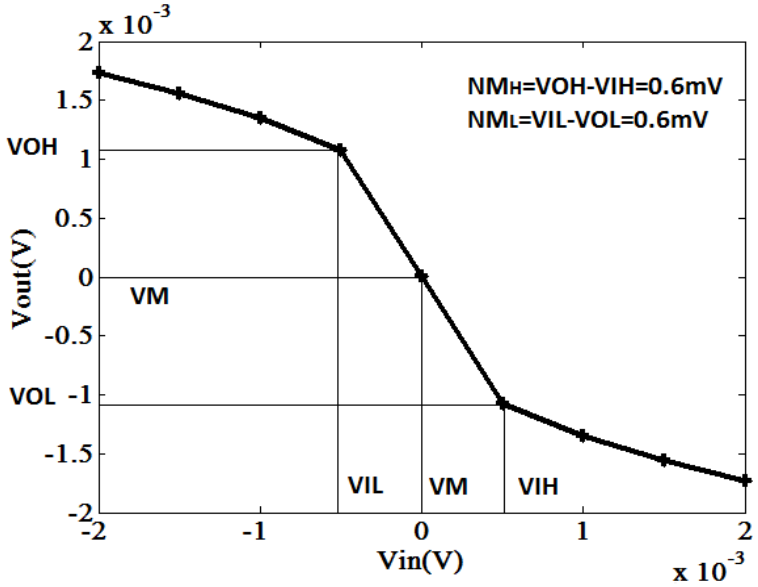


**Figure 2.13:**Calculation of Noise Margin from SET inverter VTC with $R_G$=100GΩ.

The process of calculating the noise margin (NM) [2.36] from the VTC of the SET inverter is shown in figure 2.13. The NM is generally defined with the two factors $NM_H$ (Noise margin high) and $NM_L$ Noise margin low). $NM_H$ can be computed by determining the difference between the $V_{OH}$ (highest $V_{out}$ where the slope is -1) $V_{IH}$ (highest $V_{in}$ for which slope is -1). Similarly, the $NM_L$ is determined from the difference between the $V_{IL}$ (smallest $V_{in}$ for which slope is -1) and $V_{OL}$ (lowest $V_{out}$ with slope -1). From the figure 2.12, the $NM_H$ and the $NM_L$ are determined as 0.6mV.

The variation of NM with the value of $R_G$ is observed in the figure 2.14. The value of $R_G$ is increased from 10GΩ to 100GΩ along with that the NM also increases. For the maximum value of $R_G$ i.e 100GΩ, the NM value is also maximum at 0.6mV.

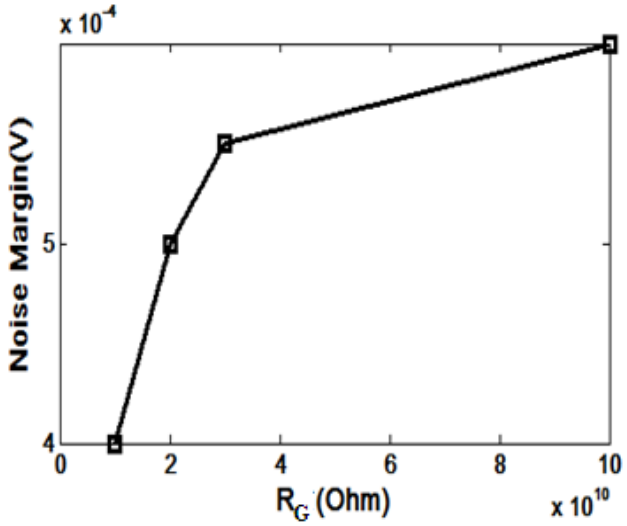


**Figure 2.14:** Noise Margin variation with $R_G$.

## 2.5.2 NDR circuit

The negative differential resistance (NDR)[2.37]-[2.39] is a property of a circuit or an electronic device where the current decreases with the increasing voltage in contrast to the conventional resistors. This negative resistance can be of two types – absolute (where the voltage-to-current

ratio is determined) and the differential (where the rate of voltage change is checked with the rate of current change).

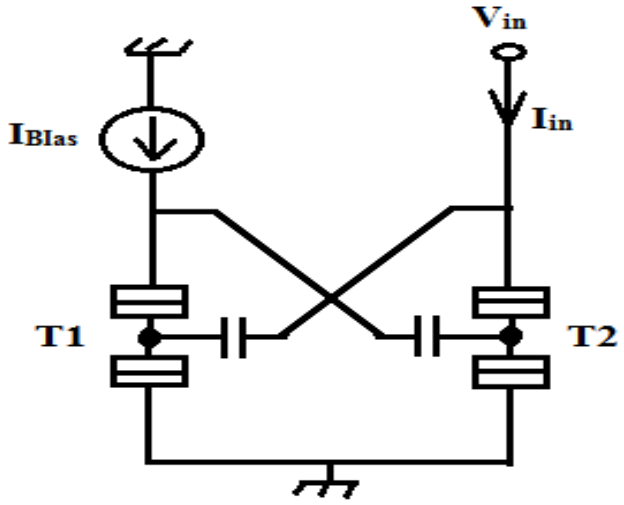


**Figure 2.15:** SET based multi-peak NDR circuit schematic diagram

The advantage of such NDR circuit is that under the certain condition it increases the electrical signal power whereas the positive resistance consumes power. The multi-peak NDR circuit is suitable for designing frequency multiplier, memory circuits with multiple-valued logic. The main two features of the NDR circuit are very high speed and the complexity of the circuit. A NDR circuit with multiple peaks based on SET is implemented and simulated using the proposed macro model. The simulation is performed in the Tanner SPICE environment. The design includes two cross-coupled SETs depicted in Figure 2.15. Here the two SETs are denoted with T1 and T2, where the current flowing through one SET is controlled by another one. This is done by connecting T1 with T2 through a feedback loop.

The designed circuit is simulated by replacing the SETs with equivalent model or subcircuit. The characteristic of SET based NDR circuit is illustrated in the figure 2.16, where the peaks are clearly visible. It has been observed that the height of the peaks increases with the increase in

bias current. Three values of bias current are considered for the plotting the figure 2.16 as 10nA,12nA, and 14nA. The other design parameter values are CI2=0.5x10$^{-9}$, CF1=40 and CVp=0.02. CR1 is chosen as 270x10$^{+6}$ and 280x10$^{+}$6 for respectively SET T1 and T2. For T1 and T2, CR2 values are selected as 70x10$^{+6}$ and 280x10$^{+6}$ respectively. The value of $R_G$ is 100GΩ.

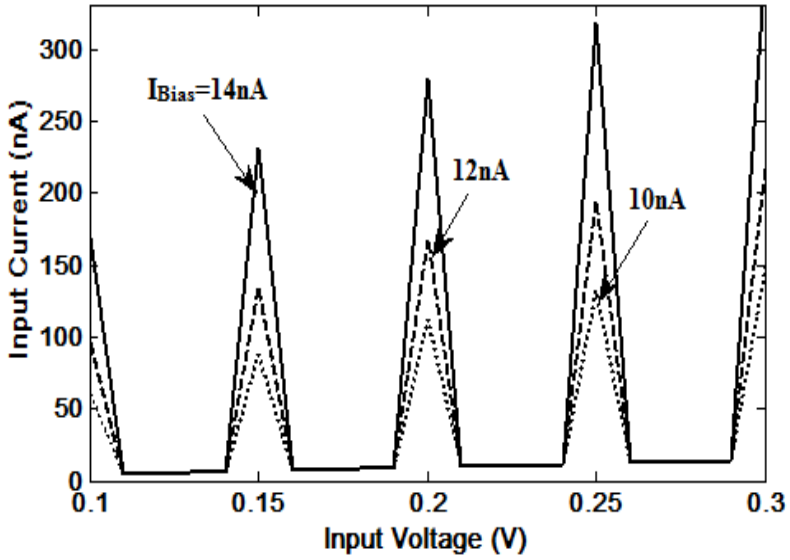


**Figure 2.16:**Multi peak NDR circuit characteristics for different bias currents with $R_G$=10x10$^{8}$Ω.

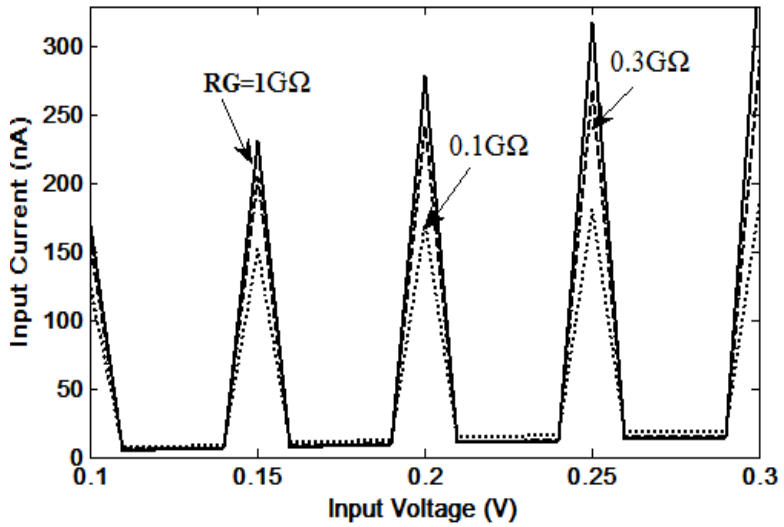


**Figure 2.17:** Effect of $R_G$ on the characteristics of the multi-peak NDR circuit.

At bias current value 14nA the circuit is simulated for the different values of $R_G$. The values chosen for $R_G$ are 0.1GΩ, 0.3GΩ and 1GΩ. The rest of the Macro Model parameters are kept as it is (for T1 SET: CR1=270x10$^{+}$6, CR2=70x10$^{+6}$ and for T2 SET: CR1=280x10$^{+6}$, CR2=280x10$^{+6}$, other parameters:, CI2=0.5x10$^{-}$9, CVp=0.02, CF1=40). The effect of $R_G$ on multi-peak NDR circuit characteristics is illustrated in the figure 2.17. It can be seen that the amplitude of the current increases for higher values of $R_G$. The range of input voltage considered here is starting from 0.1Volt to 0.3Volt. For $R_G$=0.1GΩ the amplitude of the current is 170nA at input voltage 0.25Volts. For the same input voltage, the current is 260nA and 325nA respectively for $R_G$=0.3GΩ and 1GΩ.

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# Chapter 3

# SMALL-SIGNAL MODELING OF SINGLE ELECTRON TRANSISTOR



## 3.1 Introduction

To fulfill the demand of an ever-increasing number of transistors in a chip MOSFET scaling has become essential. Due to the complications related to MOSFET scaling [3.1] nanodevices with a new principle of operations are drawing the attention. SET [3.2] being one of the nanodevices with unique characteristics and the lucrative feature is used for different digital as well as analog circuit designs. To analyze the behavior of SET under different external environmental conditions, it is essential to understand its characteristics in presence of large and small-signal both. Testing the circuit in each and every condition extensively is not at all cost-effective and feasible through the fabrication process. Appropriate modeling tools are required to simulate the behavior of the

SET without even fabricating a prototype. So far different works are reported on Macro Models [3.3]-[3.5] and analytical models [3.6]-[3.8] but no work has been done in the field of Small-signal modeling of SET. This portion of the thesis includes the constructional details of the small-signal equivalent model of the SET. The different parameters related to the intrinsic and extrinsic small-signal model are also deliberated in this part.

Keeping the AC input signal magnitude very small the drain characteristics of the SET can be confined in the linear region of operation. Thus the related input-output parameters can be correlated with each other through a linear set of equations. The characteristic equation of the SET is linearized by neglecting the higher order terms of the Taylor Series expansion of the same. It is possible to design a small-signal equivalent model of a device by counterfeiting the actual behavior. In presence of small-signal, the set of linear equations are formed from the nonlinear characteristics of the SET. Generally, the proper operation is limited by the range of excitation level.

The small-signal model of the SET has been developed for the first time. This part of the thesis describes the small-signal equivalent circuit of SET for getting the overview of parameters associated with the model. These parameters are predominantly responsible for deciding the nature of the device characteristics under different conditions. From the analog circuits designing point of view, the conductance parameters are vital to be determined. The frequency dependencies of the model parameters with capacitance and resistance value variation are also presented. The first part of this chapter mainly concentrates on the SET intrinsic part.

At high frequency (HF) several parasitic elements become effective and the characteristics of the device are often disturbed. The small-signal of SET is thus further modified to accommodate the parasitic elements. The physical structure of the device under test as well as the various testing instrument set up are mainly responsible for these extrinsic

components. The impact of these components on the network has been illustrated by incorporating several extrinsic parameters in the improved model.

This part of the thesis elaborates the formulation of the intrinsic SET small-signal model as well as the modified model which includes all the intrinsic and extrinsic parameter at high frequency.

## 3.2 Literature Survey

This section of the chapter highlights the related works and studies of available literature on the concerned topic. A few of the reported research works and concepts seminal to the field of interest are studied and elaborated here. The basic concentration of the SET research work has always been on either SED circuit design [3.9]-[3.12] or fabrication [3.13]-[3.16]. The circuit design always craved for equivalent circuit modeling of SETs and so the research works in the field. Different such modeling techniques with examples are highlighted over here firstly. Several works on SET analytical, Macro Model and SPICE equivalent model [3.17] are already reported on the field of SET modeling. The PSPICE model of SET is proposed by A.K. Abu E-Seoud et al. [3.18] in 2007. A realistic SET model is developed by Song et al. [3.19]. The demonstration of a device level SET model with verification has been also done by Hien [3.20] in 2009. Recently Frans Willey and Y. Darma [3.21] reported a work on SET simulation and modeling with ME in 2016. The popular Macro models [3.22] and Analytical models are also extensively used for exploring the circuit design area of SEDs. There are a few works reported in high-frequency operation of SET called RF-SET (Radio Frequency SET) [3.23]-[3.26]. But the model development for simulation purpose of SEDs mainly lacks suitable small-signal equivalent development of SETs.

Secondly, the works done so far on the small-signal model development of transistors apart from SETs are assembled over here. A numerous number of works are reported in the field of small-signal modeling of MOSFET from very earlier days to recent past. Kwon et al. [3.27] introduced an extraction method for MOSFET small-signal parameters at HF in the year of 2000. FET small-signal model was explained by Dambrine et al. [3.28] in 1988. The extraction procedure for Silicon-MOSFET small-signal parameters was described by Lovelace et al. [3.29]. Apart from these, several MOS small-signal model [3.30]-[3.37] oriented articles are already published.

According to the literature survey indicates that no such work in recent past has been reported in the field of SET small-signal modeling.

## 3.3 Intrinsic Small-Signal model of SET

The small-signal model formulation requires the study of the SET structure and its ideal characteristics. SET is constructed with two tunnel junctions and a conducting island shown in figure 3.1. The source and the back gate terminal of the SET are considered to be grounded for simplicity. The basic geometry of the SET is the essential part to be studied for constructing the small-signal equivalent circuit.

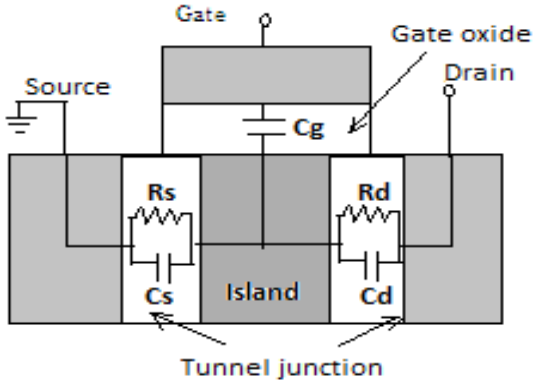



**Figure 3.1:** Physical structure of Single electron transistor

The DC characteristic of the SET is first thoroughly studied for small-signal analysis. The drain current depends upon the gate-to-source ($V_{GS}$) and drain-to-source voltage ($V_{DS}$) of SET.

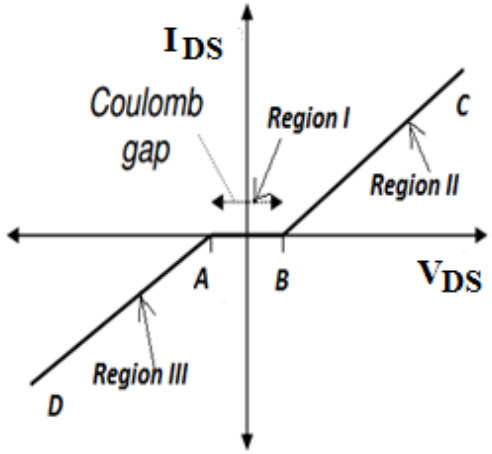



**Figure 3.2:** $V_{DS}$-$I_{DS}$ characteristics of ideal SET with symmetric junction.

The three regions of the V-I characteristics shown in figure 3.2 for constant $V_{GS}$ are

i. Region I: Coulomb gap or CB region with zero drain current (neglecting co-tunneling event and maintaining proper temperature condition) marked with A to B
ii. Region II: positive non-CB region (C to B)
iii. Region III: negative non-CB region(A to D)

The slope of the three regions is different. In ideal SET with symmetric junctions, the slope of region II and III are generally matched.

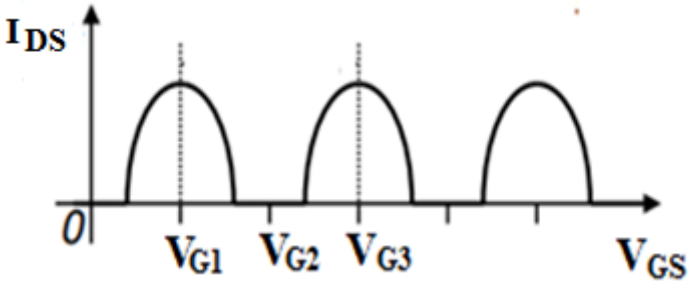



**Figure 3.3:** Ideal SET $V_{GS}$-$I_{DS}$ characteristics with constant $V_{DS}$.

The single electron oscillation can be observed from the figure 3.3 where $V_{DS}$ is kept constant and the $I_{DS}$ is plotted against $V_{GS}$. The peak values of $I_{DS}$ are marked for the corresponding $V_{GS}$ values denoted with $V_{G1}$, $V_{G2}$, $V_{G3}$.

### 3.3.1 Model Formulation

The equivalent model is constructed according to the inherent resistances and capacitances of the intrinsic SET exhibited in figure 3.1 where $R_d$, $R_s$, $C_d$, $C_s$ are the resistance of drain tunnel junction, source tunnel junction and the capacitances of drain tunnel junction, source tunnel junction respectively. Gate capacitance $C_g$ is considered between the gate and the island. Figure 3.4 illustrates the intrinsic part of the proposed small-signal equivalent circuit. The mentioned figure portrays the three terminals as gate (G), source(S) and drain (D). The $R_d$ and $C_d$ are parallelly connected to the drain terminal. $R_s$, $C_s$ are attached to the source terminal and $C_g$ to the gate terminal. Another capacitor $C_0$( $f\left(V_{gs},V_{ds}\right)$), dependent upon the $V_{gs}$ and $V_{ds}$, is connected apart from the SET geometry.

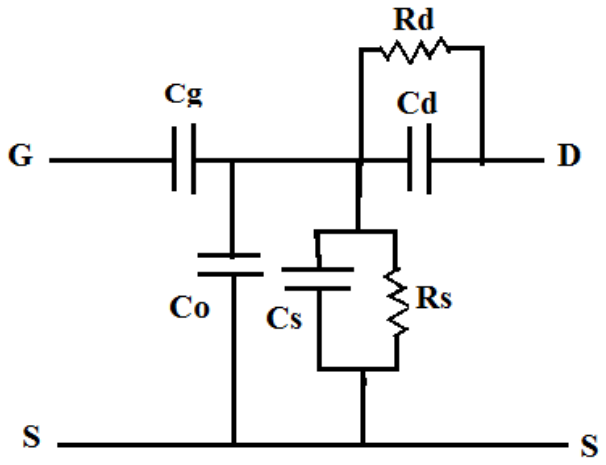



**Figure 3.4:** Intrinsic SET Small-signal model

The following assumptions are considered for small-signal analysis of the SET

a) SET is regarded as a three-terminal device where linear superposition can be applied.
b) The absence of independent sources within the network
c) Zero stored energy inside the network
d) Source terminal is grounded
e) Symmetric tunnel junctions

The two-port equivalent circuit of figure 3.4 is determined by assuming the gate-to-source terminal as the input port and drain-to-source terminal as the output port. $I_{ds}$ (drain current) and the $I_{gs}$ (gate to source current) works as the output port and input port current respectively. The $C_g$, $C_s$, and $C_d$ are expressed using equation (3.1) and (3.2).

$$C_g = \varepsilon_{ox}.\frac{L_g.W_{ch}}{T_{gox}} \tag{3.1}$$

Here,

$L_g$ : length of the gate

$\varepsilon_{ox}$ : dielectric constant of the oxide

$T_{gox}$ : gate oxide thickness

$W_{ch}$ : Channel width

$$C_s = C_d = \varepsilon_{Si}.\frac{T_{Si}.W_{ch}}{L_g} \tag{3.2}$$

The value of $C_g$ and $C_d$ can be varied by altering different fabrication parameters such as $T_{gox}$, $W_{ch}$ and $L_g$ of SET.The fabrication parameters of SET are used according to table 3.1[3.15] for $V_{ds}$=0.15mV. Silicon is used for the junction material and $SiO_2$ as the junction dielectric.

**Table 3.1:** Fabrication Parameters from [3.15]

| **Parameters** | $T_{gox}$ | $T_{Si}$ | $W_{ch}$ | $L_g$ |
|---|---|---|---|---|
| **Value (nm)** | 5 | 15 | 15 | 20 |

### 3.3.1.1 Impedance Parameter of Intrinsic Model

The impedance (Z parameters) or open circuit parameters are expressed as the ratio of voltage and currents by open circuiting the input and output port respectively. The different impedance parameters such as input and output impedance $Z_{11}^{i}$, $Z_{22}^{i}$ are expressed using equations (3.3) and (3.4) respectively. The expression of the open circuit impedance parameters $Z_{21}^{i}$ and $Z_{12}^{i}$ calculated from T equivalent of figure 3.4. are presented with equation (3.5) as they are equal.

$$Z_{11}^{i} = \frac{1 + j\omega R_s C_s + j\omega R_s C_0 + j\omega R_s C_g}{j\omega C_g - \omega^2 R_s C_s C_g - \omega^2 R_s C_0 C_g} \tag{3.3}$$

$$Z_{22}^{i} = \frac{R_d}{1 + j\omega R_d C_d} + \frac{R_s}{1 + j\omega R_s C_s + j\omega R_s C_0} \tag{3.4}$$

$$Z_{12}^{i} = Z_{21}^{i} = \frac{R_s}{1 + j\omega R_s C_s + j\omega R_s C_0} \tag{3.5}$$

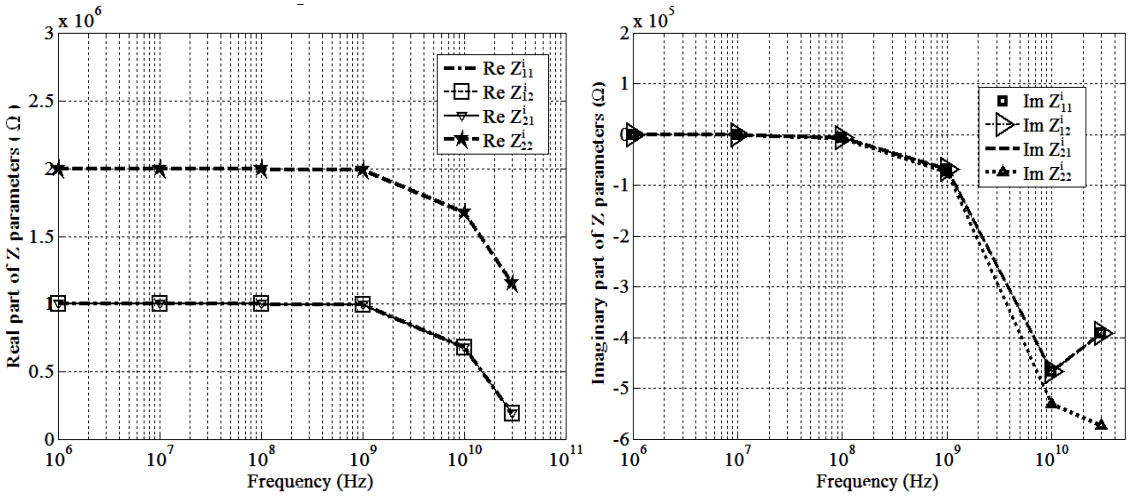
$$\Delta Z^{i} = Z_{11}^{i} Z_{22}^{i} - Z_{12}^{i} Z_{21}^{i} \tag{3.6}$$

The transfer impedances between two ports are denoted with $Z_{12}^{i}$ and $Z_{21}^{i}$. $\Delta Z^{i}$ is the difference between $Z_{11}^{i} Z_{22}^{i}$ and $Z_{12}^{i} Z_{21}^{i}$, presented with equation (3.6). $\omega$ is the angular frequency, which is equal to $2\pi f$, $f$ is the frequency.

The $Z^i$ matrix formed with the parameters is presented in equation (3.7)

$$Z^i = \begin{bmatrix} \dfrac{1+ j\omega R_s C_s + j\omega R_s C_0 + j\omega R_s C_g}{j\omega C_g - \omega^2 R_s C_s C_g - \omega^2 R_s C_0 C_g} & \dfrac{R_s}{1+ j\omega R_s C_s + j\omega R_s C_0} \\ \dfrac{R_s}{1+ j\omega R_s C_s + j\omega R_s C_0} & \dfrac{R_d}{1+ j\omega R_d C_d} + \dfrac{R_s}{1+ j\omega R_s C_s + j\omega R_s C_0} \end{bmatrix} \quad (3.7)$$

Frequency dependency of different Z parameter ($Z^i_{11}, Z^i_{12}$, $Z^i_{21}, Z^i_{22}$) real parts and imaginary parts of intrinsic-SET is checked in figure 3.5 (a) and (b) respectively. For both the figures symmetric junctions with $R_d$=$R_s$=1MΩ and $C_d$=$C_s$=1aF is considered. The other parameters are used as $C_0$=10aF and $C_g$=0.1aF. According to figure 3.5 (a) the real part of Z parameters $Z^i_{11}, Z^i_{12}$, $Z^i_{21}$ remain constant at 1MΩ and $Z^i_{22}$ at 2MΩ up to 1GHz frequency, afterwards they start decreasing along with the increasing frequency. The figure reveals the input impedance of SET is sufficiently high at 2MΩ up to 1GHz of frequency.




(a) (b)

**Figure 3.5:** Variation of (a) real part, (b) imaginary part of Z parameters with frequency for intrinsic SET.

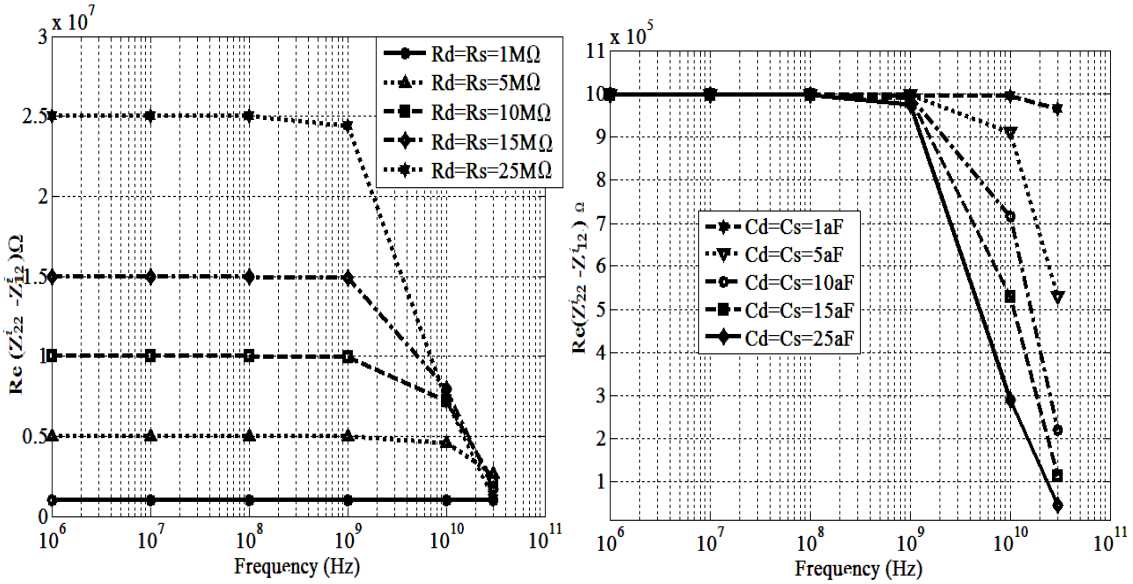
After that specified frequency, the magnitude of the input, output and the transfer impedance of the intrinsic-SET falls. Figure 3.5 (b) illustrates the nature of the imaginary parts of all the Z parameters to be slightly decreasing from100MHz to 1GHz but afterward the values suddenly drop

with a further rise in frequency. It indicates the phase of the $Z^i$ parameters is more prone to frequency change than the magnitude. By determining the difference between $Z^i_{22}$ and $Z^i_{12}$ the $C_g$,$C_0$,$C_s$ and $R_s$ parameters can be omitted. The consequence of only the drain tunnel junction can be witnessed in the real and imaginary part of the difference $(Z^i_{22} - Z^i_{12})$.

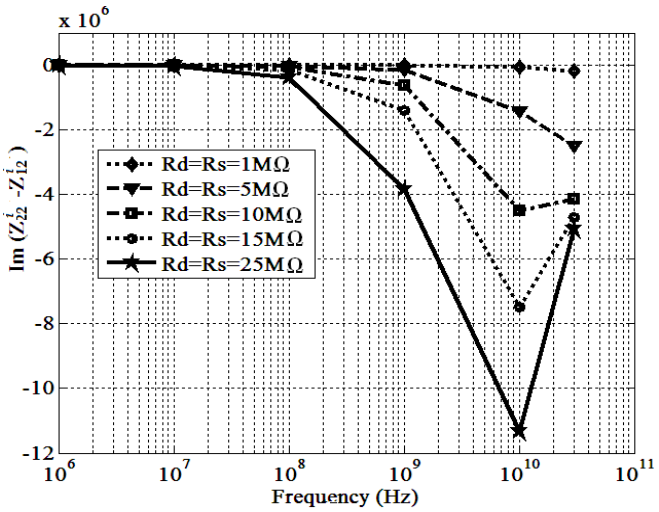
$$\mathrm{Re}(Z^i_{22} - Z^i_{12}) = \frac{R_d}{1+\omega^2 {R_d}^2 {C_d}^2} \tag{3.8}$$

$$\mathrm{Im}(Z^i_{22} - Z^i_{12}) = \frac{-j\omega {R_d}^2 C_d}{1+\omega^2 {R_d}^2 {C_d}^2} \tag{3.9}$$

The dependency of $\mathrm{Re}(Z^i_{22} - Z^i_{12})$ and $\mathrm{Im}(Z^i_{22} - Z^i_{12})$ on $R_d$ and $C_d$ can be identified from the above-mentioned expressions (3.8) and (3.9). The deviation of $\mathrm{Re}(Z^i_{22} - Z^i_{12})$ with $R_d$ and $C_d$ values is revealed in figure 3.6(a) and (b) respectively. While plotting figure 3.6 (a) the symmetric tunnel junction resistance values are taken as 1MΩ to 25 MΩ with an interval of 5 MΩ. The values of $R_d$ (or $R_s$) are kept sufficiently higher than the




(a) (b)




(c)

**Figure 3.6:** Variation of (a) $\mathrm{Re}(Z_{22}^{i} - Z_{12}^{i})$ for different $R_d$,(b) $\mathrm{Re}(Z_{22}^{i} - Z_{12}^{i})$ for different $C_d$ (c) $\mathrm{Im}(Z_{22}^{i} - Z_{12}^{i})$ for different $R_d$ with frequency.

quantum tunneling resistance according to primary rules of 'Orthodox theory' of tunneling. With the increment in the value of $R_d$, the magnitude of the real part of the difference is seen to be growing. The maximum value of the magnitude is 25MΩ for $R_d$=$R_s$=25MΩ. It remains in the same value up to frequency range of 100MHz. A gradual reduction up to 1 GHz is observed after that a steep change in the value can be visualized. Whereas for the lower values of $R_d$ (or $R_s$), rate of fall in the value with respect to the frequency also reduces. Even for the 1MΩ value of $R_d$, the difference becomes 0MΩ and the value change with frequency become almost negligible.

The next figure 3.6 (b) illuminates on the variation of the magnitude of the difference between the two impedances ($Z_{22}^{i}$ and $Z_{12}^{i}$) for junction capacitance values. Here for the symmetric junction capacitance values are taken from 1aF to 25aF with the increment of 5aF. For this figure, the magnitude of the difference of two impedances is more affected by the higher values of the capacitances than the lower values after 1GHz

frequency. The constant frequency response is seen up to 100MHz then from 1GHz rapid value degradation is noticed for the higher capacitance values. The maximum achievable magnitude value of the difference is 1MΩ for all the $C_d$ values up to 100MHz.

The above two figures 3.6 (a),(b) check the variation of two impedances magnitude difference with $R_d$ and $C_d$. Figure 3.6(c) gives an overview of the change in imaginary part of the difference , $\mathrm{Im}(Z_{22}^i - Z_{12}^i)$, for $R_d$. The same values of $R_d$ (1MΩ to 25MΩ) have been taken into consideration. It shows up to 10MHz there is no change noticeable in $\mathrm{Im}(Z_{22}^i - Z_{12}^i)$ as it remains 0 for all the $R_d$ values. Similar to the previous two observations with higher resistance value $\mathrm{Im}(Z_{22}^i - Z_{12}^i)$ becomes more negative from 1GHz to 10GHZ. Then the value starts increasing again with frequency and $C_d$ both.

The real and the imaginary part of the transfer impedance are expressed with equation (3.10) and (3.11). The dependency of $\mathrm{Re}(Z_{12}^i)$ and $\mathrm{Im}(Z_{12}^i)$ on $C_0$ is checked in figure 3.7. The magnitude of the transfer impedance ($Z_{12}^i$) stays constant till 100MHz at 1MΩ for all values of $C_0$ starting from 1aF to 50aF.

$$\mathrm{Re}(Z_{12}^i) = \frac{R_s}{1+\omega^2 R_s^{\,2}(C_0+C_s)^2} \tag{3.10}$$

$$\mathrm{Im}(Z_{12}^i) = \frac{-j\omega R_s^{\,2}(C_0+C_s)}{1+\omega^2 R_s^{\,2}(C_0+C_s)^2} \tag{3.11}$$

The gradual reduction in the value is observed till 1GHz, afterward the rate of change of the $\mathrm{Re}(Z_{12}^i)$ or $\mathrm{Re}(Z_{21}^i)$ becomes very high with frequency for higher values of $C_0$ though for 1aF value the change is almost negligible up to 10GHz. As the $C_0$ is the only parameter which depends upon the $V_{gs}$ and $V_{ds}$, the effect of these voltages also can be checked through varying $C_0$.

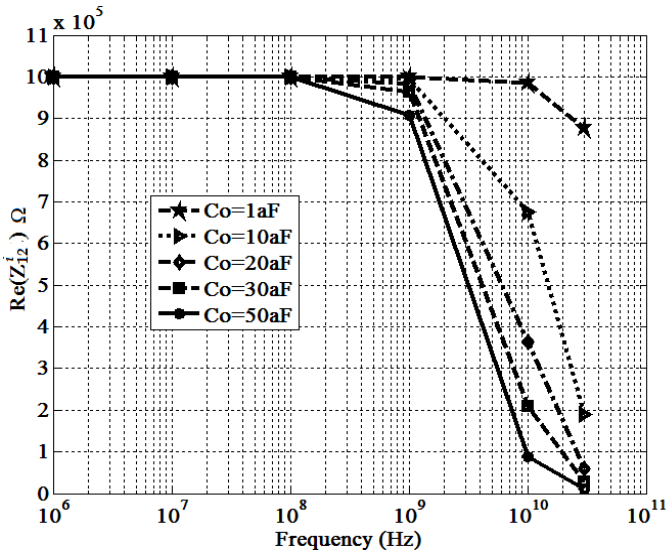



**Figure 3.7:** $\mathrm{Re}(Z_{12}^{i})$ variation with frequency for different $C_0$ values

### 3.3.1.2 Admittance Parameter of Intrinsic Model

The admittance or the Y parameters are essential to design the circuits in very high frequency. Being one of the important two port parameters the Y parameters can be defined with the current phasor and the voltage phase ratio. In that condition the small-signal voltage should be applied to one of the terminals keeping rest of the terminal grounded. This parameter is also called the short circuit parameter as either of the ports needs to be short-circuited for parameter determination. As the Y parameters are basically the ratio of current and voltage, the dimension is admittance. The drain current of intrinsic-SET can be expressed with the following Y parameter based equation shown in equation (3.12)

$$I_{ds} = Y_{21}^{i} \times \Delta V_{gs} + Y_{22}^{i} \times \Delta V_{ds} \tag{3.12}$$

Where, the intrinsic transconductance and drain conductance of SET are respectively $g_m = \left( \frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=Const} \right) = Y_{21}^{i}$ and $g_d = \left( \frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{gs}=Const} \right) = Y_{22}^{i}$

By using the conversion formula (3.13) the Z parameters of intrinsic SET are converted to Y parameters.

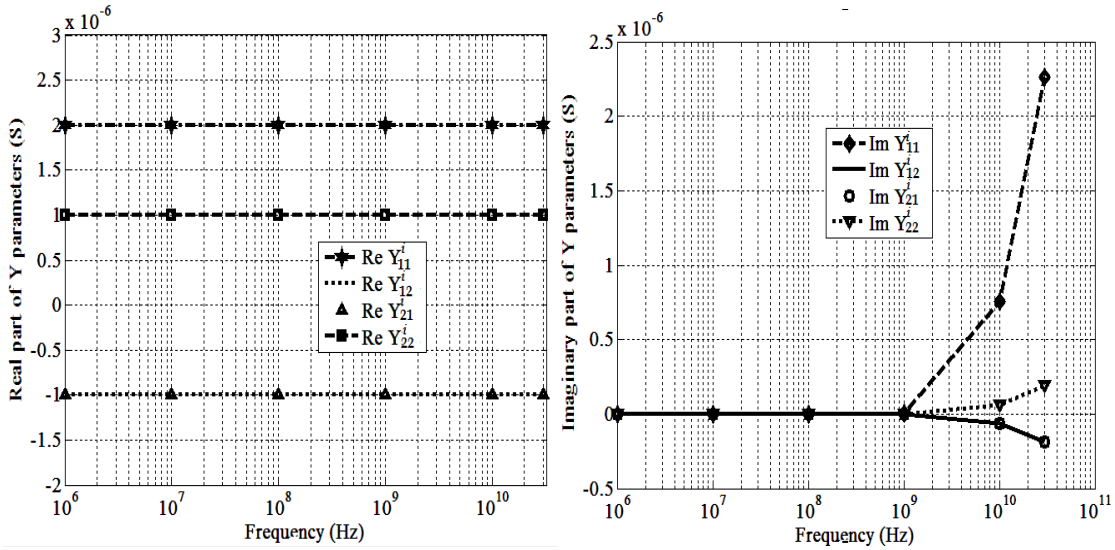
$$\begin{bmatrix} Y_{11}^i & Y_{12}^i \\ Y_{21}^i & Y_{22}^i \end{bmatrix} = \begin{bmatrix} \frac{Z_{22}^i}{\Delta Z^i} & \frac{-Z_{12}^i}{\Delta Z^i} \\ \frac{-Z_{21}^i}{\Delta Z^i} & \frac{Z_{11}^i}{\Delta Z^i} \end{bmatrix} \tag{3.13}$$

The calculated Y parameters are expressed in the following equations (3.14)-(3.16).

$$Y_{11}^i = \frac{(1+ j\omega C_s R_s + j\omega C_0 R_s)(j\omega C_g R_d) + j\omega C_g R_s (1+ j\omega C_d R_d)}{Rd + j\omega C_s R_s R_d + j\omega C_0 R_s R_d + j\omega C_g R_s R_d + R_s + j\omega C_d R_d R_s} \tag{3.14}$$

$$Y_{12}^i = Y_{21}^i = -\frac{j\omega C_g - \omega^2 C_s C_g R_s}{2 + j\omega R_s (C_g + 2C_s + C_0)} \tag{3.15}$$

$$Y_{22}^i = \frac{(1+ j\omega C_s R_s + j\omega C_0 R_s)(1+ j\omega C_d R_d) + j\omega C_g R_s (1+ j\omega C_d R_d)}{Rd + j\omega C_s R_s R_d + j\omega C_0 R_s R_d + j\omega C_g R_s R_d + R_s + j\omega C_d R_d R_s} \tag{3.16}$$




(a) (b)

**Figure 3.8:**.Intrinsic-SET Impedance parameters (a) real part and (b) imaginary part deviation with frequency

The figure 3.8 (a) depicts the Y-parameter real parts of the intrinsic-SET if plotted against the frequency. All the admittance parameters remain constant throughout the frequency range . In Figure 3.8 (a) it can be witnessed that the $\mathrm{Re}(Y_{11}^{i})$, $\mathrm{Re}(Y_{12}^{i})$, $\mathrm{Re}(Y_{21}^{i})$ and $\mathrm{Re}(Y_{22}^{i})$ remain constant at 2μS,-1μS,-1μS and 1μS respectively for the entire frequency range under consideration.

The imaginary part values whereas increase with the frequency starting from 1GHz shown in figure 3.8 (b). Below 1GHz all the imaginary parts remain near to 0 Siemens value. $\mathrm{Im}(Y_{11}^{i})$ increases rapidly with frequency above 1GHz, whereas a small rise in value is detectable for $\mathrm{Im}(Y_{22}^{i})$. The variation in $\mathrm{Im}(Y_{21}^{i})$ as well as in $\mathrm{Im}(Y_{12}^{i})$ is very small with respect to the other two.

The complete drain current equation of intrinsic-SET shown in equation (3.17) is formulated using the above mentioned Y parameter.

$$I_{ds} = \mathrm{Re}\left[-\frac{j\omega C_g - \omega^2 C_s C_g R_s}{2 + j\omega R_s (C_g + 2C_s + C_0)}\right].V_{gs} + \mathrm{Re}\left[\frac{(1 + j\omega C_s R_s + j\omega C_0 R_s)(1 + j\omega C_d R_d) + j\omega C_g R_s (1 + j\omega C_d R_d)}{Rd + j\omega C_s R_s R_d + j\omega C_0 R_s R_d + j\omega C_g R_s R_d + R_s + j\omega C_d R_d R_s}\right].V_{ds} \quad (3.17)$$

The Y-parameter equivalent intrinsic-SET circuit is revealed in figure 3.9.

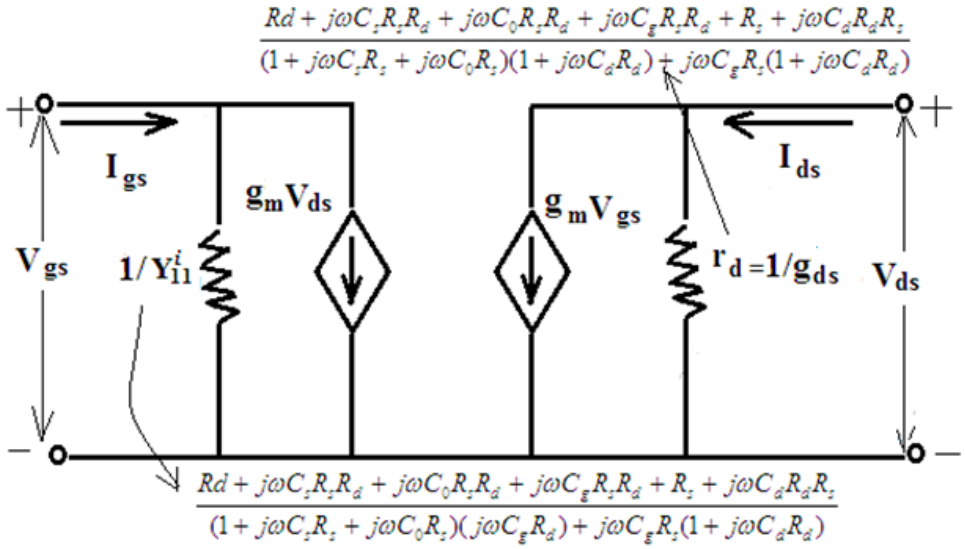



**Figure 3.9:** Intrinsic-SET Y-parameter equivalent circuit

The equation (3.17) is utilized to build the shown equivalent circuit. In the circuit ($g_m.V_{ds}$) and ($g_d.V_{gs}$) are two voltage controlled current sources. Where,the transconductance is $g_m = Y_{12}^i$ and the drain conductance is $g_d = Y_{22}^i$. For the presented circuit the value of current $I_{gs}$ is 0 as in case of ideal SET no current flows through gate terminal.

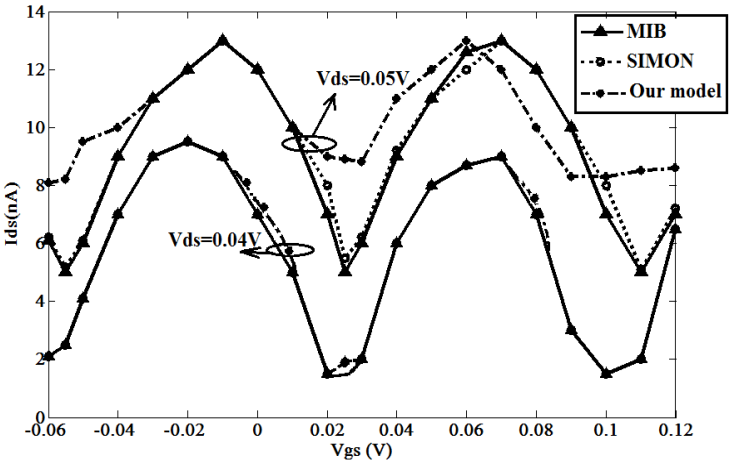


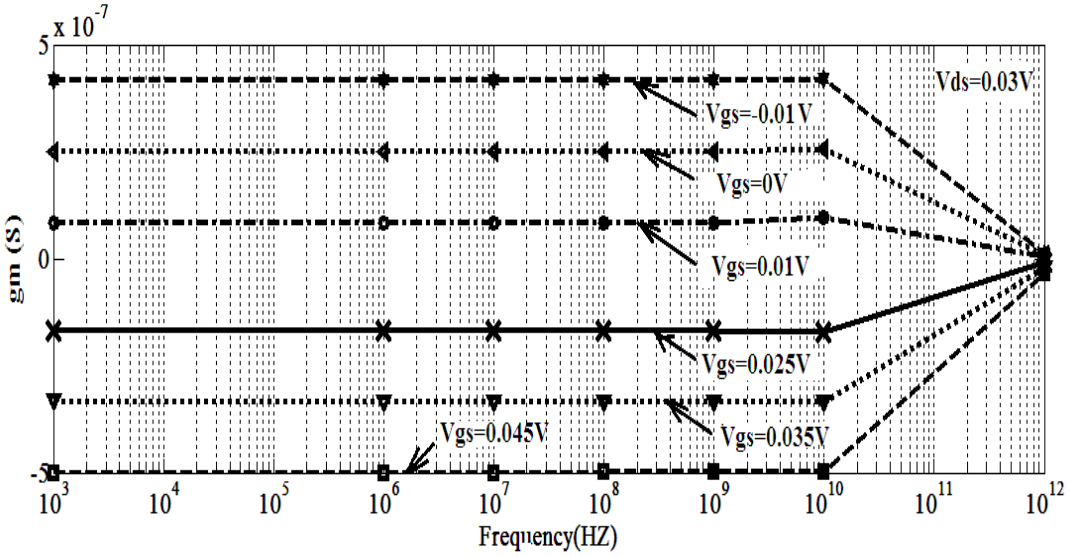

**Figure 3.10:** $I_{ds}$ deviation with $V_{gs}$ for $V_{ds}$ value 0.05V and 0.04V for the MIB, SIMON and proposed model

The drain characteristic of the intrinsic-SET is plotted using equation (3.17) in figure 3.10. It depicts the variation of drain current $I_{ds}$ with respect to the $V_{gs}$ for two different values of $V_{ds}$ such as 0.04V and 0.05V. The comparison of the drain characteristics between the results of MIB model and SIMON simulation has also been accomplished. The plot implies the nature of the DC characteristics of the proposed model is similar to the other two methods. The oscillating nature of the diagram is also revealed in the figure 3.10.

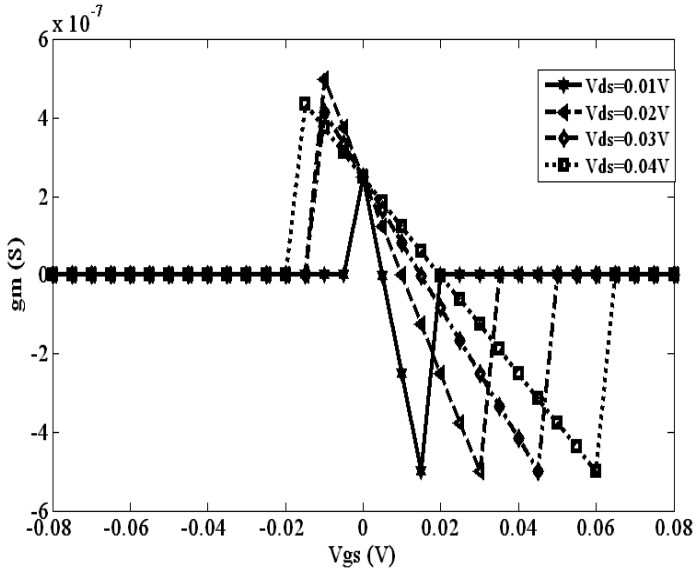
### 3.3.1.3 Transconductance and Drain Conductance

The drain current equation provides the opportunity to determine the two conductances such as $g_m$ (transconductance) and $g_d$ (drain

conductance). For analog circuit applications related to any transistor these two conductance play very important role. The expression of the $g_m$ and $g_d$ can be determined from the constructed Y-parameter equations. The intrinsic $g_m$ variation with frequency for different $V_{gs}$ values and $V_{ds}$=0.03V is reflected in figure 3.11 (a).For SET the positive or negative both types of transconductance is possible due to the oscillating nature of drain current with $V_{gs}$.




(a)



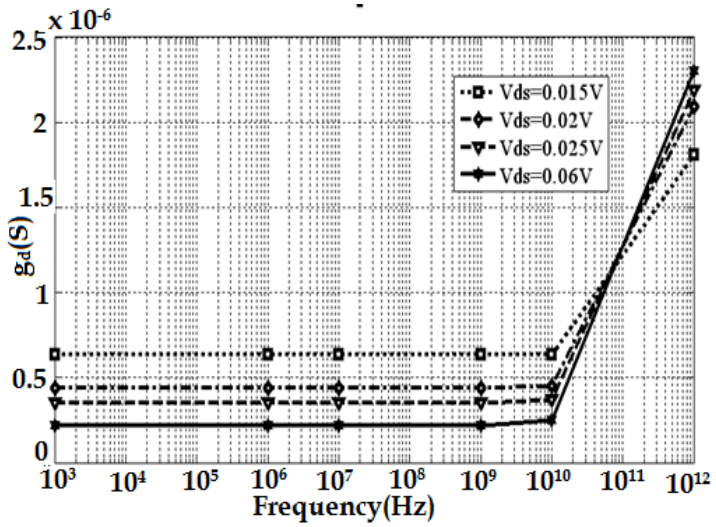

(b)

**Figure 3.11:** Variation of $g_m$ with respect to (a) frequency (b) $V_{ds}$

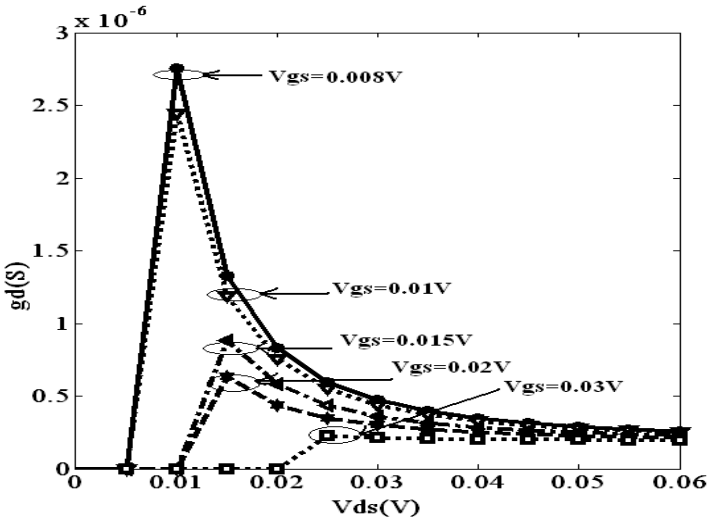
For $V_{gs}$=-0.01V to 0.045V the $g_m$ value changes from 0.5μS to -0.5μS. The value remains constant for a particular $V_{gs}$ till the frequency value of 10GHz is reached. For positive $g_m$ values after 10GHz frequency a certain decrease can be noticed while for negative $g_m$ a certain increase is noticeable.

The $g_m$ is a function of $V_{gs}$ voltage and can be defined as the rate of change of the $I_{ds}$ with respect to $V_{gs}$ change keeping the $V_{ds}$ constant. In a similar way, the $g_m$ variation with $V_{gs}$ has been checked in the figure 3.11 (b) for constant $V_{ds}$. The range $V_{gs}$ for which $g_m$ is plotted is varied from -0.08V to 0.08V. The selected values of $V_{ds}$ is starting from 0.01V to 0.04V. Only the positive value of $V_{ds}$ is considered. The frequency is fixed at 1GHz for the particular plot. It can be observed that the $g_m$ slope changes with the $V_{ds}$ .the value change from 0.5μS to -0.5μS.

The observation of the $g_d$ value for frequency change and $V_{ds}$ change is presented in the figure 3.12 (a) and (b) respectively. The drain conductance is defined as the rate of change of $I_{ds}$ with respect to $V_{ds}$ for constant $V_{gs}$. In figure 3.12 (a) frequency is varied from 1kHz to 1THz range for which $g_d$ is plotted. For all the concerned values of $V_{ds}$ (starting from 0.015V to 0.06V) $g_d$ values remain constant up to 10GHz.




(a)




(b)

**Figure 3.12:** $g_d$ variation of with respect to (a) frequency and (b) $V_{ds}$

The range of $g_d$ till 10GHz is between 0.25μS to 0.6μS. Higher the $V_{ds}$ value lower is the $g_d$ value.

Figure 3.12 (b) provides the $g_d$ variation with $V_{ds}$ and frequency. In the figure, $g_d$ is checked for $V_{gs}$ 0.008V to 0.03V and the range of $V_{ds}$ is taken as 0 to 0.06V. It can be seen that the $g_d$ value falls for higher $V_{gs}$. Whereas with increment in $V_{ds}$ value sudden reduction in the value is visible.

## 3.4 Complete Small-Signal model with Intrinsic and Extrinsic Elements

The formation of the HF small-signal model by considering all the extrinsic parameters even along with the intrinsic elements of the SET is conferred in the present section. The complete circuit is shown in the figure 3.13. It depicts the intrinsic block with a dashed block and rest of the parameters is actually the extrinsic elements generated in the high-frequency operation of SET.

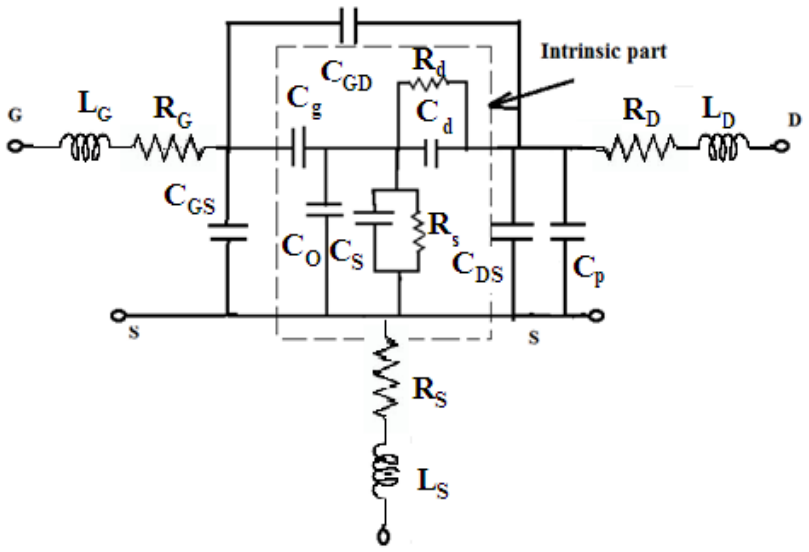



**Figure 3.13:** HF Small-signal equivalent circuit of SET

Among them, the different inductances are $L_G$, $L_D$, $L_S$. The parasitic resistors and capacitors are denoted with $R_S$, $R_D$, $R_G$ and $C_{GD}$, $C_{GS}$, $C_{DS}$, $C_p$ respectively. The parasitic elements are the spurious elements those are formed due to the high-frequency operation of the SET and also the use of different testing instrument connections. The chip carrier on which generally the device is tested introduces the parasitic inductance associated to Gate terminal ($L_G$), inductance related to the drain terminal ($L_D$), inductance formed in the source terminal ($L_S$). The parasitic capacitance between the gate-to-drain, drain-to-source, and gate-to-source terminal are represented with $C_{GD}$, $C_{DS}$ and $C_{GS}$ respectively. The $C_p$ or pad capacitance is formed due to the presence of the contact pad. Rest of the intrinsic parameters is already discussed in section 3.3.

### 3.4.1 Z Parameter Formulation

The total $Z_{total}$ parameters of the above circuit are computed by doing the two-port network analysis. The expression of the calculated impedance parameters are shown in the expression (3.18)-(3.21).

$$Z_{11} = \frac{\left(1+ j\omega R_d C_d\right)\nabla z^2}{\left(R_d + j\omega C_{GS}\nabla z - \omega^2 C_d C_{GS} R_d \nabla z\right)\rho} \times \left( \frac{1+ j\omega (C_s + C_o) R_s}{R_s + j\omega (C_s + C_o) R_s - \omega^2 (C_s + C_o) C_{GD} \nabla z R_s} + \frac{j\omega C_g}{\left(1 - \omega^2 C_{DS}, C_g \nabla z\right)} \right)$$

$$+ (R_S + R_D) + j\omega (L_S + L_D) \tag{3.18}$$

$$Z_{12} = \left( \frac{j\omega C_g \nabla z \left(1+ j\omega C_d R_d\right)}{\rho\left(R_d + j\omega C_{GS}\nabla z - \omega^2 C_d R_d C_{GS}\nabla z\right)\left(1 - \omega^2 C_g C_{DS}, \nabla z\right)} \right) + \left(R_s + j\omega L_s\right) \tag{3.19}$$

$$Z_{21} = \left( \frac{j\omega C_g \nabla z \left(1+ j\omega C_d R_d\right)}{\rho\left(R_d + j\omega C_{GS}\nabla z - \omega^2 C_d R_d C_{GS}\nabla z\right)\left(1 - \omega^2 C_g C_{DS}, \nabla z\right)} \right) + \left(R_s + j\omega L_s\right) \tag{3.20}$$

$$Z_{22} = \frac{j\omega C_g \nabla z^2}{\left(1 - \omega^2 C_{DS}, C_g \nabla z\right)\rho} \times \left( \frac{1+ j\omega (C_s + C_o) R_s}{R_s + j\omega C_{GD}\nabla z - \omega^2 C_{GD} (C_s + C_o) R_s \nabla z} + \frac{1+ j\omega R_d C_d}{R_d + j\omega C_{GS}\nabla z - \omega^2 C_d C_{GS} R_d \nabla z} \right) + (R_S + R_D) + j\omega (L_S + L_D) \tag{3.21}$$

Where,

$$\rho = \nabla z \left\{ \frac{1+ j\omega R_S (C_s + C_o)}{R_s + j\omega C_{GD}\nabla z - \omega^2 R_d (C_s + C_o) C_{GD}\nabla z} + \frac{1+ j\omega R_d C_d}{R_d + j\omega C_{GS}\nabla z - \omega^2 R_d C_d C_{GD}\nabla z} + \frac{j\omega C_g}{1 - \omega^2 C_g C_{DS}, \nabla z + j\omega C_{DS}, \nabla z} \right\}$$

$$\nabla z = \left( \frac{R_d + j\omega R_S R_d (C_S + C_O) + j\omega C_g R_d R_S + R_S + j\omega C_S R_S R_d}{j\omega C_g (1+ j\omega C_d R_d)(1+ j\omega (C_S + C_O) R_S)} \right)$$

## 3.4.2 Scattering Parameter Formulation

The reflection and transmission coefficients related to the RF (Radio-frequency) and Microwave Designs are known as the S-parameters or the scattering parameters. These parameters are a combination of magnitude and the signal phase. S parameters are known as the mathematical constructs which quantifies the propagation of RF energy in a multiport system.

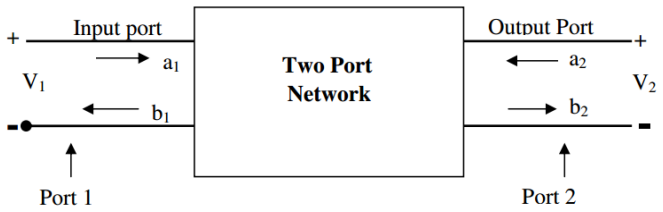



**Figure 3.14:** S parameter determination with a Two-port network

A simple black box representation of the network for S-parameter determination is shown in figure 3.14 with two ports (input and output). Representation of an extremely complicated network is possible through S-matrix formation. The generalized diagram with V1,V2 input output voltages, a1,a2 incident waves and b1,b2 reflected waves is presented in the figure. According to the defined parameters the basic equations are formed as (3.22).

$$\left.\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned}\right\} \tag{3.22}$$

With the characteristics impedance 50Ω the following conversion equations (3.23)-(3.25) are used to determine SET S-parameters from the already calculated Z parameters of the same.

$$S_{11} = \frac{(Z_{11}-50)(Z_{22}+50)-Z_{12}^2}{(Z_{11}+50)(Z_{22}+50)-Z_{12}^2} \tag{3.23}$$

$$S_{12} = S_{21} = \frac{2\times 50.Z_{12}}{(Z_{11}+50)(Z_{22}+50)-Z_{12}^2} \tag{3.24}$$

$$S_{22} = \frac{(Z_{11}+50)(Z_{22}-50)-Z_{12}^2}{(Z_{11}+50)(Z_{22}+50)-Z_{12}^2} \tag{3.25}$$

The stability gain (k) is represented by the equation (3.26) based on S-parameters. k is known as Rollett stability factor.

$$k = \frac{\left(1+\left|S_{\Delta}\right|^2-\left|S_{11}\right|^2-\left|S_{22}\right|^2\right)}{\left(2\left|S_{11}S_{22}\right|\right)} \tag{3.26}$$

where, $S_\Delta = S_{11}S_{22} - S_{12}S_{21}$

The maximum unilateral transducer power gain ($G_{TUmax}$) is expressed by the following equation (3.27).

$$G_{TU\max} = \frac{|S_{21}|^2}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} \tag{3.27}$$

### 3.4.2.1 Dependency on Parasitic Capacitance

The different parasitic capacitances are discussed in the section 3.4.2 among them the capacitance due to the contact pad is known as the pad capacitance and denoted with $C_p$. This section deals with the effect of $C_p$ on the different S-parameters of SET. The $C_p$ is considered across the drain-to-source terminal as it is mainly effective at the terminal from which the output is taken.

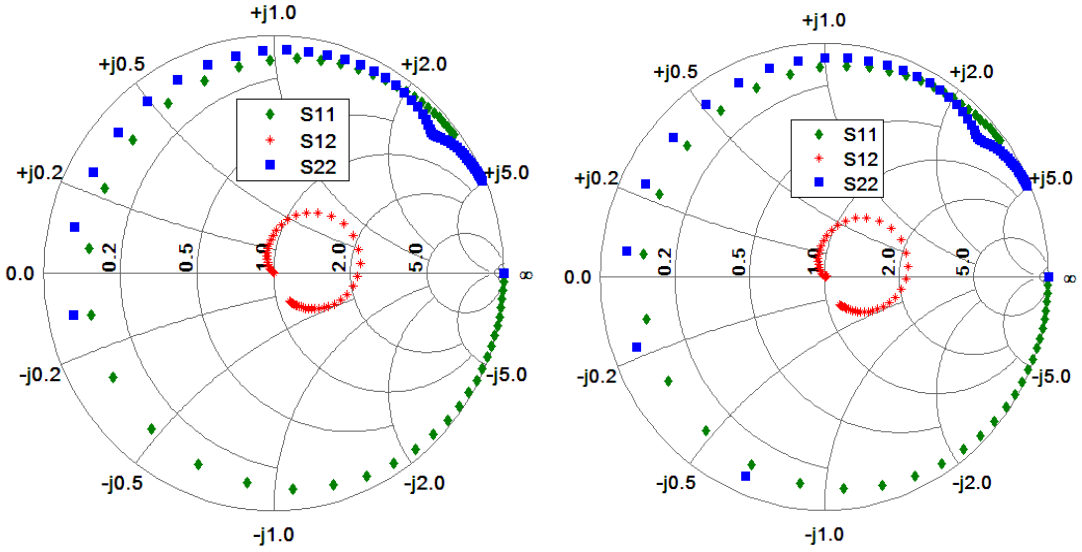
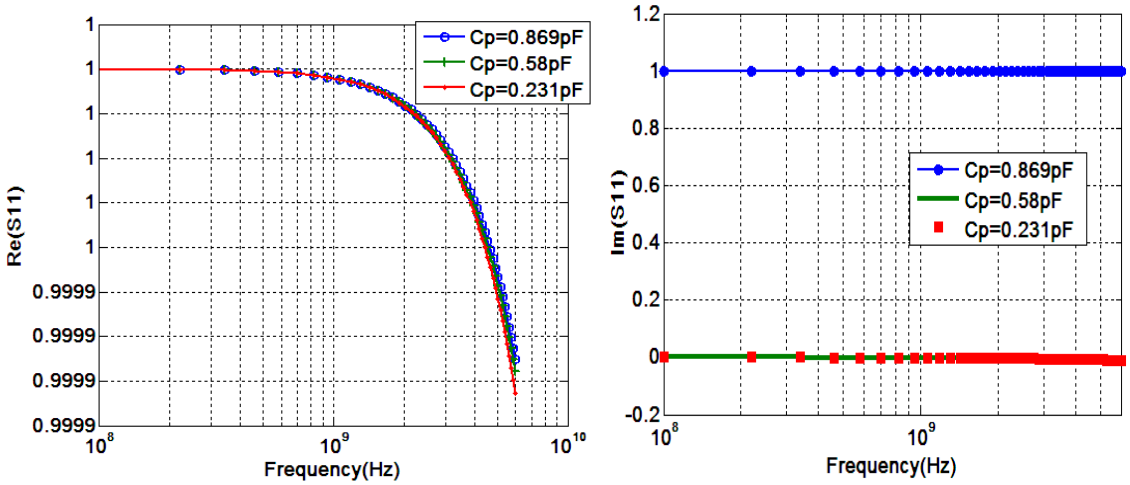



**Figure 3.15:** S-parameter variation with frequency in Smith chart for (a) Cp=0.869pF and (b) Cp=0.231pF.

Following parameter values are used for simulation purpose according to [3.25], $C_g=20\times10^{-18}F$, $C_s=50\times10^{-18}F$, $C_d=50\times10^{-18}F$, $R_s=1\times10^{5}\Omega$, $R_d=1\times10^{5}\Omega$, $R_G=2.1\Omega$, $R_D=1.7\Omega$, $R_S=1.3\Omega$, $L_G=25.8\times10^{-12}H$, $L_S=9.50\times10^{-12}H$, $L_D=32.2\times10^{-12}H$, $C_0=9\times10^{-18}F$, $C_p=0.58\times10^{-12}F$, $C_{GS}=1.16\times10^{-15}F$, $C_{DS}=0.38\times10^{-15}F$, $C_{GD}=1.6\times10^{-15}F$, $Z_0=50\Omega$. The resistance and inductance values are utilized according to [3.37]. The effect of $C_p$ is investigated by changing the value and keeping rest of the parameters as it is.

According to the previously reported article on RF-SET [3.38] the $C_p$ values are considered as 0.869pF and 0.231pF. The change in the different S-parameter is detected with the Smith chart exhibited in figure 3.15 (a), (b) and (c) for $C_p$=0.869pF and 0.231pF respectively. $S_{22}$ and the $S_{11}$ are presented by a green rhombus. As theoretically the values of $S_{12}=S_{21}$, only $S_{12}$ is shown in the figures. It is detected that the parameter $S_{22}$ is predominantly affected by the change in $C_p$. With rising value of $C_p$, $S_{22}$ turns into more capacitive as most of its values prevail in the upper half of the Smith chart. The considered frequency range is 100MHz to 6GHz for Smith Chart plotting.




(a) (b)

**Figure 3.16**: Variation of (a) Re($S_{11}$) (b) Im($S_{11}$) with frequency for $C_p$=0.869pF,0.58pF and 0.231pF.

The study of the S parameter real parts and the imaginary part deviation is crucial as the real part of S-parameter is analogous to the magnitude of power and the imaginary part, on the other hand, represents the phase angle. The variation of Re($S_{11}$) and Im($S_{11}$) is plotted in figure 3.16 (a) and (b) with different $C_p$. Figure 3.16 (a) displays the variation of Re($S_{11}$) with frequency for different $C_p$. Here $C_p$ is considered as 0.869pF, 0.58pF and 0.231pF. For all $C_p$ values Re($S_{11}$) is below 1 (at f=100MHz,0.999999979 with $C_p$=0.869pF ,0.999999979999932 with $C_p$=0.58pF and 0.999999976 with $C_p$ 0.231pF). Along with the reduction in values of $C_p$, Re($S_{11}$) reduces slightly (at frequency 6GHz , Re($S_{11}$)=0.999927 with $C_p$=0.231pF; Re($S_{11}$)=0.999932 with $C_p$=0.58pF and Re($S_{11}$)=0.999935 with $C_p$=0.869pF ) with rising frequency in the GHz range. With $C_p$=0.869pF the Im($S_{11}$) stays almost constant for the chosen frequency range at nearby 1 (0.999999979 at f=100MHz and 0.999934787 at f=6 GHz). For $C_p$ 0.58pF and 0.231pF, value of Im( $S_{11}$) is constant at 0 for the entire frequency range . This is depicted in the figure 3.16 (b).

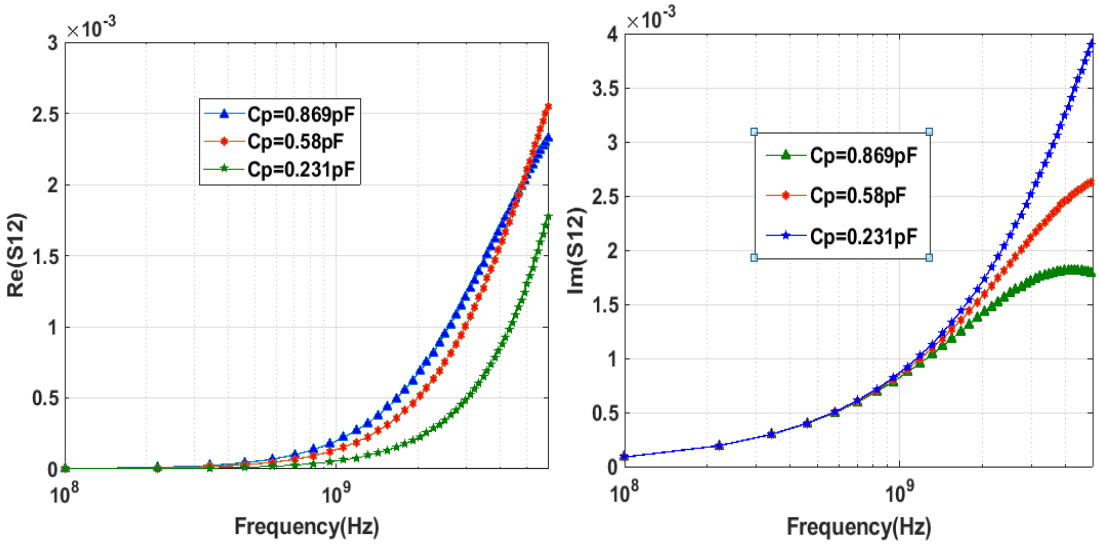



**Figure 3.17:** Variation of (a)Re($S_{12}$) and (b)Im($S_{12}$) with frequency for Cp=0.869pF,0.58pF and 0.231pF.

The variation of $Re(S_{12})$and $Im(S_{12})$ with different $C_p$ and increasing frequency is examined with the figure 3.17 (a) and (b). From figure 3.17(a) it can be easily found that with rising $C_p$ values $Re(S_{12})$ increases subsequently starting from 500MHz to the gigahertz range. Similarly the $Im(S_{12})$ increases with frequency for all the $C_p$ values depicted in figure 3.17(b). but with less $C_p$ value increase in $Im(S_{12})$ is more observable.

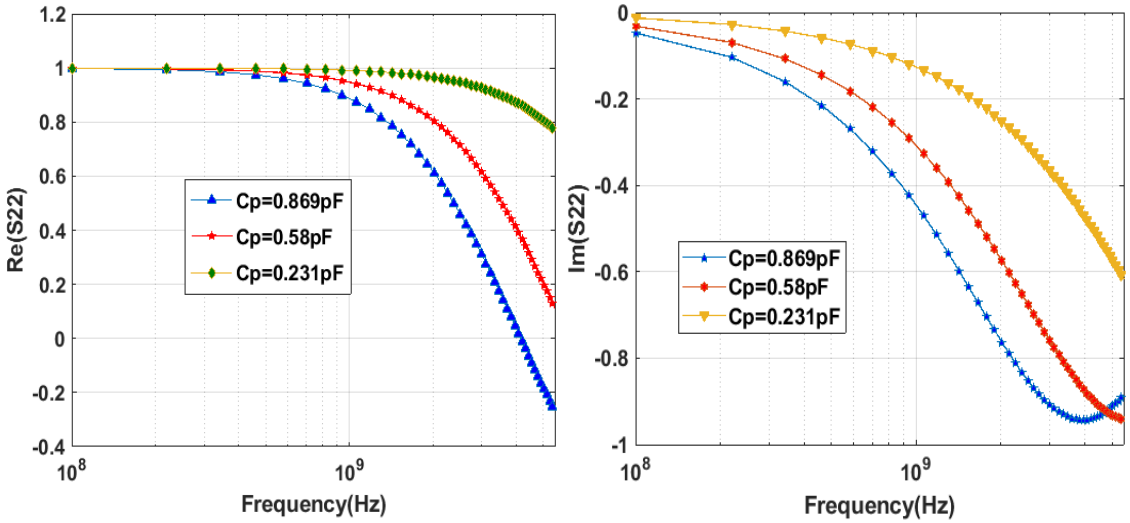



**Figure 3.18:** Variation of (a)$Re(S_{22})$, (b) $Im(S_{22})$ with frequency for $C_p$=0.231aF,0.58aF,0.869aF

Figure 3.18 (a) and (b) reveals if $C_p$ value increases the $Re(S_{22})$ and $Im(S_{22})$ decreases. The maximum value of the real part of $S_{22}$ is 1 while the maximum value of the imaginary part is nearby 0.

The effect of $C_p$ on the stability factor k and $G_{TUmax}$ is studied with the figure 3.19 and 3.20 respectively.

The circuit seems to be conditionally stable as the k is below 1 for all the values of $C_p$ throughout the frequency range as per figure 3.19.

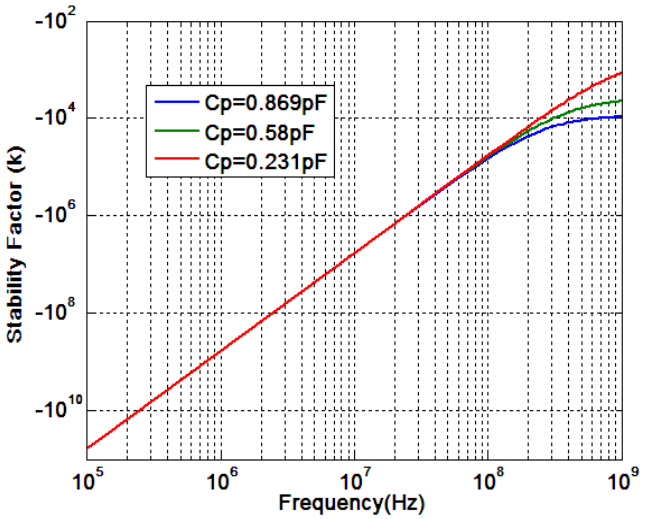



**Figure 3.19:** Variation of stability factor k with frequency with for $C_p$=0.869pF, 0.58pF and 0.231pF.

In figure 3.20 , $G_{TUmax}$ (maximum unilateral transducer power gain) is portrayed against the frequency. $G_{TUmax}$ (in dB) rises linearly up to 10MHz frequency.From 10MHz onwards it increases exponentially and attains the peak value of 55dB. The maximum $G_{TUmax}$ value is 55dB for all the $C_p$ values. Higher the $C_p$ value $G_{TUmax}$ obtains the peak in more lower frequency. After attaining the peak value, with the further rise in frequency value, $G_{TUmax}$ falls.

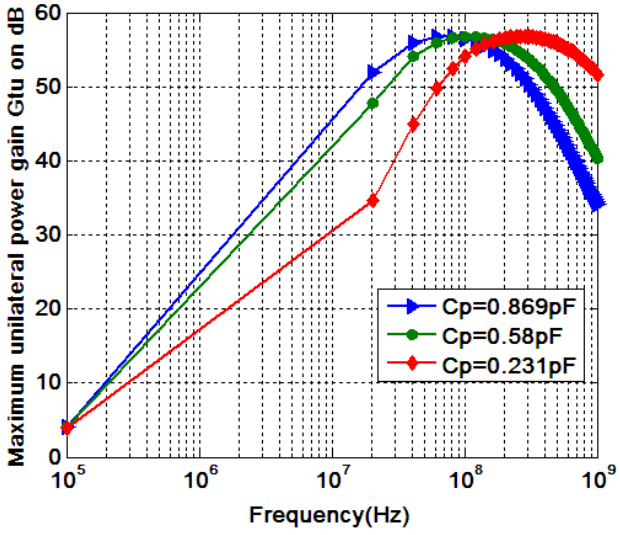



**Figure 3.20:** Variation of maximum unilateral transducer power gain ($G_{TUmax}$) in dB with the frequency with for $C_p$=0.869pF, 0.58pF and 0.231pF.

### 3.4.2.2 Dependency on $R_S$, $R_D$, $R_G$

The dependency of S-parameters on the series resistance $R_S$, $R_D$ and $R_G$ is investigated through the Smith Charts plotted in figure 3.21 (a), (b) and (c).$R_S$,$R_D$, and $R_G$ are respectively connected to the source, drain and the gate terminals of the intrinsic-SET model.The parasitic resistance values considered for Smith Chart plot are 0Ω, 10Ω and 100Ω respectively

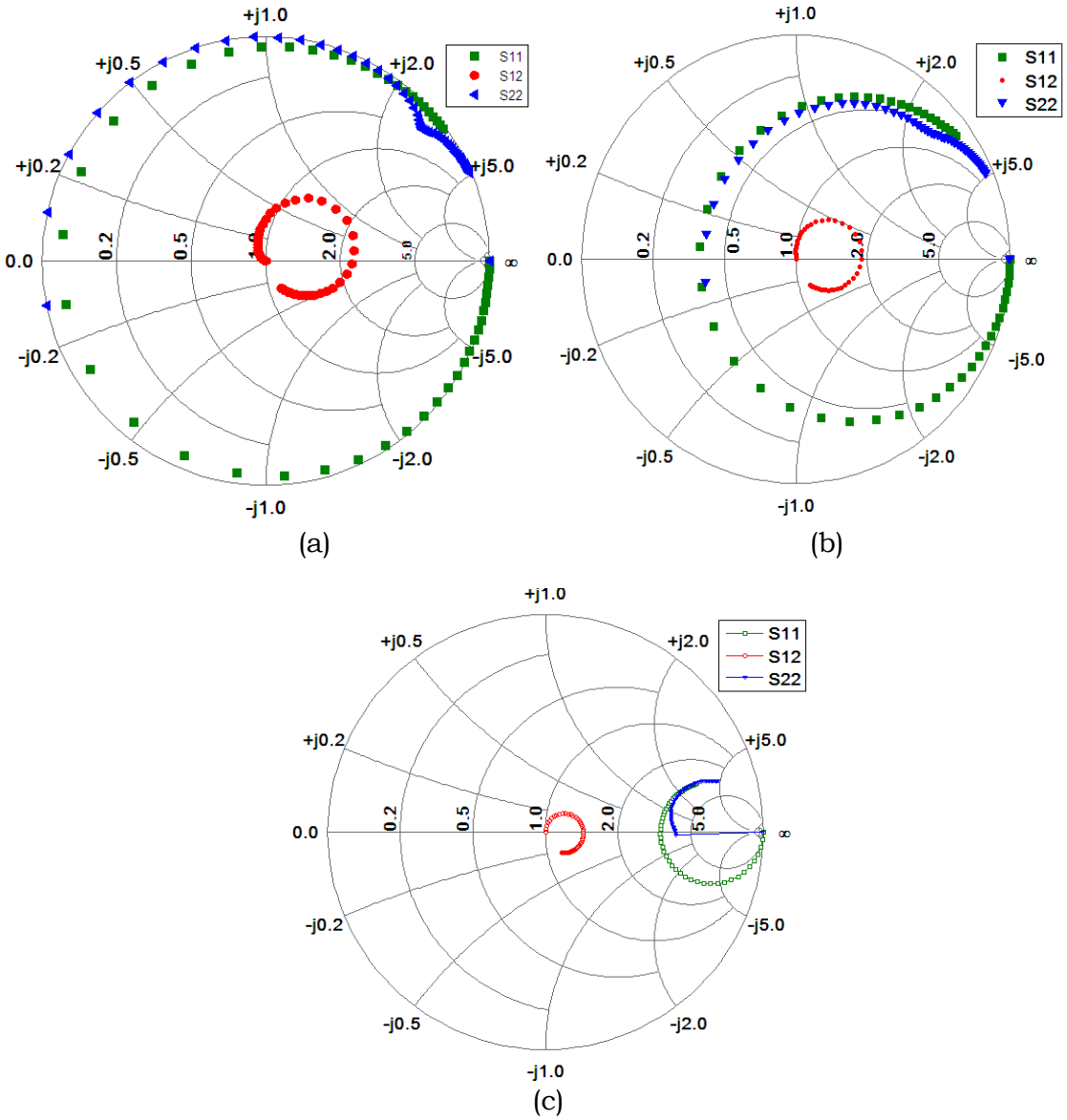



**Figure 3.21:**.S parameter variation with frequency for (a) $R_S$=$R_D$=$R_G$=0Ω,(b)$R_S$=$R_D$=$R_G$=10Ω and (c)$R_S$=$R_D$=$R_G$=100Ω

In figure 3.21 (a) variation of $S_{11}$, $S_{12}$ and $S_{22}$ parameter is revealed for frequency variation. The locus curve of $S_{11}$ begins from $S_{11} \approx 1 = \infty * Z_0$ for low frequency. Here the values of the three resistors are considered as 0Ω. Along with the rising frequency, the curve turns clockwise into the lower capacitive region of the chart and after that in the upper inductive region. Initially, the $S_{12}$ parameter starts from the mid-point of the Smith Chart and turns clockwise. For the lower frequency range, it stays in the upper half of the chart and it turns to the capacitive part of the chart for upper frequencies. The figure 3.21 (b) and (c) is depicted for10Ω and 100Ω. The gradual increase in parasitic resistance value affects the magnitude as well as the phase angle of all the S-parameters. Both the magnitude and phase angle are reduced with frequency when $R_S$,$R_D$ and $R_G$ attains higher value from 10Ω to 100Ω shown in figure 3.21 (b) and (c).

### 3.4.2.3 Dependency on $L_S$, $L_D$ and $L_G$

The parasitic inductances and consequences of their variation on the SET S-parameters are investigated in this section. Keeping all the extrinsic inductance values at 0H , the $S_{11}$,$S_{12}$, and $S_{22}$ are plotted in the Smith chart with frequency variation in figure 3.22 (a). Throughout the frequency range $S_{12}$ lies down in the middle point of the chart. Rest of the two parameters $S_{11}$ and $S_{22}$ remain in the lower half for all the frequencies.

The starting point for both is $\infty * Z_0$. Figure 3.22 (b) also provides, plotted with $L_S$=$L_G$=$L_D$=10fH, similar results to the figure 3.22 (a) no such variation of parameters is observed in this figure. So from this figure, it can be predicted that from 0 to 10fH values of extrinsic inductance no such deviation is seen. The prominent change in the $S_{11}$,$S_{12}$ and $S_{22}$ value for $L_S$=$L_D$=$L_G$=10pH is illustrated in figure 3.22 (c).

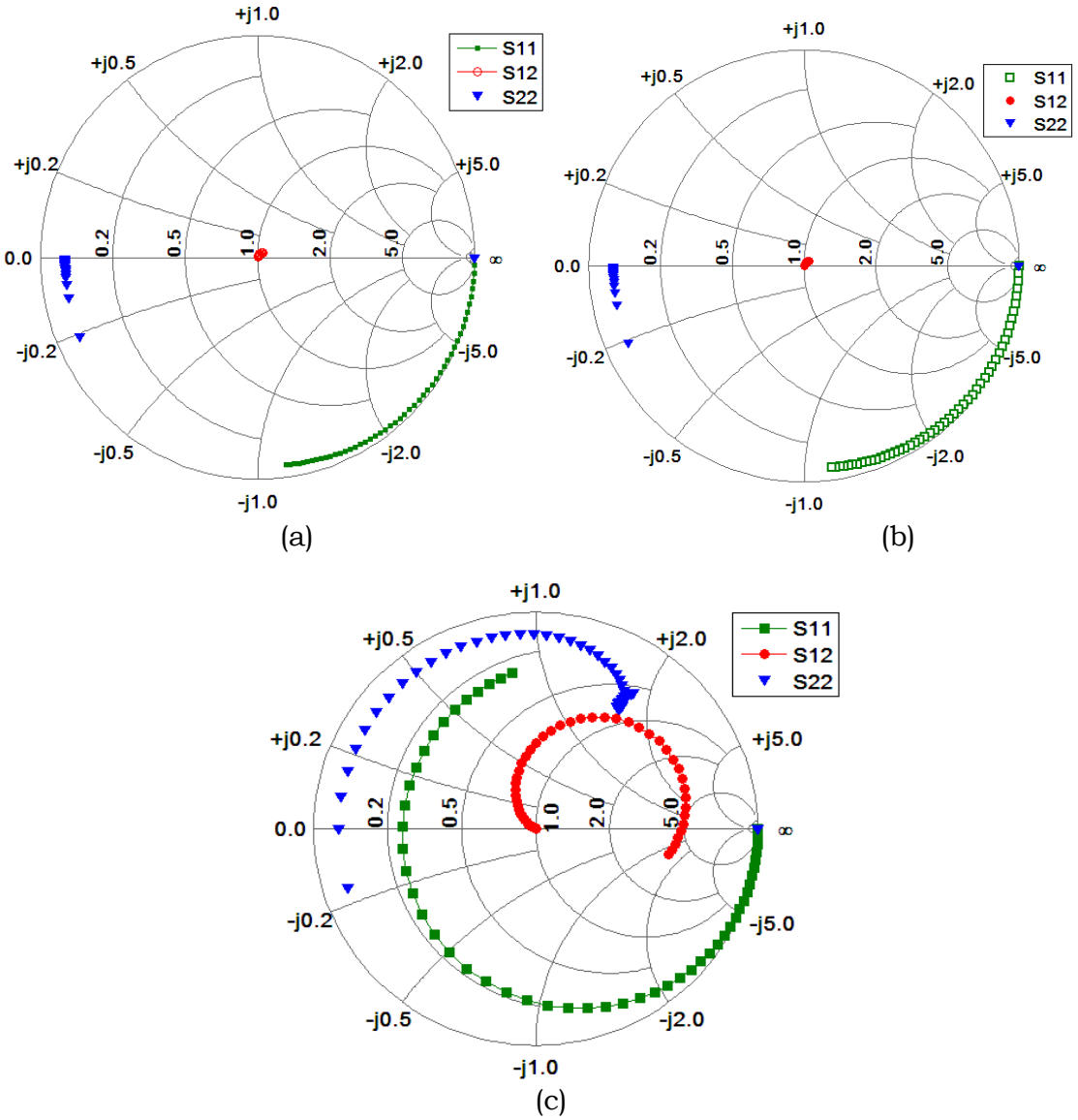



**Figure 3.22**: Smith Chart of SET, $S_{11}$, $S_{12}$, $S_{22}$ with $L_S$=$L_G$=$L_D$=0H(a), (b) $L_S$=$L_G$=$L_D$=10fH, (c) $L_S$=$L_G$=$L_D$=10pH.

$S_{12}$ remains mostly in the inductive region for increasing frequency. The inductive effect is clearly noticeable on the values of $S_{22}$ and $S_{11}$from the figure.

### 3.4.2.4 Parasitic parameter extraction:

The simplified version of the figure 3.11 network is demonstrated in figure 3.23 (a). In this figure, a black box is used to represent the

intrinsic part which is connected to other SET extrinsic elements. To extract the parasitic elements the circuit is considered to be at CB with gate-to-source and drain-to-source voltages both at 0V. With this condition the inner intrinsic part becomes open circuit as no current flows in the CB region.

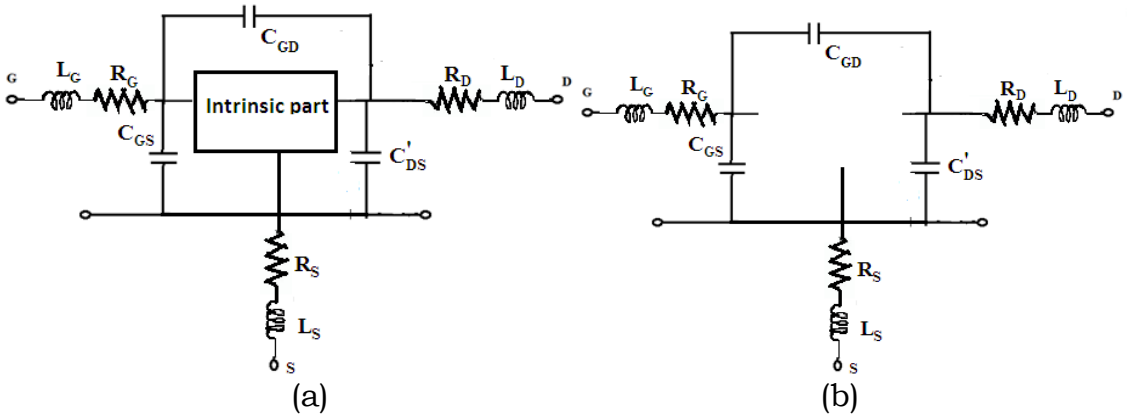



**Figure 3.23**: (a) Simplified network of figure 3.11 (b) Simplified network at Coulomb Blockade

The figure 3.23 (b) shows the simplified circuit in the CB. The circuit depicted in figure 3.23(b) can be evaluated as a combination of a π and a T network. The pi network is formed with the parasitic capacitances and the T network comprises of series resistors and inductors. To extract the extrinsic parameters from the network this simplification is done. The following steps describe the extraction procedure of parasitic elements.

a. Step 1: Z-parameters of the total circuit is determined ($Z_{total}$).
b. Step 2: Convert $Z_{total}$ to $S_{total}$
c. Step 3: Form $Z^P$ from the T network of parasitic elements.
d. Step 4:Strip off series inductances and resistances and determine ($Z^I = Z_{total} - Z^P$)
e. Step 5: Convert $Z^I$ to $Y^I$
f. Step 6:Strip off parasitic capacitances .Build $Y^P$ from π model
g. Step 7:Determine intrinsic Y parameters ($Y^i = Y^I - Y^P$)

The equivalent π network Y parameters can be denoted with the expression (3.28). The extracted parasitic capacitance values are shown in equation (3.29)-(3.31)

$$Y^P = \begin{bmatrix} Y_{11}^P & Y_{12}^P \\ Y_{21}^P & Y_{22}^P \end{bmatrix} \tag{3.28}$$

$$C_{GD} = -\frac{\mathrm{Im}\left(Y_{12}^P\right)}{2\pi f} \tag{3.29}$$

$$C_{GS} = \frac{\mathrm{Im}\left(Y_{11}^P + Y_{12}^P\right)}{2\pi f} \tag{3.30}$$

$$C_{DS'} = \frac{\mathrm{Im}\left(Y_{11}^P + Y_{22}^P\right)}{2\pi f} \tag{3.31}$$

$Z^P$ formed from the T network is defined with the expression (3.32).

$$Z^P = \begin{bmatrix} Z_{11}^P & Z_{12}^P \\ Z_{21}^P & Z_{22}^P \end{bmatrix} \tag{3.32}$$

The extrinsic inductance ($L_S$,$L_D$,$L_G$) and resistance parameters ($R_G$,$R_D$,$R_S$) can be extracted from the $Z^P$ shown in the following expressions (3.33)-(3.38)

$$L_S = \frac{\mathrm{Im}(Z_{12}^P)}{2\pi f} \tag{3.33}$$

$$L_D = \frac{\mathrm{Im}(Z_{22}^P - Z_{12}^P)}{2\pi f} \tag{3.34}$$

$$L_G = \frac{\mathrm{Im}(Z_{11}^P - Z_{12}^P)}{2\pi f} \tag{3.35}$$

$$R_G = \mathrm{Re}(Z_{11}^P - Z_{12}^P) \tag{3.36}$$

$$R_D = \mathrm{Re}(Z_{22}^P - Z_{12}^P) \tag{3.37}$$

$$R_S = \mathrm{Re}(Z_{12}^P) \tag{3.38}$$

It is possible to extract these parasitic elements by subtracting the intrinsic parameters from the total parameters as mentioned in the steps.

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# Chapter 4

# SINGLE ELECTRON THRESHOLD LOGIC BASED CIRCUIT IMPLEMENTATION



## 4.1 Introduction

The typical Boolean logic is still predominantly used for designing the arithmetic logic unit of present computers. CMOS based circuit implementation has been proved quite effective with high speed and compact design. Single Electron Tunneling Technology (SETT)[4.1]-[4.3] which reveals switching behavior entirely different from CMOS, can be utilized for more efficient design style.

In the preceding two chapters, the emphasis is given to the modeling of the SET [4.4]-[4.6]. This chapter demonstrates the detailed circuit design and implementation of SED circuits.

The SETT based research work is broadly classified into two areas-

a. Device research which is mainly based on the fabrication aspects of the device
b. Application of SED in logic and memory circuit design.

Most of the SETT research has intensified on the device level but a very limited amount of circuit, system level innovation has occurred so far. While designing any SED based circuit primarily the adopted design style is CMOS-like [4.6]-[4.10]. Being one of the SEDs, the SET can mimic the MOS behavior under proper bias condition and in this way it can be used in place of either p-MOS (p channel MOS) or n-MOS (n channel MOS). Thus the standard Boolean logic functions are implemented with the SET circuits in CMOS-like fashion. These circuits however require transportation of more number of electrons for switching the output value. As a result the energy consumption and delay are increased. Such attempts result into limited use of the promising attributes of the technology itself. Being one of the emerging options of the nanodevices SED can be used efficiently for circuit, device and systems if its exclusive behavior is properly utilized. The transportation of one by one electron is the unique feature of SED. It can be used for encoding the Boolean logic. The presence and absence of electron is encoded as the logic '1' and logic '0'. For transportation of charge a voltage threshold (known as the critical voltage) needs to be crossed. This introduces the Single Electron Threshold Logic Gate approach (SE-TLG) [4.11]-[4.13] by combining the technological concept of SET with TLG, which uses Single Electron Encoded Logic (SEEL) as principle of operation.

The generic SE-TLG is composed of passive elements such as capacitors and a tunnel junction. Generally, a strong crosstalk occurs by virtue of the construction of SE-TLG based network and leads to erroneous behavior. For SE-TLG paradigm output value switches due to the two types of cross talks -

i. Supply voltage
ii. Charge transportation

These crosstalks can be dramatically reduced by using active buffers [4.14]-[4.15] to the back end of the passive SE-TLGs.

The energy dissipation of a SED is related to the number of junctions involved in electron tunneling. As circuits designed with SE-TLG approach requires less number of tunnel junctions they consume less amount of power than the CMOS-like SET based circuits.

This chapter deals with the architecture and working technicalities of the SE-TLG based five input majority gate circuit and a Programmable Logic Array (PLA) circuit. The power consumption and the delay analysis of the designed two circuits are elaborated in this chapter.

## 4.2 Literature Survey

In 1987 Likharev and Semerov proposed physical charge transport [4.20] between gates so that the presence and absence of electron can generate the Boolean signals. Later in 1992 Nazarov and Vyshenskii suggested to scale down the transport of charge [4.21] to a few numbers of electrons. This approach introduced the SEEL when the transport of charge was reduced to only a single electron. To date the SED based circuit design is focused on the application related to the memory [4.22]-[4.27]. In spite of having several technological constraints several SED logic architectures are reported [4.28]-[4.33]. Tucker first developed the SET inverter circuit[4.34], and the modification to that circuit was incorporated by Likharev [4.35]. Most of the earlier works on SED was based on the CMOS-like implementation of the circuits majorly for the digital applications [4.6],[4.7]. A CMOS-like NOR gate [4.19] was introduced by Chen et al. in 1996. The re-utilization of the tools and previous knowledge is the only plus point of the CMOS based circuit design. But this technique of circuit design does not use the special features of the SED to its full extent. One of the popular design style based on the Binary decision diagram (BDD)[4.29],[4.36]-[4.37] concept have been also used by some researchers for designing the SED logic

circuits. The majority logic gate based design style was proposed by Oya et al.[4.38]. The implementation methodology is different from the Boolean logic as the digital logics are manipulated according to the majority decision. Another different type of single electron logic circuit was proposed by Yamamura and Suda [4.39] with CIST(Charge-induced-Signal-Transmission). A programmable SET [4.40] was demonstrated by Uchida et al. The implementation of XOR [4.41] and XNOR [4.42] with SED was done by Takahashi and Saitoh respectively. Later on Kitade et al. also demonstrated a room temperature XOR with Si-SET [4.43]. A generic TLG [4.12] was contemplated by Lageweg et al. Avedillo et al. in 1995 introduced the TLG concept with CMOS [4.44]. SE-TLG based clocked coupled inverters were implemented by J. F. Ramos et al. [4.11] in 1998. A PLL circuit [4.45] was proposed by Zhang in 2007.The circuit for binary encoder with n-bits [4.46] was proposed by Rehan in 2012. Bahrepour and Sharifi proposed an application of linear TLG Full adder to design a 4-2 compressor [4.47] in 2013. A sequence generator [4.48] circuit with SED was designed by Samanta et al. in 2010. Design of Flip-flops [4.49] was also reported previously by Lageweg et al. in 2004. RAM cell with SE-TLG was designed by Abutaleb in 2013 [4.13].A 4:1 multiplexer [4.50] design with the same was introduced in 2012 by Jain and Sarkar. A detailed design of a four bit carry look ahead adder [4.51] with SE-TLG was elaborated in 2015. Recently SE-TLG based 3:8 decoder circuit [4.52] and Feynman Gate [4.53] is also reported. Through the rigorous literature study it is clear enough that there are several important logic circuits yet to be implemented by SE-TLG for getting a compact and power efficient version of the same.

## 4.3 Threshold Logic Gate

The core concept of the SETT is the transportation of charge through tunnel junction. For tunneling to tunneling to occur Vj (junction voltage) must cross the critical voltage Vc. In TLG, output is computed by comparing the weighted sum with the threshold value. The output is logic '0' when the functional value is less than the threshold and the output is logic '1', if the same is greater than or equal to the threshold.

### 4.3.1 Basic Structure

The symbolic portrayal of threshold gate is depicted in figure 4.1 with threshold T, inputs X1,X2…Xn and weights W1,W2,…….Wn.

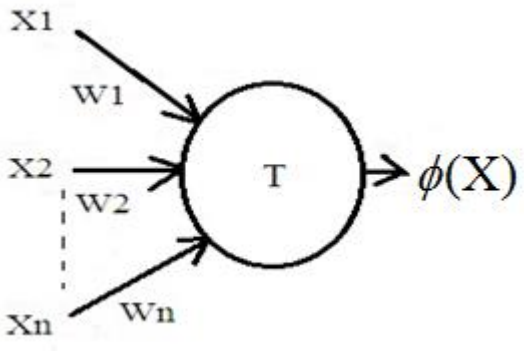



**Figure 4.1:** Threshold logic gate symbol

$$\phi(\mathrm{X}) = sgn\{\Psi(\mathrm{X})\} = \begin{cases} 0 \text{ if } \Psi(\mathrm{X}) < 0 \\ 1 \text{ if } \Psi(\mathrm{X}) \geq 0 \end{cases} \quad (4.1)$$

$$\Psi(X) = \sum_{i=1}^{n} W_i X_i - T \quad (4.2)$$

The decision of the logical output is made with the equation (4.1). The comparison of weighted sum ($\sum_{i=1}^{n} W_i X$) is done with T using equation (4.2).

## 4.4 Single Electron Threshold Logic Gate (SE-TLG)

### 4.4.1 Working of SE-TLG

A simple SE-TLG gate is illustrated in figure 4.2 with the positive and negative nodes marked using x and y. The characteristics of the single tunnel junction involved are defined with the junction, capacitance, resistance, and voltage denoted with $C_t$, $R_t$, Vj.

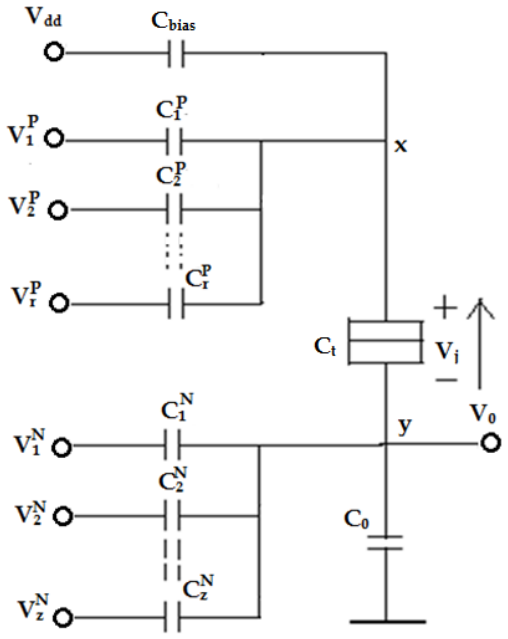



**Figure 4.2:** Structure of a simple SE-TLG

Input voltages and their corresponding weights associated to node x are $V_1^P, V_2^P \ldots\ldots V_r^P$ and $C_1^P, C_2^P \ldots\ldots C_r^P$. Similarly for node y inputs are $V_1^N, V_2^N \ldots\ldots V_z^N$ and weights are $C_1^N, C_2^N \ldots\ldots C_z^N$. The bias voltage and capacitor are denoted with $V_b$, $C_{bias}$. $C_0$ is the load capacitor. The threshold computation is done with following expression (4.3).

$$T = \frac{1}{2}(C_\Sigma^P + C_\Sigma^N)q_e - C_\Sigma^N C_{bias} V_{dd} \qquad (4.3)$$

Where, $C_\Sigma^P = C_{bias} + \sum_{k=1}^{r} C_k^P$ and $C_\Sigma^N = C_0 + \sum_{l=1}^{z} C_l^N$

The function is expressed in equation (4.4)

$$\Psi(X) = C_{\Sigma}^{N} \sum_{k=1}^{r} C_K^P V_K^P - C_{\Sigma}^{P} \sum_{l=1}^{z} C_l^N V_l^N - T \tag{4.4}$$

### 4.4.2 Energy dissipation and Delay calculation

The tunneling of the individual electron is designated by a stochastic process as it is a quantum physical process. It is possible to compute the probability of electron tunneling after the time interval of $t_D$. The charge transport probabilities are thus calculated by applying stochastic modeling of the system. The complexity of the stochastic computation increases when huge numbers of tunneling events are involved. For a single tunnel junction based system it is assumed the probability of tunneling at a time is non-zero for the sake of simplicity. An event chain for which one event is dependent upon the execution of the previous one with a constant rate of tunneling ($\Gamma_R$) can be described by the Poisson process. It is considered the state change occurs up to $n^{th}$ discrete state in the unidirectional way. The initial state is defined with n=0 and from there it evolves to the next states monotonically. The Poisson process equation is defined in the following expression (4.5).

$$P_n(t) = \frac{(\Gamma_R t)^n}{n!} e^{-\Gamma_R t} \tag{4.5}$$

For n=0 and $t=t_D$

$$P_e = P_0(t_D) = e^{-\Gamma_R t_D} \tag{4.6}$$

If no charge transport occurs after $t_D$ amount of time the probability is defined by $P_0(t_D)$ also known as the probability of error ($P_e$) expressed with

equation (4.6). The minimum amount of delay to reach the $(1-P_e)$ accuracy of switching is computed as in equation (4.7).

$$t_D = \frac{-\ln(P_e)}{\Gamma_R} \tag{4.7}$$

Where $\Gamma_R = \left(|V_j| - V_c\right) / q_e R_t$

The tunneling rate of SED is expressed as (4.8)

$$\Gamma_R = \frac{-\Delta F_E}{q_e^2 R_t (e^{\Delta F_E / k_B T} - 1)} \tag{4.8}$$

Here $\Delta F_E$ is the change in free energy which can be computed by summing up the charge stored in the capacitors and the work done by the voltage sources for charge transportation. It becomes complicated to find the $\Delta F_E$ for large circuits with numerous numbers of capacitors, voltage sources and the tunnel junctions. This problem can be resolved with an introduction to the equivalent capacitance $C_{equ}$ for complete circuit consisting of all the tunnel junctions and the capacitors. The simplified expression $\Delta F_E$ is shown in equation (4.9).

$$\Delta F_E = q_e . \left(|q_j| - q_c\right) / C_t \tag{4.9}$$

Where $q_c$ is the critical charge which is related to the critical voltage and $C_{equ}$. The expression of energy change is simplified to the following expression (4.10).

$$\Delta F_E = q_e . \left(|V_j| - V_c\right) \tag{4.10}$$

## 4.5 Circuit Implementation and Simulation with SE-TLG

The circuits built with SE-TLG architecture are simulated with SIMON [4.54]. It is a GUI (Graphical user interface) and circuit editor created

with TCL and TK toolkit [4.55]-[4.56]. The software supports different types of input voltage sources such as constant type, piecewise linear with time and voltage controlled type. The CPU time requirement related to the SIMON based circuit simulation is dependent on the number of tunnel junctions (*j*) and nodes (*n*). A total number of tunnel rates to be calculated for the every tunnel event simulation is twice of the tunnel junction numbers for the normal tunneling. The matrix operations to calculate the voltages and charges of all nodes are quadratically scaled with node number shown in equation (4.11) where, $a_0, a_1, a_2, a_3$ are the three coefficients and CPU time $\tau_{cpu}$.

$$\tau_{cpu} = a_0 + j(a_1 + a_2 x + a_3 x^2) \tag{4.11}$$

The acceleration algorithm is used for reducing CPU time drastically. Temperature and bias voltages are also two factors on which the CPU time depends for accelerated simulation because the number of states increases with increasing bias voltage value and temperature.

The sub-section 4.5.1 ,4.5.2 deals with the detailed design of five input majority gate circuit and function implementation with PLA circuit design respectively. The simulation is done with the SIMON simulator version 2.0.

### 4.5.1 Five Input Majority Gate Circuit

The voting based decision circuits require a majority logic gate [4.36] where a number of votes or same inputs are judged. It primarily contains an odd number of inputs. The judgment based on the majority function can be simply selected. If at least (N+1)/2 inputs are high among N (N is an odd number)inputs, the majority gate results as a logic high otherwise the output remains at logic low. The constructional details for simulation of a five input based majority gate with SE-TLG are presented here. The

output of the majority gate is produced by considering all conditions of the input value. If logic level of the majority number of inputs is high then the output is set to high otherwise low.

The circuit design is portrayed in figure 4.3.This circuit does not suffer from the feedback related issue as only a single TLG is sufficient to generate the output. So there is no requirement to add a backend static inverting buffer to the circuit design. The circuit structure includes a single electron tunnel junction having, a junction resistance, and , junction capacitance. C1 bias capacitor is connected to the bias voltage $V_{dd}$.C2 is the load capacitor or the output capacitor. The input signals are joined to node N1 through input capacitors denoted with Cg. All the gate capacitors work as the weights to the input signals. Five inputs considered in the design are Input 1, Input 2, Input 3, Input 4, and Input 5. The output is extracted from node N2. The output is expressed with following equation (4.12)

$$Output = \overline{Input1}(Output\_Input1\_low) + Input1(Output\_Input1\_high) \tag{4.12}$$

Output_Input1_low and Output_Input1_high denote the overall output result for Input 1 conditions (Logic 0 and Logic 1). The Output_Input1_low is expressed with the equation (4.13). Whereas the expression of Output_Input1_high is presented in equation (4.14).

$$Output\_Input1\_low = \begin{pmatrix} \overline{Input2}.Input3.Input4.Input5 + \\ Input2.\overline{Input3}.Input4.Input5 + \\ Input2.Input3.\overline{Input4}.Input5 + \\ Input2.Input3.Input4.\overline{Input5} + \\ Input2.Input3.Input4.Input5 \end{pmatrix} \tag{4.13}$$

$$Output\_Input1\_high = \begin{pmatrix} \overline{Input2}.\overline{Input3}.Input4.Input5 + \overline{Input2}.Input3.\overline{Input4}.Input5 + \\ \overline{Input2}.Input3.Input4.\overline{Input5} + \overline{Input2}.Input3.Input4.Input5 + \\ Input2.\overline{Input3}.\overline{Input4}.Input5 + Input2.\overline{Input3}.Input4.\overline{Input5} + \\ Input2.\overline{Input3}.Input4.Input5 + Input2.Input3.\overline{Input4}.\overline{Input5} + \\ Input2.Input3.\overline{Input4}.Input5 + Input2.Input3.Input4.\overline{Input5} + \\ Input2.Input3.Input4.Input5 \end{pmatrix} \quad (4.14)$$

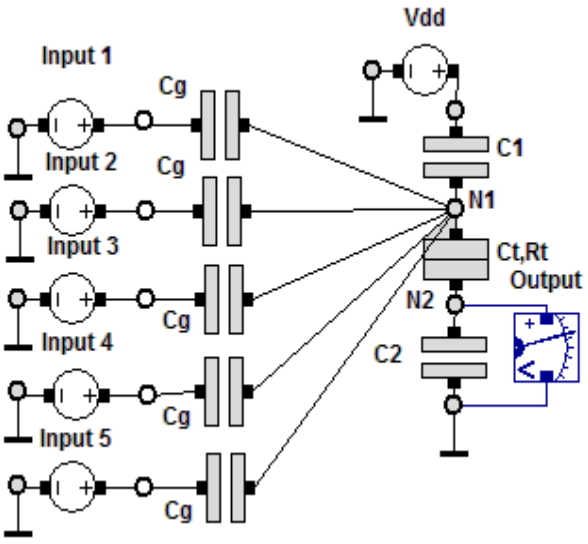



**Figure 4.3:**SE-TLG based Majority Gate with five inputs.

**Table 4.1**: Parameter values of SE-TLG five input Majority Gate

| Parameter | Values |
|---|---|
| Cg | 0.5xCj |
| $C_t$ | 0.1xCj |
| C2 | 10xCj |
| C1 | 10xCj |
| $R_t$ | 0.1MΩ |

The power supply is computed as $0.1q_e / C_j$ where $C_j$ is 1aF. The weighted capacitors connected to node N1 contribute $C_\Sigma^P$ value. Considering the capacitor values from the table 4.1 $C_\Sigma^P$ becomes 12.5aF with $C_b$=C1. Only a single capacitor C2 is connected to node N2 , thus $C_\Sigma^N$ is 10aF where

$C_0$=C2. The area of a circuit is defined by the number of components present. The designed circuit is built with total 8 elements out of which seven are capacitors. According to the basic equation of threshold logic the expression of the five input majority gate can be written as (4.15).

$$Output = \text{sgn}(Input1 + Input2 + Input3 + Input4 + Input5 - 2.5) \quad (4.15)$$

The threshold value is calculated as 2.5 from the equation (4.1) and (4.2).

#### 4.5.1.1 Simulated results of five input majority gate

For the sake of simplification two conditions of the input signal 1 are considered separately , first one is for input 1 at logic low (0V) and second one is for logic high (16mV). The rest of the input signals are used according to the figure 4.4.

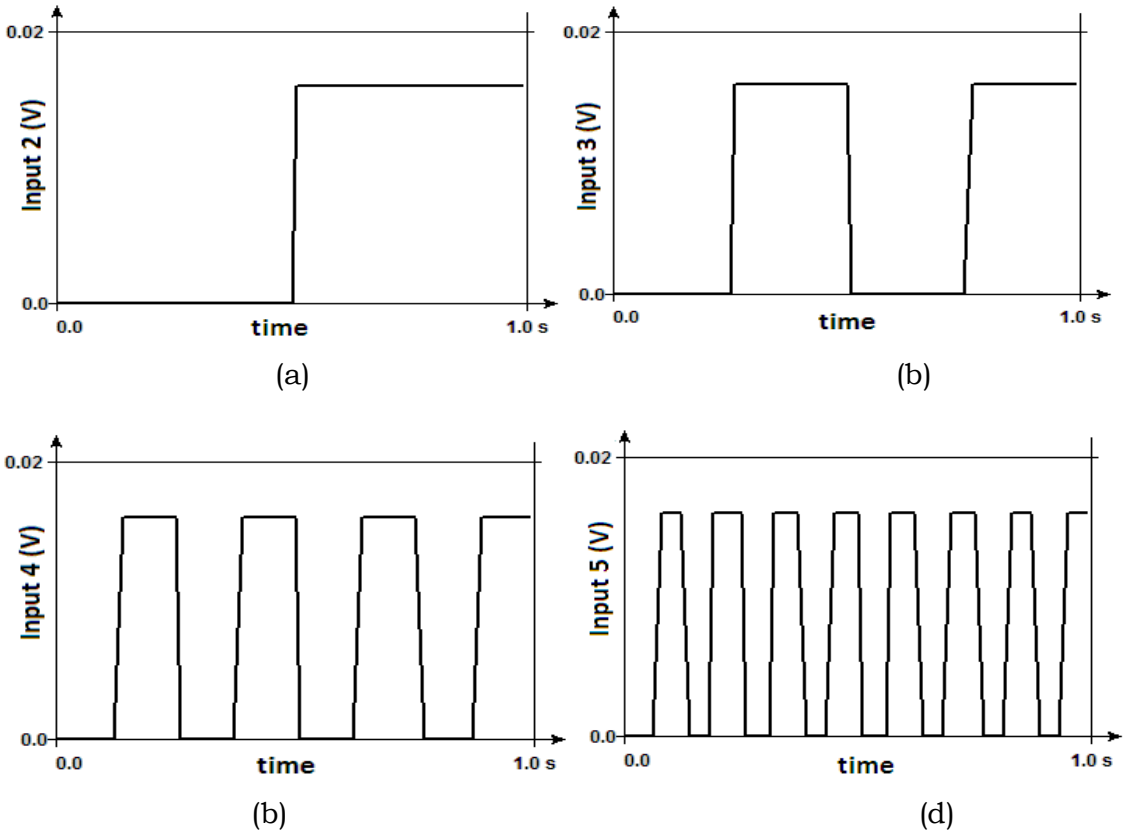
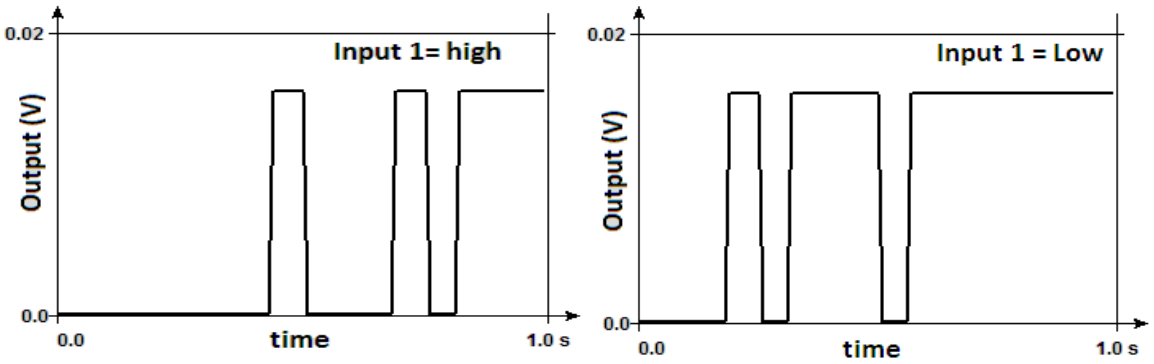



**Figure 4.4:**Waveforms of (a) Input 2,(b)Input 3, (c) Input 4 and (d) Input 5

The amplitude of Input 2, Input 3, Input 4 and Input 5 are plotted with frequency respectively in figure 4.4 (a), (b),(c) and (d). These input signals are plotted with respect to time. For all the signals duty cycle is taken as 50%. But the frequency of all the inputs are varied (frequency of Input 2 is double of Input 1, for Input 3 it is double of Input 2 and so on) to check all the logical combinations of the input signals. Frequency of Input 2 ,3 ,4 ,5 are respectively 1,2,4 and 8Hz. The simulation of the designed circuit is carried out with SIMON software. It uses Monte Carlo technique for the simulation of SEDs. The output signals are furnished in figure 4.5 (a) , (b) for the two logic levels (high and low) of the Input 1 signal respectively. When Input 1, 4, 5 are in high state output is set to high according to majority principle. Similarly when Input 2,3,4,5 or




(a) (b)

**Figure 4.5:**Output waveforms for (a) with high Input 1 and (b) with low Input 1.

2,3,4 or 2,3,5 or 2,3 or 2,5 or 2,4 or 3,4,5 or 3,4 or 3,5 are high in presence of high Input 1 following the majority principle the output stays in logic high. As per the Figure 4.5 (b) output is high for all high input combination of 2,3,5 or 2,4,5 or 2,3,4 or 3,4,5 with low Input 1 satisfying equation (4.13). The output waveforms simulated with SIMON proves the logical functionality of the SE-TLG five input majority gate circuit.

### 4.5.2 Programmable Logic Array

The circuit implementation of the PLA with SE-TLG is presented in this sub-section. The PLA circuit has been designed here for two particular functions F1 and F2 expressed with (4.16) and (4.17).

$$F1 = X_2^{'}X_3^{'} + X_1^{'}X_3 \tag{4.16}$$

$$F2 = X_1^{'}X_2 + X_1^{'}X_3 + X_1X_2^{'} \tag{4.17}$$

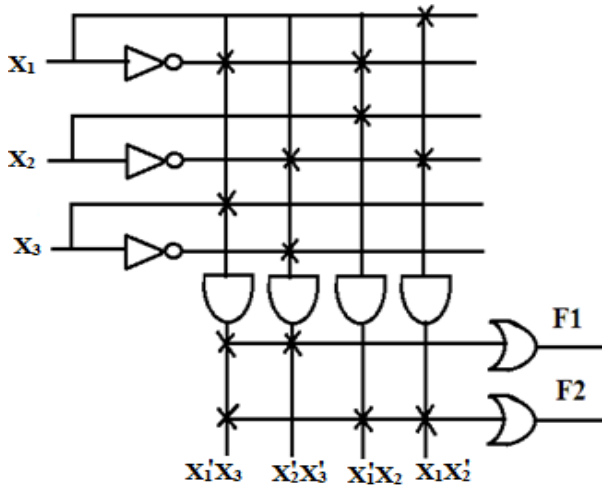



**Figure 4.6**: Conventional Boolean logic based PLA for function F1 and F2.

The circuit implementation of the above-mentioned functions F1 and F2 in equation (4.16) and (4.17) is depicted in figure 4.6 where $X_1$, $X_2$ and $X_3$ are the three input signals.The conventional circuit is designed with mainly three parts- inverters or NOT gates, AND gates and OR gates. The SE-TLG based circuit design also consists of three layers. First one comprises the input signals X1, X2, X3 and their inverted forms generated using the NOT gates formed with SE-TLG.The first layer or the layer 1 is revealed in figure 4.7.

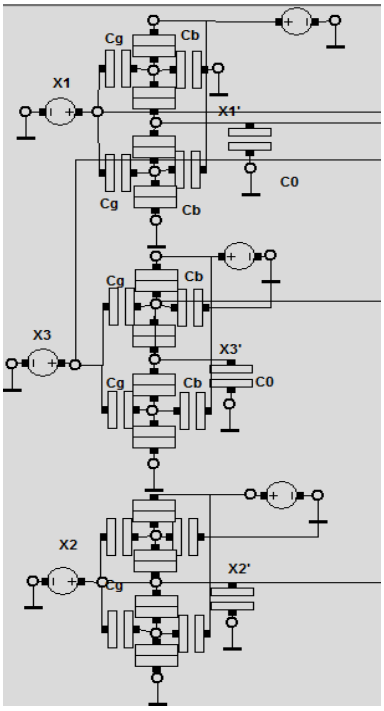



**Figure 4.7:** Layer 1 of designed PLA circuit.

Each inverting buffer gate requires total four tunnel junctions and five capacitors. Structure of a single NOT gate is shown in figure 4.8.

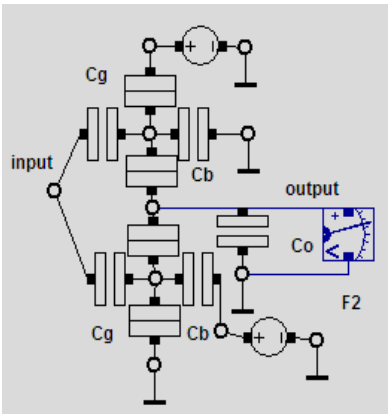



**Figure 4.8**: Inverting buffer or NOT gate

The parameter values of the NOT gate are tabulated using Table 4.2.Gate capacitors and back gate capacitors are denoted with Cg, and Cb respectively.The load capacitor or the output capacitor is $C_0$. The capacitors associated with junction 1,2,3,4 are respectively denoted with

Cj1,Cj2,Cj3 and Cj4. Layer 1 is constructed using three such buffers to form $X_1$', $X_2$' and $X_3$'.

**Table 4.2:** Inverting Buffer parameter values

| Capacitance | Value |
|---|---|
| Cg | $0.5\text{x}10^{-18}$F |
| Cb | $4.25\text{x}10^{-18}$F |
| $C_0$ | $9\text{x}10^{-18}$F |
| $C_{j1}$,$C_{j4}$ | $0.1\text{x}10^{-18}$F |
| $C_{j2}$,$C_{j3}$ | $0.5\text{x}10^{-18}$F |
| $R_t$ | 0.1MΩ |

The output of the first layer is then used as input to the layer 2 consisting of buffered AND gates. The addition of static buffer at the end of each TLG reduces the feedforward and feedback problem of the network of SE-TLGs. The augmentation of the buffers allow proper functioning of the TLGs in a network.

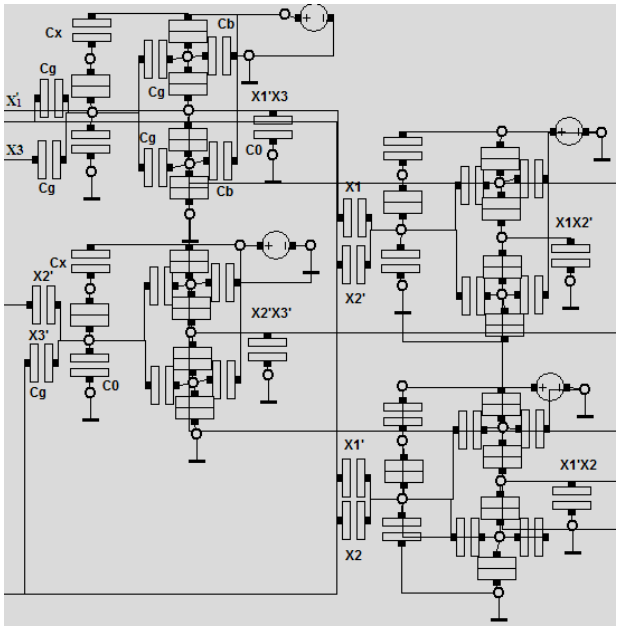



**Figure 4.9**: Layer 2 of designed PLA circuit built with four buffered AND gates.

Layer 2 generates the outputs as $X_2'X_3'$, $X_1'X_3$, $X_1'X_2$ and $X_1X_2'$ using the first layer input and the outputs shown in figure 4.9. The individual

buffered AND gate is actually formed combining a TLG based NAND with NOT gate. The expression of SE-TLG NAND with two inputs I1 and I2 is written using equation (4.18). Equation (4.18) is generated from the basic expression (4.1) of threshold logic. Here the threshold value T is of 1.5. As this one is a two input NAND gate the two input capacitors are connected to the negative node 'y' of the threshold gate structure shown in figure 4.2.

$$NAND(I_1, I_2) = \text{sgn}\{-I_1 - I_2 + 1.5\} \tag{4.18}$$

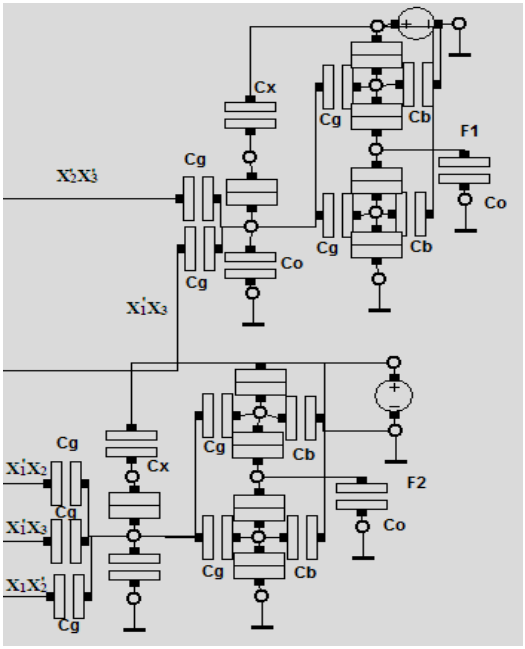



**Figure 4.10**: Layer 3 of designed PLA consisting of two OR gates

Layer 3 of the PLA design is for the OR plane where two buffered SE-TLG OR gates are used to generate the ultimate functions F1 and F2 presented in figure 4.10. The construction of the buffered OR gate is done with NOR and NOT gate. The basic threshold logic equation of two inputs NOR gate is shown in equation (4.19).

$$NOR(I_1, I_2) = \text{sgn}\{I_1 + I_2 - 1.5\} \tag{4.19}$$

Entire circuit of PLA combining all the three layers is depicted in figure 4.11.

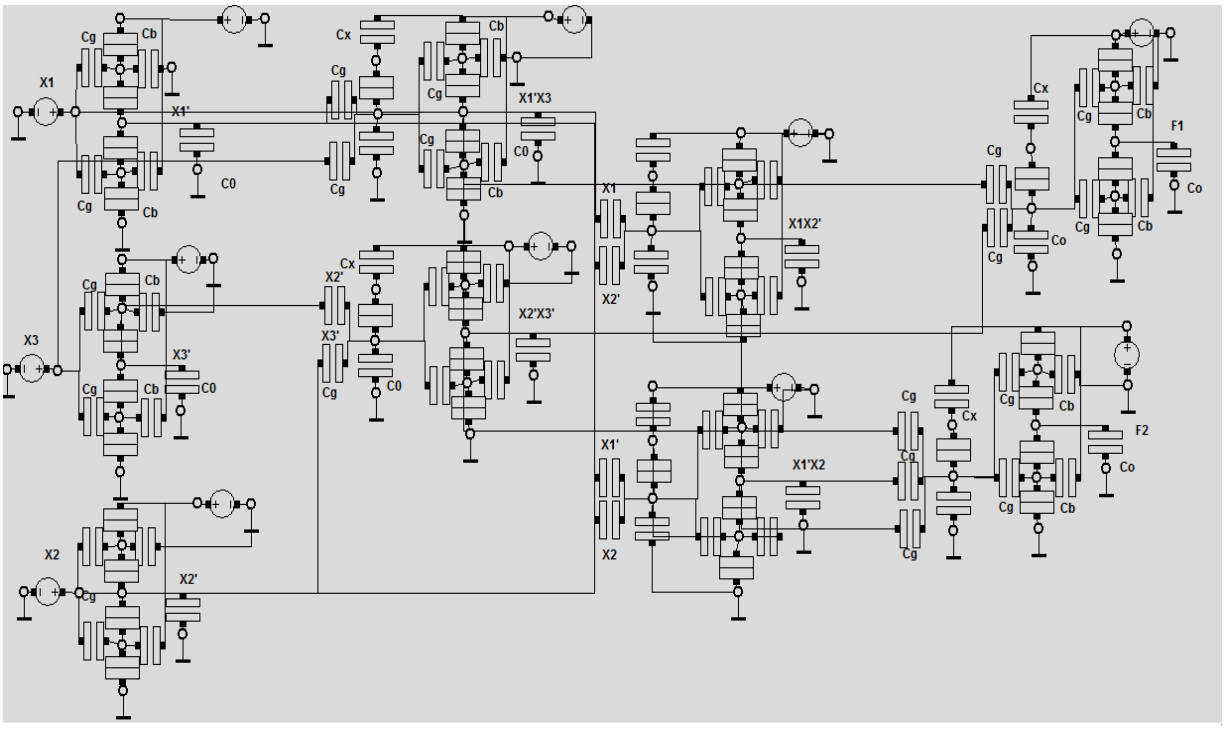



**Figure 4.11**: PLA circuit design with a SE-TLG approach

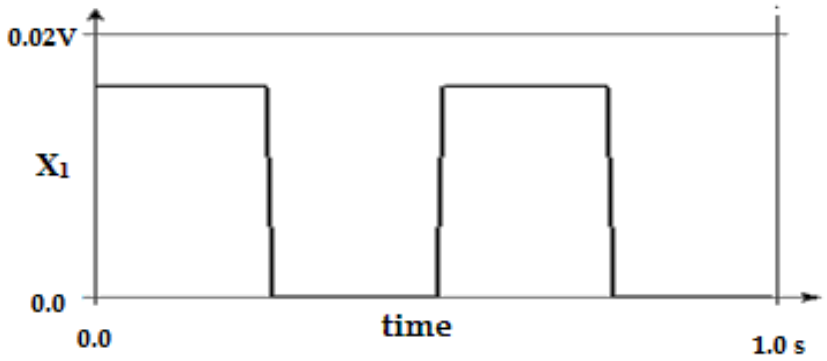
The truth table of the PLA is provided in Table 4.3 where the input signal is $X_1$,$X_2$, and $X_3$. It is required to verify the logical output of the functions F1 and F2.

**Table 4.3**: Truth Table of the PLA circuit with inputs $X_1$,$X_2$,$X_3$ and functions F1, F2 .

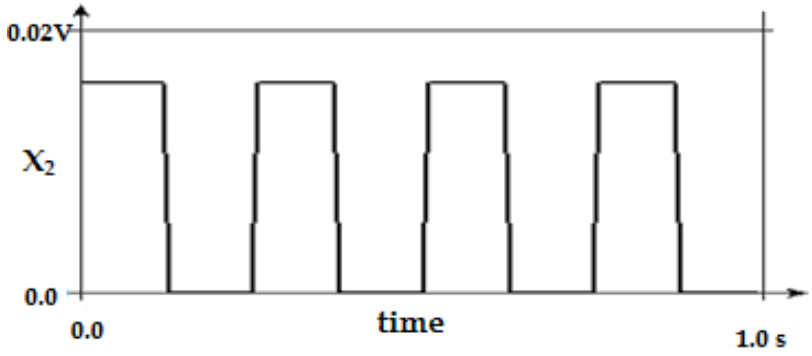
| $X_1$ | $X_2$ | $X_3$ | F1 | F2 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |

### 4.5.2.1 Simulated results of designed PLA

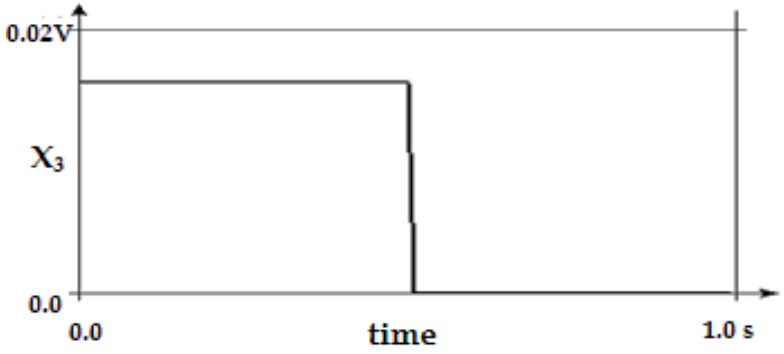
The designed PLA circuit is simulated with SIMON 2.0. The input signals $X_1$, $X_2$, and $X_3$ are depicted in figure 4.12 (a), (b) and (c) respectively. Here all the inputs are considered to have a duty cycle of 50%. Logic '0' signifies 0Volt and Logic '1' signifies 16mV.




(a)




(b)




(c)

**Figure 4.12**: Simulated input signals (a) $X_1$ (b) $X_2$ and (c) $X_3$ where voltage level of logic '0' is 0.0V and the voltage level of logic '1' is 0.016V.

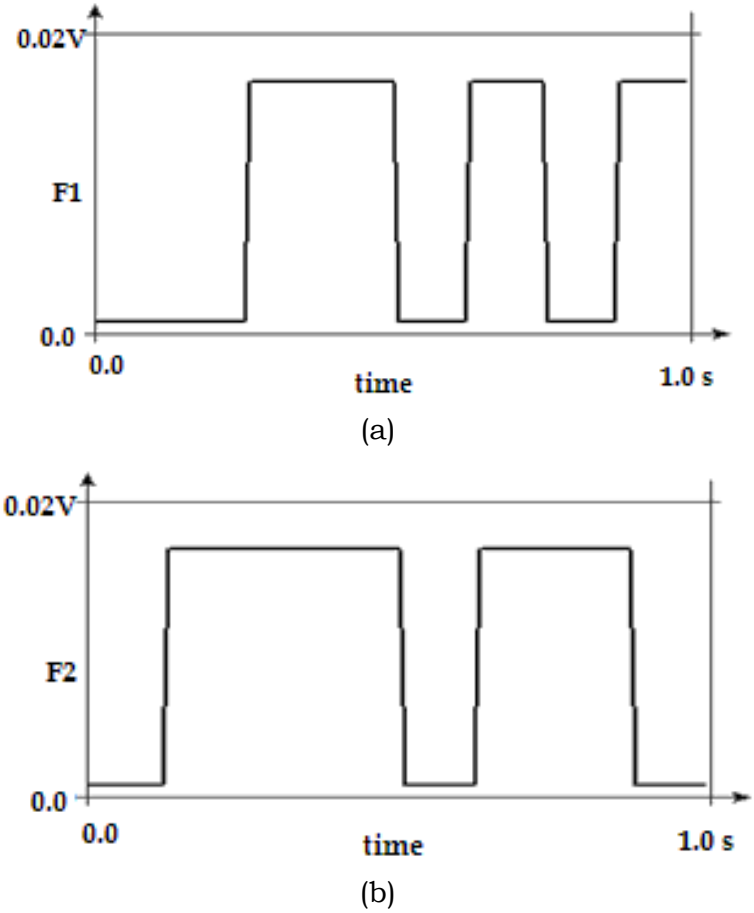



**Figure 4.13:** Simulated output waveforms for (a) F1 and (b) F2 function.

Simulated output waveforms for the two functions F1 and F2 are depicted in figure 4.13 (a) and (b) respectively. It can be observed in figure 4.13 (a) and (b) both that they clearly follow the logical behavior according to the truth table shown in Table 4.3. For the output functions also the logic 'high' or '1' is denoted with 16mV and the logic 'low' or '0' is interpreted with 0V. The simulated results justify the correct operation of the designed circuit and prove that it has been successfully implemented using the single electron buffered threshold logic.

## 4.6 Power Consumption and Delay of designed circuits

The power consumption of the SE-TLG circuit is defined with equation (4.20).The energy consumption related to each tunnel event multiplied

with the gate output switching frequency provides the SE-TLG power consumption shown in the equation.

$$P_{\max} = \frac{\Delta F_E}{t_D} = -\frac{(|V_j| - V_C)^2}{\ln(P_e).R_t} \tag{4.20}$$

The relationship between the frequency and delay is given in the following equation (4.21).

$$f_{\max} = \frac{1}{t_D} \tag{4.21}$$

The $C_{\Sigma}^{P} = C1 + 5 \times 0.5aF = 12.5aF$ and $V_j = \frac{1}{2}.\frac{C_k^P \times 0.016}{C_{\Sigma}^{P}} V = 0.32mV$ for the majority gate designed in section 4.5.1. Time delay for the circuit is calculated as 0.92nS using the equation (4.7). The computed minimum energy for the circuit is 0.8meV as the circuit consists of 5 capacitors with each 0.5aF value.

For the designed PLA circuit total energy consumption is correlated to the number of inverters, NAND, NOR gates. According to the calculations the two input NOR and NAND gate consumes 0.76meV energy each. Layer two is formed using 4 two-input NAND gates and Layer 3 needs 1 two input NOR gate. A three input NOR gate which consumes 1.14meV energy is required in the Layer 3. Layer 1 formed with three inverters, layer 2 with four and layer 3 with two inverters need energy consumption 10.9meV for each. So the energy consumption of the entire circuit is 104.04meV. For designed the PLA circuit power consumption is calculated as 37.49pW. Related switching frequency and the delay time is computed using equation (4.21) as $f_{\max}$ =1.369x$10^9$ Hz and $t_D$=0.73 nSec respectively. The tunnel rate is calculated as 0.249x$10^{11}$ from the equation (4.22) and thus the time ($\tau_t$) of average tunneling is predicted to be 0.02pSeconds with equation (4.23).

$$\Gamma_R = \frac{V_j - V_C}{q_e . R_t} \tag{4.22}$$

$$\tau_t = \frac{1}{\Gamma_R} \tag{4.23}$$

The time delay of the entire circuit can be determined by summing up the delay for the Layer 1 (caused by operation of a single inverter), delay for Layer 2 (caused by a buffered two input AND gate ) and maximum delay provided by the Layer 3 operation (three input NOR gate delay) . The total delay is calculated as 3nSec.

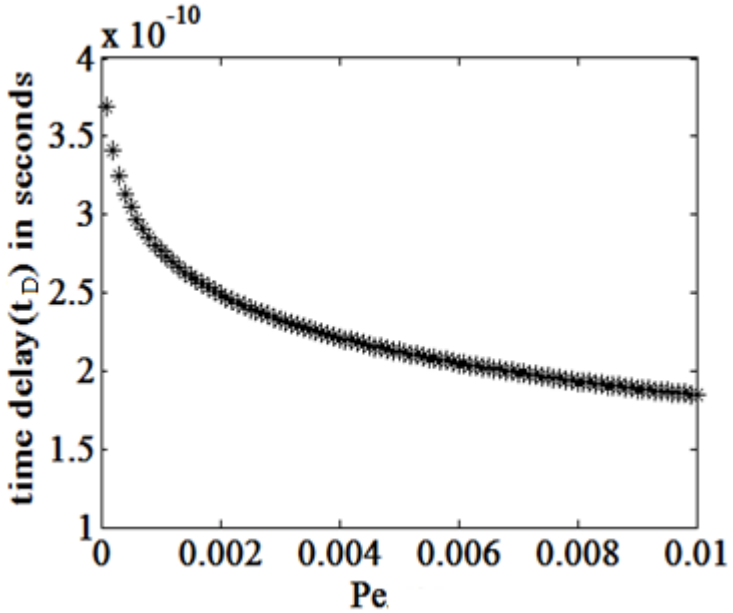



**Figure 4.14:** Time delay $t_D$ plotted with respect to error probability $P_e$

The time delay $t_D$ is plotted against the Probability of error $P_e$ in the figure 4.14. The values of error probability are considered from 0 to $10^{-2}$. The minimum value of $P_e$ shows maximum amount of time delay as $3.75 \times 10^{-10}$ seconds. With higher values of $P_e$ the time delay gradually falls.

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# Chapter 5

# SET-CMOS HYBRID APPROACH BASED CIRCUIT IMPLEMENTATION



## 5.1 Introduction

To fulfill the requirement of future ULSI circuit [5.1] devices with a new principle of operation are coming into the limelight. SED [5.2] being one of the promising device, is studied, fabricated and tested by the researchers. It has been observed that the pure SED circuits dissipate ultra-low power, support nanometer-scale feature size, very high packing density, along with unique features like Coulomb blockade and Coulomb oscillation. But they suffer from small voltage gain, low current drivability, low-temperature operability and susceptibility towards random background charge. These limitations bound the application domain of SED. Moreover, it faces several challenges such as lack of interconnect technology adaptation and lack of proven SED specific fabrication technology. Contrarily the CMOS provides high voltage gain and high-speed drivability, but suffers from several issues related to scaling [5.3]-[5.5]. This limits the CMOS operation in the sub-nanometer regime. The co-integration of SET and CMOS technology can provide a

potential technological solution in the form of SET-CMOS [5.6]-[5.9] technology which combines the strengths of both the technologies as they almost compensate each other's drawback. This results in a hybrid technology which is popular as SET-CMOS or SET-MOS [5.10]-[5.11] architecture. As, a basic structure of this hybrid circuit requires two transistors one SET and one MOSFET to work in the complementary mode it is called SET-MOS. As mainly the CMOS technology concept (complementary working of two transistors) is used for circuit design purpose hybrid circuit is also called SET-CMOS.

For the co-fabrication[5.12] mainly the Silicon-based process which is compatible with CMOS is more demanding though SET can be fabricated also with the group III-IV materials and metals. The co-fabrication methods of SET-CMOS are already proposed by research lab of NTT and Toshiba [5.13].

The co-simulation of SET-CMOS technology demands appropriate and accurate SPICE compatible model of SET and CMOS both. For MOSFETs, the existing BSIM models [5.14] can be used. For the simulation of SET Macro model [5.15]-[5.18], Master Equation [5.19] based method or MC methods [5.20]-[5.22] are primarily used. Among them, the Macro model and the Master equation based analytical models [5.23]-[5.25] are SPICE compatible. Co-simulation needs both the model files of SET and MOSFET to be compatible to the same simulation software platform. One of the most popular analytical models of SET proposed by Mahapatra et al. is known as MIB (Mahapatra-Ionescue-Banerjee model) [5.26]. Mainly the design and implementation of a very common digital logic circuit half subtractor and a binary multiplier are elaborated in a stepwise manner with supporting simulation results.

## 5.2 Literature Survey

Several SET-CMOS circuits such as quantizer [5.27], SRAM with MVL (Multiple-Valued-Logic) [5.28], VCO (voltage-Controlled-Oscillator) [5.29], negative differential resistor (NDR) [5.30] were proposed during the earlier days. Design of static memory cell [5.31] was demonstrated by Lee et al. in 2003 with SET-CMOS. In 2008 Li et al. proposed different SETMOS logic circuits [5.32]. Ou & Wu in 2005 explained the ADC (Analog-to-Digital converter) and DAC (Digital-to-Analog Converter)[5.33] structures with SETMOS. SET-CMOS as the future of ULSI (Ultra-Large-scale-integration) system was reported in 2002 by Uchida et al. [5.34]. Several works on SET-CMOS co-fabrication has been also reported earlier. Kim et al. demonstrated the literal gate fabrication with SET-FET (Single-electron-transistor-field-effect-transistor) for MVL cell [5.35] in 2006. The first successful fabrication of SET-MOS circuit was elaborated by Prager et al.[5.36].The simulation of SET-CMOS circuit with Macro model was introduced by Yu et al. [5.37]in 1999. A compact model for SET-MOSFET co-simulation was described in 2004 by Royer et al. [5.38]. Hasaneen et al. developed ME (Master Equation) based model [5.39] for SET simulation. One of the most popular SET analytical model, MIB for co-simulation purpose was elaborated by Mahapatra et al. [5.40].In 2003 Liehtschnig et al. [5.41] also presented the simulation method of SET-FET. New design methodology based on the 22nm technology was demonstrated by Parekh et al.[5.42] in 2012 for SET-MOS hybrid logic circuits. Logic circuit simulation with CMOS-SET was elaborated in the work of Jana et al. [5.43]. Jain et al. [5.44] in their works highlighted on the pass transistor implementation of SET-MOS logics. Recently hybrid circuit based PLA (Programmable Logic Array) [5.45] was also presented. A static differential style of SET-MOS circuits was also explained by Abutaleb in [5.46]. B. Sui first introduced hybrid reconfigurable cell

[5.47]. The further extension of hybrid circuit to the multi gate and multi tunnel junction [5.48] was done by G. Deng et al. W. Wei et al. developed the memory cell[5.49] using hybrid concept. Other notable works in this field includes the design of pulse divider circuit [5.50],electron pump[5.51].

## 5.3 SET-CMOS Co-simulation

The three approaches of SET circuit simulation are already discussed in details. The MC method established on probability calculations is considered as one of the most accurate SED circuit simulation methods. The time constraints and moreover the SPICE non-compatibility makes it unsuitable for SET-CMOS co-simulation. SIMON [5.52] is one of such MC simulators. The ME-based method supports SPICE environment for co-simulation and also the time requirement of this method is much lower than the MC method. The following work uses BSIM4 (supports 65nm MOSFET technology) model for MOSFET and MIB model for SETs. The results of MIB model are in close agreement with the widely accepted SIMON results. It uses the ME-based technique.

### 5.3.1 MIB model

MIB is one of the popular models of SET based on Master Equation method. The Verilog A version of the model file is used for the simulation of the hybrid circuits to declare the SET parts. This MIB model is easily integrated with the SPICE through the Verilog A interface. MIB is compatible with BSIM as well as charge-based EKV (Enz-Krummenacher-Vittoz) [5.53] model of MOSFET.

This compact modeling (MIB) of SET is developed with the following assumptions-

a. Orthodox theory is obeyed
b. Device capacitance is much smaller than the interconnect capacitance related to the gate, drain and source terminal. It ensures the total island capacitance is equal to the summation of all the capacitances associated with the device.

$$C_{sum} = C_s + C_d + C_{g1} + C_{g2} \tag{5.1}$$

Here, $C_{sum}$: summation of all capacitances

$C_s$: Source capacitance

$C_d$: Drain capacitance

$C_{g1}$: Capacitance of gate 1

$C_{g2}$: Capacitance of gate 2

From the Orthodox theory, the equation of tunneling rate related to the free energy change can be determined

$$\Gamma(\Delta F_E) = \frac{\Delta F_E}{q_e^2 . R_t (1 - e^{-\frac{\Delta F_E}{k_B T}})} \tag{5.2}$$

Where, $\Delta F_E$ : the Gibb's free energy

$R_t$ : Tunnel junction resistance

$k_B$ : Boltzmann's constant ($1.38 \times 10^{-23}$ J/K)

For many body systems or the system with tunneling of many electrons, ME is applied considering tunneling junction is memoryless and the system evolves between states in a jump like fashion at random times expressed with (5.3).

$$\frac{\partial p_x(t)}{\partial t} \sum_{x \neq y} \left[ \Gamma_{xy} p_y(t) - \Gamma_{yx} p_x(t) \right] \tag{5.3}$$

The steps of MIB model are as follows

i. Calculation of island potential

The island potential is calculated from the equation (5.4)

$$V_i = \frac{C_d}{C_{sum}} V_{ds} + \frac{C_{g1}}{C_{sum}} V_{gs1} + \frac{C_{g1}}{C_{sum}} V_{gs2} - \frac{\beta q_e}{C_{sum}} \tag{5.4}$$

$V_{ds}$ : drain to source voltage

$V_{gs1}$: Front gate to source voltage

$V_{gs2}$ : Back gate to source voltage

$\beta$ : Background charge

ii. Drain current window shifting and

MIB model is developed for the range of $(V_{ds}/2) \le V_i \le ((2q_e/C_{sum})+(V_{ds}/2))$. The window of drain current can be shifted within this range of island potential.

iii. Finally, drain current calculation

Using ME for the state of 0 to 1, 1 to 2, -1 to 0, the tunneling rates are determined with the equation (5.2). The tunneling rates are then replaced by tunneling currents ($I_t = q_e.\Gamma_R$). The final expression of drain current is presented in the equation (5.5). Here s is the sign of $V_{ds}$, $a = \frac{q_e}{C_{sum}}$ and $V_t = \frac{k_B T}{q_e}$

$$I_{ds} = s.\frac{(I_{ts}(0)-i_{ts}(0))(i_{ts}(1)+I_{td}(1))+(I_{ts}(1)-i_{ts}(1))(I_{ts}(0)+i_{td}(0))+(i_{ts}(1)+I_{td}(1))(i_{ts}(0)+I_{td}(0))}{(i_{ts}(1)+I_{td}(1))+(I_{ts}(0)+i_{td}(0))+\frac{(I_{ts}(1)+i_{td}(1))}{I_{td}(2)}+\frac{(i_{ts}(1)+I_{td}(1))(i_{ts}(0)+I_{td}(0))}{I_{ts}(-1)}} \quad (5.5)$$

Where, $I_{ts}(0) = \frac{s.V_i - a}{\left(1-e^{-(\frac{s.V_i-a}{V_t})}\right)R_s}$, $i_{ts}(0) = \frac{-s.V_i - a}{\left(1-e^{-(\frac{-s.V_i-a}{V_t})}\right)R_s}$, $i_{ts}(1) = \frac{-s.V_i + a}{\left(1-e^{-(\frac{-s.V_i+a}{V_t})}\right)R_s}$,

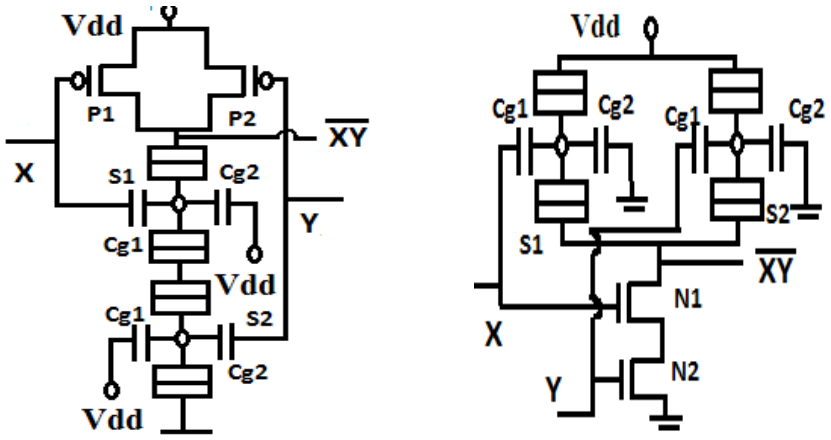
$I_{td}(1) = \frac{sV_{ds} - sV_i + a}{\left(1-e^{-(\frac{sV_{ds}-s.V_i+a}{V_t})}\right)R_d}$, $I_{ts}(-1) = \frac{sV_i + a}{\left(1-e^{-(\frac{s.V_i+a}{V_t})}\right)R_s}$, $I_{td}(0) = \frac{sV_{ds} - sV_i - a}{\left(1-e^{-(\frac{sV_{ds}-s.V_i-a}{V_t})}\right)R_d}$

$I_{ts}(1) = \frac{-sV_i + a}{\left(1-e^{-(\frac{-s.V_i+a}{V_t})}\right)R_s}$, $I_{td}(2) = \frac{sV_{ds} - sV_i + 3a}{\left(1-e^{-(\frac{sV_{ds}-s.V_i+3a}{V_t})}\right)R_d}$,

$$i_{td}(1) = \frac{-sV_{ds} + sV_i + 3a}{\left(1 - e^{-\left(\frac{-sV_{ds} + s.V_i + 3a}{V_t}\right)}\right) R_d} \quad \text{and} \quad i_{td}(0) = \frac{-sV_{ds} + sV_i - a}{\left(1 - e^{-\left(\frac{-sV_{ds} + s.V_i - a}{V_t}\right)}\right) R_d}$$

## 5.4 Circuit Implementation with SET-CMOS Hybrid

The NAND gate can be designed with the hybrid approach where two p-MOS are connected in parallel to form the pull-up-network (PUN)and two SETs are connected in the series to form the pull-down-network (PDN) as depicted in figure 5.1 (a). Another way of designing the hybrid NAND is by doing the reverse i.e. parallel connection of SETs to form PUN and series connected n-MOSs for PDN formation depicted in figure 5.1 (b). In both cases, the two inputs are X and Y. The front gate and back gate capacitors are denoted with Cg1 and Cg2. Power supply voltage is marked as Vdd. In figure 5.1 (a) Vdd is also connected to the back-gates of the two SETs to make them work like n-switches and in figure 5.1 (b) back–gates are grounded.




(a) (b)

**Figure 5.1:** NAND gate circuit with SET-CMOS (a) SET as PDN,(b) SET as PUN, with input X and Y.

An inverter circuit is presented in figure 5.2 with SET-CMOS hybrid following the similar way of figure 5.1(a). The p-MOS is kept as it is

whereas the n-MOS is replaced with the SET which now works as an n-switch in CMOS technology.

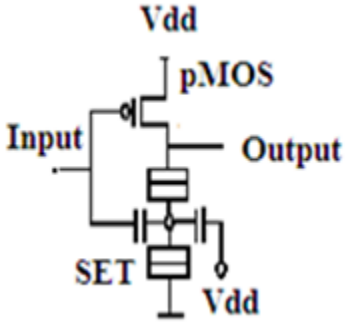



**Figure 5.2:** Hybrid SET-CMOS NOT Gate

In this section, two arithmetic circuit designs with SET-CMOS hybrid is elaborated one is the half subtractor and another one is the binary multiplier (2 bit). Verilog A version of the MIB model has been utilized for implementing the SETs while the BSIM 4.6.1 is used for MOS. The appropriate model parameters for the two above mentioned circuits are discussed with supporting simulation results.

Tanner SPICE (T-SPICE) is chosen as the environment for co-simulation of the hybrid circuit. The accuracy and the speed of the circuit simulation for T-SPICE are controlled by the different tolerance values. The finite arithmetic precision is used to solve the circuit equations in T-SPICE. It results in several approximations executed during each step of the solution. The errors in T-SPICE are bound by different tolerance settings. Due to the application of precision arithmetic for solving the circuit related KCLs (Kirchhoff's Current Law) the residual current becomes non zero. If the residual current is within the tolerance limit defined by tolerance 'abstol' and 'reltol' then the result converges. For both the proposed designs the default values of reltol and abstol are taken i.e.$1\times10^{-4}$ or 0.01% for reltol and 0.5 nano-Amp for abstol. The number of allowed iterations for solving the KCL is fixed with 'numnd' . The 'numnd' is considered here as 100 for both the circuit designs.

## 5.4.1 Half Subtractor Circuit

For any arithmetic logic circuit, the half subtractor is one of the elementary blocks. The aim of the design with hybrid approach is to get the outcome in the form of an ultra-low power consuming half subtractor circuit with the drastically reduced area.

### 5.4.1.1 Circuit implementation

The conventional structure of a half subtractor is presented in figure 5.3 with A, B as the two inputs along with D (the difference between A and B) and borrow as the outputs. The traditional circuit requires three gates - one XOR gate, one AND gate and an inverter. Output $D = \overline{A}B + A\overline{B}$ and $Borrow = \overline{A}B$.

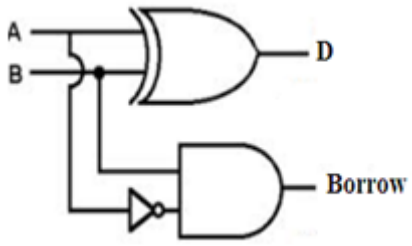



**Figure 5.3:** Conventional schematic of Half Subtractor with Boolean Gates.

Already the structure of inverting buffer with its elements is presented in section 5.4. The NAND equivalent circuit of XOR is used in the design. The schematic of the hybrid half subtractor is depicted in figure 5.4 with power supply voltage Vdd as 0.8V.

The circuit construction demands 9 SETs and 9 p-MOSFETs along with total 18 numbers of capacitors. Circuit parameters and their values are mentioned in Table 5.1. The threshold voltage (Vth) specification of the p-MOS is -220mV. The W/L of the p-MOS is fixed at 100/65, where both the width(W) and length(L) p-MOS are in the nanometer range. The operation of SET as a n-switch is controlled by the back-gate voltage,

which is kept at 0.8V for this particular circuit as the power supply is 0.8V.

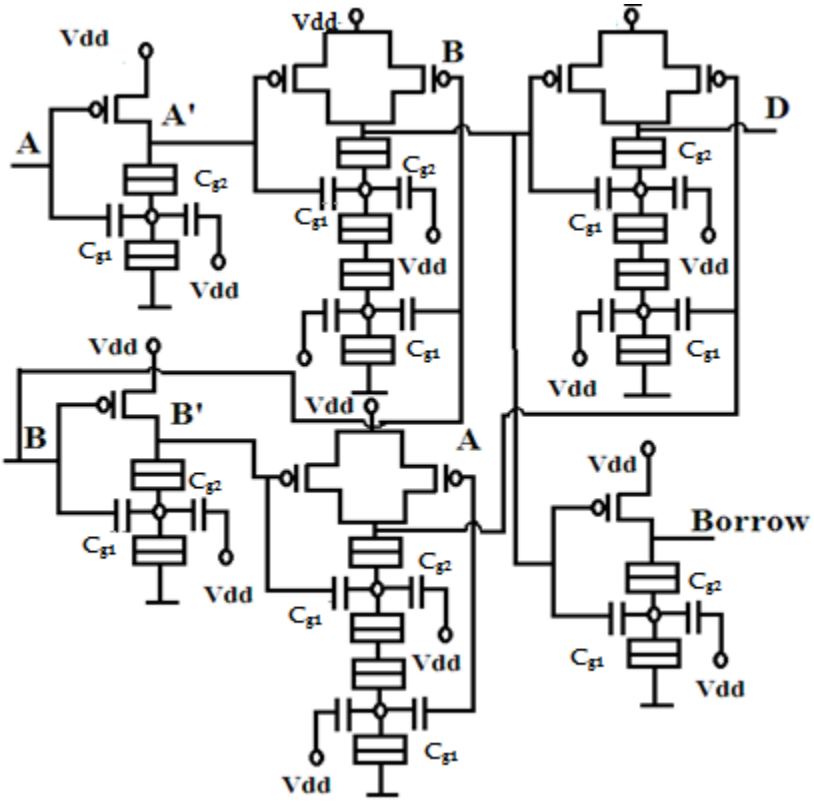



**Figure 5.4:** SET-CMOS hybrid half subtractor circuit design with inputs A, B, and the power supply Vdd.

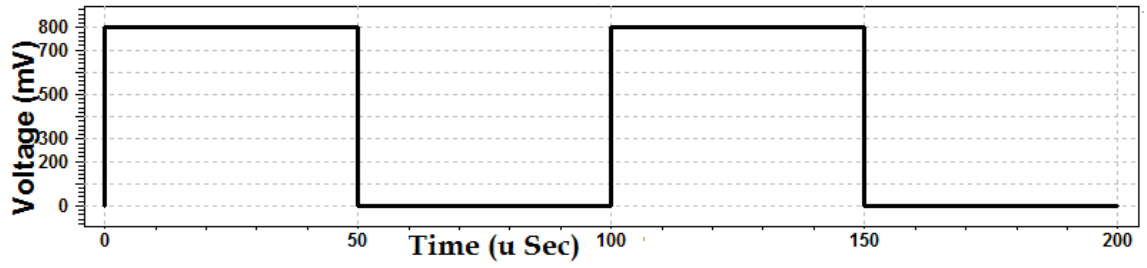
**Table 5.1**: Circuit parameters used for hybrid SET-CMOS half Subtractor design

| Component | Specification |
|---|---|
| p-MOSFET | L=65nm<br>W=100nm<br>Vth=-0.22V |
| n-SET | Back-gate connected to Vdd<br>Cg1=2.7x10$^{-19}$F<br>Cg2=1.25x10$^{-19}$F<br>Cd=1.0x10$^{-19}$F<br>Cs=1.0x10$^{-19}$F |
| Vdd | 0.8V |

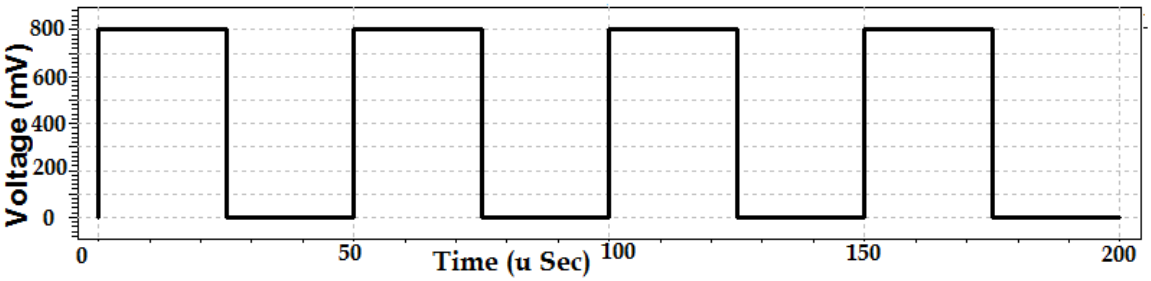
Other parameter values of SET ,defined using the behavioral Verilog –A model (MIB model), are presented in the Table 5.1 such as Cg1=0.27aF,Cg2=0.125aF,Cd=0.1aF,Cs=0.1aF. The tunnel resistance $R_t$ is fixed at 0.1MΩ.

### 5.4.1.2 Simulation Results

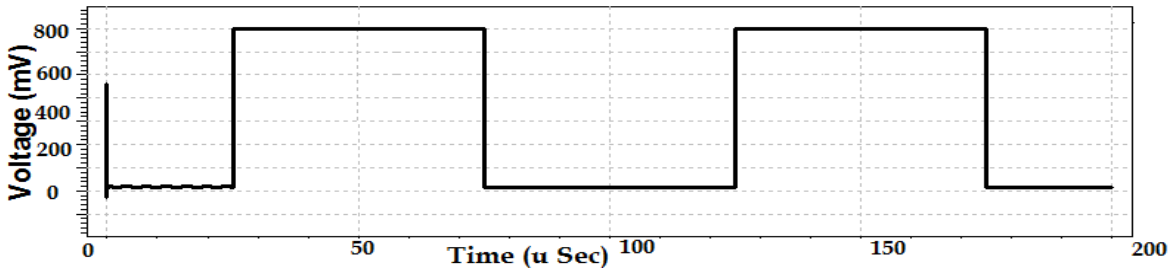
The simulation is performed in Tanner EDA (Electronics Design Automation) tool by defining the SETs with the MIB model and MOSFETs with the BSIM 4 model. The transient analysis of the circuit consumes 0.17Seconds of time whereas the total time required is 3.71Seconds with the Intel Core i3 processor (2.4GHz). The simulation temperature specification is set to $25^0$C. The simulated input waveform A is depicted in figure 5.5 (a) where the frequency is 10 KHz with 50% duty cycle. Input B with same duty cycle and double frequency are presented in figure 5.5 (b). Here logic'1'is defined with voltage level 0.8 V and the logic '0' is defined with 0V. The results are exhibited in the next two figures 5.5 (c) and (d) for all the logical combination of A and B.



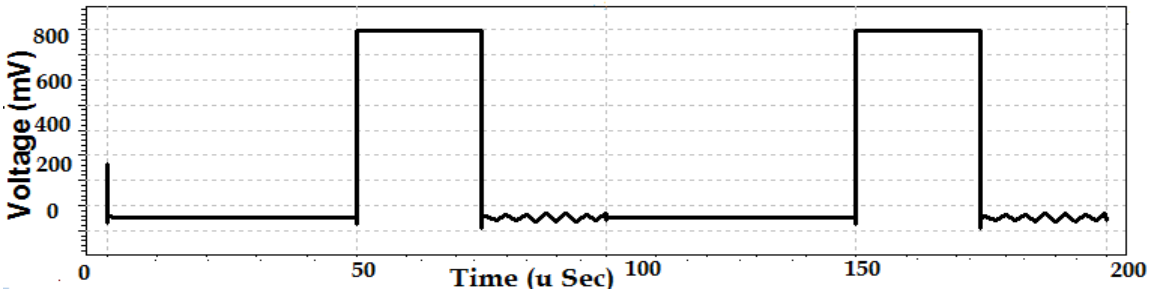

(a)




(b)




(c)




(d)

**Figure 5.5:** Simulated waveforms of SET-CMOS hybrid Half subtractor for (a) input A, (b) input B, (c) Output D(difference) (d) Output Borrow

The figure 5.5 (c) is for the difference between two inputs A, B and remains in high logic when alternate of the two signals is at logic '1'.The borrow is illustrated in figure 5.5 (d), which remains at logic '0' except for A= 'low' and B= 'high' condition. Both outputs maintain the desired logic level and thus the generated waveforms prove the circuit functioning to be proper. The designed circuit simulation time requirement is total 3.87Seconds. The minimum and maximum power consumption are $3.29x10^{-8}$Watts (at time 0 Second) and $1.11x10^{-6}$Watts (at time $7.5x10^{-5}$ Seconds) respectively. The calculated average power consumption for the time range of 0to 0.0001Seconds is $4.45x10^{-7}$ Watts.

## 5.4.2 Two-bit Binary Multiplier Circuit

Multiplication being one of the primary mathematical operations is frequently used for computing devices. The computational performance

can be enhanced with the compact size, high speed and reduced power consumption. Most of the present computing device requires the multiplication to be done in the binary form.

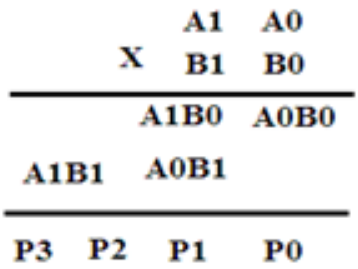



**Figure 5.6:** Two-bit binary number multiplication

**Table 5.2:** SET-CMOS hybrid 2bit Multiplier Truth Table

| **Inputs** | | | | **Outputs** | | | |
|---|---|---|---|---|---|---|---|
| **Multiplicand** | | **Multiplier** | | **P3** | **P2** | **P1** | **P0** |
| **A1** | **A0** | **B1** | **B0** | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

Here a simple but yet fast and compact sized implementation of the two-bit binary multiplier has been presented with SET-CMOS hybrid technology. As an example, two binary two-bit numbers A and B are taken into consideration. The multiplication of the two binary numbers and their generated product P is provided in figure 5.6. The two bits of A are represented with A0, A1 while B0, B1 represents two-bit input binary number B. The product is P with four bits denoted with P0, P1, P2, P3.

The truth table for the circuit is presented with Table 5.2. Figure 5.6 shows the multiplication of the two-input binary numbers A, B having LSB (Least significant bit) A0, B0, and MSB (a Most significant bit) A1, B1.

The schematic of the binary multiplier with usual logic gates and two half adder (HA) is illustrated in figure 5.7. Inputs of the HAs are represented with Aha1, Bha1 (for the first HA), Aha2, Bha2 (for the second HA). Outputs are denoted with S1, Carry1,S0,Carry0 for second and first HA respectively. The generated product output is denoted with P and has four bits (P0,P1,P2,P3) among which P0 is the LSB and P3 are indicated as the MSB.

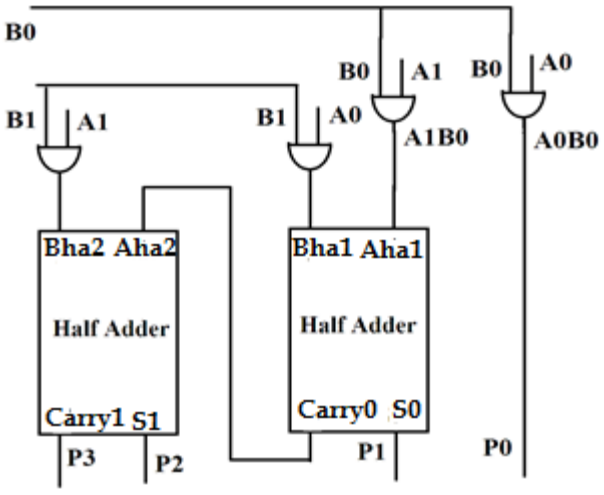



**Figure 5.7:** Conventional Structure of Binary multiplier circuit with two half adders

### 5.4.2.1 Circuit implementation

The detailed circuit design of SET-CMOS based two-bit binary multiplier is provided in figure 5.8. The circuit design is done by replacing the PUN with p-MOS and PDN with n-SETs .A0,A1,B0,B1 are the four input signals using which different intermediate stage outputs are generated.

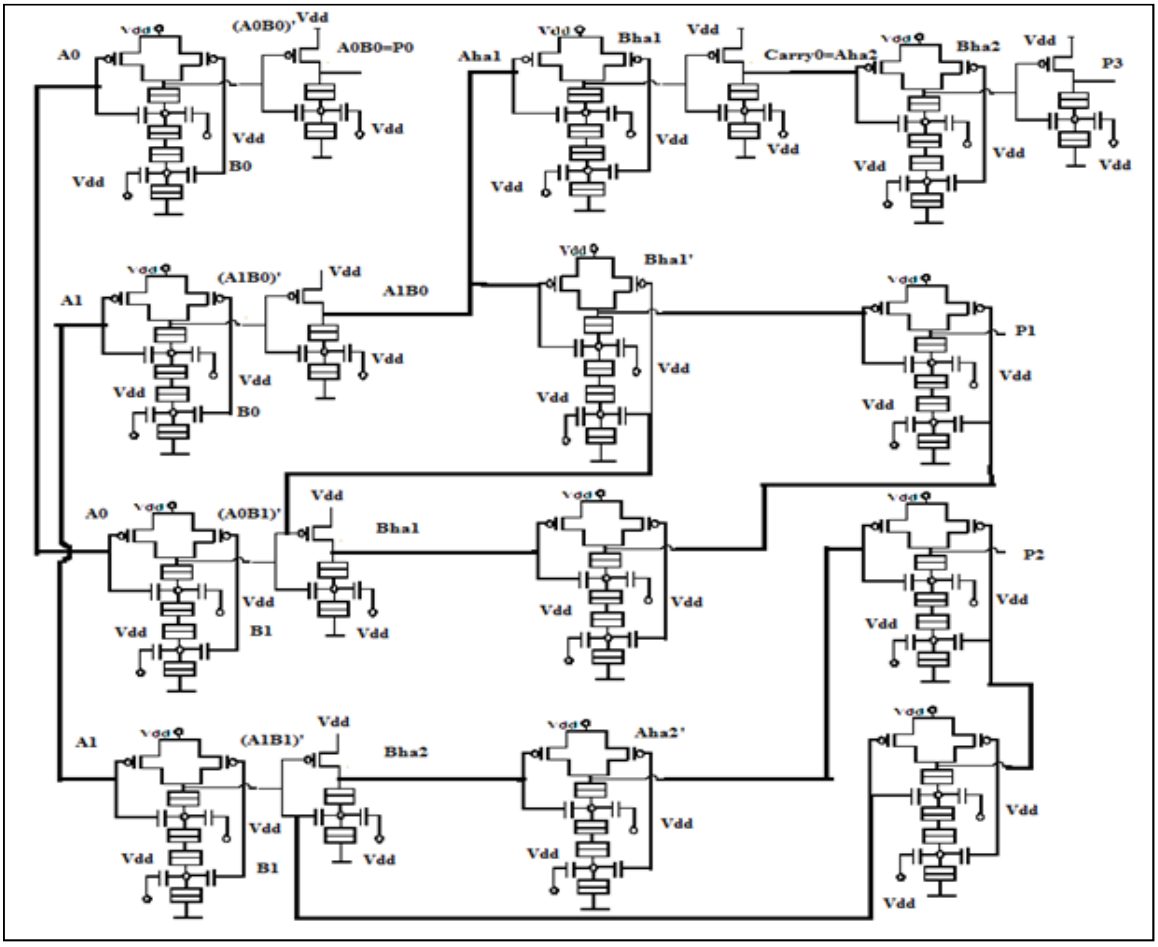


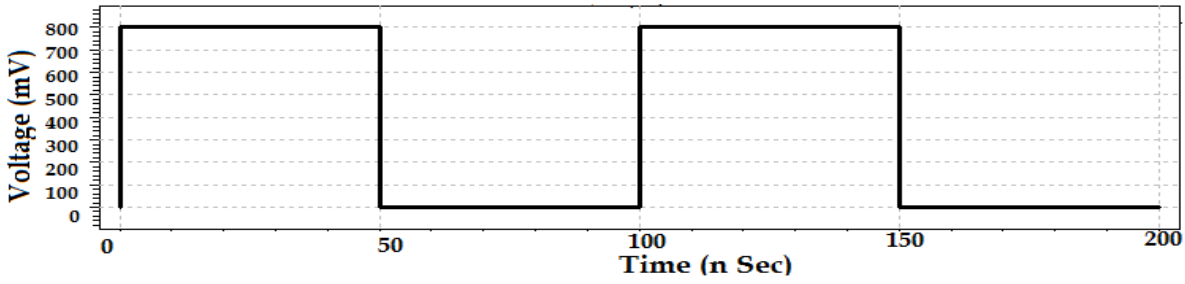

**Figure 5.8:** SET-CMOS circuit design of two-bit binary multiplier with two 2 bit inputs A and B.

P0 is related to the inputs using the expression $P0 = A0.B0$ which is designed using a combination of hybrid NAND and NOT gate. The Aha1,Bha1,Aha2,Bha2 are the inputs to the first and the second half

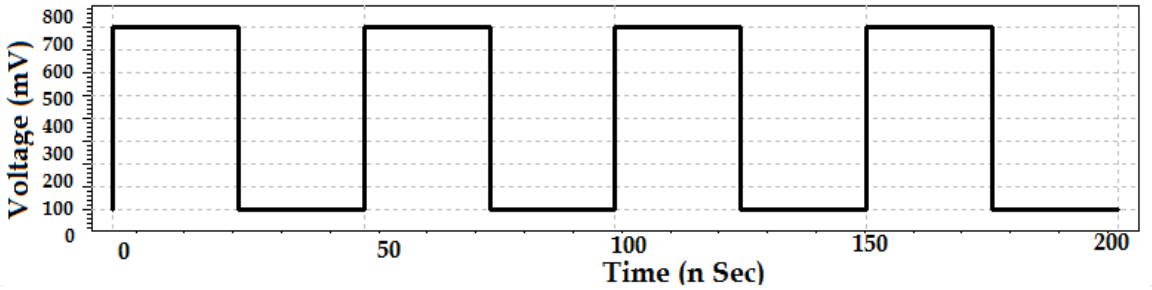
adder.Sum of Aha1 and Bha1 is P1 and the carry is denoted with Carry0 which works as the input Aha2 for the next half adder. The required number of p-MOSFETs and n-SETs are 30 each. Total 60 capacitors are needed for the construction of the circuit. The capacitor values of the SETs are same as mentioned in table 5.1.

### 5.4.2.2 Simulation Results

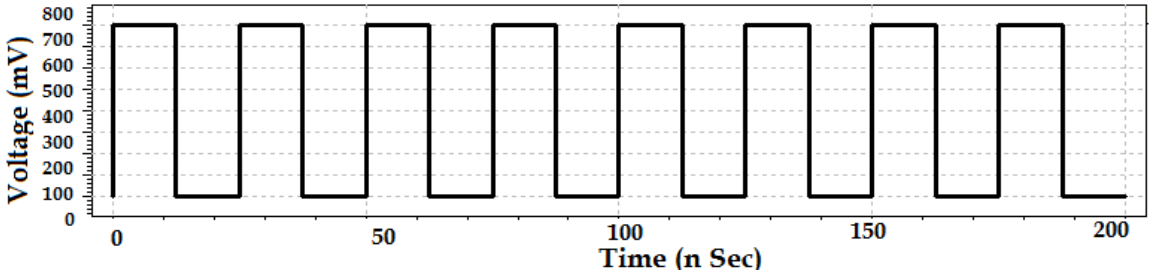
Verilog A file of the MIB has been utilized for the SET circuit simulation purpose along with the BSIM 4.6.1 for MOSFET counterpart. The simulation time for the entire circuit in Tanner SPICE is 4.12 Seconds out of which 2.68 Seconds are dedicated for the transient analysis. The temperature is selected as $25^0$C. The simulated waveforms of input A with LSB A0 ,MSB A1 ;input B with LSB B0, MSB B1,are shown in figure 5.9 (a), (b),(c) and (d) respectively. Logical interpretation is as follows Logic 1=0.8V and Logic 0=0V for input and output both.The input and output simulated signals are plotted against the time. The total time period considered is 100nSeconds. All the inputs are set with 50% duty cycle and frequency of B0 is double of B1. Similarly, B1's frequency is double of A0 and in a similar way, A1's frequency is half of A0.




(a)


Voltage (mV)
800
700
600
500
400
300
200
100
0
0
50
100
150
200
Time (n Sec)

(b)


Voltage (mV)
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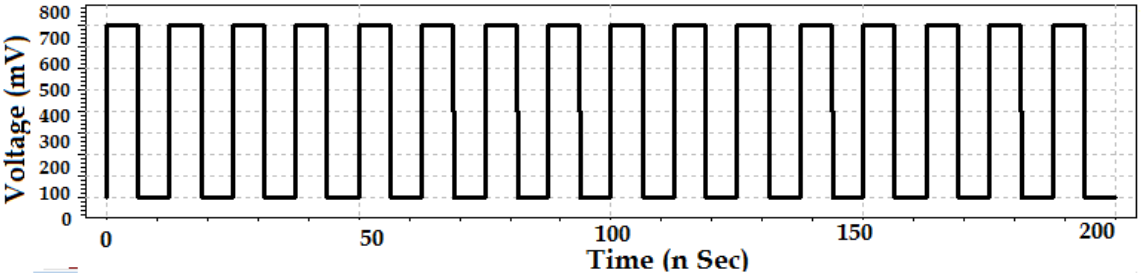
Time (n Sec)

(c)


Voltage (mV)
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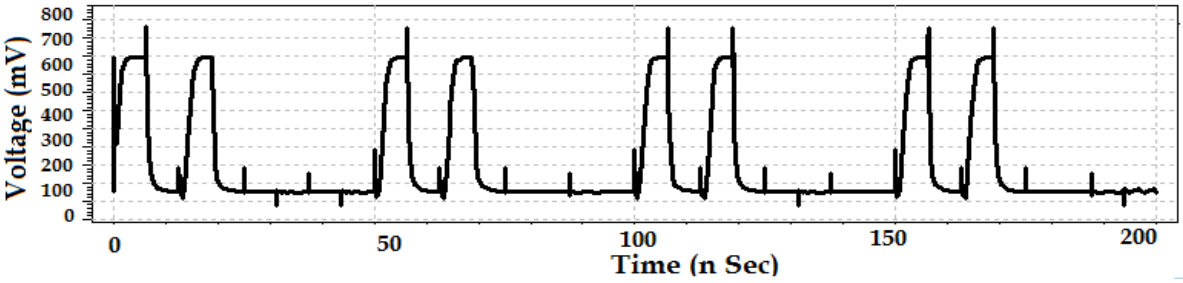
Time (n Sec)

(d)


Voltage (mV)
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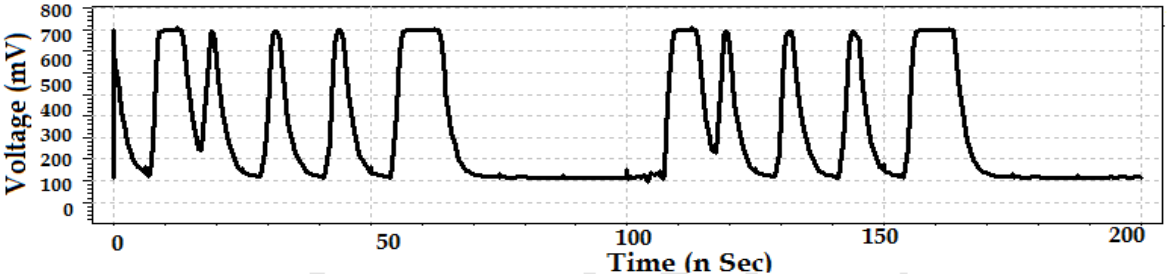
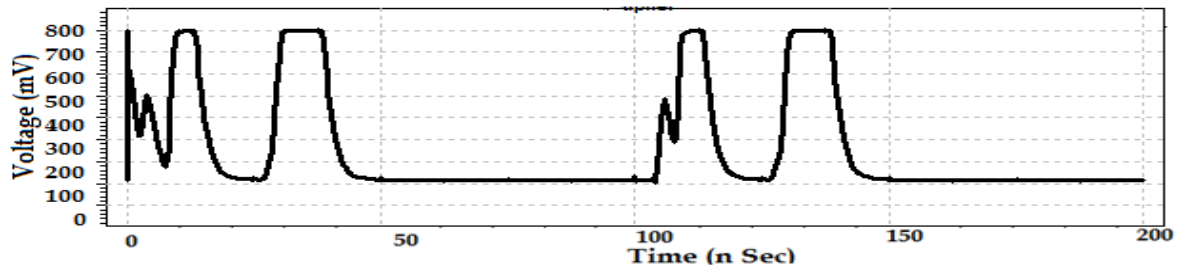
Time (n Sec)

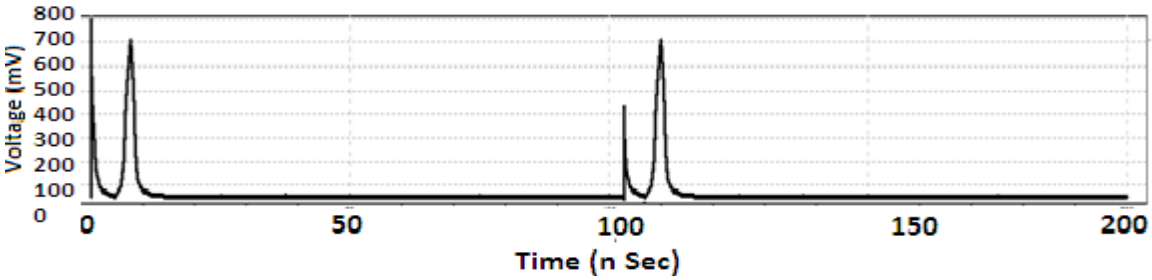
(e)


Voltage (mV)
800
700
600
500
400
300
200
100
0
0
50
100
150
200
Time (n Sec)

(f)




(g)




(h)

**Figure 5.9:** Simulated waveforms for (a)input A1,(b) input A0,(c)input B1,(d)input B0,(e)output LSB P0,(f)output P1,(g)output P2,(h)output MSB P3

The inputs are considered in such manner to observe the outputs for all the logical combinations of inputs. The circuit simulated with Tanner SPICE provides the result as waveforms of P0,P1,P2 and P3 depicted in figure 5.9(e), (f), (g) and (h) respectively. P0 is the LSB of the generated output of the circuit i.e the product of input A and B. The waveform of the P0 provided in figure 5.9 (e) is at logic high for input A=01&B=01;A=01&B=11; A=11&B=01; A=11&B=11 which resembles with the truth table values. Figure 5.9 (f) for P1 indicates the waveform is at logic 1 for B=10,11 with A=01; B=01,11 with A=10 and A=11& B=10 which matches with Table 5.2. The waveform of P2 and P3 are presented in figure 5.9 (f) and (g) respectively. Logic 1 of P2 is observable at A=10 & B=10; A=10 & B=11;A=11 & B=10. Whereas from the figure it is clear that the P3 or the MSB of product is high when all the input bits of A and B are high. The logic high is properly transmitted but the logic 0 in some part of the waveform is not completely at 0V. This is due to the

glitch introduced by the SET as it is unable to properly pass the logic 0. But by ignoring the glitches the simulated results are satisfactory enough to judge the circuit as a two-bit multiplier. The average power consumed for time 0 to $1x10^{-7}$ Second is $1.025x10^{-6}$ Watts. At time $5x10^{-8}$ Second the maximum power consumption is determined as $6.88x10^{-4}$ Watts , whereas the minimum power is $1.12x10^{-7}$ Watts at time 0 Second.

## 5.5 Comparative Analysis of SET-CMOS hybrid circuit design with others

A comparative study of the SET-CMOS based 1-bit comparator circuit design with conventional CMOS and SE-TLG based design of the same is presented in Table 5.3.

**Table 5.3:** Comparison of 1-bit Comparator circuit design with CMOS, SE-TLG, SET-CMOS approach.

| **Parameters** | **CMOS based** | **Threshold logic based** | **SET-CMOS hybrid based** |
|---|---|---|---|
| Number of MOSFETs | 20 | N/A | 10 |
| Number of tunnel Junctions | N/A | 27 | 20 |
| Number ofcapacitors | 7 | 42 | 20 |
| Number ofislands | 0 | 24 | 10 |
| PowerSupply (V) | 0.8 | 0.016 | 0.8 |
| PowerConsumption | 2.21e-05W | 0.225e-09W | 6.05e-07W |
| Simulation time(sec) | 4.27 | 1.5 | 3.84 |
| Temperature | Room Temperature | Few mK temperature | Room Temperature |

The basic parameters for the comparison are the numbers of MOSFETs, tunnel junctions, required capacitors, involved SET islands. Apart from that, the simulation time of the same circuit using the three design technologies is compared. The power supply requirement of the three approaches is also deliberated. As SE-TLG requires only tunnel junctions to be driven for the comparator circuit design, this technology demands a minimum amount of power supply of 0.016V. Whereas the complete CMOS oriented design and SET-CMOS co-integration based circuit needs to use higher power supply voltage to provide sufficient amount of voltage to make the MOSFET functional. Thus both the approach based circuit needs 0.8V as a power supply. The power consumption of a circuit is always associated to the power supply requirements. As the SE-TLG requires a minimum amount of power supply the power consumption of the circuit is also lowest among the three in the range of nanowatts. While SET-CMOS circuit consumes a moderate amount of power (about 0.605 micro Watts) among them. As the CMOS circuit is designed entirely based on pMOS and nMOS it dissipates the highest power (22.1 micro Watts).

The area of the designed circuit can be predicted from the required number of components. Circuit with CMOS technology needs 27 components among them 20 MOSFETs are there, so it needs a huge area to accommodate them. Whereas the area requirement for SE-TLG based design is least because of having tunnel junction as main component. Simulation time is even lowest for SE-TLG and highest for CMOS based. From the comparison it is clear enough that the SE-TLG provides power consumption in the nanowatt range, uses a power supply of only 16mV, area requirement is also very small on the other hand the CMOS based circuit supports room temperature operation but low power consumption, low power supply requirement, but high packing density

is not supported. So it seems the SET-CMOS hybrid approach gives a pretty compromised solution in between the SET-TLG and CMOS circuit.

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# Chapter 6

# *RELIABILITY ANALYSIS*



## 6.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) [6.1] within the year 2020 a single chip will accommodate near about 12 billion transistors. Along with the time, CMOS scaling will become much complicated to match the requirement of below 10nm [6.2]. The trends of miniaturization are reaching towards the physical limits of CMOS device operation and the process of manufacturing. It has already become very critical to characterize device parameters practically due to the inadequate efficient solution. Moreover, the reduction in the device geometries below 45nm range [6.3] has forced the margin of reliability to be reduced drastically. The future foundation of the fabrication technology of integrated circuits can be developed with the new devices having unique nature of working in the nanoscale regime. Due to the transient and permanent errors, the future non-CMOS nanodevices are supposed to undergo low reliability issues. The constraints imposed by the technology of fabrication will increase the rate of the permanent error. The presence of nondeterministic effects of

parasitic elements such as background charge (BC), increases the rate of transient error. The BC disrupts the proper functioning of the device in both space and time. According to IEEE standards, reliability can be illustrated as the system capability or ability of a component to do the required operations for specified time duration under stated conditions. An optimal operability of a system is often guaranteed by understanding the reliability issues of the used technology. Different fault tolerant solutions are available to cope up with the reliability issues. But before that the extensive study of the reliability assessment is essential for any electronic device. The BC related reliability issues of SEDs are here mainly taken into account along with the island dimension while carrying out the reliability analysis.

## 6.2 Literature Survey

In 1956, a method of reliability analysis from the unreliable components was proposed by Von Neuman [6.4]. An algorithm was developed by Abraham and Siewiorek in 1974 for reliability assessment of the network with triple modular redundancy [6.5].Constantinescu in his work explained the reliability related challenges to be faced in the VLSI circuits [6.6]. Cotofona et al. designed an framework for building reliable systems from unreliable nano-electronic components [6.7].Reliability has been described as the fourth pillar of optimization [6.8] after the power dissipation, area and operational speed by Lazarova-Molnar in 2007. In another work, a strategy [6.9] was developed for the future nano device based circuit reliability evaluation by them. The available methods of logic circuit reliability analysis are such as the numerical method based on the Bayesian network [6.10], Markov Process[6.11], Bifurcation process[6.12] etc. Apart from these methods Probability-based methods such as PGM (Probability gate model)[6.13] and PTM (probability transfer

matrix)[6.14]-[6.16] are also popular for digital logic circuits. A work on the reliability evaluation of QCA (Quantum Cellular Automata) multiplier circuit was reported by Dysart and Kogge [6.17] in 2007. In another work (in 2009) they elaborated the reliability of circuit designed with Electrostatic and Magnetic QCA [6.18]. There are some other device reliability analysis works [6.19]-[6.21] reported previously. Abdollahi in 2007 proposed a PDD (probability-decision-diagram)[6.22] based on the exact probabilistic analysis. Krishnaswamy et al. [6.23] recommended reliability technique with PTM in 2005.

Work on SED circuit reliability is reported by Shimato et al. in 1999[6.24]. The demonstration was mainly based on the reliability computation taking BER (Bit error rate) into consideration. Han and Jonker provided a promising solution[6.25] to nano-electronic component unreliable operation. In their work they investigated a NAND multiplexing based system architecture for studying the BC issues of SET. Kumder and Hoekstra proposed a circuit architectural elucidation for BC susceptibility of SET[6.26] .In 2008 Chen et al. explained a statistical model[6.27]for the analysis of circuit reliability for SE-TLG circuits. M.H. Sulieman in his work investigated the gate fan-in based reliability issues [6.28] of SED gates. Reliability of hybrid NAND, NOR with SET-CMOS is proposed by Jain et al.[6.29]. Several notable works on fault tolerance of nano-electronic system are reported [6.30]-[6.36]. Also, there are few reports on the logic circuit reliability [6.37]. Recently several research works on the reliability of combinational circuits are published [6.38]-[6.39]. The pervasive literature study in the field suggests, though a remarkable number of works on the fault tolerance of SED are reported only a countable number of works are done in the field of SED circuit reliability analysis.

## 6.3 Techniques for Reliability Evaluation

The reliability determination methodologies are broadly classified into the analytical and simulation type. Analytical evaluation technique relies upon the mathematical or simple logical relationship with some assumptions. It gives an analytical solution according to the system behavior. For small circuits, this can be applied without losing any accuracy. But along with the realistic inclusion of model parameters, analytical solutions become difficult. As a reasonable solution, the simulation methods are used for reliability evaluation of the circuits. The numerical evaluation of a system for a relevant time period with gathered data from the behavior of device model is done using the simulation method. For the stochastic systems in two ways reliability evaluation can be accomplished with the experimental and numerical type of simulation method. The observation of results of many experiment runs is the base of experimental type method. One of the most popular methods of experimental type simulation is DES (Discrete-event-simulation). Another popular method is the Monte Carlo simulation (MC) [6.40]. The MC generally imitates the real system behavior with an adaptation of parameters in each run. The numerical methods are mainly formulated to analyze stochastic models without the inclusion of any random behavior.

Another way of reliability calculation relies upon the probabilistic calculation of the error-free output. It covers the PTM, PGM based methods of reliability computation.

## 6.4 SET Reliability Issues

The revolutionary progress in technology can be achieved by novel design methods along with advancement of physics and nanotechnology. The nanoscale devices face challenges due to their noise sensitivity

known as transient faults. The statistical description of the transient faults is possible through a probabilistic approach. The possibility that a gate can produce erroneous output provides the modeling opportunity of this fault at the gate level. When the input values of the gate control the gate reliability it is called conditional otherwise unconditional.

SET is one of the promising candidates of the future nanotechnology. The major issue related to the approapriate functioning of SET is the fluctuation in background charge [6.26]. The trapped electrons and impurities in the substrate region interrupt the correct operation of the devices because of the electrostatic interaction. Besides the development of different novel schemes of computing the fault tolerant architectures can be adapted to tackle this BC issue. Due to irregularities in the fabrication, leakage or presence of the external perturbation, BCs are generated. The randomly generated BCs temporarily or permanently may hamper the operability of SETs. The individual SET based logic gate output affects the reliability of the whole circuit.

The reduction of device dimension in sub-nanometer regime may ensure the reliable SET operation with reduced sensitivity to BC. But in the foreseeable future, it is not that much feasible.

## 6.5 Reliability Analysis of the SE-TLG based circuit

### 6.5.1 Monte Carlo Simulation Based Method

The design steps along with the parameter values of the SE-TLG PLA circuit for two considered functions (F1 and F2) has been already discussed in the section 4.5.2 of the thesis. The performance evaluation of the same circuit is done through the reliability and stability analysis. This section deals with the reliability evaluation method and results of the same circuit with MC approach. The simulation-based experimental

method has been adapted over here for reliability check. Two issues related to the SED reliability are considered here such as

- Background Charge
- Diameter of the island

## *Background Charge*

The trapped charges and ionized impurities of the Silicon wafer during the fabrication procedure of SEDs introduce the random BCs at the nodes of the device. The tunneling of the electrons strongly depends upon the voltage across the tunnel junction. In presence of such extra node voltages the junction voltage gets modified according to expression (6.1).

$$V_j^{'} = V_j + V_{backgrnd} \tag{6.1}$$

Here $V_j$ is the junction voltage prior to the addition of the background charge and $V_j^{'}$ is the modified junction voltage. $V_{backgrnd}$ is the voltage due to background charge at nodes.The randomly generated BC is denoted with $\varsigma$, disturbs the circuit operation and as a result the circuit becomes unreliable. The generated charges can take any form of the random distribution. Here mainly two distribution functions are taken into account such as the normal distribution (ND) and the uniform distribution (UD) function. According to the ND where $\sigma$ is the standard deviation. Expression (6.2) defines the ND of BC .

$$p(y_1) = \frac{1}{(\sqrt{2\pi}\sigma))} e^{\left(-y_1^2/2\sigma^2\right)} \tag{6.2}$$

Where, $y_1 = y/q_e$, $y$ is the random variable with range $\pm\eta q_e$. Where the variation factor is denoted with $\eta$ .In case of the ND within two $\sigma$ , 98% of

the area is there and within three $\sigma$ 99.7% of the area is there. The value of standard deviation has been taken as $\sigma = \frac{1}{3}\eta q_e$.

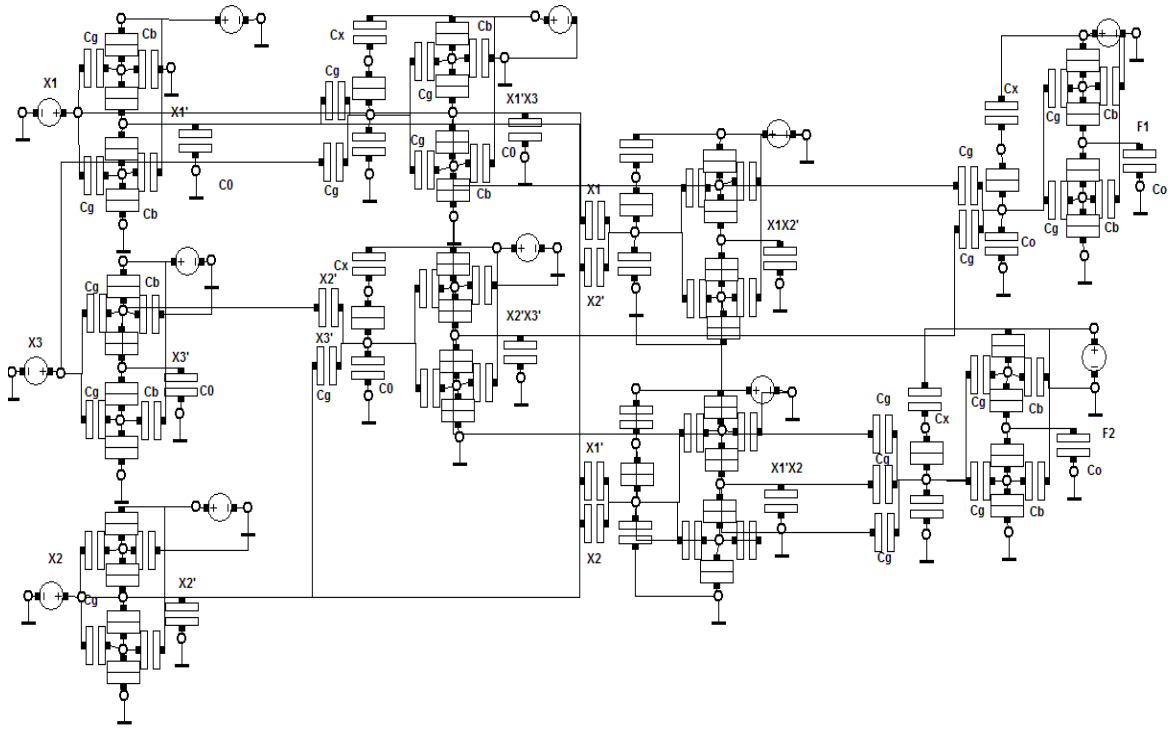



**Figure 6.1**:SE-TLG Programmable Logic Array design for function implementation.

The probability distribution function expression for UD is presented in the equation (6.3).

$$p\left(y/q_e\right) = \begin{cases} 1/2\eta, -\eta \leq\leq +\eta \\ 0, otherwise \end{cases} \tag{6.3}$$

The steps of reliability analysis are as follows

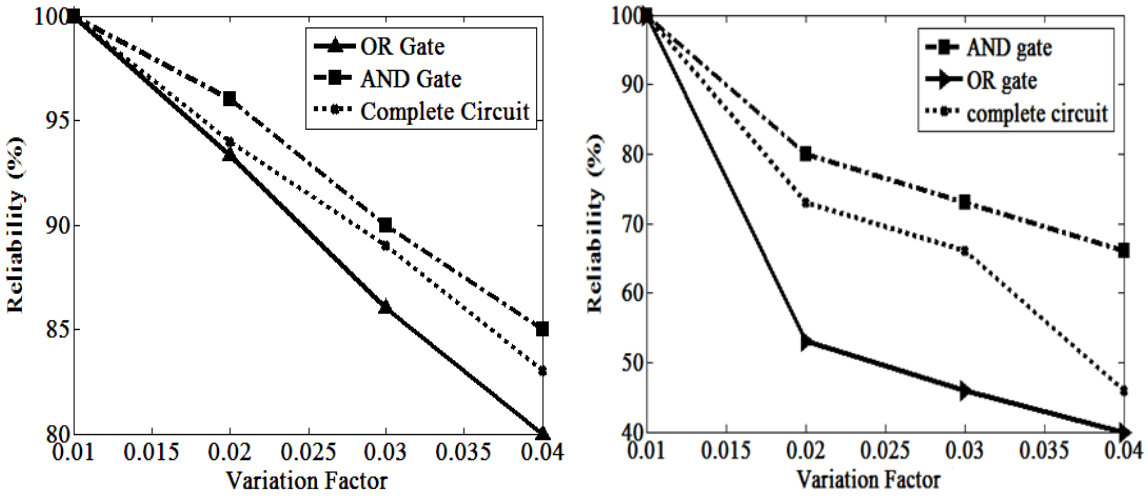
i. Random charges are generated by means of the two distribution function for different variation factors.
ii. These randomly generated charges are distributed among the different nodes of the designed circuit.
iii. The simulation results are checked with MC based simulator SIMON[6.41].

iv. The proper logical functioning of the circuit is marked as Sr or the successful result.

v. This procedure is repeated for 100 numbers of times.

vi. The ration of a successful number of results to the total number of the runs provides the reliability which is then converted to a percentage.

The individual SE-TLG logic gate reliability and the circuit as a whole both have been analyzed by using this method. The results for the ND function are furnished in figure 6.2 (a). It depicts the variation of the reliability percentage with the variation factor related to the normally distributed background charge.




(a) (b)

**Figure 6.2:** Percentage of Reliability with variation factor η for background charges (a) normal distribution and (b) uniform distribution.

According to the figure, the OR gate is more affected by the normally distributed background charge variation than the AND gate. Along with the increase in the variation factor the reliability of both the SE-TLG gate reduces. For $\eta = 0.04$ the reliability, percentage is 80, whereas for 0.01 it is 100. The complete circuit reliability depends upon the reliability of the

individual gates. It can be observed that the reliability of the overall circuit is somewhere in between the reliability of the OR and AND gate. For $\eta = 0.04$ overall circuit, reliability is near about 83% but for the variation factor, $\eta = 0.01$ it is almost 100%.In figure 6.2 (b) the effect of BC variations on the individual OR, AND layers and the whole circuit are plotted for UD of charge. The reliability of the whole circuit, as well as the individual gates, reduces with the increase in variation factor for uniformly distributed BCs. In this case, also the entire circuit reliability is in between the individual reliability of the two layers. But it has been observed that the results for the ND of charges gives better reliability than the UD as for the UD at $\eta = 0.04$ the reliability of the complete circuit is only 45% whereas for ND it is 83%. At $\eta = 0.01$ all the three reliability percentages are 100 but with a gradual increase in variation factor, the circuit reliability is tremendously affected. At $\eta = 0.02$ it becomes 71% which is much lower than the ND result. So from the results, it appears that the circuit reliability is much more affected by the uniformly distributed charges than the normally distributed charges.

## *Diameter of the island*

The electrostatic single-electron charging energy ($E_C$) depends upon the total capacitance ($C_{sum}$) and the elementary charge of the electron shown in equation (6.4)

$$E_C = \frac{q_e^{\,2}}{2C_{sum}} \tag{6.4}$$

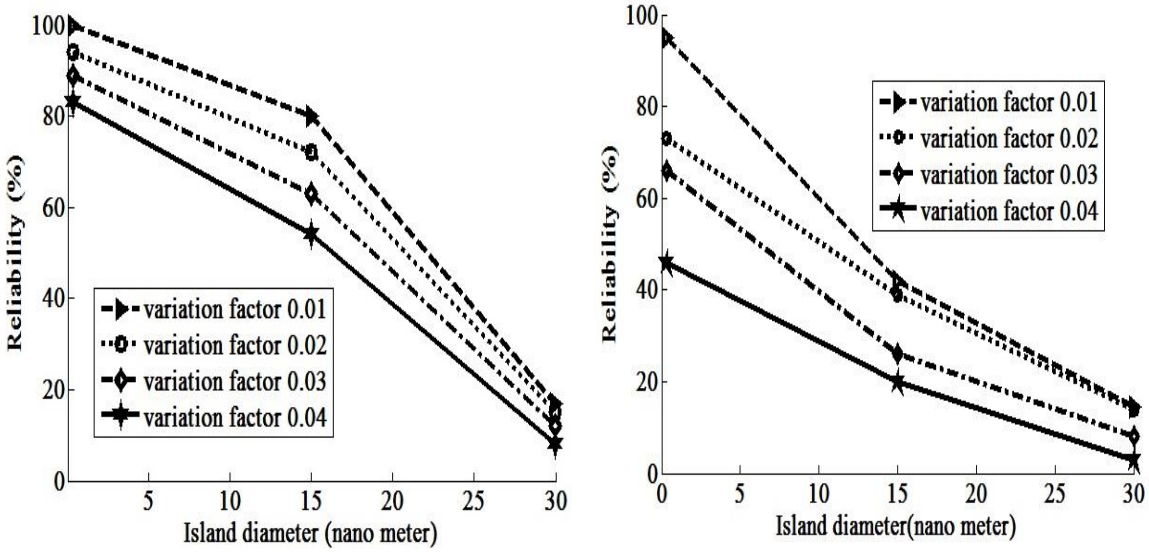
Whenever the charging energy is much more than the thermal energy the tunneling is controlled by the charging energy ($E_C >> k_B T$).

For temperature 1K, the value of total capacitance or $C_{sum}$ should be much less than 0.929 fF ($C_{sum} << 0.929\,fF$). The value of $C_{sum}$ should be

much less than 3.09aF for T=300K.The island shape and the size control the capacitance value. The fabricated islands are of mainly disc or spherical shaped. The capacitance for the disc (circular) shaped island with diameter $d$ is $4\varepsilon d$. Accordingly, the charging energy is modified as $E_C = q_e^2/8\varepsilon d$. $\varepsilon$ is the permittivity expressed with equation (6.5).

$$\varepsilon = \varepsilon_0 \varepsilon_r \tag{6.5}$$

Where, $\varepsilon_0$ (8.85x10$^{-12}$ F m$^{-1}$) and $\varepsilon_r$ are the permittivity of vacuum and insulator respectively. The value of $\varepsilon_r$ is considered here as 8 for $Al_2O_3$.



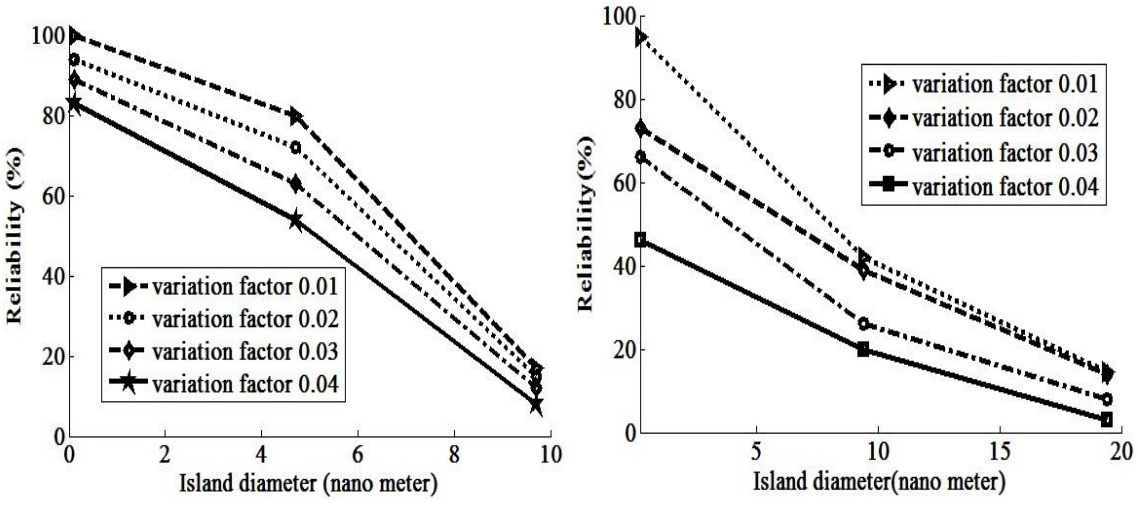

(a) (b)

**Figure 6.3:** Percentage of Reliability variation with respect to diameter of the island (disc) with(a) normal distribution and (b) uniform distribution of background charges.

The figure 6.3 (a) and (b) are plotted for checking the reliability percentage variation with the diameter of disc-shaped island. Different variation factors related to the ND and the UD are varied respectively for figure 6.3 (a) and (b). The range of diameter is considered up to 30nm according to the calculations based on the related charging energy

expression and equation (6.4). The percentage reliability decreases with the increase in the diameter of the circular disc-shaped island. For different variation factors, the reliability percentage is checked with increasing disc island diameter in figure 6.3 (a) for ND of charges. For $\eta = 0.04$ at 10nm diameter the reliability is 60% and at 30nm it is below 15 %. The reliability result is 90% and 18% respectively for 10nm and 30nm diameter with 0.01 variation factor. It indicates for increasing disc island diameter the reliability percentage degrades for higher values of $\eta$.

The same procedure of reliability analysis with UD is carried out and illustrated in figure 6.3 (b). The diameter range under consideration is from 0.35 nm to 30 nm for disc-shaped island and for η the considered values are 0.01,0.02,0.03,0.04. From the figure, it is clear that the ND exhibits better result than the uniform one. The variation of reliability for diameter variation is from 100% to 8% for ND,whereas in case of UD the variation is from 100% to 3 %. With η above 0.01 even for 5nm diameter, all the reliability percentages are below 80 for figure 6.3(b).




(a) (b)

**Figure 6.4**: Percentage of Reliability with island (sphere) diameter variation for different variation factors of (a) normal and (b) uniform background charge distribution.

The results of the spherical island reliability are plotted in figure 6.4 (a) and (b) for the normal and uniform distributed BCs respectively. For both the graphs, nature is same as discussed for the disc island case. The $C_{sum} = 2\pi\varepsilon d_{sphere}$ where $d_{sphere}$ is the diameter of the spherically shaped island. Thus the charging energy is modified to $E_C = q_e^{\,2} / 4\pi\varepsilon d_{sphere}$. Figure 6.4 (a) is plotted for diameter range up to 10nm starting from 0.22nm for ND whereas for figure 6.4 (b) the range is considered up to 19.4nm for UD of charges. For both the figures the reliability percentage for 0.04 variation factor reduces to 0, this is the reason behind the consideration of the range of island diameter to be chosen within the above stated limit. Similar kind of result is observable for the figure 6.3 and 6.4. The reliability percentage is mostly dominated by the UD. The increasing diameter of both shape of island reduces the reliability of the complete circuit. Moreover, the increase in variation factor is also responsible for the reduction in reliability percentage.

### 6.5.2 Monte Carlo with PTM

This sub-section of the thesis chapter elaborates a combined formulation of the Monte Carlo and PTM (Probability Transfer Matrix) based method of reliability evaluation, simulated with MATLAB platform. The individual gate error probabilities of the SE-TLG circuit [6.42]-[6.44] are determined with the MC method as mentioned in section 6.5.1 and applied to determine the PTM of the complete circuit. Further the reliability evaluation is accomplished with PTM. The reduction of computation complexity and time is the main aim of this method.

The MC method uses the tunnel rate equations as input for all the tunnel events. The change in free energy gives the expression of the tunnel rates shown in equation (6.6) and (6.7).

$$\Delta F_E = E_{final} - E_{initial} + workdone \tag{6.6}$$

$$\Gamma_R = \frac{-\Delta F_E}{q_e^2 R_t (e^{\Delta F_E / k_B T} - 1)} \tag{6.7}$$

Entire circuit reliability analysis by simulating the circuit for multiple numbers of times in SIMON increases the time complexity. Reliability analysis with PTM formulation from the individual gate error percentage reduces the time. The steps of the process are as follows

*Step1*: Two sets of 100 random numbers are generated with the UD and ND

*Step 2:* Individual gate error percentage is determined with MC by computing the ration of error-free output to the total run is determined. It gives individual gate error percentage.

*Step 3*: PTM of the individual gate is formed and applied to the complete circuit PTM.

*Step 4*: Complete circuit reliability is calculated.

**Table 6.1**: Reliability of AND, OR, NOT gate for uniform and normal distribution variation factors.

| **Gates** | **Uniform Distribution Variation factor** | | | | **Normal Distribution Variation factor** | | | |
|---|---|---|---|---|---|---|---|---|
| | **0.01** | **0.02** | **0.03** | **0.04** | **0.01** | **0.02** | **0.03** | **0.04** |
| **AND** | 0.99 | 0.80 | 0.73 | 0.66 | 1 | 0.96 | 0.90 | 0.85 |
| **OR** | 0.99 | 0.51 | 0.46 | 0.40 | 1 | 0.93 | 0.86 | 0.80 |
| **NOT** | 1 | 0.84 | 0.81 | 0.72 | 1 | 0.98 | 0.94 | 0.89 |

As an example reliability of a SE-TLG based combinational circuit is evaluated in this section with above mentioned steps. In the earlier section already the calculation of the gate reliabilities for normal and uniform distribution of BC through the simulation of the circuit for different variation factors are elaborated. All the of individual gate error free output percentage considered for the process are tabulated here in

Table 6.1. For normal distribution with variation factor (vf) 0.02 the individual gate reliability or probability of error free output are 0.93, 0.96, 0.98 for OR, AND, NOT SET based gates respectively.

### 6.5.2.1 Probability Transfer Matrix formation and Reliability calculation

The PTM is one of the reliability analysis methods. In this method, the individual gates are represented by their PTMs. According to the circuit configuration (series connected and parallelly connected), it is decided how to compute the overall PTM. In PTM matrix $(i \times j)$, the entry indicates for given input value i probability of occurrence for output j, i.e. $P(j|i)$ .

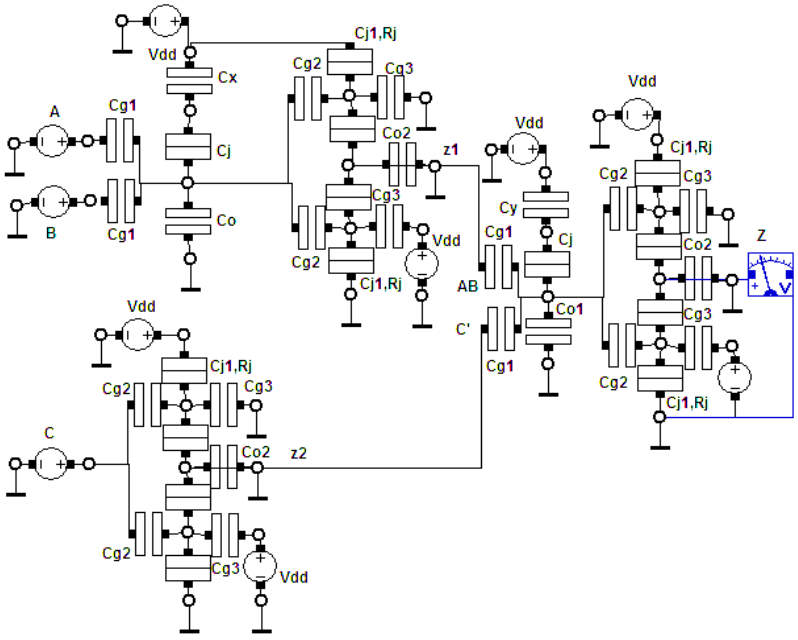



**Figure 6.5:** Single electron tunneling based combinational circuit for function $Z = AB + \overline{C}$ , where A, B,C are three inputs.

Here the signal probability [6.45] is considered as 0. BC effects are accounted for the reliability of SE-TLG circuits. Complete circuit PTM provides the path to compute the reliability percentage.

Here the reliability percentage determination of a combinational circuit described in the stepwise manner using the PTM method.

The reliability analysis of the circuit shown in figure 6.5 is done in this part. The circuit consists of a buffered AND, a buffered OR and a NOT gate. In Layer 1 z1($z1=AB$) and z2 ($z2=\overline{C}$) are generated as output from the AND and NOT gate. The next layer combines the two parallel outputs. Complete circuit PTM is denoted with $PTM_2^{SE-TLG}$ and determined as per the equations (6.8) and (6.9)

$$PTM_1^{SE-TLG} = PTM_{AND}^{SE-TLG} \otimes PTM_{NOT}^{SE-TLG} \tag{6.8}$$

$$PTM_2^{SE-TLG} = PTM_1^{SE-TLG} \bullet PTM_{OR}^{SE-TLG} \tag{6.9}$$

$PTM_1^{SE-TLG}$ is the Layer 1 PTM and represented with equation (6.15). Where the individual gate PTMs for AND, NOT,OR are denoted with $PTM_{AND}^{SE-TLG}$, $PTM_{NOT}^{SE-TLG}$, $PTM_{OR}^{SE-TLG}$ respectively.

***A. Determination of*** $PTM_{AND}^{SE-TLG}$, $PTM_{NOT}^{SE-TLG}$ ***and*** $PTM_{OR}^{SE-TLG}$ ***:***

From the truth table of the AND gate related $ITM_{AND}^{SE-TLG}$ (Ideal transfer matrix) is generated. ITM is the error-free PTM. Equation (6.10) and (6.11) represents ITM and PTM of AND.

$$ITM_{AND}^{SE-TLG} = \begin{array}{c} \\ 00 \\ 01 \\ 10 \\ 11 \end{array} \begin{array}{c} \begin{array}{cc} 0 & 1 \end{array} \\ \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \end{array} \tag{6.10}$$

$$PTM_{AND}^{SE-TLG} = \begin{matrix} 0 & 1 \end{matrix} \begin{bmatrix} q_{AND}^{SE-TLG} & 1-q_{AND}^{SE-TLG} \\ q_{AND}^{SE-TLG} & 1-q_{AND}^{SE-TLG} \\ q_{AND}^{SE-TLG} & 1-q_{AND}^{SE-TLG} \\ 1-q_{AND}^{SE-TLG} & q_{AND}^{SE-TLG} \end{bmatrix} \quad (6.12)$$

Here $q_{AND}^{SE-TLG}$ is the probability of error-free output and $(1-q_{AND}^{SE-TLG})$ is the probability of erroneous output for the AND gate. For ITM $q_{AND}^{SE-TLG}=1$.

$$PTM_{NOT}^{SE-TLG} = \begin{matrix} 0 & 1 \end{matrix} \begin{bmatrix} p_{NOT}^{SE-TLG} & q_{NOT}^{SE-TLG} \\ q_{NOT}^{SE-TLG} & p_{NOT}^{SE-TLG} \end{bmatrix} \quad (6.13)$$

The PTMs of the NOT and OR gates are formulated using the same concept and shown in equation (6.13) and (6.14).

$$PTM_{OR}^{SE-TLG} = \begin{matrix} 0 & 1 \end{matrix} \begin{bmatrix} q_{OR}^{SE-TLG} & p_{OR}^{SE-TLG} \\ p_{OR}^{SE-TLG} & q_{OR}^{SE-TLG} \\ p_{OR}^{SE-TLG} & q_{OR}^{SE-TLG} \\ p_{OR}^{SE-TLG} & q_{OR}^{SE-TLG} \end{bmatrix} \quad (6.14)$$

Here $p_{NOT}^{SE-TLG}$, $p_{OR}^{SE-TLG}$ are the error probabilities of the NOT and OR gate respectively, whereas the $q_{NOT}^{SE-TLG}$ and $q_{OR}^{SE-TLG}$ are the probabilities of error-free output for NOT and OR gate respectively. By substituting the values of $PTM_{NOT}^{SE-TLG}$, $PTM_{OR}^{SE-TLG}$, $PTM_{AND}^{SE-TLG}$ in equation (6.8) and (6.9) $PTM_1^{SE-TLG}$ and $PTM_2^{SE-TLG}$ are determined.

### *B. Reliability Calculation from the PTM*

ITM of the complete circuit is expressed in equation (6.15)

$$ITM_{Ckt} = \begin{matrix} 0 & 1 \end{matrix} \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 0 & 1 \\ 1 & 0 \\ 0 & 1 \\ 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \quad (6.15)$$

The ETM (Element Transfer Matrix) of the entire circuit is evaluated by doing the element-wise multiplication of PTM and ITM according to the following expression (6.16).

$$ETM_{Ckt} = PTM_{2}^{SE-TLG} * ITM_{Ckt} \quad (6.16)$$

The ETM consists of the desired input/output values as all the erroneous values are zeroed out. The reliability of the circuit is the probability of the correct output. Finally, ETM is multiplied with a column vector k having $2^n$ values, where n is the number of inputs, for reliability calculation.

The column vector k has the elements which are actually the probability of each input combination occurring. As here A,B,C are the 3 inputs, the number of elements in the column vector is 8. Considering the probability of each input combination to occur equally the value of each element is equal to 1/8=0.125. In this way, k is generated as shown in equation (6.17).

$$k = \begin{bmatrix} 0.125 \\ 0.125 \\ 0.125 \\ 0.125 \\ 0.125 \\ 0.125 \\ 0.125 \\ 0.125 \end{bmatrix} \quad (6.17)$$

The following expression (6.18) is used to determine the reliability of the complete circuit.

$$R_{ckt} = \sum_{ITM(x,y)=1} p(y|x).p(x) \tag{6.17}$$

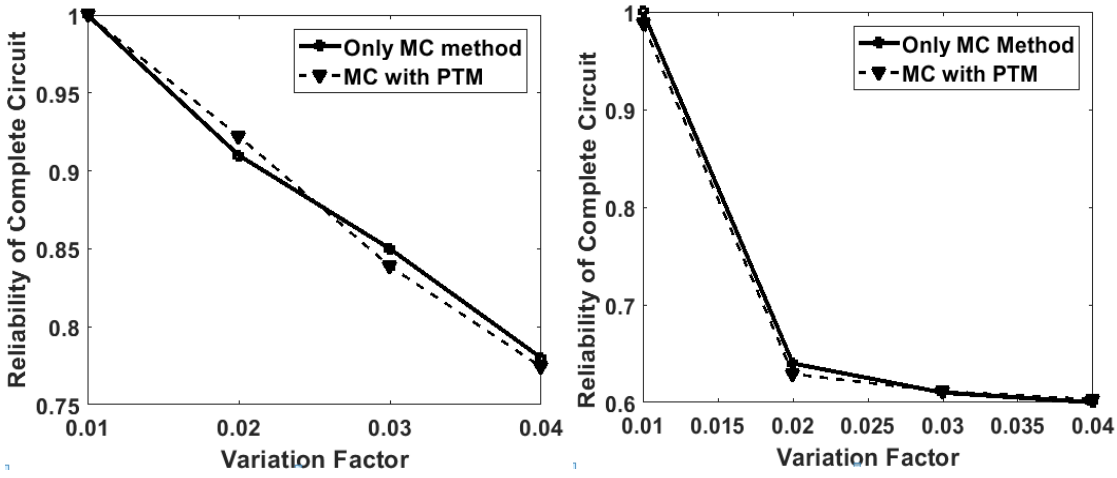
*p(x)* is the probability of input *I* to be $I_x$. Expression (6.18) provides the summation of all the probabilities for the correct outputs. If the element (x,y) of the ITM has a value 1 then only that specific position (x,y) element of PTM matrix contributes to the sum. The above expression gives the accurate reliability assessment as the PTM is considered to provide a probability of getting correct outputs exactly.

## 6.5.2.2 Results

The results are checked for two conditions one is for the different gate reliability and another one is for same gate reliability. The first one treates the individual gates of the circuit separately and their corresponding percentage of error free output is used for overall circuit performance metrics. The values of individual gates are already discussed in the previous sections with MC method. In the second case it has been considered that all the gates are having equal error. According to this two cases the overall SE-TLG combinational circuit (shown in figure 6.5 ) reliability is determined.

### *A. For the Different Values of Gate Reliability*

Using the values of error free output percentage with ND and UD from Table 6.1 figure 6.6 (a) and (b) is depicted. Results of the only MC based and MC along with PTM based techniques are presented here with ND of background charges in figure 6.6 (a).




(a) (b)

**Figure 6.6:** Complete circuit reliability with variation factor for only MC based approach and MC with PTM Approach (a)for ND (b) for UD

The circuit reliability is plotted for different variation factors for both the methods. For the $vf_n$.(variation factor of ND) 0.01, $R_{ckt}$=1with MC method as well as MC combined with PTM method. But with increase in $vf_n$ values from 0.01 to 0.04, $R_{ckt}$ decreases monotonically from values 1 to 0.7742 for combined MC-PTM method. The MC method result for the same $vf_n$ is 0.78. The error probability of the circuit on the other hand increases with both methods. The figure indicates the results of both the methods are near to each other for ND.

The work is repeated for the UD and depicted in figure 6.6(b). It displays the $R_{ckt}$ falls with the $vf_u$ (variation factor of UD ). For $vf_u$=0.02, $R_{ckt}$ is even below 65% for both the approaches. For rest of the values of $R_{ckt}$ are almost adjascent to each other for the two techniques. The simulation time for individual gate reliability is same for both the methods as first step is executed with MC only. The second part takes 0.03168 Sec time for the combined MC-PTM as it is executed with MATLAB coding inspite of simulating the circuit 100 times in SIMON (in only MC method).

SIMON simulation in contrast needs almost more than 1minute time as a whole to complete 100 times circuit simulation.

### *B. For the same values of gate reliability:*

For $q_{AND} = q_{OR} = q_{NOT}$ the whole circuit reliability or error-free output, probability can be extracted. Table 6.2 displays the gate error probability, gate reliability, corresponding output error probability and output reliability. Using the values the $R_{ckt}$ is evaluated with PTM approach as 89.54% and output error probability is 10.46%.

**Table 6.2:**Reliability for Equal Probability Values For All Gates

| Gate error | Gate reliability | Output error probability | Output Reliability |
|---|---|---|---|
| 0.05 | 0.95 | 0.1046 | 0.8954 |
| 0.10 | 0.9 | 0.194 | 0.8060 |
| 0.15 | 0.85 | 0.2694 | 0.7306 |
| 0.20 | 0.80 | 0.332 | 0.6680 |
| 0.25 | 0.75 | 0.3828 | 0.6172 |
| 0.30 | 0.70 | 0.428 | 0.5770 |
| 0.40 | 0.6 | 0.476 | 0.5240 |
| 0.50 | 0.50 | 0.50 | 0.50 |
| 0.60 | 0.40 | 0.504 | 0.4960 |

Figure 6.7 illustrates the variation of the output reliability with gate reliability variation where all the gate probabilities are considered as same. From the figure, it is clearly noticeable that along with the reduction in the individual gate reliability the output reliability also falls.

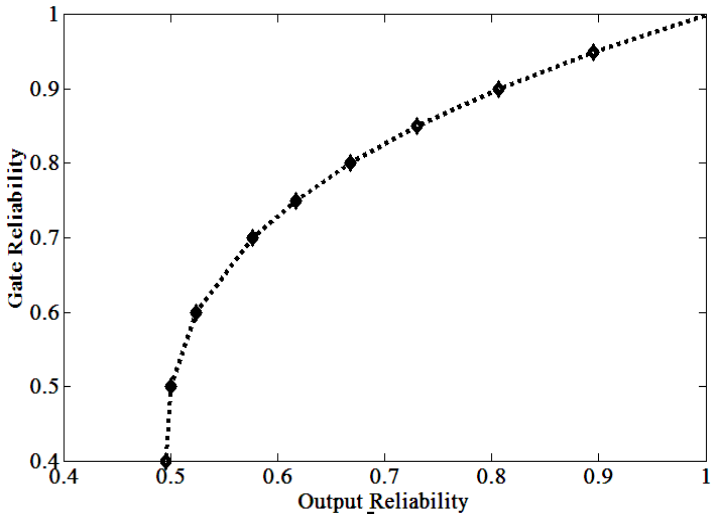



**Figure 6.7:** Output Reliability variation with the gate reliability

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# Chapter 7

# STABILITY ANALYSIS



## 7.1 Introduction

The stability of SEDs [7.1]-[7.3] is defined as the condition in which no tunneling takes place or system stays in the Coulomb blockade (CB) region [7.4]-[7.10]. It can be determined by the input bias combinations, and the tunneling rate $(\Gamma_R)$ which is proportional to the free energy change ($\Delta F_E$).The change in free energy is evaluated with the difference between final ($E_{Final}$) and the initial energy ($E_{initial}$).Free energy of a circuit is calculated by summing up the stored charges in the capacitors and charge transported by the voltage sources.

If the temperature is non zero but charging energy is greater than the thermal energy the electron tunneling occurs after $t_D$ time. This is applicable when the free energy change is below 0, otherwise tunneling event probability becomes 0. No tunneling implies the stable state of operation i.e. at T=0K, $\Gamma_R = \frac{-\Delta F_E}{q_e^2 R_t}$ for $\Delta F_E < 0$ and at 0K $\Gamma_R = 0$. For 0K

temperature, if no tunneling occurs through the single electron tunnel junction then the bias condition is said to be at stable state if there is no quantum fluctuation or co-tunneling. The stable state, in other words, indicates the CB region. Generally, the stability of an SED is analyzed with a two-dimensional stability diagram. The stability diagram [7.11] is often plotted with the bias voltages in both the axes x and y. The points are color coded for indicating unstable and stable points. The intermediate unstable grey valued points denote the current flowing strength or the tunnel event numbers for a specific time interval. The white points are the indications of no current at all whereas the black points denote more numbers of tunnel events or strong flow of current. For the non-zero temperature or even in presence of co-tunneling [7.12]these stability plots become useful due to the color coding. Apart from bias voltages the temperatures and other circuit related parameters such as circuit capacitance or the resistances can also be plotted in the stability diagrams for generalization. These generalized stability plots are further used for the parameter optimization of a SED circuit.

The simulation of the SED circuits is mainly done by tried and proven Monte Carlo algorithm [7.13]-[7.14] for their stability analysis. In case of Single-electron circuits, strong confinement of electron takes place on quantum dots (islands) which can be accurately modeled as the discrete-event oriented regime. In this discrete event oriented regime the MC method is proved to be very intuitive and effective.

Usually, for absolute stability, zero temperature and zero cotunneling are considered. The circuit can be always lifted to the excited state due to thermal agitation or presence of co-tunneling. This problem is successfully handled with the use of the genetic algorithm [7.15] and simulated annealing technique[7.16].

The stability results of the SE-TLG [7.17]-[7.20] based PLA [7.21] circuit is presented and judged in this part of the thesis. Often the different

system or circuit parameters affect the circuit stability. The investigation of the stability of SE-TLG inverting buffer with the same approach is executed for different parameter variations. Further, the work concentrates towards the hybrid SET-CMOS inverter circuit stability determination.

## 7.2 Literature Survey

The stability is associated with the CB region. The theory of CB oscillation was proposed by Beenakker in 1991[7.22]. In 1992 the analytical method of plotting the stability diagram was introduced by Grabert and Devoret [7.23] . The observation of CB at 77K was done by Chen et al [7.24] in 1995. Several other CB related theoretical and experimental works [7.25]-[7.29] were proposed in earlier days. In 1989 N. Bakhvalov et al.[7.30] first proposed MC method for SED circuit simulation. Kirihara et al. [7.31] in 1994, S.A. Roy in 1994 [7.32] followed by Chen et al. in 1996 [7.33] adopted this method for SED circuit simulation. Günther Lientschnig designed an online stability plot simulator named SETNETS[7.34]. Amakawa et al. in 2001 presented the stability diagram for Single Electron pump circuit [7.35]. Shin et al. analytically plotted the stability diagrams of stability of a coupled-SET [7.36] in the same year. A stability diagram based on ME model for multi-island SET [7.37] was proposed in 2010 by Zhang. Imai et al. deliberated stability plots of SET with single gate double dots [7.38] for different values of gate capacitance and arbitrary junction number. The stability evaluation of the SET based Carry look ahead adder [7.39] was reported in 2015. Azuma et al. observed of rhombic shaped coulomb diamond in a chemically anchored nano-sized gold [7.40] particle SET in 2016. The simulation of the hybrid SET-CMOS architecture based NAND and NOR gate has also been reported in 2014[7.41]. Takiguchi et al. extracted

stability diagrams with analytical calculation of SETs with and without input discretizer [7.42]. Analysis of CB and coulomb diamond of fullerene SET [7.43] is recently explained by Hoesseini et al. The detailed survey of previously done work on stability indicates most of the works are based on the numerical analysis or the experimental observation of stability diagrams. Very less attention has been given to the simulation based stability diagram observation of the SED based circuits as a whole.

## 7.3 Determination of Stable Region

The determination of the stability plot or the stability diagram is possible using two ways – analytical approach [7.44] or the simulation approach. In case of analytical approach certain steps are to be followed to determine the equations and after solving those equations it is possible to detect the stable region. But in case of the simulation type of stability determination, the whole SED based circuit is designed and simulated in the SIMON [7.45] environment for plotting the stability diagram. According to the plotted stability diagram, the circuit stability is analyzed. The method adopted here is mainly the simulation type for stability analysis of the circuits.

### 7.3.1 Analytical Approach

For the analytically determining[7.23] the stable regions the following steps are to be followed-

a. State of the circuit is considered first
b. Calculation of the change in free energy due to every tunnel event as a function of both the bias voltages of two axes is done.

c. Zero change in the free energy defines the stable region boundaries
d. The stability plot is divided into stable and unstable half-planes.
e. The intersection of the stable half –planes results in a convex polygon shaped stable region

Figure 7.1 (a) shows the circuit of SET with the different bias voltages and the connected capacitors. The voltage across the junctions is marked as $V_D$ and $V_S$. The charge of the island is indicated as $-nq_e$. The tunnel characteristics capacitance and resistances are marked with $C_d$, $C_s$ and $R_d$, $R_s$ (where 's' indicates the source side and 'd' indicates the drain side). $V_G$ is the voltage source connected to gate terminal through $C_g$ capacitor. From the figure 7.1 (a) the four free energy change values are determined as presented in equation (7.1)-(7.4).

$$\Delta F_{E1} = \frac{q_e}{C_{sum}}\left[ nq_e + \frac{q_e}{2} - C_s V_{ds} - C_g V_G \right] \tag{7.1}$$

$$\Delta F_{E2} = \frac{q_e}{C_{sum}}\left[ -nq_e + \frac{q_e}{2} + C_s V_{ds} + C_g V_G \right] \tag{7.2}$$

$$\Delta F_{E3} = \frac{q_e}{C_{sum}}\left[ nq_e + \frac{q_e}{2} + C_s V_{ds} - C_g V_G \right] \tag{7.3}$$

$$\Delta F_{E4} = \frac{q_e}{C_{sum}}\left[ -nq_e + \frac{q_e}{2} - C_s V_{ds} + C_g V_G \right] \tag{7.4}$$

The tunneling rates are generated with (7.5) and by calculating different free energy changes with (7.1)-(7.4).

$$\Gamma_R = \frac{-\Delta F_E}{q_e^2 R_t \left( e^{\Delta F_E / k_B T} - 1 \right)} \tag{7.5}$$

Where, $\Delta F_E = E_{Final} - E_{initial}$ , $\Gamma_R$ is the tunneling rate which is defined as the average tunnel events per second, $\Delta F_E$ is the free energy change due to tunneling, $E_{Final}$ is the final and $E_{initial}$ is the initial energy, T is

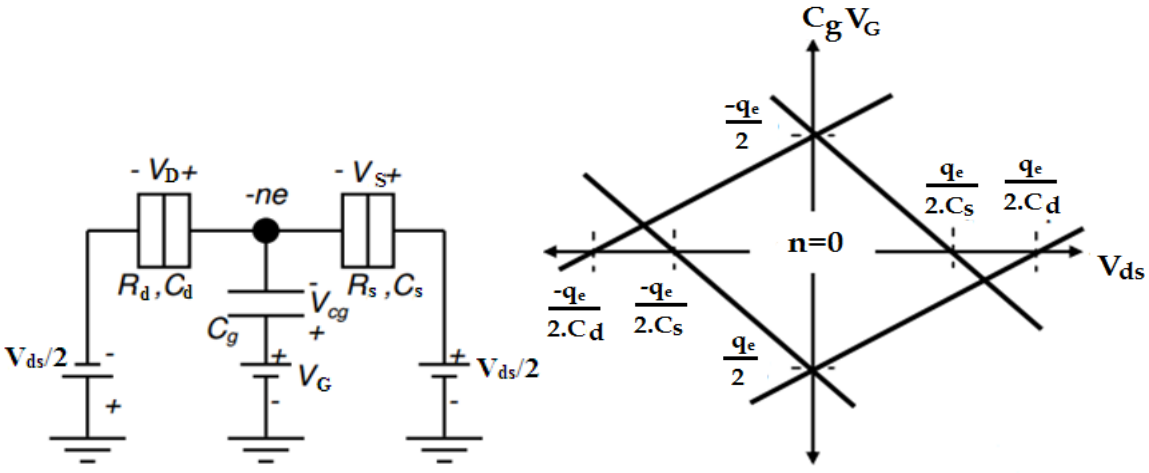
the temperature. The four tunneling rate equations (7.6)-(7.9) provide the four boundary conditions of the stability plot.

$$\Gamma_{R1}:\left[nq_e+\frac{q_e}{2}-C_sV_{ds}-C_gV_G\right]<0 \tag{7.6}$$

$$\Gamma_{R2}:\left[-nq_e+\frac{q_e}{2}+C_sV_{ds}+C_gV_G\right]<0 \tag{7.7}$$

$$\Gamma_{R3}:\left[nq_e+\frac{q_e}{2}+C_sV_{ds}-C_gV_G\right]<0 \tag{7.8}$$

$$\Gamma_{R4}:\left[-nq_e+\frac{q_e}{2}-C_sV_{ds}+C_gV_G\right]<0 \tag{7.9}$$




(a) (b)

**Figure 7.1:** (a)SET circuit for Stability Diagram with two tunnel junctions and a gate terminal (b) Analytically determined Stability Diagram of the SET circuit

Figure 7.1 (b) shows the stability plot for the SET circuit depicted in figure 7.1 (a) with $C_g << C_s$ and $C_d$ both. Here n(state) is considered as 0. Due to unequal values of $C_s$ and $C_d$, applicable for asymmetric junctions, the plot is tilted. The area enclosed by the four boundaries is the stable zone inside which the tunneling rate is zero.

The analytical approach of stability analysis is time consuming even for small circuits. Whenever a larger circuit is considered for stability analysis it becomes almost impossible to generate and track all the related tunneling rate equations for all the circuit states. So the simulation method is generally embraced for the stability evaluation of the SED based larger circuits.

### 7.3.2 Simulation Approach

There are several simulation tools available for SED circuits among them the MC based tools are SIMON, KOSEC[7.46], MOSES[7.47] etc. Using the mentioned simulation tools also it is possible to generate the stability plot for analysis of the concerned circuit stability condition.The heart of the MC approach is the generation of pseudo-random numbers. The time interval ($\Delta t_{\text{int}}$) of two consecutive tunnel events is determined with equation (7.10).

$$\Delta t_{\text{int}} = \frac{-\ln(r_n)}{\Gamma_{\text{int}}} \tag{7.10}$$

Where $r_n$ is the uniformly distributed random number over (0,1) interval and $\Gamma_{\text{int}}$ is the tunnel rate.

The steps of Monte Carlo Method-

i. Concrete random time for tunnel is calculated for all listed possible tunnel events and their corresponding tunnel rates.

ii. Event with small time requirement happens first.

iii. According to tunnel event computation, node charges are updated as a result the node potentials are also changed.

iv. Charge per time interval computed according to winning tunnel events results in the current.

v. Electrons are transported along a certain path due to each tunnel event.

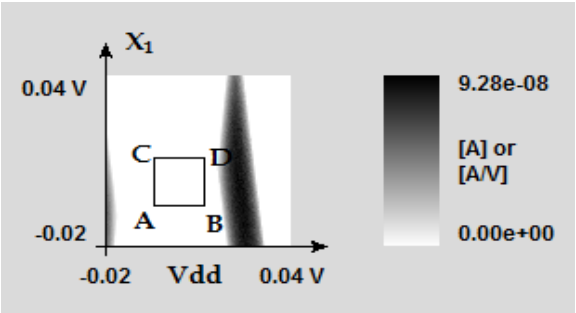
vi. Through stochastic sampling, a new winner is determined from the newly calculated tunnel rates. On the basis of summing and averaging of all the transported charges in each circuit branch, the new tunnel rates are formulated.

vii. Repeating this several times gives the macroscopic behavior of the circuit.

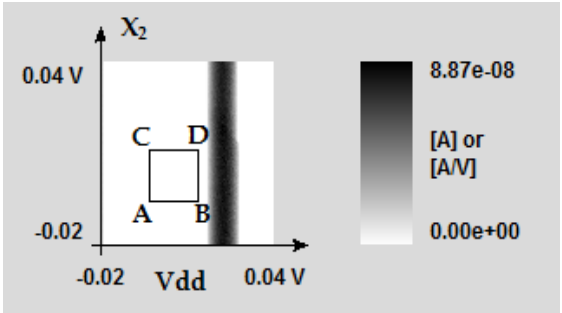
The SIMON (Simulation of Nano-Structure) simulator has been used here to simulate the stability plot of the SE-TLG PLA circuit and inverting buffer. This GUI software is developed by C. Wasshuber at Microelectronics, TU, Vienna. SIMON based stability plots can be generated for two voltage sources or even for the variation of capacitance, the resistance or operating temperature variations.

## 7.4 Stability Analysis of SE-TLG based PLA circuit

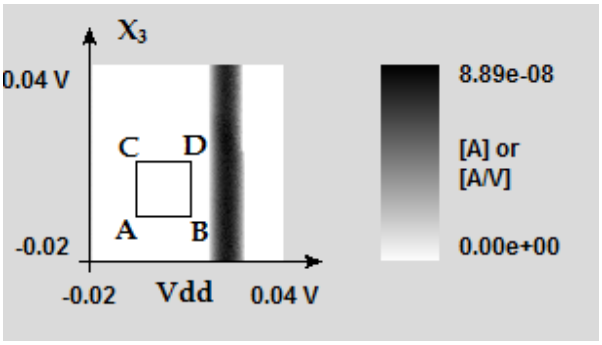
This section deals with the detailed explanation of the stability analysis of SE-TLG based PLA circuit for the function $F1=X_2'X_3'+X_1'X_3$ and $F2=X_1'X_2+X_1'X_3+X_1X_2'$ explained in Section 4.5.2. Through the stability, diagram plotted using the SIMON 2.0, an MC based simulation tool, the stability analysis of the designed circuit has been evaluated. The two input signals are plotted in the two axes of the stability plot.




(a)




(b)




(c)

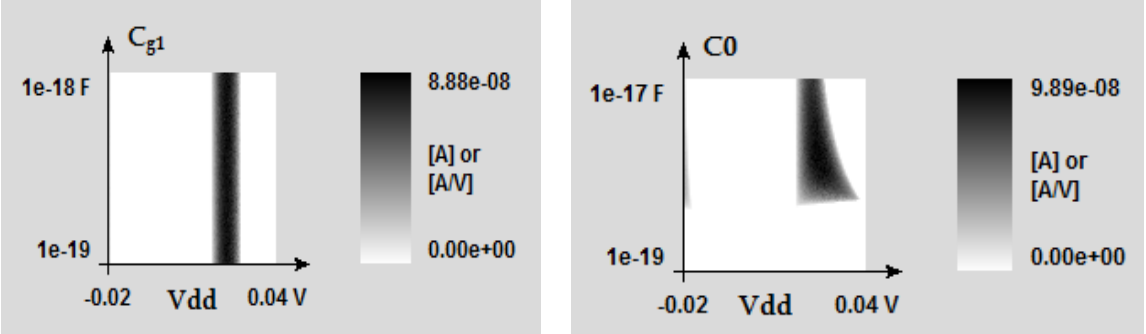
**Figure 7.2:** Designed PLA circuit Stability plot of the different combinations of input and power supply signal (a) Vdd and $X_1$ (b) Vdd and $X_2$ (c) Vdd and $X_3$ with A [0, 0], B [1,0],C [0,1],D [1,1] at T= 0 K.

Corresponding to all the combinations of the input signals the free energy changes are calculated. In all the above stability plots are shown in figure 7.2(a),(b),(c) and (d), A, B, C, D four logic points are marked.

Here A corresponds to the logic vector [0,0], B indicates logic vector combination of [0,1], C is interpreted as [1,0] and the D is for [1,1] at T=0K. The logic high level is indicated with 16mV and the logic low indicates 0mV.The Figure 7.2 (a)shows the stability plots for power supply Vdd versus input $X_1$, where stability point A[0,0] defines logic 0 for both the signals.Vdd is 16mv but input $X_1$ is 0mV for B stability point [1,0].The stability point C[0,1] indicates input Vdd=0mV and $X_1$at 16mV . When both the inputs Vdd, $X_1$ are at 16mV, it is specified with D [1,1]. The stability plots for $X_2$ with Vdd and X3 with Vdd are presented in figure 7.2 (b) and (c) respectively. The interpretation of the control signal vectors (A,B,C,D) remain same for the figure 7.2 (b) and (c). The stability analysis time for all the three above mentioned combinations of signals is 33Seconds for each in SIMON. The charge fluctuation ranges for the three figures are in the range of $9.28x10^{-8}$, $8.87x10^{-8}$ and $8.89x10^{-8}$ respectively.

No electron tunneling or the stable state is marked with the white region and the local minima of the circuit free energy are related to this region.

Likewise, the black point indicates the circuit free energy local maxima. The grey points represent small current flow through the junction. With the tunnel junction current flow, the shades of the grey level starting from white to black varies.The circuit is stable as all the stability points (A,B,C,D) are within the white region of the stability plot.




(a) (b)

**Figure 7.3:** Stability plot (a) Vdd with Cg1 and (b) Vdd with C0 for PLA

The stability diagram not only plots two bias voltages for stable operation determination but can be also used for the parameter optimization. Here in Figure 7.3 (a) and (b) such two stability plots are shown where the capacitors $C_{g1}$, C0 are plotted against Vdd. The first plot figure 7.3 (a) gives an estimation of the $C_{g1}$ value to be chosen. For the Vdd values -0.02V to 0.02V with $C_{g1}$ values starting from $1x10^{-19}$ F to $1x10^{-18}$ F circuit remains in stable condition. But for a specific range of Vdd starting from 0.02V to 0.028V, for all the $C_{g1}$ values instability occurs. The fluctuation range in this region is from 0 to $8.88x10^{-8}$. In figure 7.3 (b) when Vdd is above 0.02V and C0 is near about above $0.5x10^{-18}$F fluctuation occurs and circuit stability is hampered otherwise the system remains stable. The range of fluctuation, in this case, is from 0 to $9.89x10^{-8}$.

## 7.5 Parametric Variation Effects on Circuits Stability of SET inverting Buffer

The buffer is one of the essential parts of any digital or analog circuit design. The networks formed with TLGs often require static buffer circuits to be added as a backend to trim down the feedback and feedforward effect. They can be of two types –inverting buffer or the NOT gate and the non-inverting buffers. The inverting buffer circuit [7.48]-[7.49] designed with the combination of SETT and TLG concept is presented in figure 7.4. The TLG function of the inverting buffer is given in the following expression (7.11).

$$V_{output} = \text{sgn}\{-V_{input} + Vdd/2\} \tag{7.11}$$

While designing the buffer circuit two conditions are generally fulfilled– firstly delay of the circuit should be minimized while using them in the buffered TLGs and single power supply needs to be used for the TLG circuits and the buffer both.

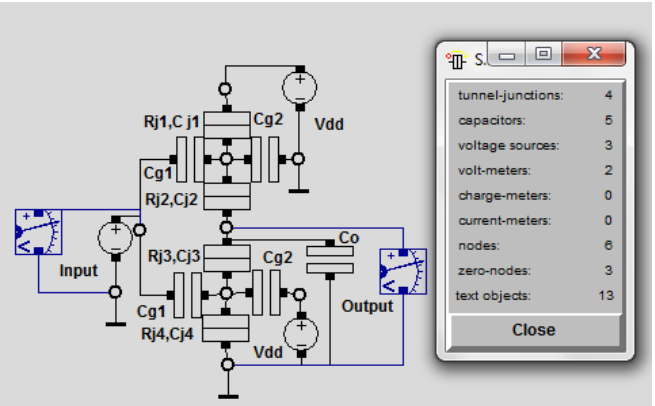



**Figure 7.4:** Inverting Buffer circuit with SET

The design consists of two SETs behaving in a complementary fashion. The parameters are chosen in such a manner that similar kind of switching behavior is shown by them. Figure 7.4 shows the structure of inverting buffer with two SETs marked as SET1 and SET2. Here SET1

behaves as nSET and SET2 behaves as pSET. Rj1,Rj2,Rj3,Rj4 and Cj1,Cj2,Cj3,Cj4 are the junction resistances and capacitances associated to the four tunnel junctions respectively. Cg1 and Cg2 are the gate capacitances. The power supply is denoted with Vdd and Co is the load capacitor. For the symmetric operation of the two SETs are ensured by making the parameter values matched i.e. Rj1=Rj4=Rj2=Rj3, Cj1=Cj4,Cj2=Cj3.

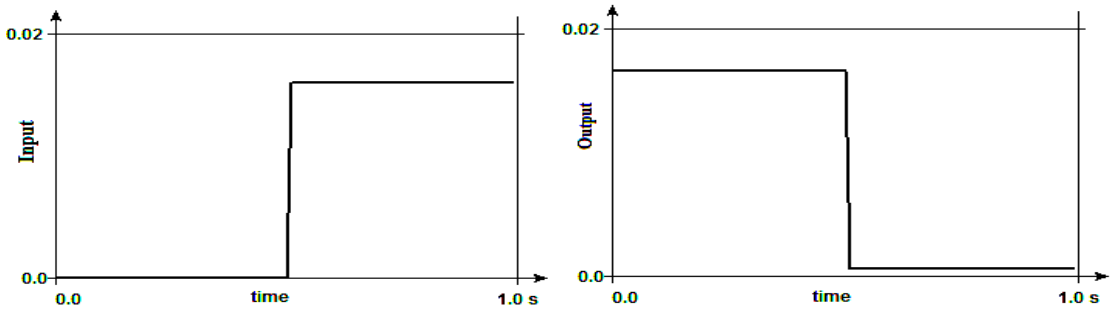
## 7.5.1 Resistance Value Variation Effects

According to the Orthodox theory, tunnel junction resistance $\left(R_j\right)$ should be greater than $\left(h/q_e^2\right) \approx 26k\Omega$, where h and $q_e$ are respectively the Planck's constant and the charge of an electron. All the circuit related resistances are nothing but junction resistances, which needs to follow the same rule.

**Table 7.1** :Randomized Values of Junction Resistance

| Rj | Randomized Rj (10% variation) |
|---|---|
| Rj1 | 145454.0Ω |
| Rj2 | 144750.0Ω |
| Rj3 | 92524.9Ω |
| Rj4 | 97602.6Ω |

The junction resistance variation effect on circuit stability is investigated for the designed buffer circuit. The resistance value has been randomized ±10%of 100kΩ fashion starting from 97.6kΩ to 145.45kΩ shown in the Table 7.1.The circuit is again simulated considering different junction resistances shown in Table 7.1.




(a) (b)

**Figure 7.5:** Simulated (a) input waveforms and (b) output waveforms of inverting buffer

The simulated results shown in Fig 7.5 (a) and (b) respectively confirm the proper circuit operation in spite of varying the tunnel resistance in a random ±10%manner over 100kΩ value.

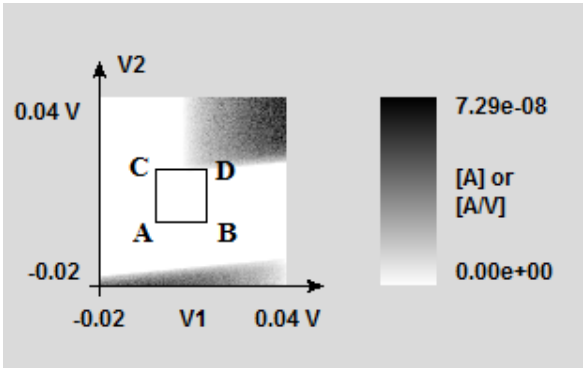
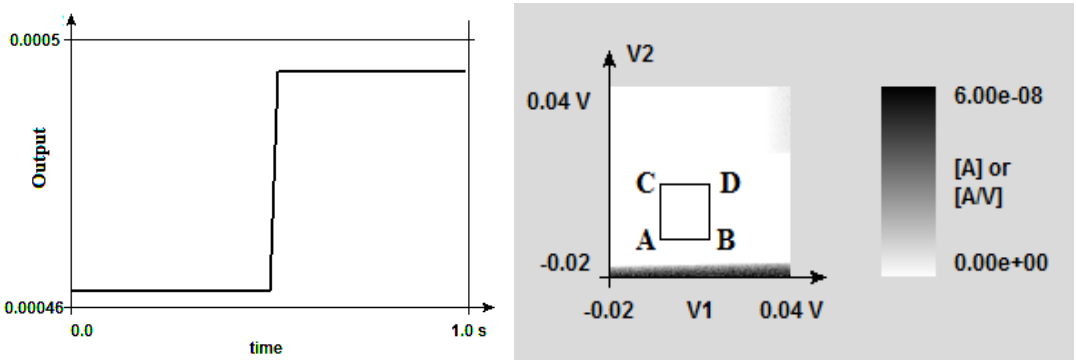



**Figure 7.6:** Stability diagram of Inverting buffer circuit with randomized resistance for V1 and V2 voltages.

In the stability plot depicted in figure 7.6 power supply,Vdd is indicated as V1 and the input voltage is denoted with V2. All the logic vectors in the stability plot marked with A(0,0),B(0,1),C(1,1),D(1,0) indicates stable operation as they are residing in the stable region (white). So the tunnel resistance variation does not affect the circuit operation as well as stability if it is retained sufficiently greater than the quantum resistance.

## 7.5.2 Capacitance value variation Effects

One of the important parts of SET based buffer design is the selection of the capacitor values. The charging energy should be larger than the thermal energy ($k_BT$) for overcoming the thermal effect, where $k_B$ is the Boltzmann's constant and T is the absolute temperature. $(q_e^2/2C_{sum})$ is the charging energy which depends upon the total capacitor values($C_{sum}$). By changing the different capacitors of the circuit the output waveform and the stability plot has been checked.




(a) (b)

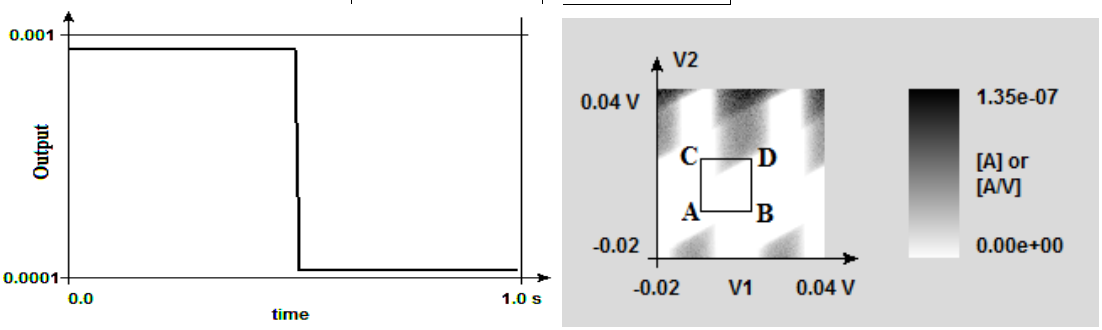
**Figure 7.7:**SET based Inverting buffer for Cg1=0.1aF (a)output waveform (b)Stability plot for V1 and V2

With the gate capacitor value changed to 0.1aF, the circuit simulation is accomplished by keeping rest of the parameters same. The result shown in figure 7.7 (a) clearly indicates a completely reversed response as it is now working as a non-inverting buffer but with very low output voltage level.

The stability plot depicted in figure 7.7 (b) indicates that the circuit stability is not as such disturbed by Cg1 variation and all the logic vectors still reside in the stable region of the plot.

**Table 7.2:** Randomized Values of Different Circuit Capacitances

| Capacitors | Values(F) |
|---|---|
| Cj1 | $0.1x10^{-18}$ |
| Cj2 | $0.5x10^{-18}$ |
| Cj3 | $0.1x10^{-18}$ |
| Cj4 | $0.5x10^{-18}$ |
| Cg1 | $5x10^{-18}$ |
| Cg2 | $4.25x10^{-18}$ |
| Co | $9x10^{-18}$ |




(a) (b)

**Figure 7.8:** Inverting Buffer circuit(a)Output waveform (b) Stability plot with Cg1=5aF

Keeping rest of the parameters same if further Cg1 value is changed to 5aF (shown in Table 7.2) the circuit behaves as an inverting buffer with low voltage levels depicted in figure 7.8 (a). The corresponding stability plot shown in figure 7.8 (b) signifies all the logic vectors are stable except D. It indicates the capacitance value variation is very crucial for buffer circuit stability.

### 7.5.3 Effect of Temperature

The temperature is another important parameter which governs the SET stability. Already it has been mentioned that to overcome the thermal effects the charging energy needs to be much greater than thermal

energy. This can be done by adjusting the capacitance values properly according to the temperature change .Otherwise the temperature will obviously hamper the circuit stability.

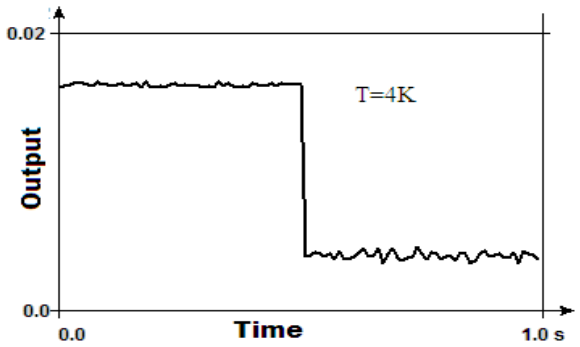
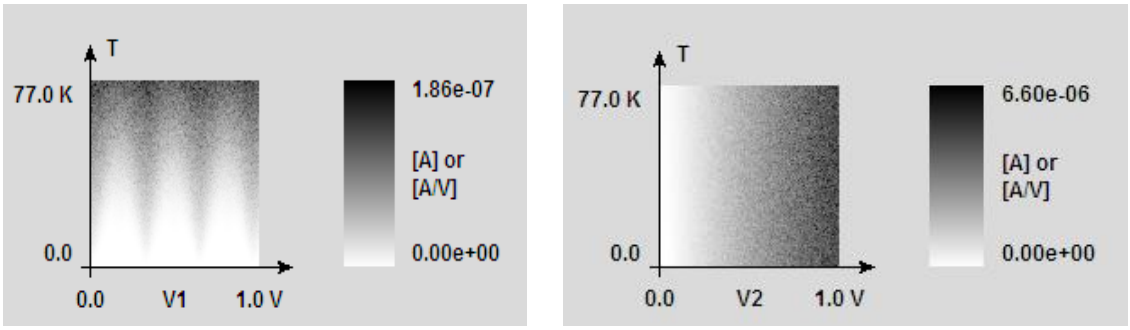



**Figure 7.9:** Inverting buffer output waveform at T=4K

The previous simulation works have been done considering the temperature to be 0K. At T=4K the simulated output of the circuit behaves according to the desired logical response shown in the figure7.9. The first stability plot shown in figure 7.10 (a) is for the power supply with the temperature. Temperature is plotted on the y-axis whereas the x-axis of the plot is utilized for the power supply voltage marked with V1.The increase in the temperature is considered from 0Kto 77K whereas the V1 range is from 0 to 1V.




(a) (b)

**Figure 7.10**: Inverting buffer circuit Stability plot for temperature values 0K to 77K(a) with V1 (b) with V2.

The circuit stability is affected highly with an increase in temperature, though for the low-temperature operation with higher values of power supply ensures stable operation. The observed maximum charge fluctuation is in the range of $1.86 \times 10^{-7}$. Figure 7.10 (b) is for the input voltage range variation from 0 to 1V with the increasing temperature from 0to 77 K. V2 indicates the input signal. From the plot, the stable operation of the circuit can be identified for the lower range of input voltage with the entire range of the temperature. But with an increase in input voltage, the stable operation of the circuit is affected by all the temperature values. Here the maximum charge fluctuation is $6.6 \times 10^{-6}$.

## 7.6 Stability Analysis of SET-CMOS hybrid Inverter Circuit

Hybrid SET-CMOS circuits [7.50]-[7.53] are often simulated in the SPICE environment by using the Macro Model or Analytical model of SETs. The SPICE software does not provide any facility to determine the stability plot of the SET-CMOS circuit through which the analysis of the stability can be accomplished. The hybrid SET-CMOS circuit stability analysis is not possible through the MC based SIMON simulator as there is no provision in SIMON to simulate the MOS. As a solution to this problem, the MOS in the hybrid circuit can be replaced with an equivalent resistance value. The circuit is constructed in such a way that it provides the proper logical output as well as due to the use of resistance in place of MOS it becomes SIMON compatible for the stability evaluation. According to the CMOS logic concept,PUN and PDN are built with the p-MOS and n-MOS respectively. Often the pseudo n-MOS are used in CMOS logic to reduce the number of p-MOS in the circuit by replacing the entire PUN with a single p-MOS. But it increases the static power dissipation of the circuit as the p-MOS always remains on. In place of that if the PUN is substituted by an equivalent resistor and the PDN by

the SET the hybrid circuit can be made well-suited for the SIMON simulation. The replacement of MOS in its linear region is possible with an equivalent 'on' resistor. For the SET-CMOS structure, the MOS is used as the PUN, so it can be replaced with the 'on'resistor ($R_{equ}$).The $R_{equ}$ is computed with [7.39], using the MOS linear region equation and also keeping in mind the Orthodox theory condition associated to SET. The range of the $R_{equ}$ is thus in between the $R_{on}$ and $R_{off}$ value according to the equation (7.3).

$$R_{on} << R_{equ} << R_{off} \tag{7.3}$$

The parameter selection is also done in accordance to support the logical operation up to 77K of temperature.

In figure 7.11 the circuit of the designed SET-CMOS inverting buffer is depicted with the $R_{equ}$ as PUN and SET as PDN .The tunnel junction parameters of the SET are Cj1 (junction 1 capacitance),Cj2 (junction 2

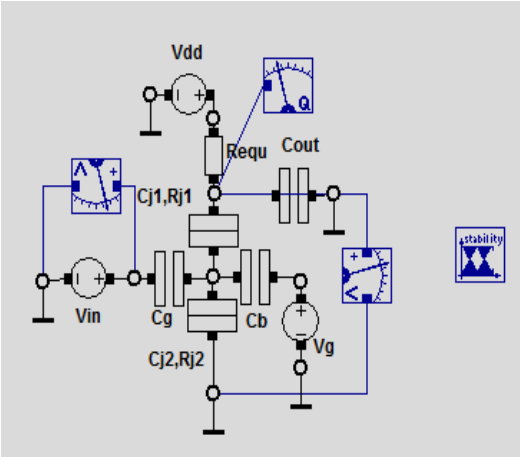



**Figure 7.11**: Hybrid SET-CMOS inverting buffer circuit for stability analysis

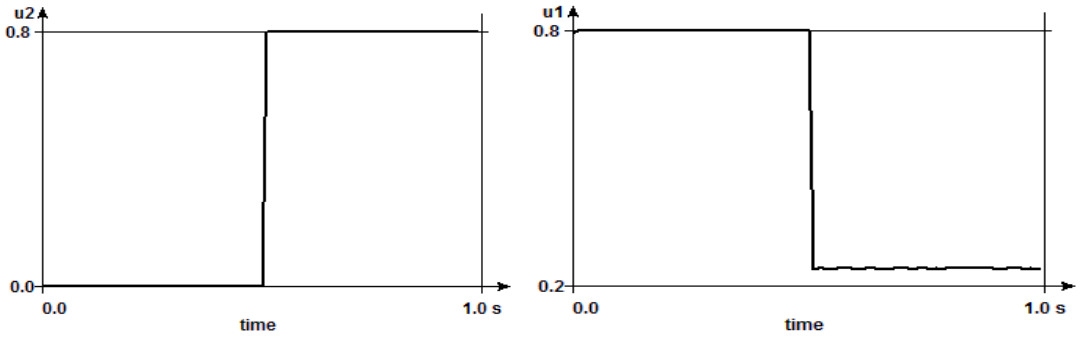
Capacitance), Rj1(junction 1 resistance), Rj2(junction 2 resistance). The front gate and the back gate capacitors are denoted with Cg and Cb respectively. The load or output capacitor is marked as Cout

**Table 7.3:** Circuit parameters of Inverting buffer with SET-CMOS for stability analysis

| Circuit Parameters | Values |
|---|---|
| Vdd | $8X10^{-1}V$ |
| Req | $9X10^{7}\Omega$ |
| Cout | $1.15X10^{-19}F$ |
| Cj1=Cj2 | $1X10^{-20}F$ |
| Rj1=Rj2 | $2.6X10^{4}\Omega$ |
| Cg | $2.9X10^{-20}F$ |
| Cb | $1.18X10^{-19}F$ |
| Vg | $5X10^{-1}V$ |

The parameter values are furnished in Table 7.3.

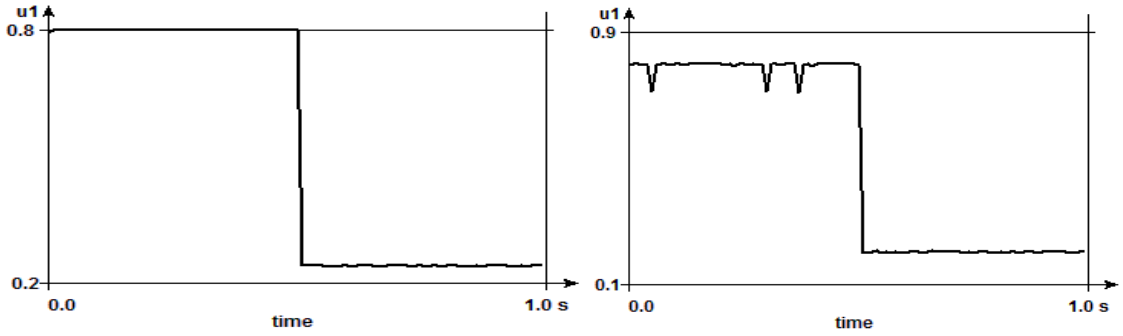
The circuit simulation results are illustrated in figure 7.12 (a), (b) for T=0K. An input signal with 0.8V as logic 'high' and 0V as logic 'low' is shown in the figure 7.12(a). The corresponding output waveform at 0K temperature is shown in the figure 7.12 (b). The nature of the output waveform justifies the logical behavior of the circuit.




(a) (b)

**Figure 7.12:** (a) Input waveform of the hybrid buffer with 0.8V as Logic 'high' and (b) the output waveform hybrid buffer at 0K .

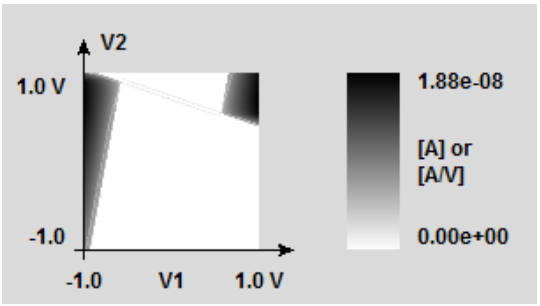
Higher temperature operation of the circuit is verified by the figure 7.13 (a) and (b).At 4K temperature, the output is similar to the waveform achieved from the 0K simulation results. The desired logical levels are maintained. Results for the circuit output at T=4K is depicted in figure 7.13 (a).



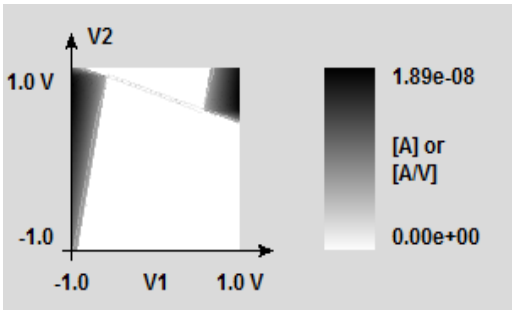

(a) (b)

**Figure 7.13**: Hybrid SET-CMOS buffer circuit output waveforms (a) T=4K and (b) T=77K

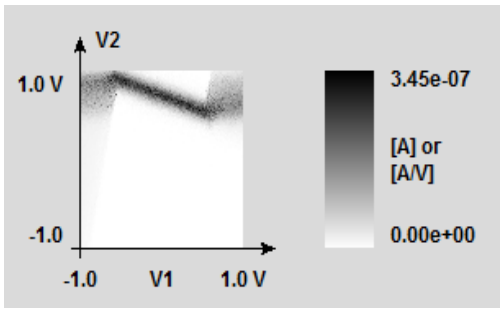
The circuit simulation result of 77K temperature is shown in figure 7.13 (b) which satisfies the required logical behavior but a little bit of fluctuation is visible in the waveform when the output is in the higher logic state. But this fluctuation is not that much to affect the logical level of the waveform. This fluctuation is mainly observable due to the higher temperature charge fluctuations.




(a)




(b)




(c)

**Figure 7.14**: Hybrid SET-CMOS buffer circuit stability (a) T=0K (b) T=4K and (c) T=77K

Finally, the stability plots of the circuit are provided in the figure 7.14. For all the three temperatures such as 0K, 4K, and 77K the circuit stability has been examined. Due to the range of the charge fluctuation in the higher temperature, the amount of tunneling current also increases. At 0K the stability diagram is plotted for the input signal with the power supply shown in figure 7.14 (a). In the plot, V1 is the power supply voltage Vdd and V2 represents the input signal, Vin. The range of V1 and V2 both are considered from -1V to 1V to clearly observe all the logical vectors. It is clear from the plot that none of the logic vectors is affected by the instability as they all reside in the white region of the diagram. The maximum range of charge fluctuation at 0K is $1.88x10^{-8}$. The next stability plot depicted in figure 7.14 (b) is for 4K temperature. Apart from a minor change in the fluctuation range ($1.89x10^{-8}$), the diagram is almost identical to the previous one i.e. for 0K. At 4K also all the logic vectors remain stable. Figure 7.14 (c) shows the diagram of stability for the temperature 77K. The logic vector (1,1) is here a little bit affected by the fluctuation. The fluctuation is $3.45X10^{-7}$ for this particular temperature.

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# Chapter 8

# CONCLUDING REMARKS AND FUTURE SCOPE



## 8.1 Concluding Remarks

This thesis covers the work in the field of SETT Based nanodevices. The application domain of the SEDs is mainly explored with the design and simulation of different analogue and digital circuits. The simulation of SED needs proper substitutes of SET in the form of equivalent models. The SET circuit equivalent model development for SPICE-based simulation is proposed in this thesis. The small-signal characteristics and the related parameter extraction are elaborated for a range of frequency. Apart from that the different logic circuit implementations with the combination of SETT and TLG is explained with their power consumption capabilities and delay time. The hybridization of SET with CMOS leads to a SET-CMOS architecture which is also used here for designing half subtractor circuit and a binary multiplier circuit. The performance metrics of the designed circuits are generally associated with the circuit reliability and stability. The SEDs being prone to the background noise faces the main challenge due to background charge fluctuation related reliability issue. In this work, the circuit reliability issues of the SE-TLG based PLA have been dealt with. The effect of the island shape has been also considered while evaluating the reliability. Mainly two methods have been discussed for reliability analysis one is the Monte Carlo Method another one is a combined approach using MC and Probability Transfer Matrix. Circuit stability is very important for the SEDs and also for the hybrid circuits. The stability analysis of the

different SE-TLG designed circuit and hybrid circuit is compiled together. The concluding remarks for the chapter wise work are illustrated below.

The second chapter demonstrates the improved version of Macro Model for SET. It successfully overcomes the drawbacks of the earlier version of the SET Macro Models. The characteristics of the drain current prove it to be suitable for the practical SET. The circuit structure with the different circuit elements is explained in details in this part. The incorporation of the two current sources which is a function of terminal voltages results into the more accurate and practical SET characteristics. The comparison with other models shows this proposed model covers the highest range of the drain current and also provides the result whose nature is in close proximity to the widely accepted MC simulator SIMON. The inverter circuit design with the model clarifies the proper functioning of the designed model. The effect of $R_G$ on the inverter output is also checked for 1GΩ to 100GΩ range which suggests that for higher value VTC of the inverter is improved. The investigation further reveals that noise margin of the inverter circuit is mostly affected by $R_G$. It has also been validated with proper plots. The multi-peak NDR circuit with the proposed model results in prominently visible peaks. With the increase in bias current and $R_G$ value magnitude of the peak increases.

The intrinsic small-signal model of SET with the calculation of different related two port parameter (Z, Y) is explained in the third chapter. Frequency dependence of the real and imaginary part of parameters shows up to 1GHz the values are almost constant with frequency but above 1GHz, most of the parameters of intrinsic-SET face fluctuation (either increase or decrease). Extracted transconductance and drain conductance for intrinsic-SET is in the μS range. Positive and negative $g_m$ is observed from the $g_m$ variation plot with $V_{ds}$ and $V_{gs}$. The input impedance of intrinsic-SET is in the mega-ohm range. At high frequency, several extrinsic elements are added to the intrinsic model. A complete model for HF is discussed with parasitic element effect on the

circuit scattering parameters. The contact pad parasitic capacitor and the series inductor, resistor mostly affects the S-parameters which are checked through the graphical representations. S-parameter based circuit stability criterion proves the SET model to be conditionally stable in presence of $C_p$. At HF with the decrease in $C_p$ the maximum unilateral transducer power gain of 55dB can be achieved.

To reduce the required numbers of junctions while designing a circuit with SETT, the TLG approach has been adopted. Together they form SE-TLG approach through which two circuits are designed and presented in the fourth chapter. The comparison between the pre-calculated thresholds with the input weighted sum results in logical output '0' or '1' in SE-TLGs. The detailed circuit components, stepwise threshold calculation, and required expressions are provided for the design of SE-TLG based majority gate with five inputs. The simulation results are presented and cross-checked with the logical outputs through the graphical behavior analysis. Another SE-TLG circuit implementation for two functional implementations with PLA is discussed in details with three-layered structure. Simulations are carried out with SIMON2.0 simulator and verified with the corresponding truth table. The power dissipation result proves the circuit to be very low power consuming in the range of few picco Watts. The delay of the designed circuits is in the range of nano Seconds and it has been analyzed with error probability variation also.

SET and CMOS hybridization results in the combined technological benefits of the SET and also CMOS. It allows higher temperature operation with a very high density of packing and high gain. Two circuit implementations are discussed with supporting simulation outputs in the fifth chapter of the thesis. Firstly the basic hybrid half subtractor circuit implementation is elaborated. Co-simulation needs proper model files of SET and CMOS both. So that the same platform can be used for their co-simulation. Here Tanner SPICE is used as the co-simulation

environment, MIB model is used for SET, and BSIM4.6.1 is used for MOSFET. The simulation time requirement is near 3.71Seconds and average power consumption is $4.45x10^{-7}$ Watts at $25^0$C temperature. The second circuit designed with this method is a two-bit binary multiplier. The waveforms generated in support proves the logical functioning. The power consumption result is $1.025x10^{-6}$ Watts for time 0 to $1x10^{-7}$ Second. A comparison between CMOS, SE-TLG, and SET-CMOS based comparator circuit design is also furnished in this section. It indicates the SE-TLG based comparator needs smallest area among the three due to use of only tunnel junctions of 27 numbers, lowest power consumption $0.225x10^{-9}$ Watts, lowest simulation time and operating temperature in the mK. Whereas CMOS based design consumes highest power consumption among three $2.21x10^{-5}$ Watts, the highest area with 20 MOSFETs, room temperature operation and highest simulation time of 4.27 Seconds. But the SET-CMOS based design provides result in the compromised manner between the CMOS and SE-TLG approach, as it consumes moderate power of $6.05x10^{-7}$Watts, moderate simulation time requirement of 3.84 Second, moderate area requirement as needs lesser number of MOSFET along with tunnel junctions and operates in room temperature.

The designed circuit reliability is highlighted in this sixth chapter with the inclusion of the reliability analysis of SE-TLG based two circuits with two different methods. The PLA circuit for the two function implementation is already discussed in chapter three with SE-TLG architecture. The same circuit's reliability has been evaluated with the MC approach for background charge variation and the island shape change. Normal and uniform two distribution functions are used for random charge generation and applied to the circuit. For normal distribution of background charge the individual as well as the entire circuit reliability is less affected with higher values of variation factor compared the uniform distribution. For disc and circular shaped island,

higher the diameter lesser is the resultant reliability. For the island diameter variation also BC modification with uniform distribution reduces the circuit reliability more than the normal one. In the second method, a SE-TLG combinational circuit reliability is checked for which the first part is related to error percentage determination of each gate with MC method and second part requires Probability Transfer Matrix. The PTM of individual gates are generated with the individual gate error probability and stepwise the overall circuit reliability is evaluated. The result of this method is also compared with the results achieved from the only MC based method. It shows close proximity with the results. Results are retrieved within 0.031Sec for the second method which is much lower compared to the first method.

Circuit stability of the SE-TLG and hybrid SET-CMOS circuits is simulated and presented in the seventh chapter. The PLA circuit with SE-TLG is simulated with SIMON and generated stability plots are used to analyze the stability of the circuit in the different input voltage and bias voltage combinations. The free energy of every possible combination of the two concerned voltages is calculated and according to the free energy minima and maxima, the points of the stability plot are color coded. The two-dimensional diagrams with the white and different level of grey shades are used to interpret the charge fluctuation in the circuit due to change in free energy. The white points indicate stable points and zero fluctuation. The shade of the grey level increases with the charge fluctuation and black point indicates the maximum amount of fluctuation. The stability plot of the designed PLA circuit shows all the logic vectors are in the stable region which ensures the stable operation of the circuit. The effect of the parametric variation on the SET inverting buffer circuit is checked. The 10% variation in the junction resistance and capacitance value is applied to the circuit for stability checking. The temperature effects on the stability are also investigated which shows along with temperature rise circuit becomes unstable. Hybrid NOT gate

stability is analyzed through the SIMON simulator by replacing the MOSFET load with equivalent resistance value.

## 8.2 Future scope

The work presented in this thesis provides a compact and accurate Macro model suitable for practical SET with two circuit implementations.

- The compatibility issues of the model can be checked with other devices such as Carbon Nanotubes FETs in near future.
- Related delay issues and their solutions can be also studied in the future.

Small-signal model of SET provided in the thesis holds the associated theoretical calculation and graphical verifications.

- With more advancement in dedicated SET fabrication procedure, the related parameters both intrinsic and extrinsic type can be determined. The temperature conditions for the small-signal model can be also checked in the future works.
- Dedicated circuit simulator development for the hybrid SET-CMOS circuits with GUI can further accelerate the circuit design aspect in the analog domain as well.
- The interconnect issues for SET-CMOS circuits need more attention in the future days from the research perspective.

Though several solutions in the field of SETT based nanodevices are proposed in this literature there is a plenty of research opportunity in this field in the near future also.