Study and Design of emerging Nanoscale MOSFETs

Thesis submitted

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CERTIFICATE FROM THE SUPERVISORS

This is to certify that the thesis entitled "Study and Design of emerging Nanoscale MOSFETs" submitted by Shri. Kalyan Biswas who got his name registered on 20.02.2017 for the award of Ph.D. (Engineering) degree of Jadavpur University is absolutely based upon his own work under the supervision of Prof. (Dr.) Chandan Kumar Sarkar & Dr. Angsuman Sarkar and that neither his thesis nor any part of the thesis has been submitted for any degree/diploma or any other academic award anywhere before.

1. **Prof. (Dr.) Chandan Kumar Sarkar** 2. **Dr. Angsuman Sarkar**

(Signature of the Supervisors and date with Office Seal)

Dedicated to My Family

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TABLE OF CONTENTS

ABSTRACT

Conventional MOSFET structures are reaching scaling limits and Short-Channel Effects (SCEs) have become most important issue for device performance. With the reduction in feature size, the density of the transistors as well as the performance in terms of speed increases, leading towards the concept of System-on-Chip (SoC) which integrates all the elements of a system (Digital, analog and RF) within the single chip. High frequency performance and power consumption of the circuits is also largely affected due to SCEs. At the nano-dimensional scale, the influence of SCEs on the characteristics of conventional MOSFETs cannot be ignored.

In current work, the problems associated with the emerging nanoscale MOSFET devices are studied and reported. In first part, the Silicon Junctionless FinFET has been considered and its analog/RF performance is analyzed. In the second part the Analog, RF and Linearity performance of InGaAs/InP hetero-junction MOSFET is studied.

Using extensive 3D TCAD simulations of n-channel Junctionless Accumulation Mode bulk FinFET, it is demonstrated that the high-k spacers improve the electrostatic integrity of FETs with sub 20 nm gate lengths. It is observed that the digital and analog performance of the device improves with high-k gate spacers. However, using high-k spacer material, the device performance is not good for RF applications. Simulation results also suggest that RF/analog performance of the device with spacer having high-k dielectric can be improved by reducing the spacer length. Effect of Fin width variation and shape of the Fin cross-sectional shape is also evaluated for the RF/analog performance of the device. It is concluded that reduction of Fin width can cause improvement in device performance in order to find their usage in analog as well as RF applications. From the analysis of Fin cross-sectional shape, an optimized value of Fin top width and Fin shape is suggested. This design is expected to provide better SCEs and reasonable maximum oscillation frequency to use the device in RF/Analog applications.

Analog, RF and Linearity performance of InGaAs/InP hetero-junction MOSFET using TCAD device simulation is also carried out. A detailed investigation of the impact of InP barrier layer thickness is reported. It is found that the RF and Analog performance of the device improves as barrier layer thickness reduces. It is understood that a trade-off is required depending upon the device application area. The impact of the channel doping and channel composition on the vital performance of the InGaAs/InP heterostructure DG MOSFET is also examined. It is found that, a trade-off in channel composition must be made to optimize the device performance and device reliability.

This research for emerging nanoscale devices such as Junctionless Accumulation Mode bulk FinFET and heterostructure MOSFET, through intensive TCAD simulations, suggests the optimal device parameters and structures. Therefore, it is established that understanding of device physics insight with design of new structures and material compositions are very crucial for enhancement of next generation device performances.

List of Figures

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Human life of modern generation is revolutionized by the advancements of Complementary Metal Oxide Semiconductor (CMOS) technology. The journey of silicon CMOS technology was started with the invention of MOSFET by Atalla and Kahng in 1960 [1.1]. In 1963, C. T. Sah and Frank Wanlass of Fairchild R & D laboratory fabricated the complementary MOS circuit from silicon [1.2]. One of the very important milestones of semiconductor integrated circuits was the famous "Moore's law". In 1965, Gordon Moore, the co-founder of Fairchild Semiconductor and Intel, predicted that the number of components per chip would double every 12 months [1.3]. In a later stage, the time to double the components was modified to 24 months. Since then, performance of MOSFET has been improved continuously at a dramatic rate via gate length scaling. In order to serve the next generation high performance requirements with lower operating power, unrelenting scaling of CMOS technology has now reached to the atomic scale dimensions. Conventional MOSFET scaling not only involves the reduction of device size but also requires the reduction in the transistor supply voltage (V_{DD}). With the reduction of V_{DD}, the threshold voltage (V_{th}) must be scaled down simultaneously in order to attain reasonable ON-state current, reduce delay and to maintain sufficient gate overdrive voltage. However, the reduction in threshold voltage increases the sub-threshold leakage and adds to standby power.

1.2 PROBLEMS ASSOCIATED WITH NANOSCALE MOSFET SCALING

This downscaling of the device dimension is essential to integrate the higher number of devices in Integrated Circuits (ICs). IC industry is following the "Moore's Law" successfully till now. Today, semiconductor industry also follows the roadmap given by International Technology Roadmap for Semiconductor (ITRS)[1.4] which predicts the future device dimension and number of transistors in an integrated circuit based on the Moore's law.

As a consequence of the Moore's law, every year channel length of the MOSFET is reducing, causing Short Channel Effect (SCEs) [1.5]. SCEs are affecting power consumption of the circuits. Transistor scaling target has been made reachable because of the advanced lithographic capability to make shorter/thinner channel. In early stage, scaling was possible with conventional structures and materials technology, but it is understood that conventional scaling technology cannot continue forever. Therefore, investigation of non-classical device structures became necessary.

As the dimensions of transistors are reduced, the control of the gate electrode on the flow of current in the channel region is reduced because of the close propinquity between the "source" and the "drain". The main problem related to the short channel MOSFET is reduced gate to channel coupling. Reduced gate control decreases the transconductance of the device. Transconductance of the device is very important for its analog application. For a short channel device along with the transconductance, the drain induced barrier lowering, ballistic transports are the Short Channel Effects (SCEs) which could affect the device performance. The solution to all the problems resides in increased electric field coupling between gate and channel and reduced electric field coupling between source/drain and channel.

Normally, six different short-channel effects can be distinguished such as (i) "Drain-Induced Barrier Lowering (DIBL)" and "Punch through" (ii) "Surface scattering" (iii) "Velocity Saturation" (iv) "Impact Ionization" (v) "Hot Electron Effect" and (vi) "Threshold voltage roll-off".

As the SCEs set hurdles to device operation and degrade device performance, these effects should be removed or minimized, so that a device with shorter physical channel length can preserve the required device characteristics. Researchers tried to overcome these problems by decreasing the gate oxide thickness and the source/drain junction depth while decreasing the gate length in conventional bulk MOSFETs. But these scaling reached the physical limit of dimension. As a remedy, gate dielectric

materials with higher permittivity were used. Use of these high-k materials as gate oxide allowed achieving smaller equivalent oxide thickness with thicker physical dimension. But shrinking of MOSFET to the sub 10 nm scale is challenging and new technologies were necessary. As per ITRS forecasts and published literatures, it is understood that main research is going on in two different directions: possible modification of the planar architecture and use of non-planner 3D structure [1.6] to push for its physical limits, or new way of making transistors, such as devices based on III-V group materials, use nanomaterials and nanotechnologies like silicon nanowires, carbon nanotubes or graphene, single electrons transistors, and also some other emerging devices such as quantum cellular automata and spin-based electronics [1.7].

1.3 STRATEGIES TO SURMOUNT SCEs

Different strategies have been considered to surmount SCEs such as (i) high-k gate metal (ii) "Silicon on Insulator (SOI)" structure (iii) "Strained Silicon" technique (iv) Multi gate structures etc. Nowadays multi-gate structures are the front runners as future technology of CMOS devices. The triple-gate MOSFET or FinFET is a thin-film, narrow silicon channel with a gate on three of its sides. Because of its improved performance and ease of fabrication, FinFET is already adopted by the semiconductor industry. Intel has started high volume production using FinFET structure in production line [1.8] since 2011. This 3D technology made it possible to pursue Moore's Law and also helped to satisfy the need of advancement in technology. With the introduction of 2nd generation 3D tri-gate transistors with metal gate in 14 nm technology node, it is possible to support high performance device with low power, high density and lower cost per transistor to manufacture a wide range of products. The main advantage of such devices is the superior "Short Channel Effects (SCEs)". Since the channel (body) is electro statically controlled by the gate from multiple sides, its performance is better than that in the conventional transistor structure. It also reduces the unwanted leakage current and allows making smaller devices with reduced cost. Lower output conductance, i.e., smaller dI_d/dV_{ds} (I_d stands for drain current and

V_{ds} stands for drain to source voltage) in the current saturation region is also achieved due to improved gate control which in turns supports greater voltage gain. This improved voltage gain is beneficial to analog circuits as well as to the noise tolerance of digital circuits. Another advantage in terms of higher ON current in multi-gate structures provides faster switching speed in circuit. These advantages of multi-gate structures are established and revealed by many researchers [1.9-1.11].The device performance can be enhanced by the use of strained silicon, a metal gate and high-k material as gate dielectrics [1.12]. However, these inversion modes devices suffer from a fabrication challenge as for short channel devices it needs the sharp control of doping profile and less variability in dopant distribution. To avoid such fabrication issues and overcome the process challenges, Junctionless MOSFETs were introduced. In Junctionless transistor, same type of semiconductor doping is used throughout the whole silicon (from source to drain), which acts like a resistor. Greater reliability of Junctionless MOSFET and its immunity to SCEs in comparison to inversion-mode MOSFETs is proved theoretically and demonstrated experimentally [1.13-1.14].

To attain high channel currents (per unit device width W) requires high electron concentration in the channel as well as high electron drift velocity. These high electron concentration and higher mobility help to achieve better transconductance and lower source drain parasitic resistances. Therefore, integration of high mobility channels in CMOS technology became a topic of intense research [1.15-1.16]. Most III-V group materials of periodic table (compound materials like InGaAs, GaAs, InAs, and InSb) can present exceptionally high electron mobility. InGaAs based channel materials have an added advantage which allows tuning its band gap by changing the mole fraction of the composition. When III-V group materials are suitable for n-channel MOSFET operations, *Ge*, a group IV material and having relatively higher hole mobility is ideal for p-channel MOSFET. However, mobility in these channel materials is inversely proportional to bandgap (E_G). To achieve higher mobility lower E_G is desirable but that in turn increases the OFF-state leakage current due to

tunnelling effect from drain to bulk or drain to source. Smaller E_G also degrades scalability of the device and worsens SCEs. Therefore proper study and careful analysis is very much important to integrate these high mobility channel materials and improve performance for the emerging Nanoscale devices.

1.4 NEED OF HIGH FREQUENCY PERFORMANCE ANALYSIS

In the area of communication, a revolution in technology is observed in recent years. Starting from the 2G, now the mobile communication is moving towards 5G. In the domain of wireless communication, there is wide need of high power amplifier circuits which are capable of handling high power and high frequency. High frequency is required to serve the present day communication band and the high power is required to provide service in a wide area. The present day power devices are capable of handling the large power but these devices are having frequency limitation. The electronic circuits required supporting front end as well as the back end for these new technologies and other applications need to have a compatibility with this high frequency range. But the parasitic effects and SCEs which are very common for the small dimension MOSFET devices, it is a big hurdle. So it is very much necessary to explore the performance of the emerging CMOS devices for its applicability in high frequency RF domain [1.17]. To overcome all these challenges, researchers need to find a device which can perform perfectly in a smaller dimension with a lower supply voltage. The features of these emerging CMOS devices will be helpful in designing the circuit in a new way. From the perspective of wide band application, the MOSFET performance in the RF domain is limited by the parasitic capacitance of the MOSFET. A new age device with high frequency range will be useful in designing the circuits for high frequency applications. Presence of high-k dielectric reduces the parasitic capacitance, which increase the bandwidth of the device. The gate lengths are kept smaller than the effective channel length, known as underlap length. The underlap length also plays a vital role in enhancement of device bandwidth. The enhanced bandwidth makes the device an ideal choice for high frequency application.

As the feature size within an integrated circuit decrease, the density of the transistors as well as the performance in terms of speed increases, leading towards the concept of "System-on-Chip (SoC)" where digital, analog, RF and mixed signal communication circuits are integrated with the memory circuits. There are many challenges in analog and RF circuits with a digital CMOS technology. For "System on Chip (SoC"), optimization of the devices becomes more challenging. So it is required to investigate the device structure to enhance the device performance for digital and analog/RF circuit applications.

1.5 MOTIVATION FOR PRESENT RESEARCH WORK

In order to continue device scaling without incurring OFF state leakage current and at the same time achieving improved performance, the planar bulk MOSFET structure should be altered. New device structures to provide better gate controllability and suppressed short-channel effects (SCEs) are necessary. Researchers are trying to solve these above mentioned problems mainly in two ways: (i) Multi-gate structures for better gate controllability, higher ON current at the constant over-drive voltage and (ii) Utilization of channel materials with higher carrier mobility. In this work, both the strategies have been employed to reduce SCEs and better analog/RF performance.

It is observed that there are many advantages of Junctionless MOSFETs over a conventional device such as better protection to Short Channel Effects (SCEs), superior scalability, enhanced drain-induced barrier lowering (DIBL) etc. FinFETs have already been emerged as the most chosen solution at or below the 22-nm technology node because of its reduced Short Channel Effects (SCEs) and better gate controllability in comparison to planar MOSFETs. They also provide greater ON/OFF current ratio and exhibit higher drive current per unit area in comparison to planar devices. Fabrication process of FinFET device structure is reasonably easy and compatible to conventional CMOS technology. In order to utilize the advantages of junctionless transistor technology and FinFET structures,

combination of both the technology is considered. In order to obtain suitable threshold voltage (V_{th}), low SS and higher I_{ON}/I_{OFF}, lower channel doping is preferred for junctionless MOSFET. But lower channel doping increases unwanted source/drain series resistances. As a solution, an additional doping density in source and drain regions are employed in junctionless FinFETs. These devices with higher doping concentrations in source and drain regions than the channel regions works in accumulation mode of operation and known as Junctionless Accumulation Mode FinFETs [1.18, 1.19]. FinFET fabricated on bulk silicon has advantages in terms of better heat dissipation capability, less defect density and lower wafer cost in comparison to SOI FinFETs. Bulk-FinFETs also helps to overcome "floating body effect". Therefore, Junctionless Accumulation Mode bulk FinFET became the topic of current day research and development [1.18, 1.19].

To permit higher drive current and transconductance as compared to Si-based counterpart, high mobility channel materials are considered [1.20]. InGaAs based channel materials have added advantages in terms of tuneable bandgap by varying the Indium mole fraction of the compound semiconductor [1.21]. Higher electron mobility and better performance is also possible using suitable barrier layer [1.22]. Therefore, study and performance investigation of InGaAs/InP material based MOSFETs varying barrier layer properties and channel composition is vital.

There are many challenges in analog and RF circuits of a digital CMOS technology when used in a "System of Chip (SoC)". For "System on Chip (SoC)", optimization of the devices becomes more challenging. So it is required to investigate the device structure to enhance the device performance for digital and analog/RF circuit applications. Based on the literature review, the proposed work is focussed on study and design of emerging nanoscale MOSFETs for analog and RF applications. Different SCEs such as DIBL, Subthreshold Slope (SS), digital performance parameters such as I_{ON}/I_{OFF}, Analog performance parameters such as Transconductance (g_m), g_m/I_d, RF performance parameters like Cut-off

frequency (f_T) and Maximum frequency of oscillation (f_{max}) etc of the devices under study are investigated in detail.

1.6 JUSTIFICATION OF THE WORK

To overcome SCEs in conventional nanoscale MOSFETs, many new technologies have been considered and studied. It is already proved that FinFET structures have advantages in terms of reduced Short Channel Effects (SCEs) and better gate controllability in comparison to planar MOSFETs. They also provide greater ON/OFF current ratio and show higher drive current per unit area in comparison to their planner counterparts. On the other hand, Junctionless MOSFET technology having same doping type in source, channel and drain region have stronger immunity against SCEs in comparison to inversion mode devices and also posses' advantages from the fabrication point of view. In junctionless FinFET structures with additional source/drain doping was proposed and demonstrated by the researchers [1.18]. Studies on SCEs and Digital performance analysis of Junctionless Accumulation mode bulk FinFET is available in literature [1.19]. But exploration of the impact of spacer on Analog/RF performance for Junctionless accumulation mode FinFET has not been reported. As the Fin dimensions and Fin cross-sectional shape of a FinFET is very important parameter to define its performance, study on these crucial parameters for Junctionless accumulation mode FinFET is important and worthwhile. Although, few investigation results on Fin dimensional effect on conventional FinFETs are already reported but those are concentrating mainly on SCEs, digital performance analysis, effect of Fin cross-sectional shape on threshold voltage variation and leakage current variations etc. Detailed RF and analog performance analysis for the Junctionless Accumulation Mode bulk FinFET has not been performed earlier to the best of my knowledge. Therefore, a scope exists for investigation of device performance variation with spacer materials, spacer length, Fin dimensions, and Fin cross-section shape for its application in RF/Analog circuits and is performed in details in this work.

On the other hand, it is proved that III-V based materials are capable of providing higher drive current and transconductance as compared to their Si-based counterpart. Indium-Gallium-Arsenide (InGaAs) has emerged as a potential high mobility channel material for future n-MOSFETs owing largely to its improved electron mobility. Moreover, it is shown that InGaAs channels have the ability to achieve a wide range of bandgap and effective mass by suitably varying the percentage of Indium composition (x) in $In_xGa_{1-x}As$ materials [1.21]. A barrier layer in an InGaAs MOSFET is known to further improve the electron mobility and an important parameter to control the device performance [1.22]. Investigation of analog/RF and linearity performance for different barrier layer thickness and channel composition is not done earlier. Therefore, effect of barrier layer thickness and variations of concentrations of Indium mole fraction in the channel material on RF/Analog performance are important parameters to study and carried out in detail in the current work.

1.7 RESEARCH PROBLEM STATEMENT

In this work, design, analysis and performance investigation of emerging Nanoscale MOSFETs have been carried out. RF/Analog performance parameters of emerging MOSFET structures have been examined in order to demonstrate its superiority over conventional bulk MOSFET structures for low power mixed signal "System-on-Chip (SoC)" applications. In order to utilize the advantages of Junctionless Transistor technology and FinFET structures, combination of both the technology has been proposed and analyzed. Different device parameters such as channel material, spacer material, channel dimension, doping levels etc. have been considered in order to achieve significant performance improvement. Moreover, an optimal device configuration has been proposed and analyzed to act as a useful guideline for improved DC and Analog/RF performance.

This is accomplished in terms of the following intermediate stages:

1. Literature review to study and survey the recent developments and trends in the Nanoscale MOSFET device technologies in VLSI and microelectronic industries
2. Device simulation using TCAD device simulation software.
3. Model calibration with published experimental results.
4. Analysis and comparison of the device performance depending on its different geometrical parameters, for Analog/RF applications.
5. Performance parameter investigation and linearity study of III-V heterostructure MOSFET for usage in Mixed Signal SoC applications.
6. Improvement in performance and device parameter optimization by performance investigation using different Channel materials, device dimensions, doping levels etc.
7. Circuit performance analysis of the device by using it in simple circuits such as on resistive load inverter, cascode amplifier etc.

1.8 ORGANIZATION OF THE THESIS

This work presents the study and design of emerging nanoscale devices for the different types of application. Work mainly focus on analysis of the device performance depending on its different geometrical parameters, for Analog/RF application of device. Different Channel materials, spacer materials, doping levels etc. are considered for performance improvement. The work is carried out in TCAD device simulator [1.23]. The thesis is having eight chapters. The organization of the thesis can be described in the following manner:

Chapter 1: It is an introductory chapter. It provides the brief idea about the research topic and also discusses the historical perspective. Motivation behind the current research and a justification for that is also

provided. Based on the literature survey, a research problem is framed and research problem statements are mentioned.

Chapter 2: It starts with the background of MOSFET and its journey towards modern era. Detailed review on challenges associated with scaling of nanoscale devices is reported in this chapter. It presents revolution of MOSFET devices for digital, analog and RF applications. It also highlights different existing device technologies that are currently used to implement these circuits and their limitations. This chapter also provides the review of possible devices and their limitations as the solution of the foresaid problems.

Chapter 3: This chapter explains the simulation and performance analysis of Bulk FinFET in the Junctionless Accumulation-Mode (JAM). Different electrical parameters such as SS, DIBL, Threshold voltage roll-off, I_{ON}/I_{OFF} ration etc. along with its Analog/RF performance are simulated and analysed for the device with different gate spacer's materials and different spacer lengths. A resistive load inverter has also been examined in order to assess the effect of the spacer material and length through the transient response.

Chapter 4: Effect of Channel dimensions for Junctionless accumulation mode device is presented in this chapter. Performance of the Junctionless Accumulation Mode FinFET is analyzed by employing the variation of Fin width so that it can be used as a high-efficiency radio-frequency integrated circuit design.

Chapter 5: This chapter describes the impact of various Fin cross-sectional shapes on Junctionless accumulation mode bulk FinFET with narrow Fin and short channel length. Different important device performance parameters are evaluated for different Fin shapes and analyzed. An optimal Fin structure for the Junctionless bulk FinFET is also obtained to have better SCEs and reasonable Analog/RF applications.

Chapter 6: In this chapter, analysis of the Analog, RF and Linearity performance of InP/InGaAs hetero-junction MOSFET using TCAD device simulation is reported. A detailed investigation of the impact of barrier layer thickness on different Analog, RF and Linearity performance of an InGaAs/InP hetero structure DG MOSFET is carried out. A design guideline in terms of barrier layer thickness is also provided.

Chapter 7: Detailed numerical analysis is performed to study and evaluate the effect of channel doping and impact of Indium concentrations of the InGaAs channel on different device performance of InGaAs/InP double gate (DG) MOSFET. A cascode amplifier is also designed using the device under study and its voltage transfer characteristics and differential gain is observed to estimate the device performance in circuits.

Chapter 8: This chapter summarizes the overall thesis in a compact form with a discussion on further scope of work in parallel areas.

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CHAPTER 2

REVIEW STUDY ON CHALLENGES ASSOCIATED WITH SCALING OF NANOSCALE DEVICES

2.1 INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is one of the most significant inventions of twentieth century. The concept of field effect conductivity modulation was first proposed by J. E. Lilienfeld in 1928. [2.1]. Though he was unable to fabricate the working device, his idea of three electrode structure later acknowledged as Field Effect Transistor. P-n junction based transistor was invented by William Shockley, John Bardeen, and Walter Brattain in 1947 whereas, in 1958, the Si MOSFET era started with the discovery of silicon dioxide (SiO_2) passivation layer for the Si by Atalla. But first breakthrough came when scientists from Bell Labs M. M. (John) Atalla and Dawon Kahng fabricated and demonstrated the first working Field Effect Transistors successfully in 1959 [2.2]. The complementary MOS (CMOS) circuit on silicon was invented by C. T. Sah and Frank Wanlass of Fairchild R & D laboratory [2.3]. They demonstrated that the complementary circuit combining n-channel and p-channel MOSFETs do not experience power losses in standby state. This revolutionary concept is known as CMOS technology and is the backbone of today's semiconductor industry. After this invention, MOSFET performance enhanced drastically with gate length scaling. The basic structure of a conventional MOSFET is depicted in Fig.2.1.

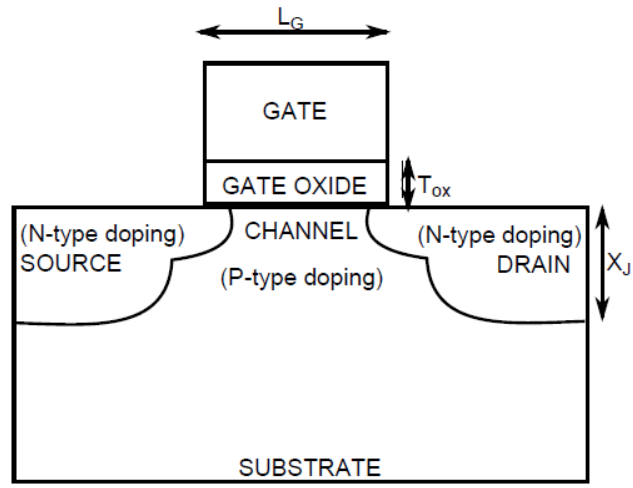

Fig.2.1: Schematic diagram of the Conventional Bulk MOSFET Structure

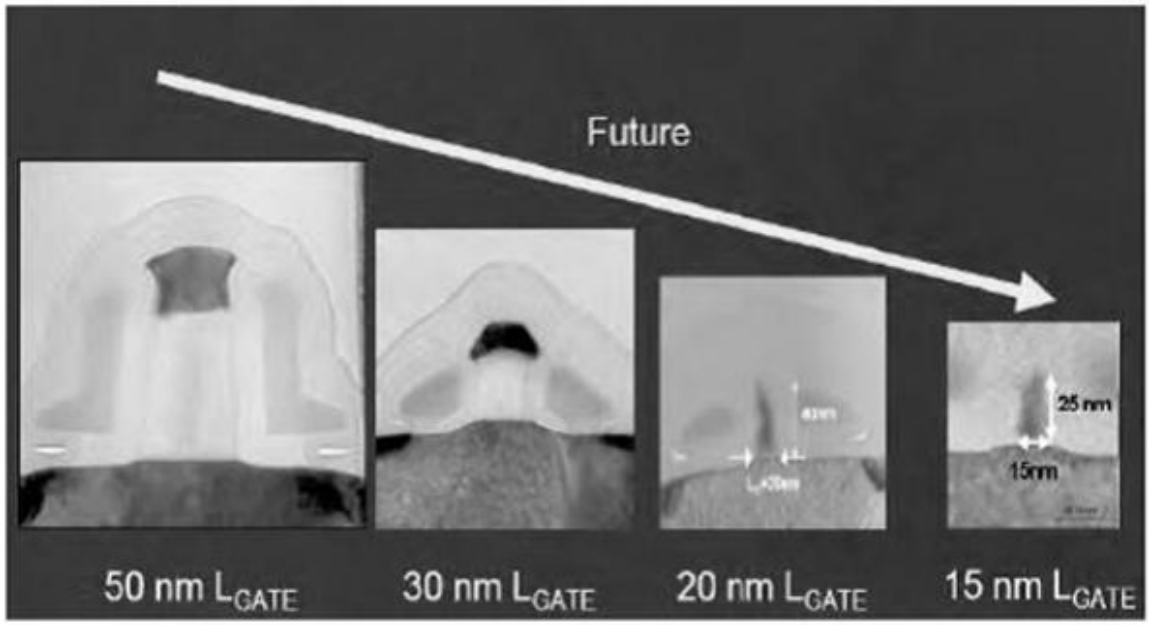

Fig.2.2: Scaling the bulk MOSFET in accordance with Moore's Law (source: Intel).

2.2 SCALING TRENDS AND CHALLENGES OF NANOSCALE MOSFETs

Driven by the Moore's Law [2.4] the size of MOSFET is reducing by a factor of two in every 18 months (Fig.2.2), without changing the basic structure as shown in Fig.2.1. This basic structure of MOSFETs continued its successful geometric scaling without any specific changes, following the ideal scaling principles "constant-field scaling." However, as the supply voltage (V_{dd}) reaches 1V, the "constant field scaling" deviates due to difficulty in reducing threshold voltage (V_{TH}). Further reduction in threshold voltage causes increased leakage current which in turn prevent supply voltage scaling. Also, high electric field inside the transistor decreases the device reliability. At the same time, high channel doping creates problems such as increased "Band-to-Band Tunnelling" (BTBT), degradation in carrier mobility, "Gate-Induced Drain Leakage" (GIDL) and fluctuations in threshold voltage due to random dopant variation. These are known as "Short Channel Effects" (SCEs) and these effects increase with decrease in device dimensions. SCEs affect the performance of the circuit designed with the low

dimensional MOSFETs. Some of the problems faced are difficulty in increasing ON current, increased leakage currents, discrepancy in parameters, low yield and reliability and manufacturing cost increase etc. High frequency performance and power consumption of the circuits is also largely affected due to SCEs. At the nano-dimensional scale, the influence of SCEs on the characteristics of conventional MOSFETs cannot be ignored [2.5-2.6].

2.2.1 ISSUES OF NANOSCALE DEVICES IN CHANNEL

The main issues due to the scalling of device dimension occur in the channel of MOSFET.

2.2.1.1 SUB-THRESHOLD SLOPE

Weak inversion conduction current flowing between source and drain through the channel is known as "Sub-Threshold Leakage Current" (I_{subth}). Partial derivatives of this leakage current with gate voltage (V_{gs}) define a parameter called sub-threshold slope (SS).

$$SS = \frac{\partial(\log_{10} I_{subth})}{\partial V_{gs}} \qquad (2.1)$$

This SS is an important parameter for the device as it shows abrupt turn off of transistor with decreasing V_{gs}. Smaller value of SS is desirable and ideal value of SS is 60 mV/dec. SS can be improved by lower oxide thickness or a lower substrate doping concentration. In SOI MOSFET, Subthreshold slope performance is better than bulk MOSFETs [2.7].

2.2.1.2 DIBL AND THRESHOLD VOLTAGE ROLL-OFF

Device speed and sub-threshold leakage current is controlled by Threshold voltage and the variation in threshold needs to be minimized. Variation of Threshold voltage (V_{th}) with different device parameters is known as roll-off and it is affected by "Drain Induced Barrier Lowering" (DIBL) also. In devices with smaller channel lengths, smaller potential barrier between source and drain causes both these phenomena. Ways to

address DIBL [2.8] includes (i) increasing the gate control (ii) increasing the substrate doping and (iii) using different material with lower dielectric constant. Decreasing oxide thickness, gate control can be increased but that increase the direct tunnelling current through gate oxide. To prevent these phenomena one approach is to silicidation of S/D junction and use of lightly doped channel [2.9]. A schematic diagram of Lightly Doped Drain (LDD) MOSFET is shown in fig. 2.3.

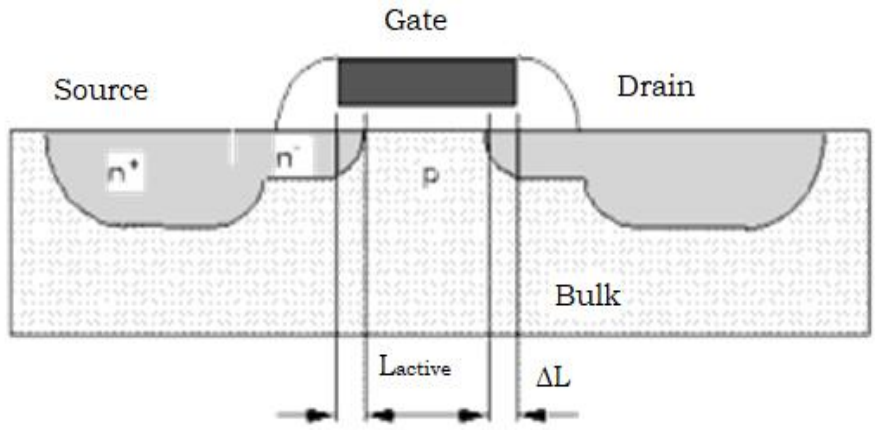

Fig.2.3: Schematic diagram of LDD MOSFET [2.9]

2.2.1.3 VELOCITY SATURATION

Since geometrical scaling is more than the supply voltage scaling, the electric fields inside the MOSFETs continue increasing in short channel devices. Though the drift velocity of carriers increase with increasing longitudinal electric field, but that is true for low field ($<10^3$V/cm). At higher electric field when the carriers reach its maximum velocity value, the carrier mobility does not increase and is known as "velocity saturation". Plot of carrier velocity with applied electric field becomes a straight line as shown in Fig. 2.4. Since current is the rate of flow of electrons, it also attains a saturated value once the carrier velocity saturates. Therefore velocity saturation effect creates the I_{ds}(sat) lower than ideally expected and also results a smaller than predicted V_{ds}(sat).

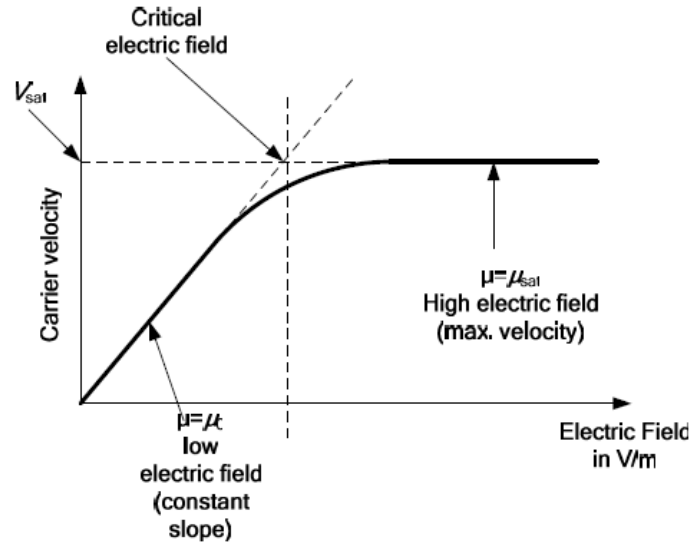

Fig.2.4: Variation of Carrier velocity with electric field

2.2.1.4 HOT CARRIER EFFECTS

The longitudinal electric field in the channel region reaches the peak value at the drain-to-channel junction. Because of the smaller channel length, carriers crossing the pinch-off point to the drain travel at their maximum saturated speed, and gain their maximum kinetic energy. The carriers known as "*hot carriers*" can attain such high kinetic energy to overcome barriers because of the amplified scattering rate at the high electric fields they experience. They might enter the regions such as gate oxide, gate or substrate region. These hot carrier effects degrades the device reliability and alter its performance. For example, electrons trapped in the oxide changes the threshold voltage V_T of the device. This leads to a long term reliability problem. In impact ionization, carriers that get accelerated in channel collide with Si lattice atoms and create dislodged electron-hole pairs. Some of these e-h pairs having enough energy also rise above the potential barrier which exists in between the silicon substrate and gate oxide. Fig. 2.5 shows the different "Hot Carriers" in gate region.

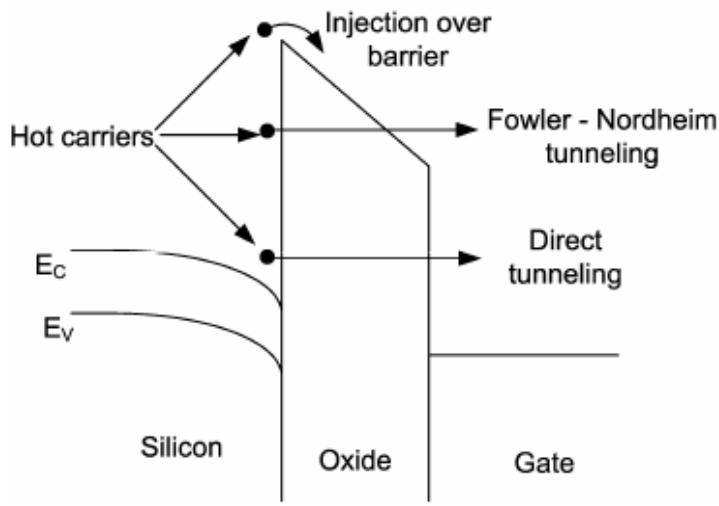

Fig.2.5: Different types of carrier injection in Gate

2.2.1.5 DIRECT SOURCE TO DRAIN TUNNELLING

If in a device, length of channel becomes very small such that electrons from source can pass through the barrier to the drain without applying any gate voltage ("tunnelling effect"), then the MOSFET cannot be used as a switch. This phenomenon defines the fundamental scaling limit of MOSFETs.

2.2.2 ISSUES IN THE GATE OF MOSFET

Due to the continuous device scaling, reduction of gate oxide thickness became necessary so that gate controllability can be maintained. But reduced oxide thickness increase the tunnelling probability and cause an increase in the gate oxide leakage current. This gate leakage current increase standby power dissipation and limit the proper device operation also [2.6]. To overcome this problem, SiO_2 may be replaced by the materials having higher permittivity (*k-value*). The Equivalent Oxide Thickness (EOT) can be calculated quickly using equation (2.2) to compare the effect of different dielectric materials with SiO2 which is standard and used as gate dielectrics from the beginning of MOSFET era. "High-k" materials enhance the "Equivalent Oxide Thickness" (EOT) and reduce gate leakage current.

Recently Hafnium oxide as gate dielectric materials is introduced to improve device performance.

$$EOT = t_{high-k}\left(\frac{k_{SiO_2}}{k_{high-k}}\right) \qquad (2.2)$$

"Poly-Si" has been generally used as preferred material for "Gate" because of certain advantages such as easy processing steps, lower parasitic resistance, and work function controllability by doping concentration control etc. However, poly-Si gate electrode has certain resistance though it may be heavily doped. This resistance introduce certain RC time delay which cannot be ignored. At the same time, if doping concentration of the poly-Si be insufficient, that creates a portion of the poly-Si at the poly-Si/SiO_2 interface depleted of carriers at higher gate bias. This "Poly depletion Effect" alters the EOT and creates problem in drive capability of the transistor. To overcome this difficulty, "Metal Gate" with appropriate work function (W_F) is used in recent nanoscale devices.

2.2.3 CHALLENGES IN DRAIN/SOURCE REGION

When the device size becomes smaller, the impact of parasitic resistance on "ON-Current" (I_{ON}) increases drastically. Therefore, it is important to control total parasitic resistance properly in order to achieve additional performance improvement. Sallower S/D junction depth obtained by increasing source drain doping is desirable to suppress SCEs but that increase the sheet resistance. However, ultra-shallow S/D junction depth increase probability of Band to band tunnelling (BTBT) and is difficult to form.

For high performance CMOS circuits, parasitic capacitance is also an important factor. Lower capacitance is desirable for digital applications with higher drive current. Thus, the performance improvement with geometry scaling has been achieved because the gate capacitance decreases with the gate length reduction in smaller MOSFETs. Total gate capacitance consisting of both intrinsic part and parasitic component should be small for better performance. However, for the nanoscale MOSFETs, due to higher parasitic

capacitance, gate capacitance does not decrease with reduced gate length. Therefore, proper technique for reduction of parasitic capacitance is very important to achieve performance improvement in emerging nanoscale devices.

2.2.4 SUBSTRATE RELATED ISSUES

Parasitic reversed-bias PN diodes formed between the substrate and the diffusion region of the transistor generates reverse "leakage current". This reverse biased "junction leakage current" consumes power from the power supply. When both n regions and p regions are heavily doped, there will also be increased "junction leakage current" due to band-to-band tunnelling (BTBT). Different leakage mechanism of MOSFET is shown in Fig. 2.6.

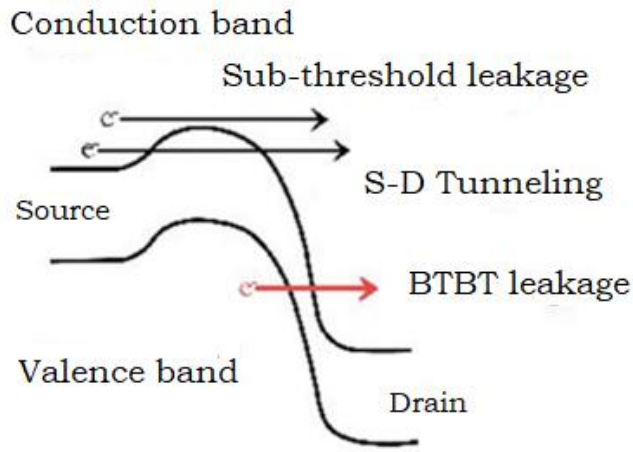

Fig. 2.6: Different leakage mechanism of MOSFET [2.6]

"Gate-Induced Drain Leakage (GIDL)" is the phenomenon caused by high electric field in the drain junction of MOS transistors. For a high drain bias and a low gate bias, in a nanoscale device, the electric field in the gate/drain overlap region become very high. Because of this high field effect in narrower depletion region formed by reverse bias between drain and channel, a current flows through drain to substrate junction because of "Band to Band Tunnelling". GIDL current increases because of higher supply voltage, thinner gate oxide, and high mobility channel materials etc.

2.3 EVOLUTION OF MOSFET

For decades, traditional scaling technique based on sinking its physical dimensions has largely dominated the development path of MOSFETs. But this traditional scaling technique is not valid for emerging devices of nanoscale. As device scaling enter beyond the 22 nm node, various significant changes in terms of device architecture and materials in the traditional MOSFET would be required for competent operation of the device and to extend Moore's law. In order to surmount SCEs researchers are employing different strategies for Nanoscale devices. The main approaches are (i) by employing different structures such as multigate MOSFETs (ii) advanced device physics approach such as Junctionless MOSFET, Tunnel FET and (iii) different channel materials having higher carrier mobility such as III-V based materials, strained silicon, Carbon Nanotubes, Graphene etc. for continuing the progress in nanoscale.

2.3.1 SILICON-ON-INSULATOR (SOI) TECHNOLOGIES

For many years' silicon-on-Insulator or SOI technologies are considered as attractive alternative technologies for device performance improvement and prevent SCEs. In SOI technology, a buried oxide layer as shown in Fig. 2.7 is used underneath the active silicon layer [2.10]. A thin uniform layer of silicon having low interface states density should be fabricated as active layer on top of SiO_2 layer. Parasitic capacitances are reduced and faster switching is obtained because of the presence of this buried oxide. SOI technology helps to avoid the connection between device and substrate which in turn helps to reduce power consumption. Some other advantages of SOI technology includes better control of SCEs, better transconductance, reduction in area consumptions etc. As this technology does not need any body doping, related issues like Random Dopant Fluctuations (RDF) and Threshold voltage variations may be avoided. However, SOI wafer cost is higher as the extra processing steps required for it and another drawback is the heat dissipation is not good. As the thermal conductivity of SiO_2 is much lower than silicon, Self-heating effect is

significant. SOI devices may be operated in (i) Fully depleted mode and (ii) partially depleted mode having relative merits and demerits. Thickness of the silicon film on top of insulator and body doping determines whether the device is Fully depleted or Partially depleted.

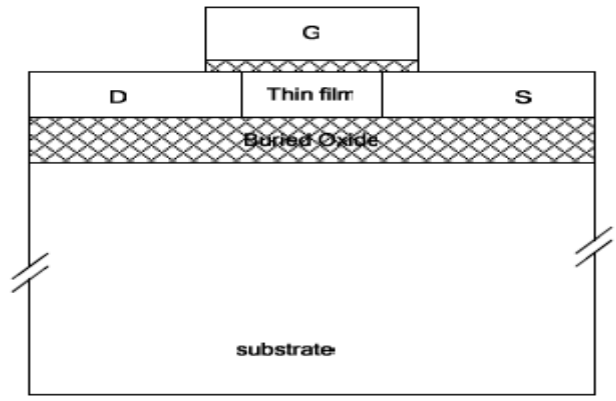

Fig. 2.7: Schematic diagram of Silicon on Insulator (SOI) MOSFET

2.3.2 MULTI GATE MOSFETS

More than one gate in MOSFET is necessary to increase the gate controllability of the device with smaller gate length. In the first stage, double gates devices were investigated and studied. Later Triple gate, Ω-gate, gate all around devices were proposed. Different Analytical models to explain the electrical characteristics of these "cylindrical surrounding-gate" MOSFETs are found in the literature [2.11]. To increase the current in smaller devices, multiple surrounding-gate channels may be stacked on top of one another. Silicon-on-Insulator (SOI) devices were very useful to prevail over SCEs. Different multi-gate devices having their relative merits and demerits are well explained by Colinge et. al. [2.11].

2.3.2.1 DOUBLE GATE MOSFET

The "Double-Gate (DG)" MOSFET is certainly sensible choice rather than Bulk MOSFETs. "Double-Gate (DG)" MOSFET, two gates are placed in both sides of the channel. The position of the gate may be in symmetry or in asymmetry. The channel which is formed near the gate is well controlled by

both the gates. In “Symmetric DG-MOSFET”, both the gates have the same dimensions and they are connected to the same potential. A schematic cross-sectional view of a symmetric double-gate MOSFET is shown in Fig. 2.8.

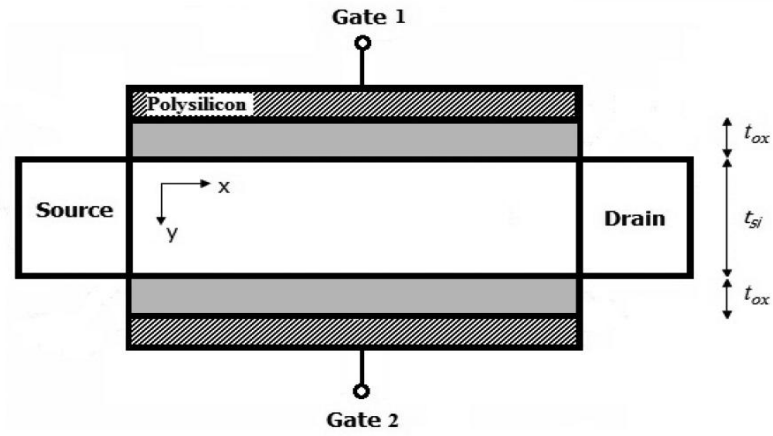

Fig. 2.8: Cross-sectional view of a symmetric double-gate MOSFET

Leakage current in this device is also reduced because the of the presence of second gate instead of substrate. The dimensions of “DG MOSFETs” are smaller than that of the bulk type devices. Sekigawa and Hayashi proposed this device structure in 1984 for the first time and it was shown to improve short-cannel effects [2.12]. In a double-gate device, the electric field lines originated from source and drain underside the device terminate on the bottom gate electrode. Therefore these field lines cannot reach the channel region. The degradation of short channel characteristics of these devices are caused only by the field lines that propagate through the silicon film itself and impinge on the channel region. Reducing silicon film thickness one can decrease this encroachment. Many researchers have reported digital, RF & analog performance of hetero-structure DG MOSFET [2.12-2.20]. Many asymmetric device structures are also studied recently [2.13].

2.3.2.2 FINFET

Most radical change in MOSFET structure happened with the invention of FinFET. Prof. Chenming Hu and his team from the University of

California, Berkeley was the first to use the term as a result of the channel shape of the device in 3D structure [2.21]. The name FinFET technology was appropriate as the FET structure is like a set of Fin when viewed from either source or drain side. A schematic view of the FinFET device structure is shown in Fig. 2.9.

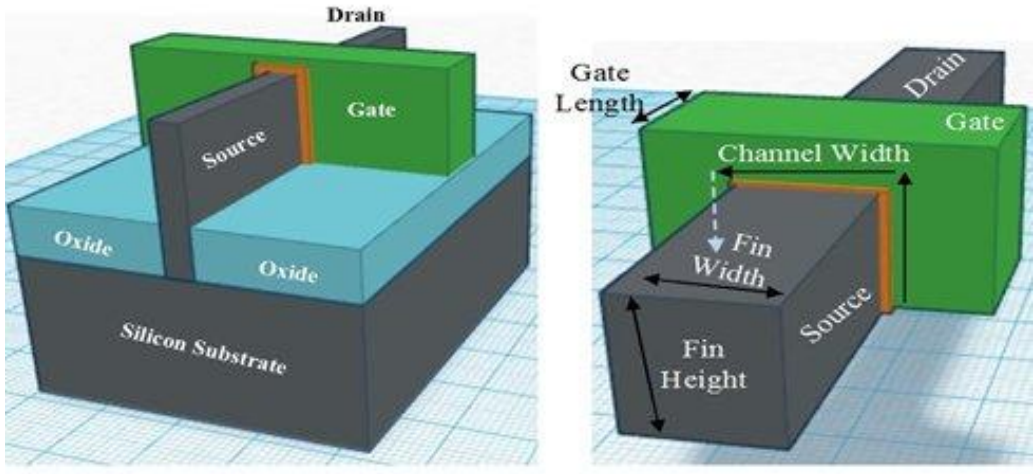

Fig. 2.9: Structure of FinFET [2.25]

FinFET technology has been natural choice as it helps in the persistent increase in the levels of integration [2.22]. Following "Moore's Law", to achieve the higher levels of integration, many device parameters have been changed [2.23-2.24]. Primarily to fabricate more devices in a given area, the feature sizes have been smaller and smaller. However, many important figures such as line voltage and power dissipation have been reduced along with increase in frequency performance. But as the process technologies reached near 22 nm node, it became unfeasible to realize the appropriate scaling of various device parameters. Power supply voltage, one of the dominant factor in decisive dynamic power, were predominantly affected. It is understood that optimizing for performance of the device resulted in unwanted compromise in other areas such as power. All these issues made it necessary to think beyond the traditional planar transistor and look at some more revolutionary options. In 2011, Intel was the first company to use FinFET in mass production. FinFET provide a significant performance improvement and also provide lower leakage current in comparison to a planer MOSFET as shown in Fig. 2.10 [2.25].

Original structure of FinFET had thick oxide on Fin top of channel & used SOI for process simplicity The triple-gate MOSFET consists of a thin-film, narrow silicon channel with gate on all the three sides [2.26]. Because of its 3D structure, Tri-Gate FET forms a conducting channel on three sides of a vertical Fin configuration, providing "fully depleted" operation. To improve the device performance further, multiple Fins may be connected together resulting higher drive current. Implementations of these related technologies include the quantum-wire Silicon On Insulator MOSFET [2.26-2.27] and the Triple gate MOSFET [2.28-2.29].

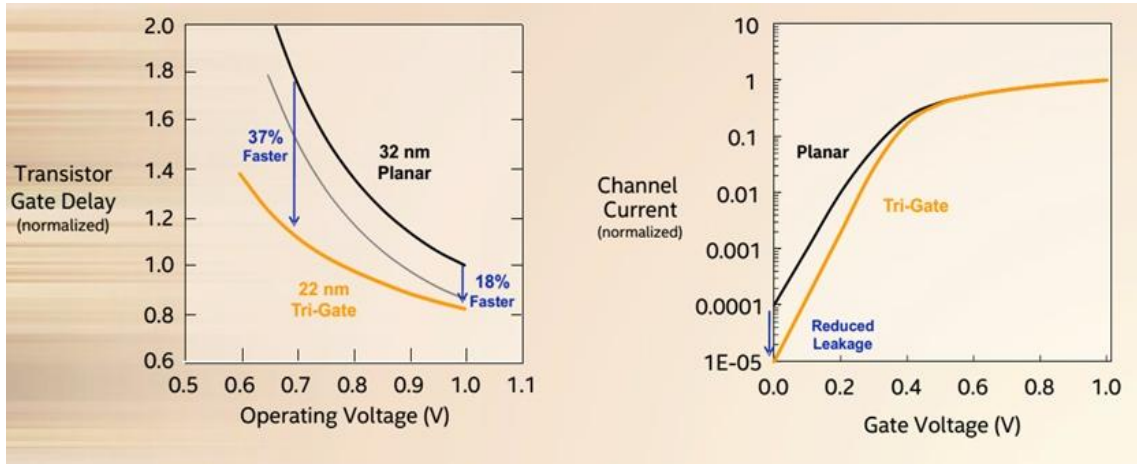

Fig. 2.10: Performance and leakage current comparison between Planar MOSFET and Fin-FET [Source: Mark Bohr, Intel]

In order to improve the Electrostatic Integrity of triple-gate MOSFETs the sidewall regions of the gate electrode is extended to some depth in the buried oxide situated underneath the channel region to form Π-gate device [2.30-2.31] and Ω-gate device [2.32-2.34]). These Π-gate device and Ω-gate device eventually increase the number of gates from 3 to 3.5. Other than only structural change, the use of strained silicon technology, a metal gate along with "high-k" dielectric as gate insulator helps in further boosting of the current drive of the device [2.35-2.38]. From literatures study it is understood that FinFETs structure and related technology have already been considered as the number one solution at the technology node beyond 22nm because of its superior performance and improved gate controllability in comparison to its planar counterparts. They also provide greater I_{ON}/I_{OFF}

current ratio and exhibit higher drive current per unit area in comparison to planar devices. Because of these advantages, FinFETs find various applications in areas like high speed digital ICs [2.39], analog ICs [2.40], SRAMs [2.40], DRAMs [2.41-2.42], and flash memories[2.43] etc. With so many recent literatures, researchers already proved that Tri-Gate transistors are significant innovation required to continue "Moore's Law".

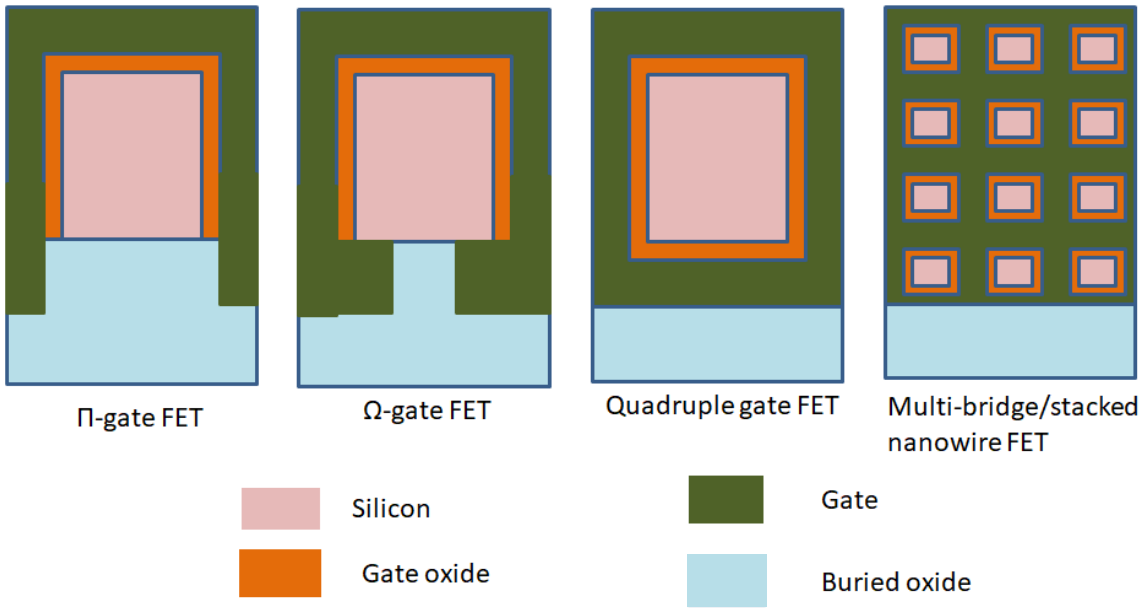

Fig. 2.11: Cross-sectional view of different gate structures [2.11].

More recently, it is established that "multiple surrounding-gate" channels can be stacked keeping gate, source and drain terminals common to increase the further current drive per unit area. Different other multi-gate MOSFET structures are available in literature. Cross sections of the channel region for the different gate orientations available in literature are shown in Fig. 2.11 [2.11].

Researchers have already shown that performance of FinFETs is greatly dependent on Fin geometry [2.44-2.49]. Recent studies on Fin shape focused on estimating the effect of Fin cross-sectional shape on SCEs, and studies on leakage current variation was found [2.46]. The effect of variability in metal grain work function and Fin-edge roughness variability affecting device characteristics are studied and reported for FinFET [2.47].

Other than SOI wafers, multiple gate devices can also be fabricated on bulk silicon wafers. Advantages of bulk wafer technology include lower wafer cost and better substrate heat dissipation rate [2.48]. However, in bulk FinFET fabrication process additional isolation steps are required which add cost to the device.

2.3.2.3 SILICON NANOWIRE FET

In the era of sub-10-nm technology node, cylindrical shaped structure with gate all around was proposed to provide better best gate controllability on the channel and reduced "Short Channel Effects" [2.49-2.50]. In this structure a gate is wrapped around the cylindrical shaped channel region and termed as Silicon nanowire FET. A schematic diagram of Si Nanowire FET and its cross-sectional view is shown in Fig. 2.12. Nanowires can be fabricated with single-crystal structures, controllable doping, and diameters as small as several nanometres. Though the Silicon Nanowire Transistors (SNWT) improves the device performance, the fluctuations in process parameters rigorously affects the device characteristics [2.51-2.52]. As per the projection of International Technology Roadmap for Semiconductor (ITRS) the multiple-gate SOI MOSFETs will be able to scale up to sub-10nm dimensions and are capable candidates for nanoscale devices in future [2,53].

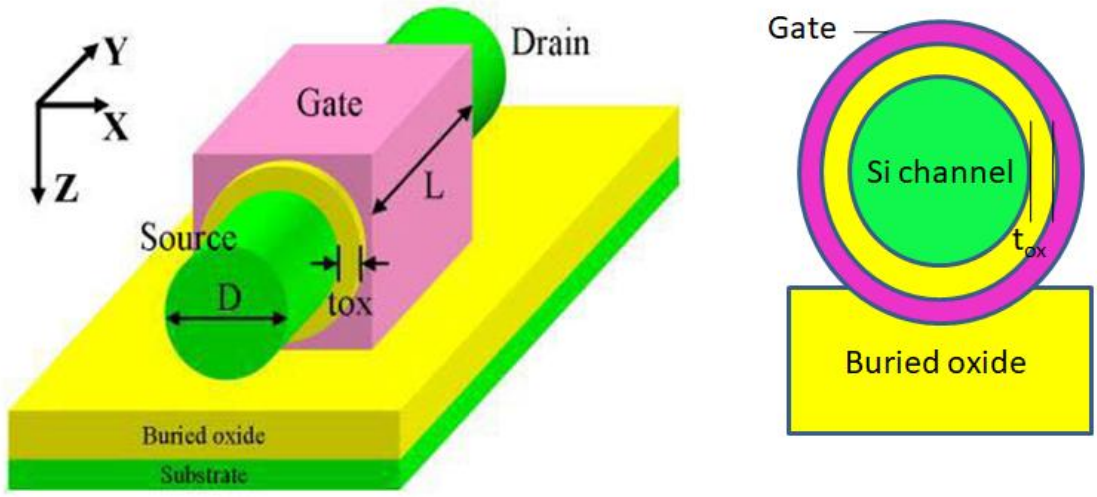

Fig. 2.12: Schematic 3D view and a cross-sectional view of a cylindrical FET

2.3.3 JUNCTIONLESS MOSFETS

Junctionless MOSFET is one of the upcoming technologies that use a novel manner to effectively control the SCEs. Junctionless FET was first proposed by Soree et. al [2.56]. The first junctionless transistor was fabricated by Colinge et al, in 2010 [2.57]. They have shown the JLTs as a potential device alternative to the conventional MOSFETs. The Junction less (JL) MOSFET is a device having same type of doping in semiconductor (i.e. either n-type or p-type) all over the silicon (from source to drain), which behaves like a resistor [2.57-2.58]. In conventional MOSFETs two PN junctions namely the "source junction" and the "drain junction" is separated by a region with opposite doping type. But in contrast, Junctionless device has same doping type in source, channel and drain region as shown in Fig, 2.13. The distance between these two junctions (source and the drain junctions) under the gate is known as physical gate length of the device. In junctionless transistors, effective gate length is larger than the physical gate length.

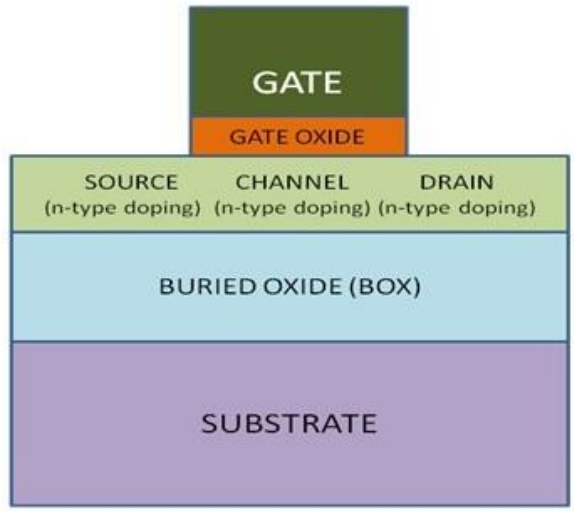

Fig. 2.13: Schematic view of the n-type Junctionless transistor

The working principle of a Double gate Junctionless MOSFET (DG-JLFET) is different from a conventional inversion-mode DGFET as discussed in Durate et. al. [2.59-2.60]. The Band diagrams of double gate Junctionless MOSFET for different gate bias is shown in Fig 2.14 [2.59]. Both gates made

of p+ poly-silicon poses the same work-function (W_F), and the gates are shorted together to apply same voltage to each gate. The electron quasi-Fermi level of the source–drain is taken as a reference for the other energy levels. Equation 2.3 may be used to estimate the work function difference between the gate and the channel,

$$\frac{E_g}{2} + qv_T \ln\left(\frac{N_{Si}}{n_i}\right) \qquad (2.3)$$

where E_g is referred as the band gap of silicon, v_T is the "thermal voltage" (kT/q), N_{si} is denoted as "doping concentration" of the silicon channel, and n_i stands for "intrinsic carrier density".

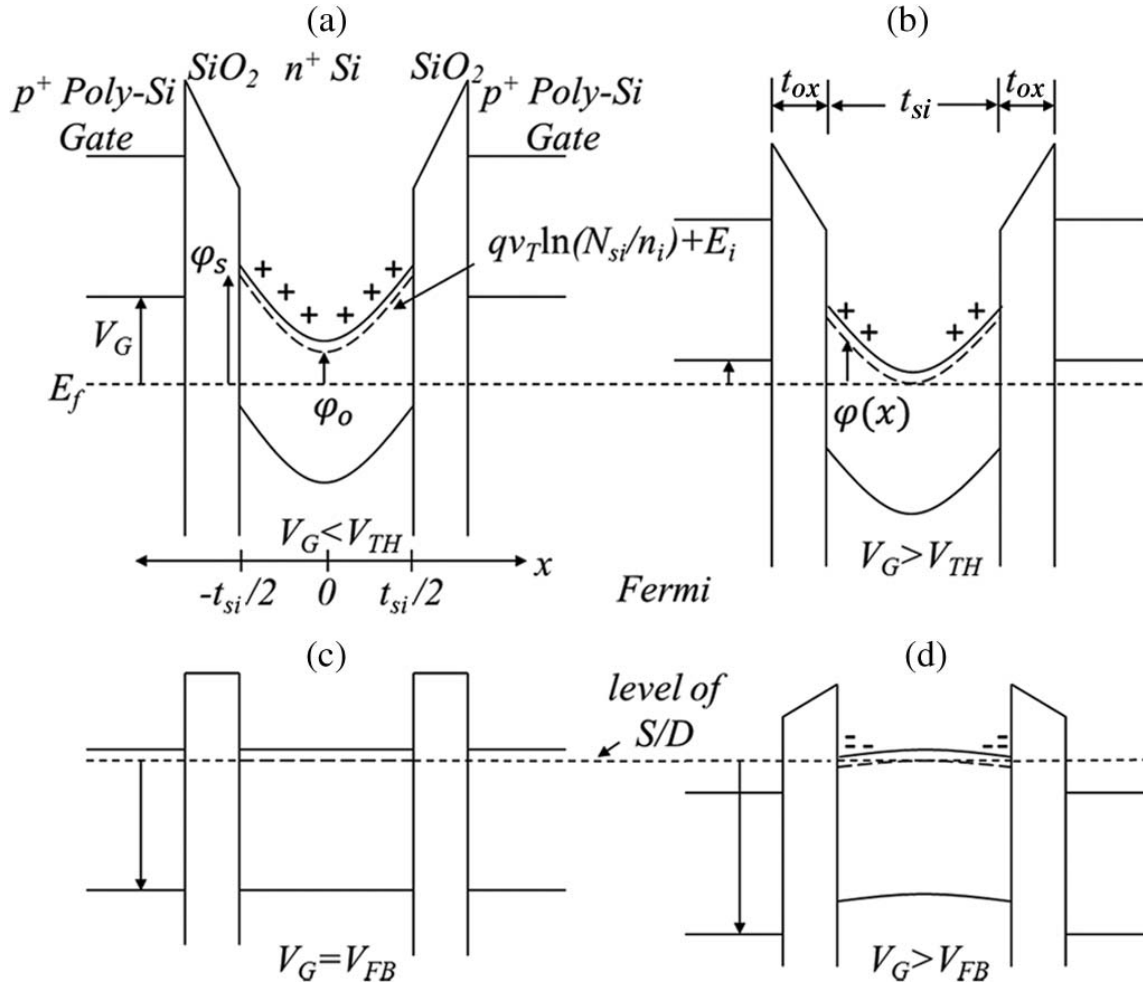

Fig. 2.14: Schematic band diagrams for a symmetric Double Gate-Junctionless FET [2.59]

In Fig, 2.14(a), the gate voltage is considered lower than the threshold voltage (V_{TH}) i.e. the device is under a sub-threshold condition. In this state

the channel is fully depleted. When the gate voltage V_G higher than V_{TH}, the channel become partially depleted allowing a small current flow through the centre of the channel via the bulk conduction mechanism as shown in Fig. 2.14(b). A completely neutral channel is created for the gate voltage equal to the "flat band voltage" (V_{FB}). High current can flow through the entire channel [Fig. 2.14(c)] in this condition. In DG-JLFETs, doping concentration of the silicon channel (~1×10^{19} cm^{-3}) is somewhat high compared to a conventional "inversion-mode" FET. This condition makes the work function difference roughly equal to band gap of Si, i.e., 1.1 eV. At a larger gate voltage than V_{FB}, the mobile carrier density is improved at the surfaces. The surface current conduction is regulated by the carriers that accumulate at the channel interface and this situation is depicted in Fig. 2.14(d). From the above mechanism it is clear that the DG-JLFET current is mostly composed of the bulk current in the linear and sub threshold regions.

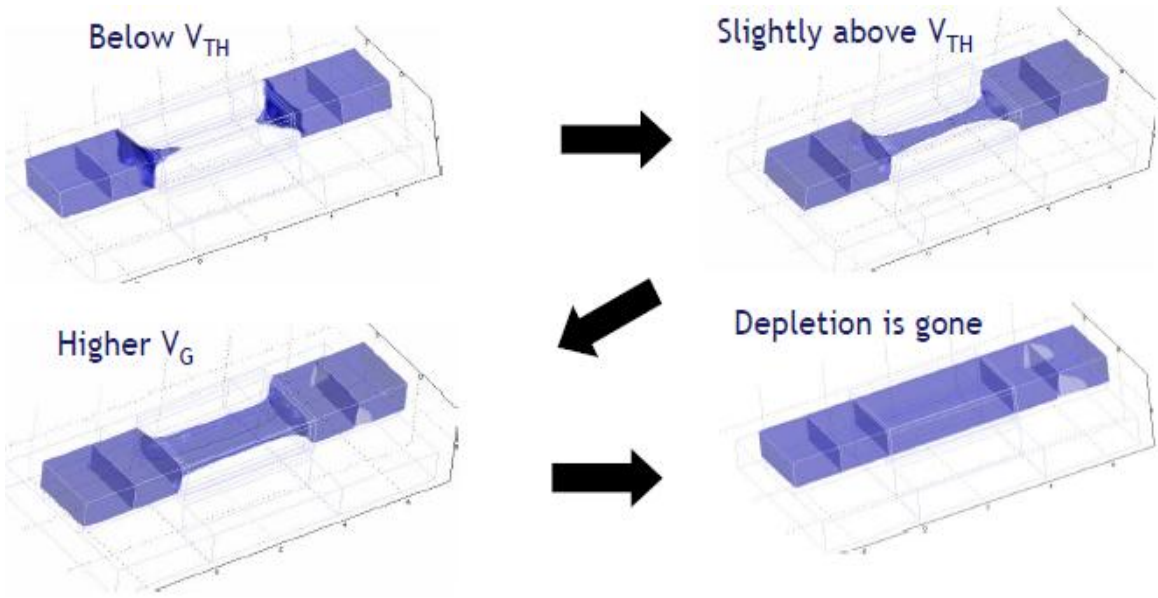

Fig. 2.15: Electron concentration contour plots in an n-type Junctionless transistor [2.62]

On the other hand, electrons in traditional "inversion-mode" Double Gate FETs are characteristically restricted near the interface in the linear region which produces the surface current. In contrast, they are concentrated at the centre of the channel due to volume inversion in the "sub-threshold" region [2.61]. Fig. 2.15 shows the neutral (non-depleted)

regions of a JNT above threshold, for different values of gate voltage [2.62-2.63]. The solid contour corresponds to the regions where the “electron concentration” is equal to N_D. The depletion region where the “electron concentration” is lower than N_D is represented by transparent portion of the diagram.

It is well recognized from the published works that JL FETs have stronger immunity against short-channel effects compared with Inversion Mode FETs. In the accumulation mode device, the channel region consists of the same type of doping as that of the source and drain regions. These MOSFETs are devices controlled by majority carriers and use the capability of the gates to accumulate or deplete a channel region to turn the device “ON” or “OFF” respectively [2.64]. These devices are termed as Junction Less Accumulation Mode (JAM) Transistor. From the fabrication point of view, the most significant issue of a Junctionless FET is the creation of a thin and narrow semiconductor layer as channel and proper channel doping concentration. This thin layer is essential to have full depletion of carriers during OFF state of the device. However if the doping level of the semiconductor is low, it may easily deplete the carriers at OFF-state but source/drain series resistances become high. On the other hand, if the doping of the device be high enough so that a sufficient amount of current flow during the ON states of the device, it in turn degrade the ability to turn-OFF. Therefore, the device with additional source/drain doping is used to prevail over this issue. The device is turned “OFF” by body depletion using a suitable gate work function. Superior reliability of “Junctionless” FET compared with “inversion-mode” FETs is demonstrated experimentally by Maria et.al. [2.65].

Junctionless Field-Effect-Transistor was studied by many researchers [2.66-2.67] as a capable technology for “highly-scaled” devices. Because of the fact that there is no junction in the junctionless devices, the cost of manufacturing of the device can be reduced. Recently a junction less-accumulation-mode p-channel MOSFET is successfully implemented and reported based on a junction-isolated bulk FinFET [2.67]. Usefulness of

Junctionless MOSFETs in achieving superior analog/RF metrics is also reported in literatures [2.68]. Literatures also reveal that the JL bulk FinFETs exhibit a favourable ON/OFF current ratio and "short-channel" characteristics [2.69-2.70]. Recently, investigation report of the junctionless accumulation-mode (JAM) bulk FinFETs showed that superior device performance in terms of SS, DIBL, and ON/OFF current ratio can be achieved with high-κ gate spacers. [2.69-2.70]. For the devices of 22nm technology, the effective oxide thickness (EOT) of the traditional SiO_2 dielectrics are required to be smaller than 1 nm, which results high gate leakage currents because of the quantum tunnelling effect. So, dielectrics with higher dielectric constant (k-value) can prevent this leakage current with thicker physical dimension but having desired effective oxide thickness. At the same time, a very large k value cause unfavourable large fringing fields around the source and drain regions and is not desirable. Hafnium-based oxides having dielectric constant of 22 poses well insulating properties and capacitance performance [2.71-2.75]. It is worth mentioning that the device with HfO_2 spacer shows much improved performance in drain current and transconductance when biased in the saturation region compared to SiO_2 spacer device [2.71].

In order to obtain suitable threshold voltage (V_{TH}), low SS and higher I_{ON}/I_{OFF}, lower channel doping is preferred. But lower doping concentration adversely increases the S/D series resistance. To overcome this problem, higher doping in source and drain (S/D) region has been used to decrease the parasitic resistance in the source/drain extension region. This device is called Junctionless accumulation mode MOSFET [2.69, 2.75-2.76]. Basic difference between Junctionless MOSFET and Junctionless Accumulation Mode MOSFET is shown in Fig. 2.16. The drain current (in log scale) of an inversion mode, junctionless mode and junctionless accumulation device as a function of gate voltage is shown in Fig. 2.17 [2.77].

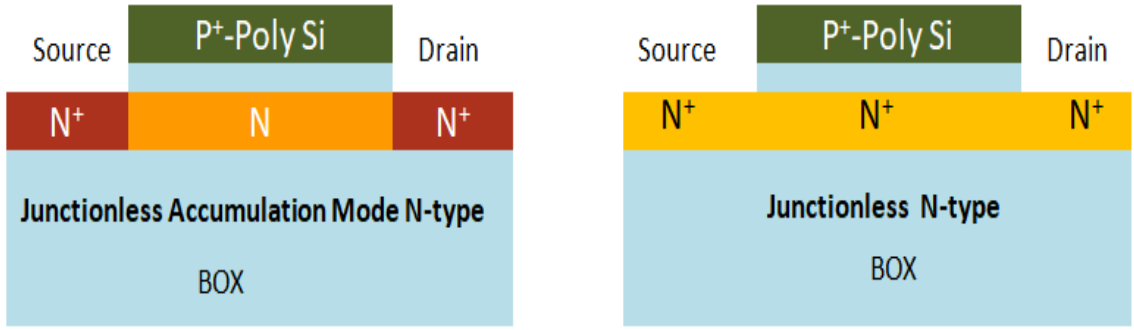

Fig. 2.16: n-type Junctionless MOSFET and n type Junctionless accumulation mode MOSFET

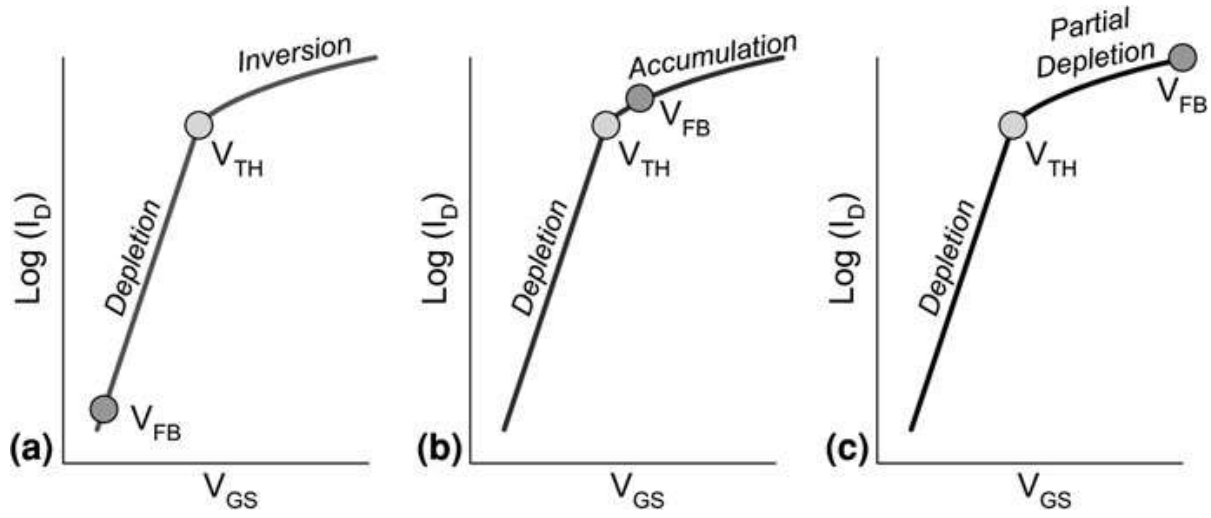

Fig: 2.17: Drain current in log scale vs. gate voltage for different MOSFETs a) Conventional inversion-mode MOSFET b) a Junctionless accumulation-mode MOSFET with higher source drain doping and c) Junctionless transistor with same high doping in source, drain and channel [2.77]

In an inversion mode device, flatband voltage (V_{FB}) is to be found much below the threshold voltage, V_{TH}. Below threshold, the device is either fully or partially depleted and is off. An inversion layer is formed in the channel above threshold voltage. In case of accumulation mode devices, the device channel is entirely depleted. For the gate voltage when a segment of the channel is no longer depleted (partially depleted), threshold voltage is reached. When at a gate voltage above V_{TH}, flatband voltage (V_{FB}) is reached

and the channel becomes neutral and no portion remains depleted. Above V_{FB}, surface accumulation channel is created by the gate voltage. In contrast, below threshold voltage, a Junctionless transistor with heavily doped source, channel and drain region is fully depleted as indicated in Fig. 2.17(c). By increasing the gate voltage, the peak concentration of electron of the channel can reach the doping concentration and it reaches the threshold voltage. With further increase of gate voltage, diameter of the conduction region increases and the flatband condition is reached. In this case, V_{FB} is much above the V_{TH} [2.77]. The fabrication of Junctionless transistors is much simpler and the elimination of junctions greatly simplifies processing. CMOS circuits implemented with JL FinFET devices were reported to perform better than the Inversion mode FinFETs. [2.75].

Some advantages of junction less Transistors are (i) Source/Drain engineering is radically simplified by removing the related junctions and the Source/Drain extension regions. (ii) SS is nearly ideal and DIBL also very small. (iii) Extremely low leakage current (iv) Less degradation of mobility with gate voltage and moderate temperature sensitivity (v) Easier to fabricate with lower thermal budget.

2.3.4 MOBILITY IMPROVEMENT

In the search for extending the progress of nanoscale devices, materials other than silicon has been under intense scrutiny. A material such as Compound semiconductors of III-V groups, carbon nanotubes, grapheme etc has been studied intensely in recent past. Mobility improvement of the channel material is a key issue.

2.3.4.1 III-V MATERIALS BASED MOSFET

III-V based MOSFETs are considered as one of the promising device structure for high performance digital logic applications [2.78-2.81]. At present, it is expected that III–V MOSFETs may permit more drive current and higher transconductance as compared to their Si-based counterpart [2.78].

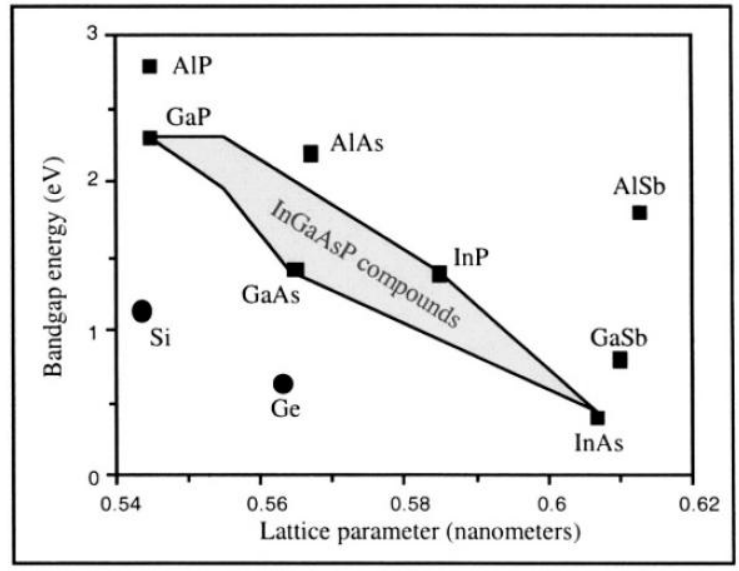

Fig. 2.18: Bandgap energy of Si, Ge and III-V Compound Semiconductors

Though, Silicon is the mostly used material in the electronics industry, other heterostructure materials are also used. A wide range of compound semiconductor materials can be obtained using elements from Periodic Table's columns III and V, like GaAs, InP, $In_xGa_{(1-x)}As$ etc. The main parameter which defines the important characteristics of these materials is the bandgap energy. Figure 2.18 shows the bandgap energy for germanium, silicon and different other III-V compounds used in Semiconductor industry [2.79]. Desired band gap energy as well as electron mobility of the channel may be obtained by using different mole fraction of the materials during fabrication. Lower effective mass (m*) of InGaAs/InAs in comparison to Silicon causes the high electron mobility and high injection velocity. Injection velocity and electron mobility is related with effective electron mass with the following relations as expressed in eq. (2.4).

$$\mu \approx \frac{1}{m^*} \quad \text{and} \quad v_{inj} \approx \sqrt{\frac{1}{m^*}} \qquad (2.4)$$

Few important material properties of III-V group materials along with Si are tabulated in Table 2.1. These smaller effective mass also provides higher tunnelling probability which ensures its better On-state performance of the Nanoscale heterostructure transistors [2.82-2.83].

Table. 2.1: Bulk carrier mobility of different channel materials

Material	Relative permittivity	Mobility ($cm^2/V.s$)	
		Electron	Hole
Si	11.9	1400	470
Ge	16.2	3900	1900
GaAs	12.9	8500	400
InAs	15.2	40000	500
InSb	16.8	77000	850

Beside greater transport properties III-V compound semiconductors also enjoys the matured fabrication technology. Few challenges remain in terms of high-k gate dielectrics with lower interface trap density which is crucial for MOSFET operations. Another major challenge is the manufacturing scheme suitable to integrate III-V materials on Si wafers. However, InGaAs is being intensively studied as one of the semiconducting materials that may replace Si in the transistor channel at or beyond the 10-nm CMOS logic technology node [2.84-2.86]. Many researchers have reported digital, RF & analog performance of hetero-structure DG MOSFET [2.87-2.88]. Many heterostucture MOSFETs based on III–V group material have been proposed and compared with their silicon-based counterpart. From published results, it is understood that the III–V group materials based heterostructure device showed exceptional control of SCEs, higher on current (I_{ON}), lower delay than that of silicon-based device of same dimension [2.88]. It is worth mentioning that the thickness of SiO_2 as gate dielectric material has reached the point where the direct tunnelling mostly increases the leakage current, affecting the circuit operation. To overcome this problem, materials with high dielectric constant have been introduced [2.89]. Hafnium based oxides HfO_2 is one of the many candidates of possible high-k gate dielectrics have been suggested to replace SiO_2 including. In a recent study, the asymmetric behaviour of the underlap DG heterostructure MOSFET was analyzed extensively [2.90]. Until now, researchers have been mainly investigating different aspects of InGaAs-channel MOSFETs for digital applications and for analog/mixed-signal applications. The impact of different barrier layers on the analog performance [2.88] and digital

performance [2.91] of an InGaAs MOSFET was also investigated. Use of barrier layers change the gate-to-channel separation which in turn affects the gate control on the conduction layers and proven to be an effective way to modulate the electron confinement in the channel and decrease short channel effect for high speed RF/analog applications. Recently, the simulation and analysis of devices with InGaAs channel and InP barrier layers DG heterostructure MOSFET has been reported for ultra low-power digital applications [2.91]. From the analysis it is understood that III-V based channel materials are one of the important materials to be thoroughly investigated in near futures.

2.3.4.2 THE STRAINED SILICON/GERMANIUM MOSFET

Strained silicon technology which creates strain in the silicon channel has been emerged as a commanding technique of improved MOSFET performance [2.92]. Conventionally, epitaxial layer growth of Si on SiGe allows the formation of strained silicon. Carrier mobility in strained silicon is enhanced by induction of biaxial strain due to increase in lattice constant of silicon. Further, carrier mobility can be increased by increasing "*Ge"* content of the "SiGe" layer [2.93]. Velocity saturation works against mobility enhancement for the nanoscale devices due to high electric field. Velocity overshoot should be taken into consideration in modelling Strained Silicon based MOSFET which becomes prominent in nanoscale devices [2.94]. Recently, many works has been reported using strained silicon technology for achieving improved performance due to higher carrier transport properties and its is also compatible with conventional CMOS technology[2.95-2.96].

2.3.4.3 CARBON NANOTUBE AND GRAPHENE

Carbon Nanotubes (CNTs) are planar graphite sheets known as graphene which are flawlessly wrapped into tubes shapes, as shown in Fig. 2.19 [2.97]. CNTs possess exceptional electrical characteristics and it can be fabricated with very small dimensions as small as 4-8Å in diameter. The favourable electrical properties of a CNT depend on its diameter and the

wrapping angle of the graphene [2.97-2.99]. Theory indicates that structure of carbon naotubes may be expressed by a chiral vector linked with two integers (n,m). CNTs can be metallic or semiconducting depending on the difference of values in fundamental tube indices (n, m), and its bandgap isdependent on the diameter. Analysis also indicates that semiconducting CNTs have very high low-field mobilities, large current carrying capability, the excellent thermal and mechanical stability and high thermal conductivity [2.100]. Because of their superior material properties, nanotubes are attractive as future interconnects and also show enormous advantages as a channel material of high-performance MOSFETs. Though CNT based MOSFETs promise great performance lots of processing issues remains such as fabrication of identical nanotubes, control of abrupt doping profiles etc [2.101].

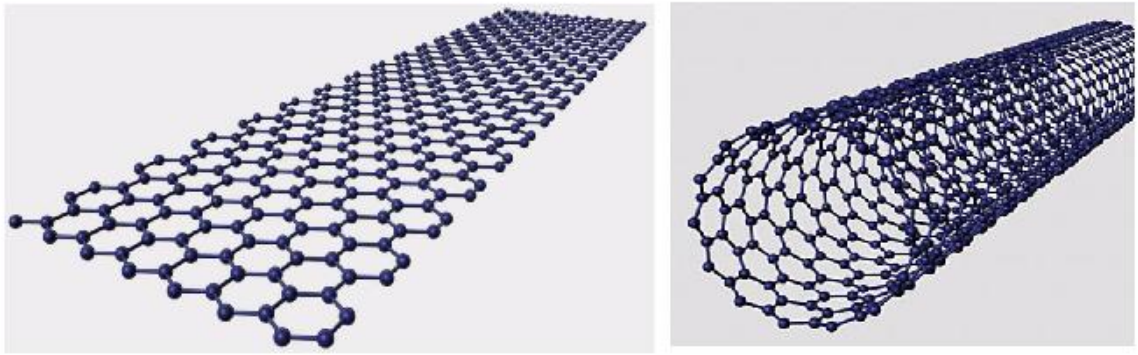

Fig. 2.19: Sketch of graphene nanoribbon and carbon nanotube.

2.3.5 TUNNEL FET

Tunnel FET (TFET) is considered as a possible replacement for CMOS in low-power applications [2.102]. The device structure of a TFET differs from that of the conventional MOSFET as type of doping in source and drain regions of TFET are of opposite types. A schematic diagram of single gate n-type TFET is shown in Fig. 2.20. A positive voltage in gate and reverse bias between source and drain is required to switch the n-type device ON. It is a semiconductor device based on the principle of band to band tunnelling of electrons rather than thermal emission. Tunnel FETs operate by tunnelling through the S/D barrier rather than diffusion over the barrier. The device

switches between ON-state as well as OFF state at lower voltages than the operating voltages of the MOSFET making it a suitable choice for low power consumption application in the era of emerging nanoscale devices. This type of device is capable of providing extremely low OFF-current and steeper sub-threshold slope than conventional MOSFET [2.103]. Tunnelling occurs for an electron between valence band of the semiconductor to the conduction band though a potential barrier without having enough energy required for this transition and this phenomenon can only be explained by quantum mechanical physics. The output characteristics of a Tunnel FET are dependent on the parameters such as the doping, the gate work function, etc. Therefore, these parameters can be modified to obtain the desired output characteristics of a tunnel FET. [2.102-2.103]. However, from the fabrication point of view TFET faces few challenges such as fabrication of ultra-thin body required for robust electrostatics, formation of abrupt junction, III-V/high-k interface with low trap density etc [2.104]

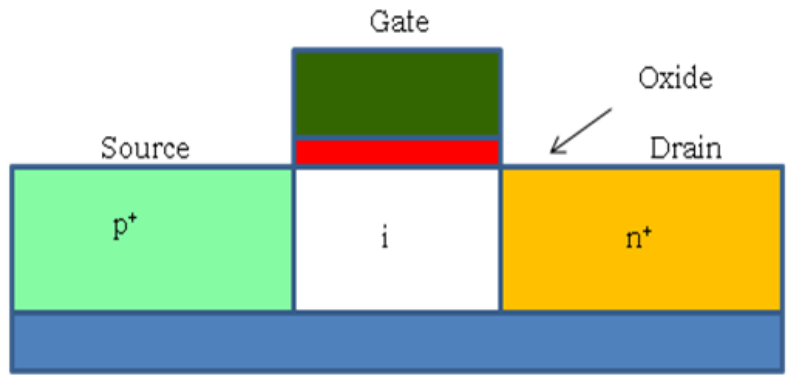

Fig. 2.20: Schematic diagram of Tunnel FET

The Tunnel FET's electrical behaviour is very promising and is considered as a strong candidate to complement or replace MOSFET technology. It finds applications particularly for devices of low standby power applications. In recent past lots of researchers are working on Tunnel FET and improvements in device performance is shown [2.105-2.107]. Today TFET is considered as the most promising device for steep-slopped switching and it also has the potential to be used as low power devices because of its low "OFF-current" [2.108-2.109].

2.4 IMPORTANCE OF ANALOG/RF PERFORMANCE

The requirement for high-performance, a low cost RF solution is mounting because of immense growth in market of the RF wireless communications system [2.110-2.111]. The silicon MOSFET is the most popular transistor structure used to digital circuits or lower-frequency analogue applications. This device now makes noteworthy inroads into the land of micro- and millimetre-wave circuits [2.112-2.117]. With gate lengths below 100 nm, its cut off frequencies f_T and f_{max} now compete with other devices. The CMOS is expected to integrate RF with digital circuits to design a system on a single IC to allow mixing of both digital and analog functionality on the same die, with growing performance while keeping system sizes reserved. There are many challenges in analog and RF circuits with a digital CMOS technology. For System on Chip (SoC), optimization of the devices becomes more challenging. Prediction of circuit performance accurately using simulation helps to achieve less time to market and reduction in design for RF products. It has been understood that that for analog and RF domain, the correctness of circuit simulation findings is powerfully determined by device models used. Initially, MOS transistor models have been developed for applications in digital circuits and low-frequency analog circuits' applications. These models mainly focussed on dc drain current, off current, I_{ON}/I_{OFF} ratio, transconductance, intrinsic capacitance behaviours up to mega hertz range. However, when the operating frequency reaches GHz range, circuit design becomes challenging and need to consider extrinsic components also. With devices downscaling importance of extrinsic device parasitic enormously increases. Parasitic are particularly important for advanced architectures such as multi-fins, 3D structures, thin-body devices etc [2.112]. In the device level, main analog/RF figures of merits includes cut off frequency (f_T), maximum frequency of oscillation (f_{max}) and output voltage gain (A_{vo}) depending on Transconductance g_m, Drive current, I_d, Output conductance, g_d, Early voltage, V_{EA} ($V_{EA}=I_d/g_d$), g_m/I_d ratio, gate capacitance, C_{gg} and Parasitics (C, R). In the IC level gain bandwidth product (GBW) is also important

parameters. In the recent past, the analogue/RF performances analysis of scaled MOSFETs has become a focus of enormous interest for their application in ultra low power high-gain analogue/RF circuits [2.113-2.117].

Linearity is also an important parameter to consider in CMOS RF circuits. Linearity analysis helps to ensure that high order harmonics and inter modulation terms are insignificant at the output. System level technique to improve linearity requires complex circuits making a device level linearization more appropriate [2.118]. For a direct evaluation of RF linearity performance, various Figure of Merits (FoM) namely VIP2, VIP3, IIP3, IMD3 and 1-dB Compression Point has been studied and reported in various literatures [2.119-2.121].

2.5 SUMMARY

In this chapter, a widespread literature review of the potential difficulties related to scaling and its remedies are presented. The motivation behind scaling is presented and the cause and possible remedies of most of the several short channel effects discussed. Existing and upcoming technologies are reviewed in connection with immunity to SCEs. Different technologies like multigate MOSFET, junctionless transistor, channel engineering employed to improve SCEs are discussed. The RF/analog performance of advanced nanoscale device structures has also been studied. Advantages of FinFET structure in Junctionless Accumulation Mode (JAM) is studied for improved SCEs performance. Fabrication and digital performance study of JAM bulk FinFET are available in literature. But no analog/RF performance of the JAM bulk FinFET was found. Investigation of the impact of spacer on Analog/RF performance has also not been reported yet. Effect of Fin Width scaling and effect of Fin shape on analog/RF performance has not been reported. III-V heterostructure MOSFETs and its advantages has been studied. RF, Analog and Linearity performance analysis of InGaAs/InP heterostructure MOSFET, especially on barrier structure and channel material compositions has not been observed.

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CHAPTER 3

SPACER ENGINEERING ON JUNCTIONLESS ACCUMULATION MODE BULK FINFET

3.1 INTRODUCTION

Scaling has been the key issues for continuous progress in silicon based CMOS technology in semiconductor industries over the past decades. In Conventional planner MOSFET structures as gate length reaches nanometer scale, Short-Channel Effects (SCEs) become most important issue for device performance [3.1] which can't be ignored. When the channel length decreases for conventional MOSFETs, the controlling capability of the gate over the channel depletion region reduces because of the increased charge sharing from source/drain which is the origin of various Short Channel Effects (SCEs). SCEs degrade the device performance significantly. To reduce the SCEs, various approaches have been explored and planned by the researchers [3.2]. New device architectures and materials are crucial to reduce the impact on "Subthreshold Slope" (SS), "Drain-Induced Barrier Lowering (DIBL)", "Threshold Voltage (V_{th})" etc. Many new device structures have been proposed such as "Fully Depleted Silicon-on-Insulator (FDSOI)" MOSFETs, Double-Gate (DG) MOSFETs, and "Multi-gate MOSFETs" etc [3.2]. Although, Multi-gate MOSFET or FinFET provide superior gate controllability, the formation of sallow junction in the time of manufacturing remains as a bottle neck. Series resistance of the channel is also an issue. These issues can be solved by employing the Junctionless MOSFET technology. In the area of device physics, Junctionless technology is one of the emerging techniques that use a novel design to effectively control the SCEs. Junctionless FET was proposed by Soree et. al in 2008 [3.3]. Later in 2010, the device was fabricated successfully by Colinge et.al. [3.4]. The Junction less (JL) MOSFET is a device having same type of doping throughout the whole silicon (from source to drain), which behaves like a resistor [3.4]. In conventional MOSFETs two PN junctions called the "source junction" and the "drain junction" is separated by a region with opposite doping type. But in contrast, Junctionless device has same doping type in source, channel and drain region. In this device, the work function difference between the gate material and the silicon channel is used for switching of the device. It is well recognized from the published works that

Junctionless MOSFETs have stronger resistance against SCEs compared with Inversion Mode FETs. In a Junctionless accumulation mode device, the doping type of the source, channel and the drain regions are same. These MOSFETs are majority carrier devices and use the capability of the gates to accumulate or deplete a channel region and turn the device ON or OFF, respectively [3.5]. In order to obtain suitable threshold voltage (V_{th}), low SS and higher I_{ON}/I_{OFF}, lower channel doping is preferred. From the experimental data available in literature, it is understood that if the channel doping increase SS and DIBL increase along with decrease in I_{ON} and increase in I_{OFF} [3.6]. It has been proved that channel doping of the order of 10^{18} helps by providing better conduction [3.7]. Threshold voltage sensitivity also reduced with decrease in channel doping [3.7]. But lower doping concentration adversely increases the S/D series resistance. As a remedy, many researchers have used additional source/drain implantation in order to decrease the parasitic resistance in the source and drain extension region [3.8-3.10]. This device is called Junctionless accumulation mode MOSFET. The principle of operation and physics behind the Junctionless transistors are different from the principle of the conventional inversion-mode (IM) devices. Greater reliability and better performance of Junctionless MOSFET compared with inversion-mode FETs is experimentally verified [3.11].

Junction less field-effect-transistor was studied by many researchers [3.10-3.14] as a capable candidate for “highly-scaled” devices. Recently, a junction less-accumulation-mode (JAM) MOSFET with p-channel is effectively implemented and reported based on a junction-isolated bulk FinFET [3.9]. Effectiveness of ultra low- power (ULP) Junctionless MOSFETs in achieving enhanced analog/RF metrics is also reported [3.13]. Literatures reveal that the Junctionless bulk FinFETs exhibit a favorable ON/OFF ratio of drain current and short-channel characteristics [3.10, 3.15]. It is also shown the use of spacer can enhance the device performance. Recently, investigation report of the “Junctionless accumulation-mode bulk FinFETs” showed that with high-κ gate spacers, superior device performance in terms of SS, DIBL, and ON/OFF current ratio can be achieved. [3.10]. In order to utilize the advantages of both the FinFET and Junctionless device

technology, Junctionless accumulation device is proposed and studied.

As the feature size within an integrated circuit decreases, the density of the transistors increases. The performance of the devices in terms of speed also increases which leads towards the concept of System-on-Chip (SoC). In SoC, the RF and analog communication circuits are integrated with the digital logic and memory circuits. There are many challenges in analog and RF circuits with a digital CMOS technology. For System on Chip (SoC), optimization of the devices becomes more challenging. So it is required to investigate the device structure to enhance the device performance for digital and analog/RF circuit applications [3.16-3.19]. Most of the existing works on FinFET are based on device design for performance improvement for inversion mode or Junctionless mode. Study on performance improvement for Junctionless accumulation mode was limited on its digital performance analysis. Therefore, requirement of Analog/RF analysis for Junctionless accumulation mode devices still remained valid.

In this chapter, exploration of the Analog and RF Performance of a Junctionless accumulation-mode (JAM) bulk FinFET along with its digital performance is presented. Extensive simulations and analysis have been performed to study various key analog/RF figures of merits of the device. Spacer material as well as spacer length of the device is varied and performance of the device is compared thoroughly in this work. The circuit level performance of JAM Bulk FinFET device on resistive load inverter has been provided in order to appraise the effect of the spacer length through the transient response. This study demonstrates the appropriateness of high-k spacer material for device performance analysis.

3.2 BULK FINFET

FinFETs can be classified as SOI FinFET and Bulk FinFET. Initially, FinFETs were fabricated on SOI wafers and were familiar as SOI MOSFETs. Structure of SOI MOSFETs helped in overcoming the Short Channel Effects related problems. SOI FinFETs are also easy to fabricate and possesses good scalability. These devices also have advantages of less parasitic capacitances. But these devices suffer from “floating body” problems and

heat dissipation issues because of thick “buried oxide”. SOI wafers are also expensive in comparison to Silicon wafers because of additional oxide layer. To overcome these challenges, bulk FinFETs are proposed i.e. body is directly fabricated on the Si wafers. These devices have very good heat dissipation path through the bulk Si wafers [3.20]. Fabrication steps of bulk FinFET is also compatible with those of planner 2D devices. They also provide almost same scalability as SOI FinFET. A schematic cross-sectional view of SOI FinFET and bulk FinFET is shown in Fig. 3.1.

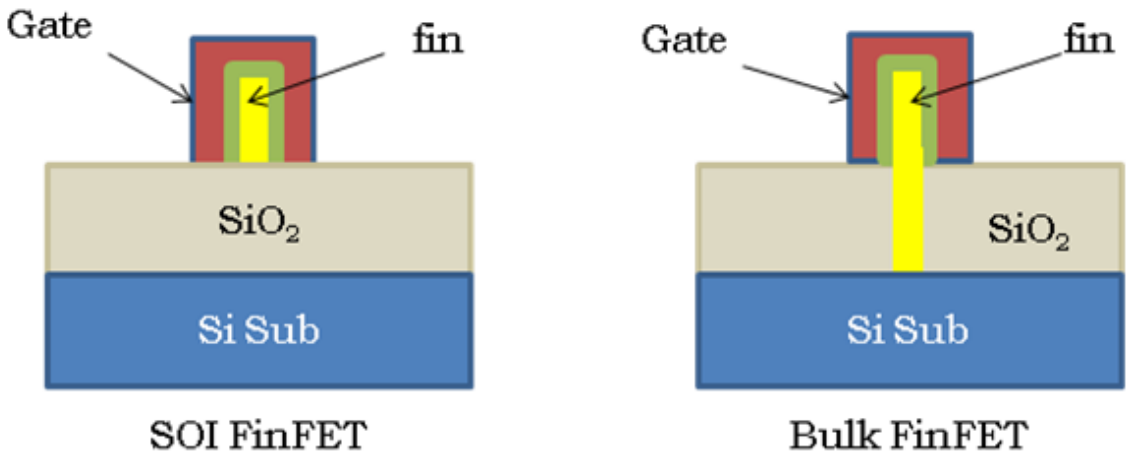


Fig. 3.1: Cross-sectional view of SOI FinFET and Bulk FinFET

3.3 Detailed Structure of the Device under Study

Fig. 3.2(a) shows the three dimensional (3-D) structure of the device and 3.2(b) shows the vertical cut plane view through the middle of the Fin. One of the simplified approaches adopted by researchers for device simulation is the use of two-dimensional simulation by taking cross-section of the 3-D device. As the device under study is a 3-D device, 2-D analysis leads to inaccuracy in simulation results [3.21] as a 2-D model would fall short to account for interactions coming from those portions of the model outside the considered plane. In a tri-gate FinFET device, there are two vertical gates on both sides of the “Fin” shaped channel and a horizontal gate situated on top. Moreover, it is important to consider 3-D Electric field for accurate capacitance evaluation of the nanoscale FinFET devices [3.21].

Hence, a 3-D simulation approach is employed in this work in order to get an accurate assessment of the influence of fringing field on performance of the FinFET. In n-type Junctionless Transistor under study, has n^+ doping for the source and drain region ($10^{21}/cm^3$) and n type doping in the channel region ($10^{18}/cm^3$). Doping concentration of different region is tabulated in Table 3.1. This additional source/drain doping is necessary to prevail over parasitic resistances in source and drain extension regions. A metal having work function equals to 4.65 eV is used as gate material. Conventionally polysilicon is preferred as gate material in MOSFETs. The work-function (W_F) in polysilicon can be varied to change the flat band voltage resulting in a change in the threshold voltage. But polysilicon is not favorable as gate material for nano MOSFETS because of its high thermal budget process and degradation due to the depletion of the doped polysilicon [3.22]. In this regard, metal gate is preferred nowadays over polysilicon [3.23-3.24]. The use of metal alloys as gate materials to obtain different gate work function has been already reported [3.23-3.25]. For devices with low channel doping such as FinFET, the gate work function is required to be close to the silicon mid bandgap (4.5eV) ± 0.2eV in order to obtain a desirable threshold voltage [3.22]. This criterion can be fulfilled by Molybdenum whose work function can be varied over a wide range (4.5- 4.9 eV) by using the implantation of nitrogen into Molybdenum followed by a thermal anneal [3.23, 3.25]. In this research, gate work function equals to 4.65 eV is considered because it corresponds to Molybdenum, as a gate material. To minimize the gate leakage current, HfO_2 gate dielectrics with an “equivalent oxide thickness” (EOT) of 1.25 nm is used. The simulated devices have a length of the gate (L_g) of 20nm, height of the Fin (H_{fin}) of 20nm and Fin width (W_{fin}) of 20nm. Among other device parameters, spacer length is assumed as 15 nm with a source/drain to spacers overlap length of 3 nm. The under Fin thickness of 60nm is used whereas field oxide thickness of 35nm is considered in this work. In order to improve SCEs, spacers are used for both sides of the gate. Different spacer materials with different dielectric constants (k) are used to verify the effect of spacers on device performance. As a result of this design, a large segment of the “lightly-doped” channel region is under the spacer

and softly controlled by the gate. So, this channel region is sensitive to the fringing field originated from the gate and passing through the spacer due to its close contact [3.21]. In order to estimate the effect of spacer length, the length of both the spacers were varied from 10 nm to 20 nm.

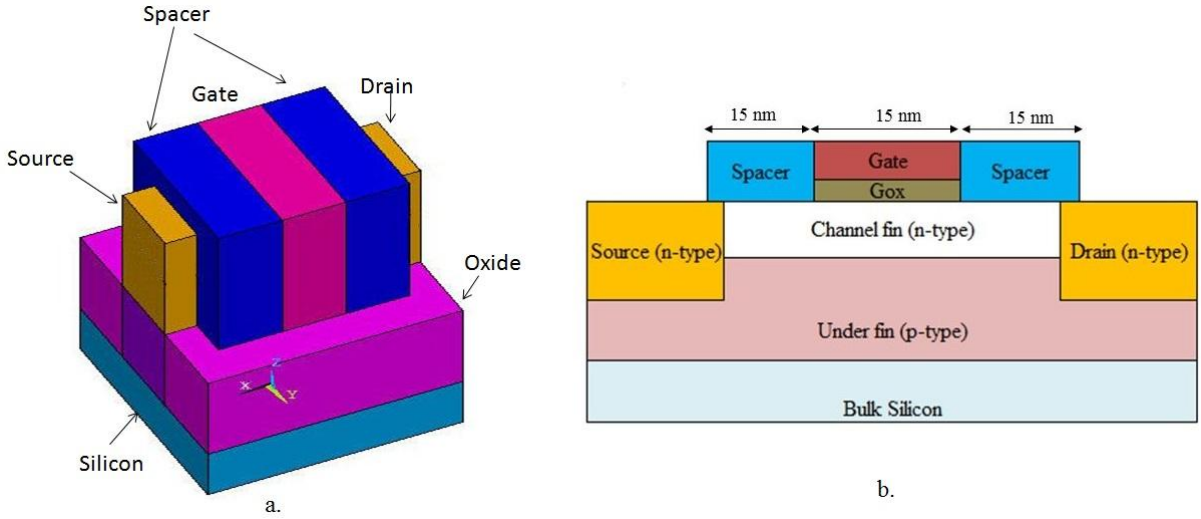


Fig. 3.2: Structure of the Junctionless Accumulation-Mode (JAM) bulk FinFET. (a) 3-D schematic view (b) Vertical cut-plane view

3.4 SIMULATION SETUP AND MODEL CALIBRATION

Silvaco TCAD device simulation tool [3.26] is used to simulate the JAM bulk FinFET. In the setup of device simulation parameters, the carrier mobility is modeled using field dependent mobility model (FLDMOB) [3.27]. Also, the "Shockley–Read–Hall (SRH)" along with Auger recombination model is included for calculating the active carrier lifetime for the precise estimation of performance parameters [3.28]. Newton and Gummel numerical methods have been utilized for the iterative calculations at a temperature of 300K. Contour plot of the distributions of electron density in the channel of the devices operate at ON and OFF states are shown in Fig. 3.3. Electron density of OFF state is plotted when the gate bias is 0V whereas gate bias of 1V is used for ON-state of the device. Other device parameters considered in this simulation model are given in Table 3.1 [3.10]. Few important device parameters used for our device modeling is set as per ITRS 2013 roadmap [3.29].

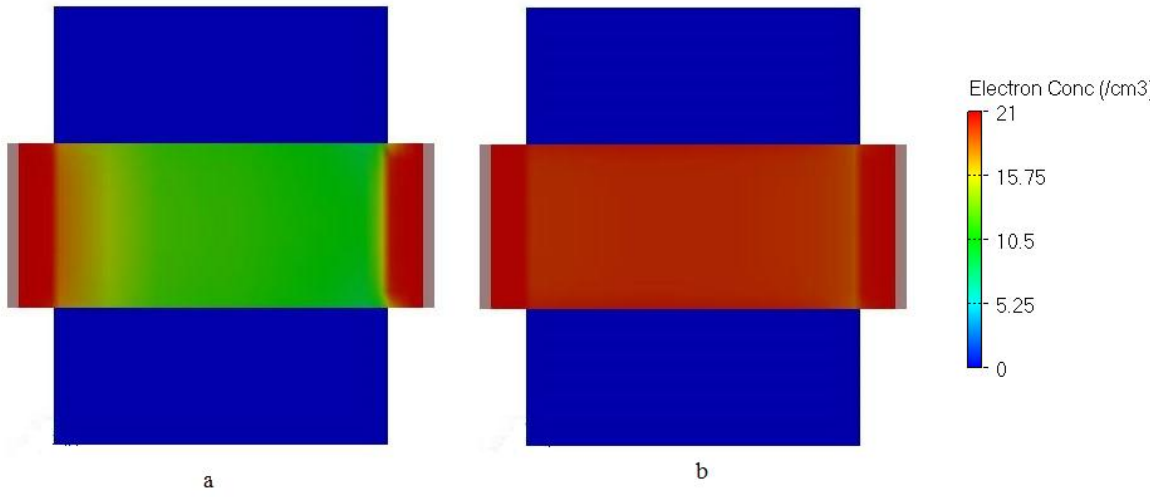


Fig. 3.3: Electron density distributions in the channel of the devices operate at (a) OFF-state (V_{gs} = 0 V) and (b) ON-state (V_{gs} = 1 V)

Table 3.1: Device parameters used for simulation of Junctionless Accumulation Mode bulk FinFET

Parameters	**Value**
Channel-Fin doping	n-type, 1×10^{18} cm^{-3}
Source/Drain doping	n-type, 1×10^{21} cm^{-3}
Under -Fin doping	p-type, 5×10^{17} cm^{-3}
Gate oxide material	HfO_2 (k=22)
Equivalent Oxide Thickness (EOT)	1.25 nm
Gate work function	4.65 eV
Drain Supply Voltage	1V

The simulation model is calibrated with the results published by Choi et. al. [3.10]. Fig. 3.4 demonstrates a qualitative matching of the transfer curves between simulation result and the result published by Choi et. al. [3.10]. Once the matching is achieved for V_{ds}=1V, the same model parameters are employed for other simulations with different spacer material and spacer length.

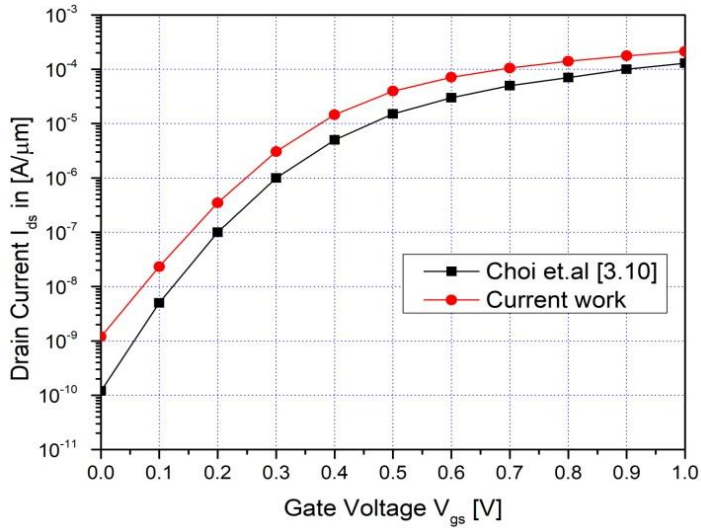


Fig. 3.4: Transfer characteristics comparison between the published results reported in [3.10] and current work for a Drain-to-Source voltage V_{ds}=1V

3.5 SIMULATION RESULTS AND ANALYSIS

It is well established that the electrostatic potential of the lightly doped channel in the underlap region is predominantly sensitive to the fringing field originated from the gate through the spacer since it is not straightforwardly under the control of the gate electric field. An analysis of device performance with and without spacer has been provided to establish the importance of the spacer. The performance of the device with and without using spacer is computed and tabulated in the table 3.2.

Table 3.2: Performance of the device with and without spacer

Gate length 20nm	**I_{ON} Current (mA)**	**I_{OFF} Current (mA)**	**SS (mV/dec)**	**DIBL (mV/V)**	**Transconductance (mmoh)**
Without Spacer	8.58×10^{-2}	4.5×10^{-6}	85	48	0.136
With high-k spacer	1.98×10^{-1}	1.2×10^{-6}	78	43	0.371

All the extracted values reported in Table 3.2 are at V_{ds}=1V, gate length of 20nm, Fin width of 20nm. A spacer of length equals to 15nm with material of *k*-value 22 has been used to study the impact of the spacers on device performance. From the table, it is observed that the major performance parameters of the device such as ON-state current I_{ON}, OFF-

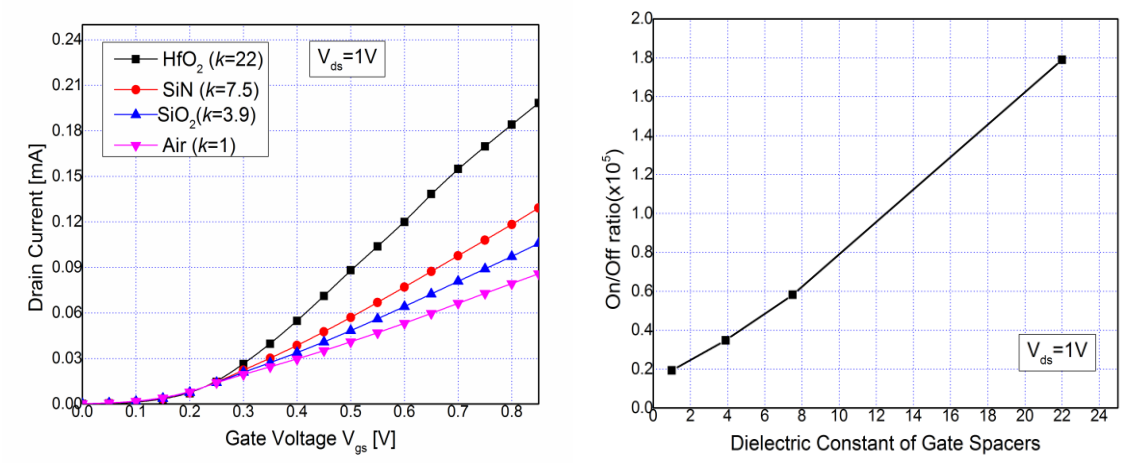
state current I_{OFF}, Subthreshold Slope SS, DIBL and Transconductance (g_m) improved significantly using spacer as compared to a device without spacer. It is worth mentioning that the results are in agreement with previously published results by Pradhan et. al. [3.30].

For MOSFETs having short gate length, one of the most important component contributing to the off-state leakage current is gate induced drain leakage (GIDL) current which is caused by "band-to-band tunneling (BTBT)" in the drain region underside the gate [3.31]. GIDL current caused by "Shockley-Read-Hall recombination (SRH)", "band-to-band tunneling (BTBT)" and "trap-assisted tunneling (TAT)". It is worth mentioning that in order to calculate the GIDL using simulation; these physical models can be considered and switched ON/OFF to identify their contributions and corresponding differences in total current. Though, GIDL is difficult to eliminate, it can be minimized by using graded junction doping, lightly doped channel and increase in underlap [3.31-3.32]. It was previously reported by Gaynor et. al. [3.32] that an optimal I_{OFF} can be achieved with a doping concentration of 10^{18} /cm^3 in the Fin-shaped channel. In this research, a channel doping equals to 10^{18}/cm^3 and an underlap with a graded doping concentration is considered. Because of this large underlap, graded doping profile and channel doping, the effect of GIDL is expected to be minimized. In the following subsections, the most important analog and RF figure of merits are simulated and presented here along with the circuit analysis using the JAM Bulk FinFET.

3.5.1 EFFECT OF SPACER MATERIALS

In order to estimate the effect of spacer materials, different values of dielectric constant of the spacer is considered and simulated. Without spacer condition is considered as air spacer. Fig. 3.5(a) shows simulated I–V characteristic of Junctionless accumulation mode device under study for different spacer materials. From the figure, it is observed that the I_{ds} of the device increases with the increase in the *k* value of the spacer. This is because of the fringing field through the spacer. Spacer material with higher

permittivity (k-value) yields higher I_{ON} as the fringing field become stronger due to the higher permittivity. Fig. 3.5(b) shows the ON/OFF current ratio of the drain current of the device with various k values of the spacer. The ON/OFF ratio of the JAM bulk FinFET is enhanced almost 10 times with increase in dielectric constant (*k*) of spacer due to higher ON-state current. Obtained simulation results establish that high-k gate spacers give better digital performance to the device.



(a) (b)

Fig. 3.5: (a) Variation of I_{ds} in linear scale as a function of V_{gs} with different spacer materials (b) ON/OFF ratio of the drain current (I_{ds}) with different k-values of spacers

To analyze the Analog performance of the device, transconductance (g_m) and transconductance-to-drain-current ratio (g_m/I_{ds}) are calculated for the device under study. The transconductance, g_m, is an important figure-of-merit (FoM) that indicates how well a device converts a voltage to a current. The variation of g_m as a function of gate overdrive voltage V_{gt} ($V_{gt}= V_{gs}–V_{th}$, where V_{th} is the threshold voltage) for different k-values of spacers is shown in Fig.3.6 (a) and variation of transconductance generation factor (TGF) is shown in Fig.3.6(b). The value of V_{th} is calculated to be 0.15V which is extracted as per the constant current definition (10^{-7} A/μm).

The approximate expression for transconductance [3.33] of a FinFET can be written as

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \left(\frac{\mu W}{L} \right).(Q_s - Q_d) \qquad (3.1)$$

where Q_s is the source end charge and Q_d is the drain end charge. W is the width of the device and μ represents the effective mobility of the electrons and L is the length of channel [3.33].

From the above expression, it is evident that g_m is directly proportional to the differences in source and drain end charges. Charge difference increases because of an increase in the electron concentration in the source end and in the drain end. This results from the feedback of the gate sidewall field through the spacer dielectric as reported earlier in [3.34]. For an increase in the permittivity of the spacer, g_m and g_m/I_{ds} increases mainly due to the reason mentioned earlier. This can also be attributed to the intensification of the fringing Electric Field lines at the channel edges through the high-k spacer material causing a reduction in potential barrier thus making an increase in I_{ds}.

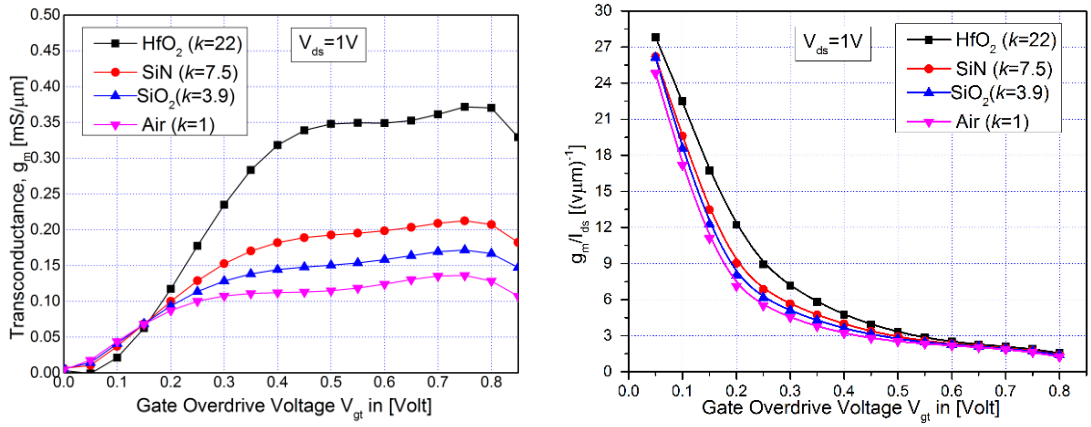
Depending on the 1st order MOS device model one can approximately quantify TGF varying inversely to overdrive voltage [3.35] and is expressed by

$$\frac{g_m}{I_{ds}} \cong \frac{\alpha}{V_{gs} - V_{th}} \qquad (3.2)$$

where α is the power law co-efficient, which indicates TGF is maximum in the weak-inversion region and gradually decreases from maximum upper limit (lowest power) with increase in $(V_{gs}-V_{th})$. Therefore findings in this work are in accordance with that of reported earlier [3.35- 3.36].

From the Fig. 3.5(a), it is clear that a considerable improvement in g_m is observed for a device having high-k spacer. As the transconductance (g_m) represents the gain specified by the device and the drain current (I_{ds}) indicates the power dissipation to attain the gain, the ratio is viewed as the obtainable gain per unit value of power dissipation. So, it is desirable to obtain the higher g_m/I_{ds} ratio for better analog performance of the device.

Fig. 3.6(b) indicates that higher g_m/I_{ds} may be obtained by using higher k-value of the spacer in the region of moderate gate bias.



(a) (b)

Fig. 3.6: (a) Variation of g_m as a function of V_{gt} for JAM bulk FinFET with different spacer materials at V_{ds} = 1.0 V. (b) Variation of g_m/I_{ds} as a function of V_{gt} for JAM bulk FinFET with different spacer materials at V_{ds} = 1.0 V.

The simulation and analysis of the RF performance of the Junctionless Accumulation Mode (JAM) bulk FinFET is carried out in terms of the cut-off frequency f_T and the maximum frequency of oscillation f_{max}. The simplified expressions for f_T and f_{max} are reported in [3.37-3.38] and are used for the calculation here.

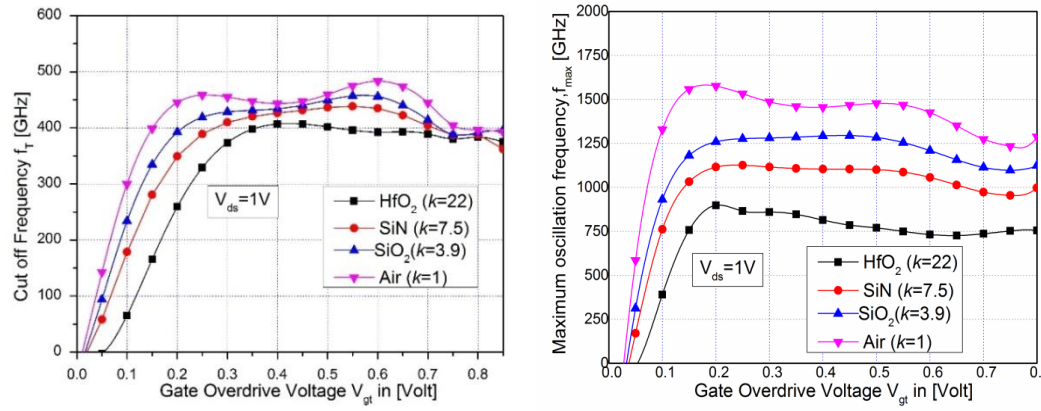
$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \qquad (3.3)$$

where g_m, C_{gs}, and C_{gd} are the transconductance, the gate-to-source capacitance and gate-to-drain capacitance respectively.

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s + R_i + R_g)(g_{ds} + g_m \frac{C_{gd}}{C_{gs}})}} \qquad (3.4)$$

where R_g, R_s, and R_i are the gate, source, and channel resistances, respectively.

To calculate and analyze these parameters (f_T & f_{max}), the values of the intrinsic capacitances (C_{gs} and C_{gd}) as a function of gate overdrive voltage, V_{gt} are extracted. These intrinsic gate capacitances are very important parameters for calculations of RF figure-of-merits. These intrinsic gate capacitances are extracted from small signal AC device simulation at an operating frequency of 1 MHz. It has been verified that for triple-gate FinFETs, the extrinsic gate capacitances are the main parameters responsible of the limited cut-off frequencies [3.39]. These extrinsic gate capacitance values are then employed in the calculation using equations (3.3) & (3.4).



(a) (b)

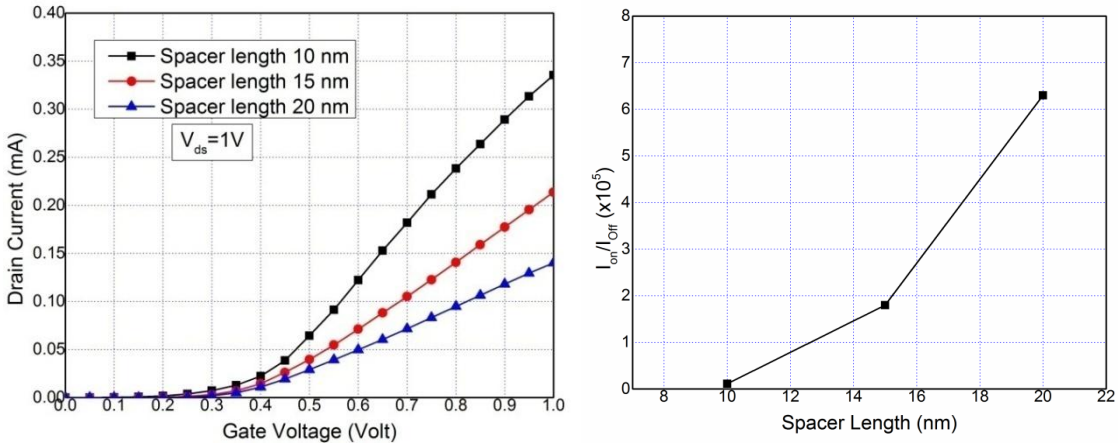
Fig. 3.7: (a) Variation of f_T as a function of (V_{gt}) for JAM bulk FinFET with different spacer materials at V_{ds} =1.0 V (b) Variation of f_{max} as a function of V_{gt} for JAM bulk FinFET with different spacer materials at V_{ds} = 1.0 V

Fig. 3.7(a) shows the variation of f_T as a function of gate overdrive voltage, V_{gt} for V_{ds} = 1.0 V for different dielectric constants (k) of the spacers. It can be observed from the Fig. 3.6(a) that f_T decreases as k-value of the spacer increases. This is because the device with HfO_2 (dielectric constant=22) as spacer has highest gate capacitance in comparison to devices with spacers of lower k values due to higher fringing field lines of high-k spacer dielectric. The device with no spacer presents superior f_T compared with other devices with higher k values, due to its considerably lower value of gate capacitance. The variation of f_{max} with different spacer material is plotted in Fig. 3.7(b). As shown in Fig. 3.7(b), the device with

spacer having low k value exhibits higher f_{max} compared to the device with spacer having high-k value.

3.5.2 EFFECT OF SPACER LENGTH

For overlap device architecture, high-k spacer material has significant role in modulation of the charge transport dynamics in the overlap region. So, length of the spacer region characterizes the device performance. As the drive current and fringe capacitance has an important role in anticipating the device performance for its circuit applications, the impact of high-k spacer length on drain current (I_{ds}) is examined. For the following simulations, device with HfO_2 (k=22) as spacer material is used and length of the spacer region is varied from 10 nm to 20 nm.



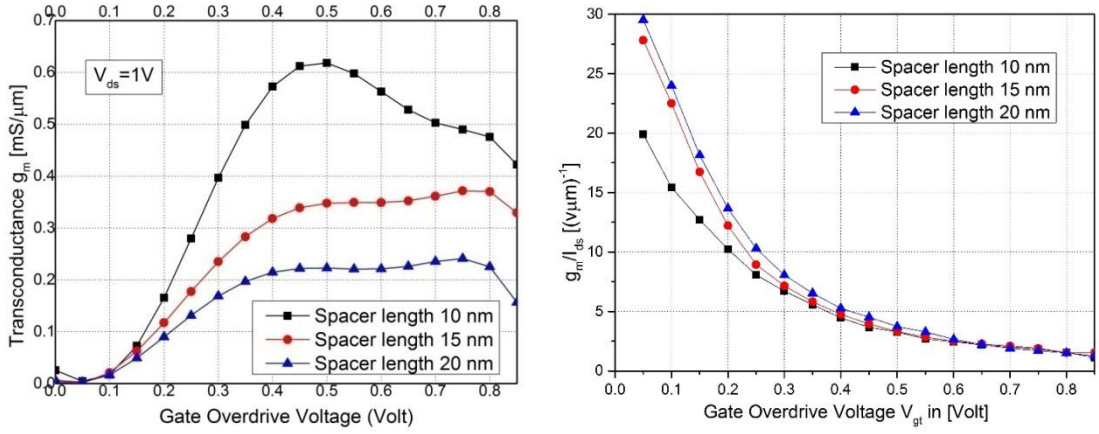
(a) (b)

Fig.3.8. (a) Variation of I_{ds} in linear scale as a function of V_{gs} with different spacer length (b) ON/OFF ratio of the drain current (I_{ds}) for JAM bulk FinFET with different spacer length

Fig. 3.8(a) shows the characteristics curves of gate voltage (V_{gs}) vs. drain current (I_{ds}) for three different spacer lengths varying from 10 nm to 20 nm. From the Fig. 3.8(a), it is observed that drain current of the device increase with decrease in spacer length. This result attributes to the decrease in series resistance of the device due to decrease in spacer length. In Fig.3.8 (b), the ON-to-OFF current ratio (I_{ON}/I_{OFF}) is plotted for different spacer length. With an increase in spacer length, I_{ON}/I_{OFF} ratio increases for the device under study. As the spacer length increase, the on-current of the

device decrease because of increase in channel resistance, but OFF-current of the device also decrease. Therefore, the I_{ON}/I_{OFF} ratio of drain current for the device increases with increase in spacer length.

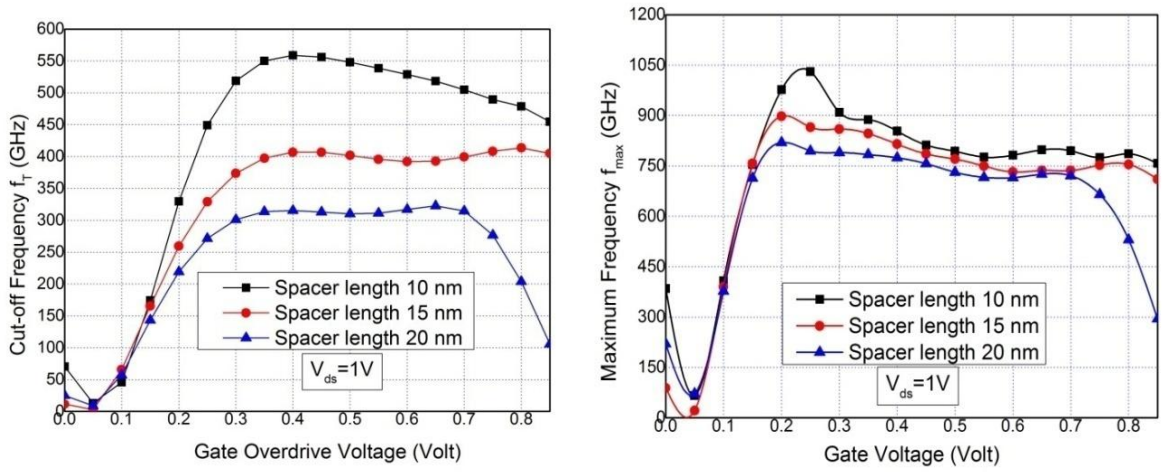
Variation of transconductance (g_m) and transconductance generation factor (g_m/I_{ds}) as a function of gate overdrive voltage (V_{gt}) is shown in Fig. 3.9. From Fig. 3.9(a), it is understood that transconductance of the device increases with decrease in spacer length. From equation (3.1), it is also found that g_m is inversely proportional to the length of channel (L). An increase in the spacer length therefore causes a boost in the effective channel length of the device. As a result g_m decreases with increase in the spacer length. The transconductance generation factor or transconductance-to-drive current ratio (g_m/I_{ds}) at V_{ds} = 1.0 V as a function of V_{gt} for JAM bulk FinFET with different spacer lengths is shown in Fig. 3.9(b). The parameter g_m/I_{ds} stands for the obtainable gain per unit value of power dissipation. g_m/I_{ds} is in upper limit in the weak inversion region and it decreases with increasing drain current in the strong inversion region [3.35-3.36]. Moreover, reduction in the spacer length causes drop in g_m/I_{ds} due to increase in short channel effects (SCEs). It is because the decrease in the spacer length causes reduction in the effective channel length hence increases the detrimental SCEs. Furthermore, I_{ds} also decrease with an increase in the spacer length.



(a) (b)

Fig. 3.9: (a) Variation of g_m as a function of V_{gt} for JAM bulk FinFET with different spacer length at V_{ds} = 1.0 V. (b) Variation of g_m/I_{ds} with V_{gt} for JAM bulk FinFET with different spacer length at V_{ds} = 1.0 V.

Fig. 3.10 shows the variation of f_T and f_{max} with increase in gate overdrive voltage (V_{gt}) for different spacer length. With spacer length reduction, f_T increase following the trend of transconductance (g_m) as shown in Fig. 3.10(a). From an application point of view in Analog circuits and to get higher f_{max}, not only better g_m is wanted, but also elevated g_m/C_{gs} and C_{gs}/C_{gd} ratios are also desirable. From our simulation results, it is noticed that with decrease in spacer length, g_m increase which it turn increase the f_{max} as a combined effect. Therefore, f_T and f_{max} of the device increase for shorter spacer length indicating that RF performances can be improved by scaling down the spacer length. Variation of f_{max} as a function of gate overdrive voltage (V_{gt}) for JAM bulk FinFET with different spacer length is shown in Fig.3.10 (b).



(a) (b)

Fig. 3.10: (a) Variation of f_T as a function of V_{gt} for JAM bulk FinFET with different spacer length at V_{ds} =1.0 V (b) Variation of f_{max} as a function of V_{gt} for JAM bulk FinFET with different spacer length at V_{ds} = 1.0 V

3.5.3 CIRCUIT PERFORMANCE ANALYSIS

In this section, the circuit performance of JAM Bulk FinFET device is investigated and analyzed for both the analog and digital considerations. In Fig. 3.11, the circuit level performance of JAM Bulk FinFET device on resistive load inverter has been provided in order to evaluate the impact of the spacer length through the transient response. The timing characteristics

of the input and output signal is shown in Fig. 3.11 along with high-to-low delay time (τ_{HL}) values indicated. τ_{HL} is defined as the time interval between 50% of the input voltage and the output voltage of the transient response. As input signal changes its value from low to high voltage, the driver device starts to turn "ON". The circuit delay τ_{HL} depends primarily on the drive current and load capacitance [3.38]. As discussed in the previous sections, drive current increases with increase in spacer length. Hence as spacer length increases, circuit delay becomes superior, which is in agreement with the findings of Sachid et al. [3.40].

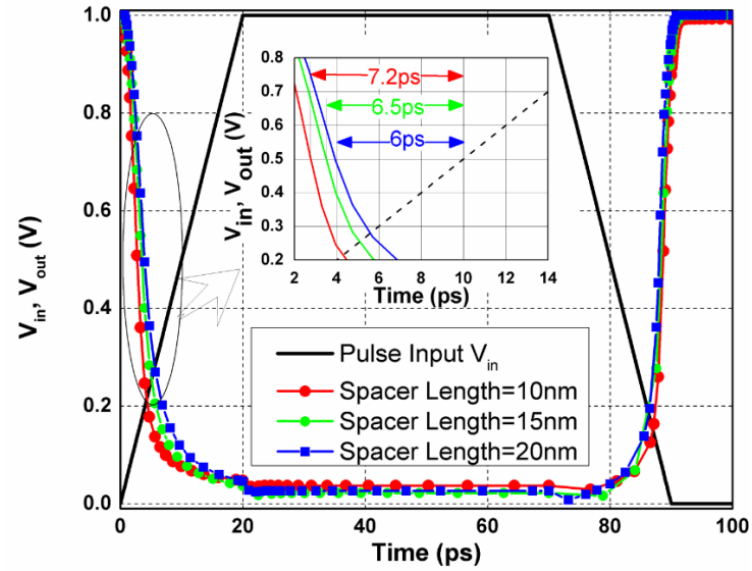


Fig. 3.11: Timing characteristics of JAM Bulk FinFET device based restive load inverter circuits for different spacer length. [Inset] extracted high-to-low delay time (τ_{HL}) for different spacer lengths.

Moreover, for a channel with low doping, the underlap regions are not under the direct control of the "Gate Electric Fields" and the electrostatics in these regions are susceptible to the fringing fields coming from the gate through the spacer. Therefore, the improvement in circuit delay with increase in spacer length can be endorsed to the drain current improvements due to the gate-sidewall induced fringing field and also due to the enhancement in the drive current I_{ON}.

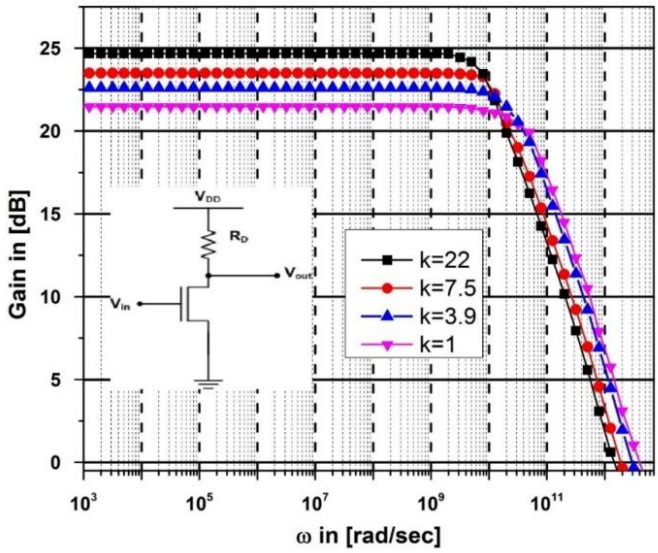


Fig. 3.12: Impact of the different k values of spacer materials on frequency response characteristics of resistive load common source amplifier using JAM Bulk FinFET device.

The circuit performance of resistive load common source amplifier using Junctionless accumulation mode Bulk FinFET device has been analyzed for assessing the impact of spacer material on frequency response. Fig. 3.12. shows the variation of gain with ω (frequency in rad/sec) in the frequency response characteristics of common source amplifier using the device for different values of spacer dielectric constant. The gain of a common source amplifier [3.41] is expressed by

$$\frac{V_{out}}{V_{in}} = \frac{(sC_{gd} - g_m)R_L}{R_s R_L C_{gd} C_{gs} s^2 + [R_s(1+g_m R_L)C_{gd} + R_s C_{gs} + R_L C_{gd}]s + 1} \qquad (3.5)$$

The multiplication of low frequency gain by Miller capacitance C_{gd} dominates the variation of gain as a function of frequency. At low frequencies, the voltage gain is primarily controlled by the g_m and effective output impedance (R_L) of the device given by

$$A_{v,LF} = g_m R_L \qquad (3.6)$$

In previous section it has been already shown that g_m increases with increase in k value. Therefore, gain increases with k as shown in Fig. 3.12.

This enhancement in g_m is caused primarily by the inversion charge modulation by the gate sidewall fringing fields in the underlap regions as described by Zhao et al. [3.21]. In a common-source amplifier, for high frequencies, C_{gd} looks much bigger than it really is so that its effect on bandwidth is multiplied by the voltage gain, known as Miller effect. At higher frequencies, due to the low-impedance feed forward path provided by the Miller capacitance, the magnitude of the poles in (3.5) decreases which causes a drop of the voltage gain with frequency. It is clear from Fig. 3.12 that as k values of spacer increases, gain bandwidth (GBW) product decreases, which can be primarily attributed by the enhancement of Miller capacitance C_{gd}.

3.6 CONCLUSION

In this work, the impact of high-k spacer materials and spacer lengths on device and circuit performance has been evaluated for Analog and RF applications for the JAM bulk FinFET. An assessment is made for the performance of the device with gate spacers having different k values. Then the performance of the device having high-k gate spacer is examined and compared for different spacer length. From the analysis, it is observed that the digital and analog performance of the device improves with high-k gate spacers. However, using high-k spacer material, the device exhibits lower f_T and f_{max} in comparison to the device with spacers having lower k-value. It is found that increase in spacer length corresponds to improvement in SS and DIBL and increase in V_{th} (lower V_{th} roll-off) but simulation results also suggest that RF/analog performance of the device with spacer having high-k dielectric can be improved by reducing the spacer length. So, a trade-off is required to optimize the device performance for analog/RF applications. Common source amplifier using junctionless accumulation mode Bulk FinFET device has been analyzed for assessing the impact of spacer material on frequency response. It is understood that the gain of the circuit improves with devices having high-k gate spacers. Current work presents valuable design guidelines in the performance of Junctionless Accumulation Mode Bulk FinFET device with optimal spacer region engineering.

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Chapter 4

Impact of Device Dimensions on Performance of Junctionless Accumulation Mode Bulk FinFET

4.1 INTRODUCTION

In recent years, lots of interests has been shown to the search of advanced transistor architectures which helps to extend MOSFET downscaling into the nanometer regime [4.1-4.2]. Various Short Channel Effects (SCEs) become significant when the gate control on the channel region is affected by electric field lines from source to drain. Various approaches have been explored and proposed to reduce the impact of SCEs on threshold voltage roll-off, drain-induced barrier lowering, sub threshold swing etc. [4.2]. In a short-channel device, it is also very difficult to form an ultra-sharp source and drain junctions and imposes extreme conditions on doping techniques and on thermal budget. Recently, Junctionless (JL) MOSFETs have been proposed and fabricated to evade these fabrications issues [4.3-4.6]. Junctionless FinFET is one of the emerging CMOS devices that use a novel architecture to efficiently control the SCEs. Recently, n-channel Junctionless accumulation mode (JAM) FinFETs built on Si bulk is developed and demonstrated for the first time [4.7]. As discussed in the previous chapter, bulk FinFET has also caught attention because of its low-cost process, better heat dissipation capability and compatibility with standard bulk CMOS technology. The main requirement of a high-performance Junctionless FET is the formation of a thin and narrow channel which can allow full depletion of carriers using a suitable gate work-function when the device is turned OFF [4.8]. In order to obtain suitable threshold voltage (V_{th}), low SS and higher I_{ON}/I_{OFF}, lower channel doping is preferred. From the experimental data available in literature, it is understood that if the channel doping increase, SS and DIBL increase along with decrease in I_{ON} and increase in I_{OFF} [4.9]. It has been proved that channel doping of the order of 10^{18} helps by providing better conduction [4.10]. Threshold voltage sensitivity also has been lowered with the reduction in channel doping [4.10]. The lightly doped channel region of accumulation-mode MOSFETs has a high resistance. Therefore, a sufficiently large gate voltage must be applied to create an accumulation layer in the silicon beneath the gate oxide. This accumulation layer having

high carrier concentration drives significant current through the device [4.4]. Therefore, in a JAM device, the presence of an initial energy barrier is observed in contrast to a JL device where there is no energy barrier between the source and the drain because of the same doping profile [4.7]. Basic difference between Junctionless MOSFET and Junctionless Accumulation Mode MOSFET in terms of doping profile is already shown in Chapter 2 [Fig. 2.15].

It is well established from the published works that JL FETs have stronger immunity against SCEs compared with inversion mode FETs. Better reliability of Junctionless FETs compared with inversion-mode FETs is also experimentally verified. This structure has no p-n junctions, operates in accumulation mode. Unlike the conventional short-channel MOSFET, the Junctionless MOSFETs eliminate the requirement to form p-n junctions thus reducing the process steps. Thus, the Junctionless MOSFET can surmount many fabrication related issues like doping techniques and thermal budget. The principle of operation of the Junctionless transistor has recently been established through simulations and fabrication by several research groups [4.11-4.12]. As the feature size of devices within an integrated circuit decreases, the density of the transistors as well as the performance of the devices such as speed increases, leading towards the concept of System-on-Chip (SoC) which integrates all the elements of a system (Digital, Analog and RF) within the single chip. Most chip manufacturing foundries and companies working in electronic design automation are giving more emphasis and investment on the 3D FinFET technology. As the performance of the FinFET as well as FinFET based circuits depends on geometry of the FinFET structure [4.13-4.17], it is essential to discuss the impact of the dimensions of Fin geometry on the analog/RF performance parameters for using it in mixed-signal SoC applications. Recently, Kranti et al. [4.17] provides the effect of the variation of Fin aspect ratio and optimal Fin spacing to achieve higher RF figure-of-merits of inversion-mode FinFET. The current chapter is concerned about the investigation of analog/RF performance of JAM bulk FinFET for varying

Fin width. The effect of the variation of the Fin dimension on the RF/analog performance of the device has been reported to find their applicability in analog as well as RF applications.

4.2 DEVICE STRUCTURE AND SIMULATION MODEL

The Fig. 4.1 shows the Junctionless Accumulation-Mode (JAM) bulk FinFET structure along with gate spacers for n-channel operation.

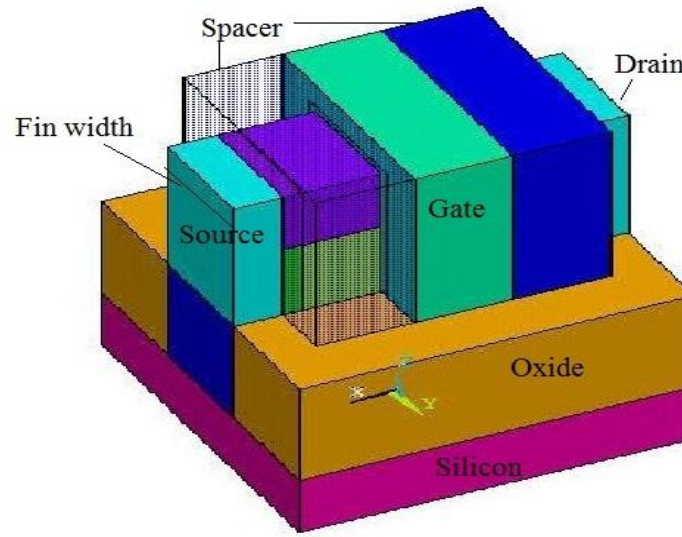

Fig.4.1: 3D Schematic view of the JAM bulk FinFET with gate spacers.

An n-type Junctionless transistor uses n+ doping for all the source, channel, and drain region. In current study additional source and drain doping concentrations are used keeping the channel with moderate doping to overcome the source/drain series resistance. Primary device dimensions and other device parameters are listed in Table 3.1. Doping concentrations of source and drain region are taken as $10^{21}/cm^3$ where as that of the channel region is considered as $10^{18}/cm^3$. Junctionless transistor should have same doping profile throughout the source, drain and channel regions. However, in a Junctionless transistor low doping profile is required to achieve suitable threshold voltage, low SS and high I_{ON}/I_{OFF} ratio. However, this adversely increases the S/D series resistance. As a remedy, many researchers have proposed and used additional source and drain doping in order to decrease the parasitic resistance [4.7, 4.18, 4.19]. These transistors

are known as Junctionless accumulation mode FET with additional doping in S/D region [4.7-4.8, 4.20-4.21]. Therefore, in this work, additional source/drain doping profile has been considered. Molybdenum (Mo) having work function equals to 4.65 eV is used as gate. The simulated devices employs HfO_2 as gate oxide material with an "equivalent oxide thickness (EOT)" of 1.0 nm, a gate length (L_g) of 20 nm, a Fin height (H_{fin}) of 20 nm, a Fin width (W_{fin}) of 20 nm. Among other device parameters, spacer length is considered equals to 15 nm with a source/drain to spacers overlap length of 3 nm. High-k spacers (k=22) are used as it enhances the device performance significantly [4.7]. Fin width (W_{fin}) is an important parameter for device performance optimization. Therefore, Fin width of the device is varied from 10nm to 20nm and performance parameters are calculated.

In this study, Silvaco TCAD [4.22] device simulation tool is used to simulate the JAM bulk FinFET. ATLAS 3-D numerical simulations have been performed to investigate the electrical characteristics of the junctionless accumulation-mode bulk transistors with various channel width. Rectangular Fin shape has been employed in this work. As Fin shape variations have an impact on the device performance, many researchers have studied the performance of the device considering realistic Fin shape [4.13, 4.23-4.25]. However, it is worth mentioning that though the consideration of realistic Fin shape in the device modelling results in some variation in the simulated data, that variation does not have lot of impact on the common trend of the findings presented here. In this chapter, the overall trends of the performance variation with Fin width is highlighted rather than the accurate values of the different performance parameters. The simulation employs the Fermi-Dirac distribution model without impact ionization. For the purpose of device simulation, the mobility is modeled using "electric field dependent mobility model (FLDMOB)". Also, the "Shockley–Read–Hall (SRH)" along with "Auger" recombination model is included for considering the lifetime of active carrier for the accurate assessment of performance parameters. "Newton" and "Gummel" numerical method have been utilized

for the iterative calculations at a temperature of 300 K. Other device parameters [4.7] used in this simulation are given in Table 4.1

Table 4.1: Basic device parameters considered for Junctionless Accumulation Mode bulk FinFET

Parameter	**Value**
Fin Width (W_{fin})	10nm-20 nm
Fin Height (H_{fin})	20 nm
Gate Length (L_g)	20 nm
Gate oxide material	HfO2 (k=22)
Equivalent Oxide Thickness (EOT)	1.0 nm
Gate work function (W_F)	4.65 eV
Drain Supply Voltage (V_{ds})	0.9V

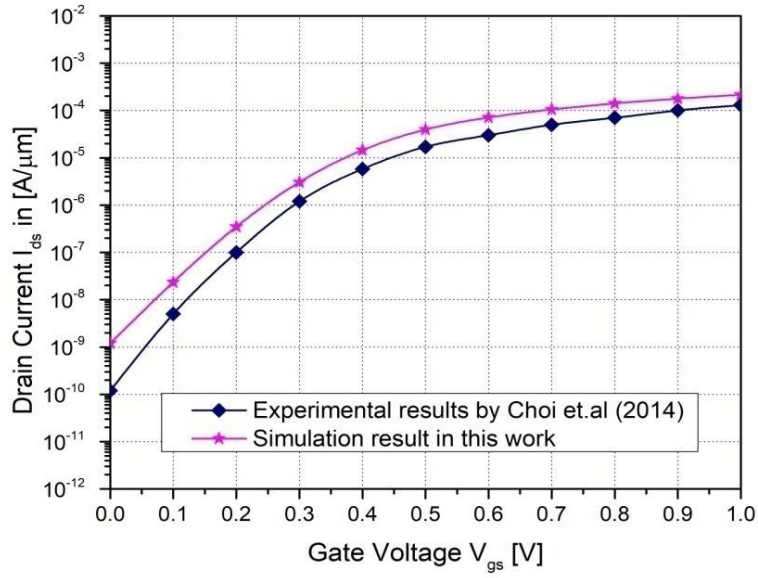

Fig.4.2: Transfer characteristics comparison between the published results reported in [Choi et.al.] and current work for a Drain-to-source voltage V_{ds}=1V

The simulation model is calibrated with the results published by Choi et. al. [4.7] varying the mobility model parameters. Fig. 4.2 demonstrates a qualitative matching of the transfer curves between obtained simulation results and the results published by Choi et. al. [4.7]. Choi et. al. has considered the quantum confinement (by choosing density gradient model) effect on the device performance in their study, which leads to the slight

difference in the I_d-V_{gs} curve. However, it is worth mentioning that the effects of quantum confinement are minimal in JLTs as compared to the conventional MOSFETs [4.26]. Once the matching is achieved between the obtained simulation results with results of Choi et al.[4.7] for V_{ds}=1V, the same model parameters is employed for other simulations with different Fin width. Few important device parameters used for the device modelling here is set as per ITRS 2013 roadmap [4.27].

4.3 RESULTS & DISCUSSIONS

Fig. 4.3 shows the current density distribution in the channel as the gate voltage (V_{gs}) equals to 0V, 0.3V, 0.6V, and 0.9 V respectively. The Fin width (W_{fin}) is an important scaling parameter for FinFETs because of its strong impact on electrostatic integrity. Fig. 4.4 shows the measured drain current (I_{ds}) plotted against gate voltage (V_{gs}) for JAM bulk FinFET with various Fin widths and ON/OFF current ration of the device for different Fin widths. From Fig. 4.4(a) it is understood that drain current (I_{ds}) is increasing with the increase in Fin width and obtained maximum values at Fin width of 20 nm. As the Fin becomes wider, the effective channel width also increases; increasing the overall carrier mobility for n-FinFETs [4.28].

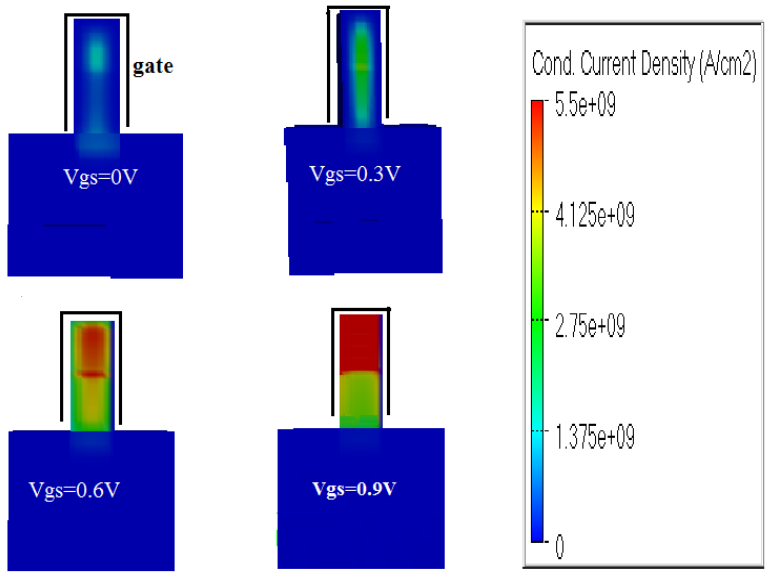

Fig. 4.3: Current density distribution in the vertical direction of the channel for different

gate voltages

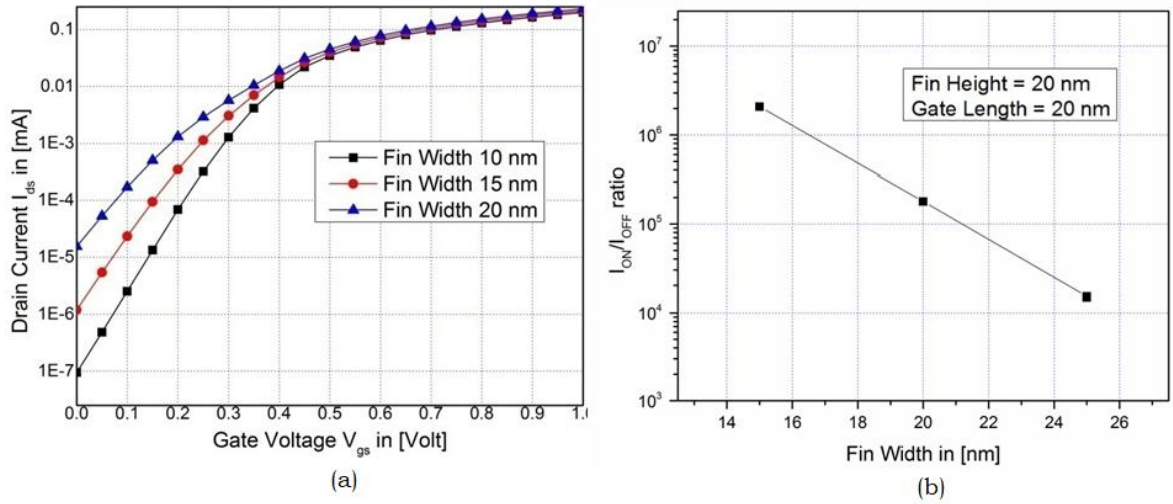

Fig.4.4: (a) Variation of I_{ds} as a function of V_{gs} for JAM bulk FinFET with different Fin width at V_{ds} = 0.9 V. (b) ON/OFF ratio of Drain current (I_{ds}) of JAM bulk FinFET for different Fin width

In the work published by Lederer et al. [4.29] and Kilchytska et al. [4.30], it is reported that a lower electron mobility for the sides than the top of the FinFET due to different crystallographic orientation for the lateral (<110> Si orientation) and top (<100> Si orientation) channels (Fig. 4 of Lederer et al. 2005). Moreover, lateral conduction is the chief contributor of the current in a FinFET having thin channel width. Therefore, it is expected that as effective channel width increases with increase in Fin width, top conduction also becomes significant, ensuing in a boost in the drain current intensity. Therefore the drain current of the device also increases with increased Fin width. However, as Fin width increases, device needs lower gate voltages to turn ON the device due to reduction in gate-controllability, resulting in a decrease in threshold voltage V_{th}, increase in subthreshold slope and increase in the short-channel effects [4.31-4.32]. This obviously indicates a trade-off between current intensity and short-channel effects.

Fig. 4.4(b) shows the drain current ON/OFF ratio of JAM FinFET for various Fin widths. Fig. 4.4(b) indicates that I_{ON}/I_{OFF} ratio increases with decrease of Fin width. It is worth mentioning that I_{ON} of the device increases with increase in Fin width at the cost of increase in the leakage current due

to increase in the gate area. This results in decrease in the I_{ON}/I_{OFF} ratio. This indicates that small Fin width is desirable in order to obtain higher I_{ON}/I_{OFF} ratio. These findings show the further downscaling potential of the JAM FinFET.

The dependence of significant parameters like SS, DIBL and threshold voltage (V_{th}) on channel dimensions like gate length and Fin width for different spacer lengths has been summarized. Fig. 4.5 (a) – Fig. 4.5(c) plots the variation of SS, DIBL and threshold voltage (V_{th}) on gate length (15-25nm) for different spacer lengths (10-20 nm). Fig. 4.5 (d) – Fig. 4.5(f) plots the variation of SS, DIBL and threshold voltage (V_{th}) on Fin width (15-25nm) for different spacer lengths (10-20nm).

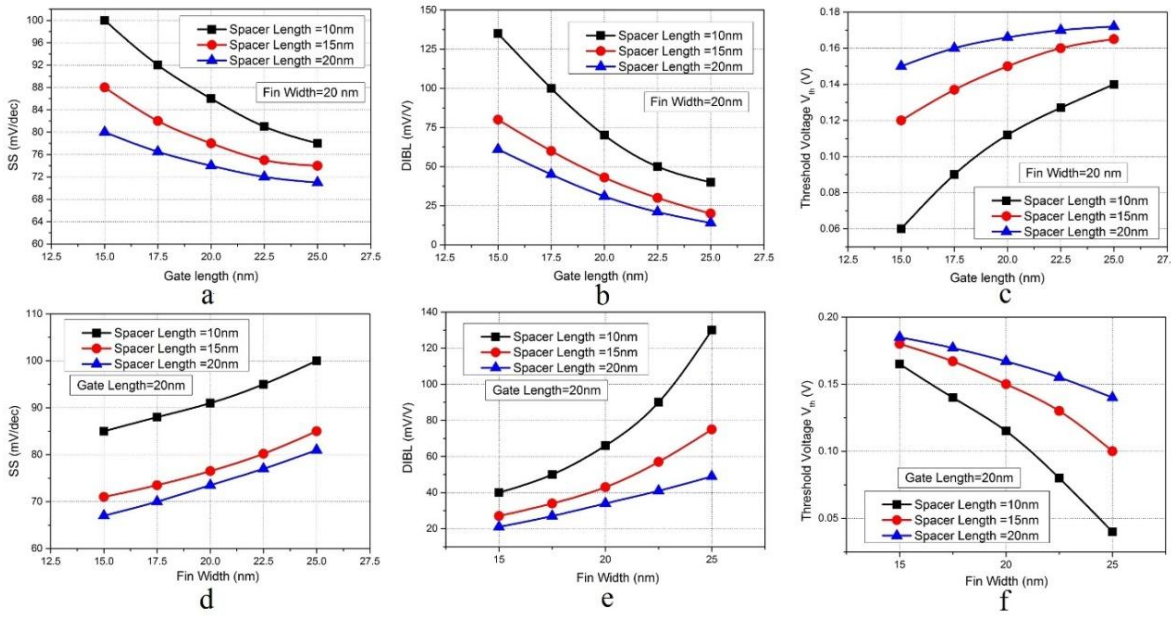

Fig. 4.5: Short-channel performance of JAM Bulk FinFET devices

(a-c). Variation of SS, DIBL and V_{th} with Gate length for different spacer lengths.

(d-f). Variation of SS, DIBL and Vth with Fin width for different spacer lengths

It is apparent from Fig. 4.5 (a-c) that for a given spacer length, SS and DIBL of the device decreases with increase in gate length whereas threshold voltage (V_{th}) increases with increase in gate lengths. Moreover, from Fig. 4.5 (a-c), it is clear that increase in spacer length corresponds to improvement in SS and DIBL and increase in V_{th} (lower V_{th} roll-off). The findings are in accordance to that earlier reported by [4.33-4.34].

It is observed from Fig. 4.5 (d-f), for a given gate length, increase in Fin width results in reduction of SS and DIBL with a decrease in threshold voltage which can be primarily attributed to the decreased gate control as a result of increase in the Fin width. It also may be noted in Fig. 4.5 (d-f) that increase in spacer length helps in improving the digital performance (SS, DIBL and V_{th} roll-off) of the device. These findings match well with that earlier reported in [4.35-4.37].

4.3.1 ANALOG PERFORMANCE ANALYSIS

In order to understand the impact of Fin width on f_T and f_{max} for JAM bulk FinFET, different analog/RF metrics such as transconductance (g_m), transconductance-to-drain-current ratio (g_m/I_{ds}) and total gate capacitance (C_{gg}) for the device under study are evaluated. Transconductance (g_m) is considered as one of the most significant parameters for assessment of the analog performance of a device.

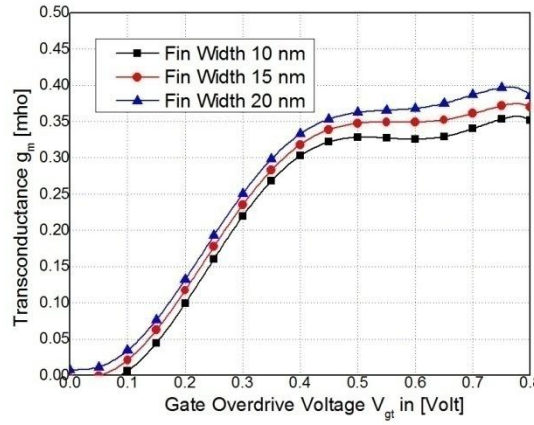

Fig. 4.6: Variation of g_m as a function of gate-overdrive voltage, V_{gt} for JAM FinFET for various Fin width at V_{ds} = 0.9 V.

Fig. 4.6 shows the variation of transconductance (g_m) with increase in gate overdrive voltage, V_{gt} (V_{gt}= V_{gs}–V_{th}, where V_{th} stands for the threshold voltage) for different Fin width. In the g_m vs. V_{gt} curve a kink is observed at higher gate overdrive voltage. It is identified that Fully-depleted (FD) SOI devices are normally free from "kink effect" because of the unfeasibility to collect majority carriers in the body that would affect the threshold voltage

in a FDSOI device [4.38]. However, the interface coupling effect, inherent to FDSOI devices, can affect their operation where many parameters (trans-conductance, threshold voltage, interface-trap response etc.) of one channel are insidiously affected by the opposite gate voltage (at the buried oxide), thus resulting in a current voltage kink still exists in the strong inversion region. Moreover, it is observed that parasitic bipolar effect still happens in a FDSOI device as long as the drain voltage is high enough [4.39]. This argument is supported by the findings of a recently published result by Fenouillet-Beranger et al. [4.40] where a parasitic bipolar effect in ultra-thin FD SOI MOSFETS (thickness = 10 nm) is reported. If the minority carrier lifetime in the silicon film is high enough, the parasitic bipolar effect can reinforce the kink observed in g_m versus gate-overdrive voltage (V_{gt}) characteristics [4.38]. Furthermore, Lederer et al. [2005] has also reported the appearance of the second kink for FinFET with large Fin width due to the effect of gate induced floating body effect. Additional technology optimization is required to reduce this kink.

As the transconductance (g_m) represents the gain given by the device and the drain current (I_{ds}) indicates the power dissipation to obtain the gain, the ratio is viewed as the offered gain per unit power dissipation. So, it is desirable to obtain the higher g_m/I_{ds} ratio for better analog performance of the device. The variation of "transconductance generation factor (g_m/I_{ds})" is shown in Fig. 4.7. In weak inversion region, the Subthreshold Slope (SS) and g_m/I_{ds} ratio can approximately be related as

$$SS \approx \ln(10) \cdot \left(\frac{g_m}{I_{ds}} \right) \qquad (4.1)$$

From the fig. 4.7 for V_{gt}=0.1V, the SS obtained for different Fin widths are 28.5, 20.5 and 14 mv/dec, resulting in the Subthreshold Slope (SS) equals to 80.7 mv/dec, 112.2 mv/dec and 164.3 mv/dec. It also indicates that an increase in the Fin width worsens the SS, which is in agreement with the previous results obtained by Seo et al. [4.31]. From the simulation results it is understood that higher g_m/I_{ds} is available with thinner Fin of the

device. Though the degradation in drive current and transconductance is observed with Fin width scaling, g_m/I_{ds} is seen to be improved for near threshold region.

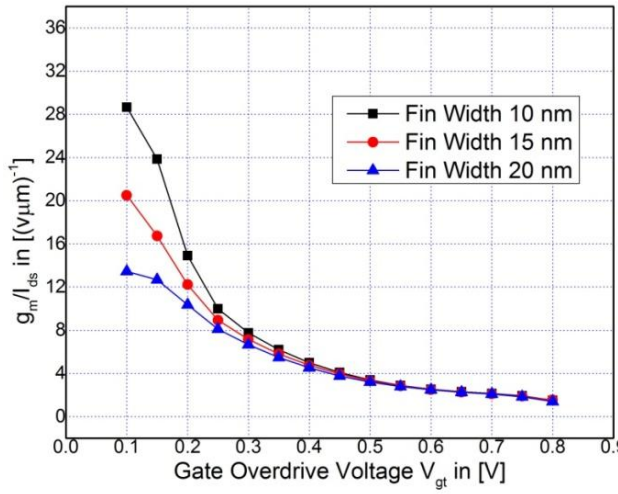

Fig. 4.7: Variation of g_m/I_{ds} as a function of gate-overdrive voltage, V_{gt} for JAM FinFET for different Fin Width at V_{ds} = 0.9V

4.3.2 RF PERFORMANCE ANALYSIS

For the device in RF circuits, the cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) are main figures-of-merits (FOMs), which define the unity gain frequencies for current and power respectively. The transconductance to gate-source and gate-drain capacitances C_{gs}, C_{gd} are related to both f_T and f_{max}. In case of f_{max}, the gate, source and channel resistances are also considered. The cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}), may be written as [4.41-4.42]:

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{4.2}$$

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4\cdot(R_s + R_i + R_g)(g_{ds} + g_m \frac{C_{gd}}{C_{gs}})}} \tag{4.3}$$

where g_m, C_{gs}, and C_{gd}, R_g, R_s, and R_i are the transconductance, the gate-to-source capacitance, gate-to-drain capacitance, the gate resistance, source resistance and channel resistances respectively.

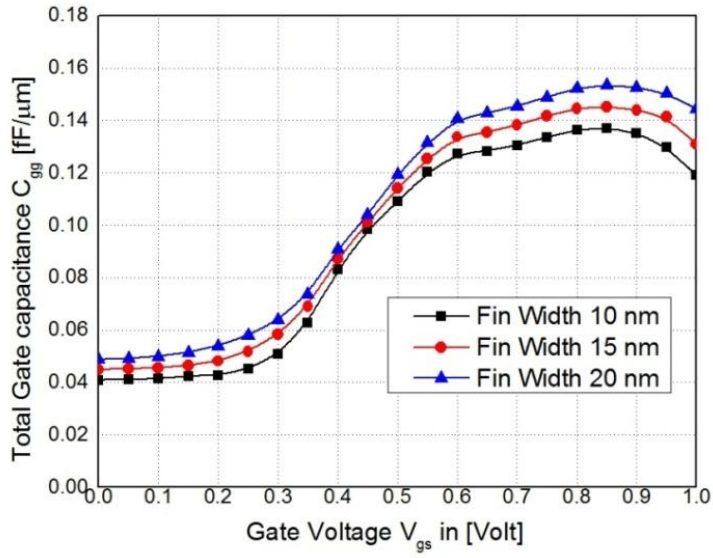

Fig. 4.8: Variation of Gate Capacitance, C_{gg} (=C_{gd}+C_{gs}) as a function of V_{gs} for JAM bulk FinFET for different Fin width at V_{ds} = 0.9 V.

The increase of channel resistance with the downscale of the Fin width may have a direct impact on the cut-off frequencies (f_T) and maximum oscillation frequency (f_{max}) of the device. As f_T depends on the total gate capacitance of the device, different gate capacitances are extracted. Fig. 4.8 plots the total gate capacitance (C_{gg}=C_{gs}+C_{gd}) as a function of gate voltage (V_{gs}) for different values of Fin width. It can be measured that the total gate capacitance (C_{gg}) is lower for FinFETs with lower Fin width. The widening of the Fins causes an increased parasitic fringe capacitances and the RF performance is affected.

Variation of cut-off frequency (f_T) as a function of gate overdrive voltage (V_{gt}) for different Fin width is shown in Fig. 4.9. Fig. 4.9 demonstrates that the cut-off frequency is not much sensitive to Fin width variation especially when the FinFET is biased in the saturation region. As Fin width increases, the corresponding increase in the g_m is compensated by a simultaneous increase in the C_{gg} resulting in a little variation in the cutoff frequency. However, for low gate bias, a little increment in f_T is noticed with increase in Fin width.

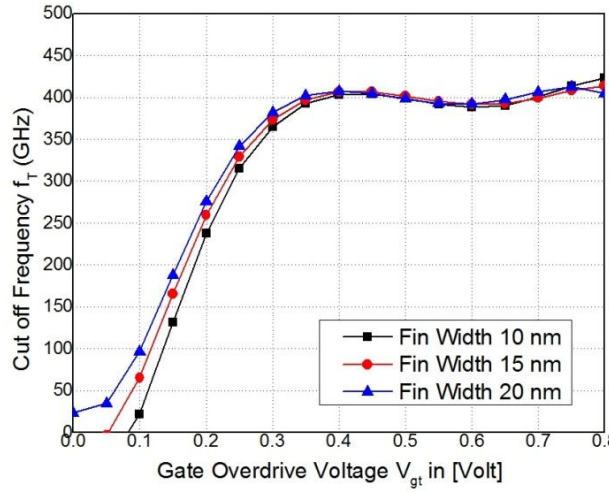

Fig.4.9: Variation of f_T as a function of gate-overdrive voltage, (V_{gt}) for JAM bulk FinFET for different Fin width at V_{ds}= 0.9 V

Fig. 4.10 shows the variation of maximum oscillation frequency (f_{max}) as a function of gate overdrive voltage (V_{gt}) for different Fin width. From Fig. 4.10, it is noticed that maximum oscillation frequency (f_{max}) of the device increases with reduction in Fin width for the strong inversion region. This is because, with narrower Fin width, the electrostatic control of the gate over the channel increases which suppresses SCEs leading to scope of scale the channel even further. From an analog point of view, the increase in gate control of the channel results in decrease of drain control on the channel resulting lower output conductance which in turn increase the f_{max}.

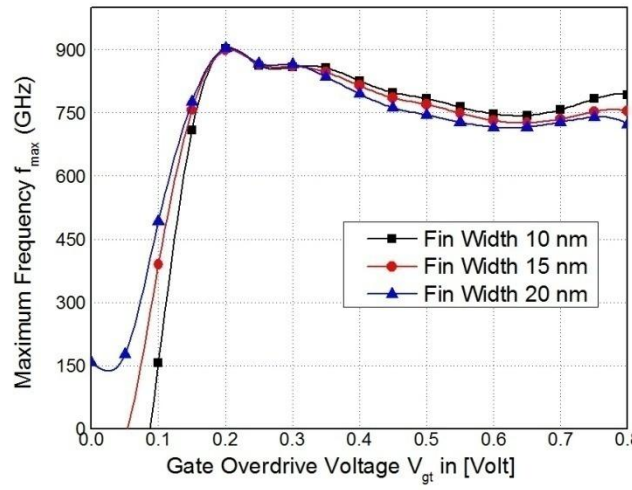

Fig.4.10: Variation of f_{max} as a function of gate-overdrive voltage (V_{gt}) for JAM bulk FinFET for different Fin width at V_{ds} =0.9 V

4.4 CONCLUSION

In this chapter, the effect of the variation of the device dimension on the RF/analog performance of the device has been presented. Variation of gate length, spacer length and Fin width scaling is conducted to study the SCEs of the device. A comparison is made for the performance of the device in analog/RF circuit application for different Fin widths. From the results, it is concluded that reduction of Fin width can cause improvement in device performance in order to find their usage in analog as well as RF applications. These findings will be useful for design and optimization of Junctionless Accumulation Mode bulk FinFETs for analog/RF applications.

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CHAPTER 5

INFLUENCE OF FIN SHAPE ON DEVICE PERFORMANCE

5.1 INTRODUCTION

The requirements of more complex and extremely dense circuits have led to the aggressive downscaling of the MOSFET. However, downscaling leads to Short Channel Effects (SCEs) which unfavorably affects the device performance [5.1-5.4]. Conventional Si MOSFETs with nanoscale channel length also suffer from increase in OFF-state current (I_{OFF}). Reduction of gate oxide thickness to suppress such effects enhances the gate leakage current which is also not desirable. Nanoscale devices also require low-resistance, high-κ dielectrics and metal (or silicide) gate electrodes to continue its growth as per ITRS roadmap [5.5]. As FinFETs having 3D Fin-shaped channels and multiple gates have potential to reduce these serious scaling issues, these structures have been widely studied by the researchers in recent years [5.6-5.18]. From these studies it is noticed that FinFETs have already been emerged as the most preferred solution [5.2-5.4, 5.7] at the 22-nm and below technology node as it provides reduced Short Channel Effects (SCEs) and better gate controllability in comparison to its planar counterparts. They also present greater ON/OFF current ratio and exhibit higher drive current per unit area in comparison to planar devices. Because of these advantages, FinFETs find various applications in areas like high speed digital ICs [5.6], analog ICs [5.8], SRAMs [5.8], DRAMs [5.10-5.11], and flash memories[5.12] etc. On the other hand, Junctionless MOSFETs comprises same doping type in the source region, drain region and channel region which leads to simple process flow during fabrication. In the accumulation mode, the device with additional source/drain doping is used to prevail over the issue of parasitic resistance. There are many advantages of Junctionless MOSFETs over a conventional device such as better protection to short channel effects, superior scalability, enhanced drain-induced barrier lowering (DIBL) etc [5.14]. CMOS circuits implemented with JL FinFET devices are reported to perform slightly better than the inversion mode FinFETs. [5.15-5.16].

In order to utilize the advantages of both these technologies, combination of Junctionless Transistor technology and FinFET structures

becoming an option. Researchers have shown that performance of FinFETs is very much dependent on Fin geometry [5.17-5.18]. However, recent studies on Fin shape are found to be mainly focused on estimating the effect of Fin cross-sectional shape on SCEs, [5.18-5.23] and described some findings on leakage current variation. The effect of Fin-edge roughness and metal grain work function induced variability affecting OFF and ON device characteristics are studied and reported for FinFET [5.24]. As FinFET performance is dependent largely on the Fin geometry, it is expected that shape of Fin cross section should have an impact on its RF/Analog Performance also. So, the investigation on device performance variation with Fin cross-section shape for its application in RF/Analog circuits became necessity. Impacts of variation in Fin shape on RF/Analog performance of the device have been discussed in this chapter. A 3D simulation study is carried out to evaluate the effect of Fin geometry on its performance for analog/RF application. To examine the effect of a nonrectangular channel shape, the geometry-dependent parameter such as Fin top width is varied keeping the bottom width of Fin constant.

5.2 DEVICE STRUCTURE AND SIMULATION FRAMEWORK

Schematic diagram of Junctionless Accumulation-Mode (JAM) bulk FinFET structure for n-channel operation is shown in Fig. 5.1(a). Fig 5.1(b) shows the cross-sectional view of the channel region for varying Fin top width. For better accuracy, the 3-D simulation of FinFET structure is carried out for 20nm gate length with 15 nm Fin height (H_{fin}). Fin bottom width is taken as 15nm while Fin top width is varied over a range between 3nm to 15nm. High-κ gate dielectric (HfO_2) is taken as an insulator material to minimize the gate leakage current caused by obvious quantum tunnelling effect across the gate oxide at this scale [5.25-5.26]. For the devices of 22nm technology and below, the "Equivalent Oxide Thickness (EOT)" of the traditional SiO_2 dielectrics is required to be smaller than 1nm, which results in high gate leakage currents due to the quantum tunnelling effect. So, dielectrics with higher dielectric constant (k-value) can prevent this leakage

current with thicker physical dimension but having desired effective oxide thickness. At the same time, a very large k value cause unfavourable large fringing fields at the source and drain regions and is not desirable. Hafnium-based oxide (HfO_2) having dielectric constant of 22 poses well insulating properties and capacitance performance [5.27-5.28]. It is worth mentioning that the device with HfO_2 spacer shows much improved performance in drain current and transconductance when biased in the saturation region compared to SiO_2 spacer device [5.26]. In this research, Molybdenum whose work function equals to 4.65 eV is considered as a gate material. Work function of Molybdenum can be varied over a wide range (4.5- 4.9 eV) by using nitrogen implantation into Molybdenum followed by a thermal annealing [5.29].Higher doping in source and drain (S/D) region is used in order to decrease the parasitic resistance in the source/drain extension region.

The device under study is simulated by using standard TCAD device simulation tool Silvaco ATLAS [5.30]. In the simulation, drift-diffusion equations are solved for electrons and holes. Field dependent mobility model (FLDMOB) specifies a lateral electric field dependent model for electrons and is used to consider the velocity saturation effect. Because of high channel doping concentration, the “Fermi-Dirac” distribution model without impact ionization is utilized in the simulation. In the simulation setup, electric field dependent carrier model is used. Due to highly doped channel, band gap narrowing effect may arise which is taken care using Bandgap narrowing model (BGN). This model (BGN) is necessary to correctly model the bipolar current gain. “Shockley-Read-Hall (SRH)” and “Auger” recombination/ generation are used in the simulation model to account for leakage currents that exist due to thermal generation. Quantum confinement effect is not considered as it is not significant in case of Junctionless transistors. For numerical calculations, “Newton” and “Gummel” methods are used and a temperature of 300K has been fixed in the simulation. Other important parameters of the device used in this work are tabulated in Table 5.1.

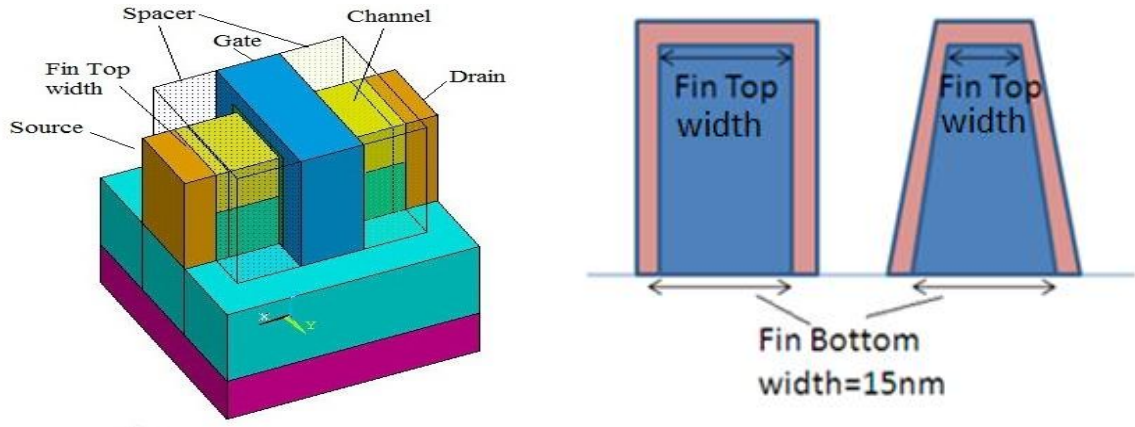

Fig.5.1: (a) 3-D schematic view of JAM bulk FinFET (b) Cross-sectional view of FinFET structure for simulation showing the variation of Fin top width

Table 5.1: Basic device parameters used for simulation

Parameter	**Value**
Fin bottom width (W_{bottom})	15 nm
Fin top width (W_{top})	3-15 nm
Fin Height (H_{fin})	15 nm
Gate Length (L_g)	20 nm
Gate oxide material	HfO_2 (k=22)
Equivalent Oxide thickness (EOT)	1nm
Gate work function (W_F)	4.65 eV
Drain Supply Voltage (V_{ds})	0.9V
Source/Drain doping (cm^{-3})	$1x10^{21}$
Channel doping (cm^{-3})	$1x10^{18}$

Simulation model is calibrated with the published experimental data of Choi et. al. [5.31]. Mobility parameters of this simulation models are chosen appropriately to achieve a qualitative matching of the transfer curves between obtained result and the result published by Choi et. al. [5.31]. Fig. 5.2 shows the matching of transfer curves. Same model parameters are used for all the simulation work here with different Fin structures.

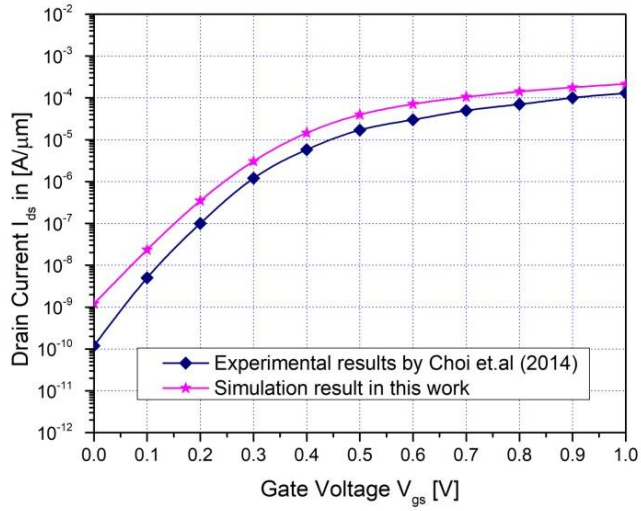

Fig.5.2: Comparison of transfer characteristics between the published results reported in [5.31] and current work

5.3 RESULTS AND ANALYSIS

To compare the impact of different Fin shapes, Fin top width is varied from 15nm to 3nm keeping the Fin bottom width constant (15nm). In order to study the effect of the non-rectangular channel geometry, various key electrical parameters such as, transconductance (g_m), transconductance to drain current ratio (g_m/I_{ds}), Threshold voltage (V_{th}), SS, DIBL, ON-state current (I_{ON}), Off-state current (I_{OFF}). Cut off frequency (f_T), Maximum frequency of oscillation (f_{max}) etc. are calculated and analyzed for each structure.

V_{gs}-I_{ds} curve for the device under study is plotted in Fig. 5.3 for different Fin shapes. It is found that with decrease in Fin top width, I_{ON} decreases as effective Fin width (W_{eff}) decrease. W_{eff} is the effective Fin width defined as perimeter of the Fin cross section adjacent to the high-k gate oxide (HfO_2), calculated basically using the Pythagorean Theorem [5.20] as given in equation (5.1).

$$W_{eff} = 2\sqrt{\left(\frac{W_{bottom}-W_{top}}{2}\right)^2 + \left(H - \frac{W_{top}}{2}\right)^2} + \pi\frac{W_{top}}{2} \qquad (5.1)$$

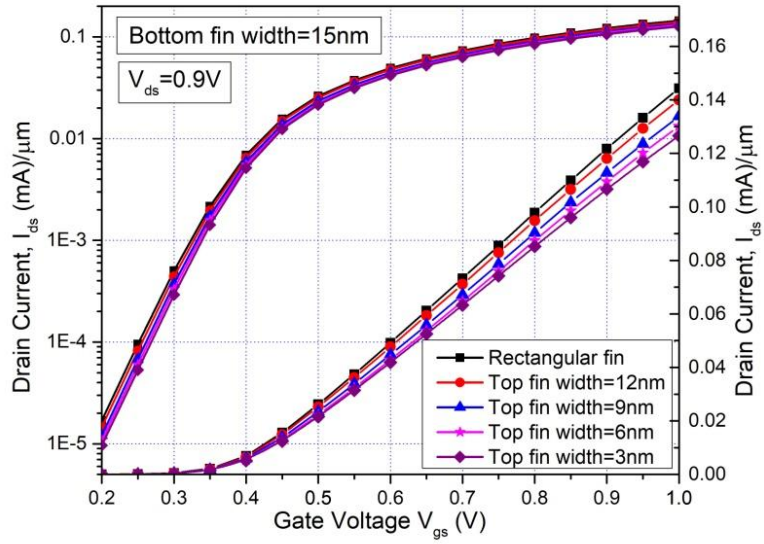

Fig.5.3: Variation of Ids in linear scale with variation of V_{gs} for JAM bulk FinFET for different Fin top width at Vds = 0.9 V.

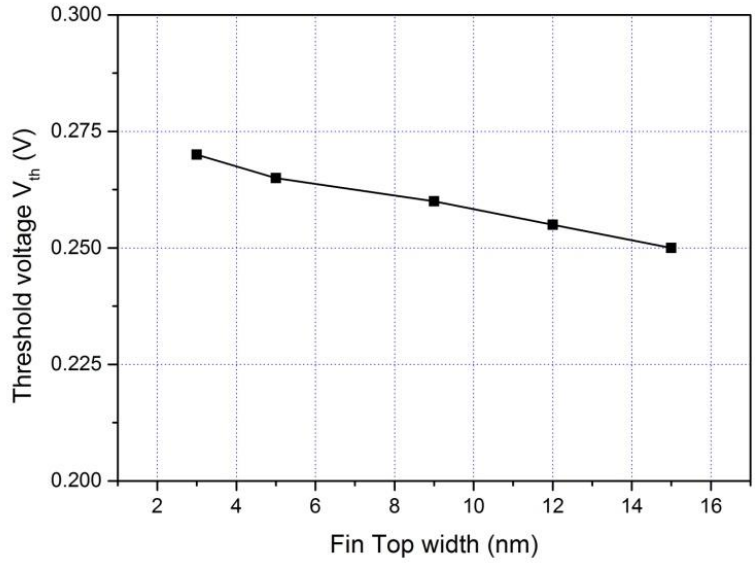

Fig. 5.4: Variation of threshold voltage, V_{th} as a function of Fin top width

In any FinFET, the series resistance of the channel is expected to increase with the reduction of Fin top width, which in turn reduces the effective Fin width, which is in accordance with previously published results by Rezali et al. [5.20]. In this work, Fin top width decrease from 15 nm to 3 nm by changing the Fin shape from rectangular to a trapezoidal shape. Smaller the Fin top width, higher the expected series resistance. As a result, I_{ds} decreases with the reduction of Fin top width.

Threshold voltage of the device for various Fin top width was determined by using the constant current method ($I_{ds}=10^{-7} \times W/L$ A) from the I_{ds} vs. V_{gs} curves. W is the effective Fin width and L represents the channel length. Change of threshold voltage (V_{th}) with Fin top width is plotted in Fig. 5.4. Results show that threshold voltage of the device increases with the reduction of Fin top width. Apparently, V_{th} shift is affected by the variation of series resistance and leakage current of the device. For FinFET with smaller Fin width, V_{th} increases due to this narrow Fin width effect. The electron density map during the ON-state of the device is shown in Fig. 5.5 to compare the electrical properties for different shape of Fin cross section. Fig. 5.5 clearly reveals that for triangular Fin shape the electron density is of more uniform nature. It is due to the fact that as charge density increases across the Fin, V_{th} will become more for triangular FinFET in comparison to rectangular Fin. By controlling Fin shape within a single chip, it is possible to construct multi-threshold FinFETs.

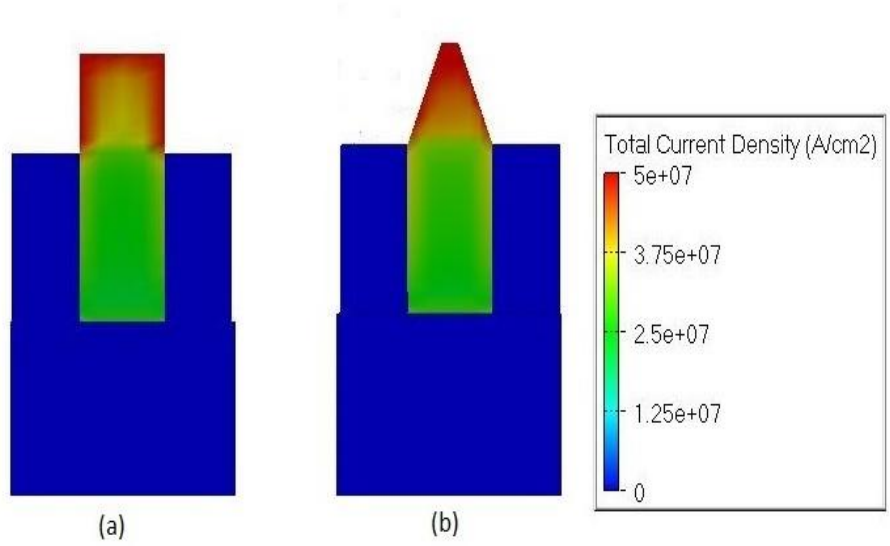

Fig. 5.5: Electron density distribution in FinFET for different Fin shape, at V_{ds} = 0.9 V.

ON current and OFF current of the device is plotted in Fig. 5.6(a). Results show that reduction of Fin top width reduces the ON current (I_{ON}) as well as leakage current (I_{OFF}). Improvement of OFF current (I_{OFF}) is achieved at the cost of reduced I_{ON} due to high parasitic series resistance. From

analysis it is understood that FinFETs on current (I_{ON}) is deteriorated maximum up to 12% (Fin top width=3nm) as Fin cross-section change from rectangular shape to trapezoidal shape. Also, reduction in leakage current is achieved using reduced Fin top width of the devices. The use of tapered Fin allows stronger gate control of the middle region of the Fin, which causes I_{OFF} reduction. Nearly 7% reduction in leakage current is obtained by reducing the Fin top width to 3nm from 15 nm.

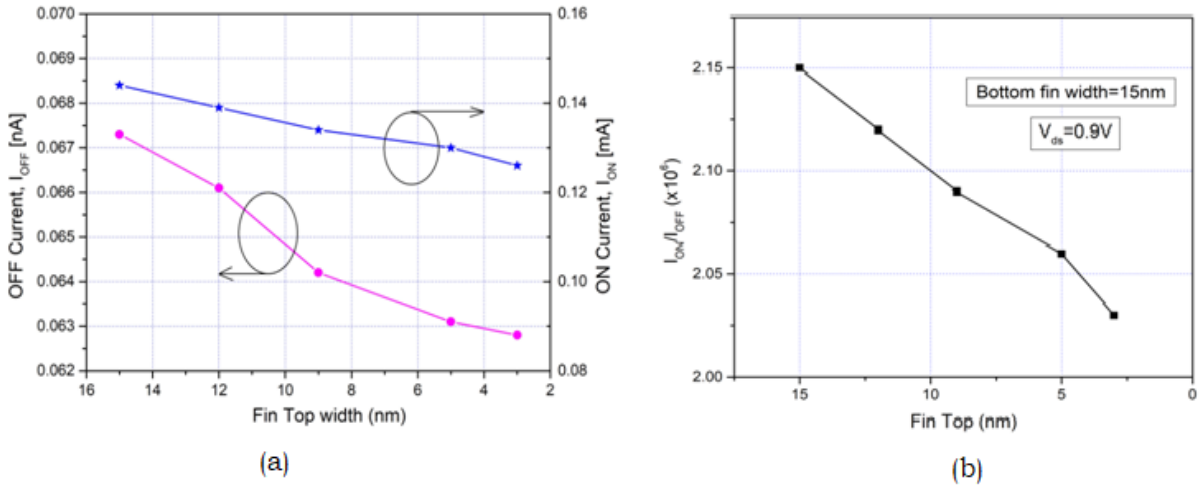

Fig. 5.6: (a) I_{ON} and I_{OFF} of JAM bulk FinFET for different Fin top width (b) ON current and OFF current ratio of the drain current (I_{ds}) for different Fin top width at V_{ds} = 0.9 V.

Change in I_{ON}/I_{OFF} current ratio of the device for different Fin top width is calculated and shown in Fig. 5.6(b). It characterizes how much the difference between the ON current and OFF current of the device under study. For digital applications any device should switch between ON and OFF state at very high speed. I_{ON}/ I_{OFF} ratio is the ratio of the drain current during ON state (I_{ds} at V_{gs}= 1.0 V and V_{ds}=0.9V) and current during OFF state (I_{ds} at V_{gs}= 0.0 V and V_{ds}=0.9V). Higher I_{ON}/I_{OFF} ratio is desirable as it directs higher switching. An appropriate value of I_{ON}/I_{OFF} of the device improves its speed and minimizes leakage. With decrease in Fin top width, I_{ON}/I_{OFF} decreases because with decrease in Fin top width, I_{OFF} decreases but at the same time, I_{ON} also decreases, showing reduction of I_{ON}/I_{OFF}. The decrease of I_{ON} simultaneously followed by decreasing I_{OFF} because of reduced Fin top width highlights that variation of Fin shape significantly

changes the device performance index. To study devices vulnerability to SCEs, the SS and the DIBL are widely used as they measure the resistance of channel control to the rise of the drain voltage. From the DIBL characteristic as shown in Fig. 5.7, it is clear that control of SCEs is possible by varying Fin top width in the FinFET. It's important to mention that the DIBL is better for the Fin shape with reduced Fin top width. Fig. 5.7 also indicates the variation of SS of the device for various Fin top widths. From the analysis, it is understood that SCEs improves for the device with smaller Fin top width. It's worth mentioning that these results match well with the findings of Gaynor et al [5.13].

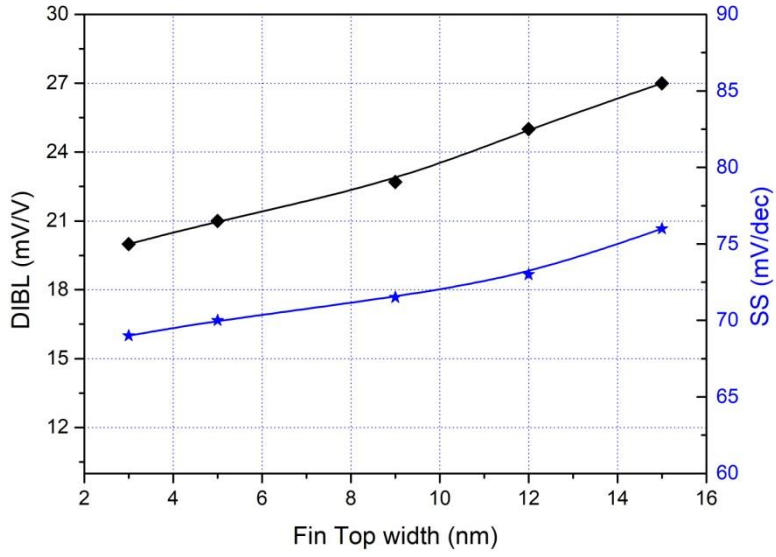

Fig. 5.7: Variation of SS and DIBL for different Fin shape at V_{ds} = 0.9 V.

5.3.1 DEVICE PERFORMANCE FOR ANALOG APPLICATIONS

The analog performance of the device was determined by calculating different analog figure of merits such as Transconductance (g_m), Transconductance generation factor (g_m/I_{ds}), etc. The better understanding of the gate control of the device for different Fin shape can be achieved through transconductance analysis. The variation of transconductance (g_m) and transconductance to drain current ratio (TGF) with gate voltage (V_{gs}) for different Fin top width is shown in Fig. 5.8. The transconductance variation of fig. 5.8 shows that it is very much sensible to Fin geometry and reduction of Fin top width reduces the transconductance. The TGF may be viewed as

the obtainable gain per unit power dissipation. In a MOS device, in weak inversion region g_m/I_{ds} is higher and reduces rigorously with increase in gate voltage (V_{gs}) i.e in the strong inversion regime. Having higher transconductance to drain current ratio for a device is desirable. It is evident from the Fig. 5.8 that TGF does not vary much for change in Fin top width.

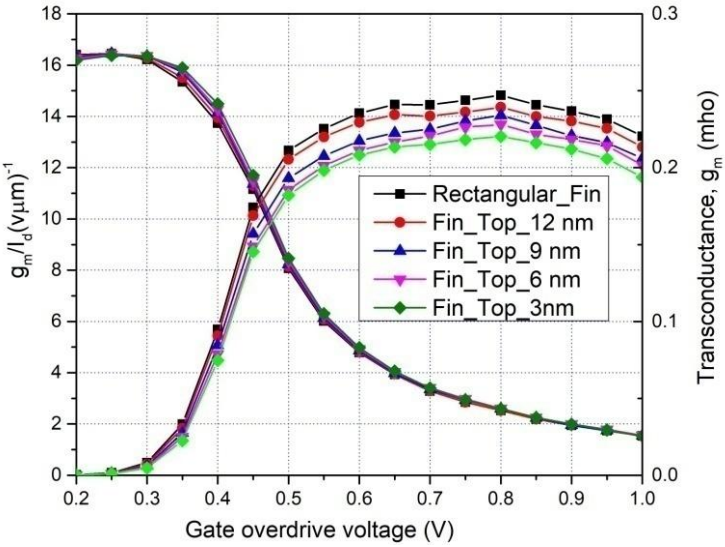

Fig. 5.8: Variation of g_m and g_m/I_{ds} with V_{gs} for Junctionless Accumulation Mode bulk FinFET for different Fin top width at V_{ds} = 0.9 V.

5.3.2 DEVICE PERFORMANCE FOR RF APPLICATIONS

The RF performance of the Junctionless FinFET under study is evaluated by extracting f_T (cut-off frequency) and f_{max} (maximum oscillation frequency) which are key figure of merits for RF circuits. The cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) are considered for different Fin top width. The f_T is extracted as the frequency for which the modulus of the short circuit current gain of the device is unity. The cutoff frequency f_T is a feature of the intrinsic transistor without considering parasitic series resistances where as f_{max} is the characteristic of the extrinsic device which includes series resistance such as source resistance, drain resistance and gate resistance. The capability of the device to provide power gain at high frequencies is justified by f_{max}. It represents the frequency for which the magnitude of the power gain is unity. The simplified expressions for f_T and f_{max} are reported in [5.32-5.33] which is used for this calculation.

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{5.2}$$

$$f_{\max} = \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s + R_i + R_g)\cdot(g_{ds} + g_m \frac{C_{gd}}{C_{gs}})}} \tag{5.3}$$

where g_m, C_{gs}, and C_{gd}, R_g, R_s, and R_i are the transconductance, the gate-to-source capacitance, the gate-to-drain capacitance, the gate resistance, the source resistance and the channel resistances respectively.

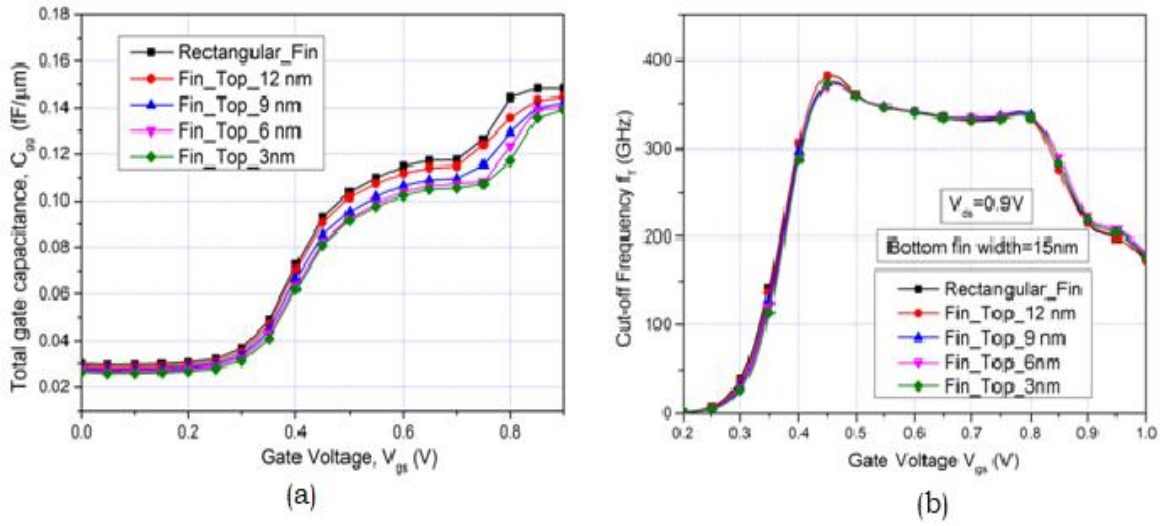

Fig. 5.9: (a) Variation of Gate Capacitance, C_{gg} (=C_{gd}+C_{gs}) as a function of V_{gs} for JAM bulk FinFET for different Fin top width at V_{ds} = 0.9 V. (b) Variation of f_T as a function of gate voltage for different Fin top width at V_{ds} = 0.9V

After obtaining required parameters from simulations, f_T and f_{max} are calculated using numerical calculations in MATLAB. As shown in (2), f_T depends strongly on transconductance and the total gate capacitance. Fig. 5.10 plots the total gate capacitance (C_{gg}=C_{gs}+C_{gd}) as a function of gate voltage (V_{gs}) for different Fin top widths. It can be observed from Fig. 5.9 (a) that the total gate capacitance (C_{gg}) is lower for FinFETs with lower Fin top width. Fig. 5.9 (a) reveals that the gate capacitance of triangular Fin is reduced by almost 6.5% when the Fin top width reduces from 15 nm to 3 nm. However, transconductance (g_m) of the device also decrease with decrease in Fin top width. As a result, the cut-off frequency (f_T) remains

almost unchanged to Fin top width variation especially when the FinFET is biased in the saturation region. Fig. 5.9 (b) plots the cut-off frequency (f_T) variation with variation of V_{gs} for different top width.

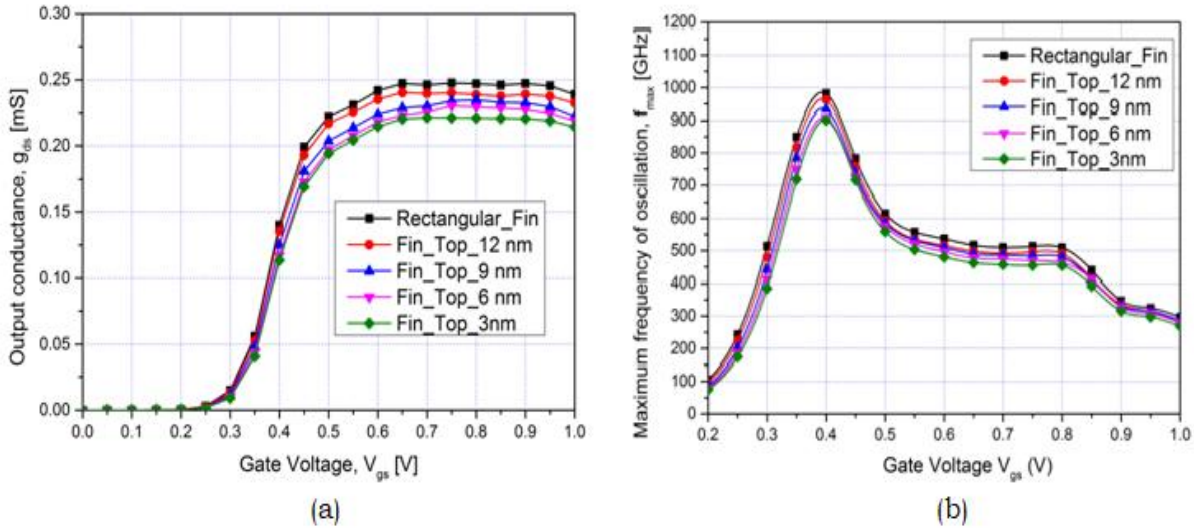

Fig. 5.10: (a) Variation of output conductance, g_{ds} as a function of V_{gs} of JAM bulk FinFET for different Fin width at V_{ds} = 0.9 V. (b) Variation of f_{max} as a function of gate voltage for JAM bulk FinFET for different Fin top width at V_{ds} = 0.9 V

The increase of channel resistance with the reduction of the Fin top width has a direct impact on maximum oscillation frequency (f_{max}) of the device. Eqn (5.3) indicates that the f_{max} includes the effect of g_{ds} and source, drain and gate parasitic resistances. Fig. 5.10 (a) shows the variation of g_{ds} as a function of V_{gs} for different Fin top width. The output conductance (g_{ds}), shown in Fig. 5.10(a), is dependent on the Fin shape. FinFET with Fin top width of 3nm have lower g_{ds} value. The variation of maximum oscillation frequency (f_{max}) for different Fin top width is shown in Fig.5.10(b). Fig. 5.10(b) reveals that maximum frequency of oscillation decreases with decrease in Fin top width. Nearly 10% decrease in maximum frequency of oscillation was noticed when the Fin top width changed from 15nm to 3nm. This is because the increase of channel resistance with decrease in effective Fin top width. The findings may be supported by the model proposed by recently published work by Kim et al. [5.34].

5.4 STRUCTURAL OPTIMIZATION

To optimize the device structure, DIBL is considered as a main performance index in SCEs where as maximum oscillation frequency (f_{max}) is considered as the RF figure of merit. Our analysis indicates that SCEs of the device can be improved by using smaller Fin top width. On the other hand, triangular Fin degrades the Analog/RF performance of the device. Normalized performance index of DIBL and f_{max} is plotted (Fig.5.11) as a function of Fin top width keeping the Fin bottom width at 15 nm. Fig.5.11 shows the variation of DIBL and f_{max} performance as a function of Fin top width. From the figure, it is observed that both the performance index cross each other for the Fin top value of around 7 nm. Therefore, the optimized value of Fin top width should be kept around 7 nm while keeping the width of Fin bottom at 15 nm for this model. This design provides better Short Channel Effects (SCEs) and reasonable maximum oscillation frequency so that the device can be used in circuits for RF/Analog applications.

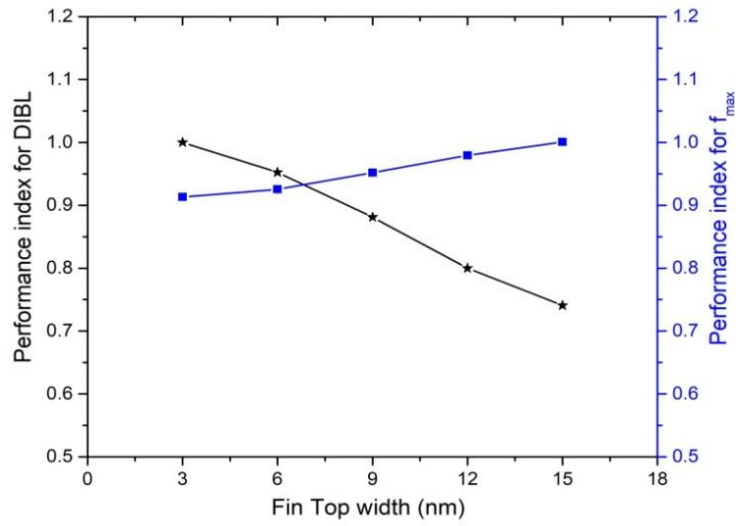

Fig.5.11: Variation of DIBL and f_{max} performance as a function of Fin top width

5.5 CONCLUSION

In this chapter, the RF/analog performance of the device has been evaluated to study the effect of the variation of Fin shape. A comparison is made by calculating different parameters of the device with different Fin

shapes. The performance of the device for digital applications degrades with decrease in Fin top width but its DIBL and SS become better. 25% reduction of DIBL and 10% reduction in SS are calculated for the device when Fin shape change from rectangular Fin of width 15 nm to trapezoidal Fin with 3nm Fin top width. Almost 7% reduction in leakage current is obtained at the cost of reduced I_{ON}/I_{OFF}. Decrease in Fin top width also increases the parasitic component such as S/D resistance. As an RF figure of merit, maximum frequency of oscillation of the device is reduced by 10% when the Fin shape change from rectangular to near triangular. However variation of Fin top width may be utilized for achieving multi-threshold applications and low leakage FinFET design. From the observations, it may be summarized that reduction of Fin top width degrades device performance in order to find their usage in analog as well as RF applications. The optimized value of Fin top width should be kept around 7 nm while keeping the width of Fin bottom at 15 nm for this model. This design is expected to provide better SCEs and reasonable maximum oscillation frequency to use the device in RF/Analog applications. These findings will be useful for optimization of fabrication process of Junctionless Accumulation Mode bulk FinFETs for analog/RF applications.

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CHAPTER 6

IMPACT OF BARRIER LAYER THICKNESS ON NANOSCALE HETEROSTRUCTURE MOSFET

6.1 INTRODUCTION

As physical dimensions of conventional MOSFET are reduced to the order of nanometers, the "Short Channel Effects (SCEs)" badly affect the characteristics of MOSFETs. In a constant endeavor to increase current drive and improved control of SCEs, Double Gate (DG) MOSFETs have been evolved as a most promising device. It is considered as one of the important option of research in VLSI technology because of its high scalability by producing ultra thin body. Other than structural modifications, research on new materials capable of providing higher carrier mobility and better performance such as III-V semiconductors are of growing interest [6.1-6.3]. As these materials are grown from Group III and Group V of periodic table, they are familiar as III-V semiconductors.

At present, it is recognized that III–V materials based MOSFETs allow higher drive current and better transconductance in comparison to their Si-based counterpart [6.1]. Among III-V group compound semiconductors, "Indium-Gallium-Arsenide (InGaAs)" has been extensively studied as a prospective high mobility channel material for future n-MOSFETs due to its improved electron mobility [6.2-6.3]. This is the front runner among semiconducting materials to replace Silicon in the transistor channel at or beyond the 10-nm CMOS logic technology node. Analysts predict that major semiconductor manufacturer Intel is going to adopt III-V semiconductors for the device at 10nm node. Many researchers have reported digital, RF & analog performance of hetero-structure DG MOSFET [6.4-6.12]. Many III–V semiconductor materials based MOSFET have been proposed and compared with their silicon-based counterpart [6.1-6.3]. From published results, it is understood that the III–V materials based devices showed superb control of SCEs, reduced delay and improved ON current (I_{ON}) than that of silicon-based device of same dimension [6.10]. It is worth mentioning that to follow the scaling rule, the thickness of SiO_2 as gate dielectric material has attained the point for which the direct tunneling mostly increases the leakage current, affecting the circuit operation. To overcome this problem, use of high-k gate dielectrics have been proposed [6.11]. Materials such as

Y_2O_3, CeO_2, HfO_2, ZrO_2, Ta_2O_5, TiO_2, La_2O_3 etc. have received considerable attention. Considering its better interface properties with Si, its thermal stability and many other issues, Hafnium based oxide (HfO_2) has been identified and continuous to be considered as a possible high-k gate dielectrics in CMOS technology [6.11]. In a recent paper, the asymmetric behavior of the underlap DG heterostructure MOSFET is analyzed extensively [6.9]. Mostly, the researchers have investigated different aspects of InGaAs-channel MOSFETs for digital applications and for analog/mixed-signal applications [6.10-6.11]. At the same time, linearity performance of Nanoscale DG MOSFET has been studied by many researchers [6.12-6.18]. For a heterostructure MOSFET, the impact of different materials as barrier layer on the analog performance [6.10] and digital performance [6.19] are also investigated. Recently, the simulation and analysis of InGaAs/InP based ultra low-power underlap DG heterostructure MOSFET has been reported for digital applications [6.19]. However, to the best of my knowledge, no such report is available on the study of barrier layer thickness on the RF, analog and linearity performance for a DG heterostructure MOSFET. In this chapter, an investigation of the impact of thickness variation of barrier layer on the Analog, RF and Linearity performance of an InGaAs/InP heterostructure MOSFET has been presented.

6.2 DEVICE STRUCTURE AND SIMULATION SETUP

The proposed structure of the InGaAs/InP heterostructure based DG nanoscale MOSFET device is shown in Fig. 6.1. The device structure considered in this work composed of a buried-channel InGaAs MOSFET having two InP barrier layers on both sides. The channel length is fixed as 12nm and the length of the Source/Drain region is taken as 2nm. The InGaAs channel thickness (t_{ch}) is taken as 2nm and InP barrier layer thickness is varied from 1 to 4nm. High-*k* gate dielectric material HfO_2 with equivalent oxide thickness of 1.2nm is used in order to achieve strong vertical confinement required to maximize transconductance and suitably

low “drain-induced barrier lowering (DIBL)”. The high-k dielectric helps to minimize gate-leakage current. The source and drain regions of the device are n type doped with high doping concentration of $10^{20}/cm^3$. Channel region is lightly p type doped with doping concentration of $10^{16}/cm^3$. Abrupt doping profile is used at source/drain ends. As channel, $In_{0.53}Ga_{0.47}As$ material is considered as it offers superb electron mobility.

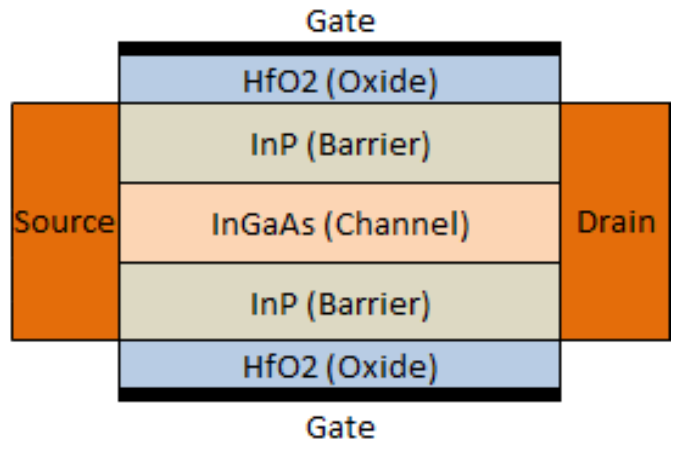

Fig. 6.1: Schematic diagram of the InGaAs/InP based DG MOSFET

The device structure corresponding to Fig. 6.1 has been simulated using a TCAD numerical device simulator SILVACO ATLAS [6.20]. Two-dimensional numerical simulations using drift-diffusion carrier transport model have been performed in detail. In drift-diffusion formalism, the basic semiconductor equations comprise Poisson equation and carrier continuity equations, where the current results from either drift or diffusion process [6.19]. For calculations, numerical method “Newton” is utilized in the model and a temperature value of 300K has been set in simulation study. In the simulation model the electric field dependent mobility is incorporated. The Shockley-Read-Hall (SRH) recombination model is taken to consider all the effects essential for calculating the carrier mobility [6.17, 6.19]. Boltzmann statistics is considered in the simulation model. Mesh density of the structure is carefully chosen for the accurate simulation results as well as to accelerate the computational efficiency. The model is calibrated using proper model parameters and by comparing simulation results with the published experimental results by Morassi et. al. [6.7]. Fig. 6.2 indicates a good qualitative matching of the transfer curves. Once the matching is achieved

between [6.7] and obtained results for V_{ds}=0.05V and V_{ds}=0.5V, the same calibrated model parameters are employed for other simulations with V_{ds}=1.0V as it is known that most of the high-speed analog/RF circuits work in the "saturation region" and not in the "linear region" [6.21].

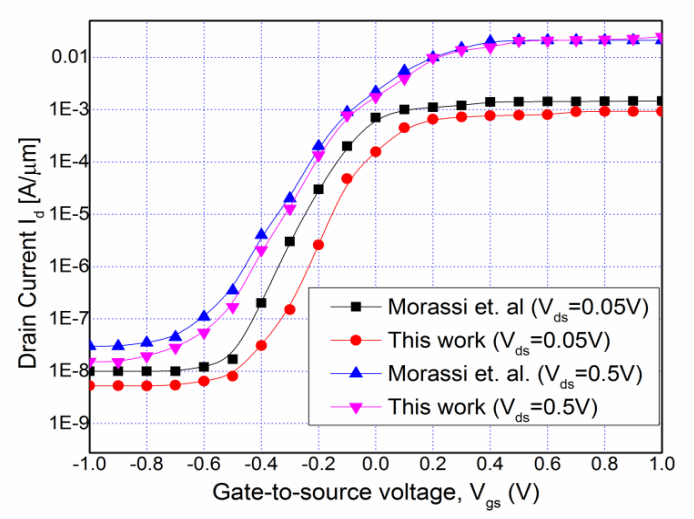

Fig. 6.2: Comparison of simulated transfer characteristics curves with the experimentally findings in Morassi et.al. [6.7] for the InGaAs/InP MOSFET

6.3 INVESTIGATION OF ANALOG PERFORMANCE

In this section, the different parameters important for analog performance analysis such as the transconductance (g_m), output resistance R_o and intrinsic gain (g_mR_o) are studied. The effect of barrier layer thickness on the crucial analog parameters is investigated initially and described in detail. The key parameters of heterostructure MOSFET are electron mobility and sheet carrier density. The gate-to-channel separation affects the gate control on the conduction layers and proven to be an effective way to dictate the physics of the electron confinement inside the channel and decrease short channel effect for high speed RF/analog applications. Higher carrier confinement indicates a better modulation of the carriers by the gate voltage under high drain voltages, resulting in a superior control of drain current [6.23]. Thus, different gate capacitances, transconductance (g_m) and frequency performance of the device is directly affected by the change in barrier layer thickness [6.18, 6.22]. The thickness of the barrier layer determines the space between the 2DEG and the gates that control the charge in the 2DEG concentration [6.24]. It is due to fact that as barrier

thickness increases, the size-quantization levels E_i shift to lower energies, resulting in an increase of the difference between E_F and E_i where E_F is the equilibrium Fermi level. The 2DEG being an explicit function of the surface barrier, increase with barrier thickness initially and saturates gradually. The trend of increasing 2DEG density with barrier thickness is in agreement with earlier reported theoretical and experimental results [6.25].

The drain current I_d of DG heterostructure MOSFET as a function of gate voltage V_{gs} varied from -1V to 2V is measured with fixed drain voltage (V_{ds}) of 1V. The V_{gs}-I_d curve of the DG MOSFET studied is shown in Fig. 6.3. Drain current increases with V_{gs} due to increase of carrier density in the channel. For this simulation, the gate length is kept fixed at 12nm and the barrier thickness is varied from 1 nm to 4nm with a step of 1nm, keeping thickness of channel constant.

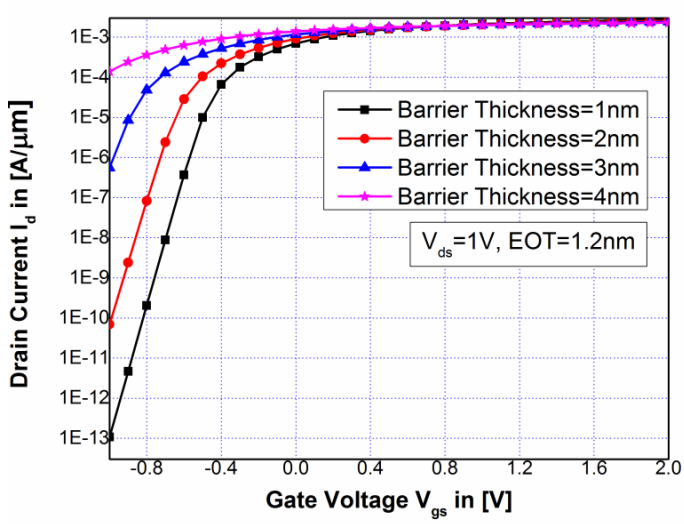

Fig.6.3: Variation of Drain current (I_d) in log-scale with gate to source voltage (V_{gs}) for different barrier thickness

From the simulated results, it is observed that for small gate bias, the drain current increases with an increase in the barrier thickness. The OFF-state current (I_{OFF}) for devices with thicker barrier is higher as is expected because of the reduced gate control with thicker barrier on both sides of the channel.

In Fig. 6.4, the variation of g_m with gate voltage (V_{gs}) as a function of barrier thickness is shown. Fig. 6.4 reveals that a considerable improvement

in g_m is observed for a device with a decrease in barrier layer thickness. Fig. 6.4 uncovers that barrier thickness of 1nm provides the highest transconductance.

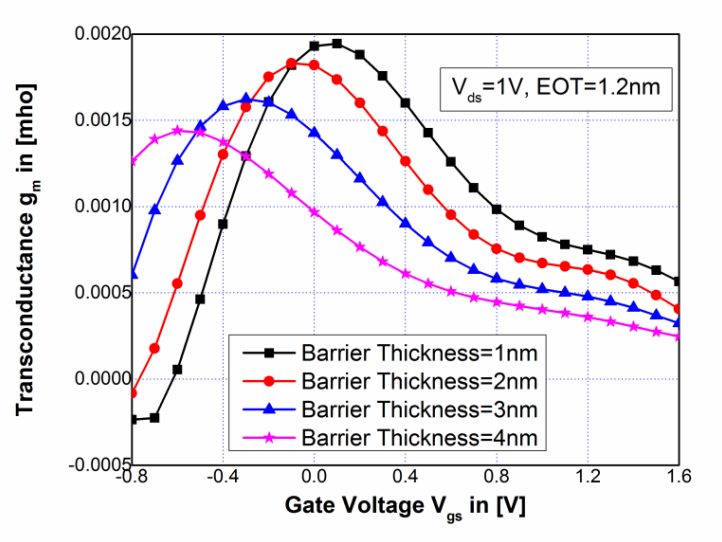

Fig. 6.4: Variation of transconduance g_m as a function of gate to source voltage (V_{gs}) for different barrier thickness ranging from 1nm to 4nm with V_{ds}=1V, EOT=1.2nm

The output resistance (R_o) and the intrinsic gain (g_mR_o) of the device as a function of the gate-to-source voltage (V_{gs}) are shown in Fig. 6.5.

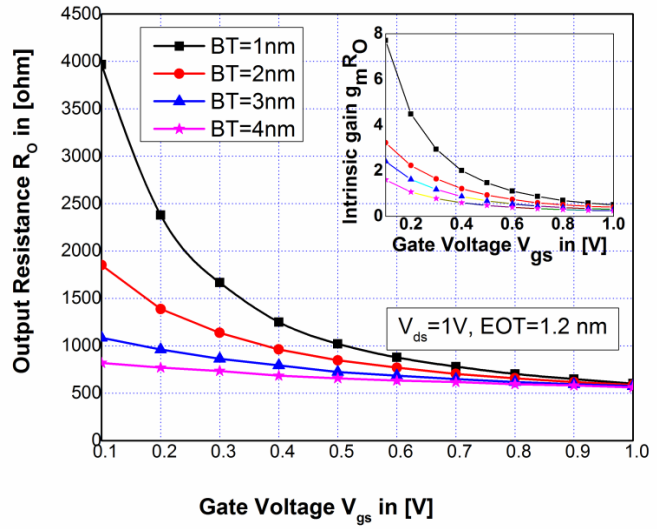

Fig. 6.5: Variation of output resistance (R_o) and intrinsic gain g_mR_o [Inset] with V_{gs} for different barrier thickness (BT) ranging from 1nm to 4nm.

From Fig. 6.5, it appears that a thinner barrier results in a higher output resistance compared with thicker barrier. For thicker barrier layer, the channel goes away from the insulator–semiconductor interface. As a

result, carriers in the channel undergo fewer amount of surface-roughness scattering, resulting in an increase in its mobility, which in turn causes a decrease in the output resistance. On the other hand, a decrease in the barrier thickness causes a decrease of charge density due to the induced higher electric fields on the barrier which leads to greater depletion of the 2DEG. This results in a low current level and high sheet resistance and output resistance. From Fig. 6.5, it is also observed that the effect of barrier thickness on R_o gradually diminishes at higher V_{gs}.

6.4 RF PERFORMANCE ANALYSIS

This section contains the analysis of the device performance for applications in RF circuits. The two most important parameters evaluated to recognize the applicability of the device for RF circuits are the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}). The f_T represents the frequency for which the current gain is unity, whereas f_{max} stands for the frequency corresponding to the unity power gain of the device. f_T and f_{max} can be defined as follows [6.8, 6.12]:

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \qquad (6.1)$$

where g_m, C_{gs}, and C_{gd} are the transconductance, the gate-to-source capacitance and gate-to-drain capacitance respectively.

$$f_{\max} = \frac{g_m}{2\pi C_{gs}\sqrt{4\cdot(R_s + R_i + R_g)\cdot(g_{ds} + g_m\frac{C_{gd}}{C_{gs}})}} \qquad (6.2)$$

Where R_g, is the gate resistance, R_s, source resistance, and R_i is the intrinsic channel resistances. g_{ds} is the output conductance.

The intrinsic capacitances such as gate-to-source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) are plotted as a function of gate voltage V_{gs} for different barrier thickness and are shown in Fig. 6.6 & Fig. 6.7 respectively.

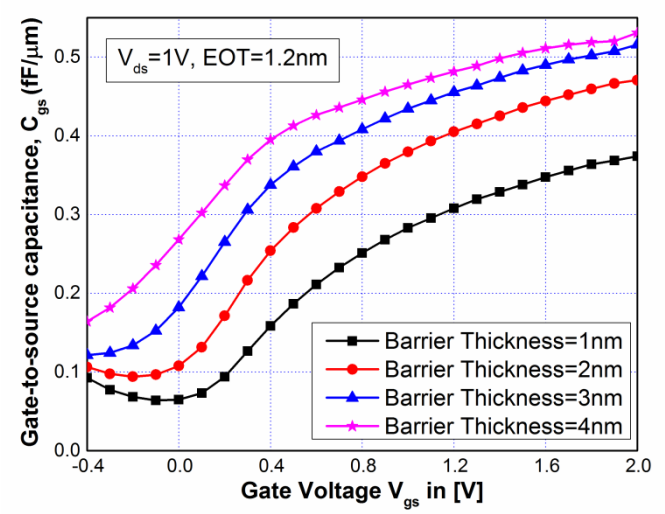

Fig. 6.6: The gate-to-source capacitance (C_{gs}) as a function of the gate voltage (V_{gs}) for different barrier thickness

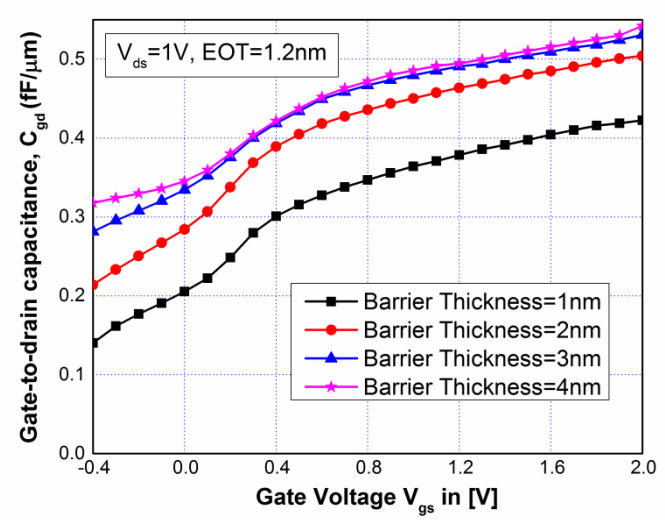

Fig. 6.7: The gate-to-drain capacitance (C_{gd}) as a function of the gate voltage (V_{gs}) for different barrier thickness

From the results shown in Fig. 6.6 & 6.7, it is noticed that the gate capacitances (C_{gs} and C_{gd}) of the device with barrier thickness 4nm are greater than that of the devices having thinner barrier. This is because, when the barrier thickness increases, thickness of the source and drain also increases, which results in an increase of the area-dependent parasitic capacitances between gate-to source (C_{gs}) and gate-to-drain (C_{gd}). It is known that outer fringing capacitances (C_{of}) are associated with electric field of lines emerging from the sidewalls of the gate and ending at the extended source/drain regions in contrast to inner fringing capacitances (C_{if})

associated with electric field of lines emerging from the inner surface of the gate electrode and the source or the drain regions passing through two different materials. Therefore, an increase in the thickness of the source/drain region causes an increase in the C_{if} and C_{of}, contributing to higher C_{gs} and C_{gd}.

Fig. 6.8 and Fig. 6.9 show the extracted f_T and f_{max} as a function of gate voltage for different barrier thickness. The device with thinner barrier exhibits the highest value of f_T and f_{max} indicating that RF performances can be improved by scaling down the barrier thickness, which is in agreement with earlier reported results [6.26-6.27]. The Cut-off frequency (f_T), which depends on the ratio of transconductance to the total gate capacitances, is highest for the device with 1nm barrier thickness, as shown in Fig. 6.8. An increase of total input gate capacitance with increasing barrier thickness (observed earlier in Fig. 6.6 & Fig. 6.7) degrades the f_T values. Value of f_{max} which indicates the power gain cutoff frequency is a more sensible measure of high-frequency device performance. To improve the value of f_{max} of the device it is required to diminish the parameters in the denominator of equation (6.2). From earlier analysis, it can be observed that the transconductance g_m increases and parasitic capacitances (C_{gs} and C_{gd}) decreases with decrease in the barrier thickness. Therefore, a decrease in barrier thickness results in an increase in f_{max}. It is evident from Fig. 6.9 that the peak f_{max} is highest for barrier thickness 1nm and it decreases with increasing barrier thickness. Increase in barrier thickness causes degradation of f_{max} due to lower transconductance (g_m) and higher gate-to-source capacitance (C_{gs}). The reduced drain conductance of the device with thinner barrier is another important factor for the higher f_{max}. C_{gd} and C_{gs} has a small value which increases with V_{gs} slowly (shown in Fig. 6.6 & 6.7), whereas the value of g_m increases and decreases rapidly as shown earlier (Fig.6.4). It is evident from Fig.6.8 and Fig. 6.9 that, as gate bias increases from subthreshold to saturation region, both f_T and f_{max} increases dominated by increase in transconductance (Fig. 6.4), and lower parasitic capacitances C_{gs} and C_{gd} (Fig. 6.6 and Fig. 6.7) . Then it reduces with gate bias because of

the collective effect of increase in the parasitic capacitances and a decrease in transconductance due to the mobility degradation at higher gate bias.

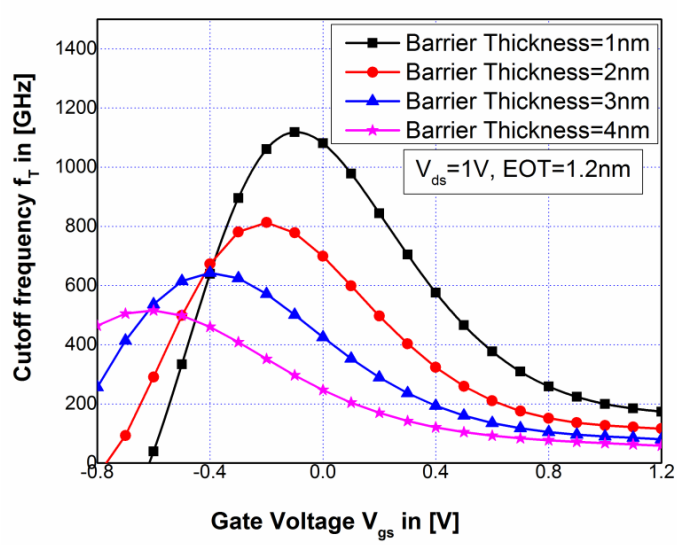

Fig. 6.8: Comparison of the cutoff frequency (f_T) as a function of the gate bias (V_{gs}) for different barrier thickness

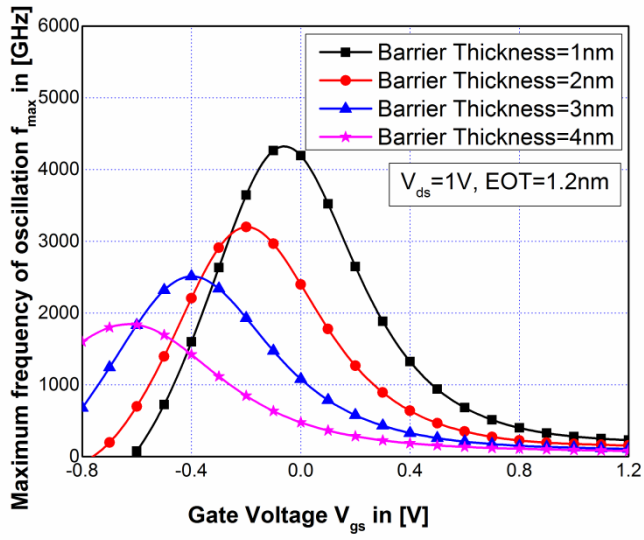

Fig. 6.9: Comparison of the maximum frequency of oscillation (f_{max}) as a function of the gate bias (V_{gs}) for different barrier thickness

6.5 LINEARITY ANALYSIS

In many Analog and RF circuits such as power amplifier and low noise amplifier, nonlinearity creates in detrimental effects and that degrade the performance of the system. So, nonlinearity needs to be controlled in order to proper function of these circuits. The use of physics-based TCAD device simulators gives a more comprehensive and accurate analysis

alternative to traditionally used compact models for linearity analysis [6.18]. For a thorough evaluation of RF linearity performance, various "Figure of Merits (FoMs)" namely VIP_2, VIP_3, IIP_3, IMD_3 and 1-dB Compression Point is studied. VIP_2, stands for the 2nd order Voltage Intercept Point which is the extrapolated gate voltages at which the 2nd harmonic becomes equal to the fundamental tone in the device's drain current. 3rd order Voltage Intercept Point VIP_3 is defined as "the extrapolated gate voltage amplitudes at which the third order harmonic become equal to the fundamental tone in the device's drain current" [6.18]. The extrapolated input power for which the first and the third harmonic are equal, i.e. IIP_3 (3rd order Input Intercept Point) and the third order Intermodulation Distortion is denoted as IMD_3. All these terms [6.17, 6.18] are mathematically given in equations (6.3-6.7) below:

$$VIP_2 = 4\frac{g_m}{g_{m2}} \tag{6.3}$$

where

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad , \quad g_{m2} = \frac{\partial^2 I_d}{\partial V^2{}_{gs}}$$

g_m stands for the transconductance and g_{m2} is the first order derivative of transconductance.

$$VIP_3 = \sqrt{24\frac{g_m}{g_{m3}}} \tag{6.4}$$

where $g_{m3} = \frac{\partial^3 I_d}{\partial V^3{}_{gs}}$

$$IIP_3 = 4\frac{g_m}{g_{m3}R_s} \tag{6.5}$$

Where R_s=50Ω taken for our study.

$$IMD_3 = 4.5(VIP_3)^3 g_{m3} \tag{6.6}$$

The 1-dB compression point represents "the level of power that causes the gain to drop by 1-dB from its small signal value". For any system to be a liner one, it should stay well below the 1-dB compression point [6.17]. The 1-dB compression point is given by:

$$\text{1-dB Compression Point} = 0.22\sqrt{\frac{g_m}{g_{m3}}} \qquad (6.7)$$

After simulations, adequate large data sets are extracted. Then, post-processing of data using MATLAB is done to obtain first, second and third derivatives of I_d (drain current) with respect to the gate voltage, V_{gs}. These results are then used in the calculations of required "Figure of Merits (FOMs)" by using MATLAB.

There are two peaks appearing for all the linearity FOMs, one at a lower gate bias and a maximum at higher gate bias for the simulated heterostructure DG MOSFET device. However, for its circuit applications, the device should be operated in the moderate inversion regime. Therefore, the maxima appearing at lower V_{gs} is considered for comparison.

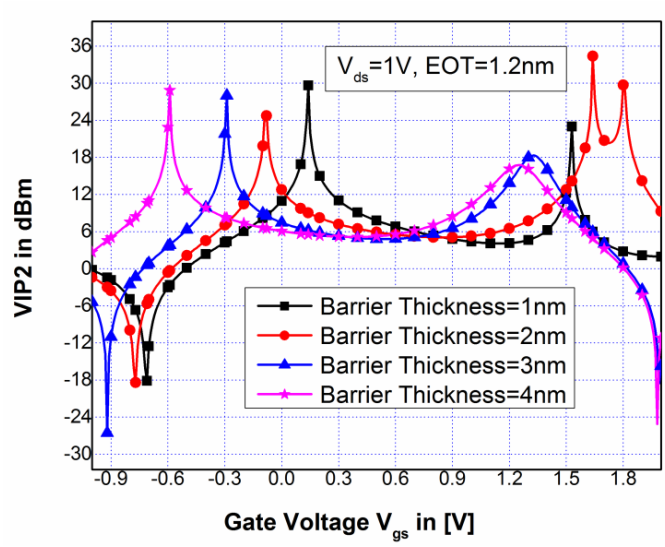

Fig. 6.10: VIP_2 as a function of the gate-to-source voltage V_{gs} for different barrier thickness

Fig. 6.10 shows the comparison of the linearity response of DG heterostructure MOSFET for different barrier layer thickness by plotting VIP_2 as a function of gate bias V_{gs}. From equation (3) and (4), it is understood that value of VIP_2 is directly proportional to the ratio of g_m/g_{m2} where as VIP_3 is proportional to the square root of ratio of g_m/g_{m3} respectively. So, the peak in VIP_2 curve is obtained when the g_m is higher and gm_2 is lower. As, peak of g_m shifts towards lesser value of V_{gs} with larger barrier thickness, the peak of VIP_2 curve also shifts towards lower

value of V_{gs}. Same trend is observed in case of VIP_3. For DG heterostructure MOSFET having barrier thickness 4nm, the peak VIP_2 occurs at a lower V_{gs}. Fig. 6.11 show the plot of VIP_3 as a function of V_{gs} for different barrier layer thickness. A peak in VIP_3 is seen at lower gate voltage, corresponds to the moderate inversion region. The position of the singularity shifts to higher V_{gs} as barrier thickness decreases. From Fig. 6.11, it looks that to achieve high linearity (i.e., large VIP_3) the gate bias has to increase for a device with thin barrier. A swing of peak VIP_3 in the direction of higher V_{gs} with thinner barrier is not pleasing as it means that a higher V_{gs} must be applied to preserve linearity of the device.

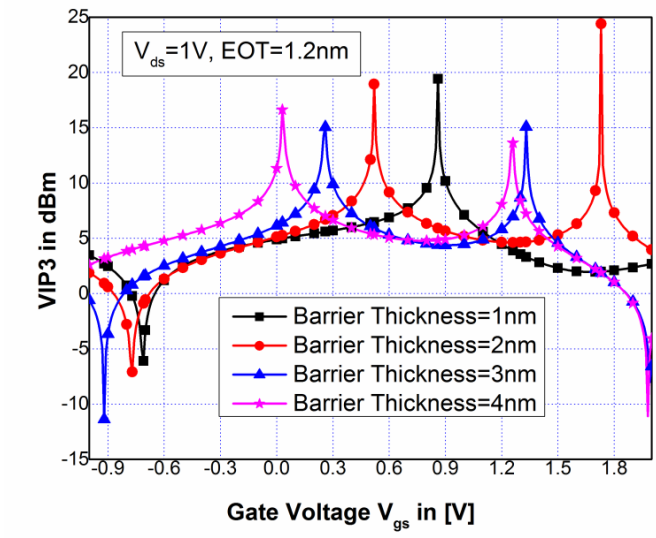

Fig. 6.11: Plot of VIP_3 with the gate-to-source voltage V_{gs} for different barrier thickness

The plot of IIP_3 as a function of V_{gs} for different barrier thickness is exposed in Fig. 6.12. It is seen that in our hetero-structure DG MOSFET, device with higher barrier thickness exhibits higher IIP_3 at lesser value of the gate-to-source voltage, V_{gs} which indicates its superior linearity performance. As barrier thickness decrease, the peak moves towards the higher V_{gs} on account of an increment in C_{gs} and lower concentrations of carriers as shown in Fig.6.12 representing that a larger value of barrier layer thickness is desirable for superior RF linearity.

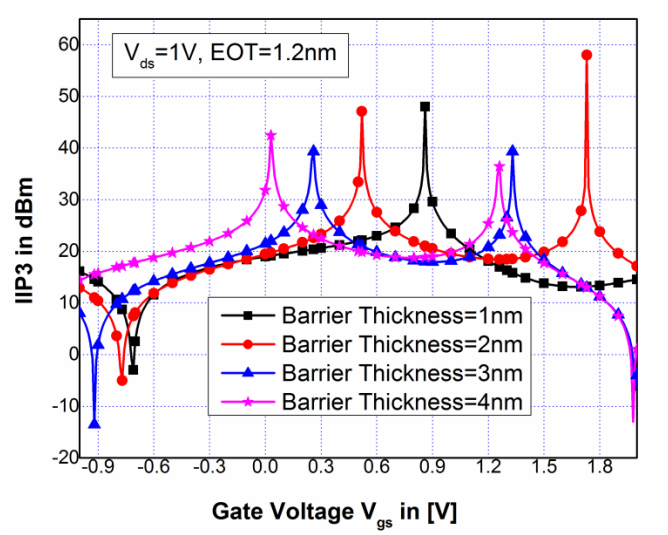

Fig. 6.12: IIP_3 as a function of the gate-to-source voltage V_{gs} for different barrier thickness

Fig. 6.13 illustrates the change in IMD_3 with gate-to-source voltage, V_{gs} which decide the distortion performance of the device under study. Lower peak of IMD_3 highlights its applicability for low distortion analog circuits. Fig. 6.10, Fig. 6.11 and Fig. 6.12 provide a clear idea that peak value of VIP_2, VIP_3, and IIP_3 do not change much for different barrier thickness. The peak position of these Figures of Merits (FOMs) also shifts towards inferior gate voltage in case of higher barrier thickness. Shifting of peak of the position towards elevated gate voltage means higher gate drive is the requisite to uphold linearity. The shift of the peak toward higher gate voltage is not advantageous. Therefore, the device with thicker barrier shows better linearity performance.

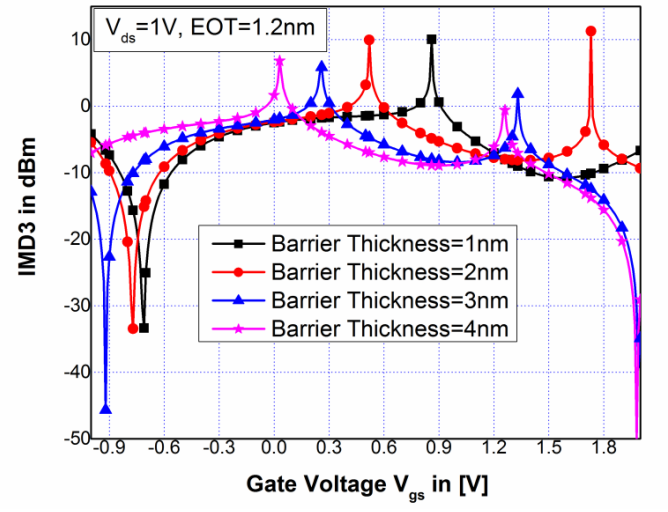

Fig. 6.13: Plot of IMD_3 with the gate-to-source voltage, V_{gs} for different barrier thickness

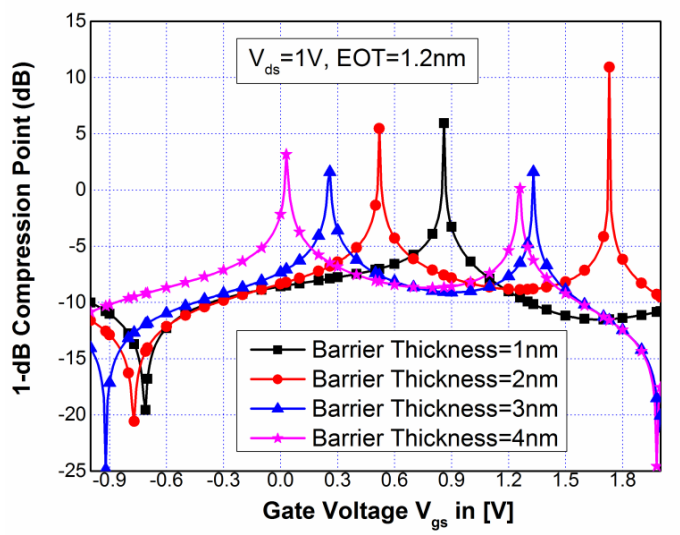

Fig. 6.14: 1-dB compression point plot with the gate-to-source voltage, V_{gs} for different barrier layer thickness

The effect of barrier thickness on "1 dB compression point" is presented in Fig.6.14. As shown in Fig. 6.14, device with thinner barrier presents higher 1-dB compression point in comparison to the device with thicker device. From the obtained results it is understood that the device with thicker barrier layer improves the linearity performance of it. However, too thick barrier layer causes a reduction of gate control and serious short channel effects. Therefore, the analysis shows that the thickness of the barrier layers is a crucial parameter to the gate control on the channel. Hence, require a careful design depending on its applications.

6.6 CONCLUSION

The consequence of barrier layer thickness on the Analog, RF and Linearity performance of an InGaAs/InP heterostructure DG MOSFET has been investigated. From the analysis, it is found that the RF and Analog performance of the device improves as barrier layer thickness reduces. However, the linearity performance worsens as thickness of the barrier layer decreases. Thus, a trade-off is required depending upon the device application area. This work provides the design guidelines for future research and investigation of the heterostrucutre III-V DG MOSFETs.

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CHAPTER 7

PERFORMANCE STUDY USING DIFFERENT CHANNEL COMPOSITIONS OF NANOSCALE HETEROSTRUCTURE MOSFET

7.1 INTRODUCTION

The continuous requirement of complex integrated and highly dense circuits has led to the aggressive downscaling of the MOSFET. However, downscaling (towards nanoscale) leads to short channel effects (SCEs) which adversely affects the RF/Analog performance of the device. To overcome this problem, the new device architecture and material compositions became essential. From the architectural point of view, Double Gate MOSFETs have emerged as one of the most promising devices to investigate [7.1-7.4]. At the same time, the III–V compound semiconductor materials promised significant improvements over silicon, germanium, and other elemental semiconductors because of their electronic band structure and material properties such as higher electron mobility [7.5]. The doping concentration in the source, drain and channel regions is an important parameter to study. Effects of source/drain (S/D) doping density and channel density on the performance of metal-oxide-semiconductor field-effect transistors were studied and reported earlier [7.6-7.9]. It is worth mentioning that in the Heterostructure DG MOSFET also, the channel doping effects are one of the important parameter and is considered in this work. Moreover, the property of InGaAs is intermediate between Gallium arsenide (GaAs) and indium arsenide (InAs) depending on the proportion of Gallium to Indium. Researchers already studied that III -V heterostructures are most important materials for n-channel field effect transistors (FETs) because of its higher electron mobility [7.10-7.15]. Many are working on the implementation of InGaAs and other III-V compound semiconductors as high-mobility channel materials in field effect transistors (FETs) on silicon (Si) so that it can be used for mainstream CMOS technology. Recently, it has been demonstrated that higher Indium (In) mole fraction(x) in $In_xGa_{1-x}As$ influence the performance of the devices and the device performance can be improved by increasing the mole fraction [7.16-7.18]. However, to the best of our knowledge, no such work is available in the literature which addressed the circuit application of such devices and Analog/RF performance dependence on its channel composition. Hence, there is a scope of investigation of

channel composition of the devices to optimize its performances to use it in Analog circuits for low power applications.

In this chapter, a simulation study of Analog/RF performance of the device with varying Indium concentration in InGaAs channel material and effect of variation in channel doping is presented. The device architectures and simulation methodology is discussed along with the detailed results analysis.

7.2 DEVICE STRUCTURE AND SIMULATION APPROACH

The device under study i.e. InGaAs/InP nanoscale heterostructure Double Gate MOSFET is shown in Fig.7.1. The channel of the heterostructure MOSFET is $In_xGa_{1-x}As$ material where effect of mole fraction is studied by varying the value of *x* which indicates the Indium mole fraction. Mole fraction may be defined as the ratio of number of moles of one component to the total number of moles of all the components (solvent and solute) present in the solution. It is denoted by the letter *x*. It may be noted that the mole fraction is independent of the temperature and is dimensionless.

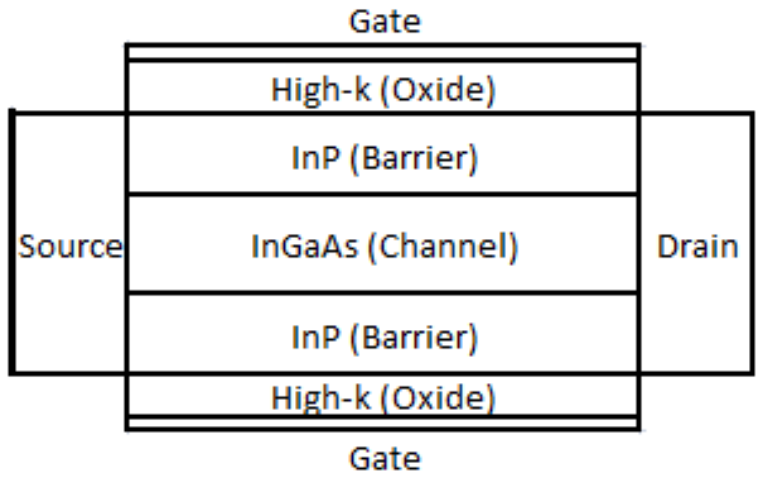

Fig. 7.1: Structure of the InGaAs/InP heterostructure DG MOSFET.

The InGaAs channel material is considered because of its low electron effective mass and high saturation velocities. On both sides of the channel, two InP barrier layers are used. Length of the channel is 12nm and the length of the Source/Drain extension is 2nm. The InGaAs layer is

sandwiched between two InP layers. The InGaAs channel thickness (t_{ch}) is 2nm and the InP barrier thickness (t_b) is 2nm. To minimize leakage currents, oxide with high-k dielectric (HfO_2) is used. The device has source/drain doping concentration of 10^{20} cm^{-3}. The heavily doped S/D was shown to be effective to enhance the current drive and transconductance of III-V channel MOSFET [7.7]. Doping in the channel region is varied to study the effect of channel doping impact.

The device under study is simulated using a 2D structure in device simulator SILVACO ATLAS [7.19]. A two-dimensional numerical simulation using drift-diffusion phenomenon has been performed. "Newton" numerical method has been used for calculation. The Shockley-Read-Hall (SRH) carrier generation-recombination model is used in this analysis. Field dependent mobility model has been considered to model the velocity saturation effect. The device model is calibrated with the experimental data as explained earlier [7.20]. The calibrated model is used for the different simulations carried out here by using different doping concentrations and channel compositions.

7.3 STUDY OF THE EFFECT OF CHANNEL DOPING

A high-k gate dielectric, heavily doped source/drain (10^{20} cm^{-1}) contact, and different channel doping have been considered for the following simulations keeping other design parameters fixed for easy comparison of channel doping effect. Since the n-channel device is studied, the p-type channel with different doping concentrations has been considered. Fig. 7.2(a) shows the Drain current (I_d) as a function of gate voltage (V_{gs}) for different channel doping. The output characteristics are identical and the changes are very little from undoped channel to channel with doping=10^{18} cm^{-3}, while the corresponding changes are higher when the channel doping changes from 10^{17} cm^{-1} to 10^{20} cm^{-1}. From Fig. 7.2 it is observed that that ON current of the device decrease with increase in channel doping. If the gate voltage is fixed, the concentration of the channel doping determines the height of the source to channel barrier; with an increment of the channel

doping at the p channel, the electron inversion is weak; which decreases ON current in the channel.

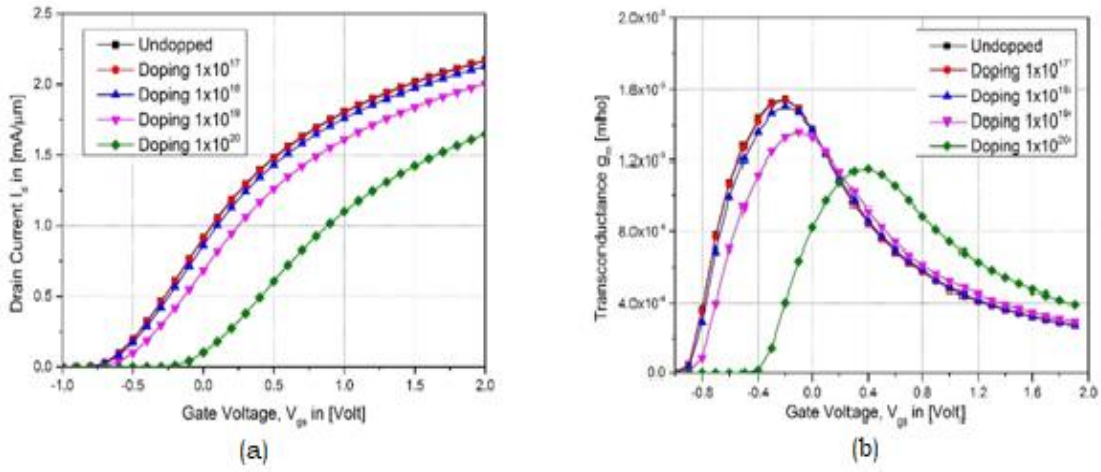

Fig. 7.2: (a)Drain current (Id) as a function of gate to source voltage (Vgs) for different channel doping material (b) Variation of transconduance (g_m) as a function of gate to source voltage (V_{gs}) for different channel doping

Fig. 7.2 (b) shows the transconductance of the device for different channel doping. It is observed that transconductance is decreased with higher channel doping due to the low 2D electron density at higher channel doping. The intrinsic capacitances (gate to source capacitance, C_{gs} and gate to drain capacitance, C_{gd}) are important parameters to compute RF figure-of-merits. The extraction of intrinsic capacitances C_{gs} and C_{gd} are done through AC small signal analysis and used for computation of f_T and f_{max}. The formulae used for computations of these parameters are discussed in previous chapters.

From Fig. 7.3 (a), the variation of f_T can be observed with respect to gate voltage V_{gs}. Here, the value of f_T obtained for a higher channel doping decrease with respect to lower channel doping. From the formulae it is clear that f_T depends strongly on g_m and the total gate capacitance, while f_{max} includes the effect of g_d and source and gate parasitic resistances also. Fig. 7.3(b) shows the variation of f_{max} as a function of gate voltage (V_{gs}) for different channel doping. From analysis, it is observed that both f_T and f_{max} decrease with increase in channel doping. Therefore, for rest of the simulations, undoped channel is used.

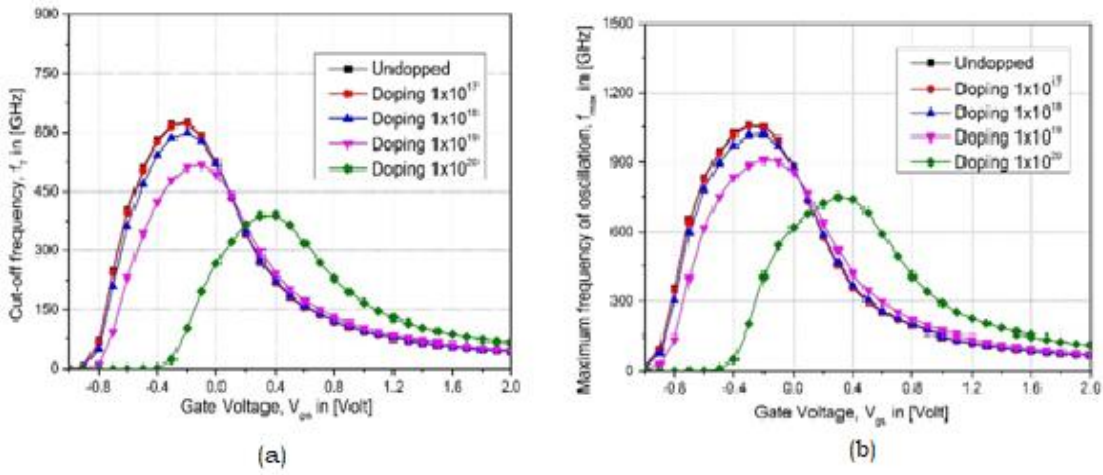

Fig. 7.3: (a) Comparison of the cutoff frequency (f_T) as a function of the gate voltage (V_{gs}) for different channel doping (b) Comparison of the maximum oscillation frequency, f_{max} as a function of the gate voltage (V_{gs}) for different channel doping

7.4 EFFECT OF INDIUM MOLE FRACTION VARIATION

Different RF and Analog performance parameters in the form of transconductance (g_m), transconductance generation factor (g_m/I_d), Cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are studied in this section. Initially, the effect of varying Indium content in the InGaAs channel is studied by calculating different analog parameters by varying the composition of the channel material. The mole fractions of Indium considered for performance analysis are 0.53, 0.58, 0.63 and 0.7 along with InAs and GaAs as channel materials, which represent two extreme conditions.

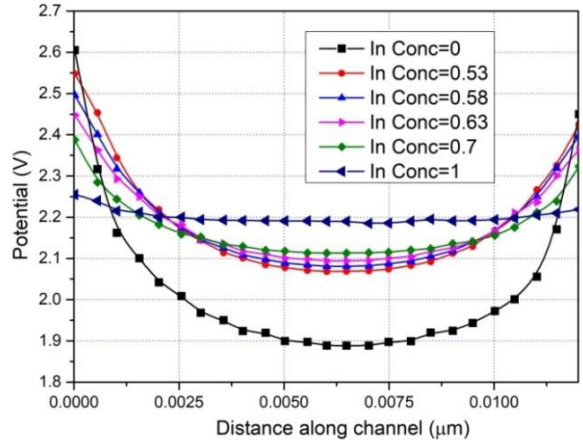

Fig. 7.4: Potential profiles along the channel of the DG heterostructure MOSFET at V_{gs}=1V and V_{ds}=1V

In Fig. 7.4, the surface potential is plotted as a function of horizontal distance in the channel of the Double Gate heterostructure MOSFET. It is observed from Fig.7.4 that as the Indium concentration increase, the peak of potential minimum shifts upward with lowering the boundary values.

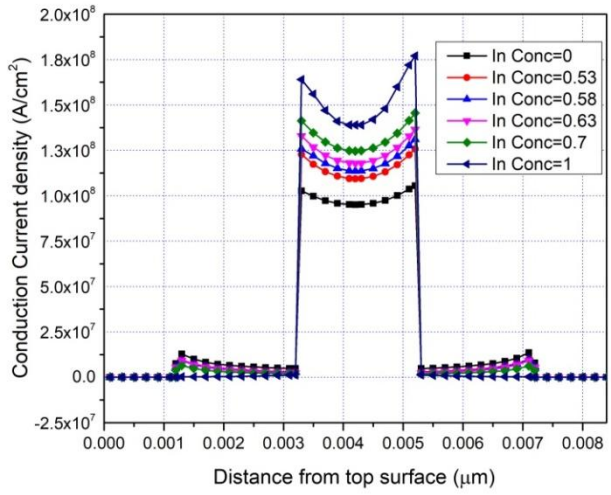

Fig. 7.5: Conduction current density perpendicular to the channel at V_{gs}=1V

Fig.7.5 shows the plot of conduction current density perpendicular to the channel for different Indium concentrations. With increase in Indium concentration, conduction current density in the channel region increases. A sudden change in conduction current density at the channel and barrier layer interface is also observed. Due to differences in electron affinity between the barrier and the channel material, a quantum well is formed allowing mobile electrons to migrate into the channel. The band discontinuities of the heterostructure create the rectangular shaped quantum well having confined high mobility electrons in the channel [7.21]. As a result of electron confinement, there they reside as a thin, high density sheet of electrons known as a two-dimensional electron gas (2DEG). Because of these 2DEG, the concentration of free electrons occurs over a very narrow region close to the hetero-interface [7.22]. The 2DEG stays in InGaAs channel and higher conduction current density occurs in the channel. Moreover, a boost in Indium content in the $In_xGa_{1-x}As$ channel enlarge the conduction band offset between the channel and barrier layer, resulting in improved carrier confinement in the channel [7.23]. The

formation of a 2DEG causes the channel to experience an overall increase in electron mobility. Electron mobility characterizes how fast an electron is allowed to drift through the InGaAs lattice under the influence of an electric field. Thus, when an electric field, in other words a drain voltage, is applied across source and drain, electrons are driven through the channel.

7.4.1 ANALOG PERFORMANCE ANALYSIS

In order to compare the device performance for varying Indium mole fraction in InGaAs channel, analog performance data is calculated and compared with different Indium concentration in $In_xGa_{1-x}As$ channel. The mole fractions of Indium considered for analog performance analysis are 0, 0.53, 0.58, 0.63, 0.7 and 1 with V_{ds}=1 V and V_{gs} varying from -1V to 2V. Fig 7.6 shows the drain current (I_d) as a function of gate-to-source voltage (V_{gs}) for different mole fractions of Indium in the channel. It is seen that the drain current increases as the mole fraction of Indium in the channel increase.

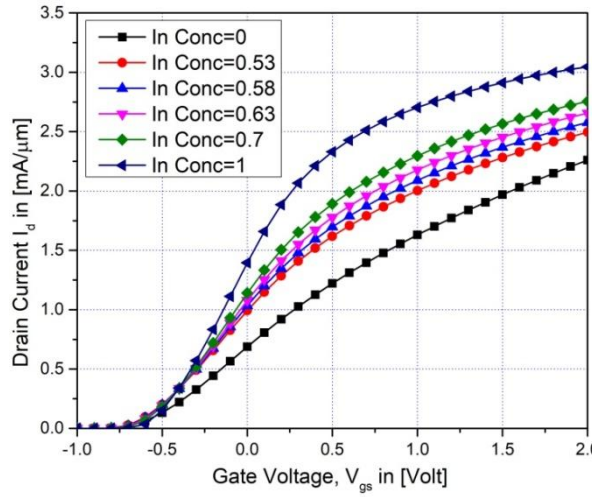

Fig. 7.6: Variation of I_d in linear scale as a function of V_{gs} for different Indium Concentration at V_{ds} = 1 V.

The transconductance of a transistor is defined as the ratio the change in drain current to the gate voltage change ($\delta I_d/\delta V_{gs}$), at a constant drain voltage. Fig 7.7 compares values of transconductance (g_m) as a function of V_{gs} for different Indium mole fraction in the channel. This figure reveals that with the increase in mole fraction of the Indium, transconductance increases considerably. We have observed that both the

maximum drain to source current (I_d) and transconductance (g_m) of the device increases with an increase in the Indium mole fraction (*x)*. This finding matches well with the findings reported by A. V. Thathachary et al. [7.24]. Main reason is that with increasing indium mole fraction, both the low-field electron mobility and saturation velocity increase because of the decreasing electron effective mass [7.25]. It is known that effective mass *m** of electron is inversely proportional to the Indium content in $In_xGa_{1-x}As$, channel, its mobility increases with increase in Indium concentrations. The bandgap energy of $In_xGa_{1-x}As$ is proportional to the indium mole fraction (x), which indicates that the $In_xGa_{1-x}As$ channel with higher indium mole fraction requires lower surface potential (band-bending or the Fermi-level movement) to attain the same density of inversion charges. InGaAs is a ternary compound between indium arsenide (InAs) and gallium arsenide (GaAs) and in order to achieve successful crystal growth without major lattice defects, the channel material should ideally be lattice-matched to the underlying InP substrate. Dislocations caused by lattice mismatch adversely affect the electrical characteristics of a device by creating localized states which act as traps for the charge carriers. $In_{.53}Ga_{.47}As$ is the alloy whose lattice parameter matches that of InP at 295K, whereas the $In_{0.75}Ga_{0.25}As$ layer is at the limit of pseudomorphic growth. Lattice constant of $In_xGa_{1-x}As$ becomes smaller than InP for mole fraction lower than 0.53 resulting a tensile strain in the channel. In contrast, the lattice constant of the InGaAs layer becomes larger than InP for an In molar fraction more than 0.53, and the channel is under a compressive strain [7.26]. This is due to the fact that in channel under compressive strain, alloy scattering decreases which in turn increase the electron mobility. Therefore, increase in Indium (In) mole fraction of the channel improves the ON current of the device. Unfortunately, increasing the Indium concentration in $In_xGa_{1-x}As$ also increases the lattice constant which increases the lattice mismatch with InP layer. Using a buffer layer, crystal growth defects may be reduced, but that degrade the performance of the 2DEG channel. Even though using high indium mole fraction in InGaAs channel material is desired for high electron

velocity [7.27], a trade-off in epilayer composition must be made to compromise between high speed performance and device reliability.

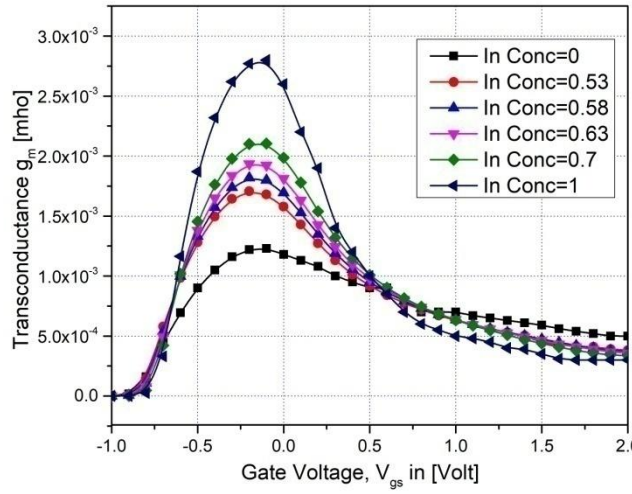

Fig. 7.7: Variation of g_m as a function of V_{gs} for different Indium Concentration at V_{ds} = 1 V.

As, the transconductance (g_m) of the device expresses the gain given by the device whereas the drain current (I_d) specifies the power dissipation to achieve the gain, the ratio is regarded as the available gain per unit power dissipation. So, it is targeted in design to have higher g_m/I_d ratio for better analog performance of the device. Fig 7.8 displays a comparison of (g_m/I_d) as a function of V_{gs} for different Indium content in the channel. From the figure, it is observed that g_m/I_d does not vary too much with the increase in Indium content in the channel.

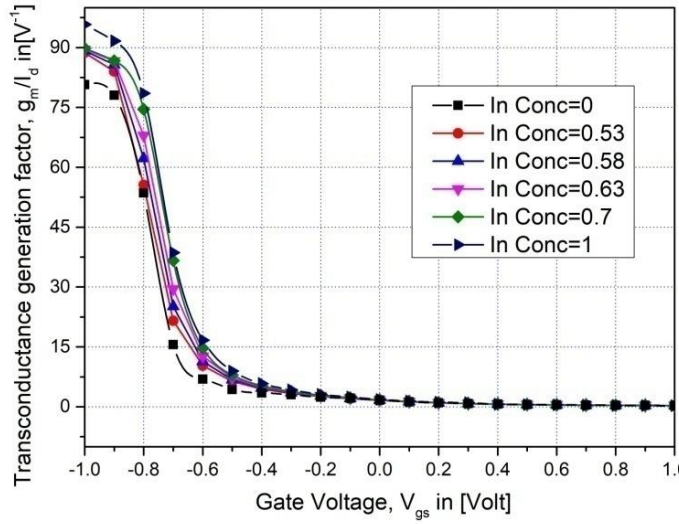

Fig. 7.8: Variation of g_m/I_{ds} with V_{gs} for different Indium Concentration at V_{ds} = 1 V.

7.4.2 RF PERFORMANCE ANALYSIS

As f_T and f_{max} is related to the gate capacitances of the device, C_{gs} and C_{gd} are extracted from the simulation. Fig. 7.9 plots the gate capacitances (C_{gs} & C_{gd}) as a function of gate voltage (V_{gs}) for different Indium concentrations of the channel.

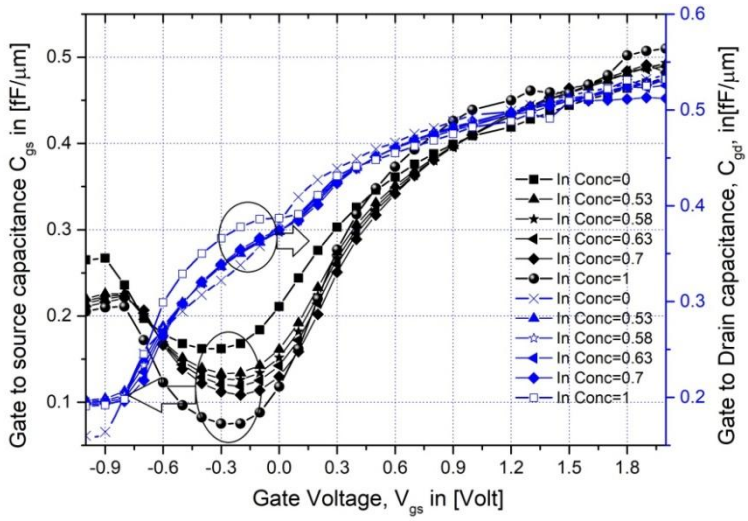

Fig. 7.9: Variation of Gate Capacitances (C_{gs} and C_{gd}) as a function of Vgs for different Indium Concentration at V_{ds} = 1 V.

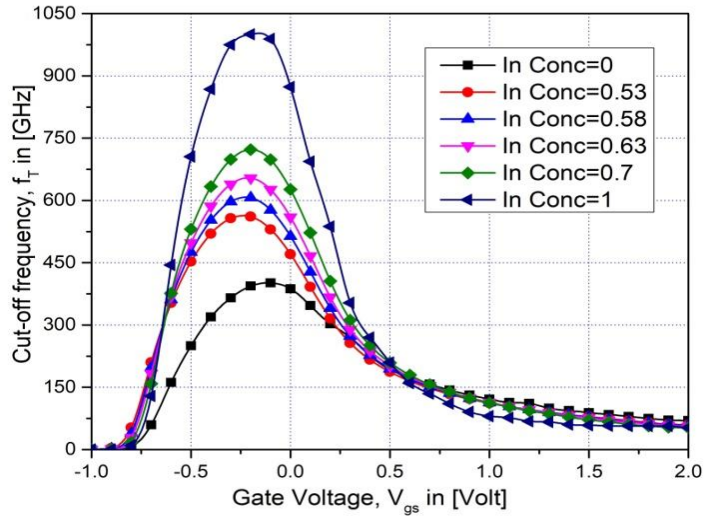

Fig.7.10: Variation of f_T as a function of (V_{gs}) for different Indium Concentration at V_{ds} = 1 V

Fig. 7.10 shows the difference of cut-off frequency (f_T) of the device for different Indium concentrations in the channel. From Fig. 7.10, it is observed that the cut-off frequency is increasing with the increase in percentage of Indium in the channel. This is caused by the improvement in

g_m for rising Indium mole fraction, as noticed in Fig 7.7. Fig. 7.11 plots the maximum oscillation frequency (f_{max}) variation with gate voltage (V_{gs}) for different Indium concentration in the channel. From Fig. 7.11, it is understood that maximum oscillation frequency (f_{max}) of the device increase with increase in percentage of Indium in the channel material.

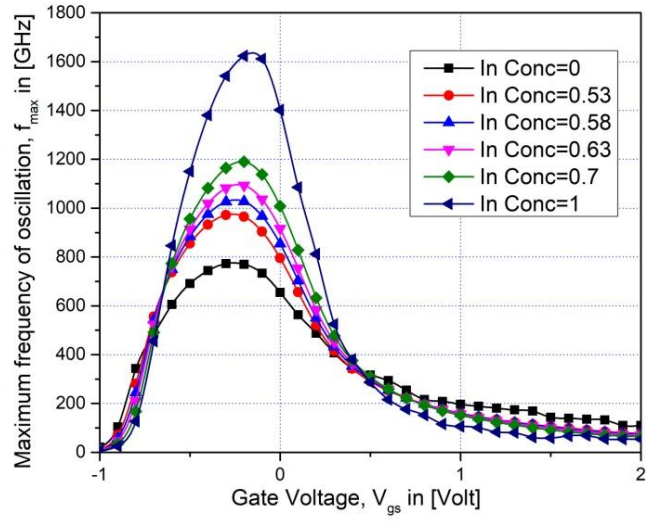

Fig.7.11: Variation of f_{max} as a function of V_{gs} for different Indium Concentration at V_{ds} =1 V

7.4.3 CIRCUIT PERFORMANCE ANALYSIS

Circuit performance was estimated by using the device in a Cascode Amplifier. The Cascode amplifier is a two-stage circuit constructed using two transistors. The schematic circuit diagram of a two stage Cascode amplifier is drawn in Fig. 7.12 where one of the MOSFETs indicated by M_2 is biased by the reference voltage V_r and in the gate terminal of MOSFET M_1, input is applied. In the circuit, one transistor operates as a common source and the other as a common gate configuration. This combination has advantages in terms of higher input-output isolation, higher gain or higher bandwidth, better stability, higher slew rate etc.

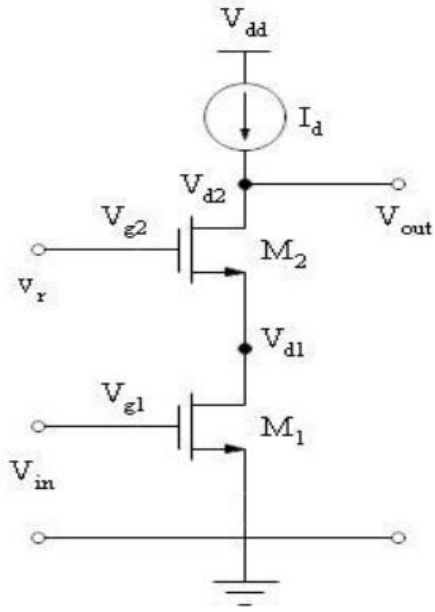

Fig.7.12: Schematic diagram of a Cascode amplifier

The output characteristics of the simulated two MOSFET Cascode amplifier constructed using the device under study is shown in Fig. 7.13. The variation of the characteristics with different Indium concentration is understood from this figure. The devices are specified by width of 1µm and reference voltage of 0.6V is used. Fig. 7.14 shows the variation of the differential gain as a function of input voltage for different Indium percentage. From the figure, it is clear that the maximum differential gain of the device with lower mole fraction is greater than the devices with higher indium content.

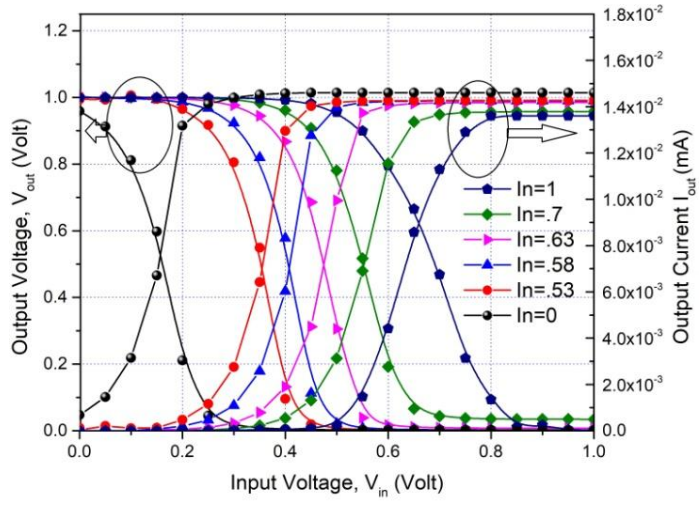

Fig.7.13: Output characteristics of the Cascode amplifier for different Indium concentrations

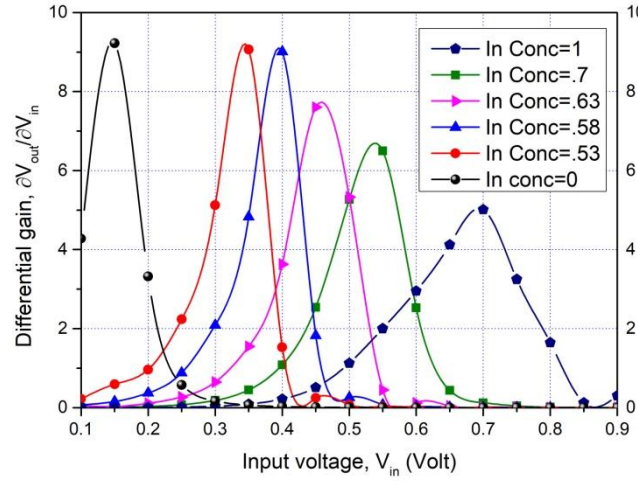

Fig. 7.14: Variation of the differential gain as a function of input voltage

7.5 CONCLUSION

Various device parameters related to analog circuit performance for InGaAs/InP heterostructure MOSFETs have been studied in this chapter. The effect of channel doping concentration is studied first to optimize the channel doping concentrations. From the analysis, it is noticed that the analog/RF performance of the device improves if the channel with lower doping concentration is used. The impact of Indium mole fraction of the channel on Analog/RF performance of the device is investigated. Higher ON current and g_m with increasing Indium percentage has been observed in this study. It is concluded that, the analog performance parameters like transconductance (g_m), transconductance-generation factor (g_m/I_d), cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) increases with increase in mole fraction of Indium in the channel. The device with higher indium content shows improved f_T and fmax. But the differential gain decreases with increase in Indium content if it is used in single stage to multi stage circuit design such as a cascode amplifier. Increase of the Indium concentration in $In_xGa_{1-x}As$ also increases the lattice constant which in turn increases the lattice mismatch with InP layer. Thus, a trade-off in channel composition must be made to optimize the device performance and device reliability. These findings outline the design guidelines to optimize the performance of the device with InGaAs channel.

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CHAPTER 8

CONCLUSION

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SCOPE OF FUTURE WORK

8.1 CONCLUSION OF THE WORK

In this thesis the effect of different device parameters on SCEs and RF/analog performance investigation of nanoscale MOSFET devices has been presented in order to extend the future scaling. In the first phase of work, scaling trends of MOSFETs, recent advancements of MOS-based devices and the problems associated with nanoscale MOS-based devices along with the possible remedies have been studied. Moreover, the limitations of recent device technologies in controlling SCEs have also been considered. These studies on technology trends setup a need of high frequency analysis of the nanoscale devices for SoC applications. Therefore, in this thesis, the applicability of emerging nanoscale CMOS devices for analog/RF applications has been investigated.

In the second phase the performance of the Junctionless Accumulation-Mode (JAM) bulk FinFET for Analog/RF applications have been investigated. Different electrical parameters have been simulated and analyzed for the device with different gate spacer's lengths and materials. From the simulation and analysis, it is observed that the digital and analog performance of the device improve with use of spacers. Different spacer materials having dielectric constant varying from 3.9 to 22 are used as a design parameter. It is observed that, using high-k spacer material, higher ON current; better I_{ON}/I_{OFF} ratio, improved transconductance (g_m) and enhanced transconductance generation factor (g_m/I_d) are obtained. However, the device with high-k gate spacer exhibits lower f_T and f_{max} in comparison to the device with spacers having lower k-value. It is also evident from simulation results that for a given spacer length, SS and DIBL of the device decreases with increase in the gate length. It is found that increase in spacer length corresponds to improvement in SCEs and increase in V_{th} (lower V_{th} roll-off) but simulation results also suggest that RF/analog performance of the device with spacer having high-k dielectric can be improved by reducing the spacer length. So, a trade-off is required to optimize the device performance for analog/RF applications. Common

source amplifier circuit using Junctionless Accumulation Mode bulk FinFET device has been analyzed for assessing the impact of spacer material on frequency response. It is understood that the gain of the circuit improves with using devices having high-k gate spacers. The effect of the variation of the Fin width on the RF/analog performance of the device has also been analyzed and reported. A comparative study is made for the performance of the device with different Fin widths ranging from 10nm to 20nm. From the obtained trends, it is understood that reduction of Fin width can improve the digital performance and it also finds applicability in analog as well as RF applications. The impact of various Fin cross-sectional shapes on junctionless accumulation mode bulk FinFET with short channel length has been evaluated. Fin top width was varied while Fin bottom width is kept constant in order to obtain a realistic Fin shape. Because of this variation, Fin cross-sectional shape changed from rectangular to trapezoidal. From the analysis, it is understood that shape of the Fin cross-section substantially change the device performance. Improvement in SCEs was noticed in terms of reduction of DIBL and reduction in SS for the device with reduced Fin top width. On the other hand, reduced Fin top width degrades the RF performance as maximum frequency of oscillation decreases. Therefore, an optimal Fin structure for the junctionless bulk FinFET is also obtained to have better SCEs and reasonable Analog/RF performance. Current work presents valuable design guidelines in the performance of Junctionless Accumulation Mode (JAM) Bulk FinFET device with optimal spacer region engineering. Thus it is possible to conclude that analog/RF performance of the JAM FinFET device can be tuned by changing the spacer material, spacer length, Fin width, Fin shape, gate length etc..

In the next phase, simulation and analysis of the Analog, RF and Linearity performance of InP/InGaAs hetero-junction MOSFET have been performed and summarized. A detailed investigation of the impact of barrier layer thickness and channel composition on different Analog, RF performance of an InGaAs/InP heterostructure DG MOSFET is carried out. A thorough analysis of the key figure-of-merits is performed for various

barrier thicknesses ranging from 1nm to 4nm. From the simulation results, it is concluded that performance of nanoscale DG heterostructure MOSFET is affected by the variation of barrier thickness of the device. From the analysis, it is established that improvement in RF and Analog performance of the device may be obtained by reducing the barrier layer thickness. However, the linearity performance is seen to be deteriorated as thickness of the barrier layer reduces. From the study of varying Indium concentrations in InGaAs channel, higher ON current with increasing Indium percentage has been observed. It is concluded that, the analog performance parameters like transconductance (g_m), transconductance-generation factor (g_m/I_d), increases with increase in mole fraction of Indium in the channel. The device with higher indium content shows improved f_T and f_{max} also. To investigate the device performance in analog circuit, a circuit simulation is also performed. A Cascode amplifier is designed using the device under study and its voltage transfer characteristics and differential gain is plotted as a function of Indium mole fraction in channel to estimate the device performance in circuits. Differential gain of the cascade amplifier is found to be lower with increase in Indium concentrations. From the fabrication point of view, increase of the Indium concentration in InGaAs channel also increases the lattice constant which in turn increases the lattice mismatch with InP barrier layer. Thus, a trade-off in barrier layer thickness as well as channel composition must be made to optimize the device performance and device reliability.

Overall, it may be summarized that the work is concerned with the design of emerging nanoscale MOSFETs for application in SoC by reducing the detrimental SCEs. It may be concluded that different device parameters such as spacer materials, spacer dimensions, Fin dimensions, channel-materials can be used as crucial device design parameter for high-efficiency radio-frequency integrated circuit design. These findings will be useful for design and optimization of nanoscale MOSFET devices for analog/RF applications with a reduction of SCEs.

8.2 SCOPE OF FUTURE WORK

To make future progress and extension to this study the following research idea could be taken up.

- Since semiconductor materials are sensitive to temperature and IC devices are supposed to work under a wide range of temperature, effect of temperature on device performance should also be simulated. Variation of temperature makes a lot of change in device parameters such as the band gap energy E_g, which decreases with the increase in temperature. The threshold voltage, carrier mobility, flat band voltage etc. are also strong function of temperature. Therefore, self heating effects may be considered for accurate prediction of drain current as well as other device parameters.
- Stain engineering may also be investigated for nanoscale devices. Use of suitable stressor in the structure is a possibility to include stress in the channel and performance improvement. Study of variation of stress due to structural change may be an interesting topic for such nanostructures.
- The proposed devices will be used in some complex circuit. Therefore a detailed circuit simulation is necessary to confirm the device performance and its applicability. In order to carry out the circuit simulation, compact modelling of the proposed device for spice simulator is very important.
- In current work, III-V based heterostructure materials are studied for the device performance improvement. New materials like Graphene, MoS_2 etc. may also be studied as alternative and future generation nanoscale devices.