EXPLORING THE NOVEL CHARACTERISTICS OF HETERO-MATERIAL GATE FIELD EFFECT TRANSISTORS

Thesis submitted by

SAHELI SARKHEL

DOCTOR OF PHILOSOPHY (ENGINEERING)

Department of Electronics and Telecommunication Engineering

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[2] Priyanka Saha, **Saheli Sarkhel** and Subir Kumar Sarkar , "Compact 2D threshold voltage modeling and performance analysis of ternary metal alloy work-function-engineered double-gate MOSFET", in **Journal of Computational Electronics, Springer**, Vol.16.No.3,pp-648-657, June 2017.

[3] **Saheli Sarkhel**, Navjeet Bagga and Subir Kumar Sarkar, " A compact analytical model of binary metal alloy silicon-on-nothing (BMASON) tunnel FET with interface trapped charges" in **Journal of Computational Electronics, Springer**, Volume 16, Issue 3, pp 704–713, September 2017.

[4] Navjeet Bagga, **Saheli Sarkhel** and Subir Kumar Sarkar. "Exploring the asymmetric characteristics of a Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate

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[1] Priyanka Saha, **Saheli Sarkhel**, Dinesh Kumar Dash, Suvam Senapati and Subir Kumar Sarkar, "Analytical Modeling and Simulation of Triple Metal Front Gate Stack DG- MOSFET with Graded channel (GC-TMDG MOSFET)", Springer International Conference on Communication Devices and Networking (**ICCDN 2017**), Sikkim Manipal Institute of Technology, Sikkim from 3rd to 4th June, 2017 and published as **book chapter in Advances in Communication, Devices and Networking: Proceedings of ICCDN 2017 (Lecture Notes in Electrical Engineering), 2018**.

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[1] 2nd International Conference on "Devices for Integrated Circuits (**DevIC 2017**)", Kalyani Government Engineering College during 23rd -24th March, 2017.

[2] Michael Faraday IET International Summit-2015 (**MFIIS 2015**), an IET International Conference during 12th -13th September, 2015, Kolkata.

[3] IEEE 2nd International Conference on Devices, Circuits and Systems (**ICDCS 2014**) during 6th - 8th March, 2014, Coimbatore.

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DEPARTMENT OF ELECTRONICS AND TELE COMMUNICATION ENGINEERING

CERTIFICATE FROM THE SUPERVISOR

*This is to certify that the thesis entitled "**Exploring the Novel Characteristics of Hetero-Material Gate Field Effect Transistors**" submitted by **Smt. Saheli Sarkhel** who got her name registered on **26.11.2014** with Ref. No. **D-7/E/868/14** for the award of Ph.D (Engineering) degree of Jadavpur University is absolutely based upon her own work under the supervision of **Prof.(Dr) Subir Kumar Sarkar** and that neither her thesis nor any part of the thesis has been submitted for any degree / diploma or any other academic award anywhere before.*

Prof. Subir Kumar Sarkar
Supervisor, (Dept. Of ETCE)
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Dedicated to

My Parents & in-laws

Sitansu Sarkhel & Dr.Anita Sarkhel

Tapan Ganguly & Rina Ganguly

Dr.Debmalya Gangopadhyay

&

Dr. Debasree Gangopadhyay

For their motivation

&

My husband

Debjit Ganguly

For his support and cooperation

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Saheli Sarkhel

ABSTRACT

In the present era of human civilization, electronic components have become indispensible in every sphere of life from industrial process control, automation to consumer electronics/wireless communication. In the last few decades, this excessive dependence on process automation and people's desire for lavish lifestyle, increased safety, security and high speed real-time interconnectivity have been propelling the technology boon in industrial automation and state of the art consumer electronics. This rapid growth in the field of electronics has been accompanied by constant device miniaturization in accordance to Moore's law. Reduction of circuit dimension reduces the overall circuit area, allowing more devices on a single die increasing circuit speed, integration density and reducing the cost and power without negatively impacting the cost of manufacturing. Ever increasing trend of device dimension down-scaling to deep sub-nanometer range allows the researchers to explore complex integrated systems on a single chip which drastically reduce their volume and power consumption per function, thereby resulting in a tremendous increase in the speed of operation and increases functionality of electronic devices. However, this fanatic pace of device dimension down scaling cannot continue indefinitely. A series of daunting challenges crop up in the areas of device fabrication combined with some inevitable performance degrading short channel effects which limit further miniaturization of CMOS devices unless these practical challenges are taken care of. Researchers have been working persistently to come up with some innovative non-conventional device structures as possible solutions to the challenges associated with sub-nano device operations. Silicon-on-Insulator (SOI) MOSFET can efficiently replace age old bulk MOSFET by exhibiting superior performance expected from next generation Si technology. Introduction of a buried oxide layer under the channel layer in a SOI structure reduces parasitic capacitances, thereby mitigating several performance deteriorating factors while simultaneously reducing propagation delay ensuring SOI to be a faster device. Moving one step further, the buried oxide of simple SOI structure can be replaced with air having a lower dielectric permittivity than oxide realizing a new Silicon-on-Nothing (SON) structure. SON is practically an improvised version of basic SOI capable of exhibiting momentous improvement in device operating speed and performance by further reducing the capacitive effects of parasitic junctions. Moreover, strain may also be incorporated in the channel region of a conventional MOS structure to enhance carrier mobility and realize notable increase in current drive and operating speed. Apart from the SOI/SON technologies, another research avenue is to realize 'multiple' gate MOSFETs exhibiting better control of gate electrode over the conducting channel capable of enhancing current drivability, mitigating SCEs, improving sub-threshold slope, thus ensuring better scalability. Gate material engineering can be also considered as an emerging research area where the vertical gate electric field and subsequently the overall electric field in the channel region of nano scale devices can be

adjusted by placing two or more metals with dissimilar work functions adjacently as a single gate electrode and the potential profile shows a sudden step due to work function disparity which is particularly effective to mollify Drain Induced Barrier Lowering (DIBL) related issues. The concept of gate material engineering can be extended to a further extent by considering binary metal alloy as gate electrode material where the individual work functions of the constituent metals are continuously varied spatially so that the gate electrode has different values of effective work function at different positions along channel direction. This unique feature of spatially varied work function reduces surface potential profile asymmetry in short channel devices, thereby improving the performance due to DIBL attenuation. Moreover, the most critical issue of precisely sharp source/drain junction formation in every nano dimensional junction based devices can be dealt with by employing Junctionless (JL) devices where the type and concentration of source and drain doping are essentially same as that in the channel region, thereby eliminating the formation of any junction, and consequently annihilating impurity dopant diffusion associated with severe concentration gradient across the junction. In spite of a number of endeavours to develop innovative MOSFETs, one of the basic drawback of MOS technology is the limiting value of subthreshold slope achievable impeding the use of MOSFETs in applications where power consumption is a crucial issue. The principle of carrier tunnelling enables Tunneling Field Effect Transistor (TFET) to overcome MOSFET's thermal limit of 60 mV/dec and to achieve much reduced value of subthreshold slope. Thus, TFET can be regarded as a potential candidate for next generation ultra low power, ultra low voltage applications. Developing an accurate analytical model is mandatory for gaining in depth knowledge about the operation of these newly emerging devices.

In view of this, the thesis presents a comprehensive analytical study of the improved characteristics of several hetero-material gate Field Effect Transistors by embodying the extreme exploration of the pioneering concept of gate material engineering. The analytical results obtained from different proposed device structures studied throughout this dissertation are compared with relevant simulation results to establish the supremacy of these devices as possible alternatives for future semiconductor industry.

Contents

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List of Abbreviations

VLSI	Very Large Scale Integration
ULSI	Ultra Large Scale Integration
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
SCE	Short Channel Effect
DIBL	Drain Induced Barrier Lowering
HCE	Hot Carrier Effect
SOI	Silicon on Insulator
FD SOI	Fully Depleted Silicon on Insulator
PD SOI	Partially Depleted Silicon on Insulator
SON	Silicon on Nothing
BL	Buried Layer
BOX	Buried Oxide
SG	Single Gate
DG	Double Gate
DMG	Dual Material Gate
DMDG	Dual Material Double Gate
DGFET	Double Gate Field Effect Transistor
DMGFET	Dual Material Gate Field Effect Transistor
CG FET	Cylindrical Gate Field Effect Transistor
QG FET	Quadruple Gate Field Effect Transistor
WFEG	Work Function Engineered Gate
LGADG	Linearly Graded Asymmetric Double Gate
JL DG MOSFET	Junctionless Double Gate Metal Oxide Semiconductor
JL CG MOSFET	Junctionless Cylindrical Gate Metal Oxide Semiconductor
TFET	Tunneling Field Effect Transistor
BMASON	Binary Metal Alloy Silicon on Nothing

Chapter I

Introduction and organization of thesis

CHAPTER I

1.1 Introduction:

Modern semiconductor industry is showing tremendous progress to quench the ever increasing technological needs of today's tech savvy generation in every possible domains starting from industrial process control, automotive improvisations to day-to-day consumer electronics gadgets like personal computers, smart phones, high definition television, high speed internet connectivity, wireless communication and so on. The unwarranted dependence on automation for a better lifestyle, safety, security and high speed real time connectivity has been the major driving force behind the present boon in VLSI/ULSI industry. Increasing need of smart electronic gadgets requires the realization of a whole host of complex functionalities from a single electronic device which entail the conglomeration of a gigantic number of circuit components into a single semiconductor chip so as to propel the Integrated Circuits (ICs) from the domain of Very Large Scale Integration (VLSI) to contemporary Ultra Large Scale Integration (ULSI) domain. This accrescent demand of complex ICs can only be satisfied by continuously down scaling the dimension of individual device components allowing the manufacture of more number of devices on a single piece of semiconductor wafer, thereby reducing the overall circuit area without negatively impacting the cost of fabrication while simultaneously enhancing the achievable circuit speed, package density and reducing fabrication cost and circuit power consumption [1.1]. This unique feature of device dimensions scalability of Complementary Metal Oxide Semiconductor (CMOS) transistors acts as a catalyst behind the boon in microelectronics industry. Continuous down scaling of device dimension to quasi-nanometer regime allows the realization of more complex ICs which drastically reduce the circuit volume and power consumed by each operating functional unit, thereby resulting in a momentous circuit speed enhancement [1.2-1.4].

The gradual shift of the developing microelectronics industry to nano-electronics is attributed by the aggressive miniaturization of the physical dimension of semiconductor devices

which doubles the number of transistors per chip in 24 months as predicted by Gordon Moore. Since the late 1960s, the number of transistors on a silicon chip has followed an exponential dependence. The Moore's law dates back to 19 April 1965 and it was presented in the article "Cramming more components onto integrated circuits" published in the Electronics magazine [1.5], by McGraw-Hill editors. The author himself, Gordon E. Moore envisaged that the number of individual transistors per integrated circuit chip (the so-called microprocessor performance) would continue to double every 24 months. Ten years after this prediction, a memory with a density of 65000 components was in production at Intel in agreement with Moore's prediction. Depending on Moore's law, the feature size is continuously shrinking as the transistor number increases and this trend continues until a value of 14 nm in 2020, as it is depicted in Fig. 1.1 below.

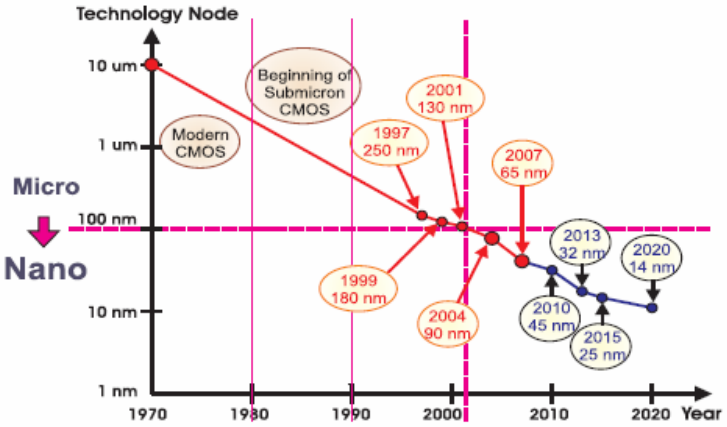

Fig. 1.1 Roadmap for feature size

This observation has been later categorized as the Moore's law [1.5]. Moore's prediction has been set as the benchmark in semiconductor industry which being followed over four long decades till date dominated by the persistent demand for increased device performance. The natural advantages of an ultra scaled device in nano meter regime is high current drivability and densely packed chips, resulting in high speed circuit operations and implementation of a variety of complex functions in a single IC chip thereby producing high end consumer products at much reduced cost [1.6]. Following Moore's trend, the International Technology Roadmap for Semiconductors (ITRS) 2013 [1.17] predicts that the physical dimension of individual transistor will go down around 10nm threshold by the year 2020-2025. As a consequence, the physical gate length will be scaled down from 32nm(2008) to 5nm (2028). The MPU/ASIC half pitch and gate length trends in ITRS 2013 are depicted in Fig. 1.2.

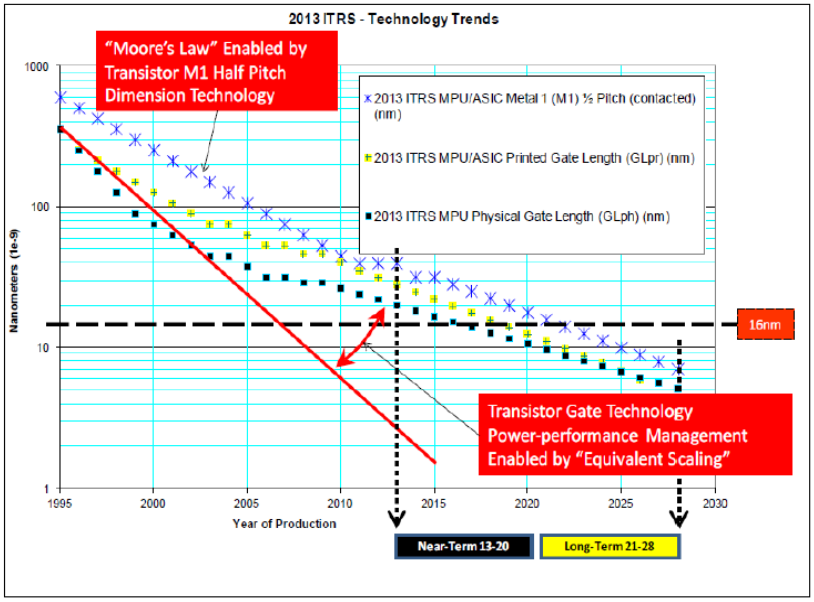

Fig. 1.2. MPU/ASIC half pitch and gate length trends in ITRS 2013

This insistent scaling demand as predicted by ITRS, has now left semiconductor industry at a cross road. Plenty of challenges crop up in many areas of nano dimensional device fabrication along with the issues related to leakage current which turn out to be the main deterrent in continuing the explosive growth in CMOS devices in near future. Fig:1.3 illustrates the progression of the transistor performance as the transistor technology continues to advance.

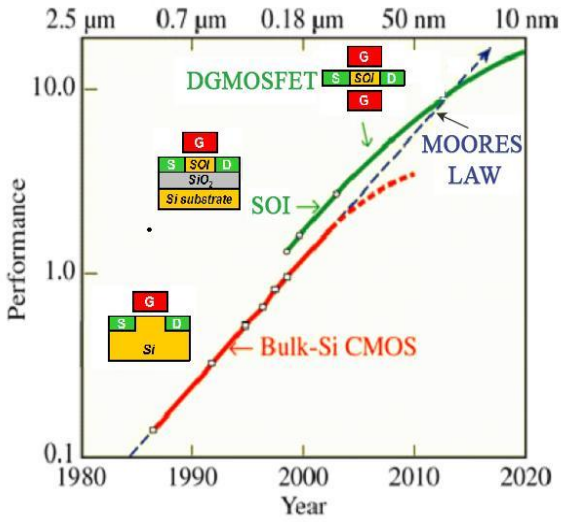

Fig: 1.3: Transistor evolution of structure and performance with size scaling

Traditional scaling technique involves a reduction in channel length and thickness of the MOS gate oxide along with simultaneous increase in channel doping concentration. The frantic scaling pace in

accordance with Moore's prediction as evident from Fig.1.3 above is impossible to be achieved by continuing the traditional scaling technique indefinitely. However, the unrelenting need for low power consuming, cost effective and high speed devices is continuously motivating the semiconductor researchers to explore innovative device structures with new material system to sustain the performance requirements described by ITRS. Further miniaturization without sacrificing functional efficiency can only be possible by combining the joint efforts of device miniaturization, innovative device structures and improved material property, which is again limited by the fundamental physical constraints in order to meet the aggressive specifications of the ITRS.

Operation of the down sized devices in sub-micrometer and nanometer regime is continuously affected by several unavoidable factors cumulatively termed as Short Channel Effects (SCEs) which are solely responsible for degrading the short channel device performance, thereby limiting pace of device dimension miniaturization as foreseen by Moore. Some of the major performance deterrents are reliability issues, direct tunneling, gate depletion, boron penetration and most importantly the short-channel effects (SCEs) such as Threshold Voltage roll Off (TVRO), Drain-Induced Barrier Lowering (DIBL), Hot carrier effect (HCE), Sub threshold conduction and junction leakage currents.

In order to be commensurate with the ongoing trend of device dimension miniaturization shown in Fig. 1.1, researchers are being continuously motivated to adopt several non-conventional geometry device structures which can eliminate the tribulations associated with conventional planar MOS structure. The schematic roadmap of future non-conventional devices is shown in Fig. 1.4 below.

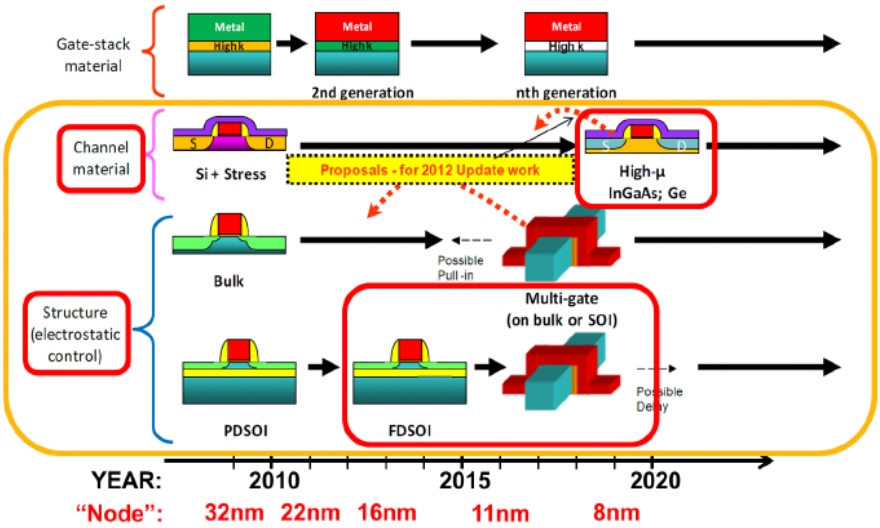

Fig. 1.4 Schematic diagram of ITRS roadmap

According to the report published by ITRS in 2009, few probable candidates as alternative MOS structure of 22 nm or 16 nm nodes are Carbon Nanotube FETs, Graphene Nanoribbon FETs, Nanowire Field-Effect Transistors (NWFETs), III-V channel replacement devices, Ge channel replacement devices etc. Moreover, several unconventional geometry MOS structures like devices with strain induced silicon channel, Multiple Gate devices and Silicon-on-Insulator (SOI) MOS structures have been considered experimentally as well as theoretically in recent times and they have exhibited improved performance in presence of several performance deterring SCEs while operating in nano dimensional region.

Out of several possible non-conventional MOS structures, Silicon-on-Insulator (SOI) MOSFET can be well thought-out as a potential alternative to conventional long channel MOSFETs by virtue of its superior performance as expected from next generation Si technology. Incorporation of a buried oxide layer under the channel layer in a SOI structure results in reduced SCEs, improved sub-threshold characteristics, reduced parasitic junction capacitances resulting in lower propagation delay, ideal device isolation due to reduced coupling effect, high radiation tolerance, reduced layout area, reduced junction leakage currents and latch-up prevention. In spite of providing so much improvement over the conventional bulk MOS, SOI structure, however, is not completely immune from the unavoidable short channel effects in nano regime [1.8-1.10]. These shortcomings of conventional SOI undoubtedly necessitate the incorporation of some additional improvisations on the basic nano dimensional SOI structure to alleviate the associated SCEs. Some the different proposed improved SOI structures are FD SOI having ultra thin body with raised source and drain, FDSOI MOSFET with Metal Source and Drain, Metal gate FDSOI, Multiple-Gate FDSOI MOSFET, Ground-Plane FDSOI MOSFET, HALO Doped SOI and **buried oxide engineered SOI**.

Recently, remarkable research activities are been experimented on an improvised SOI structure where the simple buried oxide layer is replaced with air having a lower dielectric permittivity than oxide resulting in the new Silicon-On-Nothing (SON) structure which effectively lessen the parasitic source-channel and drain-channel capacitances leading to significant improvement in circuit speed. By virtue of this BOX permittivity engineering technique, the SON structure reduces fringing field related DIBL or 2D charge sharing effect, indicating quasi-total suppression of SCEs compared to conventional SOI counterpart [1.11-1.16].

Furthermore, in the search of structural improvisations, '**strain engineering**' can also be another prospective option with enhanced functionalities. Introduction of a layer of SiGe over the bulk silicon substrate of a MOSFET incorporates strain into the silicon channel which generates significant stress on the strained channel, resulting in considerable energy shifts and distortions in energy band spectrum of the channel. This in turn enhances the mobility of channel carriers, thereby

improving device threshold voltage characteristics indicating that strained devices achieve high operational speed rendering them as suitable alternatives for high speed circuits [1.17].

Having explored several structural modifications on the basic MOSFET structure by introducing a BOX layer, buried oxide engineering and strain engineering, one more area of innovation is possibly in altering the gate properties. For nanoscale devices, the dimension of device channel length is in sub 100 nm range resulting in the unwanted infringement of electric field lines from the drain into the channel region, which can be understood by lowering of potential barrier by the drain bias. This shortcoming can be answered by adopting '**gate engineering**' technique where multiple gates are used to direct the flow of carriers through the channel resulting in what we call 'multi gate' devices. By using multiple gates, the conducting channel region (also known as 'finger' or 'fin') is wrapped by the gate electrode increasing the gate-to-channel coupling, which effectively increases the overall control of gate electrode on the silicon channel providing better scalability, improved sub-threshold slope and higher current drivability [1.18-1.26]. Some of the popular multi gate structures gaining research significance comprise of double-gate transistors, triple-gate transistors, quadruple-gate transistors, gate-all-around transistors, π-gate transistors, Ω-gate transistors, DELTA transistors and vertical pillar MOSFETs etc.

Till now, the different improvised device structures discussed are primarily some structural modifications on the basic conventional junction-based MOS transistors. The performance improvements realized by exploring modifications on the basic MOS structure are somehow limited by the major drawback of ultra sharp source-to-channel and drain-to-channel p-n junctions associated with any junction based device. If the channel length is considered to be as small as around 10 nm, ultra-sharp source and drain junctions will be formed where highly doped source and drain regions are separated from the low doped channel by a very sharp junction having significant difference in doping concentration over a separation of a few nano-meters. This drastic concentration gradient imposes stringent conditions on techniques associated with impurity doping and thermal estimations [1.27]. One possible way to surmount this restraint is to adopt a completely new alternative device structure, namely Junctionless (JL) transistor where the type and concentration of source and drain doping are essentially same as that of the channel region, thereby eliminating any junction and impurity dopant diffusion associated with severe concentration gradient across the junction [1.28-1.29]. This relaxes the thermal budget and realizes superior turn-on and output characteristics, near ideal sub-threshold swing, sufficiently high ON-current, and interesting temperature behaviour in the Junctionless devices mainly due to the fact that as the impurity concentration becomes significantly high, the mobilities of channel carriers exhibit average sensitivity on temperature [1.28].

Aggressive device dimension miniaturization has become crucial in order to equiponderate Moore's frantic scaling trend to sustain the escalation of semiconductor industry. The above discussion suggests that continuous down scaling is getting limited by the performance deterring factors in nanometer regime. The unhindered pace of Moore's scaling trend can only be maintained through a calculated permutation of device scaling, innovative device structures and improved material property, which is again limited by the fundamental physical limits to assure the aggressive specifications of the ITRS. Another approach to achieve better device performance is by introducing the idea of the '**gate material engineering**'.

From the basic study of MOSFETs, it is well understood that polysilicon has been an obvious choice as the material of gate electrode. However, poly-Si gates were seen to be affected by some unavoidable short channel effects, boron penetration and formation of depletion regions in polysilicon preventing poly-Si from being a natural choice for gate electrode [1.30], which are gradually being replaced by metal gates [1.30]. The metal gates in turn have some stringent limitations such as chemical or thermal instability with high-k dielectric, work function sufficiency, passivation of interface charges, plasma damage due to reactive ion etching or material deposition or cross contamination issue [1.31]. This opens up quite a few research opportunities on '**gate material engineering**'. The basic motivation behind this is the fact that in low dimensional devices, electric field at any point within the channel has two factors: one is the vertical field (controlled by gate bias) and the other is the horizontal field (controlled by drain bias). Thus the overall electric field can be modulated by suitably adjusting the vertical gate electric field by the incorporation of dual or triple materials, with different work functions, side by side as a single gate electrode, altering the overall field and consequently improving performance [1.32]. Numerous research outcomes on this concept suggest that the use of Dual Material Gate (DMG) or Triple Material Gate (TMG) results in a step-like feature in the channel potential profile screening or protecting the source-channel junction from any random variation in drain bias, thereby mitigating several short channel effects and enhancing device scalability.

This concept of 'gate material engineering' can be further extended to an altogether different level by considering a binary metal alloy ($A_\alpha B_{1-\alpha}$) as gate electrode where the mole fraction concentrations of individual pure constituent metals are continuously varied from being 100% A at the source side to 100% B at drain side establishing the concept of '**work function engineered gate**' or '**binary metal alloy gate**' or '**linearly graded gate**'. The vertical field and consequently the overall field in this system will be adjusted by the incessant variation of work function to reduce the asymmetry in the profile of surface potential in an ultra low dimensional device [1.33-1.42]. This in turn controls the DIBL significantly and improves the device performance by removing the uneven transition of surface potential and surface electric field.

Apart from the various unwanted short channel effects related with the operation of ultra scaled conventional MOSFETs, one of the most significant drawbacks of MOS technology which makes it unsuitable for application requiring low power consumption is the limitation to achieve subthreshold slope below thermal limit. At room temperature MOSFET requires minimum gate voltage of 60 mV to increase the current by magnitude of one order [1.34] limiting the value of minimum attainable subthreshold slope to be 60 mV/dec. Tunneling Field Effect Transistors (TFETs) exhibit significant improvement over MOSFETs in terms of reliable device operation, reduced leakage current during OFF state, inherent ability to achieve subthreshold slope below the limiting value of 60mV/dec and reduced SCEs (due to built-in tunneling of electrons). By virtue of above mentioned improved characteristics, TFETs can be regarded as an appropriate alternative device to MOSFETs for circuit applications driven by very low voltage and requiring very low power consumption. Several improvisations on TFET structure (for example, based on 'gate engineering' and 'gate material engineering' techniques) are also being proposed by contemporary researchers.

From the discussion presented above, it appears that there are plenty of opportunities for innovations in the area of semiconductor devices urging researchers to develop new alternative devices with superior performance in terms of lower power consumption, high package density and high speed operations in order to cope up with the ever expanding technological demand.

1.2 Literature Survey

The last few decades have witnessed tremendous boost in the development of nanoscale semiconductor devices. Instead of simple scaling, SOI MOSFET has been recognized as a possible choice for increasing the performance of MOSFET [1.35]. Although the development processes have begun in early eighties, the IBM Research Division launched a new program in 1989 on the device design of SOI based CMOS and related material research [1.36]. The development of SOI was initiated in the early 1990s at the Advanced Silicon Technology Center (ASTC) of the IBM Microelectronics Division. The year 1994 saw the development of a "fully" functional Power PC [1.37] using CMOS SOI technology as an outcome of those research efforts.

Following this significant development, the current-voltage characteristics of the SOI device has been studied based on exhaustive analytical modeling considering the front channel to be in strong inversion region of operation while the back channel was considered to be either in accumulation or in depletion [1.38-1.39]. Extremely small device dimension requires that the device threshold voltage should also scale down for low voltage operation [1.40]. The dependence of the

threshold voltage of SOS (silicon on sapphire) MOSFET on the epitaxial film thickness has been considered by Sasaki and Togei [1.41] in 1979.

A rigorous two dimensional numerical model for threshold voltage (V_{th}) has been developed by Sano et. al.[1.42] in 1980 by including its dependence on back gate bias. Concurrently, an analytical calculation based threshold voltage model for an SOS MOSFET was developed by Worley [1.43] considering coupling of induced charges between the front and the back gates in the same way as seen in *SOI MOSFET* excepting the fact that only the back surface of the silicon channel was assumed to be depleted in this case. A model for threshold voltage was proposed by H. K. Lim et. al. and Depletion approximation I-V model was developed by P. W. Barth et. al. in 1983 [1.44]. Lim and Fossum [1.45] in 1983 studied charge coupling between the front and back gate by considering a general steady state analysis which eventually developed closed form expressions for *threshold voltage* under every possible steady state charge conditions. A current-voltage model (1984) and a charge-based large-signal model (1985) was developed by H. K Lim et. al. [1.46-1.47]. The variation of the linear region channel conductance on the applied back gate voltage and other device parameters was also discussed. Ballestra et. al. [1.48] in 1985 considered both n-SOI and p-SOI MOSFETs to study the effects of the interface parameters on the back and the front threshold voltages [1.49].

The requirement of the ultra low dimensional devices to consume ultra low voltages mandated research initiatives to explore device subthreshold characteristics. The subthreshold swing is a figure of merit which gives an idea about the subthreshold behavior of a *MOSFET*. A low value of this subthreshold slope indicates reduced leakage current and enhanced overdrive voltage required for high speed. The dependence of the subthreshold swing (***S***-factor)* with current drivability of the *MOSFET* has been studied for the device dimension down to *0.1 μm* [1.50].
In the subthreshold regime, the presence of a floating body (of *PD SOI* device) results in a reduction in the subthreshold slope lower than the theoretical value of *60 mV / decade* for an ideal *MOS* transistor at room temperature. In 1986, it was further observed by Davis et. al.[1.51] that an n-channel SOI MOSFET exhibited a better subthreshold slope of about 50 mV/ decade. Vivid understanding of the subthreshold characteristics of floating body SOI MOSFET is very much crucial to design and model circuits. The previous S-factor studies were carried out considering a simplified potential profile variation along only one direction of the SOI MOSFET and thus cannot be applied to short channel devices where the potential profile varies in both vertical and horizontal directions. Double Gate FD SOI MOSFETs require two-dimensional analysis of subthreshold behavior based on numerical analysis as reported in [1.52-1.53].

In 1987, a subthreshold current-voltage model for a submicrometer FD SOI MOSFET was proposed by Fossum [1.54]. It was observed by Fossum [1.55] that the device current was abnormally large while operating in subthreshold regime and the above study related this current behavior to

the floating body effects initiated by high field impact ionization near the drain end. Again in 1987 only, the Green's function technique was implemented to solve 2D Poisson's equation by Lin and Wu [1.56] for a bulk MOSFET.

In 1987, a novel device structure called Volume Inversion Double Gate SOI MOSFET was reported by Balestra and Cristoloveanu. Here, a thin Si film was sandwiched between a thin gate oxide and a comparatively thicker buried oxide and bias was applied simultaneously to both the gates. Device operation was considered to be a blend of two MOSFETs working simultaneously in parallel. The concept of "Volume Inversion" was applied here to achieve enhancement in current drive and to reduce the impact of surface-induced scattering events and interface defects [1.57]. In the very next year, Susan Edwards and Kevin Yallup analyzed the floating region of SOI MOSFET using two dimensional numerical simulations. In their work, the floating region formed in the bulk silicon film was highlighted in the simulation. As this region is not connected to any external electrode, they can act as a trap for charge generated by avalanche ionization and the trapped charges inside the floating body can influence the device output characteristic which is termed as kink phenomenon [1.58].

Later in that year, a model based on charge sharing was formulated by Veerraghavan and Fossum al. [1.59] which predicted a L^{-1} threshold voltage dependence considering surface potential to be constant and independent of drain bias variation. However, this model does not include the important issue of Drain Induced Barrier Lowering (DIBL) and coupling between the front and the back gates remain. So this model must use *a priori* charge sharing model, which requires empirical fitting parameters. These parameters, being difficult to compute, are not suited for modeling.

In 1989, K. K. Young proposed an analytical model for the formulation of threshold voltage of a short-channel FD SOI MOSFET based on the solution of 2D Poisson's [1.60]. That model has included both vertical and lateral electric field effects under parabolic potential profile approximation. At the same time in that year only, an innovative concept of split-gate structure was proposed by Shur et. al. [1.61]. Later on, the Dual Material Gate structure had its roots from this particular concept of a split-gate connected to different gate-voltages. But, this concept had the limitation of handling noticeable fringing field capacitance between the two amalgamated metal gates, which increases with the decrease of separation between the two gates. Some asymmetric structures were also investigated [1.62-1.63] in which the distribution of electric field in the channel was considered to be continuous.

In 1990, Jason C. S. Woo et. al. adopted a new technique based on infinite series method to numerically solve the Poisson's equation of a SOI MOSFET [1.64]. The said model included both the thin silicon channel along with the gate and buried oxide regions. Later in that year, Francis Balestra et. al. proposed a reliable model based on analytical calculations for thin-film and ultra-thin-film SOI MOSFET considering two or three interfaces [1.65]. This model considered the linear

variation of channel potential in the Si film, which has been inferred by standard simulation results. This model also initiated the concept of Compact Capacitive Model which has been considerably studied by some other researches later on. Simultaneously, the temperature dependence of ultra thin n-channel SOI MOSFET threshold voltage was studied by Groeseneken [1.66]. Studies by Matloubian et. al. [1.67], on the other hand, established that measurable shift in threshold voltage with an improvement in subthreshold slope can be observed in *n*-channel *SOI MOSFETs* with floating bodies considering higher drain biases. This improvement was brought by the positive feedback between the body potential and the channel current of the transistor.

Tokunaga et. al. [1.68], in 1991, considered an n-channel FD SOI MOSFET in submicron regime and exhibited the variation of subthreshold slopes with applied substrate bias, operating temperature and drain bias. The results of measurement show that for a low drain voltage, the experimental results can be illustrated by the model of a simple capacitor. It was seen that if the drain voltage was large, the subthreshold characteristics were anomalously sharp for a high value of applied negative voltage at the substrate. The results also suggested a qualitative model based on the charge state of the lower SOI interface to elaborate the anomalous effect of substrate bias.

Fully depleted devices exhibit significantly smaller variation of threshold voltage with temperature as compared to bulk devices. The dependence of threshold voltage on the depletion level was also discussed. The variation of *Vth* resulting from the randomness in the distribution of doped impurities considering both conventional and *SOI MOSFET* was discussed by Chen and Li [1.69] in 1992. It was evident from their study that the threshold voltage of a *Double Gate FD SOI MOSFET* is much more immune to inevitable fluctuations in dopant atom distribution. The design considerations required to minimize the statistical threshold voltage variation was also discussed.

For many years, the basic limitation for IC designers has been the conglomeration of an ever increasing number of devices with high yield and reliability. With the device physical size approaching deep submicron regime, the behaviour of a conventional MOSFET approaches that of a resistor [1.70]. Increasing the concentration of dopants leads to an increase in device threshold voltage which therefore solves this problem. However, this in turn requires an increase in the supply voltage and a higher capacitance, which thereby results in higher power dissipation and low speed which are naturally undesirable. So, a trade off is required. Depending on Brew's empirical scaling rule [1.71], some guidelines for designing SOI MOSFETs were advocated by Yan et. al. [1.72] in 1992. Several structural variations of conventional SOI structure were proposed in terms of natural length scaling. 1992 was also significant for the inception of a technique to solve two dimensional Poisson's equation for short channel *MESFETs* using Green's function, as contemplated by Chin and Wu [1.73].

In 1993, Guo and Yu [1.74] proposed a scheme for evaluating an exact solution of the two dimensional Poisson's equation of a FD SOI MOSFET based on three zone Green's function

technique. Again in 1993, subthreshold slope was investigated for ultrathin fully depleted SOI MOSFET considering different channel lengths starting from the long channel region down to 0.1 μm. This study inferred that the S factor degradation in short channel devices is governed mainly by three factors [1.75]:

- An increase in the source-channel and drain-channel capacitances resulting from the two dimensional distribution of the channel potential profile
- the unwanted subthreshold conduction at the interface of back-gate and channel and
- the modulation of effective thickness of the channel through which current flows during the gate voltage swing in the subthreshold region

In 1994, Tommy C. Hsiao et. al. presented an analytic current-voltage model for sub-micrometer fully-depleted SOI MOSFET [1.76]. One year later the same research group has presented an analytic current-voltage model in sub-threshold regime [1.77]. The drain voltage dependence of the effective depleted charges, substrate region voltage drop just beneath the buried oxide layer, enhancement in current conduction induced by drain bias, source-drain series resistances, Threshold Voltage Roll-Off and Drain-Induced Barrier Lowering effects have been incorporated in these models.

In the same year, 1995, Srinivasa R. Banna et. al. developed a threshold voltage model for short channel SOI using a quasi-two-dimensional approach similar to the models used for evaluating the current in the substrate, threshold voltage and other hot-electron phenomena in low dimensional bulk type MOSFET's [1.78] describing the Threshold Voltage Roll-Off (TVRO) phenomenon. This model has not included a priori charge partitioning or constant surface potential making it suitable for application in circuit simulation. The threshold voltage shift was found to be identical to that of its bulk MOSFET equivalent. With the effective channel length being fixed, threshold voltage roll-off in FDSOI was evidently reduced than bulk MOSFET.

An year later, in 1996, Yuhua Cheng et. al. developed an improved physical I-V model for a fully depleted SOI MOSFET with channel length in deep sub-micrometer range [1.79]. This model used a single expression and has successfully demonstrated a continuous and smooth transition of I-V and C-V characteristics from the sub-threshold to near-threshold and above-threshold regimes of operation. The said model also included various important short channel effects. Accuracy of this model is greatly improved by including various important short channel effects such as velocity saturation, Drain Induced Barrier Lowering (DIBL), Drain Induced Conductivity Enhancement (DICE), Channel Length Modulation (CLM), gate bias dependent mobility and floating body effect. Later in the same year, the same research group presented another I-V model of SOI MOSFET

incorporating self heating effect which is an important issue with the SOI MOSFET in deep sub-micrometer range [1.80].

Later, in 1997, following the studies of Shur et. al., Long et. al. [1.81] came up with a new device structure termed Dual Material Gate Field Effect Transistor (DMGFET) where the gate was constituted of two separate materials having different work functions amalgamated side by side touching each other. In this newly proposed structure, the threshold voltage near drain end was found to be more negative than that in the source end ensuring a shielding effect which effectively reduces the SCEs. The presence of two different materials in the gate electrode results in a discontinuous channel electric field distribution, which subsequently increases carrier transport along with simultaneous suppression of the SCEs.

In 1998, a fully continuous compact model was developed by Jeffrey W. Sleight et. al. for circuit simulations considering the correct body depletion condition [1.82]. The uniqueness of this model lies in the fact that it provides the flexibility of transition between fully-depleted (FD) or partially-depleted (PD) behavior during device operation unlike the previous models which considered either FD or PD operation but not both.

In 2000, J. B. Roldán et. al. developed an analytical current-voltage model for ultra-short channel SOI MOSFET intended for circuit simulation. This model includes the velocity overshoot, series resistance and self-heating effects [1.83]. Again in the same year, Zhou et. al. [1.84] suggested a novel structure called Hetero-Material Gate (HMG) MOSFET which can be easily fabricated by introducing one additional mask in the bulk CMOS technology.

In 2001, M. Youssef Hammad et. al. proposed yet another analytical model for the partially-depleted (PD) Silicon-on-Insulator (SOI) MOSFET above threshold incorporating front-back interface coupling with all the possibilities of accumulated, neutral, and depleted back interface [1.85]. This model was extremely physical and highly predictive, and hence has been applied to both tied-body and floating-body devices. Later in that year, Keunwoo Kim and Jerry G. Fossum [1.86] presented an asymmetrical double-gate (*DG*) *CMOS* utilizing n+ and p+ polysilicon gates. The study established that the structure can be superior to symmetrical-gate counterparts. The most significant result obtained was an asymmetrical *Double Gate MOSFET*, optimally designed and having only one dominant channel, are capable to yield comparable and even enhanced device currents at low supply voltages.

T. Ernst et. al., in 2002, suggested an original compact model for lateral field penetration in the buried oxide layer and underlying substrate of fully depleted SOI MOSFET [1.87].

In 2003, Kunihiro Suzuki et. al have proposed a new model for threshold voltage formulation for fully depleted single-gate SOI MOSFETs taking into account the effects of two-dimensional charge sharing in both SOI and buried-oxide layers [1.88]. This model shows the dependence of

short-channel effects on the device parameters like channel-doping concentration, gate oxide and buried-oxide thickness.

The next year saw the development of another new model for Silicon-on-Nothing (SON) transistors with thin fully depleted Si film and ultrathin buried oxide established by Jérémy Pretet and Stephane Monfray et. al.. The proposed model incorporated several intrinsic mechanisms in the SON MOSFET operation such as substrate depletion by source and drain via doping modulation, significantly reduced coupling between the front and back gates and role of ultrathin buried oxide [1.89].

Guruprasad Katti et. al. have presented a three-dimensional Poisson's equation solution based analytical threshold voltage model for a mesa-isolated FD SOI MOSFET [1.90]. This model presents accurate analytical expressions for the threshold voltages of both front and the back gates enabling the model to predict short channel as well as narrow width effects.

Anurag Chaudhry et. al., in 2004, published a review article on the undesirable short-channel effects induced performance degradation of a SOI MOS device [1.91]. In another study, they have proposed a Dual-Material Gate (DMG) SOI MOSFET [1.92] and have presented the efficiency of their proposed device structure in suppressing various SCEs such as gate depletion, Drain-Induced Barrier Lowering (DIBL), Hot-Carrier Effects (HCEs) and Channel Length Modulation (CLM). Later in that year, Wei Ma and Savas Kaya [1.93] studied a Double Gate SOI MOSFET structure and investigated the impact of device physics on the structure to compare the performances of the said structure with that of bulk MOSFET considering drain-to-source current, device transconductance and output or drain conductance.

Next year, in 2005, G.V. Reddy and M.J. Kumar incorporated the merits of the DMG and DG structures developed earlier to present another novel structure called Dual Material Double Gate (DMDG) Fully Depleted SOI MOSFET [1.94] and it was clearly evident from the results that the newly proposed DMDG SOI MOSFET was superior to the earlier structures.

In 2005, Giorgio Mugnaini et. al. developed a physics-based analytical model in two parts for nano-scale MOSFET which covers the whole range of regimes from drift-diffusion to ballistic transport, considering quantum confinement effect in the silicon channel [1.95].

A contemporary work by Adelmo Ortiz-Conde et al. [1.96] presented an explicit expression of the surface potential of an undoped symmetric dual-gate device based on analytical formulations. The error involved in the solution compared to exact results is quite negligible for typical device dimensions and bias conditions.

In 2006, Norio Sadachika et. al. reported a HiSIM-SOI circuit simulation model based on a complete surface-potential description [1.97]. In that model, the channel surface potential is solved iteratively along with the front and back potentials at both surfaces of the buried oxide, including all relevant device features of the SOI MOSFET explicitly.

In 2008, Guohe Zhang et. al. proposed a novel approximation of vertical 2-D potential function in the FD SOI MOSFET channel with vertical Gaussian profile [1.98]. This approach enables one to calculate the threshold voltage for non-uniform FD-SOI devices.

Te-Kuang Chiang, in 2009, developed a model to study the sub-threshold behavior of short-channel tri-material gate-stack SOI MOSFET consisting of the two-dimensional potential, threshold voltage and sub-threshold current [1.99].

Next year, W. Wu et. al. developed a surface potential based model for partially depleted (PD) SOI MOSFET [1.100] following the outline of the latest industry standard bulk MOSFET model. This physics-based model also includes some special effects like floating body simulation capability, parasitic body currents and capacitances and nonlinear body resistance which are typically seen in SOI devices.

Taking another step ahead, Weimin Wu et. al., in 2010, presented a complete surface-potential-based compact analytical model of dynamically depleted SOI MOSFET [1.101]. The surface potential equation avoids the unphysical behaviors near the flat-band voltage. Therefore, the coupling equations for the front and back surface potentials have been modified to capture the dynamic depletion effect by incorporating the effect of back gate bias. A new method has been proposed based on symmetric linearization with an aim to obtain accurate explicit expressions for drain current and charges at the device terminals.

Apart from the above mentioned theoretical models, there are numerous other models which have made significant contribution to the development in the theoretical modeling of SOI MOSFETs. Few of them are listed below:

- Sub-threshold slope model by J. P. Colinge et. al. in 1986 [1.102]
- Self-heating effects by D. Yachou et. al. in 1993 [1.103]
- Quantum mechanical model by Y. Omura et al. in 1993 [1.104]
- Monte Carlo simulation model by F. Gámiz et. al. 1998 [1.105]
- Electron mobility model by F. Gámiz et al. in 1999 [1.106]
- Threshold voltage model with Gaussian profile by C. Ravariu et al. in 2000 [1.107]
- HiSIM SOI model by D. Kitamaru in 2003 [1.108]
- Compact charge and capacitance model by O. Moldovan et al in 2008 [1.109]

Although SOI features significant performance improvements over conventional MOSFETs, SOI is not fully immune to SCEs. Hence, some improvised SOI MOSFET structure like Silicon-On-Nothing (SON) MOSFET has received considerable attention in recent times [1.110-1.112]. Different technological solutions to fabricate SON MOSFETs have been invented in recent years like Silicon-On-Nothing process from ST-Microelectronics [1.113], Empty Space in Si (ESS) from Toshiba Electronics [2.78], Silicon-On-Void (SOV) created by Chinese Institute of Microelectronics [1.114]. A

new and more efficient SON structure has proposed and developed by V. Kilchytska et.al.[1.115], by Silicon layer transfer over a pre-etched cavity through wafer bonding technique.

Jurczak et. al. [1.116] suggested a new architecture called Silicon-on-Nothing which is competent enough to reduce SCEs by fabricating extremely thin layers of oxides and silicon films. SON devices exhibit excellent threshold voltage roll-off and I_{on}/I_{off} trade-off .They are also immune to the drawbacks like self-heating, high S/D series resistance etc. found in conventional SOI devices. By dint of the above mentioned advantages, SON is gradually becoming the fundamental technology for the next generation ULSI era.

Although there are considerable numbers of experimental reports available in literature but there is lack of theoretical investigations related to the modeling of SON MOSFET. First time in 2004, Jérémy Pretet, et. al. developed a compact capacitive model to formulate the threshold voltage of SON which has SOI like architecture [1.117]. This model incorporates different short-channel effects like charge sharing, DIBL and fringing field model and investigates threshold voltage and sub-threshold swing behavior of SOI and SON MOSFET.

In 2008 B. Svilic˘ic et. al. have presented another threshold voltage model for a novel vertical fully-depleted Silicon-on-Nothing MOSFET based on compact capacitance equivalent circuit [1.118]. The channel region is considered to be coupled to the source and drain through the buried oxide by the obvious fringing fields which have been considered in their model.

The discussions presented so far consider junction based devices which operate basically in the inversion mode. Despite of a host of advantages, the most significant deterring factor of any junction based device is the formation of ultra-sharp source-channel and drain-channel junctions when the device dimension reduces to nanoscale. This shortcoming can be alleviated by new device "Junctionless" transistors proposed by Colinge et. al. in 2010 [1.119]. Because of this junctionless architecture, the type and concentration of channel doping are identical to that of the source and drain extensions, thus eliminating the creation of doping concentration gradient. This prevents the possibility of impurity diffusion during thermal processing steps, thereby sufficiently relaxing the thermal budget.

Exploring the popular idea of multiple metal gate electrode, Deb et. al. developed a novel concept of considering a binary metal alloy ($A_\alpha B_{1-\alpha}$) gate electrode having continuously varying mole fraction from source side (100% A) to drain side (100% B) in a FD SOI MOSFET [1.120].

The concept of binary metal alloy as gate electrode was first coined by Tsui et. al. in 2003 [1.121]. To characterize the binary alloy systems, (100)-oriented phosphorus doped Si wafer was chosen as starting material to fabricate MOS structure. Standard RCA process was adopted to clean the wafer where a 2-nm thick gate oxide was subsequently grown thermally. Patterning of the gate electrodes was done using the liftoff process. Ta Pt alloys were co-sputtered simultaneously upto a thickness of 10 nm on patterned photoresist. The deposition conditions and the atomic composition

were monitored using Rutherford Backscattering Spectroscopy (RBS). After patterning, the samples had to be annealed in nitrogen ambient at temperatures of 400, 500, and 600 degree Celsius for about 30 min, after which aluminium was deposited at the back. Subsequently, the approximate work-function of the annealed samples was found out by performing a comparative analysis of the measured C-V characteristics curve with theoretical C-V curve. The true essence of this concept lies in the fact that the effective work function of the alloy can be precisely adjusted by cleverly modulating the atomic composition of the alloy. Normally, the work function requirement of a fully-depleted SOI is approximately around 4.6 eV which can be easily achieved by using the Ta/Pt alloy ratio close to 0.74/0.26.

A more recent study by A. Pan et. al. in 2010 combines spatial source reagent gradient with a temperature gradient in order to realize continuous mole fraction variation of a ZnCdSSe alloy nanowire on a single substrate, thereby establishing the fabrication feasibility of such alloy system [1.122-1.123]. Earlier study by Christen et. al. in 2003 proposed a suitable method for continuous compositional spread (CCS) thin film based on pulsed laser deposition (PLD) [1.124-1.125]. In their work, a CCS–PLD apparatus was developed and implemented to fabricate as-grown epitaxial CCS thin film on substrates having long dimension. These studies establish that the compositions at each and every position of the CCS film are in good agreement with the analytical/designed values. Thus, the recent fabrication trend discussed so far indicates fabrication of binary metal alloy gate electrode ($A_{\alpha}B_{1-\alpha}$) with continuous lateral concentration variation from source (100% A) to drain side (100% B) is certainly feasible in near future. Motivated by the fabrication feasibility of such binary metal alloy gate electrode, Sarkar et. al. has incorporated this unique concept of using a binary metal alloy as gate electrode in several nanoscale device structures to investigate the advantages of using such spatial composition graded work function engineered gate electrode over conventional single metal gate electrode in terms of surface potential, electric field distributions, subthreshold slope, current driving capacity and output voltage gain [1.126-1.130].

In spite of several improvisations on the basic MOSFET suggested by ongoing research in the domain of semiconductor devices, one of the primary deterrent factors in the path of unhindered progress in MOS technology lies in the limitation of minimum achievable subthreshold slope of 60 mV/dec. As already stated, at room temperature MOSFET requires minimum gate voltage of 60 mV to increase the current by magnitude of one order [1.131] limiting the value of minimum attainable subthreshold slope to be 60 mV/dec. Tunneling Field Effect Transistors (TFETs) have the potential to replace MOSFETs for low power consuming low voltage applications by their intrinsic virtues of reliability, low leakage current in OFF state, ability to achieve subthreshold slope value below the limiting value of 60mV/dec and significantly reduced SCEs (due to built-in tunneling of electrons).

A Tunnel field effect transistor is basically a simple gated reverse biased p-i-n diode where the device source and drain regions are heavily doped with opposite impurities and the channel region is ideally intrinsic [1.132]. The device structure operates on the principle of band-to-band tunneling of carriers. In spite of having several aforementioned operational advantages, TFETs too have several limitations. The operating principle of TFETs indicates that the device current originates principally due to tunneling of carriers from the source side valence band to the channel conduction band which results in low OFF state current on one hand, whereas reducing the ON state current on the other hand [1.133] making sufficiently lower than the required ON current specified by ITRS. This necessitates the search for several improvisations on the basic TFET structure in order to deal with this limitation of ON current. Studies by different groups of researchers are available in contemporary literature on TFETs. Vanderberghe et. al proposed different modifications on gate positioning by placing the gate covering the area near source region only to mitigate point tunneling current [1.134]. A similar structure with gate only on the source region has also been studied [1.135] showing considerable improvements.

The concept of 'gate engineering' popular with MOSFETs may very well be applied in TFETs also with the purpose of reaping the benefits of enhanced device current and increased package density in multi gate device structures. Several researchers have endeavoured to incorporate gate engineering technique in TFETs to achieve higher ON current which forms the major bottleneck for simple conventional TFET structures. Several groups of researchers have presented various research attempts to institute a physics based analytical model of Double Gate TFETs with a view to obtain a clear insight to the internal physics associated with the device operations. A generic analytical model was developed by Verhulst et. al [1.136] to explore a comparative performance analysis among single gate, double gate and gate all around TFET structures with special emphasis on the dependence of tunneling current on various device parameters. Another research group (Vandenberghe et. al. [1.137]) attempted to present an analytical model of a novel Double Gate TFET where the gate electrode covers the source region only. Again, in another approach, a new model for TFET has been presented by Shen et. al. [1.138] implementing the idea of non-linear Poisson's Equation (normally used for MOSFETs) in TFETs.

Just like gate engineering, the much discussed concept of '**gate material engineering**' may also be incorporated into the basic TFET structure with an intention to increase the normally low ON current in simple TFETs by lowering the barrier at the junction between the source and channel regions, whereas the drain-channel barrier is maintained to be high in order to suppress the OFF-current by properly choosing the workfunctions of the gate metals. M. J. Kumar et. al. [1.139] reported a Dual Material Gate (DMG) TFET where two metals having different work functions are amalgamated adjacently forming the single gate electrode. The variation in gate metal work

function modulates and effectively enhances the electric field in the channel near the source to channel junction so that an increased number of carriers effectively tunnel from the source side into the channel and reaches the drain end, resulting in a sharp rise in ON current. Furthermore, the dual concepts of 'multi gate' TFETs and 'gate material engineered' TFETs can be compounded together to explore improved device functionalities in some improvised TFET structures like Dual Material Double Gate TFETs (proposed by Balamurugan et. al. [1.140]) and Dual Material Gate all around TFETs (proposed by M.J.Kumar et.al [1.141]). Placing three metals adjacently will result in a Triple Material Gate TFET structure (recently proposed by Bagga et. al. [1.142])

Taking one step further, the perception of gate material engineering can be explored to an extreme level by using a 'binary metal alloy gate' in TFETs also where the mole fractions of the individual metals of that alloy is continuously varied from source side (100% A) to drain side (100% B). Motivated by the fabrication viability of such binary metal alloy gate electrode as already discussed in sufficient details, some research endeavors are currently available in literature which attempt to incorporate this unique concept of 'work function engineered' gate electrode into the basic TFET structure [1.143-1.144] with an aim to realize some improvised TFET structures which can alleviate the short comings of a simple TFET.

1.3 Organization of the thesis

The thesis has been organized as different chapters focusing on different non conventional nano device structures for improved performance along with a concise introduction of nano devices and relevant literature survey and ends with a concluding chapter. Continuous progress in the VLSI industry is dominated mainly by the design and implementation of low power nanoscale devices to meet the growing demands of human beings which can be accomplished by down scaling the dimensions of each constituent transistor. This trend of aggressive down scaling of conventional field-effect transistors is limited by the quantum mechanical laws, the limitations of available fabrication facilities and fabrication costs and results in inevitable performance degradation due to several detrimental short channel effects which mandates the quest for alternative non conventional devices beyond CMOS. The dictum of this thesis is to present the analytical modeling based performance study of several such non conventional ultra low dimensional device structures to provide a solution for future nanodevices.

- **Chapter 2** presents an in depth overview on the basic concepts of nano dimensional devices starting from the journey of conventional long channel MOSFETs to present short channel MOSFETs, the problems associated with device dimension miniaturization and the possible non conventional devices to alleviate the inadequacy of short channel devices.

- **Chapter 3** presents a detailed analytical two dimensional Poisson's equation based surface potential and device current behavior of a Dual Material Gate SOI/SON MOSFET with strained channel. Two gate metals M_A and M_B of different work functions φ_A and φ_B are placed together adjacently as a single gate electrode which increases trans-conductance and mitigates the SCEs due to the formation of a step like feature in the surface potential profile which practically screens the potential in the channel region under the gate material on the source side (M_A) from any random variations in the drain bias, giving effective protection from DIBL. Initially, the variation of carrier mobility in the strain incorporated silicon channel has been studied in details against mole fraction variation, impurity concentration and transverse electric field. Then a Poisson's equation based two dimensional analytical model for threshold voltage has been evaluated from the surface potential minimum and various drain characteristics are studied.

- **Chapter 4** exhibits an overview of some better MOSFETs based on improved gate structure by incorporating the dual concepts of 'gate engineering' by adopting multiple gate MOSFETs (Double Gate, Cylindrical Gate and Quadruple Gate) and 'gate material engineering' by using a binary metal alloy gate electrode with linearly graded mole fraction and comprises of three sections. The first section investigates the attributes of an asymmetric Double Gate MOSFET incorporating the novel theory of 'work function engineered gate' by continuously varying the mole fraction in a binary metal alloy gate from source side to drain side in a fully depleted Double Gate MOSFET. The second section presents the performance analysis of a Cylindrical Gate MOSFET incorporating the 'work function engineered gate' concept and finally the last section explores the performance analysis of a Quadruple Gate MOSFET with Work Function Engineered Gate electrode.

- **Chapter 5** focuses on the novel idea of nanoscale work function engineered gate Junctionless devices as better alternative to conventional MOSFETs. The first section of this chapter will investigate the analytical modelling based relative performance investigation of a Junctionless Work Function Engineered Gate Double Gate (JL WFEG DG) MOS structure with respect to simple JL DG MOS. The next section presents similar analytical modelling based performance study of Junctionless Work Function Engineered Gate Cylindrical Gate (JL WFEG CG) MOS structure compared to its simple JL CG MOS equivalent. Both the studies exhibit superior performance of the WFEG JL structures compared to their simple JL counterparts in terms of Threshold Voltage Roll-Off (TVRO), Drain Induced Barrier Lowering (DIBL) and voltage gain.

- **Chapter 6** aims to investigate improvised 'gate material engineered' Tunnel Field Effect Transistors (TFETs) as possible alternatives to MOSFETs for future low power, low voltage

applications. The first section of this chapter investigates the analytical modelling based comparative performance investigation of a Work Function Engineered Gate Double Gate (WFEG DG) TFET structure compared to normal DG TFET. The next section presents similar analytical modelling based performance analysis of a Binary Metal Alloy Silicon-on-Nothing (BMA SON) TFET compared to its simple SON TFET equivalent highlighting the effects of interface trapped charges near the source region on the performance of the device under consideration. Both the studies will exhibit superior performance of the work function engineered/binary metal alloy gate structures compared to their normal single material gate counterparts.

- The outcomes of all the presented works and the conclusion are summarized in **Chapter 7**.

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Chapter 2

An overview on Nano devices

CHAPTER II

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2.1. Introduction

The continuous progress in the microelectronics industry is dominated mainly by the design and implementation of low power nanoscale devices to meet the tremendously escalating technology needs of this tech savvy generation. Significant performance improvement of contemporary ULSI circuits can be realized with simultaneous increase in operating speed and decrease in device power consumption in addition to proportional device dimension down scaling in accordance to Moore's scaling principle [2.1]. Aggressive reduction in the size of conventional field-effect transistors is expected to be limited by the quantum mechanical laws, the limitations of fabrication techniques and associated excessive costs [2.2]. Moreover, such small scale devices integrated on a single chip may

not be able to function properly to realize the operation of the circuit comprised by them. Continuing with this frantic pace of device miniaturization without sacrificing any functional competence can only be achieved by combining different non-conventional approaches of device down sizing, innovating alternative device structures with simultaneously improvising material properties. However, device performance in sub-micron regime is severely affected by reliability issues, direct tunnelling, gate depletion, boron penetration and most importantly the inevitable short-channel effects (SCEs) which can be briefly categorized as Threshold Voltage Roll off (TVRO), Drain-Induced Barrier Lowering (DIBL), Hot Carrier Effect (HCE), unwanted conduction in sub threshold region, leakage currents associated with several parasitic junctions etc [2.2]. Continuing with Moore's scaling trend is being possible primarily due to persistent research endeavour in pursuit of non-conventional devices capable of replacing the conventional ones without any loss in performance.

These alternative devices are either based on the quantum mechanical phenomena that crops up in the nanometer regime or incorporate some structural or material modifications [2.3]. The non-conventional devices based on the principle of different quantum mechanical phenomena are referred to as **revolutionary nano electronic devices** (quantum well, quantum wire and quantum dot based devices, e.g., RTD, HEMT, Spintronics, SET etc.). In parallel, the continuous structural improvisations in existing semiconductor technology realize modified devices termed as **evolutionary nano electronic devices** (Carbon Nanotube FETs, Graphene Nanoribbon FETs, Nanowire Field-Effect Transistors (NWFETs), III-V channel replacement devices, Ge channel replacement devices, Unconventional Geometries for FET devices etc.). The structures, operating principles and modelling techniques of such devices are drastically different from conventional bulk mode devices. The advantages of these non-conventional devices over bulk devices, options of further scaling and parameter optimization are some primary issues which have been focussed in the present thesis work.

2.2. Nano Devices

The Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have been the most promising semiconductor device since 1970s by virtue of their simple structure, low power consumption, low cost of fabrication, inherent property of high input impedance, superior noise immunity etc. Combined with these basic advantages, the superior scalability of MOSFETs leads to the extreme device dimension down scaling as predicted by Moore's law, which in turn increases the transistor count per chip almost exponentially resulting in the evolution of semiconductor industry from sub-micron to today's sub-nano regime. MOSFETs are the basic building blocks of both digital and analog integrated circuits. Device operations in such sub 100 nm regime again gives rise to various unwanted short channel effects which play an important role in deteriorating performance of such

nano dimensional devices motivating the researchers to explore new innovative non-conventional device structures defining the future of nano devices. This chapter aims to present an in depth insight on the journey of semiconductors from bulk MOSFETs to ultra scaled non conventional nano devices.

2.2.1. Metal Oxide Semiconductor Field Effect Transistor (MOSFET): an overview

The Metal Oxide Semiconductor Field Effect Transistor was initially proposed by Julius Edgar Lilienfeld in 1925 and performs the basic transistor functions of signal amplification and switching of electronic signals. The name MOSFET gives the clue to its construction indicating that the working principle of the device is based on the MOS capacitor structure arising due to a dielectric silicon dioxide oxide (SiO_2) layer sandwiched between the metal gate electrode and the underlying bulk silicon substrate. Fig. 2.1 below describes a basic MOSFET structure.

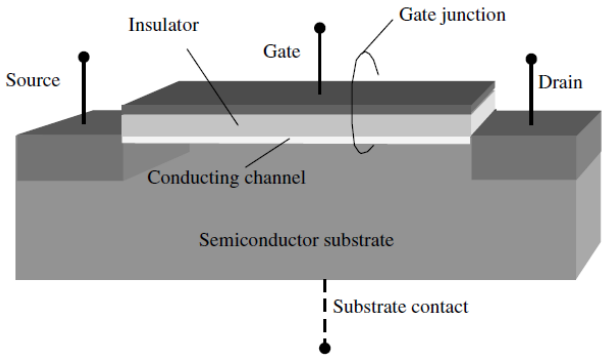

Fig. 2.1. A basic MOSFET

It can be seen from the figure above that MOSFET is a four terminal device with the source (S), drain (D), gate (G) and substrate (SS) terminals. A conducting channel connects the two heavily doped source and the drain regions through which charge carriers actually flow from the source towards the drain region depending on suitable drain bias applied. This conducting channel is actually a layer of inversion charge formed at the interface region of oxide-semiconductor having opposite nature than that of the fundamental silicon substrate. MOSFET can be categorized as n-channel and p-channel variants based on the type of impurities used to dope the source and the drain regions which determine the type of the produced channel. Considering a MOSFET with p-type substrate, if the source and drain regions are doped with n^+ impurities, the induced channel is n-type in nature having electrons as the majority carriers and the resulting MOSFET is called an n-channel MOSFET. Similarly, in a MOSFET with n-type substrate and with p^+ source and drain regions, a p-type channel is formed and the MOSFET is said to be a p-channel MOSFET where holes are the majority carriers. The figure below shows the basic structure of an n-channel MOSFET.

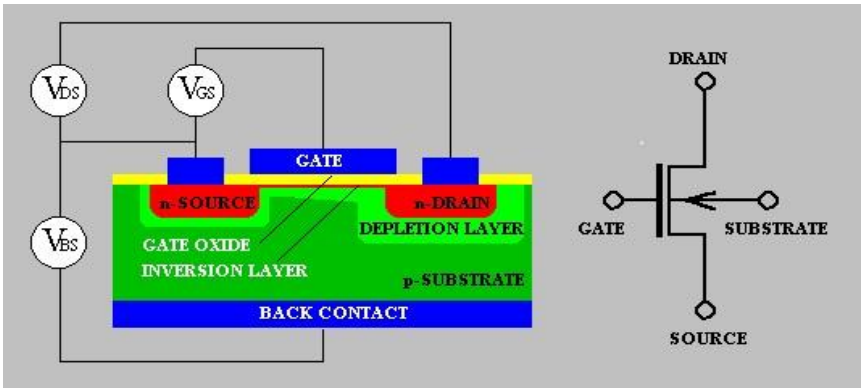

Fig.2.2: Basic n-channel MOSFET Structure and Symbol

For n-channel MOSFET, as mentioned above, the source and the drain regions are two heavily doped n+ regions diffused into the p-type substrate. A layer of silicon-di-oxide is grown on the surface of the semiconductor substrate between the two heavily doped regions of source and drain and the metal (or polysilicon) layer is subsequently deposited over this gate dielectric creating the MOS structure. The dielectric layer existing between the metal gate and the silicon serves the purpose of dielectrically insulating the gate from the main device which prevents the flow of any charge/current from the gate into the device itself, thereby ensuring the high input impedance (in Mega ohms or almost infinite) in MOSFETs. The device is completely symmetrical with respect to the drain and source terminals; the different roles of these two terminals are identified only in conjunction with the direction of device current flowing through the channel depending on the voltages applied to the these two terminals. The dimension of the region of semiconductor existing between heavily doped source and drain regions represents *channel length L.* Similarly, lateral extention of channel (perpendicular to the direction of channel) represents *channel width W.*

A conducting channel connecting the source with the drain regions will be formed by applying suitable voltage on the gate terminal. MOSFETs have the inherent advantage of very high input impedance (in orders of Mega-ohms) attributed by the presence of gate oxide dielectric which ensures a near ideal isolation of the substrate from the gate electrode. This induces a capacitive action by shielding the conducting channel from the controlling gate terminal, thereby blocking any current from flowing into the gate making MOSFET a simple voltage controlled resistor identical to JFET [2.4]. Very high input impedance in MOSFETs poses a limitation of unwanted accumulation of reasonable amount of static charges which may damage the MOSFET unless it is protected or handled cautiously. The limitation of another kind of FET (i.e. JFET) is that the gate biasing has to be properly chosen so as not to forward bias the gate-channel junction in order to ensure the basic JFET operation. However, in MOSFET, there is no such limitation and bias voltage of either polarity

(positive or negative) can be applied [2.5]. This makes MOSFET a viable alternative for being used as digital switches or logic gates.

2.2.1.1 Types of MOSFET:

Both the p-channel and the n-channel MOSFET can again be operated either in Depletion mode or in Enhancement mode depending on the process of channel formation [2.4, 2.6].

2.2.1.1.1. Depletion-mode MOSFET:

The existence of a preformed channel connecting the source with the drain regions distinguishes the depletion mode MOSFETs from the widely used enhancement mode counterpart. The prior existence of this conducting channel makes the depletion mode MOSFET a normally switched "ON" device even without gate bias. A gate to source voltage (V_{gs}) must be applied to switch the device into "OFF" state. Considering an n-channel depletion mode MOSFET for example, application of a +ve gate voltage enhances the effective number of charge carriers in the channel, widening the channel and resulting in an enhanced current flow. On the contrary, on applying a –ve gate voltage, the channel gets more and more depleted of charge carriers resulting in an effective reduction in drain current. P-channel MOSFETs show the opposite behavior.

Basic construction of depletion-mode MOSFET bear close resemblance with that of JFETs as in both devices, the channel region extending between the source and drain terminals is pre-doped with charge carriers i.e. electrons or holes depending on the type (n-channel or p-channel respectively). This results in the existence of a low-resistance path between drain and source terminals facilitating current conduction subjected to application of proper drain bias even if no bias is applied to the gate terminal.

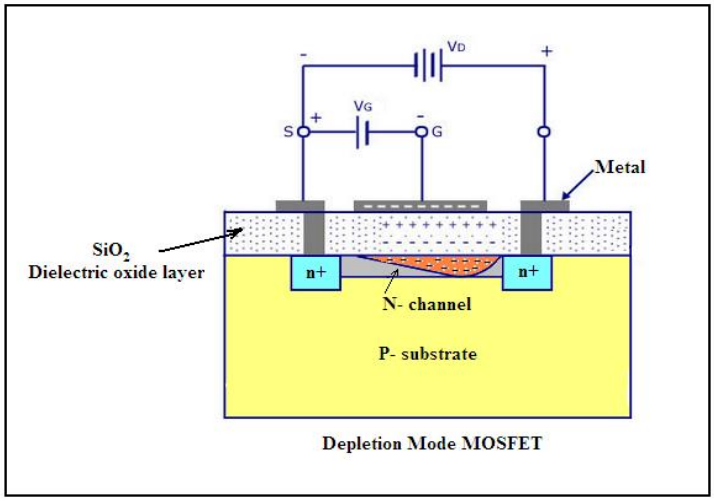

Fig. 2.3 An n-channel Depletion MOSFET

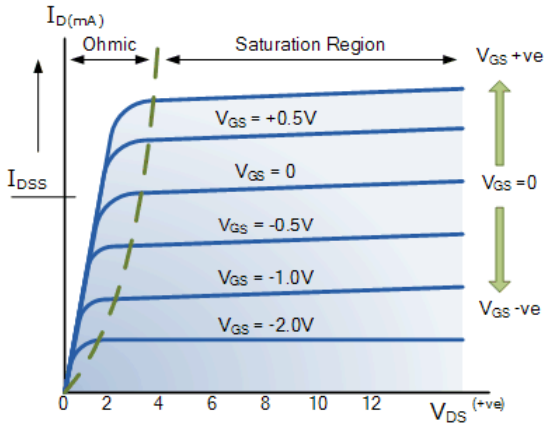

Fig 2.4 Current-voltage characteristics of Depletion-mode n-channel MOSFET

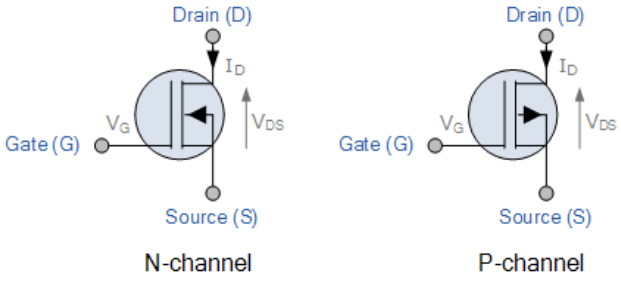

Fig. 2.5 Symbols of n-channel and p-channel Depletion-mode MOSFETs

2.2.1.1.2 Enhancement-mode MOSFET:

The operating principle of enhancement MOSFET is distinctly different from a depletion mode MOSFET by dint of the difference in their construction mechanism. The channel region of an enhancement MOSFET is normally undoped or very lightly doped making it non-conducting or 'Normally OFF' under zero gate bias condition. If the gate voltage is increased, i.e. making it more positive for an n-channel enhancement MOSFET, a vertical electric field is created directed from gate towards channel which pushes the holes within the p-type substrate near the oxide-semiconductor interface and attracts minority electrons from p-substrate towards the interface, thereby increasing the thickness and reducing the overall resistance of the channel allowing current to flow. Increasing the gate voltage above the threshold voltage results in 'channel inversion' creating a continuous electron rich n-type channel connecting the source with the drain region. Once the channel has been inverted, a positive drain bias pulls the electrons towards the drain side resulting in a continuous flow of electrons from source to drain side i.e. resulting device current is directed from drain to source. The gate voltage at which the channel is fully inverted is known as threshold voltage and the voltage range before the formation of inversion layer is called sub threshold voltage as elucidated in Fig. 2.6.

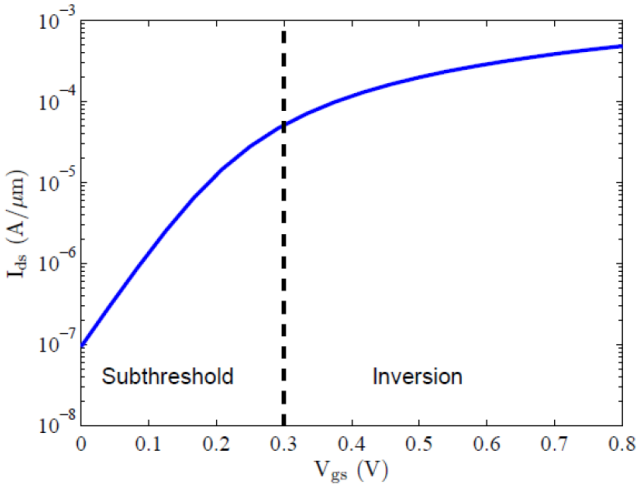

Fig. 2.6 nMOS I_D-V_{GS} characteristics illustrating subthreshold and inversion voltages

On gradually increasing this positive gate voltage, an effective increase is observed in the drain current. Thus, the name enhancement mode MOSFET is justified. If the positive gate voltage is increased further, the channel becomes less resistive allowing an effective boost in channel current. Thus, it can be deduced that for an n-channel enhancement MOSFET, application of positive gate bias operates the device in 'ON' state while application of zero or negative gate bias operates it in 'OFF' state making the enhancement-mode MOSFET a "normally open" or "normally OFF" switch.

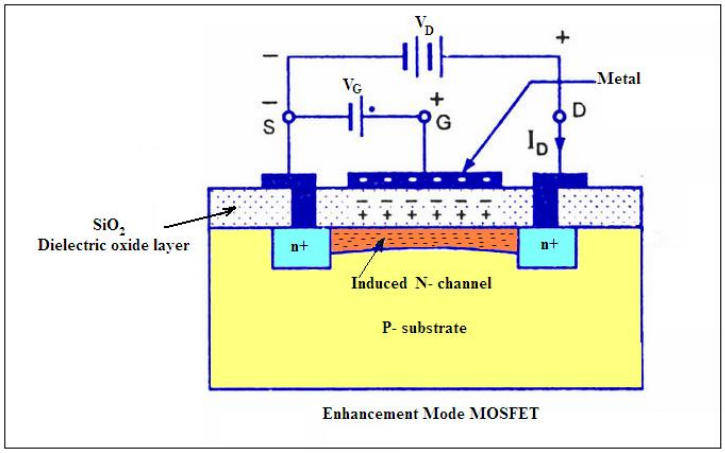

Fig. 2.7 A basic n-channel Enhancement-mode MOSFET

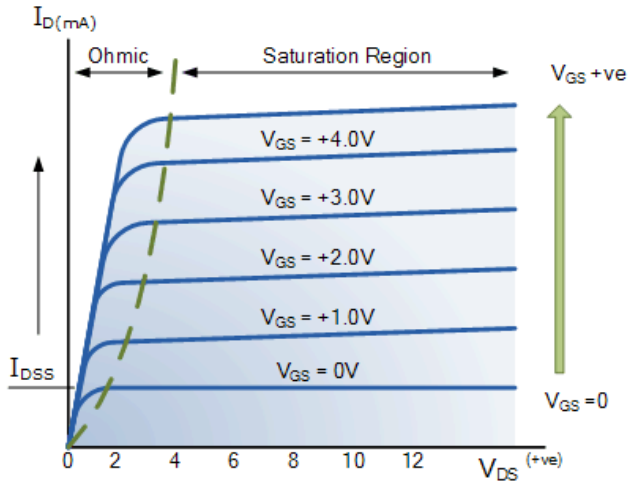

Fig 2.8 Current-voltage characteristics of an Enhancement-mode n-channel MOSFET

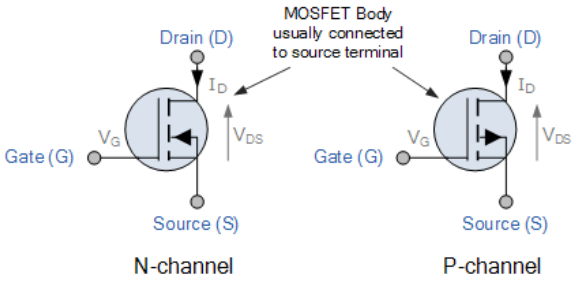

Fig. 2.9 Symbols of n-channel and p-channel Enhancement-mode MOSFETs

From the operating principle of enhancement MOSFET, it can be understood that it offers very low resistance in 'ON' state and extremely high resistance in 'OFF" state along with having an intrinsic

very high input impedance making it a suitable device for being used in integrated circuits as CMOS logic gates and in power switching circuits.

2.2.1.2 Regions of MOSFET operation:

MOSFETs can be operated in any of the three regions listed below depending on applied gate bias.

a. Cut-off Region

If the applied gate-to-source voltage is less than device threshold voltage, no current flows i.e. $I_{DS} = 0$ and the transistor is said to be "fully OFF" operating as an open circuit.

b. Linear or Ohmic Region

If the applied gate-to-source voltage exceeds device threshold voltage provided that the applied drain bias is more than the gate bias, the transistor will operate as a voltage controlled resistor and current through the transistor will increase linearly with an increase in drain bias. The value of this voltage controlled resistor depends on gate voltage (V_{GS}).

c. Saturation Region

Ultimately, if the applied drain bias exceeds the saturation voltage ($V_{DS,sat} = V_{GS} - V_{th}$) keeping the gate-to-source voltage well above threshold voltage, the drain current ceases to increase linearly and it saturates to an almost constant value. Now, the transistor is said to be 'fully ON'.

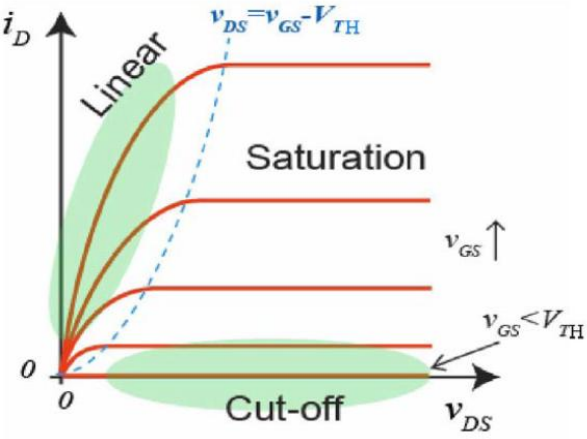

Fig. 2.10 Drain characteristics of MOSFET showing different regions of operation

2.2.1.3. MOSFET Models:

Initially, MOSFET modeling had the sole emphasis on a precise description of the device behavior. However, with the enlarging sphere of application, aggressive scaling and growing circuit complexity, there has been a distinct paradigm shift on emphasis. In this background, a number of approaches, each with an individual characteristic framework, have emerged both in public and proprietary domains [2.7]. Among the model categories of MOSFETs which are currently available in the public domain, and have undergone through a sustained phase of development are given as follows [2.7-2.10].

a. Threshold Voltage (V_T) Based Models

This piece-wise approach of MOSFET modeling is basically an overly simplified version of the benchmark Pao-Sah model [2.11]. The MOSFET behavior is described in both weak and strong inversion regions separately, demarcated by threshold voltage. The popular models like Berkeley's LEVEL 1, LEVEL 2, LEVEL 3, BSIM1, BSIM2, BSIM3, and BSIM42 models, along with the Philips–MM9 model fall under this category. Some of the major limiting issues faced by this approach are ever increasing number of model parameters and complex fitting parameter adjustments. However, this approach still remains a de facto industry standard [2.12-2.13].

b. Charge Based Models

This model involves complex formulation of drain current in terms of inversion charge density at the source and drain end of the channel [2.14]. These models are specifically applicable in low-power analog circuit designing. The mathematical formulation is purely based on device physics and requires less number of empirical fitting parameters and follows a relatively easier parameter extraction procedure. This approach involves EPFL, EKV, ACM and Berkeley's BSIM 5 MOSFET models [2.15].

c. Surface Potential Based Models

This approach is somewhat similar to charge based models excepting the fact that the drain current formulation in this case is dependent on the nature of source end drain end surface potentials instead of inversion charge density in the previous case. The difference in this case is that the drain current is formulated in terms of surface potential at the source and drain end of the channel. Adoption of some efficient analytical (PSP) or numerical (HiSIM) algorithms reduces the computational complexity associated with surface potential based modeling. In sharp contrast with the piece wise approach, SP models consider drift-diffusion current transport, which provides a single-piece expression for the current, with continuity of its derivatives, over the entire operating

region. Surface potential models are entirely physics based making them apt for being used in RF simulations and show excellent response to scaling induced phenomena modeling. Philips MM11, HiSIM 5 and PSP are some of the popular surface potential based models [2.16-2.18].

2.2.1.4. An analytical approach towards MOSFET

The simple principle behind a functional MOSFET relies on the vertical electric field generated by applying proper bias on the contolling gate terminal which effectively controls the net flow of charge carriers through the channel from the source region towards the drain region. For current conduction in the device, a conducting channel must be formed beneath the gate between the source and drain regions of the structure. Since the source and drain regions are of a different doping type than the substrate, in order to form a conducting channel, the semiconductor layer must be biased to induce inversion. The gate-to-source voltage V_{GS} at which the semiconductor channel is inverted to support subsequent conduction is known as threshold voltage V_{T0}. If the applied gate bias is less than $V_{T0,}$ inversion is not attained and the absence of an inverted channel prevents any current from flowing between the source and drain regions unless the gate bias exceeds $V_{T0.}$ If the gate-to-source voltage is chosen to be more than device threshold voltage, the induced vertical field attracts a large number of minority carriers (electrons for n-channel MOS) which accumulate near the surface to form the inverted channel capable of supporting current conduction.

The threshold voltage mainly comprises of four physical components [2.19]:

i. The difference in work function between the gate and the channel (Φ_{GC})

ii. The component of applied gate required to alter the surface potential (Φ_F)

iii. The component of applied gate bias required to compensate the depletion region charge ($-Q_{B0}/C_{ox}$)

iv. The component of applied gate bias required to compensate the fixed charges trapped at the interface between the gate oxide and silicon ($-Q_{ox}/C_{ox}$)

The overall threshold voltage expression comprising of these factors can be given by:

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{2.1}$$

Where,

$\phi_{GC} = \phi_F(substrate) - \phi_M$ for metal gate

$\phi_{GC} = \phi_F(substrate) - \phi_F(gate)$ for polysilicon gate

Φ_F is the bulk Fermi potential and for a p-type substrate, it is given by:

$$\phi_F = \frac{kT}{q} \ln \frac{n_i}{N_A} .$$

The second term in the eq. 2.1 represents that component of the gate voltage essential to alter the surface potential by $-2\Phi_F$ and achieve channel inversion.

Now, at inversion, the density of charges present in the depletion region can be approximated as:

$$Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}\left|-2\phi_F\right|} \tag{2.2}$$

If the substrate is biased at a different voltage level than the source, which is at ground potential, the depletion region charge density will become a function of the source-to-substrate bias and can be given as:

$$Q_B = -\sqrt{2qN_A\varepsilon_{Si}\left|-2\phi_F + V_{SB}\right|} \tag{2.3}$$

The gate voltage component that compensate this depletion region charge is given as $-Q_B/C_{ox.}$

The lattice impurities or lattice matching imperfections at the oxide-silicon interface results in the existence of some fixed positive charge density Q_{ox} at the interface region. The component of applied gate bias required to counterbalance this positive trapped charge is given as $-Q_{ox}/C_{ox.}$

The one dimensional Gradual Channel Approximation (GCA) approach is normally adopted to evaluate the expression for drain-to-source current in a conventional long-channel MOSFET. This approach assumes the vertical or gate electric field along the channel to dominate (neglecting the horizontal electric field), thereby simplifying the complex mechanism of current conduction in the channel into a one dimensional scenario. Using the GCA approach, the final expression of the drain current can be obtained as:

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left[2\left(V_{GS} - V_{T0}\right)V_{DS} - V_{DS}^2\right] \quad \text{in linear region of operation.} \tag{2.4}$$

Beyond saturation, the drain current at a constant V_{GS} ceases to vary much with applied drain V_{DS}, and remains approximately constant around the peak value reached for $V_{DS}=V_{DSAT}$. This saturation drain current can thus be obtained by substituting $V_{DS} \geq V_{DSAT} = V_{GS} - V_{T0}$ and is given by:

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS} - V_{T0}\right)^2 \text{ in the saturation region of device operation.} \quad (2.5)$$

This makes the expression for saturation region drain current to be a function of gate-to-source voltage only.

The transconductance is a figure-of-merit signifying the rate of change of device drain current with proportionate variation in gate-source voltage at a fixed value of drain-source voltage [2.20-2.21];

$$g_m \triangleq \frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=Const.} \quad (2.6)$$

The transconductance in the linear region and saturation region is given by;

$$g_{m,lin} = \mu_n C_{gox} \frac{W}{L} V_{ds}$$

$$g_{m,sat} = \mu_n C_{gox} \frac{W}{L}(V_{gs} - V_T) \quad (2.7)$$

Similarly, the output conductance is also a figure-of-merit signifying the rate of change of device drain current with proportionate variation in drain-source voltage at a fixed value of applied gate-source voltage [2.20-2.21];

$$g_d \triangleq \frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{gs}=Const.} \quad (2.8)$$

The output conductance is given by;

$$g_{d,lin} = \mu_n C_{gox} \frac{W}{L}(V_{gs} - V_T - V_{ds}) \quad \& \quad g_{d,sat} = 0 \quad (2.9)$$

Advanced nanoscale MOS structures need more accurate model to describe device behaviour at such ultra low dimension [2.13-2.20].

2.2.1.5 Power consumption in MOSFETs

An operating MOSFET consumes two types of power: Active and static power consumptions.

(a) Static Power consumption: Static power consumption is due to the leakage current existing in the device which may have a number of parasitic components like: gate-drain leakage, gate-source leakage, drain-source leakage and drain to bulk leakage. The power dissipation is given by:

$$P_{static} = I_{leakage} V_{DD} = (I_{drain,leakage} + I_{gate,leakage}) V_{DD} \quad (2.10)$$

where $I_{leakage}$ is the overall leakage current in the device and V_{DD} is the supply voltage.

The primary source of such leakage currents is the tunnelling of carriers through the oxide. The gate oxide thickness and barrier height determines the intensity of the leakage current. Generally, conventional MOSFETs use silicon-di-oxide as the gate dielectric due its ease of fabrication by oxidation of the silicon substrate. However, keeping pace with the aggressive scaling trend demands the proportionate downsizing of the gate oxide thickness also which effectively triggers the tunnelling probability of carriers through the oxide leading to increased leakage current. In order to overcome this limitation, researchers are now looking for suitable alternative oxides with comparatively higher dielectric permittivity (high-k) so that a thicker layer of oxide can be used in order to achieve the same range gate oxide capacitance obtained using a thin gate oxide layer, thereby improving the overall device performance.

The leakage at the drain side has three basic components-

i. leakage due to direct transfer of the carrier from source to drain

ii. leakage from drain to bulk i.e. the gate induced drain leakage (GIDL)

iii. leakage between source and drain region in sub-threshold condition

Hence, $I_{drainleakage} = I_{direct-tunneling} + I_{GIDL} + I_{subthreshold}$ (2.11)

(b) **Active Power Dissipation:** This type of power dissipation is due to switching of the transistor. When the device switches to ON state on application of suitable gate bias, charges build up in the channel and transported into the source/drain contacts and also at the gate electrode. Now, when the device switches to OFF state by removing the power supply, then these accumulated charges must be evacuated from the device. But, this is irreversible process and hence power dissipation takes place.

The energy required for charging and discharging the device during a switching action is stored in the form of gate capacitance expressed as $C_g = \frac{dQ_g}{dV_g}$. This can be easily recognized to be a simple parallel plate capacitor in inversion condition. Therefore, $C_g = C_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}}$ where W and L stands for width and length of the device respectively while ε_{ox} and t_{ox} represent the relative permittivity and thickness of the oxide layer. Considering Cox to be constant, the switching energy is given by $E = C_{ox}V_{DD}^2$. If f is the switching frequency, then the active power dissipation is given by:

$$P_{active} = fC_{ox}V_{DD}^2 \tag{2.12}$$

2.2.1.6. Advantages and applications of MOSFET

MOSFETs by dint of their extremely low power dissipation and smaller area requirement in an IC (which immediately translate into higher packing density and lower cost per function) have become the sole choice as component of high performance high speed complex ICs. Years of research in the domain of semiconductor devices have presented several path breaking improvisations in terms of its fabrication aspects, which made its performance improve drastically. Low power consumption property has made MOSFETs ideal for use as electronic switches or common-source amplifiers. Secondly, a large number of MOSFETs can be integrated on a single chip as compared to BJTs. Nowadays, MOSFETs are being immensely used to make an almost ideal buffer amplifier as its input resistance is very high due to an insulated gate. MOSFET has excellent low noise properties and hence it is used near the front end of a system where the signal is very weak. However, one limitation faced by the MOS device is its slightly poor frequency response characteristic as compared to BJTs due to the presence of several parasitic capacitances.

2.2.1.7. Complementary Metal Oxide Semiconductor

Complementary metal oxide semiconductor field effect transistor utilizes the complementary mode operation of a p-channel and an n-channel MOSFET i.e. both the MOS transistors are never ON at the same time. Complementary nature of the MOSFET makes only OFF state leakage current loss effective for steady state. This unique feature of complementary technology results in low static power consumption and noise immunity making CMOS technology ideal for integrated circuits. The structural view of CMOS and connection for a CMOS inverter is shown in Fig. 2.11 and Fig. 2.12 respectively.

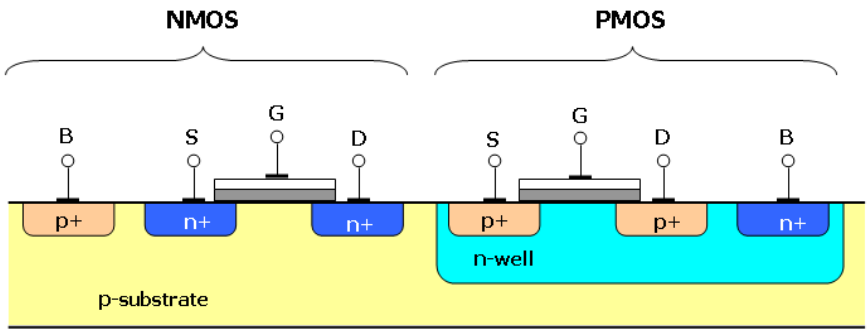

Fig. 2.11 Cross-sectional view of a CMOS

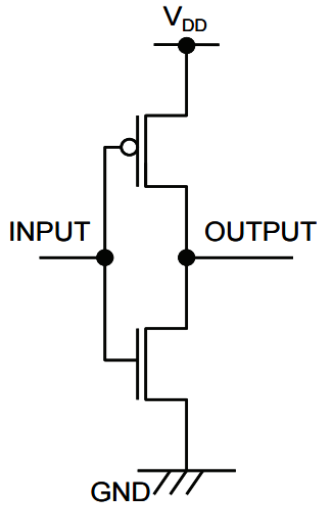

Fig. 2.12 A simple inverter implemented with CMOS logic

2.2.1.8 MOSFET scaling and its limitations:

With the advent of Integrated Circuits by Jack Kilbey at Bell labs, the explosive growth in modern digital electronics and computing has been credited by the adoption of integrated circuits as the fundamental building block. Functionality per chip has grown in accordance with Moore's law. Device miniaturization has been the main trick behind the unhindered technological advancement. The continuous improvisations in device miniaturization and concomitant increase in device density and circuit complexity on a single chip have realized the tremendous boost in the computing capability leading the consumers to expect ever better products at reduced cost.

The scaling rule of MOSFET was published by R. Dennard in 1974 [2.22] which states that all the dimensions of the device are scaled by a scaling parameter α , with multiplying factor of $1/\alpha$. The

doping concentration of the device is multiplied with α and the voltages of the device are also scaled by $1/\alpha$ so as to keep the internal electric field unchanged. Moreover, the circuit operating speed also boosts up by a factor of α with a simultaneous reduction in power dissipation by α^2. Fig. 2.13 illustrates the technology trend with the scaling. The threshold voltage reduction does not follow Dennard's rule because of the gate overdrive as shown in Fig. 2.13. The scaling law is shown in Fig. 2.14.

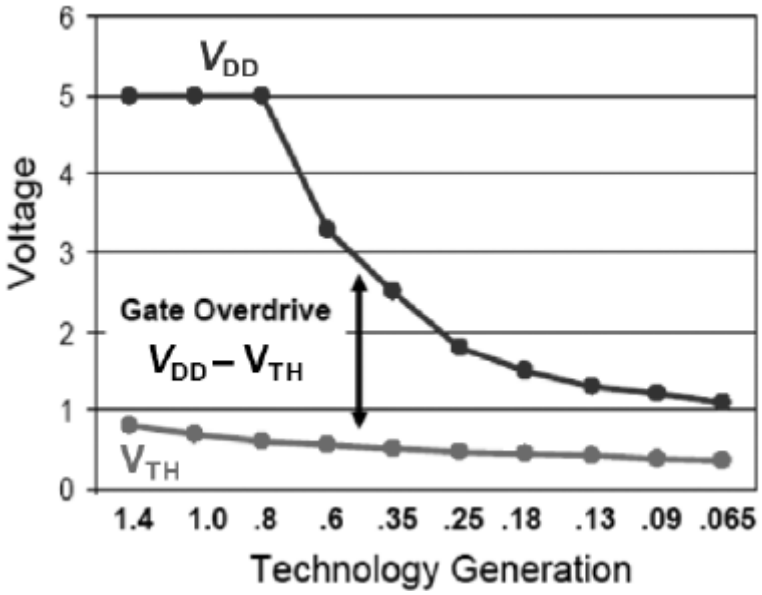

Fig. 2.13 Supply voltage scaling trend

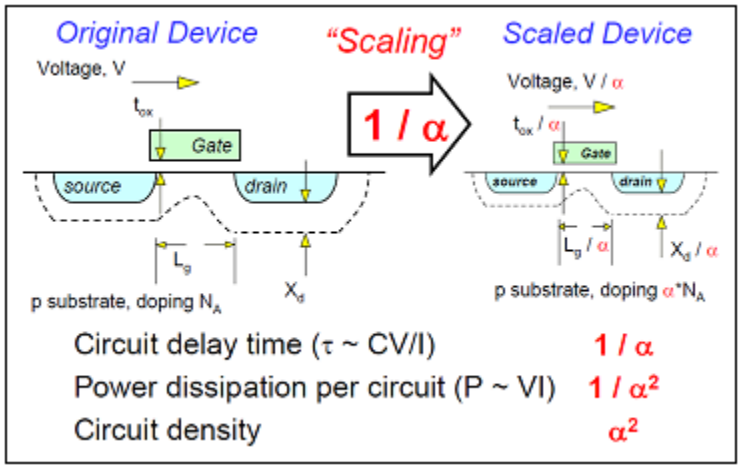

Fig 2.14 Principle scaling rule

With the continuous pace of scaling, the device feature size decreases each year and the number of transistors on a LSI chip doubles every two years as predicted by the industry benchmark Moore's law. Following this trend, the transition from micro-technology to nanotechnology and nano-electronics has already happened in 2002 which involves scaling down of transistor feature size from

micrometer to sub 100 nm orders. Preserving the transistor performance with scaling down was the key behind the unhindered successful progress of microelectronics technology. The trend of device dimension miniaturization for the future technology nodes is defined by the International Technology Roadmap for Semiconductor (ITRS) [2.1].

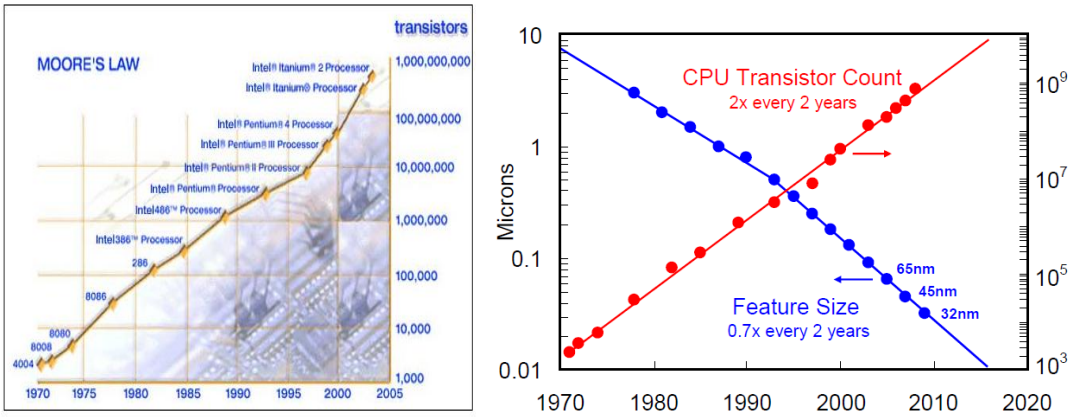

Fig 2.15 Moore's Law

Year	2003	2006	2009	2012	2015	2018
Technology node (nm)	100	70	50	35	25	18
MPU gate length (nm)	45	28	20	14	10	7
V_{dd} (V)	1.2	1.1	1.0	0.9	0.8	0.7
T_{ox} (Å)	13	10	8	7	6	5
Clock frequency (MHz)	2 976	6 783	12 369	20 065	33 403	53 207
Maximum power (W)	149	180	210	240	270	300
Static power (W/μm)	4.0×10^{-7}	6.1×10^{-7}	7.7×10^{-7}	9.9×10^{-7}	2.6×10^{-6}	3.9×10^{-6}
Nominal gate delay (ps)	30.24	18.92	12.06	7.47	4.45	2.81
Power delay product (J/μm)	1.4×10^{-15}	9.7×10^{-15}	7.7×10^{-16}	4.8×10^{-16}	3.0×10^{-16}	1.7×10^{-16}
Transistors per chip ($\times 10^6$)	153	307	614	1227	2454	4908

Table 2.1 ITRS 2003 roadmap for high-performance logic

Table 2.1 and Figure 2.15 show the scaling trend of MOSFET indicating that the MOSFET feature size is becoming smaller and smaller with the transition to each technology node as proposed by Moore, which radically increases the number of transistors packed together in a CPU and reduces the cost associated with each MOSFET by half every two years. However, the major hindrance related to this high integration density is enhanced power consumption. Researchers are continuously trying to adopt alternative methods to reduce the power consumption. But every method has its pros and cons. Dependence of dynamic power dissipation on the supply voltage makes reduction of supply voltage an obvious option to achieve lower power dissipation. Observing the scaling trend from 2005 to 2011 suggests that the bias voltage is varied slightly from 1.2 V to 1 V,

complying with the scaling rules. Therefore, threshold voltage too needs to be scaled down to a range of about 0.5V−0.6V for maintaining a high drive current and improving device performance. Till the end of the road-map, this voltage will not go below 0.45 V, due to the transistor control reasons. However, there is a trend towards substantially increased values of the leakage current and decreased current drivability which requires some kind of optimization.

Scaling limitations:

So far, the development of device scaling through various technology nodes and the associated advantages have been discussed. However, there is obviously some price to pay to reap these revolutionary benefits of realizing high speed and higher package density integrated circuits.
When the feature size is scaled down to nanometer regime, normal device operations are affected by some detrimental short channel effects (SCEs) which play a major role in negatively affecting the device performance. The reason behind the occurrence of various short channel effects on continuously reducing the device dimension is that on excessively reducing the channel length, charge sharing between the source and drain regions increase significantly making the gate electrode lose its sole control over the channel region [2.23-2.24]. As an effect of this reduced gate control, the threshold voltage and subthreshold slope become functions of channel length. Some of the salient short channel effects can be summarized as the Drain Induced Barrier Lowering (DIBL), Threshold Voltage Roll-Off (TVRO), random doping fluctuations and high field induced Hot Carrier Effects (HCEs). Contemporary research in the field of nano devices is mainly dominated by the urge to discover innovative strategies to prevent these short channel effects.

Apart from these physical limitations, the progress of scaling trend also faces some daunting practical challenges associated with the actual fabrication and manufacture of such miniaturized devices. These problems include lithography, gate oxide thickness reduction and formation of interconnects for each device. Any one or a combination of these effects poses to be a serious threat to the further progress of Moore's law.

In addition to the practical or physical challenges related to individual nano scale device, there are other alarming issues related to overall ICs. Formidable challenges are encountered in design, testing and packaging of integrated circuits containing billions of transistors. In spite of these difficulties in miniaturization, progress may still be kept unhindered by progressive refinements in IC technology (CMOS technology). However, before adopting such alternative technologies aggressively, it is worth to examine how much better computing hardware can be realized with it. It would be very unwise to pursue an expensive revolutionary technology aggressively if only marginal performance improvements can be attained.

Low dc power dissipation is the key feature behind the popularity of CMOS circuits in complex digital computation ICs making them a natural choice in portable applications where battery life is an important factor. Moreover, low power dissipation is very much desired in highly dense circuitry. Several transistors are conglomerated on a single chip to realize complex circuits. Under such circumstances, total IC power dissipation is very critical to maintain room-temperature operating condition. As temperature increases, silicon becomes intrinsic! Thus, instead of depending on the doping condition (as expected from extrinsic silicon), the free carrier concentration within the conduction band is hugely contributed by the inter-band thermal generation resulting in device failure. Even using extensive heat-sinking techniques, it is difficult to dissipate waste heat completely. Therefore, use of low power dissipation circuitry such as CMOS is essential for proper thermal management.

Thus, it can be summarized that aggressive device miniaturization involves several complications including material and processing problems or intrinsic device performance problems. With the shirking of device dimension, even the basic fabrication steps become difficult to be performed. As the device dimensions becomes smaller and the circuit gets denser and more complex, various problems are encountered in lithography, interconnects, and processing. Even different intrinsic device properties also get affected by device miniaturization. The different effects arising from device miniaturization alter device behavior and are cumulatively referred to as short-channel effects.

2.2.1.9. Different Short Channel Effects (SCEs) associated with device miniaturization:

A MOSFET is said to be a short channel MOSFET if the dimension of effective channel length L_{eff} approaches source and drain junction depths (x_j). As the channel length of a long channel conventional MOSFET device is being continuously scaled down it approaches to be short channel MOSFET and a number of undesirable effects crop up which negatively impact the performance of the short channel device. These undesirable effects are collectively known as 'short channel effects' (SCEs). Depending on their physical origin, different short channel effects can categorized as [2.27]:

1. **Two Dimensional electric-field profile:**

In a short channel MOSFET, the current flowing in the channel between the source and the drain gets controlled by both vertical and horizontal electric fields existing in the channel, which is in sharp contrast with the case of a long channel MOSFET where the dominant vertical electric field only controls the device current. This restricts the use of simple one-dimensional Gradual Channel Approximation (GCA) approach to account for some of the device characteristics observed in such a small-dimension. The physical significance of this two dimensional electric field are now being discussed vividly [2.28] as follows:

(a) Drain Induced Barrier Lowering and Threshold voltage roll off:

The Drain Induced Barrier Lowering (DIBL) effect occurring in short channel devices is manifested by threshold voltage roll off (i.e. a sharp decrease in the device threshold voltage as a function of drain voltage with a decrease in channel length) which can be considered as one of the primary short channel effects in nano dimensional MOSFETs. By definition, a MOSFET is said to be a short channel device only if the channel length approaches the order of dimension of the source and drain junction depths. With incessant reduction in channel length, the source and drain depletion regions approach each other making the source and drain regions very close to each other, thereby causing the horizontal electric field in the channel to increase which can no longer be ignored as it was being ignored using GCA approach. Under such circumstances, the total charge in the silicon channel is now being controlled by both the gate-to-source and drain-to-source voltages – a situation termed as '*two dimensional charge sharing*'. Constant reduction in channel length results in further increase of the horizontal channel electric field. Ultimately, the gate voltage loses its sole control over the total channel charge, which is now getting controlled by both gate and drain voltages for short channel devices. Naturally, a lower gate voltage is sufficient to attain threshold or 'channel inversion' condition in short channel devices indicating the fact that there is considerable reduction in the device threshold voltage with continuous channel length reduction.

The same phenomena of threshold voltage roll off may possibly also be understood from a different perspective of surface potential barrier in the channel between the source and drain. In long channel devices, a uniform potential barrier exists across the device and source/drain electric fields are only influential near the source and drain ends only due to wide enough separation between the source and drain regions. Under thermal equilibrium condition, carriers are not able to overcome this potential barrier and move from the source to drain region as there is no existing channel in enhancement type MOSFETs. In MOSFETs, conduction of current through the channel necessitates the creation and maintenance of the inversion layer near the oxide-semiconductor interface. If the applied gate bias voltage is less than the device threshold voltage ($V_{GS}<V_{T0}$), the surface is not inverted and the potential barrier effectively blocks the flow of carriers from source to the drain in absence of the inverted channel. Under this condition, only a small subthreshold current flows from the source to the drain regions. On increasing the gate voltage, this potential barrier gets reduced such that the carriers succeed in overcoming the obstructive barrier and successfully reach the channel region from source, driven by the electric field. The height of this potential barrier is expected to be controlled solely by the applied gate bias (in ideal condition) so as to increase device transconductance. However, this simple process of potential barrier getting controlled by the gate bias becomes complex in case of short channel MOSFETs where the channel potential barrier gets controlled by both gate and drain voltages. Under such circumstance, a gradual increment in the

drain-to-source voltage plays a crucial role in lowering the potential barrier even if the applied gate voltage is well below threshold voltage, thereby facilitating the carriers to overcome this reduced barrier and flow from the source towards the drain resulting in undesired current conduction in subthreshold state. This physical phenomenon of sub-threshold conduction due to drain bias induced barrier lowering is one of the major short channel effects termed as Drain Induced Barrier Lowering (DIBL) [2.29] and is explained in Fig. 2.16. It can be understood from the said figure that the height of potential barrier near the source end is reduced considerably on applying a high value of drain bias (the DIBL effect) enabling the injection of a large number of carriers into the channel which contributes to an enhanced drain current even in the OFF state.

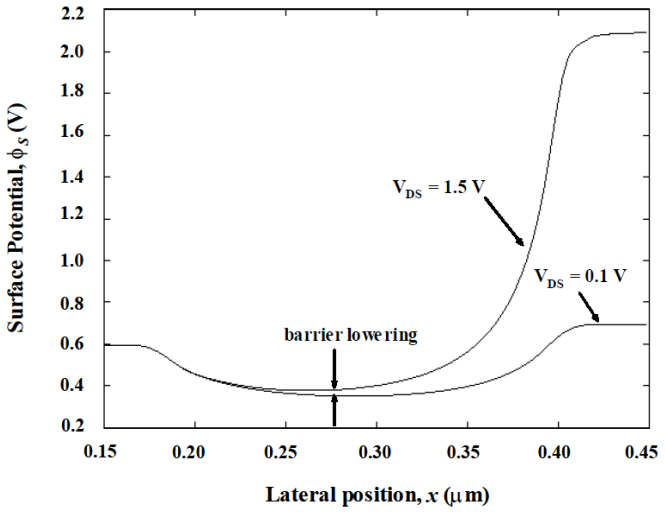

Fig.2.16 Variation of surface potential along channel position for V_{DS} = 0.1 V and 1.5 V

The DIBL effect gets manifested in the device threshold behavior. For a large value of applied drain bias, the depletion region from the drain region gradually encroaches into the channel leading to a considerable reduction in channel potential barrier. Hence, threshold condition i.e. subsequent current conduction can be attained for a lower gate voltage. The strength of DIBL is usually measured as the difference in threshold voltage V_{th} between a low (approximately 50-100mV) and a high (V_{DD}) drain bias. A large value of calculated DIBL represents a device having poor short-channel behavior with large threshold voltage roll off (TVRO) and high off current.

(b) Mobility reduction by gate-induced surface fields:

Keeping pace with the ongoing scaling trend necessitates size reduction of every device dimensions which includes not only the channel length, but also the thickness of gate oxide. As the gate thickness is scaled down proportionally, the vertical electric field directed from gate towards the silicon channel increases making the transverse electric field dominant. The carriers flowing in the channel from source to drain comes under the influence of this strong transverse electric field, suffer

collision and get accelerated towards the oxide-substrate interface. This high transverse field induced phenomena is known as surface scattering resulting in a measurable reduction in carrier mobility. Current conduction in MOSFETs is primarily dependent on the transport of carriers from source to drain through the narrow inverted channel region making it difficult for the carriers to flow parallel to the interface. On top of this, even a small increase in transverse electric field induces additional scattering as explained above, thereby reducing the average surface mobility to almost half of that of bulk mobility.

2. Electric-field strength in the channel becomes very high:

It is a well-known fact that electric field in the channel is inversely proportional to channel length with voltage being constant. As the channel dimension is continuously scaled down keeping the voltage sources to be constant, there is a notable increase in the channel electric field [2.30]. This uncontrolled increase in electric field results in some detrimental effects in short channel devices which may eventually lead to device breakdown.

(a) **Carrier velocity saturation:**

Current conduction in a MOSFET is due to the flow of carriers with a certain velocity through the inverted channel. The velocity of charge carriers is a strong function of channel electric field. At low value of channel electric field, the carrier velocity hold a linear dependence with the electric field which can be written as $v = \mu E$ where v and E represent carrier velocity and channel electric field respectively, while μ stands for the proportionality factor termed as carrier mobility. In short channel devices, the electric field within the channel increases considerably on gradually decreasing the channel length. At such high electric field, the linear relation between carrier velocity and electric field no longer exists due to optical phonon emission induced enhanced scattering rate of these highly energized carriers resulting in an effective rise in transit time required by these carriers to move through the channel. Drift velocities of both electron and hole saturate if the applied electric field is above100 kV/cm. In short-channel devices, the electric field near the drain attain excessive value (could be more than 400 kV/cm).

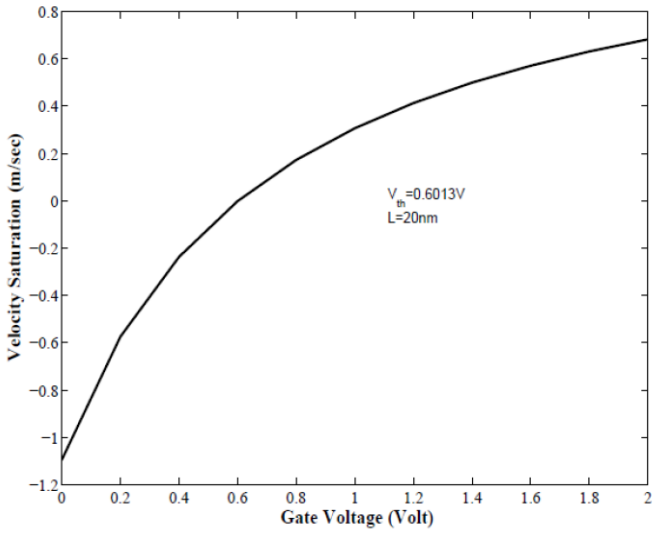

Fig. 2.17. Carrier velocity saturation with increase in gate voltage

(b) **Impact ionization near the drain:**

Application of sufficiently large drain-to-source voltage in a short channel MOSFET results in another adverse performance degrading SCE called the impact ionization near the drain. As the channel length gets scaled down, the electric field in the channel becomes considerably high near the drain end which can well surpass the minimum field required for the initiation of impact ionization. This occurs when a carrier moving through the channel from source to drain comes under the effect of high electric field at drain end and gains sufficient kinetic energy to hammer an electron from its bound state in valence band and provide it sufficient energy to move into a higher energy state in the conduction band, forming an electron-hole pair as illustrated pictorially in Fig. 2.18. The phenomenon thus explained is referred to as electric field induced impact ionization. As the mobility of electron is more than that of holes, the chances of electron induced impact ionization in nMOS is much more than hole induced impact ionization in pMOS for obvious reasons.

Considering the occurrence of electron induced impact ionization under a high channel electric field for an ultra scaled MOSFET, most of the electrons generated from the resulting electron-hole pair formation get accelerated towards the drain due to the high positive drain bias, while the holes reach the substrate to contribute to the parasitic substrate current. For an n-channel MOSFET, the channel region between the n type source and drain can act as the p type base of an n-p-n BJT with the source and drain acting as emitter and collector terminals of equivalent BJT respectively. Accumulation of holes (generated due to impact ionization) in the substrate region may create a voltage drop sufficient to forward bias the normally reverse biased substrate-source junction which in turn will result in injection of large number of electrons from the n-type source into the channel

eventually increasing the current. These newly injected electrons again come under the influence of high electric field existing in the channel and gain sufficient kinetic energy to initiate creation of more electron-hole pairs, thereby making this high field induced impact ionization a cumulative process altogether.

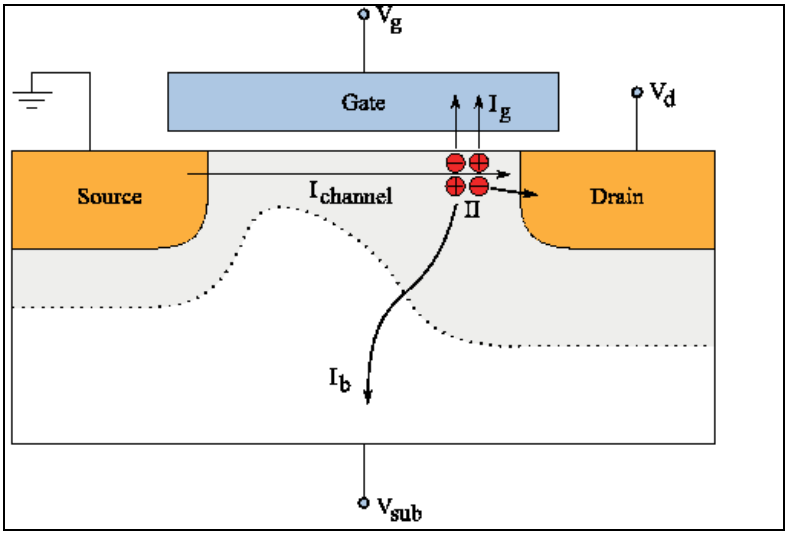

Fig.2.18 Hot carriers lead to impact ionization generating electron-hole pairs

(c) **Carrier heating or Hot Electron effect:**

Successive trend of device downsizing increases the horizontal electric field strength between source and drain which is sufficient to heat the carriers near the drain end to a very high kinetic energy resulting in another short channel effect which we normally call '***hot-electron effect***'. This term was first coined by Conwell [2.31] to explain the behavior of non-equilibrium electrons in semiconductor crystal. Under such scenario, the electron distribution can be represented using Fermi Dirac distribution function, but with a higher effective temperature. This effect can be neglected in metals as electron mobility in metals is not dependent on energies. However, for semiconductors, this 'hot-electron effect' is very much contextual due to the dependence of electron mobility on effective temperature. The term 'hot- electron' basically implies electrons having sufficient kinetic energy which enables them to even penetrate through the semiconductor material instead of their normal conduction through the channel generating device current. While penetrating with excessive kinetic energy, the electrons give away their excess energy in the form of phonons. Existence of high electric field near the drain end in short channel MOS enables 'hot' electrons to jump from the drain into the gate or substrate, thereby resulting in device heating and consequently an increase in device leakage currents.

(d) Parasitic Bipolar Effect:

This short channel effect comes hand in hand with the impact ionization effect explained earlier. Excess electron-hole pairs are generated due to high drain-to-source electric field induced impact ionization near the drain end. The holes thus generated get accumulated in the substrate region resulting in a net positive charge to build up in the p-type substrate with respect to the grounded source which serves the purpose of forward biasing the otherwise reverse biased source-substrate junction of an nMOS. This phenomenon is termed as '***Parasitic Bipolar Effect***' where the n-type source, p-type substrate and n-type drain constitute an n-p-n parasitic transistor. Forward biasing of the substrate-source junctions encourages injection of electrons from the n-type source into the p-type substrate underneath the inversion layer which in turn increases device current. These newly injected electrons comes under the influence of high electric field near the drain and participates in impact ionization resulting in avalanche multiplication of the number of electron hole pairs. The net positive feedback existing between the avalanche breakdown and the parasitic bipolar action results in breakdown at lower drain voltage threatening device reliability.

(e) Gate oxide charging:

Proportionate downscaling of gate oxide thickness in association with channel length minimization offers serious threat to oxide reliability resulting in breakdown of oxides. From the ongoing discussion, it can be well understood that continuous shrinkage in device dimension results in uncontrolled increase in both horizontal and vertical electric fields existing in the channel region which become sufficient to heat up the channel carriers to a high kinetic energy value enabling the so called 'hot' carriers to ascend into the gate oxide by surmounting the potential barrier existing at the interface between gate oxide and silicon channel. Buildup of these hot carriers in the gate oxide slowly degrades the quality of the oxide layer affecting the threshold voltage negatively which may eventually result in breakdown of oxide layer. This performance degrading effect in short channel devices is a kind of SCE named as ***time dependent destructive breakdown*** (TDDB) or ***hot electron aging***. This alarming issue threatening the reliability of oxide layer may be addressed by replacing conventional silicon-di-oxide (SiO_2) by some alternative high-k dielectric oxides like HfO_2, Al_2O_3, ZrO and TiO with higher relative permittivity as compared to SiO_2. Larger value of relative permittivity of such **high-k dielectric** oxide facilitate the realization of same gate capacitance using a much thicker oxide, thus mitigating the reliability and breakdown issues related to scaled gate oxide layer.

3. Physical separation between drain and source decreases:

As the channel length of low dimensional devices is scaled down, some of the major short channel effects resulting from the reduction of physical separation between the source and drain regions [2.32] can be summarized as follows:

(a) Channel Length Modulation:

The channel-length modulation (CLM) is a very common short channel effect affecting the drain or output characteristics of short channel devices. If the bias applied to the drain terminal of a short channel MOSFET is increased, the depletion region at the drain side widens and intrudes into the silicon channel resulting in considerable reduction of effective channel length which approximately becomes equal to the actual or metallurgical channel length minus the depletion region width at the source and drain junctions. This effective decrease in the channel in turn increases the current beyond saturation which can be clearly visualized from the existence of a finite non-zero slope in the drain characteristics of the device as shown in Fig. 2.19. The CLM effect is more prolific in small devices with low doped substrates.

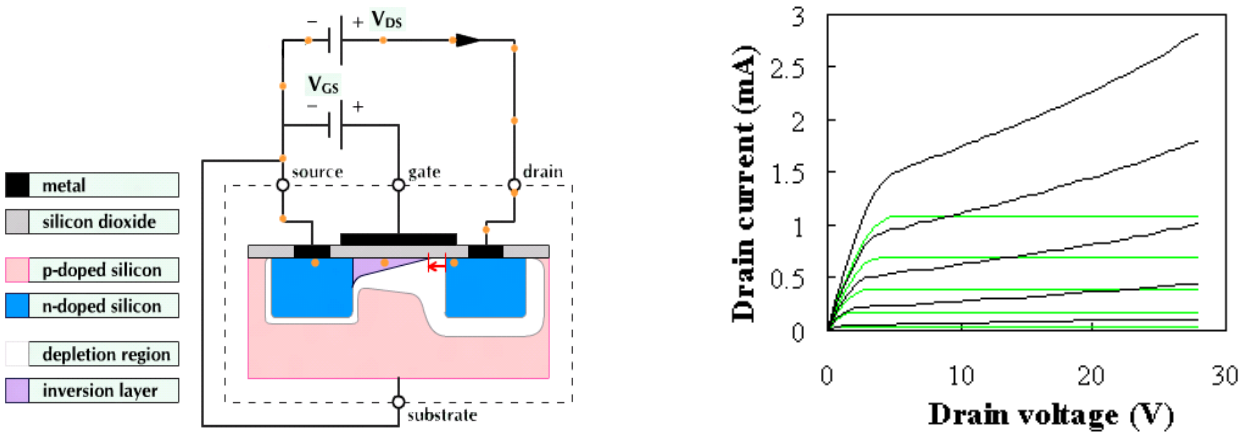

Fig. 2.19 Structure and current-Voltage characteristics of a MOSFET considering channel length modulation

(b) Punch through

On continuously increasing the applied drain bias, the drain side depletion region becomes more and more wide and an extreme situation of channel length modulation may occur where the source and drain depletion regions become so close, that the effective channel length almost reduces to zero. Such extreme case of channel length modulation is termed as punch through. Thus, the channel region underneath the gate becomes the function of drain voltage and causes an undesirable rapid increase in the drain current with an increase in drain voltage.

Apart from the major short channel effects discussed so far, there are some other issues like gate leakage current, random dopant fluctuation, source-drain resistance and some fabrication process related limitations [2.33] affecting the operation and performance of low dimensional devices.

2.2.2 SILICON ON INSULATOR (SOI) MOSFET:

The significant challenges associated with the scaling of planar CMOS can be alleviated by adopting several recently proposed non-conventional geometry MOS structures in order to continue with the scaling trend specified by ITRS. Silicon-on-Insulator (SOI) technology can be considered as a possible alternative to conventional bulk MOSFET when the ongoing trend of device dimension down scaling of MOSFET transistors can no longer be continued due to fabricational and operational limitations. Alternative SOI devices exhibit significant performance improvement to keep up with future Si technology. The primary aspect leading to a boom in SOI technology is that it still maintains silicon wafers to be basic starting point in the fabrication of integrated circuits by dint of being cheap compared to other semiconductors. Moreover, silicon facilitates the formation of a good oxide layer on its surface.

Different SCEs were studied experimentally by Young et. al. [26] and simulated as well to establish the efficacy of thin-film SOI MOSFETs in effectively subduing these detrimental SCEs as compared to conventional MOSFETs. This superiority of thin-film SOI devices is primarily due to thinner source/drain junction depths. For example, the junction depth of a SOI MOSFET is taken as 50-100 nm compared to the junction depth of 100-200 nm for the same gate length. The surface CMOS SOI MOSFET technology has been developed in parallel with the bulk CMOS technology. The family tree of SOI MOS technology is shown below:

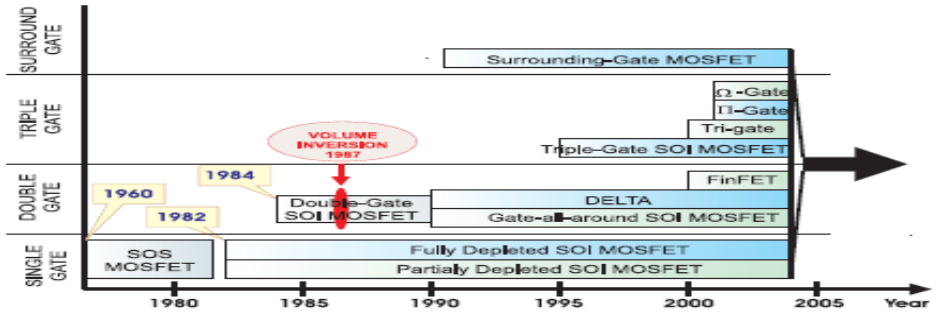

Fig. 2.20 SOI MOSFET technology road map

At first, Silicon On Sapphire (Al_2O_3) SOS transistor was proposed as early as in 1960. In this structure, sapphire was used as insulator. After observing the successful behavior of SOS MOSFETs for almost 20 long years, the researchers were motivated to realize Partially Depleted (PD) and Fully

Depleted (FD) Silicon-on-Insulator (SOI) MOSFET structures in the early 1980s and these were implemented to design circuits of microprocessors and memory chips. Journey from SOS to SOI involves the replacement of the mono-crystalline substrate, sapphire (Al_2O_3) (Figure 2.21 a) by a silicon dioxide layer (BOX - buried oxide) grown on silicon substrate (Figure 2.21 b).

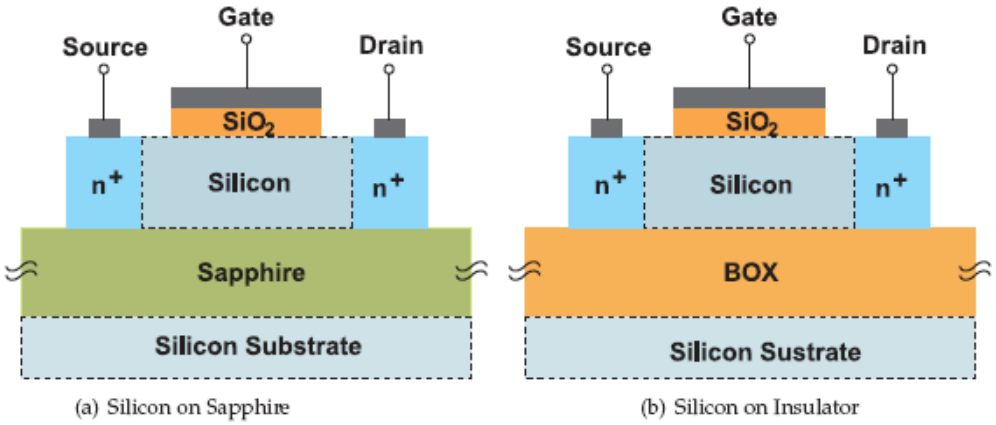

Fig 2.21 Cross sectional view of Silicon On Insulator (SOI) MOS device

The major advantage of the most promising alternative SOI technology over the conventional MOS technology is the existence of a buried oxide layer clearly shown in Figs. 2.22 and 2.23 which enables the SOI devices to attain increased scalability, very high operating frequency, low leakage currents and radiation hard operations in different applications. The presence of a layer of buried oxide (BOX) underneath the channel region prevents the extension of drain/source depletion regions into the substrate, thereby reducing the parasitic capacitances. This unique structural improvisation by incorporating the BOX layer results in many significant advantages in SOI devices. Some of them are: i) higher frequency of operation due to a lower parasitic capacitance, (ii) lower electric power dissipation due to reduced device leakage currents and (iii) ability of the BOX layer to remove radiation related performance degradation. The manufacturing compatibility with the existing bulk silicon CMOS technology represents a very important benefit for the SOI technology because of the need to keep the cheap silicon semiconductor as the base technology while developing further innovative devices. On the other hand, with the advent of some novel devices (like dual gate DG SOI MOSFET transistors) in the innovative SOI technology, the short channel effects are greatly minimized with a simultaneous improvement in sub-threshold slope.

Despite of having a plethora of advantages over conventional MOS technology, the newly proposed SOI device structures are not completely free from all sorts of short channel effects. Some of the notorious short channel effects existing in SOI devices are mainly due to floating body effect (especially in the partially depleted SOI devices) where the silicon substrate just below the gate does not have any electrical connection to some external bias, leaving a neutral region between the upper

and lower silicon interface. This floating body effect triggers several undesirable short channel effects in SOI devices namely: drain current overshoot, kink effect, latch effect, self heating effect, difficulties associated with Si thickness control for ultra thin Si films etc. In short channel SOI, the existence of BOX layer again induces a fringing field effect where drain and source electric fields terminate on the BOX oxide and back substrate interface, giving rise to a drain induced virtual bias on the back gate. This virtual back gate bias together with two dimensional charge sharing and DIBL effects result in an additional threshold voltage reduction. Due to the presence of more than one oxide and channels, the hot carrier degradation is more complex in SOI devices than bulk MOSFETs.

2.2.2.1 SOI Structure:

The unique feature of a SOI structure is the existence of a relatively thick (hundreds of nanometers) layer of silicon oxide in between a thin layer (tens of nanometers) of silicon and the silicon substrate [vide Fig. 2.24]. This layer of thick oxide isolating the silicon channel from the substrate is known called the buried oxide or BOX layer which is grown by the oxidation of basic silicon substrate or by oxygen implantation into silicon. Depending on the type of this thin silicon film on top of the BOX layer, the resulting device can be either SOI device (if the silicon film is mono-crystalline) or thin-film-transistor TFT (if the silicon film is polycrystalline). The thin silicon film is called the top Si layer, the SOI layer, or just the Si film. The Si substrate beneath the BOX may be termed as Si Substrate or supporting substrate. The SOI layer forming the body of a MOSFET is known as "Si body" or "SOI body".

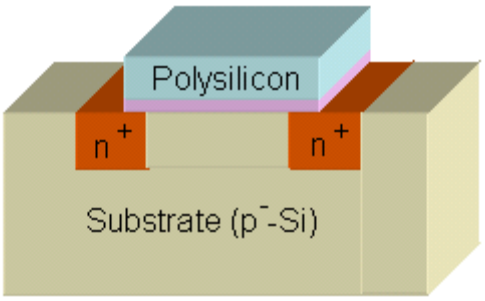

Fig.2.22 A bulk MOSFET cross section

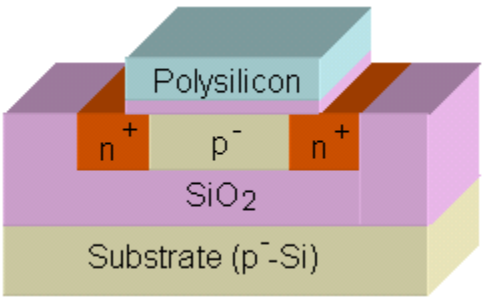

Fig.2.23 A fully depleted SOI MOSFET cross section

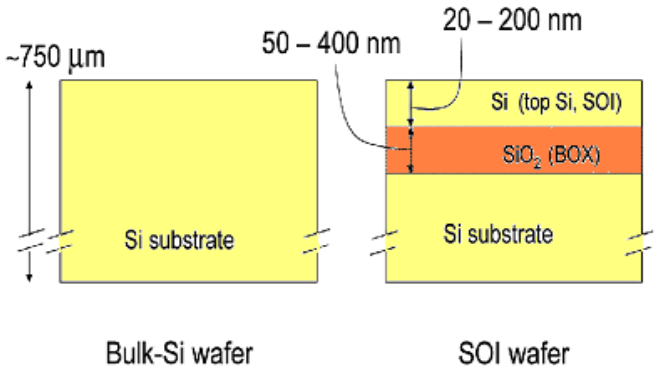

Fig. 2.24 The range of thicknesses of SOI and BOX layers

2.2.2.2 Operating modes of SOI MOSFET Devices:

Depending on the thickness of the thin silicon layer on top of the BOX layer, SOI MOSFETs operates either in fully depleted (FD) or in partially depleted (PD) regimes.

(a) Partially Depleted (PD) SOI MOSFET:

Figure: 2.25(a) shows partially depleted Silicon On Insulator MOSFET device. It is practically a MOSFET transistor realized with SOI technology. In PD SOI, the depletion region does not extend in the whole silicon film of SOI and therefore, a neutral region of undepleted Si layer exists, even after biasing the device in the inversion. Thus, the silicon film thickness is greater than the maximum gate depletion width. The neutral region of silicon is called "body".

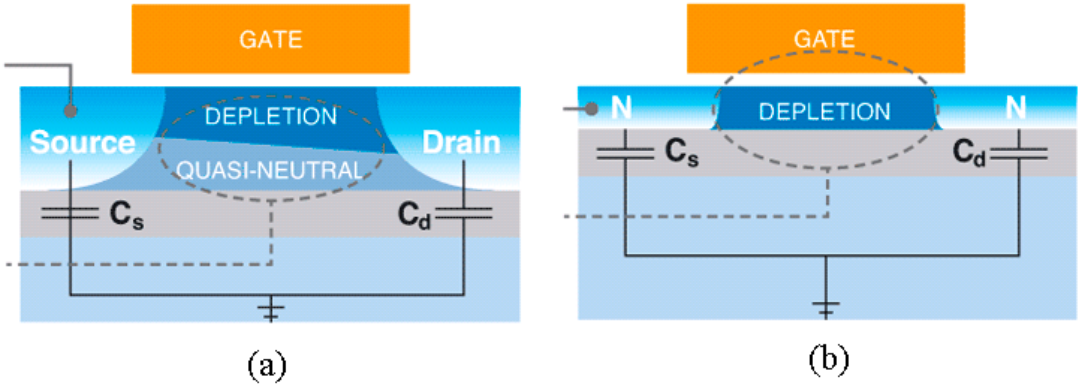

Fig. 2.25: A cross view for a (a) partially depleted and (b) a fully depleted SOI MOSFET

(b) Fully Depleted (FD) SOI MOSFET:

In Figure 2.25(b), a fully depleted SOI MOSFET is described. For a fully depleted SOI, the silicon thickness should be lower than the gate depletion width, which thus covers the entire silicon film under the oxide-semiconductor interface even before the gate voltage reaches the threshold condition, thereby eliminating floating body effects. The buried oxide must be very thick in order to drastically reduce the junction capacitance. However, following the scaling rule, the BOX thickness is also exposed to scaling process. Reduction of BOX thickness results in a better electrostatic control of the multi-gate SOI MOSFET transistors, at the cost of increased parasitic capacitances and reduced circuit speed.

A fully depleted device is more advantageous than a partially depleted device as it offers the following benefits: immunity from soft-error [2.34], protection from kink effect [2.35], increased circuit operating speed, reduced power consumption with substantial improvement in sub-threshold swing [2.36]. Moreover, fabrication of FD SOI devices is easier than bulk devices due to a lesser number of masks required in fabrication [2.37].

2.2.2.1 Advantages of SOI MOSFETs:

The performance advantages of a SOI MOSFET attributed by the presence of the BOX layer underneath the conducting channel are summarized below:

(a) Reduced Parasitic Capacitance:

The schematic diagram in Fig. 2.26 illustrates various components of parasitic capacitances in bulk and SOI MOSFETs. It can be seen from the said figures that the existence of thick layer of SiO_2 (BOX layer) underneath the silicon channel by virtue of having much reduced dielectric permittivity than silicon considerably reduces the source-substrate and drain-substrate parasitic capacitances which effectively increases the speed of SOI devices. The relation between power consumption and access time has been illustrated in Fig. 2.27 considering a 4 MB SRAM.

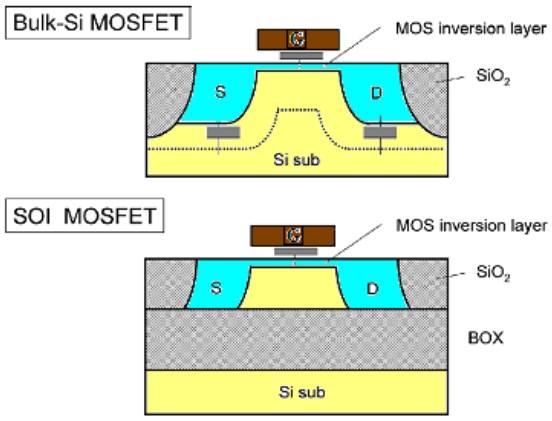

Fig. 2.26 Parasitic capacitances in bulk-Si and SOI MOSFETs

For a particular power consumption, presence of the BOX layer in SOI devices improve their speed performance by almost 20-25% compared to an equivalent bulk device by significantly reducing the parasitic capacitances. Moreover, power consumption of a SOI device is reduced by half to one-third of that required by bulk MOSFETs to achieve a certain access speed. This momentous improvement in speed and power consumption attained with SOI devices corresponds to performance gain obtained by jumping one technology node ahead.

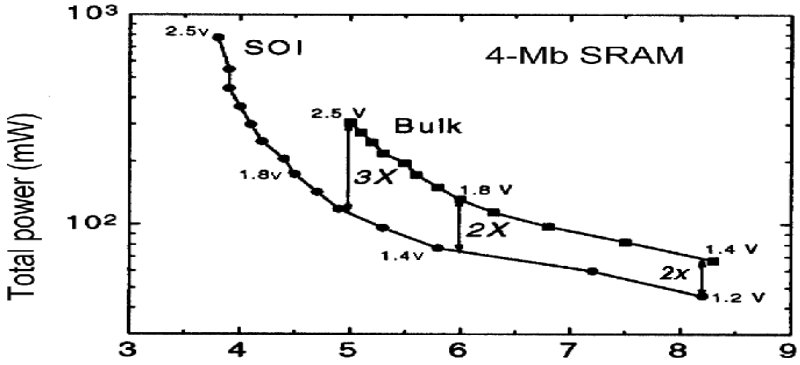

Fig.2.27 Power consumption and access time behavior for a 4 MB SRAM (SOI vs bulk)

(b) Ideal device isolation:

Normally, adjacent SOI devices are isolated from each other laterally by an insulator film. The existence of a thick BOX layer provides an additional level of vertical isolation between adjacent SOI devices [2.38].

(c) Smaller layout area:

The near ideal device isolation provided by the incorporation of a BOX layer facilitates closer packaging of the SOI devices as compared to the bulk ones. The n^+ and p^+ diffusion regions can be connected together forming the output of CMOS inverter due to the presence of the buried layer. This reduces the overall size of the individual SOI MOSFETs resulting in a higher circuit package density [2.25, 2.38].

(d) Latch-up prevention:

The problem of accidental latch up in conventional bulk MOSFET based CMOS circuit sets a limit on the maximum operating voltage. Latch up occurs when the parasitic PNPN or NPNP thyristor existing in a bulk MOS based CMOS (shown in Fig.2.28) turns on. This issue can be solved in SOI devices having a BOX layer which insulates the source/substrate and drain-substrate p-n junctions (illustrated in Fig. 2.28) eliminating any chance of such parasitic capacitance formation. This particular feature of SOI based circuits makes them automatically immune to latch up induced breakdown mitigating the need of any special circuit or fabrication process to prevent latch up [2.25, 2.38].

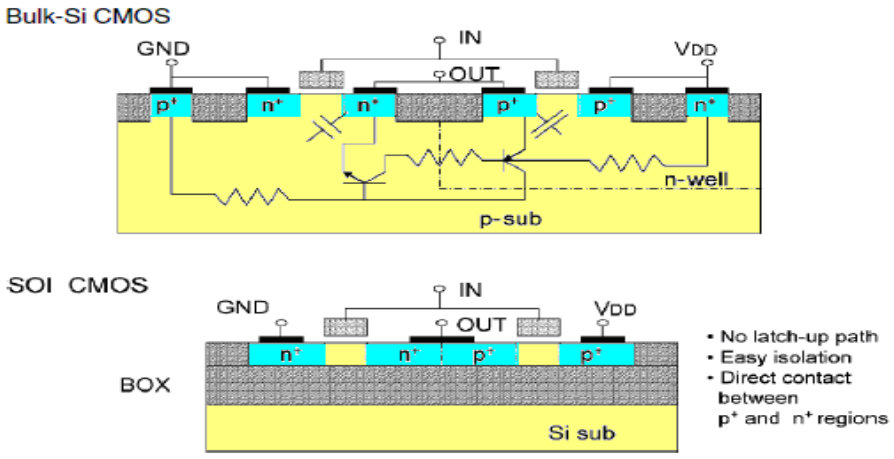

Fig. 2.28 Bulk device showing parasitic thyristor and a SOI showing absence of such parasitic thyristor

(e) Small p-n junction leakage current:

SOI MOSFETs come with an inherent advantage of ultra thin silicon film where the n+ and p+ regions are formed by doping the thin regions by relevant dopants creating p-n junctions only at the sidewalls of those shallow diffused regions. The reduced depth of these p-n junctions leads to a

remarkable decrease in junction leakage currents which is a critical requirement for low stand-by power applications (mobile phones, PDAs for example) in order to enhance battery life.

(f) Stacked gate speed improvement:

The floating body effect witnessed in SOI MOSFETs keeps the body of the device floating unless some special layout is designed so as to connect the body to ground potential. Let us consider a NAND gate implemented with bulk Si MOSFETs for example. It can be seen from Fig. 2.29 that the bodies of both the pull-down transistors are grounded allowing the flow of current to ground, thereby developing a negative bias in the body region of a pull-down transistor. This problem of negative body bias increases the threshold voltage resulting in higher fall time. On the other hand, if the same NAND circuit is implemented using SOI MOSFETs, the body attains a positive bias leading to a lower threshold voltage and consequently a larger drain current and a lower fall time, thereby improving the speed of performance [2.25, 2.38].

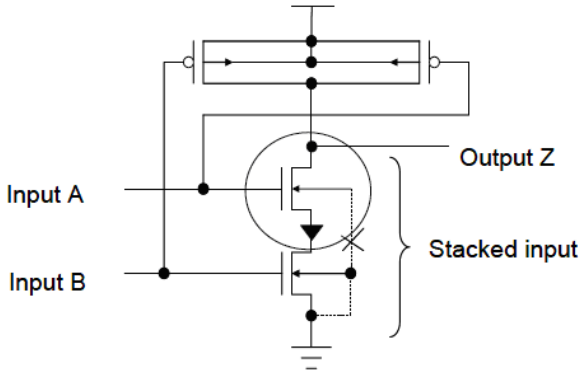

Fig. 2.29 A stacked gate circuit implemented with bulk-Si MOSFETs

(g) Reduced SCEs:

SOI MOSFETs with ultra thin body have reduced source/drain region depths. This ultra thin channel region allows better gate control over the channel potential profile resulting in an effective reduction of various short channel effects [2.25, 2.38].

(h) Radiation hardness and good soft-error immunity:

Trace amounts of radioactive elements existing in IC materials are the source of various unwanted highly energized radioactive particles (neutrons or alpha particles etc.). These generated radioactive particles possess high energy in the range of about 5MeV making it possible for them to penetrate through silicon upto depths of 25μm! As these highly energized particles penetrate through the silicon crystal, electron-hole pairs are generated along their path of movement which results in an effective accumulation of positive and negative charges of almost 10fC per micron sufficient enough to destroy the stored memory charge of a DRAM cell or to disturb the memory state

of an SRAM cell. Soft errors are also caused by neutrons generated as a result of secondary cosmic rays. Figure 2.30 depicts the soft error rate (SER) for a 64-kbit DRAM formed on an SOI substrate as a function of the thickness of the SOI layer. On careful observation, it can be inferred that the SER decreases as the layer becomes thinner. Innovative SOI structures removes these radiation-related issues as most of the electron-hole pairs generated by alpha particles are blocked by the BOX and are not allowed affecting the device layers.

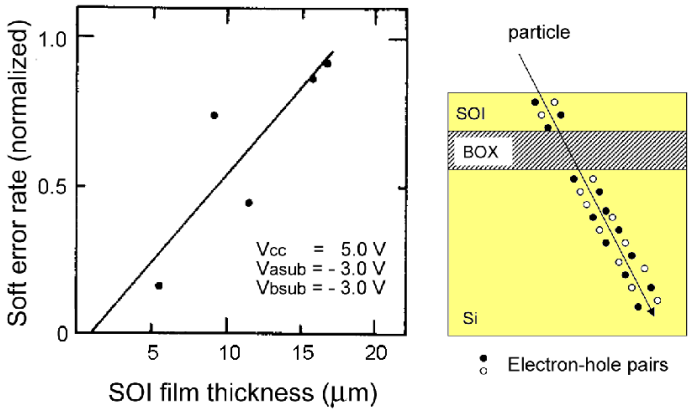

Fig. 2.30 Depiction of the soft-error rates

2.2.2.3 Some characteristic features of SOI MOSFETs:

Some intrinsic characteristics of SOI MOSFETs are now being discussed below to gain a better insight about the device operations.

(a) Kink effect:

This particular feature is observed in the drain characteristics of SOI MOSFETs where a sharp rise in drain current occurs beyond a specific drain voltage keeping the gate voltage fixed at a certain value. This sharp rise in drain current is known as '***kink effect***' which is basically caused due to a combined effect of impact ionization and parasitic bipolar effect discussed earlier. Considering an n-channel SOI, the electrons moving with high kinetic energy towards the drain gain sufficient energy to generate additional electron-hole pairs by impact ionization induced by high drain electric field. The newly generated electrons come under the drain bias pull and move towards the drain and contribute to the increase in drain current. On the contrary, the newly generated holes move towards the source and accumulate in the body region increasing the body voltage leading to threshold voltage drop and subsequent increase in drain current. This abrupt rise in drain current at a particular drain voltage is known as 'kink effect' which is most commonly evidenced in PD SOI MOSFETs due to the undepleted body [2.25, 2.38-2.39].

(b) Dynamic Floating body effects:

The undepleted body is isolated from the main channel region and does not have a fixed potential. The effect of different values of body potential on the device performance is collectively termed as "***floating body effects***". As the PD SOI MOSFETs have a layer of undepleted body, the floating body effects are more commonly observed in PD SOI [2.38-2.39]. On the contrary, the FD SOI shows stable performance unaffected by dynamic floating body effects. The holes generated as a result of high drain electric field induced impact ionization accumulate in the body altering the body potential which leads to dynamic floating body effects evident from the device behavior when it is operating in a circuit.

(c) Parasitic Bipolar Effects:

The drain electric field induced impact ionization results in the creation of electron-hole pairs out of which the holes mount up in the body region. Considering n-channel SOI, the body region rich with holes along with the n+ source and drain regions forms a '**parasitic bipolar transistor**' with the source, body and drain terminals functioning as the emitter, base and collector terminals of the parasitic bipolar transistor respectively. Such parasitic bipolar transistor is typically more common in PD SOI compared to FD SOI due to the undepleted body region. Normal operations of a device get severly hampered by such a 'parasitic bipolar transistor'. Some of the negative impacts are: an observable reduction in threshold voltage, steep sub-threshold slope, reduction of the source-to-drain breakdown voltage, undesired single transistor latch phenomenon etc. to name a few [2.38-2.39].

(d) Threshold Voltage Roll-Off (TVRO):

One of the most common short channel effect observed in nano dimensional devices is the proportionate decrement in device threshold voltage with a reduction in the dimension of channel length and is known as '***Threshold Voltage Roll-Off (TVRO)***'. SOI MOSFET, being an improvised non-conventional semiconductor device, mitigates several performance degrading short channel effects compared to conventional MOSFETs. Thus SOI (particularly FD SOI) devices show significant improvement in threshold voltage roll off characteristics [2.38-2.39].

(e) Sub-threshold slope:

Another important characteristic of SOI MOSFETs is their steep sub-threshold slope close to the limiting value of 60mV/decade. Again, the FD SOI excels the PD SOI in sub-threshold behavior due less SCEs [2.38-2.39].

(f) Self Heating Effect (SHE):

The performance improvements evident in SOI MOSFETs are mainly attributed by the presence of an insulating BOX layer isolating the body region from the silicon channel. However, this BOX layer itself is again responsible for another unavoidable issue of poor thermal behavior in SOI causing heating effect as shown in Fig. 2.31. Due to the BOX layer insulation, heat generated in the channel due to drain current is not able to escape through the buried layer which in effect increases the temperature of the high power consuming device substantially higher than that of its surroundings. This phenomenon is termed as '***self–heating'***. Self heating effect enhances lattice temperature which, in turn, degrades carrier mobility. Now, it is well known fact that the electron mobility is far more than hole mobility. Moreover, the chances of high temperature scattering induced mobility degradation is more for electrons than holes. These two factors attribute to the prominence of self-heating effect in NMOS transistor compared to PMOS equivalent. Mobility degradation in turn negatively impacts the drain current and causes almost 6-7% reduction in saturation current in nSOI devices. The self-heating effect is a serious threat to device performance and reliability which can affect the operation of SOI MOSFETs through a variety of mechanisms such as reduced drive current, excess hot carrier current generation, diminished breakdown voltage and accelerated turn-on of the parasitic bipolar transistor.

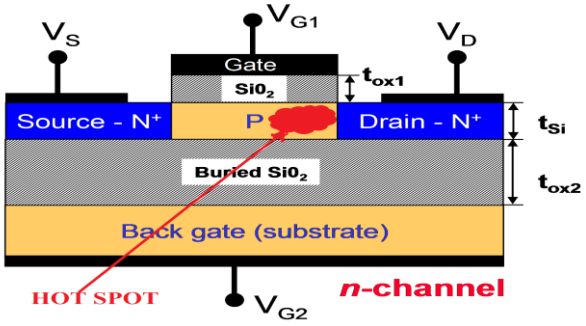

Fig.2.31 Theoretical model of self-heating

2.2.2.4 Disadvantages of simple SOI structure:

From the discussions so far, it can be inferred that SOI shows significant performance improvements over conventional MOSFET. However, short channel SOIs are still limited by some inherent drawbacks which are mainly due to the various SCEs. The disadvantages can be synopsized as [2.40-2.43]:

i. Floating body effects in partially depleted SOI MOSFETs results in '***Kink effect***' in DC circuits resulting in drain-current overshoot in switching circuits [2.41].

ii. ***Dynamic floating body effects*** and ***parasitic bipolar effects*** are inherent features of the SOI structure which are very difficult to mitigate [2.42]. These become significant in ultra low dimensional SOI structure thereby degrading device performance.

iii. The body-source junction gets accidentally forward biased by high drain voltage, thereby resulting in sharp rise in ***off-state leakage current***.

iv. Fabrication of ***ultra-thin films*** is crucial for the realization of fully depleted SOI devices. This involves many critical design adjustments for growing such thin films [2.40].

v. Buried oxide-silicon layer ***interface quality*** must be very good in order to ensure reduced interface scattering and other effects.

vi. The lower thermal conductivity of silicon oxide in the BOX layer of SOI structure leads to ***self heating effect***, which can seriously impact device performance and reliability through a variety of mechanisms [2.43].

SOI structure is more immune against different SCEs compared to short-channel conventional MOSFETs, but it is not fully free from the adverse effects of SCEs. So there are plentiful scopes for further performance upgrading [2.44].

2.2.2.5 Some improved SOI Structures:

Researchers are continuously putting effort to propose several improvised non-conventional device structures capable of solving the problems of SCE induced performance deterioration in sub-nano dimensional SOI MOSFETs. Some of those alternative devices have been presented below:

(a) Metal Source and Drain SOI MOSFET:

Thin-film SOI MOSFETs comes hand-in-hand with the unavoidable problem of increased resistance of source and drain regions. This issue can be addressed by realizing the source and drain regions to be formed of metal or silicide which requires formation of ohmic contacts between source/drain and channel along with careful prevention of formation of Schottky barriers between source-channel or drain-channel regions. A very low (ideally zero) Schottky barrier is desirable for allowing the establishment of the required ohmic contact. Existence of such low Schottky barrier in a metal source/drain SOI MOS makes the height of the barrier dependent on applied gate bias when the

device operates in inversion mode. Thus, to avoid this dependence, SOI MOSFETs with metal or silicide source/drain regions are preferably operated in accumulation mode [2.45-2.46].

(b) Metal gate SOI:

Polysilicon gates are normally used for long channel MOSFETs. However, following scaling trend, when the device dimension reaches sub 100nm regime, several operational difficulties associated with boron penetration, poly-Si gate depletion and high gate resistance come into play and negatively affects device performance [2.47]. These problems triggered the need to search for some alternative gate. The concept of using a metal as gate electrode was first proposed by Ushiki et. al [2.48] and was experimentally demonstrated by replacing poly-Si gate by tantalum gate as shown in Fig. 2.32 which presents a comparative analysis between metal and poly-Si gate in terms of their respective threshold behavior.

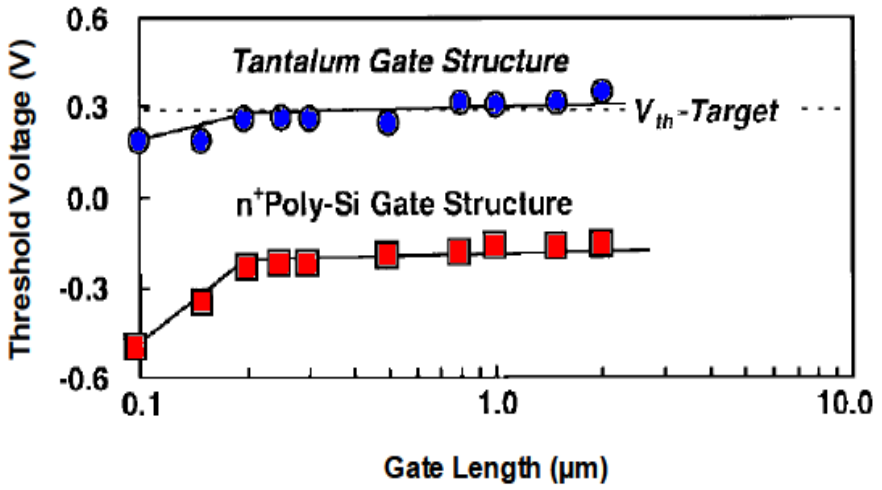

Fig. 2.32: Variation of threshold voltage with respect to channel length of an FD SOI n-channel MOSFET device using tantalum and polysilicon gates [2.48]

The basic idea of metal gate was to modify the threshold voltage of SOI devices by utilizing the workfunction of tantalum instead of the thin-film doping concentration of poly-Si gate. A comparative analysis of threshold voltage variation with respect to the channel length of a FD SOI NMOSFET with tantalum and polysilicon gate electrodes having film thickness of 100nm, front gate oxide thickness of 5nm and a buried oxide thickness of 420nm can be observed from Fig.2.32 [2.48]. The purpose of threshold voltage adjustment can be done by proper selection of work function value of the metal to be used as gate electrode. This mitigates the problems associated with polysilicon gate depletion in polysilicon gates, which in turn reduces several SCEs [2.49-2.50].

(c) Thin body FD SOI with raised source/drain:

Presence of unwanted sub-surface leakage paths in low dimensional devices is one of the major SCE degrading device sub-threshold characteristics. These leakage paths in SOI devices can be avoided by chosing thin silicon films making them thin-body FD SOI MOSFETs. Carriers flow from source to drain in such thin-body MOSFETs through the restricted thin silicon film in close proximity with the gate electrode which thus has excellent control over the lightly doped conducting channel. Thus, adopting thin-body low dimensional device structures alleviates the problems associated with threshold voltage variation as a result of random dopant atom variation in highly doped channels and channel impurity scattering induced mobility degradation [2.51].

Thin body structures on the other hand, have thin source/drain regions which effectively increases the source/drain series resistances resulting in subsequent deterioration in device current. This problem of high series resistance of thin source/drain regions can be solved by using the concept of raised source/drain regions as proposed and experimentally demonstrated by Choi et. al. [2.52]. Fig. 2.33 (b) depicts a raised source/drain MOSFET structure.

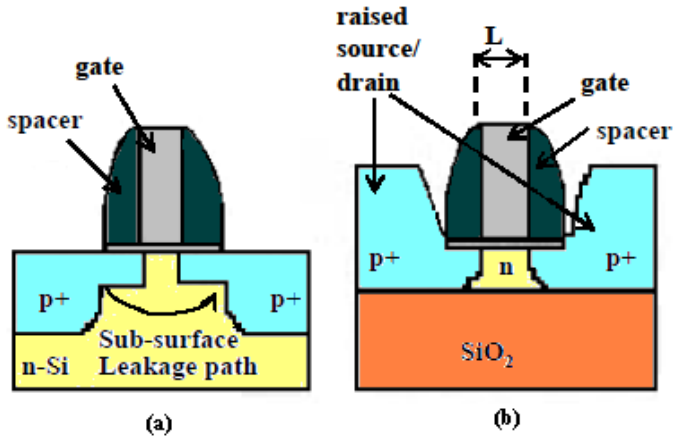

Fig. 2.33 Comparative study of device structures for (a) a conventional MOSFET and (b) a raised source/drain thin-body transistor [2.51]

However, parasitic capacitances between the raised source/ drain and the gate will inherently exist in such raised S/D structures which become the primary deterrent factor affecting the speed of operation and power consumption. If the distance between the raised S/D and gate is increased, the parasitic capacitances are reduced in addition to proportional increase in series resistance. This

mandates the need for an optimization between the drain current reduction and parasitic capacitance formation while considering such a raised S/D MOS structure.

(d) Ground plane SOI MOSFET:

Uncontrolled penetration of electric field lines from the drain and source regions into the channel region through the buried oxide (BOX) layer can be considered as another possible short channel effect. This unwanted field line penetration can be prevented by adopting some new device structures [2.53-2.55] with ground-plane formed in the substrate region underneath the BOX layer. This can be done using two approaches as depicted in Figs. 2.34 (a) and 2.34 (b). In Fig. 2.34 (a), it can be seen that a heavily doped region can be placed in the substrate underneath the BOX layer either between the source-channel or drain-channel which serves the purpose of blocking the penetration of electric-field lines. Yet another approach of blocking this field-line penetration is demonstrated in Fig. 2.34 (b) where the heavily doped electric field stop is grown just below the conducting channel. These electric field stop regions improve the SCEs and subthreshold slope significantly by preventing unwanted field line penetration from the drain/source regions into the channel region [2.53].

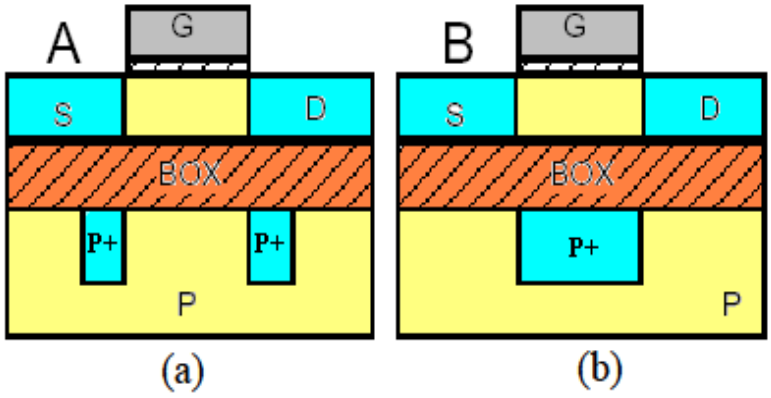

Fig. 2.34: Ground plane or 'electric field stop' grown under (a) source-channel and drain-channel junction [2.54] or (b) channel region [2.55]

(e) Graded channel SOI:

Yet another approach for mitigating short channel effects in sub-nano devices is the use of graded silicon channel. A comparative picture of threshold voltage variation with channel length for a uniformly doped channel and graded channel SOI MOSFET is depicted in Fig. 2.35.

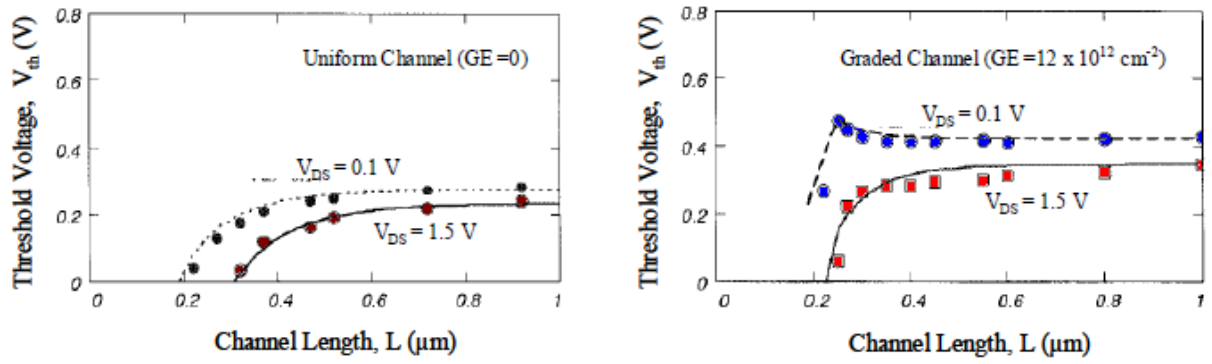

Fig. 2.35: Variation of threshold voltage vs channel length of SOI MOSFET with uniform and graded channels [2.56]

In case of a graded channel, the doping concentration at the center of the channel is same as that of a uniformly doped channel; while the source and drain ends of a graded channel are heavily doped using gate-edge (GE) implant techniques. The heavily doped drain and source ends of the graded channel helps to achieve considerable improvement in subduing the short channel effects, especially at large drain voltage, as compared to an equivalent uniformly doped channel device.

Instead of using graded channel, a thin-film device with heavily doped channel may also be used to suppress the destructive SCEs. This approach, however, comes hand in hand with the problem of excessively high value of threshold voltage required to achieve channel inversion in such a heavily doped channel.

(f) HALO doped SOI:

Another promising approach to alleviate the problems associated with short channel effects in ultra low dimensional devices is the use of HALO or pocket doping technique where a selected region is much heavily doped compared to the rest of the channel. HALO implantations are found to be beneficial for various applications. Selective HALO implants reduce the off-state leakage current and increases linear and saturation region drive currents of transistors operating as digital switches. On the other hand, HALO implants are essential for analog base-band applications using longer channel transistors. However, HALO implants adversely impact high speed applications of short channel transistors operating in strong inversion [2.57]. A high dose HALO implantation increases the kink

effect in PD SOI and affects the distortion characteristics of SOI transistors operating as resistor [2.57]. It was experimentally demonstrated by Taur et. al. [2.58] that a MOSFET of channel length 25 nm exhibits excellent SCE suppression if its channel and body regions have super-HALO highly non-uniform two dimensional doping profile. Recently, different research groups have reported asymmetric single HALO (SH) doping for bulk [2.59-2.66] as well as SOI MOSFETs [2.63-2.64]. A schematic cross sectional view of a typical SH SOI n-channel MOSFET [2.63] is shown in Fig.2.36. Single HALO doping carefully adjusts the threshold voltage, thereby suppressing the harmful short channel and hot carrier effects.

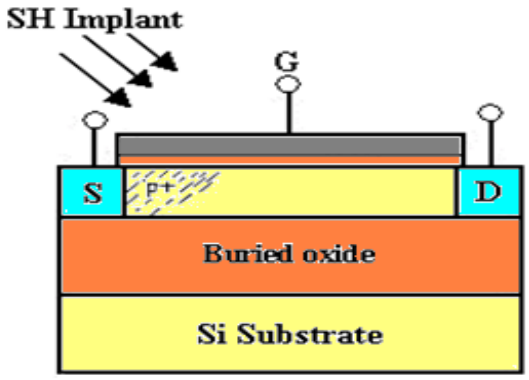

Fig. 2.36: Cross-sectional view of a single-halo (SH) doped n-type SOI MOSFET [2.63]

(g) Multiple gate SOI MOSFET:

Conduction in conventional long channel MOSFETs is attributed to the accumulation of channel charge and formation of inversion layer controlled primarily by the gate induced vertical electric field. But, when the device dimension approaches sub nano regime, the intrusion of electric field lines from the drain into the channel region results in two dimensional charge sharing where both gate and drain electric fields simultaneously control the channel charge. This, naturally reduces the sole gate control over the channel charge, thereby leads to various unavoidable short channel effects. Some special structures known as 'multiple gate' SOI MOSFETs are recently gaining significant research spotlight due to their abilty to mitigate the SCEs associated with the unwanted infringement of electric field lines from the drain end. Multiple gate structures can be double-gate transistors, triple-gate transistors, quadruple-gate transistors, gate-all-around transistors, π-gate transistors, DELTA transistor and vertical pillar MOSFETs etc. [2.67]. Presence of more than one gate enhances the overall control of gate electrode on the channel charge, increases device drive current due to the volume inversion phenomenon and show improved sub-threshold slope, thereby resulting in better device scalability [2.68-2.70].

Extensive research is being done on multi-gate MOSFETs. There are mainly two categories: ***planar and vertical***. The ***planar multi-gate*** device structures are basically improvised SOIs comprising of ground plane and back-gate devices. Some innovative ***vertical multi-gate*** structures are FinFET [2.71-2.74], Omega FET [2.75] and Tri-gate [2.76] structures as shown in Fig. 2.37.

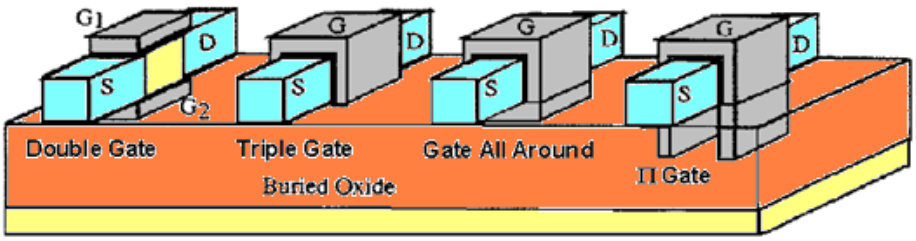

Fig. 2.37: Double-gate, triple-gate, gate all around (GAA) and Π-gate SOI MOSFETs [2.67].

A planar dual-gate device can be operated in two modes: *tied gate or independent gate*. In tied gate mode, both the front and back gate electrodes are connected together to the same gate voltage and simultaneously control the channel charge providing better sub-threshold characteristics and enhanced scalability. In independent mode, the front and back gates are operated separately with two gates independently connected to separate gate voltages. This enables front-gate threshold voltage control using back gate bias. However, the two independent gates introduce an additional gate-to-gate capacitance.

The concept of double-gate was first recommended by Hayashi in 1984 [2.77] and it exhibited enhanced gate control over the channel charge leading to increased transconductance due to the volume inversion effect [2.78] and better subthreshold slope. Since then, double-gate devices have been fabricated and experimentally studied by several groups. However, the fabrication of double gate MOSFETs involved complex process steps like lateral epitaxial overgrowth and an underneath cavity etching [2.79] making double gate devices somewhat commercially unpopular. Moreover, the silicon channel thickness existing between two gates is usually smaller than the physical gate length of the nano scale device. Thus, patterning of such ultra thin film poses a difficult challenge in fabricating double-gate transistors.

The Tri-Gate device is a mesa-isolated SOI device where the gate electrode wraps the entire active silicon channel. The three surfaces i.e. two sides of height H, and the top surface of width W simultaneously control channel charge conduction. The conduction in the corners, where two side surfaces meet the top surface, is a critical contributor to the device operation. On the contrary, the FinFET has a higher aspect ratio than the Tri-Gate device. The top surface is covered by a thick

oxide and does not contribute to the channel conduction. The 'fin-width' is defined by its height and width and the 'fin-height' is defined by the thickness of the active silicon channel.

In order to enhance the scalability of low dimensional devices to a further extent, surrounding gate or gate all around devices have been gaining significant research interest by dint of their unique feature of gate wrapped channel. The most fascinating feature of the surrounding gate MOSFETs lies in its novel device geometry which significantly enhances the device packing density along with providing a host of advantages. The surrounding gate electrode encircling the channel on all sides facilitates an enhanced electrostatic control over the channel conduction and results in remarkable improvement in device sub-threshold behavior and better suppression of unwanted Short Channel Effects (SCEs) in sharp contrast with conventional single and double gate counterparts.

Fig. 2.38 below compares different multi gate structures: double, triple, quadruple and Π-gate devices in terms of threshold voltage roll-off and DIBL in the same figure. The quadruple gate provides the best performance with Π-gate being the close competitor. The results show that the gate electrode of the above mentioned structures provide efficient shielding of the channel from the electric field lines originating from drain.

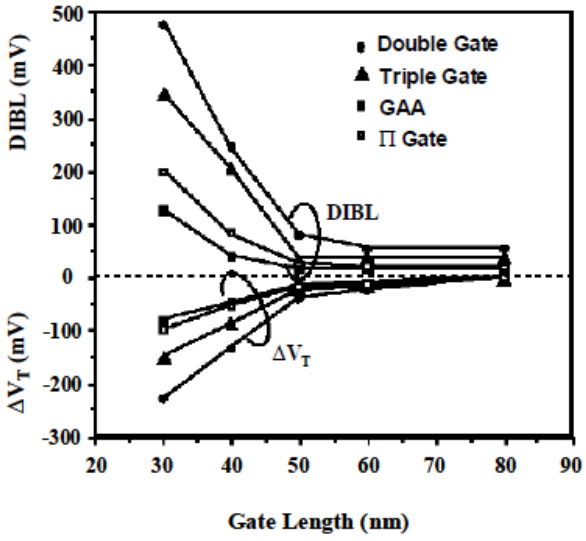

Fig. 2.38: Comparison of TVRO and DIBL in double, triple, quadruple and Π-gate SOI MOSFETs [2.67]

(h) Dual Material Gate (DMG) SOI MOSFET:

When the device dimension of conventional MOSFET is scaled down to sub 100nm, sub-threshold current begins to flow even if the gate voltage is well below the threshold voltage. This occurs due to two dimensional charge sharing by both gate and drain applied biases due to an increase in drain electric field resulting in several short channel effects, especially DIBL. Some structural

improvisations need to be done on the basic MOS structure so as to reduce the drain side electric field and its consequent impact upon the channel.

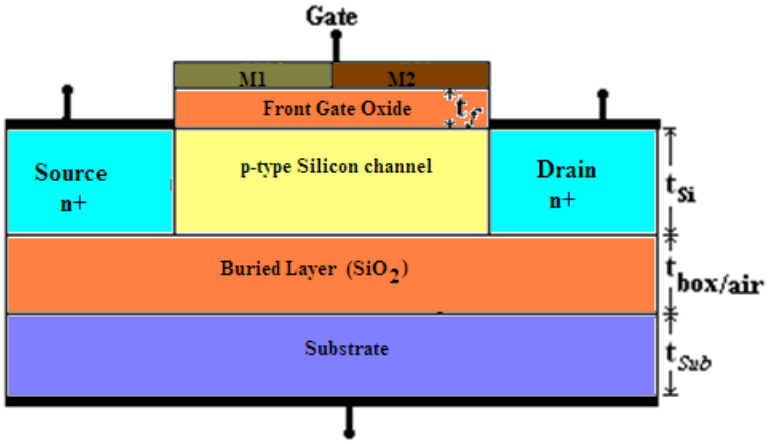

Fig. 2.39: Dual Material Gate (DMG) SOI MOSFET

Proposed by Long et. al. [2.80], the Dual Material Gate system is a possible solution for these SCE associated problems in ultra low dimensional devices by exploring the concept of "***gate-material engineering***" to adjust the threshold voltage as an alternative of conventional "doping engineering". In DMG, two different metals having different workfunctions are amalgamated side by side forming a single gate electrode as shown in Fig. 2.39. The discontinuity in workfunction value at the junction of two metals introduces a step in the surface potential profile [2.80] which screens the source side potential barrier from any random variation in drain bias, thus mitigating the DIBL induced performance degradation. This step in potential profile increases the channel electric field and subsequently improves the carrier transport efficiency in the channel. The DMG structure thus allows the designer to choose the channel doping, thin-film thickness, buried oxide thickness and permittivity flexibly in short channel SOI MOSFET design.

(i) Buried Insulator Engineering:

Fig. 2.40 elucidate threshold voltage roll-off variation with buried oxide permittivity as a result of charge sharing and DIBL considering SOI MOSFETs with channel lengths of 30nm and 500nm [2.81]. On careful observation, it can be understood that as the permittivity of the buried oxide is reduced, there is a notable reduction in the penetration of electric field lines from the drain end into the channel which has a direct effect in improving the DIBL along with other SCEs. But, the effect of buried layer permittivity on the charge sharing is not so significant.

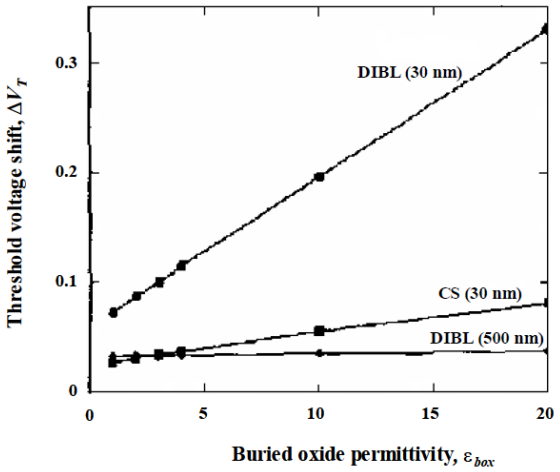

Fig. 2.40: Variation of threshold voltage roll-off vs buried oxide permittivity due to DIBL and CS [2.46]

In this approach, normally used SiO_2 in the buried layer of SOI can be replaced with sapphire, silicon nitride, silicon carbide, gallium arsenide etc. attempting to improve device performance. It can be noted that 'air' having the lowest permittivity of unity offers highest electrostatic isolation for the active channel region from unwanted field line penetrations. Replacing the SiO_2 BOX layer of a SOI MOSFET with a layer of 'air' results in an altogether new structure known as ***Silicon-On-Nothing MOSFET*** and has been discussed in the next section.

Some improvised alternatives to SOI devices:

2.2.3 Silicon On Nothing (SON) MOSFET:

Based on the concept of buried layer engineering, one of the most recently developed innovation on SOI structure is the Silicon-on-Nothing (SON) MOSFET where the buried oxide of simple SOI structure is replaced with air. It has been proved both theoretically as well as experimentally that the layer of air-gap in the SON structure is capable of suppressing SCEs and exhibits excellent electrical performance [2.82-2.84]. SON MOSFET is basically an improvised SOI structure which can be considered as a lucrative alternative solution to achieve further scalability in SOI structures to meet up with the aggressive scaling requirements of ITRS [2.85].

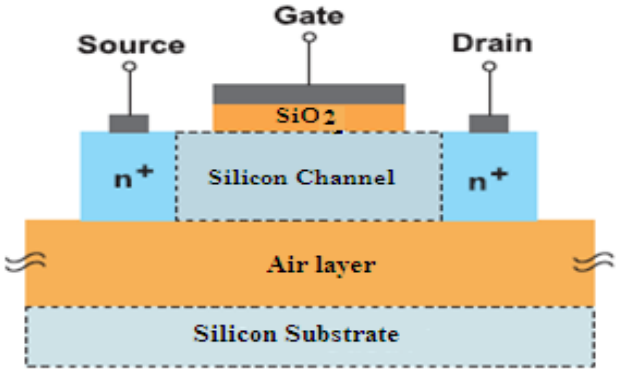

Fig. 2.41 Silicon-on-Nothing (SON) MOSFET

2.2.3.1 Advantages of SON over SOI:

The major advantage of SON architecture as compared to a fully depleted SOI MOSFET is the highest dielectric isolation of the active channel layer achieved by using 'air' as buried layer material [2.86]. Lower permittivity reduces electrostatic coupling through the buried layer and relaxes the requirement of an ultra thin silicon film. The presence of the buried 'air' layer embedded below the Si active film having lower dielectric permittivity than oxide of SOI significantly reduces the parasitic capacitances between source/drain and substrate, thereby considerably increasing the operating speed of SON devices [2.88]. In addition to retaining all the advantages of existing SOI structure, SON structure improves radiation immunity in extreme environment, reduces power consumption, enhances further scaling capability, shows low noise, develops higher short channel effect immunity, offers faster switching action and reduces cost [2.88].

2.2.4 Junctionless Devices

So far, some non-conventional MOSFET and SOI/SON devices have been discussed. All these devices are mere improvised versions of the basic MOSFET transistors which are all junction based devices. Wherever there is a contact between two semiconductor regions doped with opposite polarities, a junction is always formed. A p-n junction is the commonest junction present in almost all conventional semiconductor devices. The basic property of such a junction is to allow or block the flow of current depending on the type of bias applied. The current conductivity of such junction based semiconductor device is totally controlled by the junction itself which mandates precise fabrication of high quality junctions, thereby triggering up the production cost excessively. Moreover, the exponential increase in the device packing density as predicted by Moore requires extreme miniaturization of the device dimension to produce smaller and more economical high performance ICs. As a result, the dimensions of individual transistors in the ICs are becoming so small that it is

exceedingly becoming difficult to continue with the conventional junction based devices. The major difficulty to fabricate such nano scale junction based conventional transistors discussed so far is the formation of ultra-sharp source/drain junctions for devices with dimensions in the range of sub-nanometer. If the channel length is very small (~ 10 nm), the formation of ultra-sharp source and drain junctions results in a considerable orders of magnitude difference in doping concentration over a distance of a few nano-meters. This drastic concentration gradient imposes stringent conditions on doping techniques and thermal budget.

In order to alleviate these problems, possible alternative, namely junctionless (JL) transistors are reported in some recent literatures. Junctionless transistor is an age-old concept. As early as in 1928, a junctionless device under the title "*Device for controlling electric current*" [2.89] was patented by Julius Edgar Lilienfield and the proposed device was popularly named as Lilienfield transistor. However, no research article was published. Basic operating principle of the proposed Lilienfield transistor bear striking resemblance with that of normal MOSFETs as in both devices, the channel current is controlled by an external applied electric field just as a simple voltage controlled resistor. The Lilienfield device had an ultra thin semiconductor film deposited on a thin layer of insulator which is again deposited on a metal electrode functioning as the gate terminal. Two contact electrodes are also present and the current flows between them akin to the drain current flowing between the source and drain terminals of MOSFETs. The conductivity of the ultra thin semiconductor film may be modulated by applying suitable voltage on the metal electrode which may fully deplete the semiconductor film making its resistance almost infinite and thereby switching the device to OFF state. The primary structural difference of the proposed Lilienfield device was that unlike conventional transistors, it did not have any junctions formed. It was basically a gated trans-resistor device where the applied gate voltage controlled the carrier density in the semiconductor film, and thereby the current. The concept was undoubtedly unique. But the limitations in available fabrication technology at that time did not allow Lilienfield to fabricate a working device based on his concept. However, this unique feature of junctionless trans-resistor laid the foundation of a new concept of Junctionless devices. Many years later in 2010, a research group at Tyndall National Institute under J. P. Colinge were able to fabricate world's first junctionless transistor [2.90] which was a quantum leap in modern semiconductor industry. Since then, several research innovations based on several structural improvisations on the basic junctionless transistor have been reported in literature [2.91-2.99].

By virtue of this junctionless architecture, the type and concentration of channel doping are identical to that of the source and drain extensions, thus eliminating the need to maintain doping concentration gradient. This prevents the possibility of impurity diffusion during thermal processing steps, thereby sufficiently relaxing the thermal budget making the fabrication quite simplified.

Consequently, the JL MOSFETs are seen to exhibit significantly improved turn-on and output characteristics, almost ideal value of sub-threshold swing, reduced source and drain resistances, appreciably high value of device ON state current and improved DIBL [2.91-2.94] along with interesting temperature characteristics which is attributed to the average sensitivity of carrier mobility on temperature when the impurity concentration is sufficiently high [2.95-2.96].

It has been studied from the available literatures that the Accumulation Mode (AM) working principle of thin-film double gate JL MOS devices enables them to achieve significantly reduced Drain Induced Barrier Lowering (DIBL) and Subthreshold-slope degradation as compared to Inversion Mode (IM) conventional MOSFETs [2.97-2.99]. Accumulation mode devices come with some added features like reduced sensitivity to the issue of gate underlap or overlap along with improved contact resistances. These devices are less sensitive to doping-fluctuations and thermal instability due to negative bias compared to equivalent inversion-mode devices and seen to exhibit less drain current variation with doping concentration. Extensive studies on junctionless transistors by several research groups testify that the junctionless devices operating in accumulation mode exhibit considerably improved short-channel electrical characteristics than conventional inversion mode devices thereby making it a suitable candidate for future nano devices.

2.2.5 Gate Material Engineering

Miniaturization of device dimension has become essential to sustain the growth of semiconductor and VLSI industry. However, it is evident from the above discussion that shrinking of device dimension gives rise to several bottlenecks which degrade the performance of the devices operating in sub-nano regime. Thus, continuous improvement in device performance can only be realized by combining efforts of device dimension down scaling along with development of some innovative device structures and improved material property, which is again limited by the fundamental physical limits to satisfy the aggressive specifications of the ITRS. Exploring the concept of gate work-function engineering may be another possible research avenue to realize devices with improved performances.

It has been widely studied that Boron penetration, polysilicon depletion effects, short channel effects pose a limit to future use of polysilicon gate. Due to these well-known problems, metal gates are becoming a possible alternative to standard poly-Si gates [2.100]. However, in spite of solving the problems associated with polysilicon, metal gates also face some stringent limitations such as chemical or thermal instability of high permittivity dielectric, adequacy in the range of available metal work functions, annealing required for the passivation of unintentionally trapped interface

charges, problems related to the damage of plasma layer as a side effect of cross contamination, reactive ion etching or material deposition [2.101]. Some of these are briefly discussed below:

- *Compatabity with High-k-Dielectric*: The combination of a high-κ dielectric gate oxide material and a poly-Si gate is not suitable for high performance applications. The metal gate electrode of a device operating in inversion mode efficiently protects the channel region from effects of phonon scattering occurring in the high-k dielectric.
- *Depletion Effects due to Poly-Si* : If donor doping concentration is much higher than acceptor doping concentration, potential changes in the poly-Si gate are negligibly small. However, if the poly-Si gates are lightly doped, the density of introduced dopants and concentration of carriers are seen to be dependent on the position creating a built-in electric field which is responsible for a built-in depletion occurring at the poly-Si/oxide interface.
- *High Gate Resistance* : Gate conductor resistance (Rg) and the gate to substrate capacitance (Cg) account for the delay in sub-micron range operation. Modern day CMOS devices widely use stacked gate electrodes with silicide (metal + poly-Si) to employ the inherent advantage of low sheet resistance of metal gates.
- *Reduction of Tunneling Probability*: If the thickness of gate oxide dielectric is sufficiently high, the carrier wavefunctions are not able to surmount the potential barrier and interfere with the gate electrode. However, following the MOSFET scaling rule, the gate dielectric thickness must be reduced along with the channel length to enhance the gate control, avoid short-channel effects and transconductance degradation. As a consequence, quantum mechanical tunneling takes place. Tunneling probability of carriers and subsequent off state leakage current can be suppressed considerably by adopting metal gates instead of poly-Si gates [2.102].

In 2D short channel devices, field at any point in the channel is a combination of vertical and horizontal fields. By adjacently placing two or three materials with dissimilar work functions to function as a single gate electrode, the vertical electric field at any point in the channel can be suitably adjusted, which, in turn, modifies the overall channel electric field resulting in a remarkable device performance improvement. This concept of 'gate material engineering' has already been discussed by presenting a Dual Material Gate (DMG) SOI structure. It has been argued that the dissimilarity of work functions of the two metals used in Dual Material Gate results in an abrupt step in the channel potential profile near the junction between two metals. This step like feature proves to be effective in suppressing the DIBL effect by screening the potential minima near the source side from any random variation in drain bias which effectively improves the device short

channel performance making 'gate material engineering' a possible research avenue to continue with the trend of device dimension down scaling.

The idea of gate material engineering can be extended further based on some innovative research works proposing the use of a metal alloy as gate electrode. Tsui et. al. [2.103] in their pioneering publication on work function engineered gate electrode proposed the concept of using a binary metal alloy as gate electrode for MOSFET applications. In recent times, Pan et. al. [2.104] proposed a fabricated ZnCdSSe alloy nanowire having a continuously varying constituent mole fraction by combining source reagent gradient along the device dimension in addition to a specified temperature gradient. Some more research accomplishments suggested a pulsed layer deposition based fabrication methodology for continuous spread thin film [2.105-2.107]. These published research works establishes the fabrication feasibility of a binary metal alloy gate electrode ($A_\alpha B_{1-\alpha}$) with continuous lateral variation of pure constituent work function in near future.

Motivated by the fabrication feasibility of such spatial composition graded gate electrode, Deb et. al. explored the idea of multiple material metal gate electrode to an extremely different level by considering a binary metal alloy ($A_\alpha B_{1-\alpha}$) gate electrode in a SOI MOSFET where the concentrations of individual constituent metals were continuously varied horizontally from source side (100% A) to drain side (100% B) [2.108]. Since then, several publications are available in literature which attempt to explore this novel concept of linearly graded gate electrode in various innovative device structures [2.109-2.112]. The vertical field and consequently the overall field in this system will be adjusted by the continuous variation of work function to reduce short channel surface potential asymmetry [2.108-2.110]. This in turn controls the DIBL significantly and improves the device performance by removing the uneven transition of surface potential and surface electric field.

2.2.6 Tunnel Field Effect Transistors (TFETs)

The tremendous escalation of present day nanoelectronics is dominated by the design and implementation of non conventional high performance high speed ultra nano dimensional devices requiring low voltages with low power consumption for which continuous downscaling of device dimension and supply voltage is mandatory. Reduced dimension results in higher package density as well as reduced gate capacitances, thereby increasing the operating speed of the devices. Similarly, power consumption gets reduced by a reduction in supply voltage. However, when the channel length of conventional MOSFET is scaled down to around 50 nm with a proportional reduction of supply voltage down to 0.5V, overcoming the OFF state leakage current due to thermionic emission becomes a daunting challenge. Gradual increment in the voltage applied to the gate terminal of a MOSFET lowers the potential barrier in the channel enabling more carriers to move from the source to the

drain region to contribute to the enhanced drain current. Dependence on thermionic emission is the primary cause for higher OFF state current due to sub-threshold conduction resulting in a higher value of sub-threshold slope. Thus, gaining a clear insight on sub-threshold slope (SS) becomes crucial. Sub-threshold slope of a MOSFET is defined to be the change in gate voltage required to increase the drain current by a factor of 10 [2.113]. Mathematically it can be expressed as:

$$SS = \left(\frac{d(\log_{10} I_D)}{dV_G} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{depletion}}{C_{oxide}} \right) \quad (2.13)$$

Where $C_{depletion}$ is the capacitance of the depletion region and C_{oxide} is the capacitance of the gate oxide. It can be well understood from the above equation that the lowest value of sub-threshold slope possible for a MOSFET at room temperature is 2.3kT/q which amounts to be 60 mV/decade i.e. changing the gate voltage by 60 mV results in the increase in drain current by a factor of 10. Thus, in order to achieve Ion/Ioff ratio of 10^6, the required gate voltage is about 6x60mV=0.36V. This fundamental limitation poses the greatest difficulty for supply voltage down scaling as predicted by contemporary scaling trend, threatening the viability of MOSFETs in near future.

Tunneling Field Effect Transistors (TFETs) provide a solution to this fundamental limitation of MOSFETs. The motivation to adopt TFETs instead of conventional MOSFETs has been the urge to realize devices below the thermal limit of 60 mV/decade. Unlike thermionic emission of carriers in MOSFETs, current conduction mechanism in TFETs is dependent on band-to-band tunneling of carriers from source side valence band to the channel conduction band through proper adjustment of the source-channel potential barrier. In OFF state, when no gate voltage is applied, the potential barrier is very wide which eliminates the chances of carrier tunneling from source to the channel resulting in very low OFF state current in TFETs. In addition to this fundamental advantage, TFETs are inherently more immune to short channel effects than MOSFETs. This host of advantages along with the strong structural similarity with conventional MOSFETs allows the use of same fabrication process making TFET a suitable alternative to MOSFETs for future low power low voltage nano devices.

2.2.6.1 A brief history of TFETs:

The history of Tunnel Field Effect Transistors dates back to 1957 when the phenomenon of band-to-band tunneling was first invented by L.Esaki [2.114]. Based on Esaki's tunneling, a gated p-i-n diode was first proposed in 1978 [2.115]. The working principle of TFET transistors is mainly based on the basic structure of a gated p-i-n diode, which has to be operated in reverse-bias mode by applying suitable voltage to the drain terminal keeping the source connected to ground. Motivated by the growing popularity of tunneling based devices, a silicon based BTBT transistor operating on the principle of band to band tunneling was first proposed in 1995 by the researcher duo- Reddick and Amaratunga [2.116]. A simple reverse biased p-i-n diode was fabricated by them on bulk silicon. The

basic concept of the fabricated structure was to modulate the tunneling current by suitably modulating the tunneling barrier width. Thus device current was controlled by controlling the tunneling of carriers instead of thermionic emission of carriers in conventional MOSFETs. Later, Eisele et al. [2.117] in 2000 experimentally proved that TFETs can possibly be a suitable alternative to conventional MOSFETs for continuing the unhindered progress in future electronics industry. The possibility to achieve sub-threshold swing below MOSFET's thermal limit of 60 mV/dec was first demonstrated by Joerg Appenzeller and his research team at IBM. In 2004, a carbon nanotube channel tunnel transistor was reported to be successfully fabricated by them exhibiting a subthreshold swing of just 40 mV/dec [2.118]. These results from a carbon nanotube based tunnel transistor proved to be path-breaking and opened up a new era in semiconductor research by instigating the concept of using tunneling mechanism in silicon devices. It is more advantageous for the researchers to implement the tunneling concept in silicon based transistors because a mature silicon technology provides a straight path to the industry.

2.2.6.2 Basics of the Tunnel FETs

Tunneling Field Effect Transistors (TFET) present a new area of low dimensional semiconductor devices where the basic operating principle is based on quantum band-to-band tunneling of carriers through a barrier. This quantum barrier is modulated by applying proper biasing to the device so as to allow or block the flow of carrier resulting in device current. Basic structure of Tunnel FET is similar to p-i-n diode where an intrinsic layer is sandwiched between a heavily doped p-region and a heavily doped n region. A gate electrode is formed above the intrinsic region. Application of proper bias on the gate electrode controls the flow of current through the device. Zener tunneling mechanism, also called the inter-band tunneling or band-to-band tunnelling is the basic carrier transport concept of TFETs. Similar to conventional MOSFETs, TFETs also consist of three terminals: source, gate and drain. But the bulk/substrate contact (i.e. is the fourth contact) is not available in TFET. Unlike MOSFETs, the source and the drain region in TFETs are oppositely doped and the channel is considered to be either intrinsic or lightly doped with n-type or p-type impurities. The general configuration of the n channel TFET is shown in Fig. 2.42. indicating the drain, gate and source regions. If the gate to source voltage increases, electrons tunnel from the source side valence band to the channel conduction band (as shown by red arrow). On reaching channel, the tunneled electrons finally reach the drain end depending on applied drain bias (as indicated by hollow arrow).

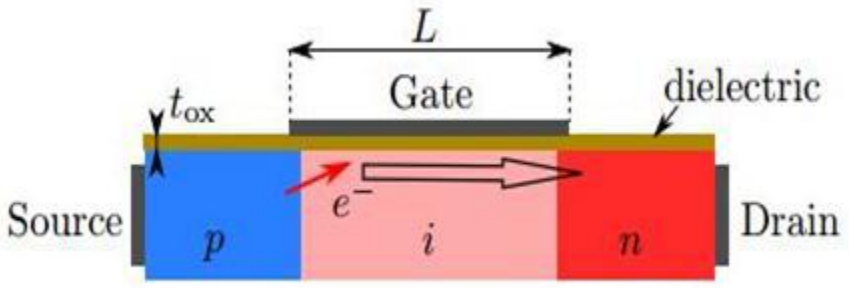

Fig. 2.42: An n-channel TFET

The achievable sub threshold slope of less than 60mV/decade in TFET empowers the designers to scale down the supply voltage while maintaining a small OFF state leakage current. The low off state current results in reduced static power dissipation and reduced supply voltage requirement reduces the active power dissipation in TFETs making TFET an alternative device suited for low power applications [2.119].

2.2.6.3 Physics of Tunnel FET- the BTBT theory

Theory of quantum mechanics forms the underlying device physics behind the Tunnel FETs. Unlike classical mechanics, quantum mechanics considers that although the carriers might not possess sufficient energy to overcome the barrier height, there is always a finite probability of carriers tunneling through that barrier instead of climbing it. In Band-to-Band Tunneling (BTBT), electron makes band transitions by moving up from the valence band to the conduction band or moving down from the conduction band to the valence band through the forbidden energy gap depending on the finite probability of the alignment of the filled and the empty energy states on the either sides. Fig. 2.43 presents a clear pictorial illustration of band-to-band tunneling. From Fig. 2.43 (a), it can be seen that the carrier present in the valence band of the p+ region encounters a barrier in its path. Though it does not have enough energy to climb the barrier and move forward, according to quantum mechanics, there is a finite probability that the carrier from the valence band of the p+ region may tunnel to the conduction band of the n+ region, provided that an empty conduction band state is aligned to the filled valence band state. The barrier seen by the carrier in its path is approximated to be a triangular potential barrier which is shown in Fig. 2.43 (b), and the probability of tunneling of the carrier is given by Wentzel-Kramers-Brillouin (WKB) approximation [2.120].

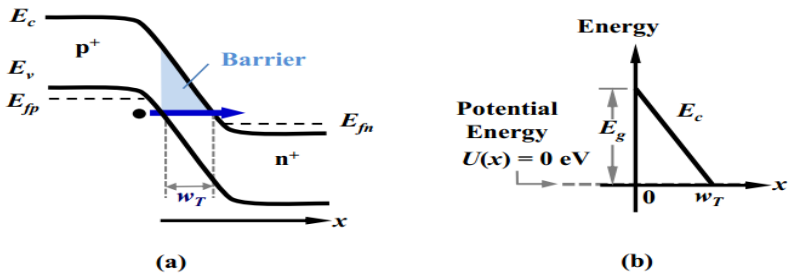

Fig. 2.43: (a) energy band diagram of reverse biased p+/n+ diode depicting BTBT mechanism. (b) triangular approximation of the barrier

For the triangular barrier the tunneling probability is given by [2.120]:

$$T_{tunnel} = e^{-2\int_0^{W_T} \frac{\sqrt{2m_r^*[U(x)-E_C]}}{\hbar}dx} \approx e^{\frac{4\sqrt{2m_r^*}E_g^{3/2}}{3q\hbar\xi}} \tag{2.14}$$

Where,

the symbols m_r^*, W_T , ħ , Eg and U(x) represent the reduced effective mass of the carrier, the tunneling width, reduced Plank's constant, energy band gap of the material and potential energy respectively. The smaller the tunneling width, the higher is the tunneling probability due to band gap and the effective mass.

The carrier generation rate in band-to-band tunneling phenomenon can be expressed as [2.120]:

$$G_{BTBT} \propto \int_{E_V}^{E_C} [f_V(E) - f_C(E)] g_V(E) g_C(E) T_{tunnel} dE \tag{2.15}$$

Where fc and fv represent conduction band and valence band Fermi Dirac distribution functions respectively, while gc and gv represent conduction band and valence band density of states respectively. Combining above two equations, it can be said that abrupt junctions are required to achieve higher tunneling rate. Fig. 2.44 explains the dependence of tunneling on applied gate bias. The dependence of surface potential energy on the gate-to-source bias can be mathematically given as:

$$\varphi_S \approx -q(V_{GS} - V_{FB}) \tag{2.16}$$

Where, V_{FB} is the flat band voltage. When $V_{GS}=V_{FB}$, bands are flat and there is no band bending. Thus no tunneling occurs under thermal equilibrium and the device is said to be in OFF state. On increasing V_{GS}, the surface potential becomes more than the band gap of the material reducing the tunneling path between the valence and the conduction band at the source-channel junction. This effectively increases the rate of carrier tunneling at source-channel junction driving the device to ON state.

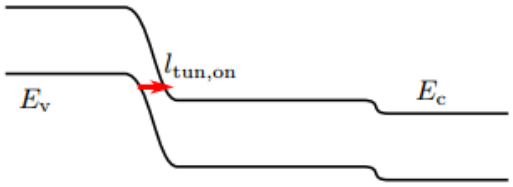

Fig. 2.44: Reduction in the tunnel path in the ON state of TFET

Tunneling rate is also dependent on the type of the semiconductor i.e. the direct band gap semiconductor or indirect band gap semiconductor (illustrated in Fig. 2.45) as the expression of tunneling rate itself has band gap as a parameter. In direct band gap semiconductors like Galium Arsenide (GaAs), Indium Arsenide (InAs) etc. the energy required by the electrons to tunnel from the valence band into the conduction band is equal to the band gap of the material, whereas, in indirect band gap semiconductors like silicon (Si), germanium (Ge) etc. transition from valence band to conduction band involves phonon assisted tunneling due to difference in momentum between the conduction band minima and valence band maxima. Thus, tunneling in indirect band gap semiconductors is far more difficult compared to tunneling in direct band gap semiconductors. Thus, material engineering is essential to design devices depending on band to band tunneling mechanism.

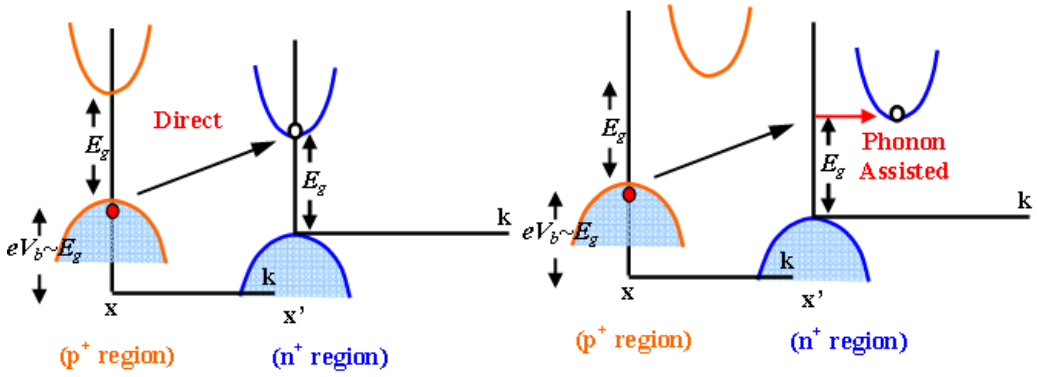

Fig. 2.45: (a) The direct band gap semiconductor (b) indirect band gap semiconductor consists of phonon assisted tunneling

2.2.6.4 Tunnel FET structure and Operation

The basic construction of TFET is similar to a MOSFET excepting that both source and drain terminals of a TFET are doped with impurities of opposite type. The heart of a simple n-type tunneling field effect transistor consists of a p-i-n diode (p-type source, intrinsic channel, n-type drain) as shown in Fig. 2.46(a). The source and drain regions are highly doped (p+ source and n+ drain) in order to achieve abrupt junctions to aid carrier tunneling. Applied bias on the gate terminal placed above the intrinsic area controls the electrostatic potential profile of the said intrinsic channel. The terminals of the TFET are named in accordance to the MOSFET terminology due to their similarity in basic structure. As the n-TFET shown is basically a reverse biased gated p-i-n diode, reverse bias voltage is required to turn on the device. Keeping the source terminal connected to ground potential, application of a positive drain voltage and a positive gate voltage (more than specified threshold voltage) switches ON a conventional n-channel MOS. Maintaining this convention, the n+ region of the p-i-n diode which is connected to positive voltage in order to reverse bias the p-i-n diode is termed as drain region while the p+ region is termed as the source region of the n-type TFET shown in Fig. 2.46(a). The doping type of the source and the drain region is opposite in p-type Tunnel FET i.e. pTFET has p+ drain and n+ source regions as shown in Fig. 2.46(b).

The basic working principle of TFET is band-to-band tunneling of carriers from source side valence to channel conduction band and subsequent drift of the tunneled carriers towards the drain under the influence of drain electric field. TFET operation can be explained using band diagram under various biasing conditions.

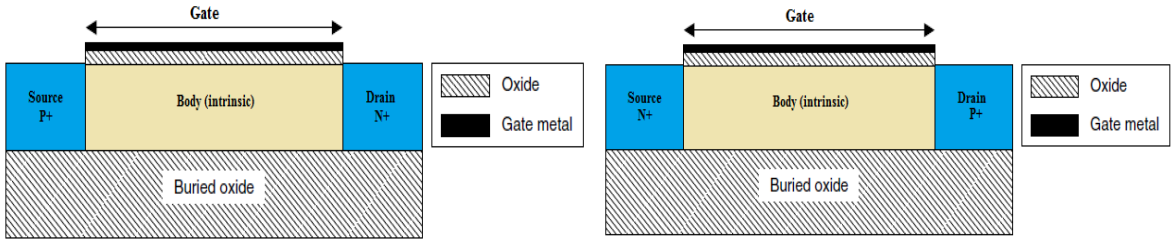

Fig. 2.46 (a): A simple gated n channel Tunnel FET structure; Fig. 2.46 (b): A simple gated p channel Tunnel FET structure

(a) Thermal equilibrium: Fig. 2.47 (a) shows the band diagram of a simple n-channel TFET under thermal equilibrium i.e. when no external bias is applied (V_G = V_S = V_D = 0). Two depletion regions exist at the source-channel and drain-channel junctions.

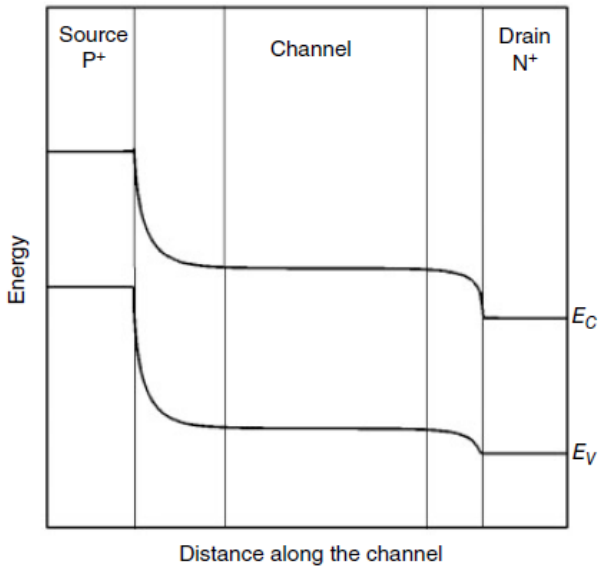

Fig. 2.47 (a) Band diagram along the surface of an n-channel TFET at thermal equilibrium [2.121]

(b) OFF state: Fig. 2.47 (b) illustrates the band diagram of a simple n-channel TFET in OFF state when the applied gate-to-source voltage is zero and applied drain-to-source voltage is positive i.e. V_{GS} =0 and V_{DS} = +*ve*. Under such biasing condition, no empty states in the conduction band of the channel is aligned with the filled states in the source valence band, thereby eliminating any chance of electron tunneling from source to channel. The source being p+ for an n-channel TFET, very few number of electrons are present in the conduction band of the source which can be injected into the channel resulting in negligible OFF state current. This is in sharp contrast with MOSFET scenario where the source is also n-type having plenty of free electrons in the conduction band which can be injected into the channel through thermionic emission over the source-channel potential barrier leading to higher OFF current. It must be noted that in OFF state, if any carrier is present in the conduction band of the channel, there is a finite tendency of these carriers to drift towards the drain on increasing the drain bias (due to barrier lowering as evident from Fig. 2.47(b)) generating a low OFF state current [2.121].

(c) ON state: If the device is intended to operate in ON state, then it must conduct some current which is possible if some charge carriers are injected from the source into the channel. Now, in case of n-channel TFET, as the source is p type, the conduction band has negligible number of free electron which can move into the channel. Thus, for steady flow of carriers from source to channel, the electrons of source side valence band must move into the channel conduction band only if some empty states are available at the channel conduction band placed opposite to filled states of source valence band as depicted in Fig. 2.47(c). This

requires band bending and modulation of the source-channel potential barrier to be done by applying suitable positive bias at the gate terminal.

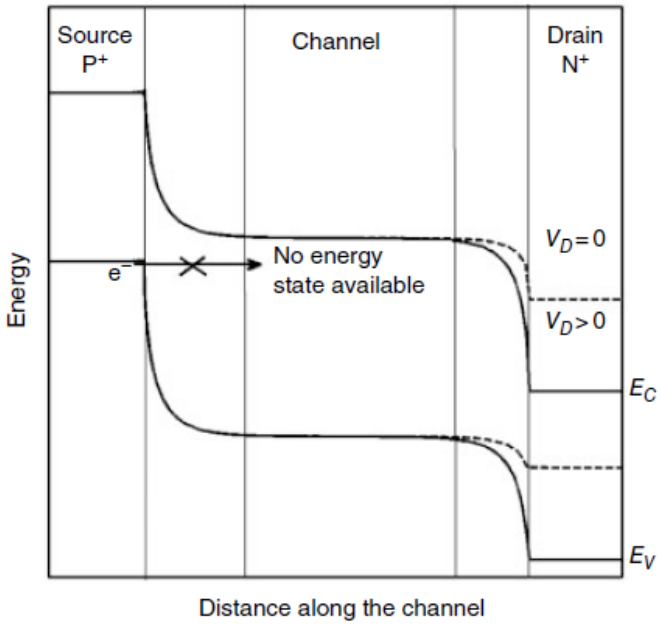

Fig. 2.47 (b) Band diagram along the surface of an n-channel TFET in OFF state [2.121]

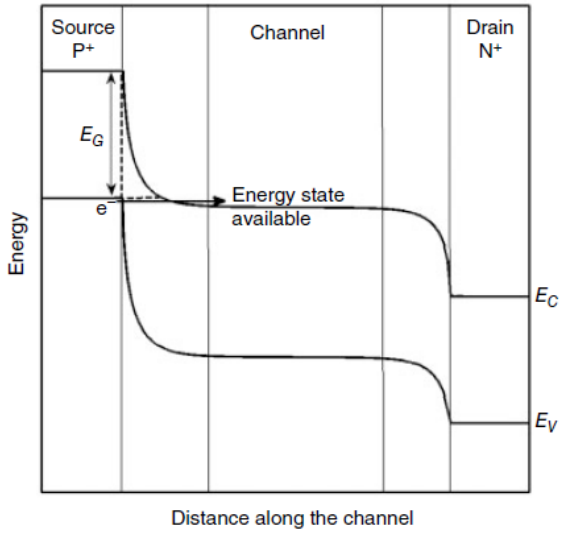

Fig. 2.47 (c) Band diagram along the surface of an n-channel TFET in the beginning of ON state [2.121]

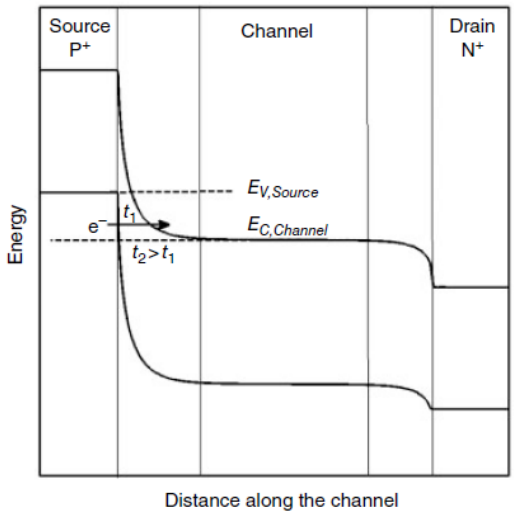

Fig. 2.47 (d) Band diagram along the surface of an n-channel TFET in deep ON state [2.121]

The gate-to-source voltage is gradually increased and the channel energy band continues to bend further. At a certain value of gate voltage, the source side valence band gets aligned with channel conduction band as depicted in Fig. 2.47(c). This band alignment places the empty states of the channel conduction band just opposite to the filled states of the source side valence band so that the electrons from filled energy states of source valence band may easily tunnel into the empty energy states in the channel conduction band through the potential barrier (approximately triangular in nature as shown by dashed lines in Fig. 2.47(c)) formed by the silicon band gap of Eg. The gate voltage at which the bands just get aligned, mark the onset of ON state of the TFET device. If the gate voltage is increased beyond this value, the channel energy bands bend down further so that more free electrons from energy states between valence band edge of source side ($E_{v,source}$) and conduction band edge of channel ($E_{c,channel}$) may tunnel into the channel conduction band (as shown in Fig. 2.47(d)) resulting in steady increase in device ON state current. Moreover, the length of the tunneling barrier i.e. tunneling length decreases on increasing gate voltage resulting in enhanced rate of carrier tunneling which in turn increases overall current. This exponential dependence of device ON current on barrier width is graphically shown in Fig. 2.48. Fig. 2.48 (a) depicts the variation of the barrier width with applied gate voltages considering different gate oxide permittivities. Fig. 2.48 (b) shows the exponential dependence of device current on barrier width.

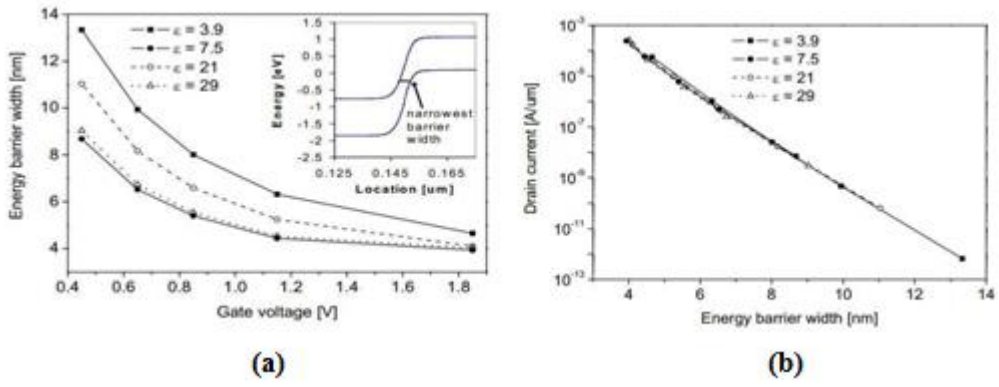

Fig. 2.48: (a) the variation of energy barrier width with gate voltage (b) The drain current dependence on the tunneling width

(d) Ambipolar behaviour: Despite of the advantage of achieving sub-threshold slope below the thermal limit of 60mV/decade of MOSFETs, TFETs suffer from a basic problem of higher OFF state current than MOSFETs. This is attributed mainly to the inevitable ambipolar conduction in TFETs where a negative gate voltage also results in effective device current. Figs. 2.49 (a-d) illustrates this ambipolar behaviour in TFETs.

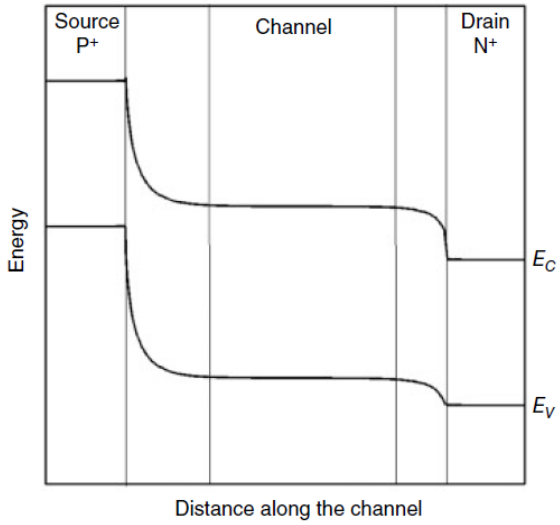

Fig. 2.49 (a) Band diagram along the surface of an n-channel TFET at V_{GS}=0 and V_{DS}>0 [2.121]

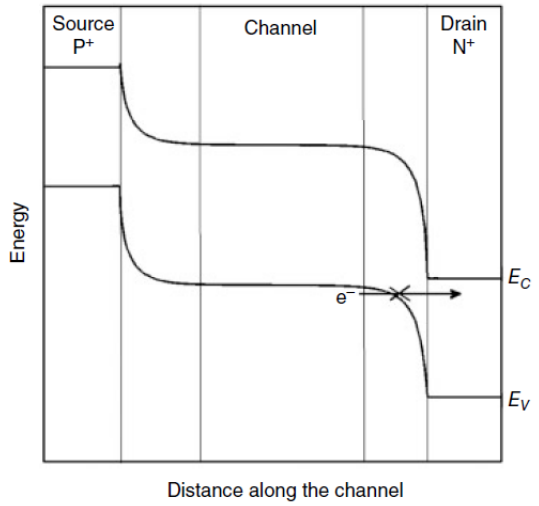

Fig. 2.49 (b) Band diagram along the surface of an n-channel TFET at V_{GS}<0 and V_{DS}>0 [2.121]

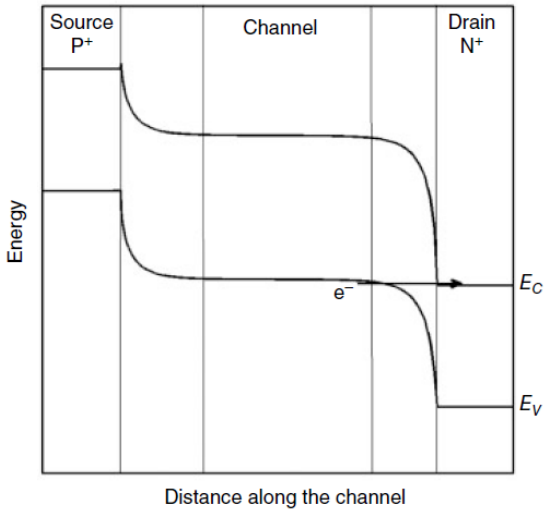

Fig. 2.49 (c) Band diagram along the surface of an n-channel TFET at V_{GS}<0 and V_{DS}>0 such that channel valence band just gets aligned with drain conduction band [2.121]

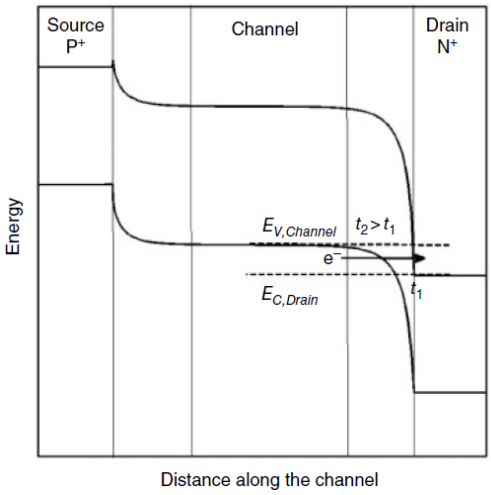

Fig. 2.49 (d) Band diagram along the surface of an n-channel TFET for V_{DS}>0 and more negative V_{GS} such that channel valence band just gets aligned with drain conduction band [2.121]

At first, when V_{GS}=0 (refer to Fig.2.49(a)), there is no possibility of electron tunneling either from he source valence band to channel conduction band or from channel valence band to drain conduction band. This indicates that even if positive voltage is applied to the drain terminal, there is no resulting tunneling current as long as the applied gate bias is zero. Now, when a negative voltage is applied to the gate (provided drain is given a positive bias), energy bands in the channel start to move up with respect to the energy bands of the drain as depicted in Fig. 2.49 (b). On increasing the negative gate voltage, a point comes when the valence band of the channel gets aligned with the conduction band of the drain (refer to Fig. 2.49(c)) allowing electrons to tunnel from the filled energy states in channel valence band to the vacant energy states in the drain conduction band. If the gate voltage is made more and more negative, the tunneling path at the channel-drain junction gets reduced along with more number of filled energy states in the channel valence band being placed opposite to vacant energy states in the conduction band of the drain (refer to Fig. 2.49(d)) resulting in an enhanced rate of electron tunneling from channel to drain, which in turn increases the effective device current. It must be carefully noted that the direction of tunneling of electrons is from left to right for both positive and negative gate voltages resulting in current of same polarity in both cases.

2.2.6.5. Device characteristics:

2.2.6.5.1. ***Transfer characteristics:*** Variation of drain current (in logarithmic scale) with gate to source voltage of an n-channel TFET is shown in Fig. 2.50 at a constant drain voltage illustrating

different regions of operation i.e. OFF state (due to no carrier tunneling), ON state (due to source-channel tunneling) and ambipolar state (due to drain-channel tunneling) as discussed previously.

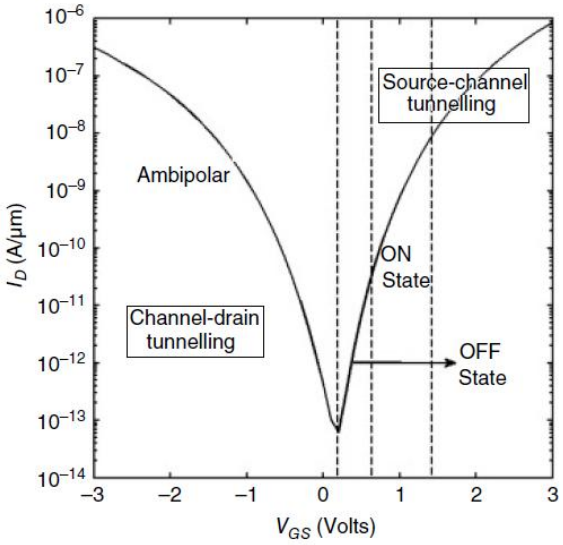

Fig. 2.50. Transfer characteristics of n-channel TFET [2.121]

2.2.6.5.2. ***Output characteristics:*** Variation of drain current with respect to drain-to-source voltage of an n-channel TFET is shown in Fig. 2.51 considering different gate biases.

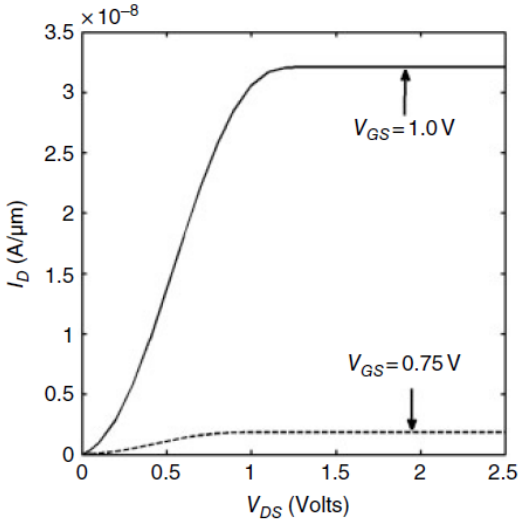

Fig. 2.51. Drain characteristics of n-channel TFET [2.121]

2.2.6.6. Analytical modeling approach of BTBT mechanism

Band to band tunneling theory is an age old concept proposed by Esaki in 1958 for the small band gap germanium (Ge) diodes [2.114].He observed that the electrons travel through the forbidden gap

and can move from one band to another band on application of suitable bias. The thermal limits of 60mV/decade on the sub threshold slope for conventional MOSFETs can be eliminated by using the technique of band-to-band tunneling in TFETs. However, current conduction by tunneling of carriers result in a reduced ON state current in TFET compared to MOSFET. This necessitates a careful study of the tunneling mechanism. Out of many popular models, the Kane's model is most commonly used to model the interband tunneling in TFETs [2.122].

2.2.6.7 Model development

Understanding the mechanism of interband tunneling requires immense knowledge of quantum mechanics. In order to formulate exact mathematical expression of tunneling probability, the exact wave function during band-to-band transition must be known. As explained in the earlier section that tunneling in TFETs occur from the source valence band to the channel conduction band through the forbidden energy gap. Thus, in order to calculate tunneling probability, understanding of the properties of the wave function in forbidden gap is very crucial. The wave functions in the forbidden gap assume the form of a wave vector which is an imaginary function with decaying value during its forward journey. Calculation of this imaginary wave vector involves consideration of the principle of conservation of energy. At the end of the transmission, the final energy of the tunneled electron in the conduction band is equal to the sum of its initial energy in the valence band and the energy gained by the acceleration due to electric field, provided there is no additional energy loss. This conservation of energy can be expressed as: $\left(E_V - \frac{\hbar^2 k^2}{2m_v^*}\right) + qFx = E_C - \frac{\hbar^2 k^2}{2m_c^*}$ (2.17)

where, F, m_v* and m_c* represent the electric field and effective masses of the electrons in valence band and conduction band respectively. This equation does not incorporate any scattering loss related terms assuming conservation of momentum, which makes it inaccurate for indirect band gap semiconductors as phonon interactions associated with tunneling are neglected for computational brevity. The energy conservation equation also assumes that electric field is constant throughout. However, in case of actual interband transition, electric field is not really constant. So, average electric field is usually considered for calculating the tunnel path. The wave vector in forbidden gap can be written as:

$$k = \frac{i}{\hbar}\sqrt{2m_r(E_g - qFx)} \quad (2.18)$$

Where Eg is the band gap and m_r is the effective mass given as $\frac{1}{m_r} = \frac{1}{m_v^*} + \frac{1}{m_c^*}$

As long as total energy is conserved, Eq. 2.18 will give correct result. However, if the value of wave vector is studied throughout the tunneling phenomenon, Eq. 2.18 will prove to be inaccurate. The wave vector function is assumed to lie in the forbidden gap and is purely imaginary. So at the two extreme points of tunneling path, i.e. at the starting and end points, the wave function must assume a value of zero so as to provide even change in wave vector. But practically if we consider average electric field throughout the tunneling process, the tunnel wave vector is found to have a large value at the starting point of tunneling path and becomes zero at the end point resulting in an abrupt jump in the value of imaginary wave vector which seems to be impractical. Thus, to avoid this impractical abrupt jump and to ensure a smooth transition in the value of wave vector along the tunneling path, the shape of the barrier is considered to be parabolic and can be written as:

$$k = i\frac{\sqrt{2m_r}}{\hbar}\sqrt{qFx\left(1-\frac{qFx}{E_g}\right)} \tag{2.19}$$

So far it has been assumed that the effective masses of electrons in conduction band and valence bands are different and together, they result in a reduced effective mass m_r as given by $\frac{1}{m_r}=\frac{1}{m_v^*}+\frac{1}{m_c^*}$ .This simplification is valid only if the valence band and conduction band effective masses are approximately equal. If the said masses differ (i.e. if $m_v^* \neq m_c^*$ as in InAs), modeling will be inaccurate. It is seen that the tunneling electron assumes the effective mass of valence band electron near the valence band edge while that of conduction band electrons near the conduction band edge. In order to take this into account, the interpolated expression can be written as:

$$\frac{\hbar^2 k_x^2}{2m_v^*}-\left(\frac{\hbar^2 k_x^2}{2m_v^*}-\frac{\hbar^2 k_x^2}{2m_c^*}\right)\frac{E}{E_g}+E_{par}=-E\left(1-\frac{E}{E_g}\right) \tag{2.20}$$

The direction of tunneling is considered to be along x axis where the transverse energy is assumed to be constant. E is the electric field due to the band bending. From this, the modified expression for the smooth and accurate wave vector in the forbidden gap can be calculated as:

$$k_x = i\frac{\sqrt{2m_v^*}}{\hbar}\sqrt{\frac{E\left(1-\frac{E}{E_g}\right)+E_{par}}{\left(1-\left(1-\frac{m_v^*}{m_c^*}\right)\frac{E}{E_g}\right)}} \tag{2.21}$$

Fig. 2.52 describes the said imaginary wave vector in the forbidden energy gap considering various electron effective masses. It can be seen that the wave vector reaches maximum value at the centre

of energy gap when the effective masses of valence band and conduction band electrons are considered to be approximately equal. The wave vector maxima shifts towards the band having smaller effective mass if effective mass transition is considered from valence to conduction bands.

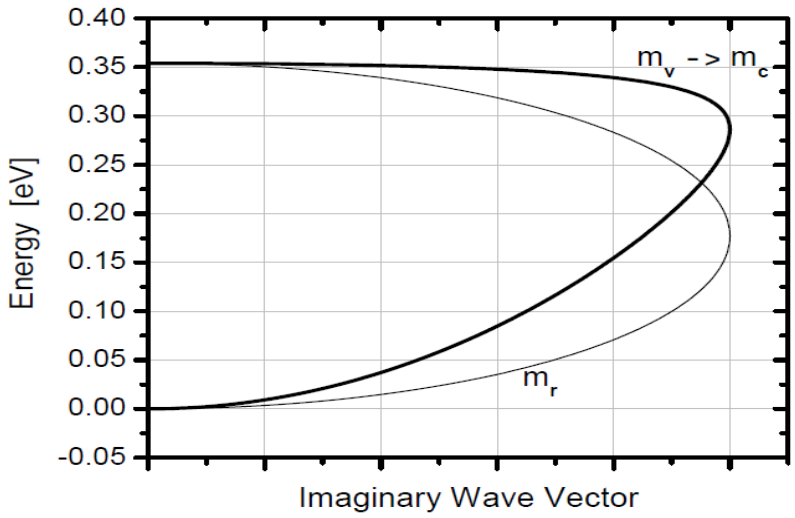

Fig. 2.52: Transition of the wave vector in the energy gap, if we consider the different masses

Having computed the expression of wave vector, the tunneling probability can be calculated using WKB (Wentzel-Kramers-Brillouin) approximation as:

$$T \simeq \exp(2i\int_{x_1}^{x_2} k_x dx) \tag{2.22}$$

where x_1 and x_2 are the starting and the ending points of interband tunneling. The distance between these two points gives the tunneling window over which carriers may tunnel from one region to another. Substituting the expression of wave vector into Eq. 2.26, the tunneling probability can be expressed in terms of effective wave vector as:

$$T \cong \exp\left(-2\int_{x_1}^{x_2} \frac{\sqrt{2m_v^*}}{\hbar} \sqrt{\frac{E\left(1-\frac{E}{E_g}\right)+E_{par}}{\left(1-\left(1-\frac{m_v^*}{m_c^*}\right)\frac{E}{E_g}\right)}}\, dx\right) \tag{2.23}$$

The resultant tunneling current is thus a direct function of band-to-band generation rate and can be written according to Kane's model [2.122] as follows:

$$I_{BTBT} = q\iiint \frac{2}{h^3}|T|^2 v_x dv \tag{2.24}$$

Substituting the expression of tunneling probability in the above expression, the resultant expression of tunneling current can be written as:

$$I_{BTBT} \cong \frac{4\pi q m_v^*}{h^3}(qV_a)\int \exp\left(-2\int_0^d \frac{\sqrt{2m_v^*}}{\hbar}\sqrt{\frac{(qFx)\left(1-\frac{qFx}{E_g}\right)}{\left(1-\left(1-\frac{m_v^*}{m_c^*}\right)\frac{qFx}{E_g}\right)}}dx\right)E_{par} \tag{2.25}$$

Thus, the entire chapter has presented sufficient insight to the basic nano devices starting from the basic MOS transistor. The operation of MOSFET has been illustrated in brief with special consideration of the MOS operations in nano regime where the dimension of a single transistor is in sub 100 nm range. The performance of such nano scale devices is severely degraded due to various short channel effects discussed throughout the chapter. In order to alleviate such performance degradation, numerous alternative nano devices are being currently studied by different groups of researchers which have been discussed briefly in this chapter to give an idea about the ongoing developments in the field of semiconductor devices.

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Chapter 3

Dual Material Gate Fully Depleted SOI/SON MOSFET with strained silicon channel for subdued SCEs

CHAPTER III

3.1. Overview and recent research trend

The modern era of VLSI/ULSI industry is being continuously driven by the need of ultra low dimensional low power consuming high speed semiconductor devices for the sake of gaining tremendous impetus on the packaging density of integrated circuits coupled with the multiple functionalities achieved along with the operating speed. This trend of the industry has primarily followed the scaling pattern predicted by Moore's law where the number of transistors doubles every 24 months. This rapid scaling trend reduces the device to quasi-nanometer level which in turn allows the integration of a huge number of transistors on a single chip resulting in the fabrication of a more complex system on a single chip, thereby significantly reducing the chip area required and power consumption per function and increasing the speed of operation. This aggressive miniaturization of device dimension, however, is restricted to some fundamental limitations specified by the International Technology Roadmap for Semiconductors (ITRS) [3.1]. Thus, the major challenge in the research domain of semiconductor devices is to continue the scaling trend predicted by Moore without sacrificing the performance efficiency of the scaled devices, which can only be feasible through a combination of miniaturization, innovation of improvised device structures along with semiconductor material improvement. However, the ongoing trend of device dimension miniaturization into sub-nano meter regime is associated with some inevitable issues of gate depletion, lack of reliability and most importantly, the major Short Channel effects (SCEs) such as

Drain-Induced Barrier Lowering (DIBL), Hot Carrier Effect (HCE), Sub threshold conduction, junction leakages etc [3.2]. These major limitations related to device down scaling can be alleviated effectively by adopting some non-conventional device structures which are being widely studied in recent times as discussed in details in the previous chapter. Among many of the widely studied device structures, Fully Depleted Silicon-on-Insulator (FDSOI) structure has gained significant research spotlight and can be considered as the most suitable alternative to conventional bulk MOSFETs due to their superior device performance. The SOI structure, by dint of having a buried oxide (BOX) layer of silicon-di-oxide underneath the channel region, exhibits appreciably improvised features of having significantly reduced SCEs, improved sub-threshold characteristics, reduced parasitic junction capacitances resulting in lower propagation delay, ideal device isolation due to reduced coupling effect, high radiation tolerance, reduced layout area, reduced junction leakage currents and latch-up prevention. In spite of providing so much improvement over the conventional bulk MOS, SOI structure, however, is not completely immune from the unavoidable short channel effects in nano regime [3.3-3.5]. Some the unsolved issues associated with ultra scaled SOI devices are threshold voltage roll-off, dynamic floating body effects, parasitic bipolar effects, increased off-current, fabrication difficulty of ultra thin films along with self heating effect due to poor thermal conductivity of underlying BOX layer which severely impacts the device performance and reliability [3.4]. Thus, the shortcomings associated with severely down scaled SOI devices can be taken care of by adopting an improvised SOI structure incorporating the concept of buried insulator engineering where a different dielectric material is used in the underlying BOX layer of the SOI MOSFET, which in effect reduces the coupling effect of both vertical and lateral electric fields in the BOX region, resulting in an enhanced device performance [3.6]. A special case of buried insulator engineering uses air (having relative permittivity of unity) in the BOX layer resulting in a well-known structure known as Silicon-On-Nothing (SON) MOSFET [3.7]. The relative permittivity of air being unity (lowest than any other BOX dielectric material) minimizes the source/drain to channel and channel-to-substrate parasitic capacitances [3.8], which in turn results in higher circuit speed [3.9] achievable with SON devices as well as providing the highest isolation of active channel region. In addition to retaining all the advantages of existing SOI structure, SON structure improves radiation immunity in extreme environment, reduces power consumption, enhances further scaling capability, shows low noise, develops higher short channel immunity, offers faster switching action and reduces cost. Although SON devices exhibit manifold performance advantages over their bulk and SOI counterparts, Moore's aggressive scaling trend reduces the channel dimension of contemporary devices to such a range, where short channel effects become inevitable even in SON. The massively scaled device dimension significantly reduces the sole gate control over the channel which subsequently impacts the drain current due to higher charge-sharing from the drain/source regions, resulting in sub-threshold slope degradation and enhanced drain off-current. Researchers in

semiconductor domain have been continuously searching for novel methods to mitigate SCEs. Gate material engineering and channel material band gap engineering can be two possible avenues of research in order to explore possible improvisations on existing device structures.

Channel material band gap engineering explores and modifies the properties of the device channel material, which in turn has a positive impact on device current characteristics. Band gap engineering can be implemented by adopting the age old concept of using silicon-germanium (SiGe) and silicon-strained epitaxial layer as channel. The strain induced in the channel can be controlled by adjusting the Ge mole fraction (X) [3.10-3.12]. If a thin silicon thin film is pseudomorphically deposited on a relaxed $Si_{1-x}Ge_x$ substrate, biaxial tension develops in the grown thin silicon film. The developed biaxial tensile strain affects the band structures of the deposited silicon film, decreases the effective bandgap and increases the electron affinity along with a net decrease in the effective masses of current carriers [3.13-3.16]. The reduction in effective masses in turn results in an increase in carrier mobility thereby significantly improving the current behavior of the resulting device [3.17].

Thus, strained SOI and SON MOSFETs combine the carrier transport advantages of strained-Si with reduced parasitic capacitance and improved scalability of thin-film SOI. Some of the major advantages associated with a thin-body fully depleted SOI are steep sub threshold slope, low junction leakage current, maximized channel mobility, and reduced threshold-voltage fluctuation due to low impurity concentration [3.18].

On the other hand, the concept of gate material engineering is based on the idea of modifying the vertical electric field in the channel region by using dual or triple materials with different work functions side by side as a single gate electrode, thereby adjusting the overall field and consequently improving performance. The Dual Material Gate system was first proposed by Long et. al. [3.19] where two different metals having different workfunctions are amalgamated side by side forming a single gate electrode. The discontinuity in workfunction value at the junction of two metals introduces a step in the surface potential profile which screens the source side potential barrier from any random variation in drain bias, with an aim to mitigate the DIBL induced performance degradation.

This chapter of the thesis presents a detailed analytical two dimensional Poisson's equation based surface potential and device current behavior of a Dual Material Gate SOI/SON MOSFET with strained channel. The strained SOI/SON structure exhibits gate material engineering where two gate metals M_A and M_B of different work functions ϕ_A and ϕ_B are placed together side by side forming a single gate electrode and provide simultaneous increase in trans-conductance and

suppressed SCEs due to a step in the surface potential profile which practically screens the channel region under the gate material on the source side (M_A) from variations in the drain potential, giving effective protection from DIBL [3.18, 3.19]. Initially, the variation of carrier mobility in the strained silicon channel has been studied in details against mole fraction variation, impurity concentration and transverse electric field. Then a two dimensional analytical model of the surface potential has been presented and the threshold voltage has been evaluated from the surface potential minimum and subsequently various drain characteristics are studied.

3.2. Analytical Modeling

A schematic cross-sectional view of the proposed strained fully depleted Dual Material Gate Silicon on Nothing (FD DMG SON) MOSFET is shown in Fig. 3.1 with gate metals M_A and M_B of lengths L1 and L2, respectively. Here t_{ox}, $t_{box/air}$ and t_{Si} are the thickness of the front gate oxide, buried layer and strained silicon channel respectively of our proposed model.

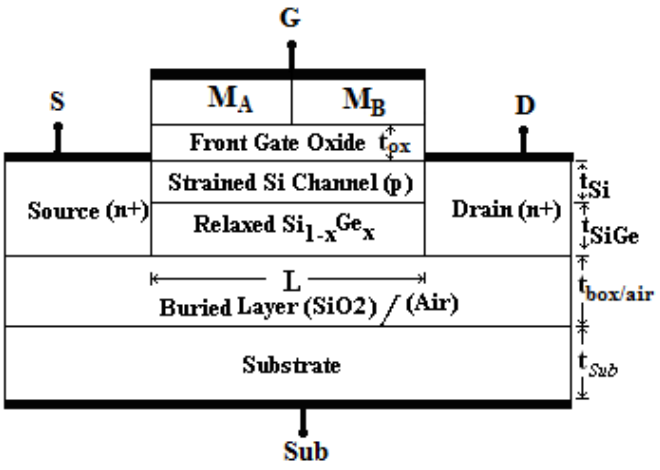

Figure3.1. Cross-sectional view of a DMG FD SOI/SON MOSFET incorporating strain in the channel

3.2.1. Effects of strain on Band parameters

In this section, the effect of strain incorporation in the silicon channel has been discussed in brief. Whenever strain gets incorporated into the silicon channel, there is a considerable increase in electron affinity along with a decrease in carrier effective masses and separation between conduction and valence band edges. Following references [3.20, 3.21], the strain induced modifications of different band parameters and device parameters can be listed as:

i. Strain induced reduction in bandgap energy, $(\Delta E_g)_{st\text{-}Si}$= 0.4X,

ii. Strain induced lowering of conduction band edge, $(\Delta E_c)_{st\text{-}Si}$=0.57X

iii. Strain modified carrier effective mass= $V_T \ln\left(m^*_{h-Si} / m^*_{h-st-Si}\right)^{1.5} \approx 0.075X$

iv. Strain modified flat band voltage, $V_{FB} \approx \left(\phi_{meff} - \varphi_{Si}\right) - 1/q^*\left(0.57X + 0.4X\right) + 0.075X$ and

v. Strain modified built in potential, $V_{bi-st-Si} \approx V_{bi-Si} - 0.4X/q - 0.075X$

where X is the Ge mole fraction in relaxed SiGe, V_T is the thermal voltage, m^*_{h-Si} and $m^*_{h-st-Si}$ are the effective masses of hole density-of-states in silicon and strained silicon respectively and V_{bi-Si} is the built in potential in silicon channel.

3.2.2. Surface potential modeling

Assuming uniform impurity density in the channel region and neglecting the effect of charge carriers and fixed oxide charges on the electrostatics of the channel, the two dimensional Poisson's equation defining the potential distribution in the silicon thin film before the onset of strong inversion can be expressed as [3.22]:

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \qquad \text{For } (0 \le x \le L,\ 0 \le y \le t_{Si}) \qquad (3.1)$$

where, $\varphi(x,y)$ is the 2-D potential profile in the silicon channel, N_{ch} is the doping concentration of the p-type substrate and ε_{Si} is the permittivity of silicon. Considering parabolic potential profile in the channel [3.22], $\varphi(x,y)$ can be written as

$$\varphi(x,y) = \varphi_{sf}(x) + d_1(x)y + d_2(x)y^2 \qquad \text{For } (0 \le x \le L,\ 0 \le y \le t_{Si}) \qquad (3.2)$$

where, $\varphi_{sf}(x)$ is the front interface surface potential and $d_1(x)$ and $d_2(x)$ are the arbitrary coefficient which are function of x only, while x and y are considered as the horizontal and vertical positional coordinates.

The device structure under consideration has two different metals in the front gate which defines two separate channel regions under each gate metal where the surface potentials under M_A and M_B can be written based on (eq. 3.2) as

$$\varphi_A(x,y) = \varphi_{sfA}(x) + d_{A1}(x)y + d_{A2}(x)y^2 \qquad (3.3)$$

$$\varphi_B(x,y) = \varphi_{sfB}(x) + d_{B1}(x)y + d_{B2}(x)y^2 \tag{3.4}$$

Where φ_{sfA} and φ_{sfB} are the surface potentials under M_A and M_B respectively, ϕ_{Si} is the silicon work function and d_{A1}, d_{A2}, d_{B1} and d_{B2} are arbitrary coefficients. Depending on the continuity of electrostatic potential and electric field at the junction of two gate metals, the four boundary conditions used here are as follows:

i) Electric flux at the gate/front-oxide interface is continuous for both the metal gates

$$\left.\frac{d\varphi_A(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\varphi_{sfA}(x) - V'_{G_A}}{t_{ox}}, \qquad \text{for } M_A \tag{3.5}$$

$$\left.\frac{d\varphi_B(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\varphi_{sfB}(x) - V'_{G_B}}{t_{ox}}, \qquad \text{for } M_B \tag{3.6}$$

where ε_{ox} is the dielectric constant of the oxide, t_{ox} is the gate oxide thickness, and

$$V'_{G_A} = V_{GS} - V_{FB_A,f} \;\; \& \;\; V'_{G_B} = V_{GS} - V_{FB_B,f}$$

where V_{GS} is the gate-to-source bias voltage, $V_{FBA,f}$ and $V_{FBB,f}$ are the front-channel flatband voltages under M_A and M_B, respectively and

$$V_{FB_A,f} = \phi_A - \phi_{Si} \text{ and } V_{FB_B,f} = \phi_B - \phi_{Si}$$

ii) Electric flux at the interface of BOX layer and the back channel is continuous for both the metal gates.

$$\left.\frac{d\varphi_A(x,y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{box/air}}{\varepsilon_{Si}} \frac{V'_{SUB} - \varphi_{back}(x)}{t_{box/air}}, \text{ for } M_A \tag{3.7}$$

$$\left.\frac{d\varphi_B(x,y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{box/air}}{\varepsilon_{Si}} \frac{V'_{SUB} - \varphi_{back}(x)}{t_{box/air}}, \text{ for } M_B \tag{3.8}$$

where $t_{box/air}$ is the buried oxide thickness, $\phi_{back}(x)$ is the potential function along the backside oxide–silicon interface, and $V'_{SUB} = V_{SUB} - V_{FB,back}$, where V_{SUB} is the substrate bias, and $V_{FB,back}$ is the back-channel flatband voltage.

iii) Surface potential at the interface of the two dissimilar metals is continuous

$$\varphi_A(L_1,0)=\varphi_B(L_1,0) \tag{3.9}$$

iv) Electric flux at the interface of the two dissimilar metals is continuous

$$\left.\frac{d\varphi_A(x,y)}{dx}\right|_{x=L1}=\left.\frac{d\varphi_B(x,y)}{dx}\right|_{x=L1} \tag{3.10}$$

v) The potential at the source end is

$$\varphi_A(0,0)=\varphi_{sfA}(0)=V_{bi} \tag{3.11}$$

where V_{bi} is the built in potential across the body-source junction.

vi) The potential at the drain end is

$$\varphi_B(L_1+L_2,0)=\varphi_{sfB}(L_1+L_2)=V_{bi}+V_{DS} \tag{3.12}$$

where V_{DS} is the applied drain to source voltage.

The coefficients d_{A1}, d_{A2}, d_{B1} and d_{B2} are all functions of x and their values are calculated using boundary conditions. Substituting these values in equation (3.3) and (3.4) and then in (3.1), two second order differential equations are obtained as in [3.23]:

$$\frac{d^2\varphi_{sfA}(x)}{dx^2}+\kappa\varphi_{sfA}(x)=\rho_A \text{, under } M_A \tag{3.13}$$

$$\frac{d^2\varphi_{sfB}(x)}{dx^2}+\kappa\varphi_{sfB}(x)=\rho_B \text{, under } M_B \tag{3.14}$$

where

$$\kappa=\frac{2\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_{box/air}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)} \tag{3.15}$$

$$\rho_A = \frac{qN_{ch}}{\varepsilon_{Si}} - \frac{2V_{G_A}^{'}\left[\frac{C_{ox}}{C_{box/air}} + \frac{C_{ox}}{C_{Si}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)} - \frac{2V_{SUB}^{'}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)} \quad (3.16)$$

$$\rho_B = \frac{qN_{ch}}{\varepsilon_{Si}} - \frac{2V_{G_B}^{'}\left[\frac{C_{ox}}{C_{box/air}} + \frac{C_{ox}}{C_{Si}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)} - \frac{2V_{SUB}^{'}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)} \quad (3.17)$$

where C_{Si} , C_{ox} and $C_{box/air}$ are the channel depletion layer capacitance, front gate oxide capacitance and buried oxide layer (/ air) capacitance respectively. The second order differential equations given by equations 3.13 and 3.14 can be solved to obtain the expressions for surface potential under M_A and M_B of the front gate and are given by:

$$\varphi_{sfA}(x) = U_A e^{\eta x} + V_A e^{-\eta x} - \frac{\rho_A}{\kappa} \quad \text{for } 0 \le x \le L_1 \text{ under } M_A \quad (3.18)$$

Similarly,

$$\varphi_{sfB}(x) = U_B e^{\eta x} + V_B e^{-\eta x} - \frac{\rho_B}{\kappa} \text{ for } L_1 \le x \le L \text{ under } M_B \quad (3.19)$$

Using the boundary conditions of surface potential at source and drain end, the co-efficients of the surface potential expression (Eq. 3.18 and eq. 3.19) can be solved and given as:

$$U_A = \frac{\left(V_{bi} + V_{DS} + \sigma_B\right) - \left(V_{bi} + \sigma_A\right)e^{-\eta L} + \left(\sigma_A - \sigma_B\right)\cosh(\eta L_2)}{e^{\eta L}\left(1 - e^{-2\eta L}\right)}$$

$$V_A = \frac{\left(V_{bi} + \sigma_A\right) - \left(V_{bi} + V_{DS} + \sigma_B\right)e^{-\eta L} - \left(\sigma_A - \sigma_B\right)\cosh(\eta L_2)e^{-\eta L}}{\left(1 - e^{-2\eta L}\right)}$$

$$U_B = U_A e^{\eta L_1} - \frac{\left(\sigma_A - \sigma_B\right)}{2}$$

$$V_B = V_A e^{-\eta L_1} - \frac{(\sigma_A - \sigma_B)}{2}$$

$$\sigma_A = \frac{\rho_A}{\kappa}, \sigma_B = \frac{\rho_B}{\kappa}, \eta = \sqrt{\kappa}$$

3.2.3. Threshold voltage modeling

Threshold voltage can be defined as the gate voltage V_{GS} at which the inversion layer is formed at the oxide-semiconductor interface which acts as the conducting channel connecting the highly doped source and drain regions of the SON MOSFET. In a fully depleted thin-film SON, it is desirable that the front channel should turn on before the back channel. Therefore, this work considers the threshold voltage to be the gate to source voltage for which $\varphi_{s,\min} = 2\phi_F$, where ϕ_F is Fermi potential. The proposed DMG SON structure has two metal gates M_A and M_B with different work functions. The threshold voltage is defined as the gate to source voltage at which the minimum surface potential under higher work function gate M_A $\phi_{s,\min}$ equals twice the said Fermi potential (ϕ_F).

Hence we can determine the value of threshold voltage as the value of V_{GS} by solving:

$$\varphi_{sfA,\min} = 2\phi_F \tag{3.20}$$

The position of channel potential minima can be obtained by equating the first order derivative of surface potential of the channel under higher work function gate M_A to zero.

$$\left.\frac{d\varphi_{sfA}(x)}{dx}\right|_{x=x_{\min}} = 0$$

$$\Rightarrow \eta U_A e^{\eta x_{\min}} - \eta V_A e^{-\eta x_{\min}} = 0$$

$$\Rightarrow e^{2\eta x_{\min}} = \frac{V_A}{U_A}$$

$$x_{\min} = \frac{1}{2\eta}\ln\left(\frac{V_A}{U_A}\right) \tag{3.21}$$

Now substituting the value of position of potential minima (x_{min}) along the channel in equation 3.18 gives the expression of $\varphi_{sfA_{\min}}(x = x_{\min})$ as:

$$\varphi_{sfA_{\min}}(x = x_{\min}) = U_A e^{\eta x_{\min}} + V_A e^{-\eta x_{\min}} - \frac{\rho_A}{\kappa}$$

$$\Rightarrow \varphi_{sfA_{\min}} = U_A e^{\eta \frac{1}{2\eta} \ln(\frac{V_A}{U_A})} + V_A e^{-\eta \frac{1}{2\eta} \ln(\frac{V_A}{U_A})} - \sigma_A$$

$$\varphi_{sfA,\min} = 2\sqrt{U_A V_A} - \sigma_A \tag{3.22}$$

Finally, substituting eq.(3.22) in (3.20),

$$\varphi_{sfA,\min} = 2\sqrt{U_A V_A} - \sigma_A = 2\phi_F$$

$$\Rightarrow 2\sqrt{U_A V_A} - \frac{\rho_A}{\kappa} = 2\phi_F$$

$$\Rightarrow 2\sqrt{U_A V_A} - \frac{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)}{2\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_{box/air}}\right]}\left(\frac{qN_{ch}}{\varepsilon_{Si}} - \frac{2V'_{G_A}\left[\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)} - \frac{2V'_{SUB}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)}\right) = 2\phi_F$$

$$\Rightarrow 2\sqrt{U_A V_A} + \theta V_{GS} = 2\phi_F + u$$

Where $u = \frac{qN_{ch}}{\varepsilon_{Si}} \frac{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)}{2\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_{box/air}}\right]} - \frac{V'_{SUB}}{\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_{box/air}}\right]} + V_{FB_A,f} \frac{\left[\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]}{\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_{box/air}}\right]}$

and $\theta = \frac{\left[\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]}{\left[1+\frac{C_{ox}}{C_{Si}}+\frac{C_{ox}}{C_{box/air}}\right]}$

Similarly, $\sigma_B = v - \theta V_{GS}$ where

$$v = \frac{qN_{ch}}{\varepsilon_{Si}} \frac{t_{Si}^2\left(1+\frac{2C_{Si}}{C_{box/air}}\right)}{2\left[1+\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]} - \frac{V_{SUB}^{'}}{\left[1+\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]} + V_{FB_B,f} \frac{\left[\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]}{\left[1+\frac{C_{ox}}{C_{box/air}}+\frac{C_{ox}}{C_{Si}}\right]}$$

Now,

$$U_A = \frac{\left(V_{bi}+V_{DS}+\sigma_B\right)-\left(V_{bi}+\sigma_A\right)e^{-\eta L}+\left(\sigma_A-\sigma_B\right)\cosh(\eta L_2)}{e^{\eta L}\left(1-e^{-2\eta L}\right)}$$

$$\Rightarrow \frac{V_{bi}(e^{-\eta L}-e^{-2\eta L})+V_{DS}e^{-\eta L}+(v-\theta V_{GS})e^{-\eta L}-(u-\theta V_{GS})e^{-2\eta L}+\left(u-\theta V_{GS}-v+\theta V_{GS}\right)\cosh(\eta L_2)e^{-\eta L}}{\left(1-e^{-2\eta L}\right)}$$

$$\Rightarrow \frac{V_{bi}(1-e^{-\eta L})+V_{DS}+v-ue^{-\eta L}+\left(u-v\right)\cosh(\eta L_2)+\theta V_{GS}(e^{-\eta L}-1)}{2\sinh(\eta L)}$$

$$\Rightarrow U_A = \frac{N_1+\theta V_{GS}(e^{-\eta L}-1)}{2\sinh(\eta L)}$$

Where $N_1 = V_{bi}\left(1-e^{-\eta L}\right)+V_{DS}+\left(u-v\right)\cosh(\eta L_2)+v-ue^{-\eta L}$

Similarly,

$$V_A = \frac{\left(V_{bi}+\sigma_A\right)-\left(V_{bi}+V_{DS}+\sigma_B\right)e^{-\eta L}-\left(\sigma_A-\sigma_B\right)\cosh(\eta L_2)e^{-\eta L}}{\left(1-e^{-2\eta L}\right)}$$

$$\Rightarrow \frac{V_{bi}(e^{\eta L}-1)-V_{DS}+(u-\theta V_{GS})e^{\eta L}-(v-\theta V_{GS})-\left(u-v\right)\cosh(\eta L_2)}{2\sinh(\eta L)}$$

$$\Rightarrow V_A = \frac{N_2+\theta V_{GS}(1-e^{\eta L})}{2\sinh(\eta L)}$$

Where $N_2 = V_{bi}\left(e^{\eta L}-1\right)-V_{DS}+ue^{\eta L}-v-\left(u-v\right)\cosh(\eta L_2)$

Re-writing equation 3.22 for calculating threshold voltage,

$$\varphi_{sfA,\min} = 2\sqrt{U_A V_A}-\sigma_A = 2\phi_F$$

$$\Rightarrow 2\sqrt{\frac{N_1+\theta V_{GS}(e^{-\eta L}-1)}{2\sinh(\eta L)}.\frac{N_2+\theta V_{GS}(1-e^{\eta L})}{2\sinh(\eta L)}}-(u-\theta V_{GS}) = 2\phi_F$$

Simplifying the above expression, we get a quadratic equation of V_{GS} as:

$$\tau V_{GS}^2 + \omega V_{GS} + \vartheta = 0 \tag{3.23}$$

Where

$$\tau = \theta^2 \left\{ e^{\eta L} + e^{-\eta L} - 2 - \sinh^2(\eta L) \right\}$$
$$\omega = N_1 \theta \left(1 - e^{\eta L}\right) + N_2 \theta \left(e^{-\eta L} - 1\right) + 2\sinh^2(\eta L)\left(2\phi_F + u\right)\theta$$
$$\vartheta = N_1 N_2 - \sinh^2(\eta L)\left(2\phi_F + u\right)^2$$

The quadratic equation 3.23 can be solved to get the final expression of threshold voltage as:

$$V_{TH} = \frac{-\omega \pm \sqrt{\omega^2 - 4\tau\vartheta}}{2\vartheta} \tag{3.24}$$

It can be easily understood that the calculated V_{TH} is a direct function of length and material work-functions of the two gate metals. This particular dependence of threshold voltage on the said factors is a unique feature of the proposed structure providing the designer with a different degree of freedom towards controlling and engineering the threshold voltage of ultra-small SON transistor design.

3.2.4. Mobility Modeling

From the knowledge of strained devices, it is known that the incorporation of strain in the silicon channel significantly enhances the carrier mobility as a function of Ge mole fraction i.e. composition of Ge denoted by 'X' in the relaxed $Si_{1-x}Ge_x$ layer underneath the channel region. The mole fraction (X) dependent electron mobility in strained silicon channel can be expressed as [3.24]:

$$\mu_{n-st} = \mu_0 \left(1 + 4.31X - 2.28X^2\right) \tag{3.25}$$

Where μ_0 is the electron mobility in unstrained silicon channel and can be approximated as [3.25]:

$$\mu_0 = \left[\left(\mu_{ph}\mu_{sr}\mu_{bl}\right) \Big/ \left(\mu_{ph}\mu_{sr} + \mu_{ph}\mu_{bl} + \mu_{sr}\mu_{bl}\right) \right] \tag{3.26}$$

Where μ_{ph}, μ_{sr} and μ_{bl} are the acoustic phonon scattering affected mobility, surface roughness limited carrier mobility and carrier mobility in bulk silicon material respectively related by Matheissen's rule. μ_0 is calculated using parameters listed in the Table 3.1.

TABLE 3.1

MOBILITY PARAMETERS

μ_{ph}	B	4.75×10^7	cm/s
	C	$1.75 \times 10^5 \times N_A^{0.125}$	N_A in cm^{-3}
μ_{bl}	μ_0	52.2	$cm^2/V.s$
	μ_{max}	1417	$cm^2/V.s$
	μ_l	43.4	$cm^2/V.s$
	γ	2.5	-
	C_r	9.68×10^{16}	cm^{-3}
	C_s	3.43×10^{20}	cm^{-3}
	α	0.680	-
	β	2.00	-
μ_{sr}	δ	5.82×10^{14}	V/s

3.2.5. Drain Current Modeling

Having obtained the analytical expression for threshold voltage, the drain current may be obtained by putting the calculated value of threshold voltage in the MOSFET current equations in different operating regions. This work considers a strained DMG SOI/SON structure with a channel dimension in the order of nanometer. Such ultra scaled channel dimension results in some inevitable short channel effects (SCEs) like Channel Length Modulation (CLM), Drain Induced Barrier Lowering (DIBL), high electric field induced mobility degradation, velocity saturation at high electric field etc. which adversely impact the device performance. These short channel effects are thus taken into consideration while modeling the drain current of the proposed short channel device and the resultant expressions can be written as [3.26]:

$$I_{DS} = \frac{W\mu_{n-st}C_{ox}}{L\left[1-\left(l_c / L\right)+\left(V_{DS} / LE_C\right)\right]}\left[(V_{GS} - V'_{TH})V_{DS} - 0.5V_{DS}^2\right] \quad \text{(in linear region)} \quad (3.27)$$

$$I_{DS} = \frac{W\mu_{n-st}C_{ox}}{L\left[1-\left(l_c / L\right)+\left(V_{DS,sat} / LE_C\right)\right]}\left[(V_{GS} - V'_{TH})V_{DS,sat} - 0.5V_{DS,sat}^2\right] \quad \text{(in saturation region)} \quad (3.28)$$

Where $l_c = f(V_{DS})$ is the channel length measured from drain side across which the voltage difference (V_{DS}-$V_{DS,sat}$) is dropped, $V'_{TH} = V_{TH}$-DIBL is the effective threshold voltage, E_C is the critical electric field at which the electron velocity ν_{sat} saturates and $V_{DS,sat}$ is the saturation voltage and are given as

$$E_C = \frac{2\nu_{sat}}{\mu_{n-st}} \quad ; \quad V_{DS,sat} = \left(V_{GS} - V_{TH}\right) \Big/ 1+\left(V_{GS} - V_{TH}\right) / LE_C$$

In order to study a comparative analysis of the drain current characteristics of the proposed device, different figure-of-merits have to be calculated. Out of them, device transconductance and drain conductance are two such figures of merits.

The trans-conductance (g_m) can be obtained by differentiating drain current equations in linear and saturation regions (eq.3.27 and eq.3.28) w.r.t V_{GS} at a constant value of V_{DS} and are given as [3.26]:

$$g_{m,lin} = \frac{W\mu_{n-st}C_{ox}}{L\left[1-\left(l_c/L\right)+\left(V_{DS}/LE_C\right)\right]}V_{DS} \quad \text{(linear region)} \quad (3.29)$$

$$g_{m,sat} = \frac{W\mu_{n-st}C_{ox}}{L\left[1-\left(l_c/L\right)+\left(V_{DS,sat}/LE_C\right)\right]}V_{DS,sat} \quad \text{(saturation region)} \quad (3.30)$$

A similar expression can be determined for drain conductance (g_d) by differentiating drain current equations in linear and saturation regions (eq.3.27 and eq.3.28) w.r.t V_{DS} at a constant V_{GS} and are given as [3.26]:

$$g_{d,lin} = \frac{W\mu_{n-st}C_{ox}}{L}\left[\begin{Bmatrix}\left(V_{GS}-V_{TH}^{'}-V_{DS}\right)\Big/ \\ \Big/\left(1-l_c/L+V_{DS}/LE_C\right)\end{Bmatrix}+\begin{Bmatrix}\left(\frac{dl_c}{dV_{DS}}-1/E_C\right)\left\{\left(V_{GS}-V_{TH}^{'}\right)V_{DS}-0.5V_{DS}^2\right\} \\ L\left(1-l_c/L+V_{DS}/LE_C\right)^2\end{Bmatrix}\right] \quad \text{(in linear region)} \quad (3.31)$$

$$g_{d,sat} = \frac{W\mu_{n-st}C_{ox}\left[dl_c/dV_{DS}\left\{\left(V_{GS}-V_{TH}^{'}\right)V_{DS,sat}-0.5V_{DS,sat}^2\right\}\right]}{L^2\left(1-l_c/L+V_{DS,sat}/LE_C\right)^2} \quad \text{(in saturation region)} \quad (3.32)$$

3.3. Results and Discussions

In this chapter, the analytical modeling and simulation of a Dual Material Gate strained SON structure has been investigated in details. The channel length is taken as 100 nm for the analysis. Two metals with different work functions have been taken with the gate with the metal having higher work function near the source end. Different parameters that we have used in both calculation and simulation are given in Table. 3.2.

Table 3.2: Simulation Parameters

Parameters	N_A	N_d	**L1=L2**	t_{Si}	t_{ox}	$t_{box/air}$	V_{GS}	ϕ_A	ϕ_B
Values	10^{21} m^{-3}	$5x10^{25}$ m^{-3}	50 nm	6 nm	3 nm	100 nm	0.15V	4.63 eV	4.17eV

In figures 3.2, 3.3 and 3.4 variation of electron mobility in strained channel is shown against Ge mole fraction, channel doping concentration and transverse electric field respectively. It can be seen that an increase in the Ge composition results in a subsequent increase in strain induced in the channel region due to the gradual change in deformation potentials, which in turn enhances the effective channel electron mobility. As temperature increases, bulk and acoustic phonon scattering limited mobility components get affected and their contribution to total effective electron mobility decreases as noticed in Fig. 3.2. Furthermore, the slope of electron mobility against Ge mole fraction

(X) decreases gradually with increase in X because of the increased misfit dislocations in the strained channel.

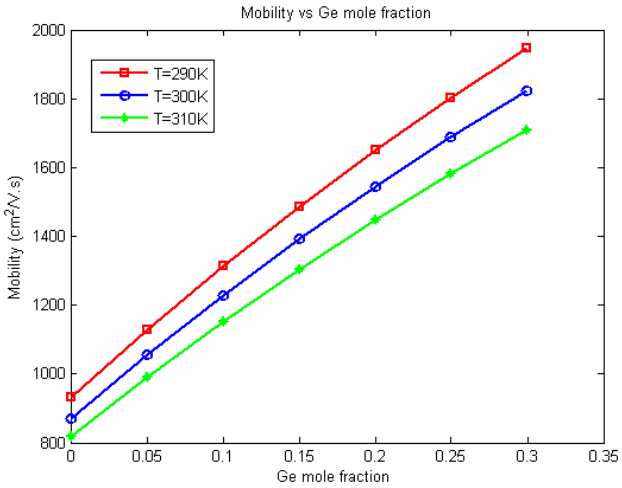

Figure 3.2. Electron mobility variation against Ge composition (X) in strained silicon channel with temperature as a parameter using parameters listed in Table 3.2. Solid lines represent analytical results. Symbols represent simulation results.

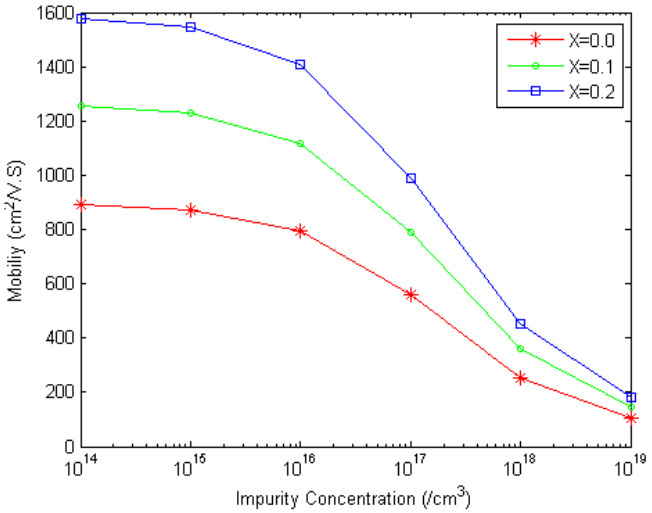

Figure 3.3. Electron mobility variation against channel impurity concentration (for three different values of X in strained silicon channel).

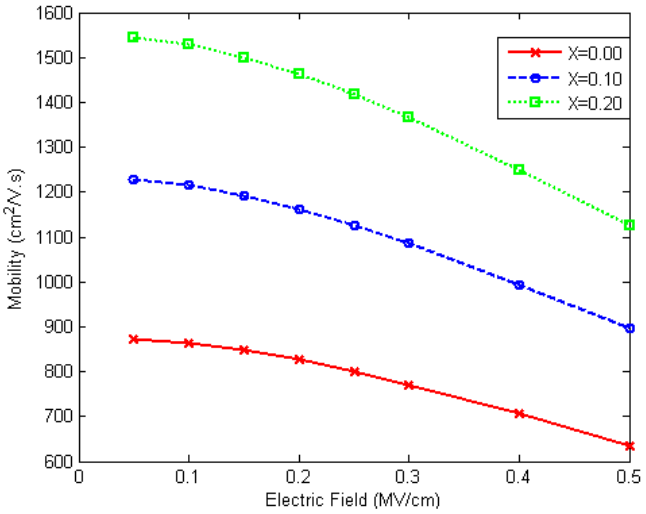

Figure 3.4. Electron mobility variation against transverse electric field in strained silicon channel for three different values of X.

The variation of carrier mobility with channel impurity concentration has been depicted in Fig.3.3. It can be seen that an increase in channel impurity concentration results in an enhanced carrier-impurity scattering effect, which abruptly reduces the effective electron mobility in the strained channel after channel doping concentration exceeds a certain limiting value. Again, it is evident from Fig.3.4 that as the electric field increases gradually, the channel electrons get distributed close to the SiO_2/Si front interface thereby increasing the probability for an electron to undergo a diffusive scattering. At a sufficiently high transverse electric field, the surface-roughness scatterings become dominant leading to the significant reduction in mobility [3.27].

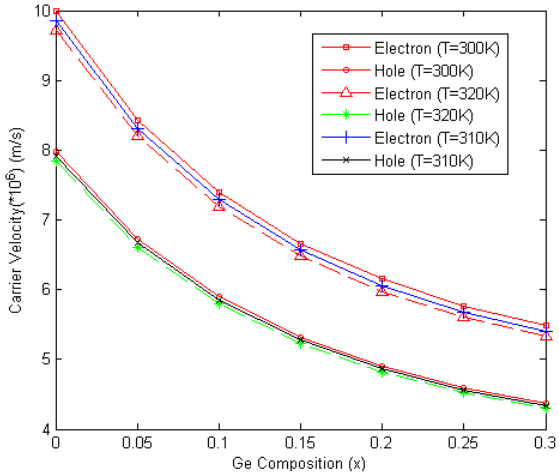

Figure 3.5. Carrier velocity variation against Ge mole fraction in strained silicon channel with temperature as a parameter.

Fig. 3.5 shows that increase in mole fraction(X) and temperature enhances the carrier scattering effect which is reflected as an effective decrease in carrier drift velocity.

Fig. 3.6 depicts the surface potential against the position along the channel for different values of Ge mole fraction. The dual material gate results in a sharp step in the surface potential profile that 'screens' the channel region under M_A from the drain bias variations resulting in practically no significant change in channel potential minima under gate M_A with increase in drain bias, thereby immensely reducing the detrimental short channel effect of Drain Induced Barrier Lowering (DIBL). Therefore, it can be inferred that V_{DS} has only a little influence on the drain current beyond the point of saturation [3.26] and as a result, the drain conductance is also reduced.

It can also be seen from the said figure that the surface potential under gates M_A and M_B increases with Ge mole fraction and it is higher for SON than that of SOI. The upward shift of potential minima is higher for SON in nano regime as evident from the figure. A higher value of surface potential minima indicates that the drain bias is having lesser impact on reducing the potential barrier which is ideally expected to be solely controlled by applied gate bias only. This ensures higher immunity to the adverse short channel effect of Drain Induced Barrier Lowering (DIBL) or Two Dimensional Charge Sharing Effects (2DCEs).

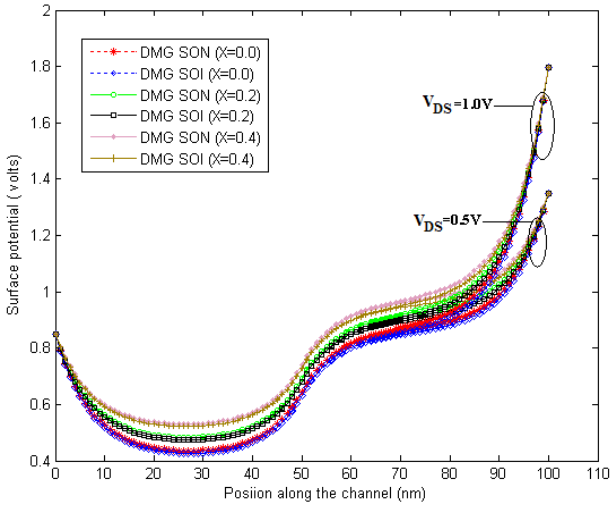

Fig. 3.6. Surface potential distribution against channel position for strained and unstrained SOI and SON structures. Symbols represent simulation results.

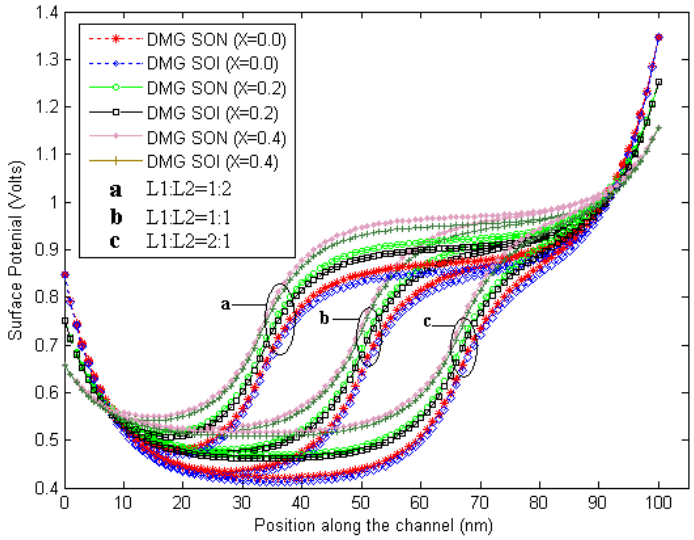

Fig. 3.7.Surface potential distribution against channel position of FD DMG SOI and SON MOSFETs considering different gate length ratios with Ge mole fraction as a parameter.

The variation of surface potential along the channel position for different gate length ratios (L1/L2= 2 : 1, 1 : 1, 1 : 2) has been shown in Fig.3.7. The gate length L is considered to be 100 nm and surface potential variation has been shown for different values of effective Ge mole fraction(X) in the relaxed $Si_{1-x}Ge_x$ buffer. Using two metals M_A and M_B with different work-functions in the gate electrode (with M_A placed near source terminal having work function value greater than M_B near the drain terminal) results in the formation of a sharp step in the surface potential profile at the interface of M_A and M_B for the DMG SOI and SON MOSFETs, which screens the source side from the drain bias variations, thereby significantly suppressing the detrimental SCEs. With the reduction of gate length ratio, the abrupt change of the potential moves toward the source side. The surface potential is also seen to shift up with increasing strain i.e. the Ge mole fraction X making the device more immune to SCEs as already explained earlier.

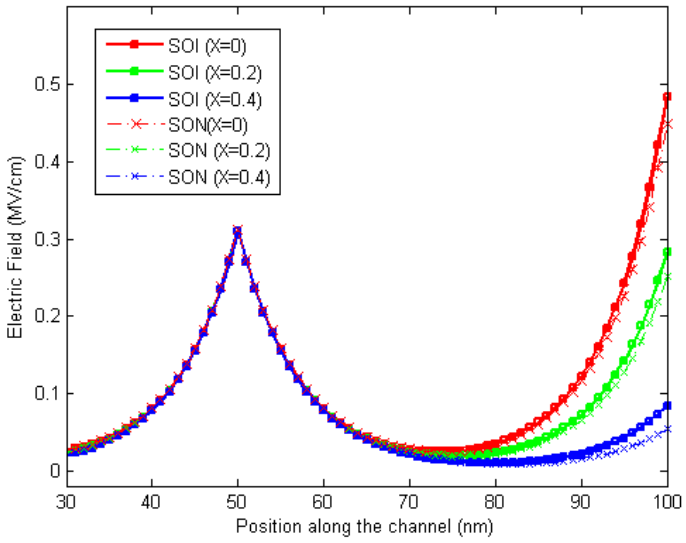

Fig. 3.8. Electric field variation with channel position of FD DMG SOI and SON MOSFETs for different Ge mole fraction.

The variation of channel electric field with position along the channel of FD DMG SOI and SON MOSFETs is shown in Fig. 3.8 for different Ge mole fraction values (X). It can be seen that for both SOI and SON devices, the peak electric field near the drain end reduces as the Ge mole fraction in the strained channel is increased from 0 to 0.4. Thus, strain incorporation reduces drain end peak electric field, which in turn reduces the chances of device performance deterioration by impact ionization induced Hot Carrier Effect (HCE). Moreover, the peak electric field in SON devices is seen to be less than their SOI counterparts for each value of X indicating the superiority of SON in suppressing SCEs over its SOI equivalent for obvious reasons discussed earlier.

Fig.3.9 exhibits the variation of threshold voltage for strained DMG SOI and DMG SON MOSFETs. For a bulk MOSFET, the threshold voltage is determined entirely from the front surface potential. The back surface potential does not have any significant effect on the threshold voltage. However, the scenario of a short channel device is entirely different from this simple ideal case. The back channel surface potential in case of sub 100 nm devices will have considerable impact on the front surface potential due a reduced value of potential coupling ratio (PCR= ϕ_f / ϕ_b). In SON, the BOX layer material is air having a lower permittivity than oxide in case of SOI giving SON a better insulation than SOI. This in turn results in a reduced impact of back channel surface potential on the front surface potential in case of SON as compared to its SOI counterpart making the SON structure more immune to SCEs than that of SOI MOSFET [3.28]. This can be understood from the much reduced value of threshold voltage in SON than SOI as shown in Fig. 3.9.

Meanwhile, it can also be seen from Fig.3.9 that the threshold voltage for both SOI and SON devices decreases with an increase in the Ge mole fraction (X) which in turn increases the current driving capability of a strained structure as compared to its unstrained counterpart, justifying the effectiveness of a strained silicon channel to get an improved device current drivability.

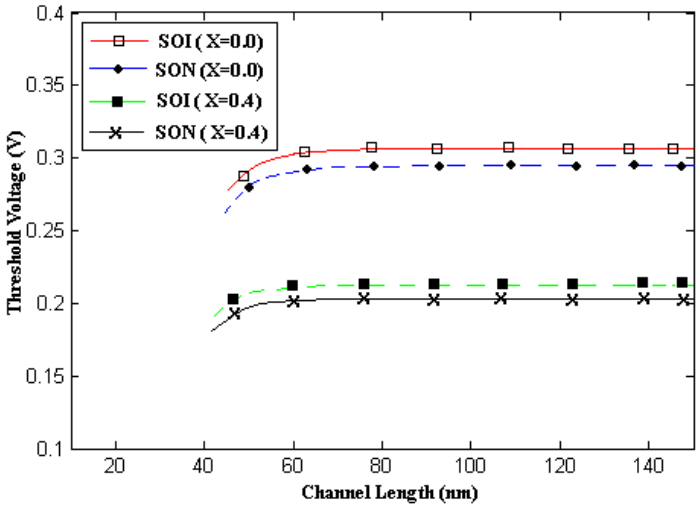

Fig. 3.9. Threshold voltage variation with channel length of strained DMG SOI and DMG SON MOSFET structures for three different values of X. Solid lines represent analytical results. Symbols represent simulation results.

Fig. 3.10 depicts the I_D-V_D characteristics of the proposed device where the variation of drain current with drain to source voltage has been shown incorporating the channel length modulation (CLM), DIBL and other SCEs. An abrupt transition is seen to occur at saturation point for higher V_{GS} due to enhanced gate control. It is evident from the figure that the drain current becomes constant in the saturation region if CLM and other SCEs are neglected, but it shows a finite slope if we consider CLM and other effects in our model [3.26].

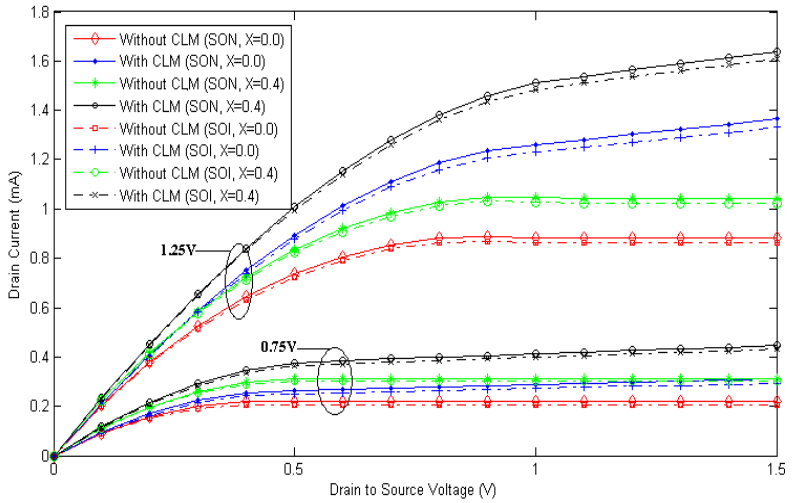

Fig. 3.10. Output or I_D-V_{DS} characteristics of strained DMG SOI and DMG SON MOSFET structures with channel length L = 100nm considering different values of V_{GS}:1.25V and 0.5V.

Fig.3.11 and Fig.3.12 show the variation of Trans conductance (g_m) and drain conductance (g_d) of the strained silicon channel DMG SOI and DMG SON MOSFET with the device channel length, L respectively. It has already been illustrated in Fig. 3.10 that the SON MOSFETs exhibit better current driving capability compared to its SOI counterpart. As a result, both transconductance and drain conductance of a SON device shows significant improvement over its SOI equivalent, which in turn improves the corresponding voltage gain of the SON device as well, making the proposed DMG SON device a suitable alternative over its SOI counterpart in terms current drivability [3.9, 3.28]. Furthermore, the current driving capability of strained DMG SON devices will be higher than normal DMG SON device without strain due to the strain induced carrier mobility enhancement.

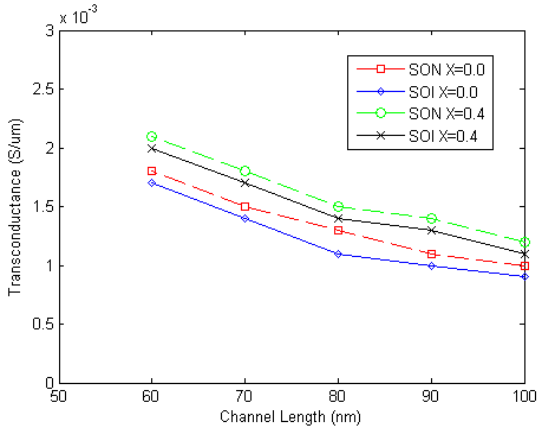

Fig. 3.11. Transconductance variation with channel length DMG SOI and SON MOSFETs considering two different values of X. Symbols represent simulation results.

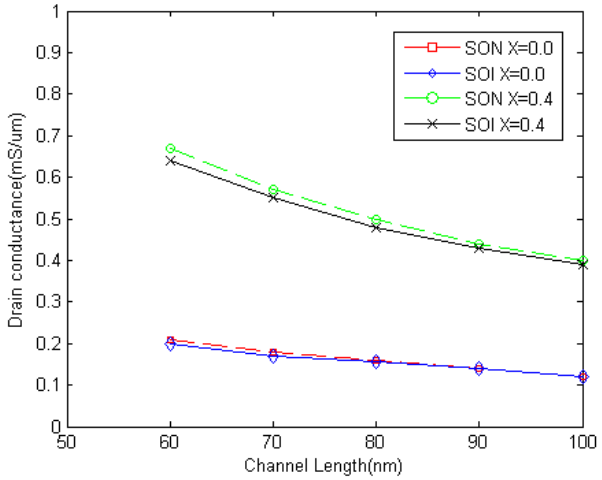

Fig. 3.12. Drain conductance variation with channel length for strained DMG SOI and SON MOSFETs considering two different values of X at V_{GS}=0.65V. Symbols represent simulation results.

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Relevant Publications:

- **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "A Compact Two Dimensional Analytical Modeling of Nanoscale Fully Depleted Dual Material Gate strained SOI/SON MOSFETs for subdued SCEs." In **Journal of Low Power Electronics, ASP**, Volume 10, Number 3, pp. 383-391, September 2014.
- **Saheli Sarkhel**, Bibhas Manna, P.K. Dutta and Subir Kumar Sarkar. "Analytical Model for performance comparison of a nano scale Dual Material Double Gate Silicon on Insulator (SOI) and Silicon on Nothing (SON) MOSFET." In **Journal of Nano Engineering and Nano Manufacturing, ASP**, Vol.4, No. 3, pp. 182-188, 2014.
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- **Saheli Sarkhel**, Sounak Naha and Subir Kumar Sarkar "Reduced SCEs in Fully Depleted Dual-Material Double-Gate (DMDG) SON MOSFET: Analytical Modeling and Simulation." In **International Journal of Scientific and Engineering Research**, Volume 3, Issue 6, June 2012 Edition.

Chapter 4

Some innovative multigate MOSFETs with work function engineered gate electrode

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CHAPTER IV

4.1. Introduction

Technology dependence of modern civilization in every sphere of life starting from industrial revolution, automotive, consumer electronics and wireless communication for the vision of lavish lifestyle, automation of safety and security is increasing each day to make the world a smarter place to live in. This excessive dependence of human civilization on process automation and high speed real time interconnectivity has been the primary and continuous driving force behind the boon in automation and consumer electronics making research and development in the field of semiconductor devices an emerging area for researchers worldwide. Ongoing development in the VLSI industry from micro to nano regime is driven by the need of ultra low dimensional, low power consuming, high speed devices so as to achieve improved performance and better functioning of available system on chips (SOCs) integrating a large number of transistors. As discussed in the previous chapters, these improvements in IC performance can only be possible by packing more and more number of devices which automatically calls for a reduction in the physical dimension of devices as predicted by Moore's scaling trend, thereby doubling the number of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) integrated on a single chip in every two years. Downsizing the device dimensions to sub-nanometer regime enhances the current drivability, processing speed and device density in the resulting VLSI circuits as desired, but there is some price to pay. Aggressive device dimension miniaturization specified by ITRS [4.1] comes hand in hand with some of the major bottlenecks of undesired Short Channel Effects (SCEs), enhanced junction leakage currents, gate depletion, direct tunneling and several other issues which degrade device performance and create some serious reliability issues.

These bottlenecks pose serious threat on the unhindered progress of semiconductor industry governed by this scaling trend of conventional MOSFET device dimension which can only be resolved by innovation of some non-conventional device structures. In the last chapter, we have already studied the performance of Fully Depleted Silicon-on-Insulator/Nothing (FD SOI/SON) over its conventional bulk MOSFET counterpart by dint of its unique geometrical feature of embedding a buried oxide or air (BOX/air) layer underneath the conducting channel in order to reduce the coupling effect, capacitances of parasitic p-n junctions and allied short channel effects ensuing notable improvement in sub threshold characteristics. Further, radiation tolerances and significant reduction in propagation delays make SOI/SON a suitable alternative. However, the advantages associated with single gate FDSOI devices in terms of sub-threshold characteristics and higher current drivability seems to be less significant in ultra-low dimensional devices [4.2-4.10].

Apart from the SOI/SON technologies, several other non-conventional MOSFET devices are being studied for many years so as to overcome the challenges of short channel effect influenced

device performance degradation. As the physical dimension of the MOSFET channel is being continuously scaled down to meet the stringent specifications of ITRS, the major hindrance faced is basically due to the intrusion of drain side electric field into the channel region. This causes the device current to be regulated by both gate and drain applied biases instead of the sole gate control on the device current drive. This problem can be mitigated by using some special gate structures where more than one gate electrode will be there to control the device performance.

The concept of multiple gate field effect transistor (MuG-FET) is to have the silicon wire (which is the channel region termed as 'finger' or 'fin') fully enclosed or wrapped by the gate electrode ensuring the best possible gate control on the conducting channel. Thus, using this gate wrapping concept, one can create a unique geometry of gate-all-around to fully deplete even a heavily doped channel so as to turn-off the device [4.11]. Some of the widely studied popular multigate FET structures include double-gate transistors (DG FETs), triple-gate transistors (TG FETs), quadruple-gate transistors (QG FETs), gate-all-around transistors (GAA FETs), π-gate transistors, Ω-gate transistors, DELTA transistors and vertical pillar MOSFETs etc [4.11-4.19]. The multi-gate devices by dint of having the silicon channel almost completely wrapped by gate electrode exhibit better gate control over the channel which effectively improves device scalability and eventually leads to higher package density as desired by modern VLSI/ULSI industry. They can also enhance the device current deliverability, conductance due to the volume inversion phenomenon and show improved sub-threshold slope. It has already been illustrated in Chapter 2 that the quadruple gate provides the best performance compared to single and double gate counterparts with Π-gate being the close competitor. This has motivated us to investigate some unique multi-gate FETs in this chapter to emphasize upon the effectiveness of the multigate concept for superior device performance relative to conventional single gate counterparts.

In addition to this non conventional geometry of multigate transistors, another fascinating concept of gate material engineering is gaining significant research interest. In the present era of ultra-scaled devices, the channel dimension is so small that the electric field at any point in the channel becomes a combination of both vertical (due to gate bias applied) and horizontal (due to drain bias applied) electric fields as both gate and drain biases gain control over the channel due to two dimensional charge sharing. Thus, the transverse channel electric field can be tailored by properly choosing two or more metal having dissimilar work functions and placing them adjacently to function as a single gate electrode, which in turn adjusts the overall channel electric field resulting in an improved device performance. The pioneering work based on this gate material engineering concept proposed a Dual Material Gate (DMG) MOS where two materials having different work functions were used as gate electrode with the metal having higher work function placed near the source end [4.20]. This difference in work function results in a steep step-function in

the channel potential profile which screens the potential barrier at the source/channel junction from any variation in the drain bias, thereby improving device performance and enhancing device scalability. This idea of gate material engineering can be exploited to an altogether different level by considering a binary metal alloy (A_α $B_{1-\alpha}$) gate electrode where the mole fractions of constituent metals are spatially varied continuously from the source end (i.e. source side having 100% of metal A) towards drain end (i.e. drain side having 100% of metal B) [4.21-4.25]. The vertical field and consequently the overall field in this system will be adjusted by the continuous variation of work function to reduce surface potential asymmetry in nano dimensional devices. This in turn controls the DIBL significantly and improves the device performance by removing the uneven transition of surface potential and surface electric field. This unique concept of using a binary metal alloy as gate electrode can be abbreviated as '***Linearly Graded Gate (LGG)***' or '***Work Function Engineered Gate (WFEG)***' or '***Binary Metal Alloy Gate (BMA gate)***' and can be incorporated into various non-conventional device structures in order to further improve their performance.

The first section of this chapter will investigate the attributes of an asymmetric Double Gate MOSFET incorporating the novel theory of work function engineering in a fully depleted Double Gate MOSFET having binary metal alloy gate electrode with continuous spatial variation of mole fraction of the constituent metals. The next section will present the performance analysis of a Cylindrical Gate MOSFET incorporating the Work Function Engineering concept and finally the last section will study a Quadruple Gate MOSFET having Work Function Engineered Gate electrode encompassing the entire silicon channel.

4.2. Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate Electrode: an analytical approach to explore asymmetric characteristics

4.2.1. Overview and recent research trend

Motivated by the intention to address various inadequacies of conventional planar device structures, non conventional Double Gate (DG) MOSFET structure with ultra thin body and buried layer thickness (UTBB) has been extensively studied due to its superior scalability, excellent SCE reduction, ideal sub-threshold swing, double on current and excellent gate control over the channel [4.26-4.28]. The primary advantage associated with UTBB structure is the existence of strong coupling between the front and back gate electrodes. This naturally enhances control of the threshold voltage by means of back gate bias, eliminating the need of using different channel doping, which in turn suppresses the problems associated with mobility degradation and random dopant fluctuation [4.29-4.30] in the ultrathin undoped channel of DG MOSFETs.

A vivid study of available contemporary literature presents various research initiatives by different research groups in this regard to establish an analytical modeling of DG MOSFETs throwing more light on understanding the physics behind the device operation. A recent study by Tsormpatzoglou et. al. has presented a new approach for the analytical modeling of the 2-D potential distribution along the channel of an undoped DG MOSFET and subsequently formulated an expression of threshold voltage [4.31]. Moreover, some literatures also present analytical study based on gate oxide thickness asymmetry in DG MOSFETs [4.32-4.37]. In addition to this, the merits of the novel concept of using a binary metal alloy as gate electrode in modifying the vertical as well as overall channel electric field causing remarkable improvement in device performance has already been discussed vividly in the preceding section.

Motivated by the possibility to fabricate binary metal alloy gate electrode, this section of the dissertation attempts to incorporate this novel concept of linearly graded binary metal alloy gate electrode into an asymmetric Double Gate MOSFET with an objective to investigate performance improvements of the proposed Linearly Graded Asymmetric Double Gate (LGADG) MOSFET.

4.2.2. Fabrication feasibility of a Linearly Graded Gate electrode

An in depth literature review suggests that the operational physics behind the novel concept of binary metal alloy gate is actually an established theory which has been proposed and studied experimentally by Ishii et. al. [4.38], Gelatt and Ehrenreich [4.39]. On the basis of this experimental study of a binary alloy system, a MOS structure with a (100)-oriented phosphorus doped Si wafer as starting material with a binary metal alloy gate electrode was proposed by Tsui et.al [4.24]. The fabrication technique of such metal alloy gate electrode involves some critical steps. Standard RCA process is used to clean the wafer, followed by gate oxide growth and patterning of gate electrodes using liftoff process. Tantalum-Platinum (Ta-Pt) alloy system was then co-sputtered on patterned photoresist. The deposition conditions and the atomic composition were monitored using Rutherford Backscattering Spectroscopy (RBS). After patterning, the samples had to be annealed in nitrogen ambient at temperatures of 400, 500, and 600 degree Celsius for about 30 min, after which aluminium was deposited at the back. Subsequently, the approximate work-function of the annealed samples was found out by performing a comparative analysis of the measured C-V characteristics curve with theoretical C-V curve. The study shows that if the composition percentage of the higher work function material (for example Pt in TaPt alloy) is increased, the effective approximate work function of the binary metal alloy gate electrode corresponds to the work function of the constituent metal having higher value. Based on this experimental observation, it can be inferred that the resulting effective work function of the binary metal alloy gate electrode can be modulated by suitably tuning the atomic composition of the binary alloy system. This flexibility in adjusting the

work function value to achieve a desired work function value makes the unique concept of using an alloy gate electrode a possible new conduit in the field of innovative research on electron devices.

A more recent study by Pan et. al. combines spatial source reagent gradient with a temperature gradient in order to realize continuous mole fraction variation of a ZnCdSSe alloy nanowire on a single substrate, thereby establishing the fabrication feasibility of such alloy system [4.22]. In another research initiative, Christen et. al. proposed a suitable method for continuous compositional spread (CCS) thin film based on pulsed laser deposition (PLD) [4.4.-4.41]. In their work, a CCS–PLD apparatus was developed and implemented to fabricate as-grown epitaxial CCS thin film on substrates having long dimension. These studies establish that the compositions at each and every position of the CCS film (determined by energy dispersive X-ray spectrometry and Rutherford backscattering spectrometry) match well with the analytical/designed values.

The above literature survey suggests that with adjustment, modification, improvisation and careful implementation of existing and upcoming fabrication techniques, it will be possible in near future to fabricate a binary metal alloy gate electrode ($A_{\alpha}B_{1-\alpha}$) with continuous lateral component concentration variation from source (100% A) to drain side (100% B). The possible fabrication feasibility of such a binary metal alloy gate electrode has been the primary motivation for us to analytically investigate the concept of considering continuous mole fraction variation in a binary metal alloy used as the gate electrode and incorporate this concept of 'binary metal alloy gate' or 'work function engineered gate' or 'linearly graded gate' in different device structures to explore the performance improvements achieved using this innovative concept over its conventional single metal gate electrode counterparts.

4.2.3. Analytical Modeling

A schematic cross-sectional diagram of the proposed Linearly Graded Asymmetric Double Gate (LGADG) MOSFET structure has been presented in Fig. 4.2.1. This section deals with an in depth study of the asymmetricity in the conventional double gate FD-SOI MOSFET incorporating the concept of linearly graded binary metal alloy in both front and back gate electrodes comprised of different constituent metals. The binary metal alloy of the front gate electrode (M_{f1}-M_{f2}) has been taken as Platinum (Pt) with a work function of 5.3 eV and Tantalum (Ta) with a work function of 4.4 eV, while on the other hand, the binary metal alloy of the back gate electrode (M_{b1}-M_{b2}) has been considered as an alloy of Tantalum (Ta) with a work function of 4.8 eV and Titanium (Ti) with a work function of 4.3 eV with the intention to make the proposed structure completely asymmetrical. The cross section view of the said structure shows the channel length is L, Vs is the source voltage, V_{DS} is the drain voltage, V_{Gf}, V_{Gb} are the front and back gate voltages respectively, and t_{oxf}, t_{oxb}, t_{Si}

are the thickness of front oxide, back oxide and silicon substrate respectively. The parameter values have been specified in Table 4.2.1.

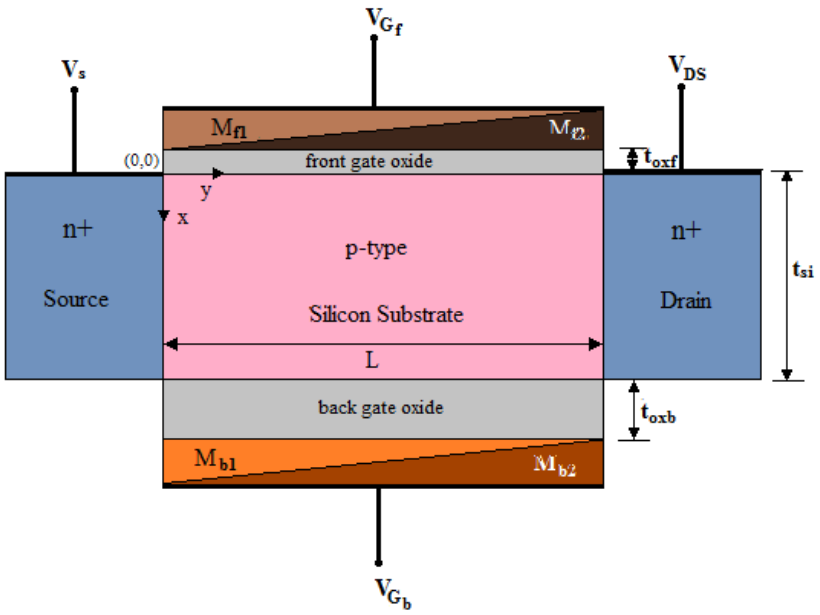


Fig.4.2.1 Schematic cross-sectional diagram of the proposed LGADG MOSFET structure

The essence of linearly graded binary metal alloy considered as the gate electrode material in this work lies in the gradual spatial adjustment of the effective work function of the binary alloy system from source towards the drain along the lateral (i.e. 'y') direction [4.25]. Metals M_{f1} and M_{b1} are considered towards the source end for front and back gates respectively. Likewise, metals M_{f2} and M_{b2} are considered towards the drain end for front and back gates respectively. The effective work functions of the front and back gate electrodes can be expressed as:

$$\phi_{meff_f} = \phi_{M_{f2}} - \frac{y}{L}(\phi_{M_{f1}} - \phi_{M_{f2}}) \quad ; \quad \phi_{meff_b} = \phi_{M_{b2}} - \frac{y}{L}(\phi_{M_{b1}} - \phi_{M_{b2}})$$

where ϕ_{meff_f}, ϕ_{meff_b} are the effective work function of front gate electrode and and back gate electrode respectively. $\phi_{M_{f1}}, \phi_{M_{f2}}, \phi_{M_{b1}}, \phi_{M_{b2}}$ are the pure constituent work functions of metals M_{f1},M_{f2},M_{b1} and M_{b2} respectively.

4.2.3.1. Channel Potential Modeling

The initial step to formulate the potential distribution within the channel in the weak inversion condition is to consider the two dimensional Poisson's equation in the channel and can be written as:

$$\frac{\partial\varphi^2(x,y)}{\partial x^2}+\frac{\partial\varphi^2(x,y)}{\partial y^2}=\frac{qN_{ch}}{\varepsilon_{si}} \qquad \text{for } 0\le x\le t_{si} \text{ and } 0\le y\le L \tag{4.2.1}$$

where $\varphi(x,y)$ is the potential function, ε_{si} is the silicon permittivity, q is electron charge and N_{ch} is the doping concentration of silicon substrate. The $\varphi(x,y)$ in the channel is considered to be parabolic in nature considering Young's Parabolic Potential Approximation (PPA) for the ease of mathematical solution [4.42] and given by:

$$\varphi(x,y)=d_0(y)+d_1(y)x+d_2(y)x^2 \tag{4.2.2}$$

Where d_0, d_1 and d_2 are arbitrary constants and functions of y only. Different values of x define different positions vertically along the channel. Considering $x=0$, $\varphi(0,y)$ becomes surface potential ($\varphi_{sf}(y)$). Similarly, if we take $x=t_{si}$ then the potential is back interface potential ($\varphi_{sb}(y)$)

$$\therefore \varphi_{sf}(y)=d_0(y) \text{ and } \varphi_{sb}(y)=\varphi_{sf}(y)+d_1(y)t_{si}+d_2(y)t_{si}^2 \tag{4.2.3}$$

Following the same procedure as used in the previous chapter, the analytical solution of Poisson equation requires some basic boundary conditions listed below:

1. Electric flux is continuous at the interface between front gate oxide and silicon channel. Hence,

$$\left.\frac{d\varphi(x,y)}{dx}\right|_{x=0}=\frac{\varepsilon_{oxf}}{\varepsilon_{si}}\frac{\varphi_{sf}(x,y)-V_{G_f}^{'}}{t_{oxf}}$$

where ε_{oxf} is the relative permittivity of front gate oxide. $V_{G_f}^{'}=V_{G_f}-V_{FBf}$ is the effective front gate voltage with V_{FBf} being the flat band voltage of the top gate: $V_{FBf}=\phi_{meff_f}-\phi_{si}$

where $\phi_{si}=\chi+{E_g}/{2q}+\phi_F$ is the work function of silicon with χ is the electron affinity, E_g denotes silicon bandgap energy at room temperature and ϕ_F represents the Fermi potential expressed by $\phi_F=V_t\ln(N_{ch}/n_i)$, where V_t signifies thermal voltage and n_i signifies intrinsic uniform channel doping concentration.

It must be noted here that the front and back gates are independent in this case making this Double Gate MOSFET to be a four terminal Double Gate MOS (4T MOS) where the front and back gates separately represent two gate terminals with the source and drain to be two remaining terminals of the device.

2. Electric flux is also continuous at the interface between back gate oxide and silicon channel. Hence,

$$\left.\frac{d\varphi(x,y)}{dx}\right|_{x=t_{si}} = \frac{\varepsilon_{oxb}}{\varepsilon_{si}}\frac{V_{G_b}^{'} - \varphi_{sb}(x,y)}{t_{oxb}}$$

where ε_{oxb} is the relative permittivity of the back gate oxide, $V_{G_b}^{'} = V_{G_b} - V_{FBb}$ is the effective back gate voltage with $V_{FBb} = \phi_{meff_b} - \phi_{si}$ being the back gate flat band voltage.

3. The channel potential at source end is $\varphi_{sf}(x,0) = V_{bi}$

where $V_{bi} = V_t \ln\left(\frac{N_{ch}N_d}{n_i^2}\right)$ is the source/drain to channel junction built-in voltage with N_d is the donor concentration of source and drain.

4. The potential at drain end is $\varphi_{sf}(x,L) = V_{bi} + V_{DS}$

The arbitrary constants d_1 and d_2 can be solved from boundary conditions 1 and 2 and are given as:

$$d_1(y) = \frac{\varepsilon_{oxf}}{\varepsilon_{si}}\frac{\varphi_{sf}(y) - V_{G_f}^{'}}{t_{oxf}} \;; \qquad d_2(y) = \frac{V_{G_b}^{'}}{t_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)} + \frac{V_{G_f}^{'}\left({}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}}\right)}{t_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)} - \frac{\phi_{sb}(y)\left(1+{}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}}\right)}{t_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)}$$

Now, on evaluating the constants d_1, d_2 and Eq. (4.2.1), the differential equation for surface potential can be obtained as:

$$\chi\frac{d^2\varphi_{sf}(y)}{dy^2} - \delta\varphi_{sf}(y) = \tau - y\sigma \qquad (4.2.4)$$

where

$$\chi = 1 + \frac{xC_{oxf}}{\varepsilon_{si}} - \frac{x^2\left(1+{}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}}\right)}{t_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)},\; \delta = \frac{2\left(1+{}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}}\right)}{t_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)},\; \sigma = \frac{2(\phi_{M_{b1}} - \phi_{M_{b2}})}{Lt_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)} + \frac{2(\phi_{M_{f1}} - \phi_{M_{f2}})\left({}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}}\right)}{Lt_{si}^2\left(1+{}^{2C_{si}}/_{C_{oxb}}\right)}$$

$$\tau = \frac{qN_{ch}}{\varepsilon_{si}} - \frac{2(V_{G_b} + \phi_{si})}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})} - \frac{2(V_{G_f} + \phi_{si})({}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}})}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})} + \frac{2\phi_{M_{b1}}}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})} + \frac{2\phi_{M_{f1}}({}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{si}})}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})}$$

The resulting differential equation given in Eq. (4.2.4) has now been solved to formulate an expression for the surface electrostatic potential in the silicon channel and is given as:

$$\varphi_{sf}(y) = A_1 e^{y\sqrt{{}^{\delta}/_{\chi}}} + A_2 e^{-y\sqrt{{}^{\delta}/_{\chi}}} + \frac{\sigma}{\delta} y - \frac{\tau}{\delta} \qquad (4.2.5)$$

To get the overall nature of the calculated surface potential, the coefficients A_1 and A_2 need to be calculated from the boundary conditions of 3 and 4 and given as:

$$A_2 = \frac{1}{2\sinh(L\sqrt{{}^{\delta}/_{\chi}})}\left[\frac{\sigma L}{\delta} + \frac{\tau}{\delta}\left(e^{L\sqrt{{}^{\delta}/_{\chi}}} - 1\right) - V_{DS} + V_{bi}\left(e^{L\sqrt{{}^{\delta}/_{\chi}}} - 1\right)\right]$$

and $A_1 = V_{bi} + \frac{\tau}{\delta} - A_2$

Till now, we have successfully evaluated an expression of front surface potential. However, to obtain a picture of the entire potential profile, a complete solution of the potential in the silicon channel is required at different channel depths (x).

Based on Tsormpatzoglou's approach presented in [4.43] (by substituting x=t_{Si}/n ; where $n \neq 0$), the overall channel potential expression of the proposed linearly graded asymmetric DG (LGADG) MOSFET can be obtained in terms of front surface potential and different channel depths and given as:

$$\varphi(x,y) = \varphi_{sf}(y)\left[1 + \frac{\varepsilon_{oxf}}{\varepsilon_{si}t_{oxf}}x - \frac{(1+{}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{Si}})}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})}x^2\right] - \left[\frac{\varepsilon_{oxf}}{\varepsilon_{si}t_{oxf}}V_{G_f}^{'}\right]x + \left[\frac{V_{G_b}^{'}}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})}\right]x^2 + \left[\frac{V_{G_f}^{'}({}^{C_{oxf}}/_{C_{oxb}} + {}^{C_{oxf}}/_{C_{Si}})}{t_{si}^2(1+{}^{2C_{si}}/_{C_{oxb}})}\right]x^2$$

(4.2.6)

It is quite evident from the final expression of total channel potential that it is a function of both x and y. Thus, the channel potential at different channel depths can be exactly determined by putting appropriate values of x for different channel depths (x=0 for surface potential; x= t_{si}/2 for mid potential and so on) in the above equation.

4.2.3.2. Threshold Voltage Modeling

Having formulated the final expression of total potential in the silicon channel, the position of minimum potential (y_{min}) can subsequently be obtained by calculating the first order derivative of potential and equating the resulting derivative to zero and can be expressed as:

$$y_{\min} = \frac{A_2\sqrt{\delta/\chi} - A_1\sqrt{\delta/\chi} - \sigma/\chi}{(A_1 + A_2)\,\delta/\chi} \tag{4.2.7}$$

The general expression for inversion charge in the channel region of undoped DG MOSFETs is known to have a nature as $Q_{inv} = \int_{x=0}^{x=t_{si}} n_i e^{\frac{\varphi(x,y_{\min})}{V_t}}\, dx$.

Studies show that the overall conduction in undoped/lightly doped DG MOSFETs is not confined to the channel center due the even spreading of free electrons in the lightly doped channel. Thus, the effective conducting path of the lightly doped device under consideration must lie somewhere between the surface and the center of the channel and it can be roughly approximated to be at $x=t_{si}/4$ from front surface-oxide interface [4.31-4.33]. Thus, the carrier sheet charge density Q_{thf} can be calculated by taking the integrand fixed at the value of $x=t_{Si}/4$ and written as:

$$Q_{thf} = n_i e^{\frac{q.\varphi(x=t_{Si}/4,\,y_{\min})}{kT}}\, t_{Si} \tag{4.2.8}$$

From the classical definition of front threshold voltage V_{THf} , it can be defined as the minimum front gate voltage V_{Gf} at which the density of carrier charge at the effective conductive path reaches a value Q_{thf} at which the device turns on. Considering the lightly doped device to operate in weak inversion, the effective conduction path can be assumed to be situated at a distance of $x=t_{Si}/4$ from the interface between the front gate-oxide and silicon channel [4.31-4.33, 4.35, 4.43]. Depending on this assumption, the simple analytical expression of front gate threshold voltage can be formulated from equation 4.2.8 and is given as:

$$V_{THf} = \frac{-\delta t_{si}^2\left(1+2C_{si}/C_{oxb}\right)}{2\chi\left(C_{oxf}/C_{si}+C_{oxf}/C_{oxb}\right)}\left[A_1 e^{y_{\min}\sqrt{\delta/\chi}} + A_2 e^{-y_{\min}\sqrt{\delta/\chi}} + \frac{\sigma y_{\min}}{\delta} - \frac{\chi}{\delta}\left[\frac{2\phi_{M_{b1}}}{t_{si}^2\left(1+2C_{si}/C_{oxb}\right)} + \frac{2\phi_{Mf_i}\left(C_{oxf}/C_{si}+C_{oxf}/C_{oxb}\right)}{t_{si}^2\left(1+2C_{si}/C_{oxb}\right)}\right] - V_t \ln\left(\frac{Q_{th}}{n_i t_{si}}\right)\right.$$
$$\left. - \frac{qN_{ch}\chi}{\delta\varepsilon_{si}} + \frac{2\chi\left(V_{G_b}+\phi_{si}\right)}{\delta t_{si}^2\left(1+2C_{si}/C_{oxb}\right)} + \frac{2\phi_{si}\chi\left(C_{oxf}/C_{si}+C_{oxf}/C_{oxb}\right)}{\delta t_{si}^2\left(1+2C_{si}/C_{oxb}\right)}\right] \tag{4.2.9}$$

The Drain Induced Barrier Lowering (DIBL) can be calculated as the difference between the threshold voltages at low and high values of drain bias as [4.35]-

$$DIBL = V_{TH}\left(V_{DS\_low} = 0.1V\right) - V_{TH}\left(V_{DS\_HIGH}\right)$$

4.2.4. Results and Discussions

The results and discussions subsection here presents a detailed insight into the asymmetric nature of the proposed Linearly Graded Asymmetric Double Gate (LGADG) MOS structure emphasizing on the comparative performance evaluation of the proposed LGADG MOS structure with respect to its normal DG equivalent based on the results obtained from exhaustive analytical modelling. Simulation data obtained from 2-D MEDICI simulator using the parameter values specified in Table 4.2.1 have also been shown to validate the accuracy of our proposed model.

Table 4.2.1: Parameters used for simulation

Parameter	**Substrate doping concentration (N_a)**	**Source/ Drain doping concentration ($N_{S/D}$)**	**Channel Length**	**Front Oxide thickness (t_{oxf})**	**Back Oxide thickness (t_{oxb})**	**Film thickness (t_{Si})**	$\phi_{M_{f1}}$	$\phi_{M_{f2}}$	$\phi_{M_{b1}}$	$\phi_{M_{b2}}$
Value	10^{20} m^{-3}	5 x $10^{25}m^{-3}$	40 nm	2 nm	6 nm	10 nm	5.3 eV	4.4 eV	4.8 eV	4.3 eV

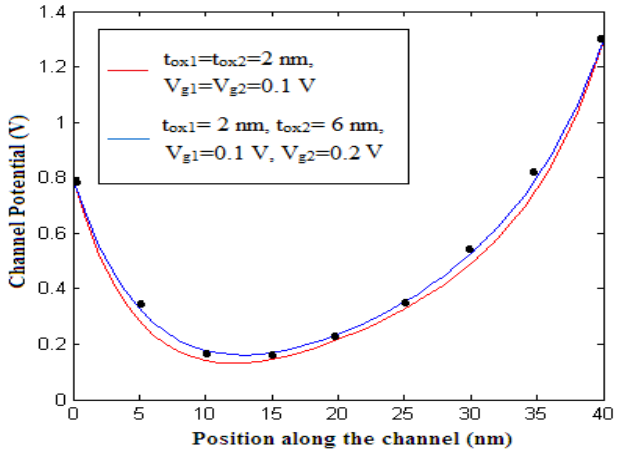


Fig. 4.2.2 Variation of channel potential along channel position of symmetric and asymmetric DG MOSFETs with different gate oxide thicknesses and gate biases. Simulation results are shown by symbols.

Careful observation of Fig. 4.2.2 indicates that inclusion of asymmetry in terms of gate oxide thicknesses and applied gate biases in a Double Gate MOSFET structure results in considerable performance improvement by shifting the channel potential profile upwards compared to its symmetric counterpart. To explore full asymmetricity in the proposed structure, all the device parameters in the front and back gate regions (variation in the gate oxide thickness, the supply voltages to both the gates and the linear variation in the work function at both the gate electrodes) are taken to be dissimilar.

The variation of channel potential along the channel position of the a DG MOSFET having linearly graded binary metal alloy gate electrode has been compared with a normal DG MOSFET having single metal gate electrode in Fig. 4.2.3. The figure also explores the effects of introducing asymmetry in both the structures.

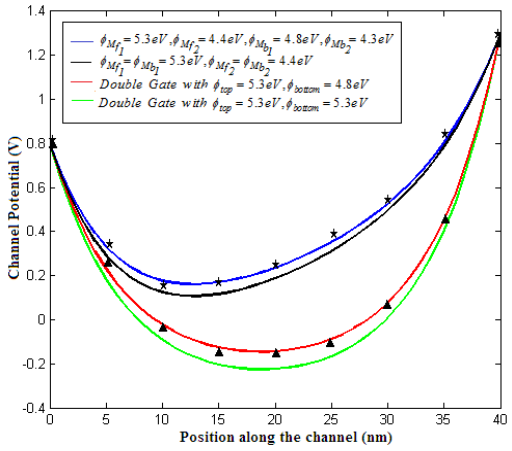


Fig. 4.2.3 Variation of channel potential along channel position of both symmetric and asymmetric DG MOSFET considering and without considering linearly graded binary metal alloy as the front and back gate electrodes. Simulation results are shown by symbols.

Studying the figure carefully, it can be easily understood that the asymmetric DG MOS having different gate metals in the front and back electrodes demonstrates improved performance while operating in nano regime. As the channel dimension is gradually scaled down, it can be observed from the figure that instead of being situated at the centre of the channel, the minima of channel potential gets gradually shifted more and more towards the source which is an obvious indication of better shielding of channel potential minima from any random drain bias variations ensuring remarkably superior short channel device performance. The blue line will always represent the default parameters of our proposed LGADG structure as listed in Table 4.2.1 unless otherwise mentioned.

In addition to this, it must also be noted that the potential minima of the Double Gate MOSFET with linearly graded binary metal alloy gate electrode has been shifted upwards compared to normal DG equivalent irrespective of the presence of asymmetry. Thus, it can be inferred that incorporation of a linearly graded gate electrode endows the proposed LGADG structure with significant performance improvement making it a viable alternative in subduing a multitude of harmful short channel effects like DIBL, Hot Carrier Effects, carrier velocity saturation, gate oxide charging etc. Moreover, notable improvement in the channel potential profile can be realized by simply varying the relative permittivities of both front and back gate oxides of the proposed linearly graded Double Gate structure with an intention to explore more asymmetricity by keeping the same front gate oxide permittivity and replacing the bottom gate oxide by air, resulting in a typical SON structure. This modification has been elucidated in Fig. 4.2.4 to substantiate the superiority of SON structure over SOI counterpart [4.44]. Going one step further, the normal silicon dioxide in the front gate oxide is now replaced with a high-k dielectric, resulting in an upward shift of channel potential, indicating the clear improvement in short channel behavior by dint of the inherent ability of a high-k dielectric to avoid oxide leakage [4.45]. It can thus be inferred that the channel potential profile of the proposed device shows a gradual improvement on continuously increasing the device asymmetricity.

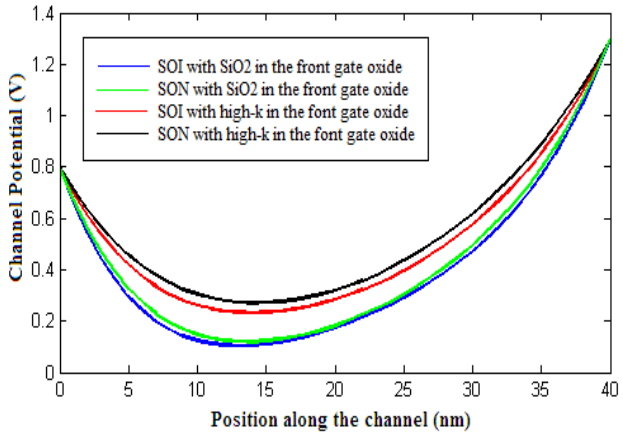


Fig. 4.2.4 Variation of channel potential along channel position of LGADG SOI and SON MOSFETs with and without high-k dielectric in the front gate oxide.

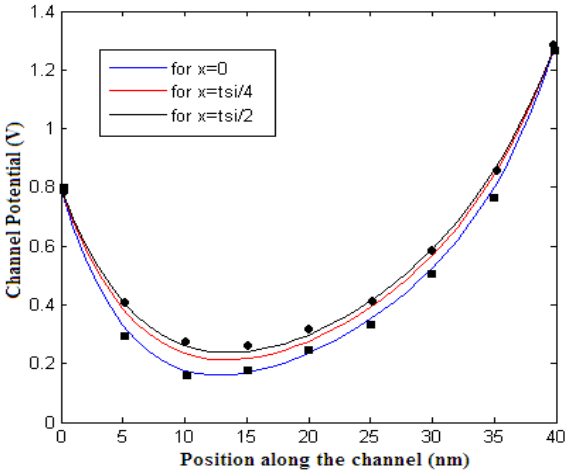


Fig. 4.2.5 Variation of channel potential along lateral channel position of LGADG MOSFET at different points along vertical (x) direction. Simulation results are shown by symbols.

The present work considers sub-nano regime operation where the gradual channel approximation is not valid and hence the channel potential is a function of both coordinates. Accordingly, the final expression of the analytical modeling investigated in this subsection presents the overall channel potential in terms of x and y coordinates. Variation of potential with channel position at different depths of silicon channel is illustrated in Fig. 4.2.5. Potential at x=0 signifies surface potential, potential at x=tsi/2 represent channel central potential and finally, potential at the point where effective inversion layer in this work has been considered (as already discussed), i.e. at x=tsi/4 [4.31-4.33] are shown individually in the said figure.

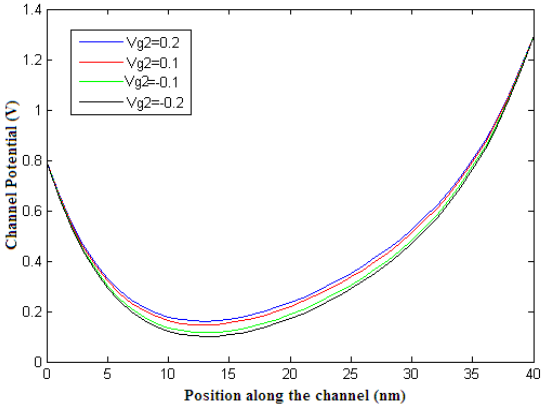


Fig. 4.2.6 Variation of channel potential along channel position of LGADG MOSFET considering different back gate biases

The figure above (Fig. 4.2.6) describes the variation of channel potential considering different back gate biases which exhibits a lowering of source-channel barrier potential with the gradual increase

in back gate bias as expected. Fig. 4.2.7 depicts the drain end channel electric field variation along the channel for symmetric and asymmetric DG MOSFET with and without linearly graded binary metal alloy as the front and back gate electrodes.

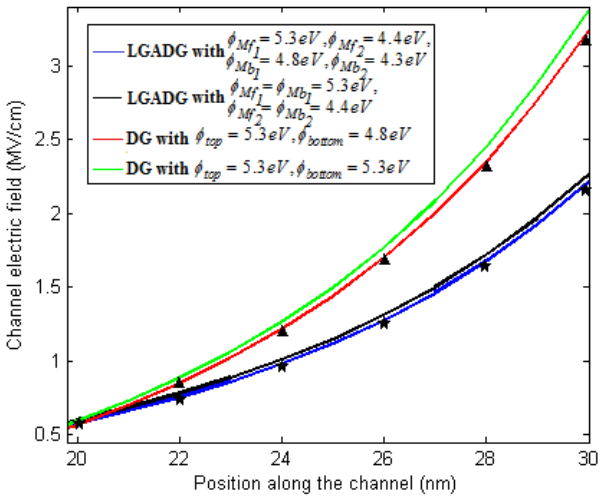


Fig. 4.2.7 Variation of channel electric field (towards drain side) along channel position of symmetric and asymmetric DG MOSFET with and without linearly graded binary metal alloy as the gate electrodes. Simulation results are shown by symbols.

It can be observed that the proposed asymmetric DG MOSFET with different gate metals in the front and back electrodes (blue line with default parameters) exhibits the lowest drain end peak electric field compared to the other equivalent symmetric DG structures (with or without linearly graded gate) which clearly indicates that the proposed asymmetric LGADG MOSFET far surpasses its equivalent structures in suppressing the drain electric field impact ionization induced Hot Carrier Effects (HCEs).

Till now, the channel potential profile of the proposed LGADG structure has been studied in sufficient detail depicting the LGADG MOSFET to give superior channel potential profile compared to equivalent symmetric structures. Thus, it can be expected from the ongoing trend that the threshold voltage of the proposed LGADG structure will also show significant improvement as compared to the conventional DG structure. With reference to this, the threshold voltage variations of LGADG structure considering different parameter values are now being studied. Fig. 4.2.8 shows considerable reduction in threshold voltage of the proposed structure with gradual increment in the bias applied to bottom gate which is attributed by a proportional lowering of the potential barrier existing at the source-channel junction. In addition to this, a reduction in channel thickness increases the overall gate control on the entire channel, which in turn reduces the device threshold voltage. This has been depicted in Fig. 4.2.9.

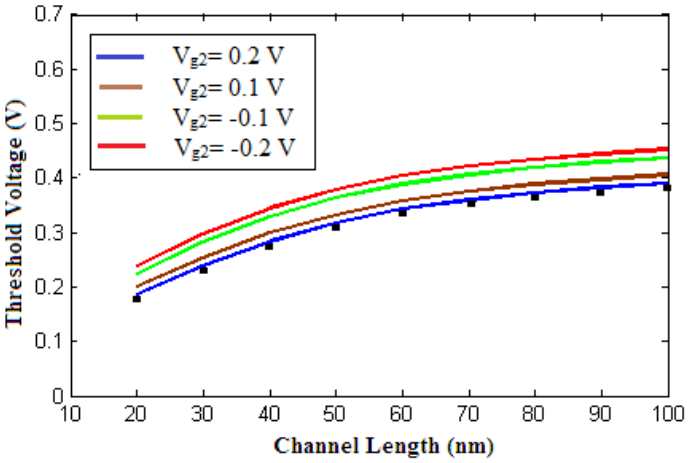


Fig. 4.2.8 Threshold voltage variation with channel length of LGADG MOSFET considering different back gate biases. Simulation results are shown by symbols.

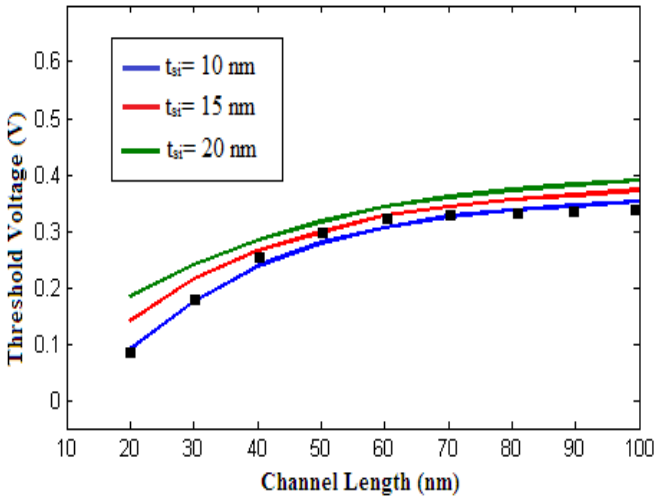


Fig. 4.2.9 Threshold voltage variation with channel length of LGADG MOSFET considering different channel thicknesses. Simulation results are shown by symbols.

The entire subsection has been dedicated to substantiate the efficacy of the proposed LGADG structure in exhibiting better immunity to short channel effects, which is again proved by the comparative analysis of our proposed asymmetric LGADG MOSFET with a normal symmetric DG MOSFET in terms of DIBL presented in Fig. 4.2.10. It can be easily inferred from the said figure that for shorter channel lengths, the proposed LGADG MOSFET shows significant reduction in the

DIBL value as compared to its normal DG equivalent.

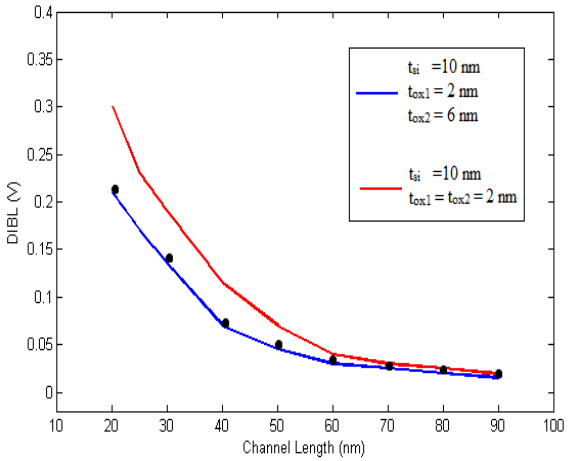


Fig. 4.2.10 DIBL variation with channel length L of normal DG and LGADG MOSFETs. Simulation results are shown by symbols.

In order to have some idea about the I-V behavior of the proposed LGADG device, both transfer and drain characteristics are detailed in Figs. 4.2.11 and 4.2.12 respectively.

The analytical results of our proposed LGADG MOS structure closely resembles the MEDICI simulated results, thereby ensuring the accuracy of the proposed mathematical model.

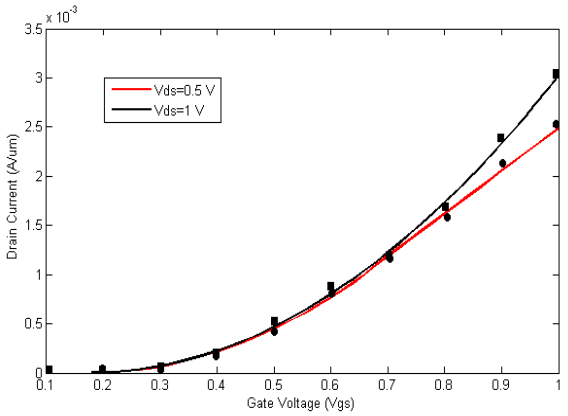


Fig. 4.2.11 Transfer characteristics of LGADG MOSFET. Simulation results are shown by symbols.

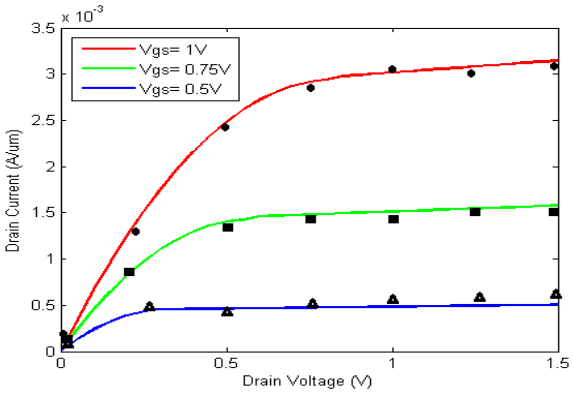


Fig. 4.2.12 Drain characteristics of LGADG MOSFET. Simulation results are shown by symbols.

4.3 Cylindrical MOSFET with Linearly Graded Binary Metal Alloy Gate: an analytical approach to study improved short channel device characteristics

4.3.1. Overview and recent research trend

The preceding section of this chapter has presented an in depth analytical surface potential and threshold voltage modeling of a Double Gate MOSFET structure incorporating the novel concept of 'work function engineered' gate electrode in order to study the impact of asymmetric device parameters and structural dimensions on overall performance of the device. It has already been discussed that the shortcomings of conventional planar MOSFET structure can be alleviated by using the Double Gate (DG) devices based on the concept of volume inversion, leading to an enhanced current drivability and higher transconductance due to excellent gate control over the channel by dint of having two gates, both of them controlling carrier conduction through the channel. In spite of these advantages, the practical use of DG MOSFETs is limited by high fabrication cost and associated process complexity [4.46-4.49]. Thus, to mitigate the problems associated with Double Gate MOSFETs and to enhance the scalability of low dimensional devices to a further extent, several other non-conventional devices have been gaining research interest out of which surrounding gate devices have been gaining significant research interest by dint of their unique feature of gate wrapped channel. The most fascinating feature of the surrounding gate MOSFETs lies in its novel device geometry which significantly enhances the device packing density along with providing a host of advantages. The surrounding gate electrode encircling the channel on all sides facilitates an enhanced electrostatic control over the channel conduction and results in remarkable improvement in device sub-threshold behavior and better suppression of unwanted Short Channel Effects (SCEs) in sharp contrast with conventional single and double gate counterparts. This unique feature has

attracted many to pursue their research activities with an aim to investigate the superiority of surrounding gate MOSFETs [4.50-4.52]. The gate wrapping may again be of two types:

1. **Cylindrical channel cross section:** In this case, the conducting channel is cylindrical in cross section and the surrounding gate is naturally a cylindrical gate wrapping the entire channel.

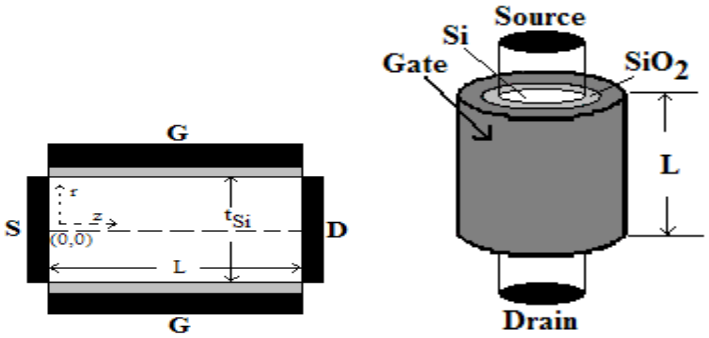
2. **Rectangular/square channel cross section:** In this case, the conducting channel can either be rectangular or square in cross section and the surrounding gate is naturally a quadruple gate wrapping the entire channel.

In this section, a surrounding gate MOSFET with cylindrical channel cross section i.e. a cylindrical gate MOSFET device will be considered where the innovative pioneering concept of 'work function engineering' is incorporated by using a binary metal alloy as the gate electrode surrounding the entire cylindrical channel resulting in the proposed Work Function Engineered Gate (WFEG) Cylindrical MOSFET. This enables to reap the dual benefits of both the surrounding gate architecture along with the work function engineering achieved by the introduction of binary metal alloy as gate material. The binary alloy metal gate considered here has two metals, Platinum (Pt) and Tantalum (Ta) with pure constituent work functions of 5.3 eV and 4.4 eV respectively. The fabrication feasibility of such binary metal alloy work function engineered gate electrode has already been discussed in sufficient details in the preceding sub section. Motivated by the possibility of fabricating such an unique gate electrode, a cylindrical cross section surrounding gate MOSFET has been considered and a two dimensional Poisson's equation has been solved in the cylindrical co-ordinate system at the onset of inversion to study the surface potential distribution in the ultra thin cylindrical silicon channel. An analytical surface potential modeling based threshold voltage calculation has also been presented.

4.3.2. Analytical modeling

The figure below illustrates the cross-sectional view of a Cylindrical/ Surrounding gate MOSFET with a binary metal alloy as gate electrode. As the device cross section considered is cylindrical, the entire analytical formulation starting from the Poisson's equation needs to be considered in cylindrical coordinate system having a radial direction 'r' and a horizontal direction 'z'. The device structure is assumed to be symmetrical such that the potential and electric field in the channel will not vary along the angular direction. Depending on this particular assumption, the angular direction of the cylindrical coordinate system can be neglected for the sake of mathematical brevity reducing the three dimensional scenario into a two dimensional one by neglecting the angular component in

cylindrical Poisson's equation. This makes a two dimensional approach suitable for the analytical modeling of the present device structure [4.53-4.55]:



(a) (b)

Fig.4.3.1. (a) Cross-sectional view of WFEG Cylindrical MOSFET along x-axis (b) Overall device structure.

As the gate electrode of the proposed WFEG cylindrical MOSFET is assumed to have a linearly composition graded binary metal alloy, the effective work function expression for the metal alloy gate electrode can be expressed as [4.25]:

$$\phi_{meff}(z) = (z/L)\phi_2 + (1-z/L)\phi_1 \tag{4.3.1}$$

Where ϕ_1 and ϕ_2 are the pure constituent work functions of metals Pt and Ta respectively and horizontal component z is normalized with channel length.

4.3.2.1. Surface Potential Modeling

The initial step towards formulation of a expression for the proposed Work Function Engineered Gate Cylindrical MOSFET (WFEG CG MOS) is the solution of a 2D Poisson's equation (in cylindrical coordinate system neglecting the angular coordinate) considering Young's parabolic potential approximation [4.42] given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi(r,z)}{\partial r}\right)+\frac{\partial^2\varphi(r,z)}{\partial z^2}=\frac{qn_i}{\varepsilon_{Si}}\left(e^{\beta\varphi(r,z)}\right) \tag{4.3.2}$$

where $\varphi(r,z)$ is the 2-D channel potential profile, n_i is the intrinsic doping concentration in the almost undoped channel, and ε_{Si} is the silicon permittivity. The parabolic potential profile in the channel along the radial direction can be written as:

$$\varphi(r,z) = \varphi_f(z) + d_1(z)r + d_2(z)r^2 \quad \text{for} \quad 0 \le z \le L; 0 \le r \le {t_{Si}}/{2} \tag{4.3.3}$$

where $\varphi_f(z)$, $d_1(z)$ and $d_2(z)$ are the functions of z only.

As discussed in the previous chapters, the analytical modeling of the proposed device mandates the solution of two dimensional Poisson's equation by considering proper boundary conditions listed as [4.56]:

i. The surface potential in the channel region can be written as:

$$\varphi_s(z) = \varphi(r = R, z)$$

Where, R represents device radius ($R = t_{Si}/2$).

ii. The potential at the source end of the channel can be written as:

$$\varphi(r = R, z = 0) = \varphi_s(z)\big|_{z=0} = V_{bi}$$

iii. The potential at the drain end of the channel can be written as:

$$\varphi(r = R, z = L) = \varphi_s(z)\big|_{z=L} = V_{bi} + V_{DS}$$

iv. The channel central potential can be written as:

$$\varphi_C(z) = \varphi(r = 0, z)$$
$$\therefore \varphi_C(z) = \varphi_f(z)$$

v. The channel central electric field can be written as:

$$\left.\frac{d\varphi(r,z)}{dr}\right|_{r=0} = 0 \Rightarrow d_1(z) = 0$$

vi. The surface electric field in the channel region can be written as:

$$\left.\frac{d\varphi(r,z)}{dr}\right|_{r=R} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\left[\frac{V_{GS}^{'} - \varphi_s(z)}{t_{eq}}\right]$$

where $V_{GS}^{'} = V_{GS} - V_{FBeff}$ and $t_{eq} = 0.5t_{Si}\ln\left(1 + {2t_{ox}}/{t_{Si}}\right)$, where V_{FBeff} signifies the flat band voltage of the binary metal alloy gate and is given by $V_{FBeff} = \phi_{meff}(z) - \phi_{Si}$.

Rewriting equation (4.3.3) and differentiating $\varphi(r,z)$ w.r.t. 'r',

$$\frac{d\varphi(r,z)}{dr} = 0 + 0 + 2d_2(z)r$$

Again from boundary condition (vi), $\left.\frac{d\varphi(r,z)}{dr}\right|_{r=R} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\left[\frac{V_{GS}^{'} - \varphi_s(z)}{t_{eq}}\right]$

The above two equations can be solved to get the value of $d_2(z)$ as $d_2(z) = \frac{C_{eq}}{2R\varepsilon_{Si}}\left(V_{GS}^{'} - \varphi_s(z)\right)$

Where $C_{eq} = {\varepsilon_{ox}}/{t_{eq}}$

Rigorous mathematical calculations considering the above mentioned boundary conditions results in the expression of overall potential in the silicon channel and is given as:

$$\varphi(r,z) = \varphi_C(z) + \frac{C_{eq}}{t_{Si}\varepsilon_{Si}}\left(V_{GS}^{'} - \varphi_S(z)\right)r^2 \qquad (4.3.4)$$

Now, substituting equation (4.3.4) in the cylindrical Poisson's equation we can write

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi(r,z)}{\partial r}\right)+\frac{\partial^2\varphi(r,z)}{\partial z^2}=\frac{qn_i}{\varepsilon_{Si}}\left(e^{\beta\varphi(r,z)}\right)$$

$$\Rightarrow\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{2rC_{eq}}{2R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))\right)+\frac{\partial}{\partial z}\left[\varphi_C^{'}(z)-\frac{C_{eq}r^2}{2R\varepsilon_{Si}}\varphi_s^{'}(z)\right]=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$

$$\Rightarrow\frac{1}{r}\left(2r\frac{C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))\right)+\left[\varphi_C^{''}(z)-\frac{C_{eq}r^2}{2R\varepsilon_{Si}}\varphi_s^{''}(z)\right]=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$

$$\Rightarrow\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))+\varphi_C^{''}(z)-\frac{C_{eq}r^2}{2R\varepsilon_{Si}}\varphi_s^{''}(z)=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)} \tag{4.3.5}$$

Now, at r=R,

$$\varphi_S(z)=\varphi(r,z)\big|_{r=R}=\varphi_C(z)+0+d_2(z)R^2$$
$$\Rightarrow\varphi_S(z)=\varphi_C(z)+d_2(z)R^2$$
$$\Rightarrow\varphi^{''}{}_S(z)=\varphi^{''}{}_C(z)+d_2^{''}(z)R^2$$

Substituting the value if $d_2(z)$,

$$\varphi^{''}{}_S(z)=\varphi^{''}{}_C(z)-\frac{C_{eq}}{2R\varepsilon_{Si}}\varphi^{''}{}_S(z)R^2$$
$$\Rightarrow\varphi^{''}{}_C(z)=\varphi^{''}{}_S(z)+\frac{C_{eq}R}{2\varepsilon_{Si}}\varphi^{''}{}_S(z)$$

Putting the obtained expression of center potential in terms of surface potential in Eq. 4.3.5,

$$\Rightarrow\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))+\varphi_C^{''}(z)-\frac{C_{eq}r^2}{2R\varepsilon_{Si}}\varphi_s^{''}(z)=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$
$$\Rightarrow\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))+\varphi^{''}{}_S(z)+\frac{C_{eq}R}{2\varepsilon_{Si}}\varphi^{''}{}_S(z)-\frac{C_{eq}r^2}{2R\varepsilon_{Si}}\varphi_s^{''}(z)=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$
$$\Rightarrow\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))+\varphi^{''}{}_S(z)\left[1+\frac{C_{eq}R}{2\varepsilon_{Si}}-\frac{C_{eq}r^2}{2R\varepsilon_{Si}}\right]=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$

In order to find an expression for surface potential, r must be replaced by R in the above equation and can be written as:

$$\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))+\varphi_S^{''}(z)\left[1+\frac{C_{eq}R}{2\varepsilon_{Si}}-\frac{C_{eq}R^2}{2R\varepsilon_{Si}}\right]=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$

$$\Rightarrow \varphi_S^{''}(z)+\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$

$$\Rightarrow \frac{d^2\varphi_S(z)}{dz^2}+\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}^{'}-\varphi_S(z))=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)} \quad (4.3.6)$$

$$\Rightarrow \frac{d^2\varphi_S(z)}{dz^2}+\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}-V_{FBeff}-\varphi_S(z))=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)}$$

$$\Rightarrow \frac{d^2\varphi_S(z)}{dz^2}+\frac{2C_{eq}}{R\varepsilon_{Si}}(V_{GS}-(\phi_{meff}(z)-\phi_{Si})-\varphi_S(z))=\frac{qn_i}{\varepsilon_{Si}}e^{\beta\varphi_s(z)} \quad (4.3.7)$$

Eq. 4.3.7 can be further simplified by neglecting higher order terms of the expanded exponential series to obtain the resulting differential equation of channel surface potential as:

$$\frac{d^2\varphi_S(z)}{dz^2}-\alpha^2\varphi_S(z)=\frac{qn_i}{\varepsilon_{Si}}+\xi\phi_{meff}(z)-\xi V_{GX} \quad (4.3.8)$$

Where $\xi=\frac{2C_{ox}}{R\varepsilon_{Si}}$, $\alpha=\sqrt{\zeta+{qn_i\beta}/{\varepsilon_{Si}}}$, $V_{GX}=V_{GS}+\phi_{Si}$ and $\beta={q}/{k_bT}$

Now, the solution of this simple differential equation (eq. 4.3.8) produces the final expression for channel surface potential which can be represented as:

$$\varphi_S(z)=\lambda_1e^{\alpha z}+\lambda_2e^{-\alpha z}+\left\{\xi\left(\frac{\phi_1-\phi_2}{\alpha^2}\right)\right\}({z}/{L})+\left(\frac{1}{\alpha^2}\right)\left[\xi V_{GX}-\xi\phi_1-\frac{qn_i}{\varepsilon_{Si}}\right] \quad (4.3.9)$$

Where λ_1 and λ_2 are the two coefficients which can be calculated using the boundary conditions at the source and drain ends (boundary conditions ii and iii) and are given as:

$$\lambda_1 = \frac{V_{DS} + V_{bi}(1-e^{-\alpha L}) - \left\{\frac{\xi(\phi_1-\phi_2)}{\alpha^2}\right\} - \left[\left(\frac{1}{\alpha^2}\right)\left(\xi V_{GX} - \xi\phi_1 - \frac{qn_i}{\varepsilon_{Si}}\right)\right]\left(1-e^{-\alpha L}\right)}{\left(e^{\alpha L} - e^{-\alpha L}\right)}$$

$$\lambda_2 = \frac{\left[\left(\frac{1}{\alpha^2}\right)\left(\xi\phi_1 + \frac{qn_i}{\varepsilon_{Si}} - \xi V_{GX}\right)\right]\left(e^{\alpha L} - 1\right) + \left\{\frac{\xi(\phi_1-\phi_2)}{\alpha^2}\right\} + V_{bi}(e^{\alpha L} - 1) - V_{DS}}{\left(e^{\alpha L} - e^{-\alpha L}\right)}$$

4.3.2.2. Threshold Voltage Modeling

It is well known from the classical definition that threshold voltage of a device corresponds to that particular gate voltage at which the value of surface potential equals twice of Fermi potential. However, the threshold voltage of the cylindrical gate MOSFET cannot be accurately determined by the above mentioned conventional concept of threshold voltage because of the cylindrical nature of device cross-section. An alternative approach of volumetric inversion is adopted for calculating the threshold voltage of the cylindrical structure where threshold voltage (V_{TH}) is considered to be the value of applied gate voltage which causes the volumetric inversion charge density (Q_{inv}) to reach the specified threshold value of $Q_{TH} \sim 10^{16}$ /m² [4.53-4.54].

The expression for volumetric inversion charge density can be written as [4.53]:

$$\begin{aligned} Q_{inv} &= 2\int_0^{r_0} n_i e^{\beta\varphi_{\min}(r,z)} dr \\ \Rightarrow \int_0^{r_0} \varphi_{\min}(r,z) dr &= \frac{1}{\beta}\ln\left(\frac{Q_{inv}}{2n_i}\right) \end{aligned} \tag{4.3.10}$$

The position of channel potential minima i.e. the virtual cathode position can be obtained by equating the first order derivative of channel surface potential to zero.

$$\begin{aligned} &\left.\frac{d\varphi_S(z)}{dz}\right|_{z=z_{\min}} = 0 \\ &\Rightarrow \alpha\lambda_1 e^{\alpha z_{\min}} - \alpha\lambda_2 e^{-\alpha z_{\min}} + \frac{\xi(\phi_1-\phi_2)}{\alpha^2 L} = 0 \end{aligned} \tag{4.3.11}$$

Simplification of eq. 4.3.11 yields the expression for virtual cathode position as:

$$z_{\min} = \frac{\left[\frac{\xi(\phi_1-\phi_2)}{(\alpha^2 L)} - \alpha(\lambda_1-\lambda_2)\right]}{\alpha^2(\lambda_1+\lambda_2)} \tag{4.3.12}$$

Substituting the value of z_{min} in the expression of channel surface potential gives the expression for minimum surface potential which can be written as:

$$\varphi_{S_{\min}}(z) = \lambda_1 e^{\alpha z_{\min}} + \lambda_2 e^{-\alpha z_{\min}} + \left\{\xi\left(\frac{\phi_1-\phi_2}{\alpha^2}\right)\right\}\left(z_{\min}/L\right) + \left(\frac{1}{\alpha^2}\right)\left[\xi V_{GX} - \xi\phi_1 - \frac{qn_i}{\varepsilon_{Si}}\right] \tag{4.3.13}$$

Eq. 4.3.4 can be modified to give the final expression of total channel potential given as:

$$\varphi(r,z) = \varphi_C(z) + \frac{C_{eq}}{t_{Si}\varepsilon_{Si}}\left(V_{GS}^{'} - \varphi_S(z)\right)r^2$$

$$\varphi(r,z)\big|_{r=R} = \varphi_S(z) = \varphi_C(z) + \frac{C_{eq}}{2R\varepsilon_{Si}}\left(V_{GS}^{'} - \varphi_S(z)\right)R^2$$

Now, at r=R, $\Rightarrow \varphi_C(z) = \varphi_S(z) - \frac{C_{eq}}{2R\varepsilon_{Si}}\left(V_{GS}^{'} - \varphi_S(z)\right)R^2$

$$\Rightarrow \varphi_C(z) = \varphi_S(z)\left[1 + \frac{C_{eq}}{2\varepsilon_{Si}}\right] - \frac{C_{eq}R^2}{2R\varepsilon_{Si}}V_{GS}^{'}$$

Substituting the expression of center potential in terms of surface potential eq. 4.3.4 can again be written as:

$$\begin{aligned}\varphi(r,z) &= \varphi_S(z)\left[1 + \frac{C_{eq}R}{2\varepsilon_{Si}}\right] - \frac{C_{eq}R^2}{2R\varepsilon_{Si}}V_{GS}^{'} + \frac{C_{eq}r^2}{2R\varepsilon_{Si}}V_{GS}^{'} - \frac{C_{eq}r^2}{2R\varepsilon_{Si}}\varphi_S(z) \\ \Rightarrow \varphi(r,z) &= \varphi_S(z)\left[1 + \frac{C_{eq}R}{2\varepsilon_{Si}} - \frac{C_{eq}r^2}{2R\varepsilon_{Si}}\right] + V_{GS}^{'}\left[\frac{C_{eq}r^2}{2R\varepsilon_{Si}} - \frac{C_{eq}R^2}{2R\varepsilon_{Si}}\right]\end{aligned} \tag{4.3.14}$$

At r=R/2, surface potential becomes the minimum surface potential. Thus eq. 4.3.14 can be re written as:

$$\varphi(R/2, z) = \varphi_{S_{\min}}(z)\left[1 + \frac{C_{eq}R}{2\varepsilon_{Si}} - \frac{C_{eq}R^2}{8R\varepsilon_{Si}}\right] + V_{GS}^{'}\left[\frac{C_{eq}R^2}{8R\varepsilon_{Si}} - \frac{C_{eq}R^2}{2R\varepsilon_{Si}}\right] \tag{4.3.15}$$

Substituting eq. 4.3.15 into eq. 4.3.10,

$$\varphi_{S_{\min}}(z)\left[1+\frac{C_{eq}R}{2\varepsilon_{Si}}-\frac{C_{eq}R^2}{8R\varepsilon_{Si}}\right]+V_{GS}^{'}\left[\frac{C_{eq}R^2}{8R\varepsilon_{Si}}-\frac{C_{eq}R^2}{2R\varepsilon_{Si}}\right]=\frac{1}{\beta}\ln\left(\frac{Q_{inv}}{2n_i}\right) \tag{4.3.16}$$

Eq. 4.3.16 can be further modified by performing relevant substitutions and simplifications to yield the final expression for threshold voltage as:

$$V_{TH}=\frac{v_T\ln\left(\frac{Q_{TH}}{2n_i}\right)-\varphi_{S\min}(z)\left\{1+\frac{3C_{eq}t_{Si}}{16\varepsilon_{Si}}\right\}-\frac{3C_{eq}t_{Si}}{16\varepsilon_{Si}}V_{FBeff}}{\left(\frac{3C_{eq}t_{Si}}{16\varepsilon_{Si}}\right)\left(1-\frac{\xi}{\alpha^2}\right)+\frac{\xi}{\alpha^2}} \tag{4.3.17}$$

The Drain Induced Barrier Lowering (DIBL) can be conventionally calculated as the difference between the threshold voltages at low (say at V_{DS}=0.1 V) and high values (say at V_{DS}=0.5 V, 1.0 V) of drain bias as-

$$DIBL=V_{TH}\left(V_{DS}=0.1V\right)-V_{TH}\left(V_{DS\_HIGH}\right) \tag{4.3.18}$$

4.3.2.3. Drain Current Modeling

The proposed device under consideration has its physical channel dimension in nano regime. Thus, the drain characteristic of the device is expected to be affected by unwanted short channel effects (SCEs). This demands the prior consideration of various SCEs like Channel Length Modulation (CLM) effect, field dependent mobility etc. to derive an exact drain current model of the proposed WFEG cylindrical MOSFET operating in sub-nano regime.

The simplified final expressions for drain current can be formulated as [4.25]:

$$I_{DS}=\frac{\pi t_{Si}\mu_{neff}C_{eq}}{L\left\{1-\left(l_c/L\right)+\frac{V_{DS}}{LE_C}\right\}}[(V_{GS}-V_{TH})V_{DS}-0.5V_{DS}^2] \quad \text{(In linear region)} \tag{4.3.19}$$

$$I_{DS}=\frac{\pi t_{Si}\mu_{neff}C_{eq}}{\left\{1-\left(l_c/L\right)+\frac{V_{DS,sat}}{LE_C}\right\}}[(V_{GS}-V_{TH})V_{DS,sat}-0.5V_{DS,sat}^2] \quad \text{(In saturation region)} \tag{4.3.20}$$

Where E_C is the critical electric field at which the electron velocity v_{sat} saturates and $V_{DS,sat}$ is the saturation voltage and μ_{neff} is the effective field dependant mobility are given as-

$$E_C = \frac{2v_{sat}}{\mu_{neff}} \qquad V_{DS,sat} = \frac{V_{GS} - V_{TH}}{1 + \frac{V_{GS} - V_{TH}}{LE_C}}$$

$$\mu_{neff} = \frac{\mu_{n0}}{1 + \kappa\left(V_{GS} - V_{TH}\right)}$$

Where μ_{n0} is the low field mobility and κ is the fitting parameter [4.57].

Having the CLM incorporated expressions of drain current in linear and saturation regions of operation, the Drain conductance and transconductance of WFEG CG MOS structure can be formulated by differentiating the drain current w.r.t drain to source voltage, V_{DS} (keeping V_{GS} constant) and gate to source voltage, V_{GS} (keeping V_{DS} constant) respectively and their expressions are given as-

$$g_{d,Lin} = \frac{\pi t_{Si}\mu_{neff}C_{eq}}{L}\left[\frac{\frac{\left(V_{GS} - V_{TH} - V_{DS}\right)}{\left\{1 - \left(l_c/L\right) + \frac{V_{DS}}{LE_C}\right\}} + \left(dl_c/dV_{DS} - 1/E_c\right)\left\{\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right\}}{L\left\{1 - \left(l_c/L\right) + \frac{V_{DS}}{LE_C}\right\}^2}\right] \qquad \text{(In Linear Region)} \qquad (4.3.21)$$

$$g_{d,sat} = \frac{\pi t_{Si}\mu_{neff}C_{eq}}{L^2}\left[\frac{\left(dl_c/dV_{DS} - 1/E_c\right)\left\{\left(V_{GS} - V_{TH}\right)V_{DS,sat} - \frac{1}{2}V_{DS,sat}^2\right\}}{\left\{1 - \left(l_c/L\right) + \frac{V_{DS,sat}}{LE_C}\right\}^2}\right] \qquad \text{(In saturation region)} \qquad (4.3.22)$$

$$g_{m,Lin} = \frac{\pi t_{Si}\mu_{neff}C_{eq}}{L\left\{1-\left(l_c/L\right)+\frac{V_{DS}}{LE_C}\right\}}V_{DS} \quad \text{(In Linear Region)} \quad (4.3.23)$$

$$g_{m,sat} = \frac{\pi t_{Si}\mu_{neff}C_{eq}}{L\left\{1-\left(l_c/L\right)+\frac{V_{DS,sat}}{LE_C}\right\}}V_{DS,sat} \quad \text{(In Saturation Region)} \quad (4.3.24)$$

4.3.3 Results & Discussions

The results and discussions sub section presents a comparative performance analysis based on analytical modeling and simulation results of the proposed WFEG CG with respect to its normal CG equivalent without considering work function engineered gate electrode. The 2-D MEDICI simulator data have also been provided to validate the accuracy of the mathematical modeling presented. In both the cases, simulation has been carried out with the parameter values as listed in Table 4.3.1.

Table 4.3.1. Parameters used for simulation

Parameter	**Substrate doping concentration (N_{SUB})**	**Source/ Drain doping concentration ($N_{S/D}$)**	**Channel Length**	**Front Oxide thickness (t_{ox})**	**Film thickness (t_{Si})**	μ_{n0}	v_{sat}	κ
Value	10^{21} m^{-3}	$10^{26} m^{-3}$	70 nm	2 nm	20 nm	$\sim 0.11 m^2/V-s$	$10^5 m/s$	0.02

The most unique feature of using a linearly graded binary metal alloy as gate electrode has been shown in Fig. 4.3.2 where the parabolic symmetry of the surface potential profile of the WFEG CG MOSFET is affected with the gradual reduction of device dimension into nano regime in contrast to the almost symmetrical parabolic surface potential profile of its normal CG counterpart. This particular asymmetry in surface potential profile results in an effective shift of surface potential minima towards the source side instead of being situated at the mid position along silicon channel as evident from Fig. 4.3.2. This shift practically screens the surface potential minima from any variation in drain bias, thereby mitigating adverse DIBL effects. Moreover, the potential minima of

WFEG MOS is clearly seen to be higher than that of CG equivalent which is an obvious indication of the superiority of the proposed WFEG CG MOS over its CG equivalent in mitigating several SCEs.

Fig. 4.3.3 depicts the channel electric field variation with position along the channel near the drain end for both WFEG CG and normal CG MOSFET structures. It can be observed from the figure that the peak electric field near the drain end, which is the prime factor for initiating impact ionization induced Hot Carrier Effect in nano dimensional devices, is significantly reduced for the proposed WFEG CG structure compared to its normal CG equivalent. This reduction in peak drain electric field in WFEG structure is attributed to the careful adjustment of gate electrode workfunction by suitably varying the composition of the binary metal alloy used, thereby making the proposed WFEG CG MOSFET much more immune to HCEs.

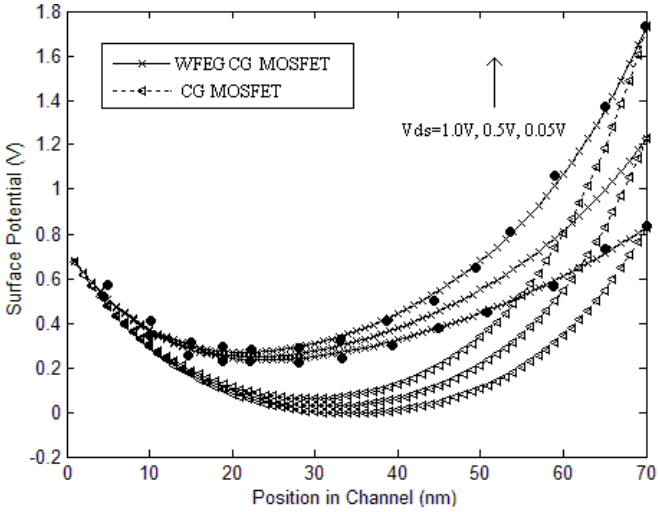


Fig. 4.3.2. Variation of surface potential along the channel position of WFEG CG and normal CG MOSFET having channel length of 70nm at a constant gate bias of 0.1V. Circular dots represent MEDICI simulated results of WFEG CG structure.

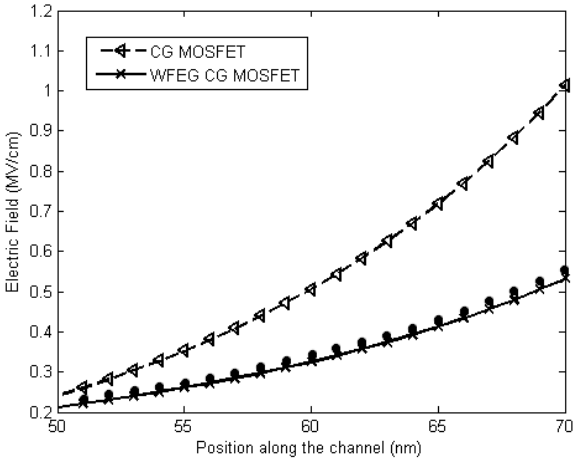


Fig. 4.3.3. Variation of electric field along the channel position of WFEG CG and normal CG MOSFET having channel length of 70nm at a constant gate bias of 0.1V. Circular dots represent MEDICI simulated results of WFEG CG structure.

Fig. 4.3.4 depicts the nature of threshold voltage variation with channel length for both WFEG CG MOSFET and normal CG counterpart having no structural or doping modifications. The asymmetric nature of surface potential profile makes the proposed WFEG CG structure more immune to SCEs. This results in an obvious reduction in threshold voltage roll-off (TVRO) in the WFEG structure under study as visible from Fig. 4.3.4.

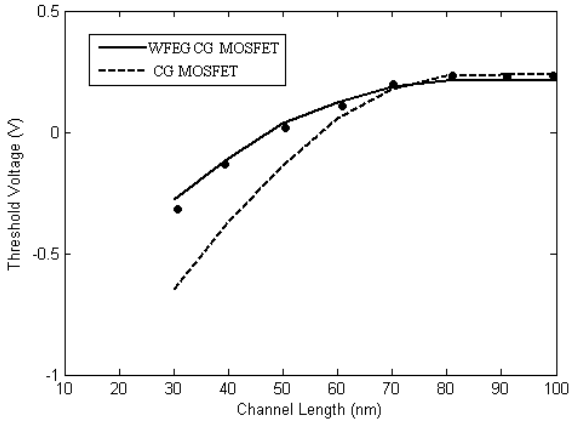


Fig. 4.3.4 Variation of threshold voltage, V_{TH} with channel length L for WFEG CG and normal CG MOSFET structures (V_{GS}=0.1V and V_{DS}=0.1 V) with same values of parameters as in table. 4.3.1. Circular dots have the same significance as in Fig. 4.3.2.

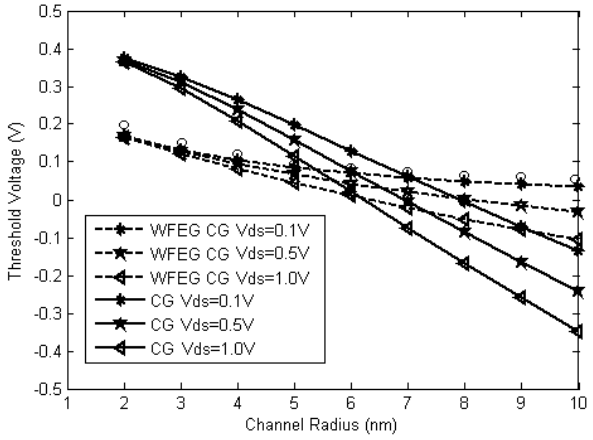


Fig. 4.3.5 Variation of threshold voltage, V_{TH} with channel radius (t_{si}/2) for WFEG CG and normal CG MOSFET structures (V_{GS}=0.1V) with same values of parameters as in table. 4.3.1. Circular symbols represent MEDICI simulated results of WFEG CG structure.

The main reason behind this improved TVRO behavior is the continuous adjustment of the mole fraction of the constituent metals of the gate electrode binary metal alloy system spatially from the source towards drain. Threshold voltage variation with the channel radius at a constant channel dimension of 50nm is now being shown in Fig. 4.3.5. As the channel radius is reduced, the threshold voltage of proposed WFEG CG MOSFET shows almost constant nature indicating that the threshold voltage instability with channel radius is much lower for WFEG CG compared to normal CG equivalent, establishing the proposed WFEG CG structure as a suitable alternative to conventional CG MOS in suppressing unwanted SCEs in deep sub-micron domain.

Now, the variation of DIBL with respect to the channel length is shown in Fig. 4.3.6 considering both WFEG CG and normal CG MOSFETs for two different values of applied drain voltages. The Drain Induced Barrier Lowering (DIBL) is simply the difference between the device threshold voltages considered at a low and a high value of drain bias respectively and can be mathematically expressed as: $DIBL = V_{TH_{low}} - V_{TH_{high}}$. Thus, increasing the drain bias will result in a proportional increase in DIBL as evident from the said figure. However, it must also be noted that DIBL of the WFEG CG MOS structure is less than that of its CG counterpart confirming the superiority of the proposed device structure.

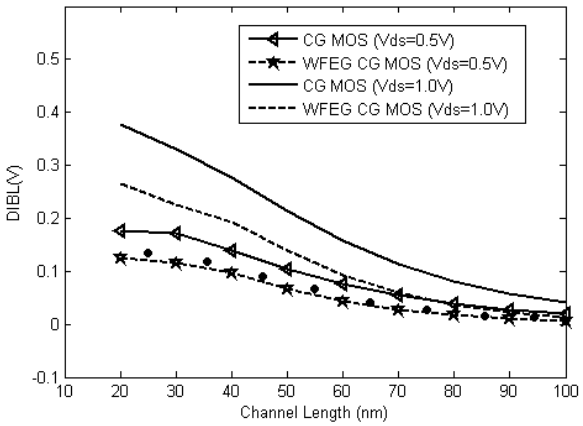


Fig 4.3.6. Variation of DIBL with respect to channel length for WFEG CG and normal CG MOSFET structures. Circular symbols represent MEDICI simulated results.

Having explored the surface potential and threshold voltage based comparative analysis of the proposed WFEG CG MOSFET in the previous figures, Fig. 4.3.7 shows the variation of drain current against drain to source voltage with gate to source voltage as a parameter of WFEG cylindrical MOS structure at a particular channel length of 60nm along with the same for its CG equivalent. The order of channel length considered (60 nm) indicates that the drain characteristics of the device under consideration will be inevitably affected by the undesired short channel effect of Channel Length Modulation resulting in a finite slope in the saturation region of the I_D-V_{DS} characteristics as clearly visible from the said figure. Low value of threshold voltage of the WFEG structure (as seen from the previous figures), results in a higher current driving capability of the WFEG structure.

Finally, comparative analysis of the WFEG CG MOS with respect to its CG counterpart is presented in Figures 4.3.8, 4.3.9 and 4.3.10 in terms of different device parameters such as drain conductance (g_d), trans- conductance (g_m) and voltage gain respectively. The unique feature of linearly graded gate removes the uneven transition in channel electric field, thereby reducing the value of drain conductance. A higher current drivability of the WFEG CG MOS compared to normal CG MOS leads to an increased value of device transconductance. Improvements in these two parameters in turn results in a desirable increase in the voltage gain (gm/gd) of the proposed WFEG CG structure.

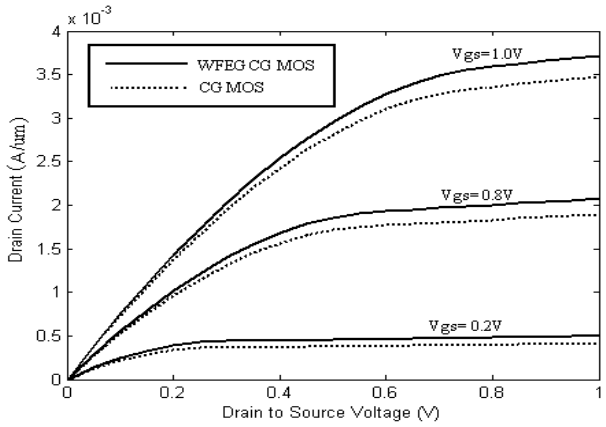


Fig 4.3.7. Output or I_D-V_{DS} characteristics of WFEG CG and normal CG MOSFET structures having channel length of 60 nm considering different gate biases (V_{GS}=1V, 0.8V and 0.2V).

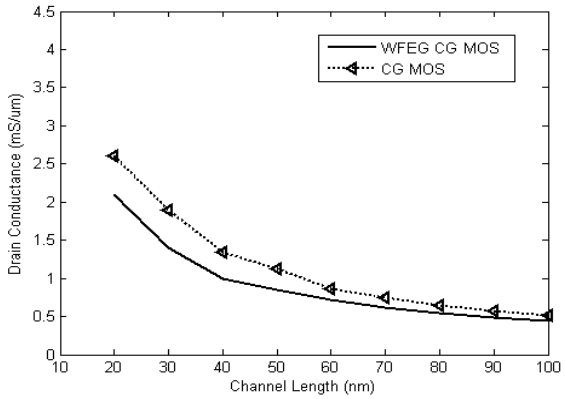


Fig 4.3.8. Variation of Drainconductance, g_d with Channel Length, L and V_{GS}=0.5V and V_{DS}=0.75V for WFEG CG and normal CG MOSFET structures.

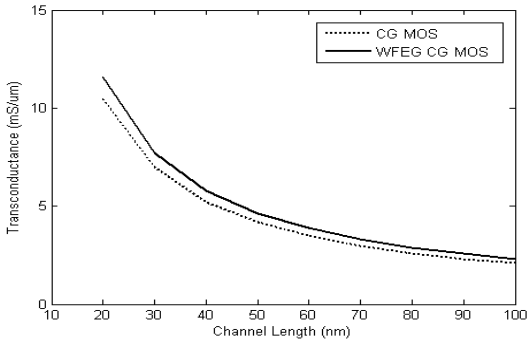


Fig. 4.3.9 Variation of Trans-conductance, g_m with Channel Length, L and V_{GS}=0.5V and V_{DS}=0.75V for WFEG CG and normal CG MOSFET structures.

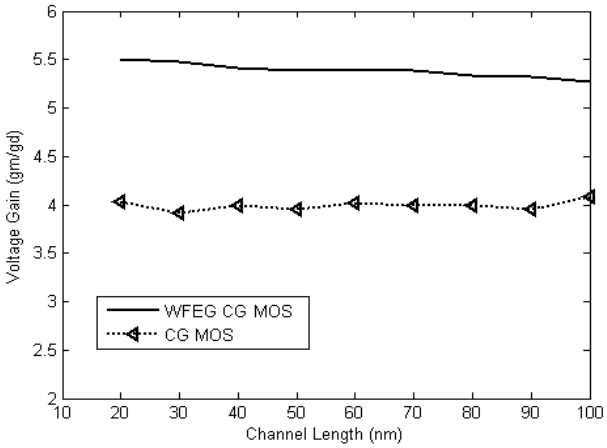


Fig. 4.3.10. Variation of voltage gain (g_m/g_d) with respect to channel length of WFEG CG and normal CG MOSFET structures with V_{GS}=0.5V and V_{DS}=0.75V.

4.4 Quadruple Gate MOSFET with Linearly Graded Binary Metal Alloy Gate: a quasi 3D analytical approach for better short channel device performance analysis

4.4.1. Overview and recent research trend

The essence of the present chapter is to explore the benefits associated with a non-conventional multi gate device structure with the incorporation of innovative concept of gate material engineering by using a binary metal alloy as gate electrode in different multi-gate MOS structures. The first sub section has already presented an in depth study of the attributes of device structure asymmetry of a Linearly Graded Double Gate MOSFET. One of the major drawbacks of a DG MOS is its associated fabrication complexity. As discussed previously, several improvised non-conventional devices are recently gaining research spotlight to overcome the issues related with Double Gate MOSFETs in order maintain the unhindered trend of device dimension down scaling to ultra nano regime, out of which, surrounding gate devices have been gaining significant research interest by dint of their unique feature of gate wrapped channel. The merits associated with a surrounding gate MOSFET has already been discussed in the previous sub section where a cylindrical gate MOSFET shows the unique feature of channel wrapping by the entire gate increasing the device packing density along with the added benefit of better gate electrostatic control over the conducting channel resulting in notable improvement in the device sub-threshold characteristics and enhancing overall current drivability of the device by shielding the device operations from harmful effects of Short Channel Effects (SCEs) compared to conventional planar single and double gate MOSFETs [4.50-4.52]. The surrounding gate geometry, as already discussed can be either cylindrical or rectangular in cross

section. The cylindrical cross section surrounding gate MOS structure has already been discussed in the second subsection incorporating work function engineered binary metal alloy gate electrode with a view to substantiate the efficacy of the WFEG concept in cylindrical MOSFETs.

Finally, in this sub section, detailed investigation of the second special case of surrounding gate MOS i.e. surrounding gate MOSFET with rectangular cross section has been adopted by considering a fully depleted quadruple gate (QG) MOSFET. The QG structure indeed is a three dimensional structure which necessitates the consideration of a three dimensional Poisson's equation as the initial step of analytical modeling. 3D Poisson's equation defines the variation of channel electrostatic potential in all three (i.e. x, y, and z coordinates) making its solution very much complex. This mathematical complexity can be simplified by adopting the novel concept of effective number of gates (ENG) proposed for the first time by J.P. Colinge [4.58]. This concept is basically based on the well known approach of Perimeter Weighted Sum (PWS) coined by Auth and Plummer [4.59]. According to this concept, a QG structure can be seen as the combination of two DG structures surrounding the rectangular cross section silicon channel from top to bottom (constituting a vertical DG arrangement) and one side to the other (constituting a horizontal DG arrangement). The PWS approach makes the calculation of natural length of a QG MOSFET very easy just by knowing the natural lengths of its constituent vertical and horizontal DG MOSFETs.

This sub section will focus on presenting a detailed analytical study of the fully gate wrapped Quadruple Gate (QG) MOS structure considering the gate electrode to be comprised of a linearly graded binary metal alloy [4.25] in order to investigate the dual benefits associated with a QG structure as well as the recently popular idea of work function engineered gate electrode. The analytical modelling presented in this work involves formulation of threshold voltage of the proposed Work Function Engineered Gate Quadruple Gate (WFEG QG) MOSFET from the position of minimum central potential in the channel region evaluated by solving a quasi three dimensional scaling equation adopting the simplified approach of 'effective number of gates (ENG)'. Based on the results obtained from this analytical modelling, an in depth comparative performance study has been investigated in terms of some important short channel parameters like Threshold Voltage Roll-Off (TVRO) , Drain Induced Barrier Lowering (DIBL) and sub-threshold behaviour in order to substantiate the superior short channel characteristics of the proposed WFEG QG structure than a conventional QG MOSFET.

4.4.2. Analytical Modeling

A schematic diagram of the proposed Work Function Engineered Gate Quadruple Gate (WFEG QG) MOSFET is shown in Fig.4.4.1 below in a three dimensional plane.

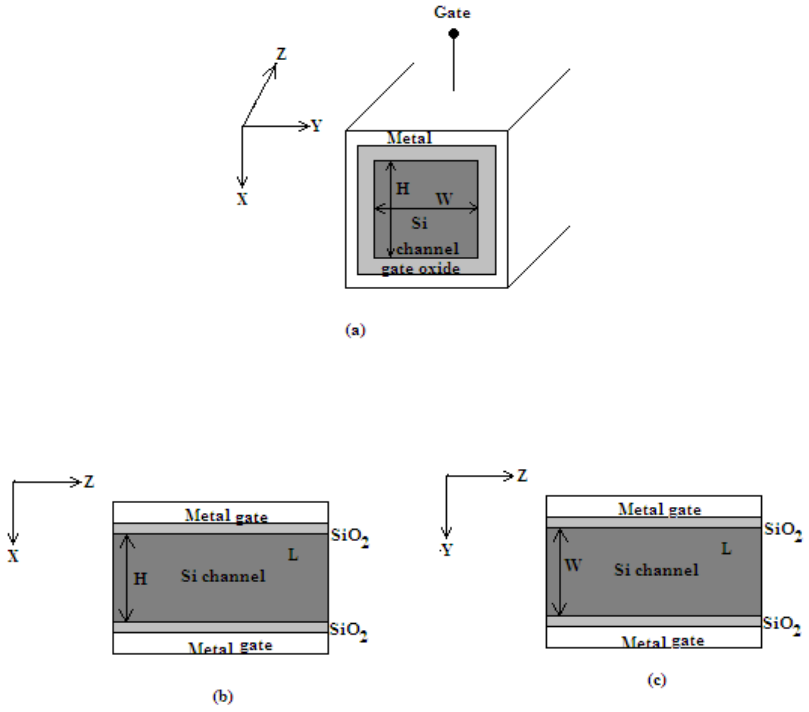


Fig. 4.4.1 WFEG QG MOSFET : (a) Rectangular cross sectional view in 3D, (b) & (c) cross sectional schematic of equivalent two dimensional DG MOSFETs along x-z and y-z planes respectively.

According to the Perimeter Weighted Sum (PWS) approach, the three dimensional QG structure can be simplified by two equivalent independent two dimensional DG MOSFETs along x-z and y-z [4.59]. Starting from the 3D Poisson's equation, the expression of quasi 3D scaling equation of QG MOSFET's central channel potential can be written as follows from the knowledge of scaling theory [4.60]:

$$\frac{d^2\varphi_C(z)}{dz^2} - \frac{1}{\lambda_{QG}^{\ 2}}\left(\varphi_C(z) - \varphi_l\right) = 0 \qquad (4.4.1)$$

Where $\varphi_C(z)$ represents the channel central potential of the short channel device, φ_l represents the conventional long channel central potential and λ_{QG} stands for the natural length of the proposed fully depleted QG MOSFET.

4.4.2.1 Natural Length Calculation

The scaling equation written above (equation 4.4.1) relates the channel central potential of a quadruple gate (QG) MOSFET in terms of its natural length. The natural length calculation of a three dimensional QG structure can be simplified using the ENG concept of Colinge et. al. [4.58] which expresses the ENG of the QG MOSFET as the simple sum of individual natural lengths of the two DG MOSFETs that constitute the QG MOSFET based on the PWS concept mentioned earlier [4.59].

Thus, it can be simply be written as: $ENG_{QG} = ENG_{DG1} + ENG_{DG2}$ (4.4.2)

Again, from the definition of Effective Number of Gates, the ENG of a QG MOSFET and DG MOSFET can be defined as

$$ENG_{QG} = \frac{\lambda_{SG}^2}{\lambda_{QG}^2} \,\&\, ENG_{DG} = \frac{\lambda_{SG}^2}{\lambda_{DG}^2} \tag{4.4.3}$$

Where λ_{SG}, λ_{DG} and λ_{QG} represent the natural lengths of single, double and quadruple gate MOSFETs respectively.

Substituting the expressions of ENG of double gate and quadruple gate in equation 4.4.2, the resultant expression of the natural length of a QG MOSFET can be determined and is given as:

$$\frac{1}{\lambda_{QG}^2} = \frac{1}{\lambda_{DG1}^2} + \frac{1}{\lambda_{DG2}^2} \tag{4.4.4}$$

It is well known and established by various researchers [4.58, 4.60] that considering device operation in bulk conduction mode, the natural lengths of the equivalent DG MOSFETs comprising the QG MOSFET can be individually expressed as:

$$\frac{1}{\lambda_{DG1}^2} = \frac{8C_{ox}}{4W\varepsilon_{Si} + C_{ox}W^2} \text{ and } \frac{1}{\lambda_{DG2}^2} = \frac{8C_{ox}}{4H\varepsilon_{Si} + C_{ox}H^2} \tag{4.4.5}$$

Where C_{ox} signifies per unit area gate oxide capacitance while width and height of the QG MOSFET are represented by W and H respectively (refer to Fig. 4.4.1). This makes the natural length calculation of complex three dimensional QG structure very simple and can be employed in the subsequent potential modeling.

4.4.2.2. Central Potential Modeling

The three dimensional scaling equation of a quadruple gate MOSFET has already been given in equation 4.4.1 as: $\frac{d^2\varphi_C(z)}{dz^2} - \frac{1}{\lambda_{QG}{}^2}\left(\varphi_C(z) - \varphi_l\right) = 0$

The expression of the long channel central channel potential can now be written as [4.60]

$$\varphi_l = V_{GS} - V_{FB} - \frac{qN_{ch}}{\varepsilon_{Si}}\lambda_{QG}^2 \tag{4.4.6}$$

Where, N_{ch} is the channel doping concentration, V_{GS} is the gate-to-source bias and V_{FB} is the device flatband voltage given as $V_{FB} = \phi_{meff}(z) - \phi_S$.

Incorporating the WFEG concept in the QG MOSFET by using a binary metal alloy as the gate electrode modifies the overall expression of gate flat band voltage and the resulting expression of effective work function expression for the gate metal can be formulated as [4.25]:

$$\phi_{meff}(z) = (z/L)\phi_2 + (1 - z/L)\phi_1 \tag{4.4.7}$$

Where ϕ_1 and ϕ_2 are work functions of Platinum and Tantalum respectively constituting gate electrode binary metal alloy where the component mole fraction is continuously varied along the horizontal channel direction i.e. along z axis as shown in Fig. 4.4.1 and horizontal component z is normalized with channel length.

Substituting the expression of V_{FB} in the expression for long channel potential and putting appropriate effective work function, we can write:

$$\varphi_l = V_{GS} - (\phi_{meff}(z) - \phi_{Si}) - \frac{qN_{ch}}{\varepsilon_{Si}}\lambda_{QG}^2$$

Now, substituting the value of φ_l , equation 4.4.1 can be re-written as:

$$\frac{d^2\varphi_C(z)}{dz^2}-\frac{1}{\lambda_{QG}{}^2}\varphi_C(z)+\frac{1}{\lambda_{QG}{}^2}\varphi_l=0$$

$$\Rightarrow \frac{d^2\varphi_C(z)}{dz^2}-\frac{\varphi_C(z)}{\lambda_{QG}{}^2}+\frac{1}{\lambda_{QG}{}^2}\left[V_{GS}-(\phi_{meff}(z)-\phi_{Si})-\frac{qN_{ch}}{\varepsilon_{Si}}\lambda_{QG}^2\right]=0$$

$$\Rightarrow \frac{d^2\varphi_C(z)}{dz^2}-\frac{\varphi_C(z)}{\lambda_{QG}{}^2}+\frac{V_{GX}}{\lambda_{QG}{}^2}-\frac{\phi_{meff}(z)}{\lambda_{QG}{}^2}-\frac{qN_{ch}}{\varepsilon_{Si}}=0$$

Where $V_{GX}=V_{GS}+\phi_{Si}$

Arranging the obtained equation, the fundamental differential equation of channel central potential can be formulated as:

$$\frac{d^2\varphi_C(z)}{dz^2}-\frac{\varphi_C(z)}{\lambda_{QG}{}^2}-\frac{\phi_{meff}(z)}{\lambda_{QG}{}^2}=\frac{qN_{ch}}{\varepsilon_{Si}}-\frac{V_{GX}}{\lambda_{QG}{}^2} \tag{4.4.8}$$

Solving this differential equation results in the final expression of the channel central potential and can be written as:

$$\varphi_C(z)=K_1e^{z/\lambda_{QG}}+K_2e^{-z/\lambda_{QG}}+\left(\frac{\phi_1-\phi_2}{L}\right)z+\left[V_{GX}-\phi_1-\frac{qN_{ch}}{\varepsilon_{Si}}\lambda_{QG}^2\right] \tag{4.4.9}$$

Where K_1 and K_2 are the two coefficients which can be calculated using the typical boundary conditions at the source and drain ends ($\varphi_C(z=0)=V_{bi}$ and $\varphi_C(z=L)=V_{bi}+V_{DS}$) and are given as [4.61]:

$$K_1=\frac{V_{DS}+V_{bi}(1-e^{-L/\lambda_{QG}})-V_{GX}(1-e^{-L/\lambda_{QG}})+\frac{qN_{ch}\lambda_{QG}^2}{\varepsilon_{Si}}(1-e^{-L/\lambda_{QG}})+(\phi_2-\phi_1e^{-L/\lambda_{QG}})}{\left(e^{L/\lambda_{QG}}-e^{-L/\lambda_{QG}}\right)}$$

$$K_2=\frac{-V_{DS}-V_{bi}(1-e^{L/\lambda_{QG}})+V_{GX}(1-e^{L/\lambda_{QG}})-\frac{qN_{ch}\lambda_{QG}^2}{\varepsilon_{Si}}(1-e^{L/\lambda_{QG}})+(\phi_1e^{L/\lambda_{QG}}-\phi_2)}{\left(e^{L/\lambda_{QG}}-e^{-L/\lambda_{QG}}\right)}$$

4.4.2.3. Threshold Voltage Modeling

From the classical definition of threshold voltage modeling, the position of central potential minima in the channel (z_{min}) is calculated by equating the first order derivative of channel central potential to zero and is given as:

$$\left.\frac{d\varphi_c(z)}{dz}\right|_{z=z_{min}} = 0$$

Now, $\varphi_C(z) = K_1 e^{z/\lambda_{QG}} + K_2 e^{-z/\lambda_{QG}} + \left(\frac{\phi_1 - \phi_2}{L}\right) z + \left[V_{GX} - \phi_1 - \frac{qN_{ch}}{\varepsilon_{Si}}\lambda_{QG}^2\right]$

Differentiating the central potential expression and equating it to zero at $z=z_{min}$, we get:

$$\frac{d\varphi_C(z)}{dz} = \left(1/\lambda_{QG}\right) K_1 e^{z_{min}/\lambda_{QG}} - \left(1/\lambda_{QG}\right) K_2 e^{-z_{min}/\lambda_{QG}} + \left(\frac{\phi_1 - \phi_2}{L}\right) = 0$$

$$\therefore K_1 e^{z_{min}/\lambda_{QG}} - K_2 e^{-z_{min}/\lambda_{QG}} = \lambda_{QG}\left(\frac{\phi_2 - \phi_1}{L}\right)$$

Considering λ_{QG} to be very small, the exponential terms can be expanded neglecting the higher order terms for computational brevity and written as:

$$\left(1/\lambda_{QG}\right) K_1 \left(1 + z_{min}/\lambda_{QG}\right) - \left(1/\lambda_{QG}\right) K_2 \left(1 - z_{min}/\lambda_{QG}\right) + \left(\frac{\phi_1 - \phi_2}{L}\right) = 0$$

$$\Rightarrow z_{min}(K_1 + K_2) + \lambda_{QG} K_1 - \lambda_{QG} K_2 + \lambda_{QG}{}^2 \left(\frac{\phi_1 - \phi_2}{L}\right) = 0$$

$$\text{Therefore, } z_{min} = \frac{\left\{\frac{\lambda_{QG}^2(\phi_2 - \phi_1)}{L}\right\} - \left\{\lambda_{QG}(K_1 - K_2)\right\}}{(K_1 + K_2)} \qquad (4.4.10)$$

As defined by the classical definition of threshold voltage, it is that particular value of gate to source voltage for which the minimum value of channel central potential equals two times the value of Fermi potential. The minimum value of the channel central potential can be calculated by substituting the above expression of z_{min} into the expression of central potential (equation 4.4.9). By

using the condition $\varphi_{C,\min} = 2\phi_F$ we have calculated for V_{GS} to find the threshold voltage expression which is given by [4.60]:

$$V_{th} = 2\phi_F - K_1 e^{z_{\min}/\lambda_{QG}} - K_2 e^{-z_{\min}/\lambda_{QG}} - (\phi_1 - \phi_2)\left(z_{\min}/L\right) - \phi_{Si} + \phi_1 + \frac{qN_{ch}\lambda_{QG}^2}{\varepsilon_{Si}} \quad (4.4.11)$$

However, it must be noted that the modeling done so far considers a three dimensional device having channel length in the range of nano meters. Obviously, Quantum mechanical (QM) effects come into play in such a low dimensional 3D device geometry resulting in bandgap widening action as [4.62]:

$$E_{g,QM} = E_{g,CL} + \Delta E_g \quad (4.4.12)$$

Where $E_{g,QM}$ represents the effective device bandgap incorporating quantum mechanical effect, $E_{g,CL}$ represents the classical long channel bandgap and ΔE_g stands for the widening in channel material bandgap as a result of QM effect and is written as:

$$\Delta E_g = q\phi_{QM} = \frac{\pi^2\hbar^2}{2m^* t_{Si}^2} \quad (4.4.13)$$

Where bandgap widening induced incremented potential barrier is represented by ϕ_{QM}.

Thus, while considering the inevitable QM effect in such low dimensional gate all around device geometry, this increased potential barrier must be added to the classical long channel device potential barrier to formulate an expression of the QM effect induced effective device threshold voltage ($V_{th,QM}$) which can be given as:

$$V_{th,QM} = V_{th,CL} + \frac{\pi^2\hbar^2}{2qm^* t_{Si}^2} \quad (4.4.14)$$

Where $V_{th,CL}$ is the classical long channel device threshold voltage (V_{th}) as given by equation 4.4.11.

The Drain Induced Barrier Lowering (DIBL) can be analytically determined by calculating the difference between the device threshold voltages considered at a low and a high value of drain bias respectively and is expressed as [4.63]:

$$DIBL = V_{th}\left(V_{DS} = 0.1V\right) - V_{th}\left(V_{DS\_HIGH}\right)$$

4.4.3 Results and Discussions

This subsection aims to investigate the performance evaluation of the proposed WFEG QG MOSFET and a normal QG MOSFET based on the analytical modeling discussed so far incorporating QM effects. MEDICI simulator data have also been provided to validate the computational accuracy of the proposed model. In both the cases, simulation has been carried out with the parameter values as listed in Table 4.4.1.

Table 4.4.1: Parameter Table

Parameter	**Substrate doping concentration (N_{SUB})**	**Source/ Drain doping concentration ($N_{S/D}$)**	**Channel width**	**Channel height**	**Front Oxide thickness (t_{ox})**	**Film thickness (t_{Si})**
Value	10^{15} cm^{-3}	10^{17} cm^{-3}	20 nm	20 nm	1 nm	20 nm

Initially, the variation of channel central electrostatic potential with channel position of QG MOSFET with or without incorporating the WFEG effect has been illustrated in Fig. 4.4.2 considering different values of drain-to-source voltages.

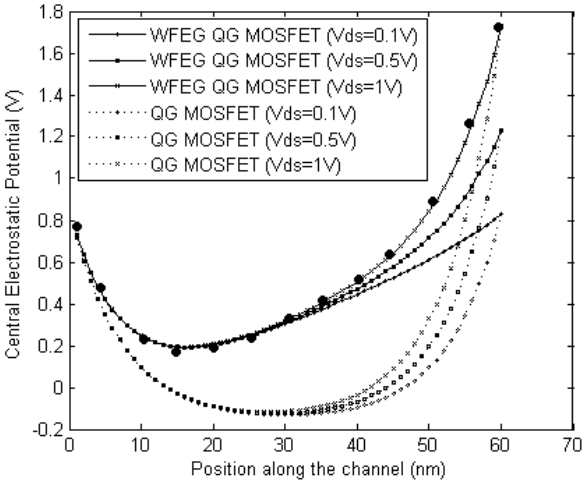


Fig. 4.4.2. Variation of central electrostatic potential along channel position of WFEG QG and normal QG MOSFETs having channel length of 60nm at applied gate bias of 0.1V. Circular dots represent MEDICI simulated data for WFEG QG MOSFET (V_{DS}=1V).

It becomes apparent from a careful observation of the said figure that as the device dimesion gets scaled down to sub-nanometer regime, the central potential minima of the proposed WFEG QG structure having a spatial composition graded binary metal alloy gate electrode gradually shifts towards the source end instead of being located at the middle of the channel, thereby shielding the potential minima from any random variation in drain bias. On the contrary, the central potential minima of the normal QG MOSFET does not exhibit this source-side shift and remains essentially positioned near the middle of the channel. Moreover, it can be clearly understood from the said figure that the position of channel potential minima of the WFEG QG MOS is shifted up with respect to its normal QG equivalent which testifies the superiority the WFEG concept in mitigating the DIBL and other SCEs. This fact is supported by Fig. 4.4.3 elucidating central electric field distribution along the channel. It is clearly visible that the peak electric field near the drain end of the proposed WFEG QG MOSFET is much reduced compared to that of normal QG MOSFET due to the continuous adjustment of effective work function along the channel direction from source end towards drain. A significant reduction in drain side peak electric field ensures sufficient immunity of the proposed WFEG QG device from impact ionization induced hot carrier effects.

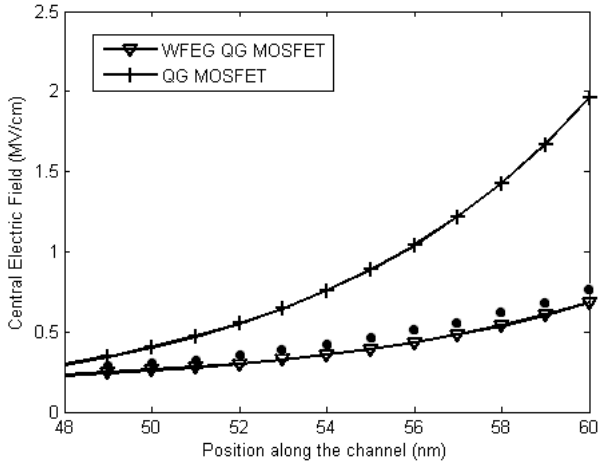


Fig. 4.4.3. Variation of central electric field along channel position of WFEG QG and normal QG MOSFETs having channel length of 60nm at a constant gate bias of 0.3V. Circular dots represent MEDICI simulated data for WFEG QG MOSFET (V_{DS}=0.5V).

Figure 4.4.4 nicely depicts a comparative analysis of the variation of the threshold voltage against the channel length of a WFEG QG with respect to normal QG MOSFET (without considering any structural or doping modifications). It can be understood from Fig.4.4.4 that the threshold voltage roll off is notably improved in the proposed WFEG QG attributed primarily by the continuous lateral mole fraction modulation of the binary metal alloy gate material indicating the superiority of the proposed WFEG QG MOS structure in suppressing unwanted SCEs.

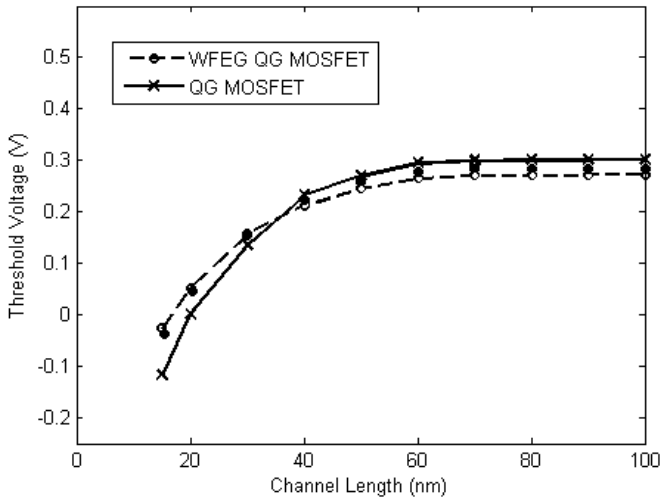


Fig.4.4.4. Variation of threshold voltage, V_{th} with channel length L for WFEG QG and normal QG MOSFET structures (V_{GS}=0.1V and V_{DS}=0.1 V). Circular dots represent MEDICI simulated data for WFEG QG MOSFET.

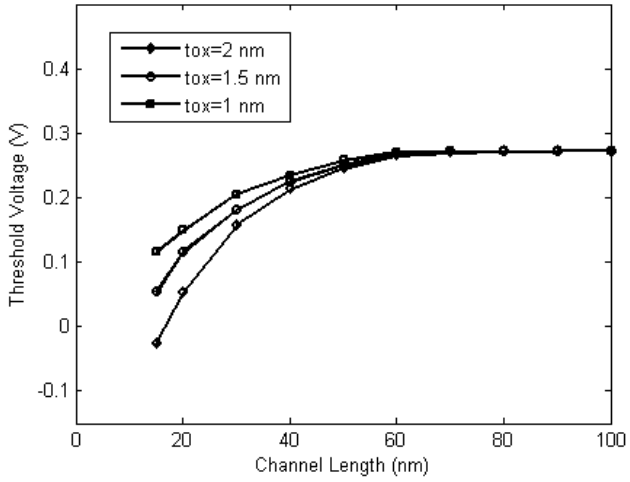


Fig.4.4.5 Variation of threshold voltage, V_{th} with channel length L of WFEG QG MOSFET structure (V_{GS}=0.1V and V_{DS}=0.1 V) for different gate oxide thicknesses.

Next, the threshold voltage behavior of the proposed WFEG QG device has been studied for various gate oxide thicknesses in Fig. 4.4.5 indicating that a thinner gate oxide reduces device natural length which in turn induces a considerable reduction in threshold voltage roll-off making the thin gate structure a possible alternative device in suppressing performance degrading SCEs

[4.17]. However, a thin gate oxide on the other hand is affected by the allied problems of enhanced gate leakage current which leads to an effective increase in static power consumption. Thus, a trade-off has to be considered for simultaneous suppression of SCEs along with avoiding an increase in static power consumption to sort out an optimal solution.

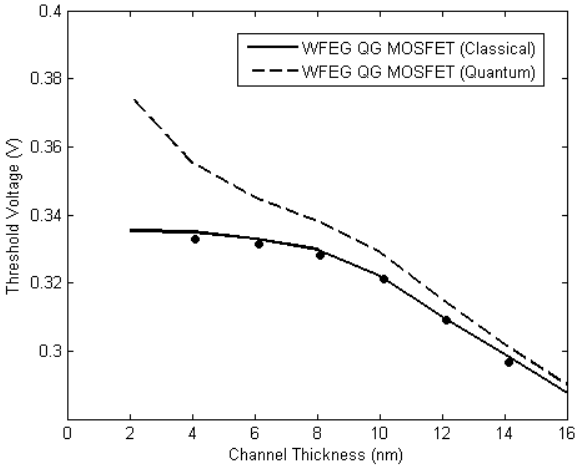


Fig.4.4.6 Variation of threshold voltage with channel thickness t_{Si} of a WFEG QG MOSFET with and without quantum mechanical effect. Circular dots represent MEDICI simulated data for WFEG QG MOSFET.

Fig. 4.4.6 establishes an important observation from the present research endeavor by depicting threshold voltage variation with channel thickness of the proposed WFEG QG MOSFET including and without including quantum mechanical effect. Observing the said figure, it can be inferred that the quantum threshold voltage deviates distinctly from the classical threshold voltage when the channel thickness is scaled down gradually. This is due to the QM band gap widening discussed in the earlier section which leads to an effective increase in the device threshold voltage according to eq. 4.4.14.

Having studied the threshold voltage behavior, the next two figures attempt to study the variation of DIBL with channel length. Figure 4.4.7 describes the impact of inclusion of WFEG effect in a QG MOS device. It is clear from the said figure that DIBL increases with a reduction in channel length as expected from the knowledge of short channel device physics. However, the comparative picture testifies that the increment in DIBL is significantly less in WFEG QG MOS than its normal QG counterpart establishing the superior DIBL performance of WFEG QG structure.

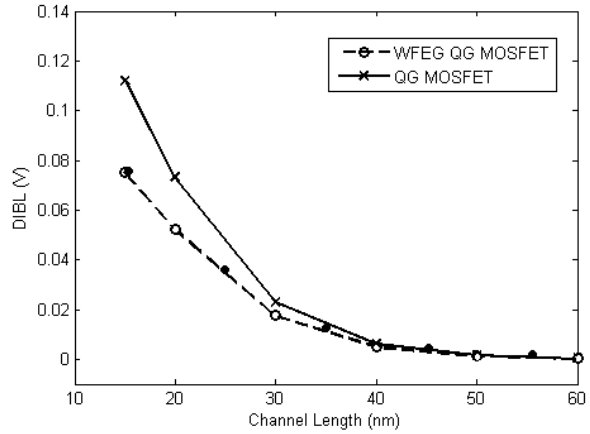


Fig 4.4.7. Variation of DIBL with channel length L for WFEG QG and normal QG MOSFET structures at a gate bias of 0.1V. Circular dots represent MEDICI simulated data for WFEG QG MOSFET.

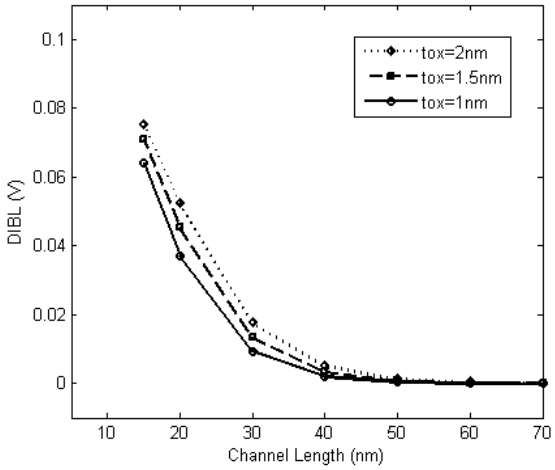


Fig.4.4.8 Variation of DIBL with channel length L of WFEG QG MOSFET structure considering a gate bias of 0.1V and drain bias of 0.1 V for different gate oxide thicknesses.

Finally, in Fig. 4.4.8, the nature of variation of DIBL with channel length has been demonstrated considering different gate oxide thicknesses of the WFEG QG MOSFET. It is quite obvious from the earlier discussions that a device with thin gate oxide will be more effective in controlling unwanted DIBL which is once again confirmed by observing the notable reduction in DIBL corresponding to gradual decrement of gate oxide thickness ensuring better SCE repression in nano dimensions.

This chapter basically aims to explore the effectiveness of incorporating the novel concept of linearly varying the mole fraction of a binary metal alloy used as gate electrode (i.e. work function engineered gate) coined by Sarkar et. al. in multigate MOSFET devices with the primary objective to establish the effectiveness of the 'work function engineered gate' concept in subduing the detrimental SCEs in

short channel semiconductor devices. This purpose has been exploited in different sub sections by incorporating the work function engineered gate concept into different multigate device structures such as Double Gate MOSFET, Cylindrical Gate MOSFET and Quadruple Gate MOSFET as discussed in details throughout the chapter.

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Relevant Publications:

- Navjeet Bagga, **Saheli Sarkhel** and Subir Kumar Sarkar. "Exploring the asymmetric characteristics of a Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate Electrode for enhanced performance." In **IETE Journal of Research, Taylor and Francis,** Volume 62, 2016 - Issue 6, Pages 786-794 , 2016
- **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "Analytical Modeling and Simulation of a Linearly Graded Binary Metal Alloy Gate Nanoscale Cylindrical MOSFET for reduced short channel effects" In **Journal of Computational Electronics, Springer**, Vol. 13, No. 3, pp. 599-605, April, 2014.
- **Saheli Sarkhel** and Subir Kumar Sarkar. "A compact quasi 3D threshold voltage modeling and performance analysis of a novel linearly graded binary metal alloy quadruple gate MOSFET for subdued short channel effects." In **Superlattices and Microstructures**, **Elsevier**, Vol. 82, pp. 293-302, 2015

Chapter 5

Some improvised multigate Junctionless MOSFETs with Work Function Engineered gate electrode

CHAPTER V

5.1. Introduction

The unimpeded advancement of VLSI industry from micro to nano regime has been possible by the continuous miniaturization of device physical dimension with a view to develop ultra low dimensional low power consuming high speed devices to quench the technological requirements of modern tech savvy civilization. This aggressive pace of continuous device dimension down scaling is facing some severe performance related issues like unavoidable Short Channel Effects (SCEs), impurity concentration induced carrier mobility degradation , enhanced gate tunneling effect due to

down scaling the thickness of transistor gate oxide, measurable p-n junction leakage current enhancement attributed to the equivalent reduction in junction thicknesses [5.1]. These unwanted short channel effects pose severe threat to the performance of conventional bulk devices which can no longer match the required high performance. This necessitates extensive research on the innovation of non conventional device structures which can alleviate the said performance deterrents and maintain the superior performance specified by the requirements listed by ITRS [5.2]. The previous two chapters of this dissertation have focused on some of the recently evolved non-conventional semiconductor device structures such as Fully Depleted Silicon-on-Insulator/Nothing (FD SOI/SON) MOSFETs and several multigate MOSFET structures like Double Gate MOSFET (where two gates: front gate and back gate are used instead of a single gate) and surrounding gate MOSFET (where the gate completely covers the cylindrical or rectangular cross sectional channel) [5.3-5.7]. All the device structures discussed so far, however, are junction based devices. The major drawback of ultra scaled junction based devices lies in the creation of ultra sharp source-to-channel and drain-to-channel junctions due to the challenges associated with available doping facilities and limitations on temperature estimations [5.8-5.9]. The allied problems of junction based devices have urged the researchers to explore some innovative device structure which can solve the sharp junction related issues. This has shifted the research interest to the growth of 'junctionless (JL)' devices which altogether removes the need of formation of source-channel and drain-channel junctions [5.10]. The junctionless (JL) devices by dint of their novel architecture, proves to be very effective in eliminating the problems related to precise impurity diffusion and creation of ultra sharp doping profile. Naturally, the JL MOSFETs exhibit significantly improved turn-on and output characteristics [5.11-5.13], almost ideal value of sub-threshold swing and appreciably high value of device ON state current along with interesting temperature characteristics which is attributed to the average sensitivity of carrier mobility on temperature when the impurity concentration is sufficiently high.

Moreover, one more emerging research idea of 'work function engineered gate' has already been elaborated in the last two chapters which involves the use of a binary metal alloy gate electrode whose effective work function can be precisely adjusted to the desired value by linearly adjusting the mole fraction of constituent metals along the channel length from source gradually towards the drain. This chapter intends to explore the performance improvements of the emerging junctionless devices incorporating 'work function engineered gate' into conventional junctionless equivalent device structures (without using work function engineered gate electrode) by achieveing much reduced Threshold Voltage Roll off (TVRO) and Drain Induced Barrier Lowering (DIBL), particularly highlighting the efficacy of the novel gate material engineering technique even on Junctionless devices.

5.2. Recent research trends

The evolution of silicon industry from the domain of microelectronics into nano electronics is dominated by the tremendous down sizing of the semiconductor device dimensions. This trend has persisted over several decades when innovative research endeavors in the domain of electron devices are mostly associated with the development and implementation of innovative low power nanoscale devices to achieve considerable performance improvement of VLSI circuits. Obviously there is some price to pay associated with this explosive technogy boon. Some of the allied complications with this incessant pace of device dimension down scaling from sub-micron to nanometer regime can be summarized as irreversible threat to device reliability, carrier mobility degradation due to excessive impurity doping, problems of poly silicon gate depletion, boron penetration, enhanced gate tunneling effect due to an equivalent down scaling of gate oxide thickness and most prominently the unavoidable Short-Channel Effects (SCEs) such as Hot carrier effect (HCE), Drain-Induced Barrier Lowering (DIBL), undesired current conduction in sub threshold region and a measurable increase in p-n junction leakage current attributed to the equivalent reduction in junction thicknesses etc. In spite of these challenges related to short channel devices, maintaining this trend of continuous device dimension downsizing without affecting device functionality is feasible only through a perfect blend of device dimension miniaturization, improvised novel structures and material engineering. This paved the way for extreme research initiatives in the area of electronic devices to develop a multitude of non-conventional device structures capable of addressing the problems of short channel effects affecting performance of devices having dimensions down to nanometer range. SOI/SON technology can be regarded as a possible alternative to conventional MOS technology by means of their superior short channel device performance achieved by replacing bulk silicon substrate under the conduction channel by a layer of buried oxide (BOX). Another possible improvisation over existing basic MOSFET structure can be the incorporation of the multigate concept, where multiple gate electrodes are used to control the resultant device current.

Double Gate (DG) MOS structures have attracted significant research attention owing to their superior scalability, excellent SCE suppression, near ideal value of sub-threshold slope, excellent control of the gate electrode over the channel resulting in ON state current almost twice that of single gate MOS, thereby making it feasible to realize ultra low device dimension even beyond the constraints of conventional fabrication technologies [5.4-5.6]. On top of this, the most interesting feature of a surrounding gate (SRG) MOSFETs lies in its novel device geometry where the gate almost envelops the entire channel which effectively increases packing density of the resultant IC in addition to the extra assistance of superior electrostatic control of the gate over the channel potential

profile resulting in considerable improvement in sub-threshold characteristics and superb resistance against detrimental Short Channel Effects (SCEs) in sharp contrast to single gate and double gate counterparts [5.14-5.16].

Inspite of having so many advantages, a major challenge faced by all junction based devices elaborated in the previous chapters is the need of forming ultra-sharp source and drain junctions for extremely down scaled devices. If the device channel length is considered to be as small as 10 nm, formation of ultra-sharp source and drain junctions implies that the highly doped source and drain regions will be separated from the low doped channel by a very sharp junction having significant difference in doping concentration over a separating distance as low as some nano-meters. This drastic concentration gradient imposes stringent conditions on fabrication techniques of doping and device temperature estimations [5.9]. In order to surmount these challenges associated with normal junction based devices, a possible alternative, namely junctionless (JL) transistors are reported in some recent literatures [5.9-5.11]. These novel devices proposed here can be fabricated using similar fabrication set up even more easily as there is no need to form precise junctions. The main essence of this junctionless architecture is that the polarity and doping concentration of the channel region is exactly similar to source and drain doping. Thus, sharp concentration gradient at the source and drain junctions have been successfully avoided. This prevents any chance of dopant diffusion during thermal processing steps, thereby sufficiently relaxing the thermal budget.

Moreover, the physics behind the operation of junctionless devices suggests that these devices operate in accumulation mode unlike the inversion mode operation of conventional MOSFETs as the channel doping concentration is same as that of the source/drain regions. Thus, the accumulation-mode devices exhibit improved contact resistance and reduced sensitivity to gate overlap or underlap issues. These devices are not affected by doping-fluctuations and thermal instability due to negative bias compared to equivalent inversion-mode devices showing less dependence of device current on the doping concentrations. These advantages make JL MOSFET a much better alternative to junction based devices due to significantly improved turn-on and output characteristics, almost ideal value of sub-threshold slope and substantially high value of device ON state current along with interesting temperature characteristics which is attributed to the average sensitivity of carrier mobility on temperature when the impurity concentration is sufficiently high as seen in the case of JL MOSFETs.

Exploring the popular idea of multiple metal gate, Deb et. al. introduced an improvised novel idea that instead of a single metal electrode, a binary metal alloy (A_{α} $B_{1-\alpha}$) can be used as gate electrode in a FD SOI MOSFET [5.17]. The mole fraction of this alloy can be continuously varied from source side (100% A) to drain side (100% B) in order to suitably tune the effective work function. This pioneering concept of 'gate material engineering' can be included into various non-

conventional device structures to realize improved short channel device performance as compared to their normal device counterparts without 'work function engineered gate'. The detailed literature survey of this ground breaking concept and its fabrication feasibility has already been elaborated in Chapter 4 [5.17-5.21]. The improved results achievable using this binary metal alloy gate electrode have been the major motivation to incorporate this concept into Junctionless device structures in this Chapter with a view to realize better device performance.

The first section of analytical modelling discussed in this chapter will investigate a comparative performance analysis of a Junctionless Work Function Engineered Gate Double Gate (JL WFEG DG) MOS structure with respect to normal JL DG MOS without any binary metal alloy gate on the basis of analytical surface potential modeling. The next section will present similar analytical modelling based performance investigation of Junctionless Work Function Engineered Gate Cylindrical Gate (JL WFEG CG) MOS structure in contrast to its simple JL CG MOS equivalent. Both the studies will exhibit superior performance of the WFEG JL structures compared to their simple JL counterparts in terms of Drain Induced Barrier Lowering (DIBL), Threshold Voltage Roll-Off (TVRO) and voltage gain.

5.3. Junctionless Double Gate MOSFET with linearly graded binary metal alloy gate: an analytical modeling based performance comparison

5.3.1. Overview

In view of the above presented discussion on the ongoing research trend starting from the inception of the search for non-conventional device structures to alleviate the shortcomings associated with conventional planar devices, it can be well understood that introduction of junctionless devices may open a new corridor of contemporary research in the field of low dimensional devices. The wide range merits of the junctionless concept originate from the very device geometry which eliminates sharp concentration gradient at the source/drain to channel junctions by maintaining a uniform doping concentration all over the device starting from source to drain regions. Moreover, it is a well known fact that Double Gate (DG) MOSFET structure by virtue of having two gates (front and back) exhibit enhanced gate control over the channel (both front and back gates controlling the charge in silicon channel), which in turn is reflected in the superior device performance in terms of SCE suppression ensuring further scalability of device dimensions. Moreover, the pioneering concept of work function engineered gate electrode has already been established in the preceding chapters to improve short channel performance of low dimensional devices. Taking these into consideration, this section of the thesis chapter aims to investigate the intricacies of analytical threshold voltage

modelling of a Junctionless 'Work Function Engineered Gate' Double Gate MOSFET (JL WFEG DG MOS) and perform a comparative analysis of the proposed JL WFEG DG structure with its normal JL DG counterpart to emphasize on the effectiveness of WFEG scheme incorporated.

5.3.2. Analytical Modeling

The basic operating principle of a conventional junction based device discussed in the earlier chapters involves channel inversion and induces a layer of minority carriers at the junction of semiconductor and gate oxide which forms a continuous channel connecting the two heavily doped regions of source and drain. On the contrary, the physics governing the operating principle of junctionless devices is based on depletion or accumulation region operation where the majority carriers of the heavily doped substrate is involved in channel current subjected to application of suitable gate voltage. The fundamental difference between a junction based and junctionless device lies in the mechanism of current conduction. Channel current in a junction based device is due to the conduction of minority carriers through the inverted channel at the oxide-semiconductor interface, whereas device current of a junctionless device arises due to the conduction of majority charge carriers through the entire volume of silicon film. The schematic structure of the proposed JL WFEG DG MOSFET is illustrated in Fig. 5.3.1. The source and drain region thicknesses are assumed to be almost negligible and source and drain electrodes are placed at the two sides of the heavily doped bulk silicon layer.

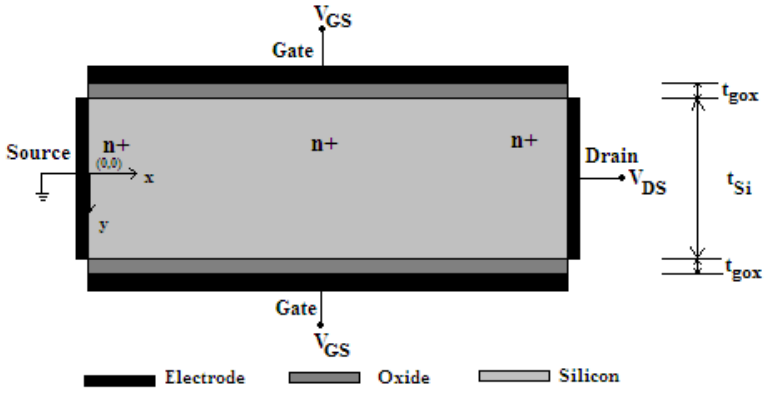


Fig.5.3.1 Schematic cross sectional view of a Junctionless Work Function Engineered Gate electrode Double Gate MOSFET

The formulation of the expression of effective workfunction of a linearly graded binary metal alloy as a function of channel position has already been elaborated is the previous chapter. Following that, the expression of the effective work function has been re-written below [5.21]:

$$\phi_{meff}(x) = (x/L)\phi_2 + (1-x/L)\phi_1 \tag{5.3.1}$$

Where ϕ_1 and ϕ_2 represents the pure constituent work functions of Platinum and Tantalum respectively. The x component (along the horizontal direction) is normalized with channel length L and the channel is assumed to be fully depleted.

5.3.2.1. Surface Potential Modeling

The two dimensional Poisson's equation for n-channel junctionless WFEG DG MOSFET under consideration operating in sub-threshold region is given as [5.22-5.23]:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \tag{5.3.2}$$

Where $\varphi(x,y)$ represents the channel potential which is two dimensional in nature, N_{ch} is the doping concentration of the uniformly doped channel of the junctionless structure and ε_{Si} is the relative permittivity of silicon.

Following earlier modeling basics, the two dimensional channel potential can be approximated considering Young's parabolic potential profile [5.24] as:

$$\varphi(x,y) = d_1(x) + d_2(x)y + d_3(x)y^2 \tag{5.3.3}$$

Considering the channel length along x axis and the normal direction to the channel is taken along along y axis keeping the origin at the centre of the silicon film.

1. Thus the central potential along x direction can be obtained by putting y=0 in equation 5.3.3 and is given by-

   $$\varphi_C(x) = \varphi(x,0) = d_1(x)$$

2. The electric field at the back gate-channel interface (where $y = {t_{Si}}/{2}$) is given as:

   $$\left.\frac{\partial\varphi(x,y)}{\partial y}\right|_{y={t_{Si}}/{2}} = \frac{\varepsilon_{gox}}{\varepsilon_{Si}}\frac{V_{GS} - \varphi_S(x) - V_{FB}}{t_{gox}}$$

3. Similarly, the electric field at the front gate oxide-silicon channel interface (where $y = -t_{Si}/2$) is given as:

$$\left.\frac{\partial\varphi(x,y)}{\partial y}\right|_{y=-t_{Si}/2} = \frac{\varepsilon_{gox}}{\varepsilon_{Si}}\frac{\varphi_S(x) - V_{GS} + V_{FB}}{t_{gox}}$$

Where $\varphi_S(x) = \varphi(x, y = -t_{Si}/2)$ is the surface potential, V_{GS} is the externally applied gate to source bias, t_{Si} is the silicon film thickness, t_{gox} is the gate oxide thickness (front and back gate thicknesses being equal), ε_{gox} is the gate oxide permittivity and V_{FB} represents flat-band voltage $\left(V_{FB} = \phi_{meff} - \phi_{Si} = \phi_1 + (\phi_2 - \phi_1)\left(\frac{x}{L}\right) - \phi_{Si}\right)$.

It must be noted at this point that both the front and back gates are connected to the same supply voltage V_{GS} making this Double Gate MOSFET a tied three terminal Double gate (3T DG MOSFET) device structure.

Using the above boundary conditions, the 2D Poisson equation (eq.5.3.2) can be re-arranged and expressed as a function of central potential of the channel as:

$$\frac{d^2\varphi_C(x)}{dx^2} - \frac{8C_{gox}}{4\varepsilon_{Si}t_{Si} + C_{gox}t_{Si}^2}\left[\varphi_C(x) - V_{GS} + V_{FB} - \frac{qN_{ch}t_{Si}}{2C_{gox}} - \frac{qN_{ch}t_{Si}^2}{8\varepsilon_{Si}}\right] = 0 \qquad (5.3.4)$$

Where $C_{gox} = \varepsilon_{gox}/t_{gox}$ represents the capacacitance of gate oxide measured in per unit area.

The differential equation of 5.3.4 can be solved mathematically to obtain the channel central potential which can now be represented as a function of horizontal 'x' coordinate by the following expression:

$$\varphi_C(x) = Pe^{x/\lambda} + Qe^{-x/\lambda} + (\phi_1 - \phi_2)\left(x/L\right) + \left[-\phi_1 + \frac{qN_{ch}t_{Si}}{2C_{gox}} + \frac{qN_{ch}t_{Si}^2}{8\varepsilon_{Si}} + V_{GS} + \phi_{Si}\right] \qquad (5.3.5)$$

Where $\frac{1}{\lambda^2} = \frac{8C_{gox}}{4\varepsilon_{Si}t_{Si} + C_{gox}t_{Si}^2}$ represents the generic expression for natural length of a DG MOSFET.

A proper picture of the nature of variation of the evaluated central potential with positional coordinate 'x' can be obtained by calculating the coefficients P and Q of equation 5.3.5 taking into account the boundary condition of channel potential at the source and drain extremities of a junctionless device as $\varphi_C(x=0)=0$ and $\varphi_C(x=L)=V_{DS}$ respectively [5.22]. The formulated coefficients are given by:

$$P=\frac{V_{DS}-(\phi_1-\phi_2)-\left[-\phi_1+\frac{qN_{ch}t_{Si}}{2C_{gox}}+\frac{qN_{ch}t_{Si}^2}{8\varepsilon_{Si}}+V_{GS}+\phi_{Si}\right]\left(1-e^{-L/\lambda}\right)}{e^{L/\lambda}-e^{-L/\lambda}}$$

$$Q=\frac{-V_{DS}+(\phi_1-\phi_2)+\left[-\phi_1+\frac{qN_{ch}t_{Si}}{2C_{gox}}+\frac{qN_{ch}t_{Si}^2}{8\varepsilon_{Si}}+V_{GS}+\phi_{Si}\right]\left(1-e^{L/\lambda}\right)}{e^{L/\lambda}-e^{-L/\lambda}}$$

5.3.2.2. Threshold Voltage Modeling

For the sake of computational brevity, the threshold voltage of the JL WFEG DG MOS under consideration can be evaluated from the classical definition of threshold which is defined to be the gate-to-source voltage for which the channel central potential minima becomes zero ($\varphi_{C,\min}=0$). For this, calculating the position of minimum central potential (x_{min}) is crucial which can be extracted by equating the first order channel central potential expression (eq. 5.3.5) to zero and written as

$$x_{\min}=\kappa/(P+Q) \text{ where } \kappa=\frac{\lambda^2(\phi_2-\phi_1)}{L}-\lambda(P-Q)$$

Putting this value of x_{min} into the expression of channel central potential, the minimum central potential can be determined which can eventually be equated to zero and solved to find the value of V_{GS} to find the threshold voltage expression which can be given by [5.22]:

$$V_{TH}=\phi_1-\phi_{Si}-\frac{qN_{ch}t_{Si}}{2C_{gox}}-\frac{qN_{ch}t_{Si}^2}{8\varepsilon_{Si}}-Pe^{x_{\min}/\lambda}-Qe^{-x_{\min}/\lambda}-\left(\frac{\phi_1-\phi_2}{L}\right)x_{\min} \quad (5.3.6)$$

Once the expression for threshold voltage has been formulated, it can now be utilized to obtain the Drain Induced Barrier Lowering (DIBL) which is simply the difference between the device threshold voltages considered at a low and a high value of drain bias respectively and is given as:

$$DIBL=V_{TH}(V_{DS}=0.1V)-V_{TH}(V_{DS\_HIGH}).$$

5.3.3. Results and Discussions

This subsection of the thesis demonstrates a contrastive performance study on the basis of a detailed two dimensional Poisson's equation based analytical modeling of a JL WFEG DG MOSFET and normal JLDG MOSFETs along with simulation results. 2-D MEDICI simulator data has also been provided to validate the accuracy of proposed analytical model. In both the cases, simulation has been carried out with the parameter values as listed in Table 5.3.1.

Table 5.3.1: Parameters used for simulation

Parameters	$N_{S/D}=N_{ch}$	t_{Si}	t_{gox}	L	ϕ_1	ϕ_2
Values	5×10^{26} m^{-3}	10 nm	2 nm	100 nm	5.3 eV	4.4 eV

To begin with, Fig. 5.3.2 depicts the nature of variation of central potential profile in the channel along the channel position from source to drain for both proposed JL WFEG DG MOSFET and a normal JL DG MOSFET (without work function engineered gate electrode) for different values of drain bias considering the device channel lengths to be 100 nm. The solution of Poisson equation has been based on Young's Parabolic Potential Approximation to formulate the final expression of channel central electrostatic potential consolidating the recently evolving innovative idea of a binary metal alloy gate electrode with linearly graded mole fractions of constituent metals. It is quite apparent from the said figure that for a relatively longer geometry MOS structure (as in case of Fig.5.3.2), the presence of the (x/L) term in the expression of channel central potential (refer to eq. 5.3.5) results in a finite linear slope in the central potential variation along channel position, thereby manifesting the impact of 'work function engineered' gate on device potential profile.

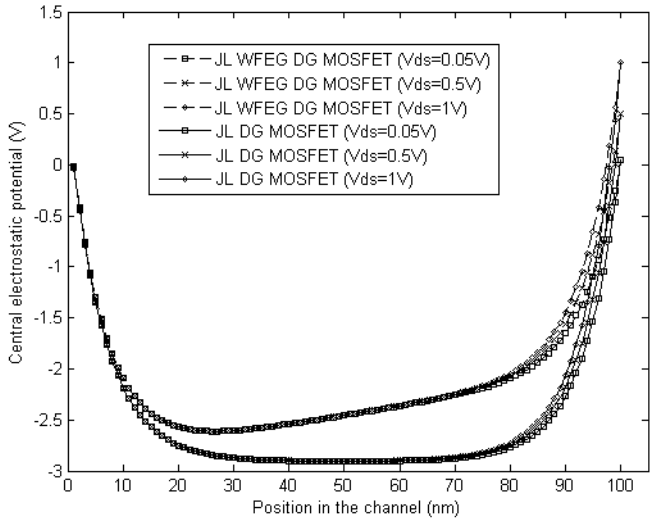


Fig.5.3.2 Central potential distribution along the channel position of JL WFEG DG and JL DG MOSFET for different values of V_{DS}

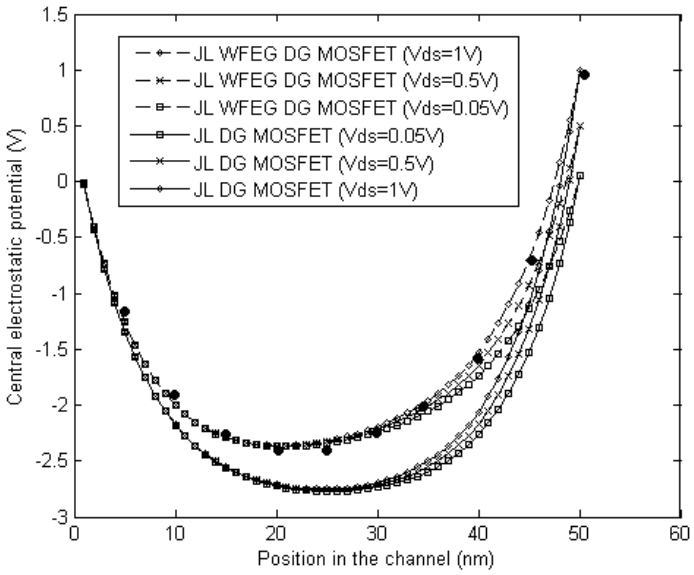


Fig.5.3.3 Variation of channel central potential along channel position of JL WFEG DG and JL DG MOSFETs considering different values of V_{DS} for a chanel length of 50nm. MEDICI simulated data for JL WFEG DG MOSFET (V_{DS}=1V) are represented by circular dots.

Fig. 5.3.3 depicts similar variation of channel central potential as in Fig.5.3.2, but for a smaller device channel length. It can be well understood from the figure that the parabolic symmetry in the potential profile gets restored by the WFEG effect for the considered device structure having channel dimension in the range of nanometer compared to conventional long channel MOS, which is a clear indication of its immunity against various short channel effects in smaller dimension. Moreover, it can be clearly observed from both the figures (Fig.5.3.2 & 5.3.3) that the potential

minima of the JL WFEG DG MOS is higher than that of the JL DG MOS and is gradually shifted towards the source/channel junction which circumstanciates the supremacy of the proposed JL WFEG DG structure under consideration in alleviating short channel effect induced performance degradation by shielding the minima of channel central potential from any unwanted impact of drain bias variations[5.17, 5.21].

Having established the superiority of proposed JL WFEG DG structure over normal JL DG MOS, Fig.5.3.4 attempts to investigate the variation of central electrostatic potential with channel position for different gate oxide thicknesses (t_{gox}).

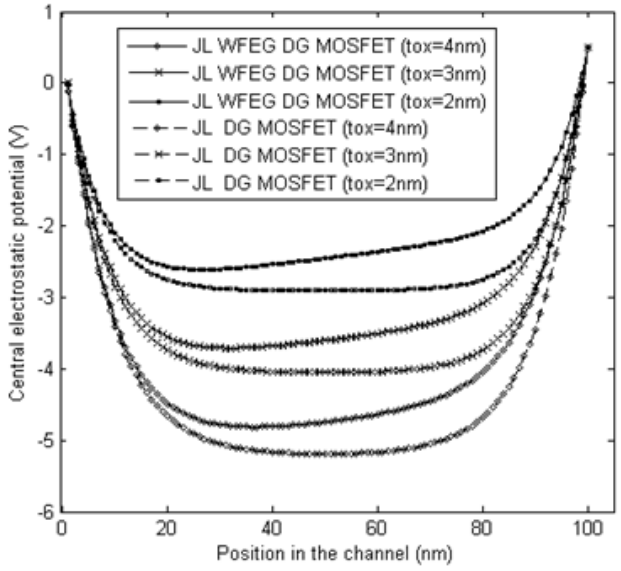


Fig.5.3.4 Variation of channel central potential along the channel position of both JL WFEG DG and JL DG MOSFETs considering different gate oxide thicknesses (t_{gox})

It is clearly evident from the above figure that with a gradual decrease in gate oxide thickness, the electrostatic control of the gate electrode on channel charge density increases, resulting in an upward shift of central potential minima indicating clear performance improvement. On the basis of this observation, it can be deduced that thin gate oxide is a better choice for nanoscale devices for suppressing the harmful SCEs.

Next, the variation of channel central electric field with the channel length has been depicted in Fig.5.3.5 (particularly the variation near the drain end as high electric field near drain end results in a number of detrimental short channel effects).

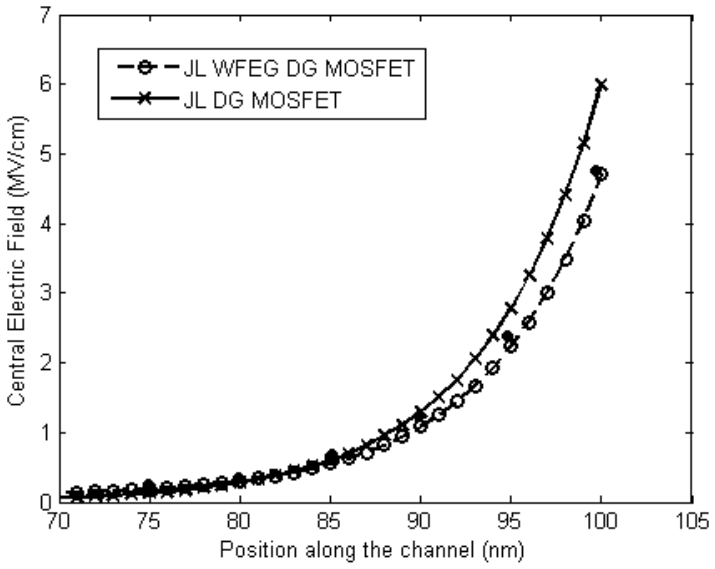


Fig.5.3.5 Variation of channel central electric field with respect to the position along the channel near the drain end for JL WFEG DG and normal JL DG MOSFETs keeping V_{GS} = 0.15V, V_{DS} = 0.75V . MEDICI simulated data for JL WFEG DG MOSFET are represented by circular dots.

The figure above clearly shows a considerable reduction in the electric field profile of proposed JL WFEG DG MOS compared to JL DG MOS which is primarily attributed due to continuous adjustment of alloy mole fraction from source end towards the drain end. This reduction eventually reduces the peak electric field at the drain end in the proposed JL WFEG DG structure resulting in significant suppression of SCEs, particularly Hot Carrier Effect (HCE) caused by high field impact ionization near the drain end. The reduction in HCE creates a further scope for gate oxide thickness down scaling which is indeed a requirement to continue the trend of device dimension miniaturization for future VLSI industry.

Having studied the potential and electric field profiles of the proposed structure, the following figures will provide some insight to the threshold voltage and DIBL variation of the considered device.

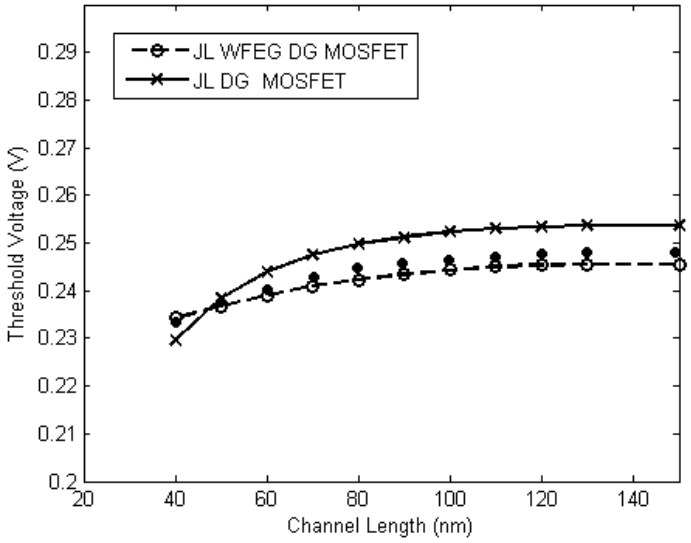


Fig.5.3.6 Variation of threshold voltage, V_{th} with channel length L for JL WFEG DG and normal JL DG MOSFET structures with same values of parameters as in table 5.3.1. MEDICI simulated data for JL WFEG DG MOSFET are represented by circular dots.

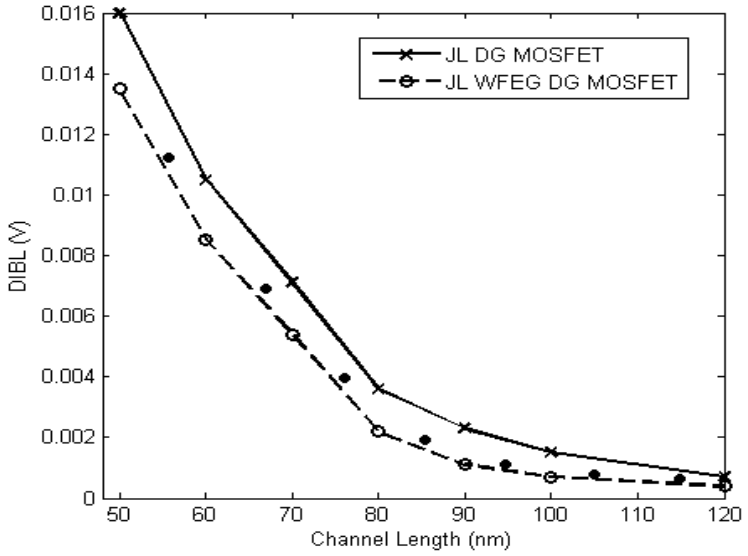


Fig.5.3.7 Variation of DIBL with channel length L for JL WFEG DG and normal JL DG MOSFET structures with same values of parameters as in Table. 5.3.1 Circular dots have the same significance as that in Figs. 5.3.5 and 5.3.6 with the same values of parameters as listed in Table 5.3.1.

Threshold voltage variation with channel length of the proposed JL WFEG DG MOSFET is depicted in Fig.5.3.6. By continuously tuning the mole fraction of binary metal alloy gate of the proposed JL WFEG DG MOS, the threshold voltage roll-off with reduction in channel length is made almost insignificant compared to significant roll-off exhibited by its normal JL DG counterpart indicating the effectiveness of the WFEG concept by protecting the proposed device structure from any

detrimental short channel effect. This has been again shown by presenting a comparative analysis of DIBL values for different channel lengths in Fig.5.3.7. The said figure undoubtedly establishes the superiority of our proposed JL WFEG DG structure compared to a normal JL DG MOS by achieving better DIBL behavior, ensuring the possibility of further device miniaturization to keep up with the ITRS specifications.

5.4. Junctionless Cylindrical Gate MOSFET with linearly graded binary metal alloy gate: a two dimensional analytical study

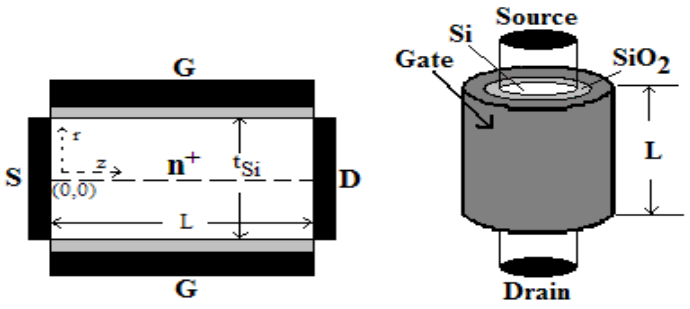
5.4.1. Overview

The preceding subsection has presented the intricacies associated with the analytical modeling and comparative performance analysis of a Junctionless Work Function Engineered Gate Double Gate MOS transistor with its normal Junctionless Double Gate counterpart without considering a linearly graded binary metal alloy gate electrode to emphasize on the effectiveness of the WFEG concept in subduing unwanted SCEs in nano scale devices. In spite of having improved performance due to the enhanced gate control over channel (by both front and back gates), the practical use of DG MOSFETs is still facing some issues of fabrication related process complexity [5.6]. The problems associated with Double Gate MOSFETs can be tackled by adopting surrounding gate/cylindrical gate MOSFETs which further enhances the gate control over the channel charge to a next level by dint of its novel geometry of completely wrapping the silicon channel with gate electrode, which in turn increases the device density in ICs with the added benefits of exhibiting significant improvement in sub-threshold behaviour along with outstanding imperviousness against detrimental Short Channel Effects (SCEs). Recent research endeavors on surrounding gate has already been discussed in details in the literature survey section [5.14-5.16]. In addition to this, the much discussed concept of Work Function Engineered gate electrode can be incorporated into a surrounding cylindrical gate MOSFET by considering a binary metal alloy gate electrode where the mole fractions of constituent metals are continuously adjusted from the source side to drain side ensuing remarkable improvement in device short channel behaviour. In view of this, the current section of this chapter will investigate a detailed analytical modeling based comparative performance analysis of a Junctionless Cylindrical Work Function Engineered Gate MOSFET with respect to its normal Junctionless Cylindrical equivalent to reap the compound benefits of junctionless cylindrical gate device structure along with gate material engineering technique.

5.4.2. Analytical Modeling

It has already been discussed in the previous section that physics behind the operation of Junctionless device bear no resemblance with that of a junction based device. In case of normal junction based devices, the conduction of current is dependent on the creation of an inversion channel by inducing a layer of minority carriers at the substrate-gate dielectric interface achieved by by the application of suitable gate bias. On the contrary, current conduction in a junctionless device is primarily due to the depletion or accumulation of majority charge carriers from the heavily doped silicon substrate by applying suitable gate bias. Current in conventional junction based is attributed by the conduction of minority carriers through the narrow inverted channel formed near the interface of substrate and gate oxide, which is in sharp contrast to the case of a Junctionless device, where the flow of majority carriers through the entire volume of the silicon film contributes to the resulting device current [5.8-5.10].

A schematic cross-sectional view of a Junctionless Cylindrical gate MOSFET with a binary metal alloy as gate electrode has been presented in Figure 5.4.1. As the device cross-section is cylindrical in nature, a cylindrical coordinate system has been adopted with radial and horizontal coordinates represented by 'r' and 'z' respectively. The device structure is assumed to be symmetrical such that the potential and electric field in the channel will not vary along the angular direction. Depending on this particular assumption, the angular direction of the cylindrical coordinate system can be neglected for the sake of mathematical brevity reducing the three dimensional scenario into a two dimensional one. This makes a two dimensional approach suitable for the analytical modeling of the present device structure [5.23].



(a) (b)

Figure 5.4.1 (a) Two dimensional cross-sectional view of a Junctionless WFEG Cylindrical Gate MOSFET considering channel length along z-axis (b) Device Structure

The gate electrode of the proposed structure is considered to be comprised of a binary metal alloy with linearly varying constituent mole fraction along channel direction. Thus the effective work function of the gate electrode can be formulated as [5.21]:

$$\phi_{meff}(z) = (z/L)\phi_2 + (1 - z/L)\phi_1 \tag{5.4.1}$$

Where ϕ_1 and ϕ_2 represents the pure constituent work functions of Platinum and Tantalum respectively. The z component (along the horizontal direction) is normalized with channel length L.

5.4.2.1. Channel Potential Modeling

Considering cylindrical device cross section, the an expression for channel surface potential of the proposed Work Function Engineered Gate Cylindrical MOSFET (WFEG CG MOS) can be formulated by solving the cylindrical Poisson's equation (reduced to two dimension) given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \varphi(r,z)}{\partial r}\right) + \frac{\partial^2 \varphi(r,z)}{\partial z^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \tag{5.4.2}$$

where $\varphi(r,z)$ is the 2-D channel potential profile, N_{ch} is the uniform channel doping and ε_{Si} is the silicon permittivity.

Assuming Young's parabolic potential profile [5.24], the 2D channel potential varying along both radial and horizontal directions can be written as:

$$\varphi(r,z) = \varphi_f(z) + d_1(z)r + d_2(z)r^2 \quad \text{for} \quad 0 \le z \le L; 0 \le r \le {t_{Si}}/{2} \tag{5.4.3}$$

Where $\varphi_f(z)$, $d_1(z)$ and $d_2(z)$ are the functions of z only.

The channel length has been considered along the z direction while the channel thickness along the radial direction keeping the origin at the centre of the silicon film.

Following the basics of analytical device modeling from the previous chapters, it can be stated that formulation of an analytical expression for channel potential requires the solution of the two dimensional Poisson's equation (eq.5.4.2) considering the device boundary conditions listed below [5.25]:

1. Surface potential of the channel is given by:

$$\varphi_s(z) = \varphi(r = R = {}^{t_{Si}}\!/_{2}, z)$$

Where, R is the radius of the cylindrical channel and is equal to half of channel thickness i.e. $t_{Si}/2$.

2. Channel central potential is given by:

$$\varphi_C(z) = \varphi(r = 0, z)$$
$$\therefore \varphi_C(z) = \varphi_f(z)$$

3. Channel central electric field is given by:

$$\left.\frac{d\varphi(r,z)}{dr}\right|_{r=0} = 0 \Rightarrow d_1(z) = 0$$

4. Electric field at the surface of the channel is given by:

$$\left.\frac{d\varphi(r,z)}{dr}\right|_{r=R} = \frac{\varepsilon_{gox}}{\varepsilon_{Si}}\left[\frac{V_{GS} - V_{FB} - \varphi_s(z)}{t_{eff}}\right]$$

Where $t_{eff} = R\ln\left(1 + {}^{t_{gox}}\!/_{R}\right)$

V_{FB} is the flat band voltage of the binary metal alloy gate and is given by $\left(V_{FB} = \phi_{meff}(z) - \phi_{Si} = \phi_1 + (\phi_2 - \phi_1)\left(\frac{z}{L}\right) - \phi_{Si}\right)$, t_{gox} is the gate oxide thickness and ε_{gox} is the relative permittivity of the gate oxide. Thus, gate oxide capacitance can be expressed as $C_{gox} = {}^{\varepsilon_{gox}}\!/_{t_{gox}}$ measured in per unit area.

Considering the above mentioned boundary conditions, eq. 5.4.3 can be re-written as follows to give an expression of total channel potential:

$$\varphi(r,z) = \varphi_C(z) + \frac{C_{gox}}{2R\varepsilon_{Si}}\left(V_{GS} - V_{FB} - \varphi_S(z)\right)r^2 \qquad (5.4.4)$$

Substitution of equation (5.4.44) into the cylindrical Poisson's equation and subsequent simplification results in the differential equation of central channel potential expressed as:

$$\frac{d^2\varphi_C(z)}{dz^2} - \frac{\varphi_C(z)}{\eta^2} - \frac{\phi_{meff}(z)}{\omega^2} = \frac{qN_{ch}}{\chi\varepsilon_{Si}} - \frac{V_{GX}}{\omega^2} \qquad (5.4.5)$$

Where $V_{GX} = V_{GS} + \phi_{Si}$, $\eta^2 = \chi/\gamma$, $\omega^2 = \chi/\beta$ and

$$\chi = \left\{1 - \frac{C_{gox}\tau r^2}{2R\varepsilon_{Si}}\right\},\ \beta = \frac{2C_{gox}}{R\varepsilon_{Si}}\left\{1 - \frac{C_{gox}\tau R}{2\varepsilon_{Si}}\right\},\ \gamma = \frac{2C_{ox}\xi}{R\varepsilon_{Si}},\ \tau = \frac{1}{\left(1 + C_{gox}R/2\varepsilon_{Si}\right)}$$

Solving the obtained differential equation finally yields an expression for the central electrostatic potential in the silicon channel and is given as:

$$\varphi_C(z) = P_1 e^{z/\eta} + P_2 e^{-z/\eta} + \left(\eta^2/\omega^2\right)\left(\phi_1 - \phi_2\right)\left(z/L\right) + \left[\frac{qN_{ch}\eta^2}{\chi\varepsilon_{Si}} - \frac{\phi_1\eta^2}{\omega^2} + \frac{V_{GX}\eta^2}{\omega^2}\right] \tag{5.4.6}$$

Finding the coefficients of this differential equation will depict the exact nature of channel central electrostatic potential. A complete picture of the nature of variation of the formulated central potential can be obtained by calculating the two coefficients P_1 and P_2 in the expression of central potential (vide eq. 5.4.6) taking into account the boundary condition of channel potential at the source and drain extremities of a junctionless device as $\varphi_C(x=0) = 0$ and $\varphi_C(x=L) = V_{DS}$ respectively [5.23]. The evaluated coefficients are given as:

$$P_1 = \frac{V_{DS} - \left(\eta^2/\omega^2\right)\left(\phi_1 - \phi_2\right) - \left[\frac{qN_{ch}\eta^2}{\chi\varepsilon_{Si}} - \frac{\phi_1\eta^2}{\omega^2} + \frac{V_{GX}\eta^2}{\omega^2}\right]\left(1 - e^{-L/\eta}\right)}{e^{L/\eta} - e^{-L/\eta}}$$

$$P_2 = \frac{-V_{DS} + \left(\eta^2/\omega^2\right)\left(\phi_1 - \phi_2\right) + \left[\frac{qN_{ch}\eta^2}{\chi\varepsilon_{Si}} - \frac{\phi_1\eta^2}{\omega^2} + \frac{V_{GX}\eta^2}{\omega^2}\right]\left(1 - e^{L/\eta}\right)}{e^{L/\eta} - e^{-L/\eta}}$$

5.4.2.2. Threshold Voltage Modeling

Potential minima can be defined as the position along the channel length at which the potential reduces to its minimum value. After formulating the expression of channel central electrostatic potential (vide eq. 5.4.6), the central potential minima (z_{min}) can be easily obtained by calculating the first order derivative of eq. 5.4.6 and equating it to zero and is written as:

$$z_{\min} = \frac{\left\{\frac{\eta^4(\phi_2-\phi_1)}{\omega^2 L}\right\} - \left\{\eta\left(P_1-P_2\right)\right\}}{\left(P_1+P_2\right)} \tag{5.4.7}$$

Substituting the expression for z_{min} in eq. 5.4.6, minimum central potential can be obtained. Now, by using the condition $\varphi_{C,\min} = 0$, the resulting expression of minimum central potential can be calculated for V_{GS} in order to find out the expression for device threshold voltage [5.23] given by:

$$V_{TH} = \left(\omega^2/\eta^2\right)\left[-P_1 e^{z_{\min}/\eta} - P_2 e^{-z_{\min}/\eta}\right] - \left(\phi_1-\phi_2\right)\left(z_{\min}/L\right) - \frac{qN_{ch}\omega^2}{\chi\varepsilon_{Si}} + \phi_1 - \phi_{Si} \tag{5.4.8}$$

Drain Induced Barrier Lowering (DIBL) is simply the difference between the device threshold voltages considered at a low and a high value of drain bias respectively and can be calculated from the following expression:

$$DIBL = V_{TH}\left(V_{DS} = 0.1V\right) - V_{TH}\left(V_{DS\_HIGH}\right). \tag{5.4.9}$$

5.4.2.3. Drain Current Modeling

The proposed Junctionless WFEG Cylindrical MOSFET device considered so far is an ultra scaled device where the device channel length is in nanometer scale. The current characteristic of such low dimensional semiconductor device is quite expected to be affected by inevitable Short Channel Effect of Channel Length Modulation (CLM) resulting in a finite slope in the drain characteristics beyond saturation. Thus, accurate modeling of drain characteristic of such a short channel length device demands prior incorporation of various SCEs like CLM, field dependent mobility etc. which will now be presented in details in this subsection.

The resulting final expressions for drain current can be formulated as [5.21, 5.26-5.28]:

$$I_{DS} = \frac{2\pi R\mu_{neff}C_{gox}}{L\left\{1-\left(l_{eff}/L\right)+\frac{V_{DS}}{LE_{Crit}}\right\}}\left[(V_{GS}-V_{TH}')V_{DS} - \tfrac{1}{2}V_{DS}^2\right] \quad \text{(for linear region operation)} \tag{5.4.10}$$

$$I_{DS} = \frac{2\pi R \mu_{neff} C_{gox}}{L\left\{1-\left(l_{eff}/L\right)+\frac{V_{DS,sat}}{LE_{Crit}}\right\}}[(V_{GS}-V_{TH}')V_{DS,sat}-1/2V_{DS,sat}^2] \quad \text{(for saturation region operation)} \quad (5.4.11)$$

Where l_{eff} is the effective channel length measured from the drain end across which the potential difference of (V_{DS}-V_{DS},sat) is dropped beyond the point of device saturation and is obviously a function of the drain bias. V_{TH}' is the effective threshold voltage which is basically (V_{TH}-DIBL); E_{Crit} is the critical electric field at which the electron velocity v_{sat} saturates ; $V_{DS,sat}$ is the drain-to-source saturation voltage ; μ_{neff} represents the effective carrier mobility dependent on electric field given as:-

$$E_{Crit} = \frac{2v_{sat}}{\mu_{neff}} \qquad V_{DS,sat} = \frac{V_{GS}-V_{TH}}{1+\frac{V_{GS}-V_{TH}}{LE_{Crit}}} \qquad \mu_{neff} = \frac{\mu_{n0}}{1+\theta\left(V_{GS}-V_{TH}\right)}$$

Where, the low field mobility is represented by μ_{n0} and θ is considered to be a suitable fitting parameter [5.26].

The final expressions of drain current incorporating the SCEs for both linear and saturation regions can be used further to obtain the performance parameters of the Junctionless WFEG Cylindrical Gate MOSFET under consideration. The drain or output conductance of the device can be calculated by simply differentiating the drain-to-source current with respect to drain-to-source voltage, V_{DS} (keeping V_{GS} constant). Similarly, the transconductance can be obtained by differentiating the drain current w.r.t. gate to source voltage, V_{GS} (keeping V_{DS} constant) respectively and their expressions are given as:

$$g_{d,Lin} = \frac{2\pi R \mu_{neff} C_{gox}}{L}\left[\frac{\left(V_{GS}-V_{TH}'-V_{DS}\right)}{\left\{1-\left(l_{eff}/L\right)+\frac{V_{DS}}{LE_{Crit}}\right\}}+\frac{\left(dl_{eff}/dV_{DS}-1/E_{Crit}\right)\left\{\left(V_{GS}-V_{TH}'\right)V_{DS}-1/2V_{DS}^2\right\}}{L\left\{1-\left(l_{eff}/L\right)+\frac{V_{DS}}{LE_{Crit}}\right\}^2}\right] \quad \text{(for linear region operation)} \quad (5.4.12)$$

$$g_{d,sat} = \frac{2\pi R \mu_{neff} C_{gox}}{L^2} \left[\frac{\left(dl_{eff} / dV_{DS} - 1/E_{Crit} \right) \left\{ \left(V_{GS} - V_{TH}' \right) V_{DS,sat} - \frac{1}{2} V_{DS,sat}^2 \right\}}{\left\{ 1 - \left(l_{eff} / L \right) + \frac{V_{DS,sat}}{LE_{Crit}} \right\}^2} \right] \quad \text{(for saturation region operation)} \qquad (5.4.13)$$

$$g_{m,Lin} = \frac{2\pi R \mu_{neff} C_{gox}}{L \left\{ 1 - \left(l_{eff} / L \right) + \frac{V_{DS}}{LE_{Crit}} \right\}} V_{DS} \quad \text{(for linear region operation)} \qquad (5.4.14)$$

$$g_{m,sat} = \frac{2\pi R \mu_{neff} C_{gox}}{L \left\{ 1 - \left(l_{eff} / L \right) + \frac{V_{DS,sat}}{LE_{Crit}} \right\}} V_{DS,sat} \quad \text{(for saturation region operation)} \qquad (5.4.15)$$

5.4.3. Results and Discussions

This results and discussions sub section aims to describe a comparative study of the performance of the proposed junctionless WFEG CG with respect to a normal junctionless CG device (without incorporating the concept of 'work function engineered gate') on the basis of detailed analytical modeling. The 2-D MEDICI simulator data is also provided to validate the computational accuracy of the proposed model. In both the cases, simulation has been carried out with the parameter values as listed in Table 5.4.1.

Table 5.4.1 Parameter Table

Parameters	Value
Substrate doping concentration (N_{SUB})	10^{21} m^{-3}
Uniform channel- S/D doping concentration (N_{ch})	10^{26} m^{-3}
Front Oxide thickness (t_{gox})	2 nm
Film thickness (t_{Si})	20 nm
θ	0.02
μ_{n0}	~0.11m^2/V-s
v_{sat}	10^5m/s

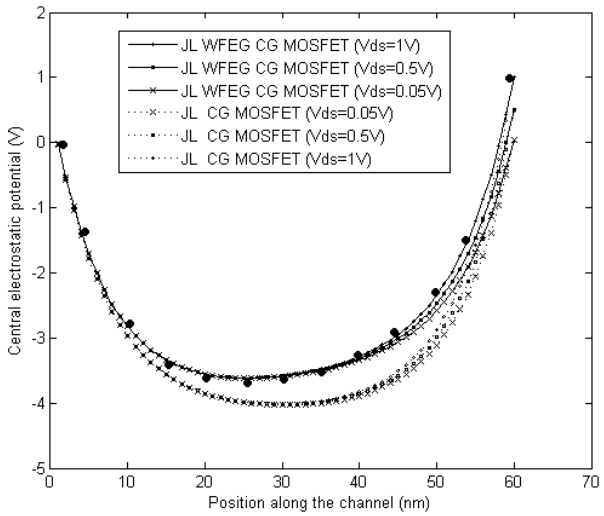


Figure 5.4.2 Variation of central electrostatic potential along the channel position of JL WFEG CG and normal JL CG MOSFETs considering channel length L = 60nm, V_{gs}=0.1V. MEDICI simulated data for JL WFEG CG MOSFET (V_{ds}=1V) are represented by circular dots.

Fig. 5.4.2 enunciates the variation of central electrostatic potential of the proposed Junctionless WFEG CG MOSFET and a normal JL CG MOSFET (without incorporating 'work function engineered gate') along the channel position considering different values of applied drain-to-source voltages. It can be easily noticed from the said figure that the parabolic symmetry is no longer maintained in such an ultra scaled device and there is a gradual shift of central potential minima towards the source end instead of being positioned at the centre of the channel. Moreover, the upward shift of potential minima of the junctionless WFEG CG MOS than that of the junctionless CG equivalent is a clear indication of the superiority of proposed WFEG structure in curbing the harmful effects of DIBL and other SCEs.

Similarly, Fig.5.4.3 depicts the variation of central electrostatic potential of JL WFEG CG and normal JL CG MOSFETs along channel position for different thicknesses of gate oxide (t_{gox}). As the gate oxide thickness increases gradually, the gate loses its sole control over the channel electrostatic charge leading to a net reduction in gate oxide capacitance shifting the position of central potential minima downwards as evident from Fig. 5.4.3. Thus, it can be deduced that devices with thinner gate oxide offers better immunity to short channel effects.

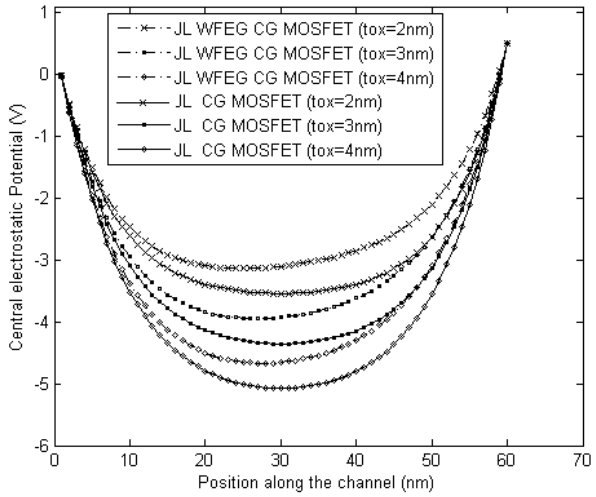


Figure 5.4.3 Central potential distribution along the channel position of JL WFEG CG and normal JL CG MOSFET for different values of gate oxide thickness t_{gox}.

The next two figures (Figs.5.4.4 and 5.4.5) illustrate the threshold voltage and subthreshold slope variation of the proposed JL WFEG CG device structure w.r.t. JL CG equivalent against different device channel lengths. The WFEG concept incorporated in the proposed device results in continuous variation of binary metal alloy mole fraction which in effect considerably reduces both Threshold Voltage Roll-Off (TVRO) and subthreshold slope, indicating suppression of short channel effects in the proposed JL WFEG CG device.

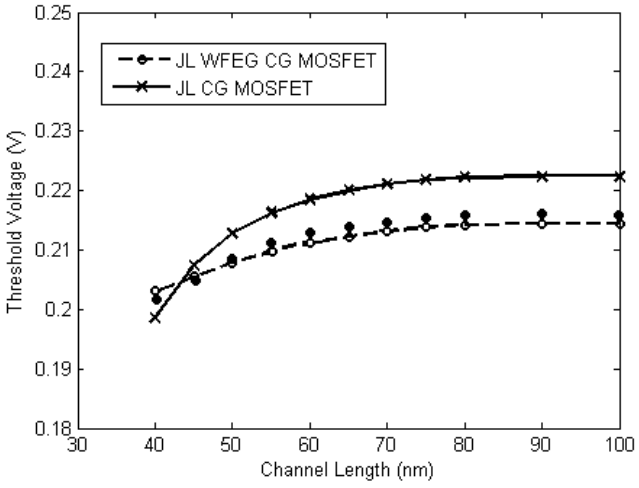


Figure 5.4.4 Variation of threshold voltage, V_{th} with channel length L for JL WFEG CG and normal JL CG MOSFET structures with same values of parameters as in Table 5.4.1. MEDICI simulated data for JL WFEG CG MOSFET are represented by circular dots.

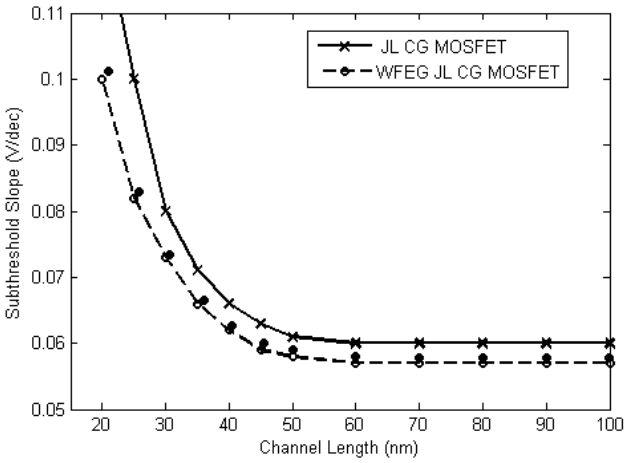


Figure 5.4.5 Fluctuation of Subthreshold slope with channel length L for JL WFEG CG and normal JL CG MOSFETs considering parameter values as in Table 5.4.1. Circular dots have the same significance as that in Figs 5.4.2 and 5.4.4 with the same values of parameters as listed in Table 5.4.1.

One of the most common SCE deteriorating the performance of short channel devices is the Drain Induced Barrier Lowering (DIBL) which illustrates the unwanted role of drain bias in controlling channel charge density attaining channel inversion before threshold condition. The variation of DIBL with respect to device channel length for both JL WFEG CG and normal JL CG MOSFETs is clearly described in the figure below (Fig. 5.4.6) which is sufficient testimony to the fact that proposed JL WFEG CG MOSFET can be chosen as a suitable alternative device for short channel operation by exhibiting much improved DIBL performance.

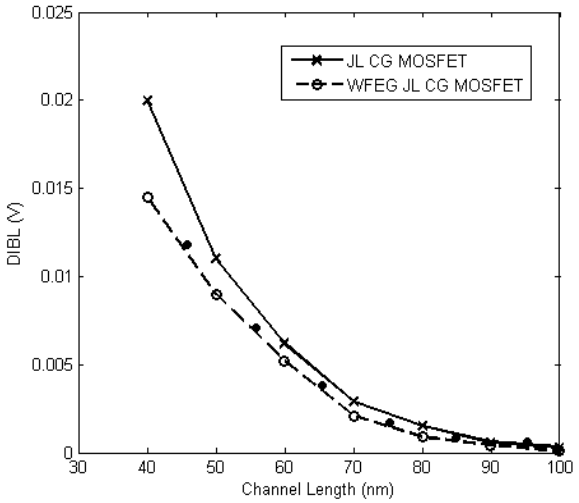


Figure 5.4.6 Variation of DIBL with channel length L for JL WFEG CG and normal JL CG MOSFET structures with same values of parameters as in Table 5.4.1. Circular dots have the same significance as that in figure 5.4.2 and 5.4.4 with the same values of parameters as listed in Table 5.4.1.

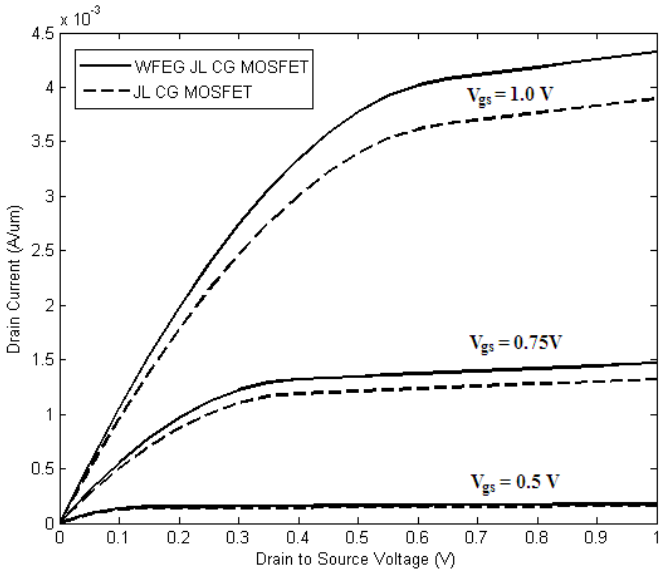


Figure 5.4.7 Output or I_D-V_{DS} characteristics of JL WFEG CG and normal JL CG MOSFET structures considering different gate biases V_{gs}: for 1V, 0.75V and 0.5V . Channel length L = 60nm and other parameters have the values listed in Table 5.4.1.

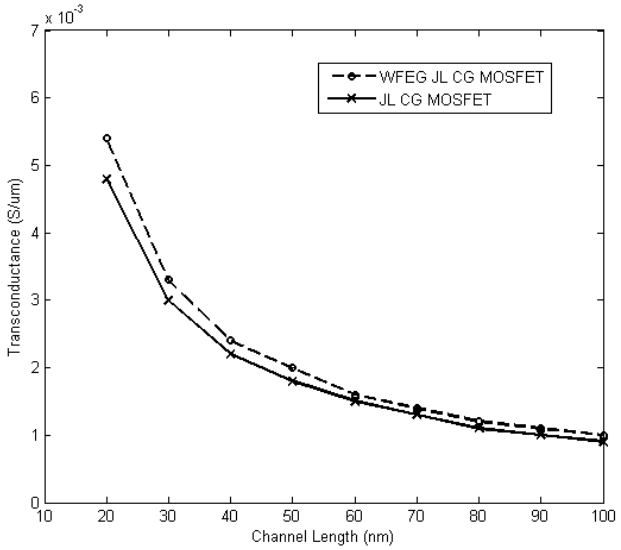


Figure 5.4.8 Variation of Transconductance, g_m with Channel Length, L for JL WFEG CG and normal JL CG MOSFET structures

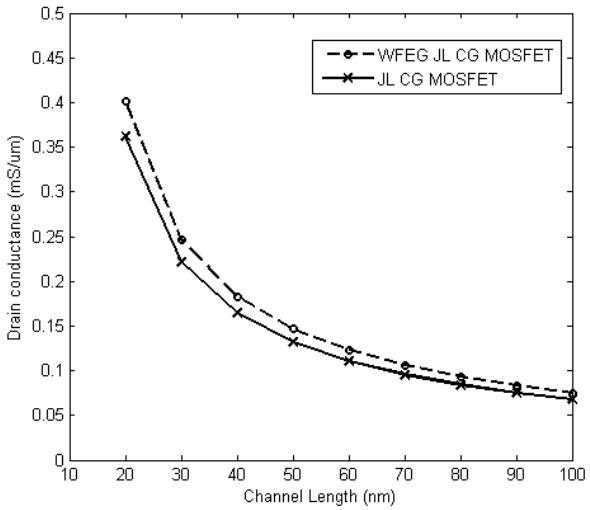


Figure 5.4.9 Variation of Drain conductance, g_d with Channel Length, L for JL WFEG CG and normal JL CG MOSFET structures

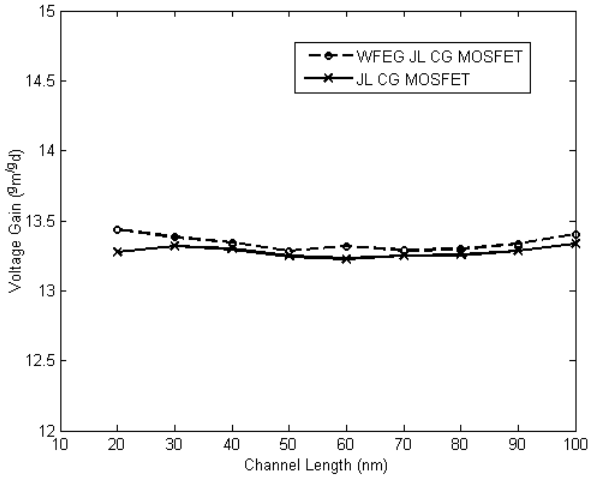


Figure 5.4.10 Variation of voltage gain (g_m/g_d) with Channel Length, L for JL WFEG CG and normal JL CG MOSFET

Having studied the central potential profile, threshold voltage and subthreshold slope of the proposed device structure, Figs. 5.4.7 to 5.4.10 will now investigate a comparative study of device current characteristics of the proposed structure under consideration with respect to its normal JL CG counterpart. Operation of a device having such aggressively down scaled channel length (L=60nm) will obviously be affected by the detrimental Channel Length Modulation (CLM) effect resulting in a finite slope in the saturation region of the drain characteristics beyond the saturation voltage as evident from Fig.5.4.7. Furthermore, the threshold voltage of our proposed JL WFEG CG being lower improves current drivability of the device. The variations of transconductance (g_m), drain

conductance (g_d) and voltage gain of the JL WFEG CG MOS structure are shown in Figs. 5.4.8, 5.4.9 & 5.4.10 respectively. The removal of uneven transition of channel electric field as a direct effect of the WFEG structure results in a lower value of g_d. Again, a higher drain current of the WFEG structure leads to an increased transconductance, g_m, thereby increasing the voltage gain (g_m/g_d) of our proposed JL WFEG CG MOS structure.

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Relevant Publications:

- **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. “Threshold voltage modeling and performance comparison of a novel linearly graded binary metal alloy gate junctionless double gate metal oxide semiconductor field effect transistor.” In **Indian Journal of Physics, Springer,** Vol. 89, No.6, pp. 593–598, 2015
- **Saheli Sarkhel** and Subir Kumar Sarkar. “A comprehensive two dimensional analytical study of a Nanoscale Linearly Graded Binary Metal Alloy Gate Cylindrical Junctionless MOSFET for improved short channel performance.” In **Journal of Computational Electronics, Springer**, Vol.13, pp. 925-932, 2014
- **Saheli Sarkhel**, Navjeet Bagga and Subir Kumar Sarkar. “Analytical Modeling and Simulation of Work-function Engineered Gate Junctionless high-k dielectric Double Gate MOSFET: A Comparative Study.” In **Michael Faraday IET International Summit-2015 (MFIIS 2015)**, An IET International Conference 12th -13th September, 2015, Kolkata.

Chapter 6

Improvised Tunnel Field Effect Transistors (TFETs) with Work Function Engineered gate electrode: a possible alternative to nano scale MOSFETs

CHAPTER VI

6.1. Introduction

Throughout this dissertation, the ongoing research trends in the field of semiconductor devices have been discussed covering the intricate details. It is apparent from the essence of this thesis work that today's microelectronics industry is predominantly driven by the design and implementation of low power nanoscale devices to meet the accrescent technology demands of human beings. The primary area of focus in contemporary ULSI industry has been continuous scaling down of device dimension along with increment in the speed of operation and reduction of circuit power consumption. The industry has seen a long journey in pursuit of circuit performance improvement by device miniaturization starting from voluminous vacuum tubes that resulted in computers occupying large rooms, to first MOSFET with gate length of 300 micrometer to some ultra scaled MOSFETs with gate lengths of 14 nanometer or less [6.1]. Short channel devices with gate lengths in sub nano orders have led to integrated circuits containing billions of transistors realizing a multitude of complex high speed operations with minimal power dissipation. However, reduced gate length results in reduced gate capacitance, thereby increasing switching speed of the circuit. Proportionate voltage scaling on the other hand reduces device power consumption. These scaling induced performance improvements, however, come hand in hand with reduced control of gate electrode over the channel and increased effect of various parasitic capacitances which effectively degrades device performance manifested by an significant increase in various Short channel Effects (SCEs) namely Hot Carrier Effect(HCE), Threshold Voltage Roll Off (TVRO), Drain Induced Barrier Lowering (DIBL), sub-threshold slope enhancement along with an abnormal rise in leakage current flowing even if the device is in OFF state thereby increasing overall power consumption [6.2].

Out of these short channel effects deteriorating the device performance, the most basic drawback of conventional MOSFET is the non-scalability of sub-threshold swing (limited to 60mV/dec). This constraint increases device leakage current with a resultant boost in power dissipation posing a serious threat to the industry in continuing with the frantic pace of device down scaling in the days to come. Rigorous research activities have been conducted to find a solution to this threat to the industry benchmarking Moore's law with a motive to innovative alternatives to MOSFET keeping all its benefits intact.

This has paved the way for an altogether new transistor namely Tunneling Field Effect Transistors (TFETs). The fundamental difference which makes TFETs a better device alternative to conventional MOSFETs is the mechanism of current control. It is known to all that thermionic emission of free carriers from the heavily doped source region into the channel region across the

potential barrier at the source-channel junction is the governing physics behind current conduction in MOSFETs. On the other hand, current in TFETs depend on the band-to-band tunneling of charge carriers from the source valence band to the channel conduction band through the potential barrier existing at the source-channel junction. Normally, under thermal equilibrium (i.e. no external bias is applied and the device is in OFF state), this source-channel junction potential barrier is sufficiently high ensuring nominal OFF state leakage current in TFETs which therefore breaks the subthrsehold limit of 60 mV/dec (in MOSFET) and can achieve subthreshold slope less than this limiting value [6.3]. Some of the added advantages offered by TFETs are enhanced immunity against SCEs, reliability, ultra low power applications and ability to reuse the MOSFET technology due the striking structural resemblance of TFETs with MOSFET [6.4-6.6]. Moreover, TFETs have an additional advantage of temperature independence of sub-threshold swing making them a promising candidate for quasi-ideal digital switch used in critical applications involving high temperature [6.6-6.8]. These prominent advantages of TFET in sharp contrast with MOSFET make TFETs a better device than MOSFETs for low power, low voltage applications.

6.2. Recent research trends

Originally, Tunnel Field Effect Transistor is nothing but a simple p-i-n diode. TFET is basically a gated reverse biased p-i-n diode in which tunneling of the carrier take place through one band to another band. A basic TFET structure consists of source and drain regions which are heavily doped with impurities of opposite polarities, while the channel region is intrinsic in nature. However, in spite of having several operational advantages, TFETs also have certain limitations. The operating principle governing current conduction in TFETs is based on band-to-band tunneling phenomena which although aids in achieving low OFF state leakage current, is also the reason behind low ON state current in TFETs [6.10] which is far less than that required as per ITRS specification [6.11]. Several improvisations are being studied with an aim to improve the ON current of TFET. Different modifications of the gate positioning have been proposed by Vanderbeghe et.al. in the literature [6.12] where the point tunneling current component can be sufficiently eliminated by placing the gate electrode over the area near the source only. A similar structure with gate only on the source region has also been studied [6.13] showing considerable improvements.

Gate engineered MOSFETs studied in the preceding chapters undoubtedly establishes the effectiveness of 'multi gate' structures over planar single gate structures in achieving higher package density and remarkably enhanced current drivability. This has motivated the researchers to incorporate gate engineering concept in TFETs to surmount the limitation of lower ON current in TFETs. Double Gate (DG) TFETs can be regarded as a promising alternative choice by virtue of having one additional gate which increases the number of devices integrated on an IC along with a

notable enhancement in the electrostatic control of the gate over the channel leading to a proportional increment in ON state current, subthrehold slope improvement and superb immunity against harmful Short Channel Effects (SCEs) [6.14]. Many contemporary researchers are working in this domain to determine physics based accurate analytical model which will be helpful in understanding the intricacies of TFET operation. An analytical model presenting comparative performance investigation of single gate, double gate and gate all around TFETs has been proposed by Verhulst et. al [6.15] with a view to explore the role of different device parameters on the TFET current. On the other hand, Vandenberghe et. al. [6.16] proposed a new DG TFET structure where the gate electrode was placed only over the source region and subsequently developed an analytical model for this structure. Again, another group of researcher (Shen et. al. [6.17]) insinuated a new approach for modeling TFETs based on non-linear Poisson's equation.

Akin to gate engineering, the well known concept of 'gate material engineering' may also be incorporated into the basic TFET structure to serve the motive of enhancing otherwise lower ON state current in TFETs by lowering the barrier at the source-channel junction, whereas the drain-channel barrier is maintained to be high so as to suppress the OFF-current by properly choosing the workfunctions of the gate metals. A Dual Material Gate (DMG) TFET structure was proposed by M. J. Kumar et. al. [6.18], where, two metals with different work functions were amalgamated side by side realizing a single gate electrode. The disparity in work function results in an effective increase in channel electric field near the source-channel junction, thereby enhancing the tunneling of carriers from source into the channel and their subsequent conduction towards drain end leading to a proportional boost in device ON state current. Taking one step further, the concepts of 'multi gate' TFETs and 'gate material engineered' TFETs have been merged together to explore improved device functionalities in some improvised TFET structures like Dual Material Double Gate TFETs (proposed by Balamurugan et. al. [6.19]) and Dual Material Gate All Around TFETs (proposed by M.J.Kumar et.al [6.20]). Placing three metals side by side will result in a Triple Material Gate TFET structure (recently proposed by Bagga et. al. [6.21])

Exploration of the concept of gate material engineering to an extreme level has proposed the recently developed concept of 'binary metal alloy gate' which has been studied widely in MOSFETs. This innovative concept considers a binary metal alloy (A_{α} $B_{1-\alpha}$) as the gate electrode where the mole fractions of constituent metals are continuously varied horizontally from the from source side (100% A) to drain side (100% B) along the channel length [6.22-6.26]. This continuous lateral variation of effective work function of the binary metal alloy gate electrode alters the vertical electric field in the channel, which, in turn adjusts the overall channel electric field, thereby restoring the surface potential asymmetry in nano dimensional devices which consequently alleviates the DIBL effect to ensure improved device performance. Motivated by the possibility to fabricate such binary metal

alloy gate electrode [6.27-6.33], this chapter attempts to present some research endeavors to incorporate this novel concept of 'work function engineered' gate electrode into the basic TFET structure in order to realize some improvised TFET structures which can alleviate the short comings of a simple TFET.

The first section of this chapter will investigate the analytical modelling based comparative performance analysis of a Work Function Engineered Gate Double Gate (WFEG DG) TFET structure with respect to normal DG TFET. The next section will present similar analytical modelling based performance analysis of a Binary Metal Alloy Silicon-on-Nothing (BMA SON) TFET compared to its simple SON TFET equivalent with special emphasis on the effects of interface trapped charges near the source region on the device performance. Both the studies will exhibit superior performance of the work function engineered/binary metal alloy gate structures compared to their normal single material gate counterparts.

6.3. Double Gate Tunnel Field Effect Transistor with Work Function Engineered gate electrode: a 2D modeling approach to investigate superior Drain Current Performance

6.3.1. Overview

From a detailed study of the journey of semiconductor devices from MOSFETs to TFETs, it can be stated for sure that TFETs have opened a new research conduit and will replace conventional MOSFETs to continue the unimpeded development of low dimensional devices. Tunneling Field Effect Transistors (TFETs) with an inherent feature of band-to-band carrier tunneling assisted current conduction exhibits remarkably improved short channel effect immunity and has thus been playing a key role in continuing the unhindered progress of device dimension miniaturization. This subsection aims to explore a new venture of incorporating the recently popular innovative concept of work function engineered binary metal alloy gate electrode into a Double Gate Tunneling Field Effect Transistor (TFET), thereby presenting a new device structure, a Work Function Engineered Double Gate Tunneling Field Effect Transistor (WFEDG TFET). The 2D Poisson's equation has been explicitly solved considering proper boundary conditions of the proposed Work Function Engineered Double Gate Tunneling Field Effect Transistor in order to formulate an expression for the surface potential of the proposed device which can be used to derive an expression for channel electric field. Subsequently, exhaustive integration has been carried out on tunneling generation rate over the entire tunneling window to obtain an expression of tunneling current in TFET. The analytical results thus obtained are studied extensively in terms of surface potential, electric field and drain characteristics to pursue a comparative performance investigation of WFEDG TFET with respect to a normal DG TFET with an intention to establish supremacy of our proposed structure.

6.3.2. Analytical Modeling

Fig. 6.3.1 illustrates a schematic cross-sectional view of the proposed Work Function Engineered Double Gate Tunneling FET (WFEDG TFET) structure with Tantalum-Platinum alloy gate electrode. t_{fox}, t_{box} and t_{Si} are the thicknesses of front gate oxide, back gate oxide and silicon channel respectively. From the device structure it must be noted that both front and back gates have been connected to the same gate bias making this a three terminal (3T) tied Double Gate structure.

The gate electrode of the proposed structure consists of a binary metal alloy with linearly varying constituent mole fraction along channel direction. Thus the effective work function of the gate electrode can be formulated as [6.23]:

$$\phi_{meff}(x) = (x/L)\phi_2 + (1-x/L)\phi_1 \tag{6.3.1}$$

Where ϕ_1 and ϕ_2 represents the pure constituent work functions of Platinum and Tantalum respectively. The x component (along the horizontal direction) is normalized with channel length L such that $\phi_{meff}(x) = \phi_1$ at x=0 (i.e. source end of the channel) and $\phi_{meff}(x) = \phi_2$ at x=L (i.e. drain end of the channel).

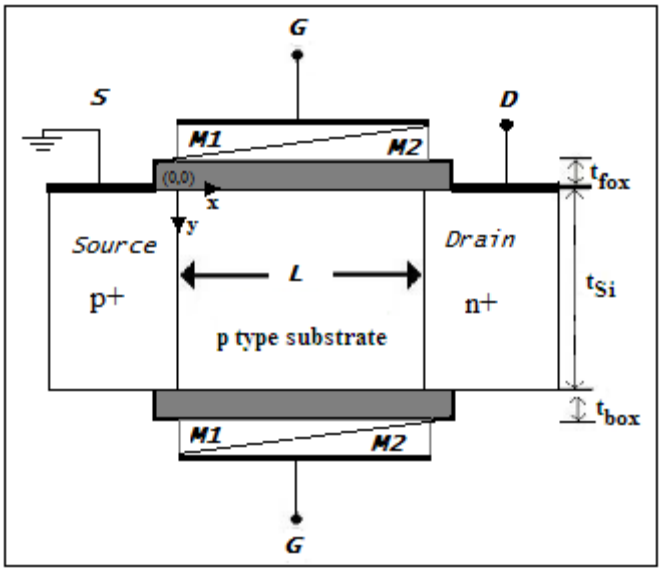

Fig. 6.3.1 Cross sectional view of the proposed n-type WFEDG TFET structure

6.3.2.1. Surface potential modeling

From the basic knowledge of device modeling, it can be said that solution of a two dimensional Poisson's equation is the first step to find an expression for channel potential of two dimensional semiconductor devices. Thus, in order to formulate an expression for channel potential of the proposed WFEDG TFET structure, the 2D Poisson's equation can be written as:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\frac{qN_{ch}}{\varepsilon_{Si}} \quad \text{for} \quad \left(0\le x\le L, 0\le y\le t_{Si}\right) \tag{6.3.2}$$

Where, $\varphi(x,y)$ represent the two dimensional channel potential, N_{ch} stands for uniform channel doping and ε_{Si} is the relative permittivity of silicon.

The analytical modeling scheme discussed in the previous chapters show that the channel potential solution of a tied/independent gate, Double Gate MOSFET resembles a parabolic form. Similarly, Young's parabolic potential approximation (PPA) [6.35] can also be used to express the two dimensional channel potential of a Double Gate TFET as:

$$\varphi(x,y)=d_1(x)+d_2(x)y+d_3(x)y^2 \qquad \text{for} \quad \left(0\le x\le L, 0\le y\le t_{Si}\right) \tag{6.3.3}$$

Device modeling techniques assume that the channel potential and electric flux are continuous at the gate oxide-silicon interface and are summarized in the following boundary conditions [6.5]:

(i) The front channel surface potential (for y=0) is given as:

$$\varphi(x,0)=\varphi_{front}(x) \tag{6.3.4}$$

(ii) The back channel surface potential (for $y=t_{Si}$) is given as:

$$\varphi(x,t_{Si})=\varphi_{back}(x) \tag{6.3.5}$$

(iii) The electric field is continuous at the front gate oxide – silicon channel interface and is given as:

$$\varepsilon_{Si}\left.\frac{d\varphi(x,y)}{dy}\right|_{y=0}=\varepsilon_{fox}\frac{\varphi_{front}(x)-V_{GS}+V_{FB,front}(x)}{t_{fox}} \tag{6.3.6}$$

(iv) Likewise, the electric field is continuous at the back gate oxide- silicon interface and is given as:

$$\varepsilon_{Si}\left.\frac{d\varphi(x,y)}{dy}\right|_{y=t_{Si}} = \varepsilon_{box}\frac{V_{GS}-\varphi_{back}(x)-V_{FB,back}(x)}{t_{box}} \tag{6.3.7}$$

where $V_{FB,\,front}(x)=V_{FB,back}(x)=\phi_{meff}(x)-\phi_{Si}$ is the front/back channel interface flat band voltage (as same set of binary metal alloy gate has been taken as front and back gate electrode), ε_{Si} is the relative permittivity of silicon channel and ε_{fox} & ε_{box} are the relative permittivities of the front and back gate oxides respectively.

Applying the above boundary conditions (Eqns.6.3.4-6.3.7), in equation 6.3.3, the co-efficient of PPA equation can be expressed as:

$$d_1(x)=\varphi_{front}(x) \qquad d_2(x)=\frac{\varepsilon_{fox}}{\varepsilon_{Si}}\frac{\varphi_{front}(x)-V_{FG}^{'}}{t_{fox}}$$

$$d_3(x)=\frac{\left[\left(\frac{\varepsilon_{box}}{\varepsilon_{Si}}\frac{V_{BG}^{'}-\varphi_{front}(x)}{t_{box}}\right)-\left(\frac{\varepsilon_{fox}}{\varepsilon_{Si}}\frac{\varphi_{front}(x)-V_{FG}^{'}}{t_{fox}}\right)\left(1+\frac{\varepsilon_{box}t_{Si}}{\varepsilon_{Si}t_{box}}\right)\right]}{\left(2+\frac{\varepsilon_{box}t_{Si}}{\varepsilon_{Si}t_{box}}\right)t_{Si}}$$

Where, $V_{FG}^{'}=V_{GS,f}-V_{FB,\,front}(x)$ and $V_{BG}^{'}=V_{GS,b}-V_{FB,back}(x)$. The structure under consideration is a tied structure having same gate bias V_{GS} applied to both front and back gates. Hence $V_{GS,f}=V_{GS,b}=V_{GS}$

Substituting the obtained co-efficient values in equations 6.3.2 and 6.3.3, the surface potential equation can be written as:

$$\frac{d^2\varphi_{front}(x)}{dx^2}+\sigma V_{BG}^{'}-\sigma\varphi_{front}(x)-\varsigma\varphi_{front}(x)+\varsigma V_{FG}^{'}=\frac{qN_{ch}}{\varepsilon_{Si}} \tag{6.3.8}$$

Where $\sigma=\dfrac{2\left(\varepsilon_{box}/\varepsilon_{Si}t_{box}\right)}{\left(2+\left(\varepsilon_{box}t_{Si}/\varepsilon_{Si}t_{box}\right)\right)t_{Si}}$ and $\varsigma=\dfrac{2\left(\varepsilon_{fox}/\varepsilon_{Si}t_{fox}\right)\left(1+\left(\varepsilon_{box}t_{Si}/\varepsilon_{Si}t_{box}\right)\right)}{\left(2+\left(\varepsilon_{box}t_{Si}/\varepsilon_{Si}t_{box}\right)\right)t_{Si}}$

By simplification and substitution of expressions, equation 6.3.8 can be re-written as:

$$\frac{d^2\varphi_{front}(x)}{dx^2}-\lambda^2\varphi_{front}(x)-\lambda^2\phi_{meff}(x)=\frac{qN_{ch}}{\varepsilon_{Si}}-\sigma\left(V_{GS,b}+\phi_{Si}\right)-\varsigma\left(V_{GS,f}+\phi_{Si}\right) \quad (6.3.9)$$

Where $\lambda^2=(\sigma+\varsigma)$.

It can be understood that eq.6.3.9 is a simple non-homogeneous differential equation of front surface potential. An expression of front surface potential can be formulated by solving eq. 6.3.9 using the knowledge of separation of variable technique and the resultant expression can be written as:

$$\varphi_{front}(x)=P_1e^{\lambda x}+P_2e^{-\lambda x}+(\phi_1-\phi_2)\left(x/L\right)+\left[\frac{\sigma}{\lambda^2}\left(V_{GS,b}+\phi_{Si}\right)+\frac{\varsigma}{\lambda^2}\left(V_{GS,f}+\phi_{Si}\right)-\phi_1-\frac{qN_{ch}}{\lambda^2\varepsilon_{Si}}\right] \quad (6.3.10)$$

A clear insight on the nature of variation of the derived front surface potential can be obtained by calculating the two coefficients P_1 an P_2 of eq. 6.3.10 by properly considering the source side and drain side front surface potential as $\varphi_{front}(x=0)=\phi_{bi,S}+V_S=-\frac{kT}{q}\ln\left(\frac{N_{sp}}{n_i}\right)+V_S$ and $\varphi_{front}(x=L)=\phi_{bi,D}+V_D=\frac{kT}{q}\ln\left(\frac{N_{dn}}{n_i}\right)+V_D$ respectively [6.36]. The calculated expressions of P_1 and P_2 are given as:

$$P_1=\frac{\phi_{bi,D}+V_D-\phi_{bi,S}e^{-\lambda L}-(\phi_1-\phi_2)-\left[\frac{\sigma}{\lambda^2}\left(V_{GS,b}+\phi_{Si}\right)+\frac{\varsigma}{\lambda^2}\left(V_{GS,f}+\phi_{Si}\right)-\phi_1-\frac{qN_{ch}}{\lambda^2\varepsilon_{Si}}\right]\left(1-e^{-\lambda L}\right)}{\left(e^{\lambda L}-e^{-\lambda L}\right)}$$

$$P_2=\frac{\phi_{bi,S}e^{\lambda L}+(\phi_1-\phi_2)-\phi_{bi,D}-V_D+\left[\frac{\sigma}{\lambda^2}\left(V_{GS,b}+\phi_{Si}\right)+\frac{\varsigma}{\lambda^2}\left(V_{GS,f}+\phi_{Si}\right)-\phi_1-\frac{qN_{ch}}{\lambda^2\varepsilon_{Si}}\right]\left(1-e^{\lambda L}\right)}{\left(e^{\lambda L}-e^{-\lambda L}\right)}$$

Where N_{sp} is the source p-type doping concentration, N_{dn} is the drain n-type doping concentration, V_D is the applied drain bias and V_S is the applied source bias (which in this case is zero as we have considered the source terminal to be grounded).

6.3.2.2. Electric field modeling

Differentiation of the channel potential expression along vertical and horizontal directions results in respective electric field expressions with a negative sign. The expression for transverse electric field can be written as [6.36]:

$$E_y = -d_2(x) - 2yd_3(x) \tag{6.3.11}$$

Similarly, the expression for lateral surface electric field can be written as:

$$E_x = -\left[\lambda P_1 e^{\lambda x} - \lambda P_2 e^{-\lambda x} + {(\phi_1 - \phi_2)}/{L}\right] \tag{6.3.12}$$

Consequently, the two dimensional total electric field can be calculated as: $E = \sqrt{E_x^{\,2} + E_y^{\,2}}$

6.3.2.3. Drain current modeling

The mechanism of current conduction in TFETs is based on tunneling of charge carriers from the filled valence band of heavily doped source to the empty conduction band of the nearly intrinsic channel across the potential barrier existing at the source-channel junction. This mandates the consideration of band-to-band tunneling probability while formulating a model for the drain current of the proposed WFEDG TFET. According to the well established Kane's model [6.37], this probability term, known as carrier generation rate, decides the effective probability of carrier tunneling and is dependent on the amount of electric field which in turn is a function of tunneling path (shown in Fig. 6.3.2).

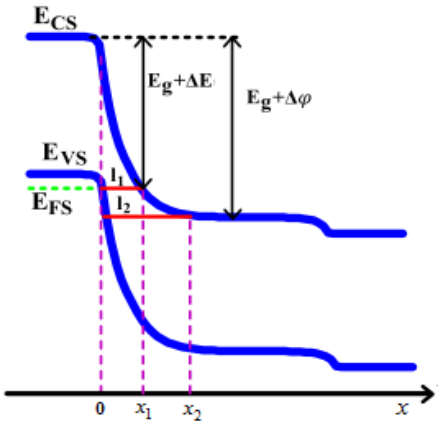

Fig. 6.3.2: Band diagram of n-type WFEDG TFET showing carrier tunneling at source channel junction

Drain current in a TFET is basically the resultant tunneling current which can be expressed as follows by integrating the tunneling carrier generation rate over the entire volume of a TFET:

$$I_D = \iiint G dx dy dz \tag{6.3.13}$$

where, G is the generation rate of the carriers given by Kane's model, x is the direction along the channel length, y is the vertical direction and z is the direction along the width of the channel. Reducing eq. 6.3.13 into a two dimensional case (for per unit width), the drain current can now be expressed as follows measured in $(A/\mu m)$:

$$I_D = \iint G dx dy \tag{6.3.14}$$

The carrier tunneling generation rate originates from traditional Kane's model and can be written as [6.37]:

$$G = A_k E^{D_k} e^{\left(-B_k/E\right)}$$

where A_k, B_k, and D_k are the Kane's parameter having values as listed in Table 6.3.1 [6.38] . The factor E in the above expression is the electric field which comprises of two contributing factors: one is the average channel electric field (E_{avg}) and while the other one is the local field (E) in the channel [6.39]. The average channel electric field (E_{avg}) depends on the effective tunneling path (l_{path}) as $E_{avg} = \left(E_g / q l_{path}\right)$.

Carriers may tunnel in both lateral and vertical directions making the tunneling phenomenon utterly complex. Thus, for the sake of mathematical brevity, lateral tunneling may be considered to be dominant while neglecting vertical tunneling [6.14]. This reduces the derivation of drain current expression into a two dimensional integration problem where the carrier generation rate is integrated along the lateral (or 'x' direction along channel length) tunneling path over the total channel thickness ('y' direction) and the drain current expression can be written as:

$$I_D = q \int_{x_1}^{x_2} \int_{y_1}^{y_2} A_k E E_{avg}^{D_k - 1} e^{\left(-B_k / E_{avg}\right)} dx dy \tag{6.3.15}$$

It can be understood from Fig. 6.3.2 that the tunneling of the carriers from source valence band to channel conduction band starts at $x = x_1$ where the surface potential reaches to $\left(\left(E_g + \Delta E\right)/q\right)$. E_g is the bandgap of silicon channel and ΔE is the difference between valence band and Fermi level of source. By using Eq. (6.3.10) x_1 can be formulated as.

$$\varphi_{front}(x)\Big|_{x=x_1} = \frac{E_g + \Delta E}{q} \tag{6.3.16}$$

Neglecting complex higher order terms, the expression of x_1 can be simplified as:

$$x_1 = \frac{E_g + \Delta E - q\left[\frac{\sigma}{\lambda^2}\left(V_{BG} + \phi_{Si}\right) + \frac{\varsigma}{\lambda^2}\left(V_{FG} + \phi_{Si}\right) - \phi_1 - \frac{qN_{ch}}{\lambda^2 \varepsilon_{Si}}\right] - qP_1 - qP_2}{q\lambda P_1 - q\lambda P_2 + q\left(\frac{\left(\phi_1 - \phi_2\right)}{L}\right)} \tag{6.3.17}$$

Similarly, when the channel potential reaches to $\left(\left(E_g + \Delta\varphi\right)/q\right)$ at a certain position along the channel (let at $x = x_2$) the tunneling of the carrier stops. $\Delta\varphi$ is the difference between the source valence band and channel conduction band. x_2 can again be calculated as:

$$\varphi_{front}(x)\Big|_{x=x_2} = \frac{E_g + \Delta\varphi}{q} \tag{6.3.18}$$

Similarly neglecting higher order terms, expression for x_2 can be simplified as:

$$x_2 = \frac{E_g + \Delta\varphi - q\left[\frac{\sigma}{\lambda^2}\left(V_{BG} + \phi_{Si}\right) + \frac{\varsigma}{\lambda^2}\left(V_{FG} + \phi_{Si}\right) - \phi_1 - \frac{qN_{ch}}{\lambda^2 \varepsilon_{Si}}\right] - qP_1 - qP_2}{q\lambda P_1 - q\lambda P_2 + q\left(\frac{\left(\phi_1 - \phi_2\right)}{L}\right)} \tag{6.3.19}$$

The channel distance between these two points (i.e. $x_2 - x_1$) actually represents the effective tunneling path over which effective carrier tunneling is taking place. As the source region is heavily doped, there is no depletion region extension into source side. Therefore, the effective tunneling path $l_{path} = x_2 - x_1$ [6.14] is assumed to be present solely in the channel region. The two points x_1 and x_2 thus define the limits of integration used to get tunneling window through which the carriers tunnel across the junctions [6.21]. Having calculated the effective tunneling path, eq. 6.3.15 can be re-written as:

$$I_D = q\int_{x=x_1}^{x=x_2}\int_{y=0}^{y=t_{si}} A_k E \frac{E_g^{D_k-1}}{q^{D_k-1}x^{D_k-1}} e^{\left(-qxB_k/E_g\right)} dxdy \tag{6.3.20}$$

Here, in this expression, the resultant electric field can be expressed as a function of both lateral and vertical electric fields Ex and Ey respectively. Thus, substituting the expressions for lateral and vertical electric fields from equations 6.3.11 and 6.3.12 in the expression of E in eq. 6.3.20, the resultanat expression for electric field E can be written as follows:

$$E = [\kappa^2 + d_2^2(x)]^{1/2}\left[1 + \frac{\tau x}{\kappa^2 + d_2^2(x)} + \frac{2yd_2(x)d_3(x)}{\kappa^2 + d_2^2(x)}\right]$$

Where, $\kappa^2 = \lambda^2(P_1 - P_2)^2 + 2\lambda(P_1 - P_2)\left(\frac{\phi_1 - \phi_2}{L}\right) + \left(\frac{\phi_1 - \phi_2}{L}\right)^2$ and $\tau = \lambda^3(P_1^2 - P_2^2) + \lambda^2(P_1 + P_2)\left(\frac{\phi_1 - \phi_2}{L}\right)$

Some higher order terms have been neglected for avoiding unnecessary mathematical complexity.

Next, the resultant expression of electric field E is substituted in equation 6.3.20 and the resulting expression has been integrated involving tiresome double integration along 'x' and 'y' coordinates to obtain a compact analytical expression of the drain current by considering various simplifactions and is given by [6.14, 6.21]:

$$I_D = \frac{qA_k E_g^{D_k-1}}{q^{D_k-1}}[\kappa^2 + d_2^2(x)]^{1/2}\left\{\left(M(x_2) - M(x_1)\right)\left[t_{si} + \frac{t_{si}^2 d_2(x)d_3(x)}{\kappa^2 + d_2^2(x)}\right] + \left[\frac{\tau t_{si}}{\kappa^2 + d_2^2(x)}\right]\left(N(x_2) - N(x_1)\right)\right\} \tag{6.3.21}$$

where the x-dependent functions M (x) and N (x) are defined as

$$M(x) = \frac{E_g e^{\left(-B_k q/E_g\right)x}}{B_k q x^{D_k}}\left\{\frac{E_g(D_k - 1)}{qB_k} - x\right\} \quad \text{and} \quad N(x) = \frac{E_g e^{\left(-B_k q/E_g\right)x}}{B_k q x^{D_k}}\left\{\frac{E_g(D_k - 2)}{qB_k}x - \frac{E_g^2(D_k - 2)(D_k - 1)}{q^2 B_k^2} - x^2\right\}$$

6.3.3. Results and Discussions

This subsection investigates an in depth analytical modeling based performance comparison of the proposed WFEDG TFET in contrast to a normal DG TFET. SILVACO ATLAS simulator data have also been provided to validate the computational accuracy of the proposed analytical model [6.40]. In both the cases, simulation has been carried out with the parameter values as listed in Table 6.3.1.

Table 6.3.1: Parameter Table

Parameters	Value
Substrate doping concentration (p type)	10^{23} m^{-3}
Source doping concentration (p+)	$6 \times 10^{26} m^{-3}$
Drain doping concentration (n+)	10^{24} m^{-3}
Channel Length	60 nm
Front Oxide thickness (t_{fox})	3 nm
Back Oxide thickness (t_{box})	3 nm
Film thickness (t_{Si})	10 nm
Kane's Parameter	
A_k	3.5×10^{21} $m^{-1/2}V^{-5/2}s^{-1}$
B_k	22.5×10^6 V/cm
D_k	2.5 for indirect tunneling 2 for direct tunneling

The results shown in this subsection has been obtained from the band-to-band tunneling drain current modeling of the proposed WFEDG TFET structure based on the solution of 2D Poisson's equation considering Kane's model. The first figure, Fig. 6.3.3 shows the variation of channel surface potential along lateral position of the channel for different values gate-to-source bias of the WFEDG TFET under consideration and its double gate counterpart. From the basic physics of TFET, the bias conditions V_{GS}=0 volts and V_{DS}=V_{DD} volts represent device OFF state while the bias conditions V_{GS}=V_{DD} volts and V_{DS}=V_{DD} volts represents device ON state. When the TFET is in OFF state, there is no overlap between source valence band and channel conduction band ideally preventing the tunneling of any carrier from source to channel. When the device is switched ON by applying appropriate biasing, the source-to-channel potential barrier height gets lowered causing the source valence band to overlap with the channel conduction band encouraging tunneling of charge carriers from source to channel region. As the gate voltage is increased gradually, the barrier height gets more and more lowered as noticeable in Fig. 6.3.3 resulting in enhanced rate of carrier tunneling with a subsequent increase in drain current. It can also be observed from the same figure that the surface potential barrier height at the source-channel junction is lowered for the proposed WFEDG

TFET as compared to its DG counterpart, resulting in improved current driving capacity of the WFEDG TFET for obvious reasons.

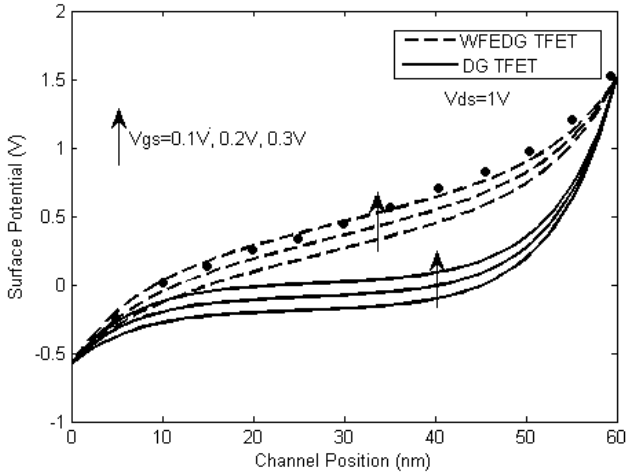

Fig. 6.3.3. Variation of surface electrostatic potential along channel position of proposed WFEDG TFET and normal DG TFET having channel length of 60nm. Circular dots represent SILVACO ATLAS simulated data for WFEDG TFET (V_{ds}=1V, V_{gs}= 0.3 V) with the same values of parameters as listed in Table 6.3.1.

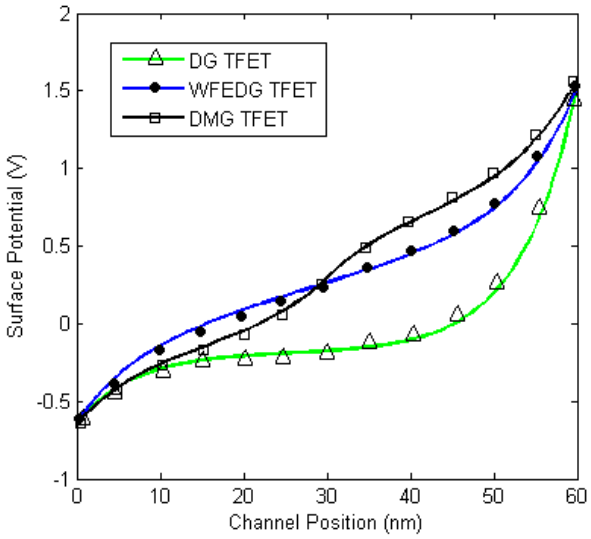

Fig. 6.3.4. Variation of surface electrostatic potential along channel position of WFEDG, DG and DMG TFETs having channel lengths of 60nm. Symbols represent SILVACO ATLAS simulated data with the same values of parameters as listed in Table 6.3.1.

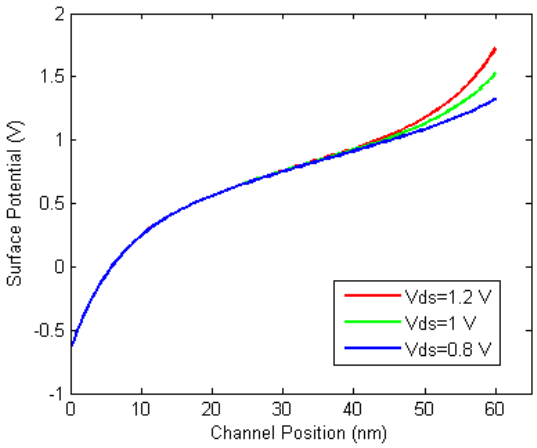

Fig. 6.3.5. Variation of surface electrostatic potential along channel position of WFEDG TFET having channel length of 60 nm considering different values of drain bias keeping V_{gs}=0.6 V

A comparative surface potential analysis of the proposed WFEDG TFET with that of normal Double Gate (DG) and Dual Material Gate (DMG) TFETs along the channel position is potrayed in Fig. 6.3.4. It has been elaborately discussed that the essence of 'work function engineering' lies in modifying the vertical (subsequently the overall) electric field by placing two metals with dissimilar work functions adjacently forming a typical Dual Material Gate (DMG) structure. The presence of two metals having two different work functions creates a step like feature in the surface potential profile as evident from Fig. 6.3.4. This concept has been extended further by using a binary metal alloy $A_{\alpha}B_{1-\alpha}$ as gate electrode whose effective work function can be varied by continuous lateral concentration variation of the mole fractions of the constituent metals starting from the source side (100 % A) towards drain side (100 % B), which consequently adjusts the total electric field existing in the channel, thereby restoring asymmetricity in surface potential profile of a nano dimensional device. As a result, there is considerable reduction in barrier height at source-channel junction enhancing the carrier tunneling probability (and subsequently the overall device current) in the proposed WFEDG TFET in sharp contrast with its DMG counterpart.

The linearly graded work function of the WFEDG TFET gate electrode introduces an x-dependent term in the final expression of surface potential (vide eq. 6.10) which is responsible for the slightly linear nature of surface potential of WFEDG TFET as compared to DG TFET with single metal gate electrode. Moreover, it can be observed from Fig. 6.3.4 that the surface potential profile of the WFEDG TFET structure near the source-channel barrier is shifted slightly upwards compared to those of DG and DMG TFETs, which is an obvious indication of enhanced carrier tunneling at the source-channel junction and subsequent boost in the current driving ability of the proposed device. The surface potential profile of WFEDG TFET for different values of drain-to-source voltages is

depicted in Fig. 6.3.5 keeping the gate-to-source voltage constant. It is clearly visible from the said figure the surface potential increases with an increase in drain bias V_{DS} only near the drain end, thereby screening the tunneling junction at the source side from any random variation in drain voltage, subsequently reducing the DIBL effect [6.41].

Having investigated the surface potential profiles, the nature of electric field variation along channel position of the proposed WFEDG TFET has been extensively studied in the next set of results i.e Figs. 6.3.6 to 6.3.8. The lateral and transverse electric fields in the silicon channel are illustrated in Figs. 6.3.6 and 6.3.7 respectively. Increasing the gate voltage turns ON the TFET and the band bending is more near the source-channel junction. An increase in band bending results in a proportional increase in the junction electric field, which, in turn, significantly enhances carrier tunneling. It must also be noted from Fig. 6.3.6 that, at the middle of the channel, the lateral electric field is somewhat increased compared to the source and drain ends which is attributed to an increase in vertical electric field component on applying higher gate voltages. Fig. 6.3.7 clearly shows that the electric field at the drain end is much reduced than that at the source end, thereby mitigating the problem of ambipolar conduction in the TFET structure, which, in turn significantly reduces the unwanted OFF state leakage current making the proposed structure suitable for low power applications. The resultant electric field in the channel (which is a combination of both lateral and transverse electric fields) is depicted in Fig.6.3.8 from which it can be understood that the electric field near the source end is much higher than that near the drain region resulting in an enhanced carrier tunneling at the junction between heavily doped source and almost intrinsic channel regions [6.42] leading to an increased ON current, while simultaneously reducing ambipolar carrier tunneling at drain-channel junction leading to decreased OFF current as discussed before.

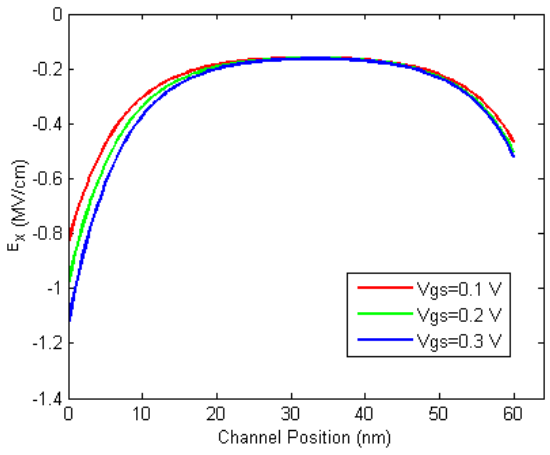

Fig.6.3.6 Variation of lateral surface electric field (x-component) along channel position of WFEDG TFET considering different gate voltages

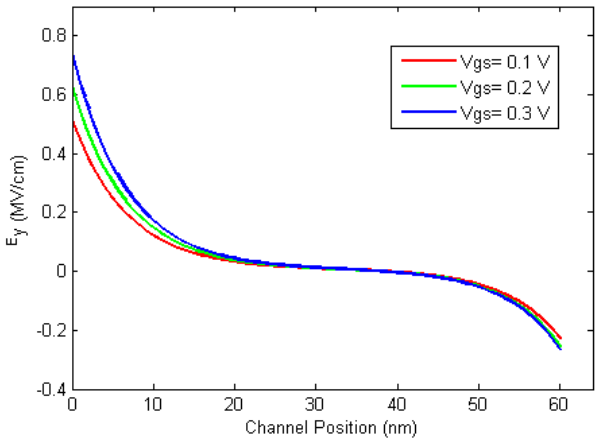

Fig.6.3.7 Variation of transverse surface electric field (y-component) along channel position of WFEDG TFET considering different gate voltages

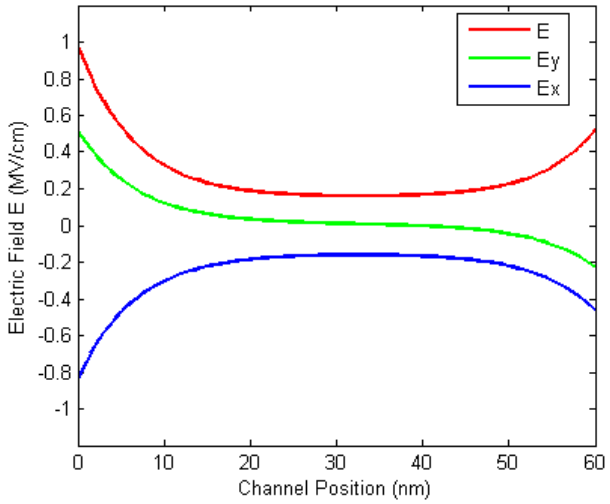

Fig 6.3.8. Variation of resultant surface electric field along channel position of WFEDG TFET considering gate bias to be 0.1 V and drain bias to be 1 V

Now, the device current characteristics will be elaborated in the following figures. A comparative analysis of WFEDG TFET transfer characteristics is shown in Fig. 6.3.9 with respect to its DG and DMG counterparts. A higher electric field at the source-channel tunneling junction of the WFEDG structure increases the carrier tunneling probability which is manifested by a substantial increase in overall device current. Dependence of drain current with varying silicon channel thickness for the proposed WFEDG TFET structure is shown in Fig.6.3.10 which indicates a an increase in drain current with the gradual reduction in channel thickness attributed by a resultant decrease in the capacitive effects of the body. It can also be observed from this figure that for similar channel thickness, the WFEDG TFET exhibits enhanced drain current compared to its DMG counterpart.

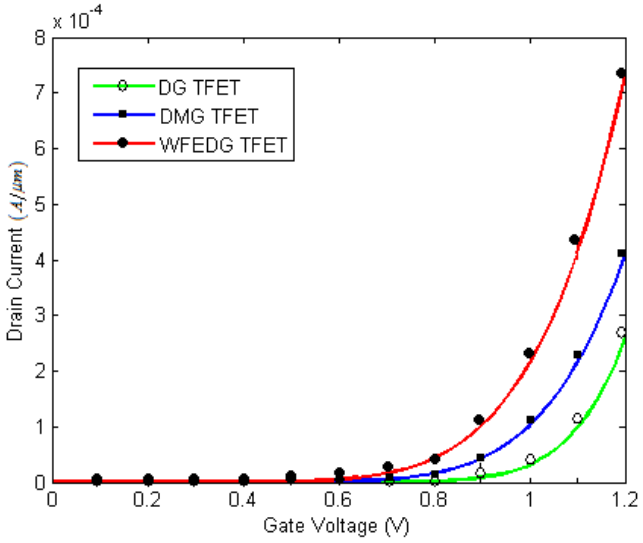

Fig.6.3.9 Transfer or I_D-V_{GS} characteristics (in linear scale) of WFEDG TFET and normal DG TFET structures having channel length of 60nm. SILVACO ATLAS simulated data are shown by symbols.

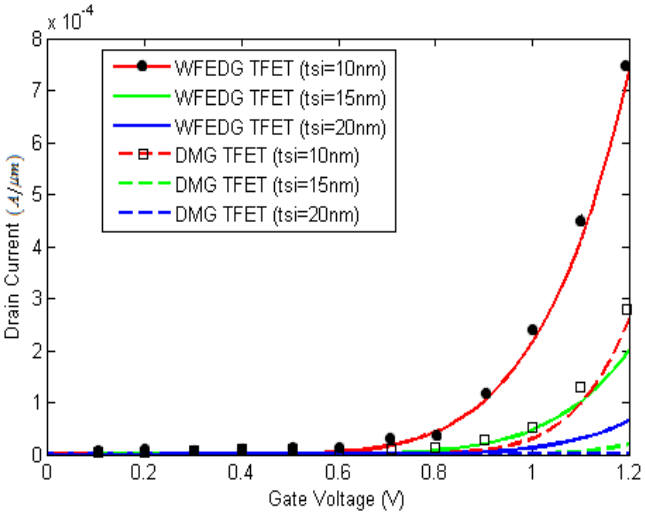

Fig.6.3.10. Transfer or I_D-V_{GS} characteristics (in linear scale) of WFEDG TFET and DMG TFET with channel length of 60 nm for different values of channel thicknesses. SILVACO ATLAS simulated data for t_{Si}=10 nm are shown by symbols.

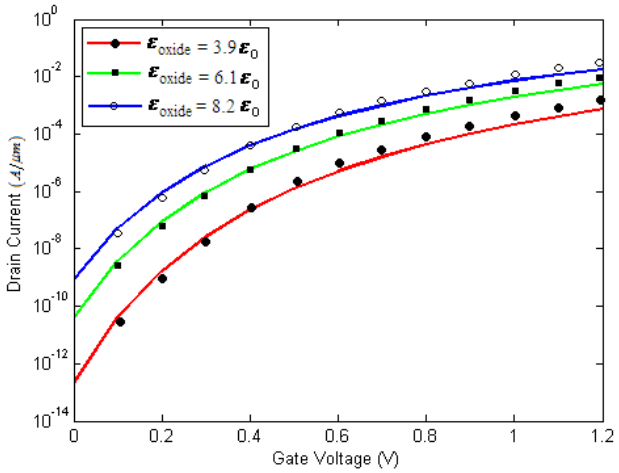

Fig. 6.3.11. Transfer or I_D-V_{GS} characteristics (in logarithmic scale) of WFEDG TFET with channel length of 60 nm for different values of gate oxide permittivities. SILVACO ATLAS simulated data are shown by symbols.

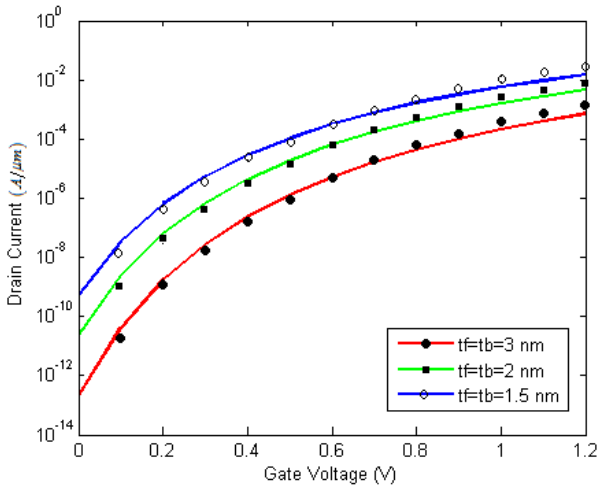

Fig. 6.3. 12. Transfer or I_D-V_{GS} characteristics (in logarithmic scale) of WFEDG TFET with channel length of 60 nm for different values of gate oxide thicknesses. SILVACO ATLAS simulated data are shown by symbols.

Figs. 6.3.11 and Fig. 6.3.12 show the I_D-V_{gs} i.e. characteristics in logarithmic scale. Introduction of a high-k material as gate oxide of the WFEDG TFET results in a higher I_{ON}/I_{OFF} ratio [6.14]. If the permittivity of gate oxide increases, the value of overall gate oxide capacitance also increases which in turn enhances the control of gate electrode over the channel, thereby boosting drain current considerably as can be inspected from Fig. 6.3.11. Increment in ON state current may also be achieved by increasing the effective gate capacitance by reducing the oxide thickness as illustrated in Fig. 6.3.12.

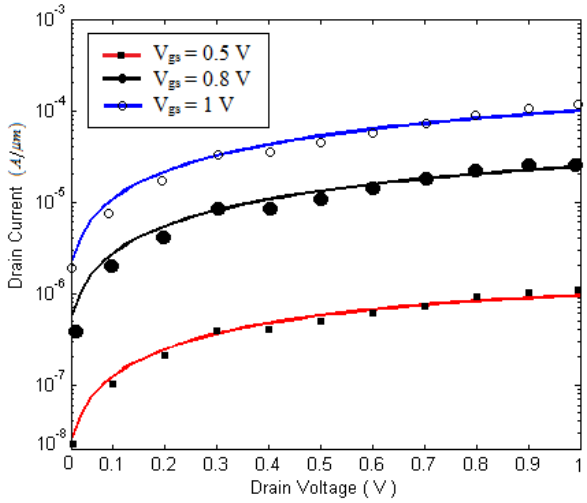

Fig. 6.3.13. Output or I_D-V_{DS} characteristics (in logarithmic scale) of WFEDG TFET with channel length of 60nm considering different values of Gate to Source voltages. SILVACO ATLAS simulated data are shown by symbols.

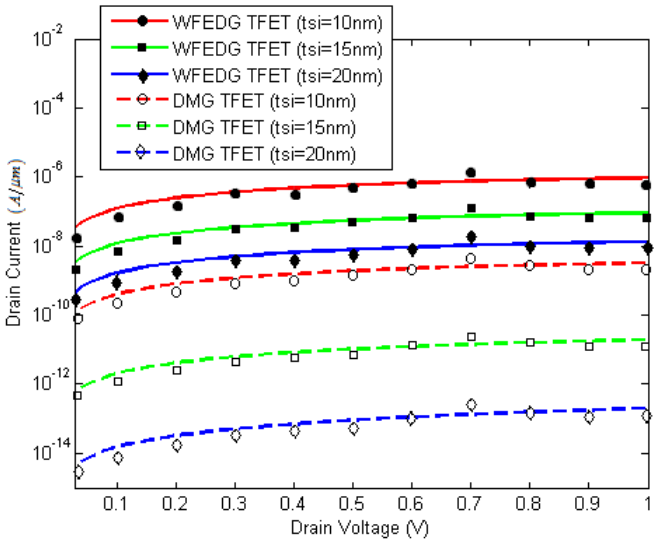

Fig. 6.3.14. Output or I_D-V_{DS} characteristics (in logarithmic scale) of WFEDG and DMG TFETs with channel length of 60nm considering different channel thicknesses. SILVACO ATLAS simulated data are shown by symbols.

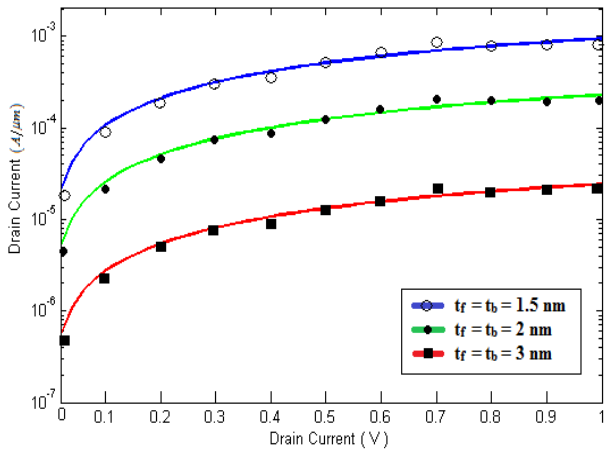

Fig. 6.3.15. Output or I_D-V_{DS} characteristics (in logarithmic scale) of WFEDG TFET with channel length of 60nm considering different gate oxide thicknesses. SILVACO ATLAS simulated data are shown by symbols.

Finally, the output or drain characteristics of the proposed WFEDG TFET has been investigated. The variations of drain current with drain-to-source voltages (in logarithmic scale) of the proposed WFEDG TFET are illustrated Figs. 6.3.13 to 6.3.15 considering different gate voltages and device geometries. The I_D-V_D characteristics for different gate bias depicted in Fig. 6.3.13 clearly indicates an effective increase in drain current with increasing gate voltages due to the lowering of barrier height at the source-channel junction. It can also be deduced from Figs. 6.3.14 and 6.3.15 that a reduction in the channel thickness and gate oxide thickness improves the body capacitive effect resulting in a momentous enhancement in the device current.

6.4. An analytical modeling based study of a Binary Metal Alloy Silicon on Nothing (BMASON) Tunnel FET to investigate the effects of Interface Trapped Charges

6.4.1. Overview

The unimpeded progress of the ever-evolving modern semiconductor industry from the domain of microelectronics to the present nanometer domain is propelled by the advent of Tunnelling Field Effect Transistors (TFETs) which by virtue of their inherent performance superiority promise to be a viable alternative to age old MOSFET technology. An in depth study of the surface potential profile and drain current characteristics of a proposed Work Function Engineered Double Gate (WFEDG) TFET presented in the preceding section of this chapter suggests that the incorporation of a binary metal alloy gate into a double gate TFET structure results in significant performance improvement over single metal double gate and dual material gate structures. The efficacy of this work function engineered gate concept in TFET applications lie in the fact that proper choice of the

binary metal alloy to be used as gate electrode makes it possible to suitably tune the potential barrier at the source-channel junction with an intention to amplify band-to-band tunneling of charge carriers from the filled valence band at source side into the empty conduction band of the channel. The continuous variation of properly chosen work function from the source to drain side lowers the source-to-channel potential barrier height so as to enhance the probability of carrier tunneling from the heavily doped source into the almost intrinsic channel. On the contrary, a comparatively lower value of metal work function near the drain end aids to maintain a higher drain-to-channel barrier potential height restricting OFF state ambipolar current. However, while considering operations of a device having gate length as low as 60 nm, the ultra low sub-100 nm channel length invites some serious short channel effects. As the channel length is getting more and more down scaled, the channel electric field increases abnormally and makes Hot Carrier Effect an inevitable issue. Under the influence of a very high channel electric field, the carriers tunneling from the source and entering into the channel can gain kinetic energy sufficient enough surmount the obstructive barrier at the oxide-semiconductor interface resulting in unwanted gate leakage current. The possible accumulation of trapped charges at the oxide-semiconductor interface near source-channel junction can tune the flat band voltage. This in turn modifies the surface potential, thereby affecting the shortest tunneling path which is manifested by the altered current characteristics [6.43]. This has been the prime motivation to study the device performance considering inevitable issues related to interface trapped oxide charges so as to gain a better insight into practical nature of device performance.

SON structure has already been discussed in sufficient details in the previous chapters. The SON architecture by dint of having air (having permittivity much less than oxide permittivity) in the BOX layer, minimizes the source/drain to channel and channel-to-substrate parasitic capacitances [6.44], which in turn results in higher circuit speed [6.45] achievable with SON devices as well as providing the highest isolation of active channel region. This makes the SON structure a better and faster device than conventional MOSFETs. Owing to the similarity in basic structure and fabrication process of TFETs with conventional MOSFETs, a BOX layer (with air as the dielectric) may also be introduced in a TFET realizing a SON TFET structure which is expected to show improved speed of operation and better performance than a conventional TFET.

In view of this, the present section aims to analytically explore the impact of interface trapped oxide charges (at the oxide-silicon interface near the source end) on the overall current behavior of a device by adopting a Binary Metal Alloy SON (BMASON) structure. The developed analytical model can thus be used to investigate the HCEs in TFETs with linearly graded binary metal alloy gate electrode and the possible design of charge-trapped memory devices based on this concept.

6.4.2. Analytical modeling

Device structure of the proposed BMASON Tunnel FET is illustrated in Fig. 6.4.1. As already mentioned, the gate electrode of the proposed TFET structure is composed of a Binary Metal Alloy (BMA) having linearly graded work functions of the constituent metal from source to drain side. To realize an n-channel TFET, the source of the BMASON TFET is heavily doped with Gr. III (Boron) dopants (N_s) and the drain is doped with Gr. V (Arsenic) dopants (N_d). The channel is kept lightly doped with Boron dopants (N_{ch}) with thickness T_{si}. A BOX layer having air as dielectric has been incorporated under the channel region to realize the advantages achievable using SON architecture [6.23]. The thicknesses of the channel, BOX and the gate oxide are T_{si}, T_{box} and T_{ox} respectively (as listed in Table 6.4.1). If the dimensions of a TFET are chosen to be in nanometer range, then its operation will inevitably be affected by Hot Carrier Effect induced localized oxide and trapped charges near the source end, thereby modifying the surface potential profile which in turn has an effect on the device current characteristics [6.43, 6.46]. Thus, for the proposed BMASON TFET structure with channel length as low as 60 nm, these unavoidable interface trapped charges have been incorporated at the interface of silicon channel and gate oxide near the source end up to a distance of L_{aff} from the source-channel interface towards the drain with a density of N_{trap} (10^{12}/ cm^2).

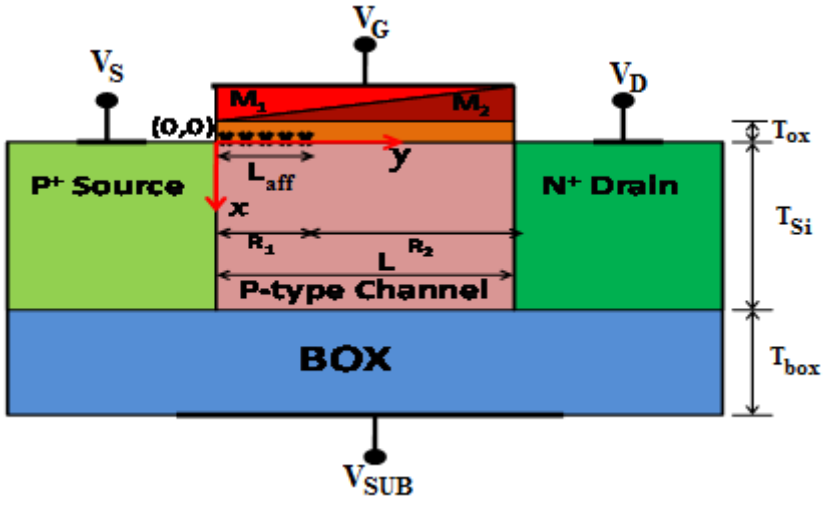

Fig. 6.4.1 Schematic cross sectional view of proposed BMASON TFET structure

The present work considers binary metal alloy gate electrode as well as accumulation of localized trapped charges near the tunneling junction of the BMASON TFET. Both of these considered factors have an effect on the flat band voltage which in turn affects the drain characteristics of the proposed structure. Inclusion of binary metal alloy as gate electrode results in an effective gate work function which can be expressed as [6.23]:

$$\phi_{m_{GATE}}(y) = (y/L)\phi_2 + (1 - y/L)\phi_1 \quad (6.4.1)$$

ϕ_1 and ϕ_2 are the work functions of two different metals considered such that $\phi_{m_{GATE}} = \phi_1$ at at y=0 (source end) and $\phi_{m_{GATE}} = \phi_2$ at y=L (drain end) [6.22-6.25].

6.4.2.1. Surface potential modeling

Solution of two dimensional Poisson's equation in the channel region is the first step of analytically modeling the surface potential. To start with, the two dimensional Poisson equation in the channel region of the proposed BMASON structure can be written as:

$$\frac{\partial^2\varphi(x,y)}{\partial x^2} + \frac{\partial^2\varphi(x,y)}{\partial y^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \quad \text{for } \left(0 \le y \le L, 0 \le x \le T_{Si}\right) \quad (6.4.2)$$

where, $\varphi(x,y)$ is the two dimensional potential of the channel region which is uniformly doped with doping concentration of N_{ch}. According to Young's Parabolic Potential Approximation [6.35], the potential is considered to be parabolic in nature to avoid the sharp change in the potential profile and can be given as:

$$\varphi(x,y) = \varphi_s(y) + d_1(y)x + d_2(y)x^2 \quad (6.4.3)$$

where $\varphi_s(y)$ represents the surface potential (at x=0), $d_1(y)$ and $d_2(y)$ are two 'y' dependent arbitrary constants.

Consideration of interface trapped oxide charges effectively divides the entire channel region (of length L) into two regions R_1 and R_2 where R_1 represents the trapped charges affected damaged region of length $L_1 = L_{aff}$ and R_2 represents the rest of the channel region of length $L_2 = L - L_{aff}$. The surface potentials in two different regions can be collectively written as:

$$\varphi_j(x,y) = \varphi_{sj}(y) + d_{j1}(y)x + d_{j2}(y)x^2 \quad \text{for } L_{j-1} \le y \le L_j,\ 0 \le x \le T_{si} \quad (6.4.4)$$

where $\varphi_{sj}(y)$ (j=1 and 2) is the surface potential for regions R_1 and R_2 respectively. Here L_0 is considered as the starting point of the channel i.e. L_0 is assumed to be zero; $d_{j1}(y)$ and $d_{j2}(y)$ are two channel position (along 'y' axis) dependent arbitrary constants.

As the entire channel region has been segregated into two distinct regions, the Poisson's equation needs to be solved separately for the two different regions of the channel. The boundary conditions required for this analytical solution can be stated as follows [6.47]:

1. Electric field at the front gate-oxide interface is continuous for the two channel regions (R_1 and R_2). Therefore,

$$\left.\frac{d\varphi_1(x,y)}{dx}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_{s1}(y)-V'_{GS1}}{T_{ox}} \qquad \text{in region } R_1 \tag{6.4.5}$$

$$\left.\frac{d\varphi_2(x,y)}{dx}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_{s2}(y)-V'_{GS2}}{T_{ox}} \qquad \text{in region } R_2 \tag{6.4.6}$$

where $V'_{GS1} = V_{GS} - V_{FB1}$ and $V'_{GS2} = V_{GS} - V_{FB2}$. V_{GS} is gate to source applied voltage, ε_{ox} is the gate oxide permittivity;

$$V_{FB1} = V_{FB0} - \frac{qN_{trap}}{C_{ox}} \text{ and } V_{FB2} = V_{FB0}$$

where $V_{FB0} = \phi_{m_{GATE}}(y) - \phi_{Si}$ is the flat band voltage for the undamaged channel region without any interface charge and $C_{ox} = \varepsilon_{ox} \big/ T_{ox}$ represents the capacitance of gate oxide measured in per unit area [6.43]. The effective work function of silicon channel is symbolized by ϕ_{Si}.

2. Electric field at the buried oxide and the channel interface is again continuous for the two channel regions (R_1 and R_2). Therefore,

$$\left.\frac{d\varphi_1(x,y)}{dx}\right|_{x=T_{si}} = \frac{\varepsilon_{box}}{\varepsilon_{Si}}\frac{V'_{SUB}-\varphi_{B1}(y)}{T_{box}} \qquad \text{in region } R_1 \tag{6.4.7}$$

$$\left.\frac{d\varphi_2(x,y)}{dx}\right|_{x=T_{si}} = \frac{\varepsilon_{box}}{\varepsilon_{Si}}\frac{V'_{SUB}-\varphi_{B2}(y)}{T_{box}} \qquad \text{in region } R_2 \tag{6.4.8}$$

where $V'_{SUB} = V_{SUB} - V_{FB,b}$; V_{SUB} is the back substrate bias and $V_{FB,b}$ is the flat band voltage of the back channel interface.

$$\varphi_B(x,y) = \varphi(x,y)\big|_{x=T_{si}}$$

$$\therefore \varphi_{Bj}(x,y) = \varphi_{sj}(y) + d_{j1}(y)T_{si} + d_{j2}(y)T_{si}^2$$

3. The front surface potential is continuous at the interface of two regions R_1 and R_2 having dissimilar flat band voltages due the presence of interface trapped oxide in the damaged region R_1:

$$\varphi_1(L1,0) = \varphi_2(L1,0)$$

4. Again, electric field at the interface of two regions R_1 and R_2 is also continuous:

$$\left.\frac{d\varphi_1(x,y)}{dy}\right|_{y=L1} = \left.\frac{d\varphi_2(x,y)}{dy}\right|_{y=L1}$$

Applying the boundary conditions 1 and 2 the constants $d_{11}, d_{12}, d_{21}, d_{22}$ are given as:

$$d_{11}(y) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_{s1}(y) - V_{GS1}^{'}}{T_{ox}}, \qquad d_{21}(y) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_{s2}(y) - V_{GS2}^{'}}{T_{ox}},$$

$$d_{12}(y) = \frac{V_{SUB}^{'} - \varphi_{s1}(y)[1 + C_{ox}/C_{Si} + C_{ox}/C_{box}] + V_{GS1}^{'}(C_{ox}/C_{Si} + C_{ox}/C_{box})}{T_{si}^2(1 + 2C_{Si}/C_{box})}$$

$$d_{22}(y) = \frac{V_{SUB}^{'} - \varphi_{s2}(y)[1 + C_{ox}/C_{Si} + C_{ox}/C_{box}] + V_{GS2}^{'}(C_{ox}/C_{i} + C_{ox}/C_{box})}{T_{si}^2(1 + 2C_{Si}/C_{box})}$$

Substituting the values of these constants in the Poisson's equation and using the parabolic potential approximation, the surface potential differential equations for two regions can be obtained as:

$$\frac{d^2\varphi_{sj}(y)}{dy^2} - \alpha\varphi_{sj}(y) + \beta V_{GSj}^{'} = \frac{qN_{ch}}{\varepsilon_{Si}} - \frac{2V_{SUB}^{'}}{T_{Si}^2\left(1 + 2C_{Si}/C_{box}\right)} \tag{6.4.9}$$

where,

$$\alpha = \frac{2(1 + C_{ox}/C_{Si} + C_{ox}/C_{box})}{T_{si}^2(1 + 2C_{Si}/C_{box})}; \qquad \beta = \frac{2(C_{ox}/C_{Si} + C_{ox}/C_{box})}{T_{si}^2(1 + 2C_{Si}/C_{box})}$$

where, $C_{Si} = \varepsilon_{Si}/T_{si}$, $C_{ox} = \varepsilon_{ox}/T_{ox}$ and $C_{box} = \varepsilon_{box}/T_{box}$. ($\varepsilon_{box} = \varepsilon_{air} = 1$ for the SON structure considered here) and ε_{Si} is relative permittivity of silicon.

Rigorous analytical solution of eq. 6.4.9 considering a number of parameter substitutions and subsequent simplifications results the following expression:

$$\frac{d^2\varphi_{sj}(y)}{dy^2} - \alpha\varphi_{sj}(y) - \beta\phi_{m_{GATE}}(y) = P_j \tag{6.4.10}$$

where, $P_1 = \frac{qN_{ch}}{\varepsilon_{Si}} - \frac{2V_{SUB}^{'}}{T_{Si}^2\left(1 + 2C_{Si}/C_{box}\right)} - \beta V_{GS} - \beta\phi_{Si} - \beta\frac{qN_{trap}}{C_{ox}}$ for the damaged R_1 region

$P_2 = \frac{qN_{ch}}{\varepsilon_{Si}} - \frac{2V_{SUB}^{'}}{T_{Si}^2\left(1 + 2C_{Si}/C_{box}\right)} - \beta V_{GS} - \beta\phi_{Si}$ for undamaged R_2 region

Eq. 6.4.10 thus obtained is a typical non-homogeneous differential equation which can be solved by adopting the approach of separation of variable to evaluate the consequential expression of front surface potential for both regions and are given as:

$$\varphi_{s_1}(y) = A\mathrm{e}^{\eta y} + B\mathrm{e}^{-\eta y} + \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right)y - \frac{\beta}{\alpha}\phi_1 - \frac{P_1}{\alpha} \qquad \text{for } 0 \le y \le L_1 \quad \text{in region } R_1 \tag{6.4.11}$$

$$\varphi_{s_2}(y) = C\mathrm{e}^{\eta(y-L_1)} + D\mathrm{e}^{-\eta(y-L_1)} + \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right)(y - L_1) - \frac{\beta}{\alpha}\phi_1 - \frac{P_2}{\alpha} \quad \text{for } L_1 \le y \le L \quad \text{in region } R_2 \tag{6.4.12}$$

Now, the coefficients A, B, C and D can be calculated considering the boundary conditions of potential at the source and the drain side as respectively [6.47],

$$\varphi_{s_1}(y=0) = V_{bis} + V_S = -\frac{kT}{q}\ln\left(\frac{N_s}{n_i}\right)$$

$$\varphi_{s_2}(y=L) = V_{bid} + V_{DS} = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) + V_{DS}$$

and are given as:

$$A = \left\{\left(V_{bid} + V_{DS} - \vartheta_2\right) - \left(V_{bis} - \vartheta_1\right)e^{-\eta L} - \left(\rho_1 - \rho_2\right)\cosh(\eta L_2)\right\}\left(\frac{e^{-\eta L}}{1 - e^{-2\eta L}}\right);\quad B = \frac{\left(V_{bis} - \vartheta_1\right) - \left(V_{bid} + V_{DS} - \vartheta_2\right)e^{-mL} + \left(\rho_1 - \rho_2\right)\cosh(\eta L_2)e^{-\eta L}}{\left(1 - e^{-2\eta L}\right)}$$

$$C = Ae^{\eta L_1} + \left(\frac{\rho_1 - \rho_2}{2}\right) \quad \text{and} \quad D = Be^{-\eta L_1} + \left(\frac{\rho_1 - \rho_2}{2}\right)$$

where $\rho_1 = \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right)\left(\frac{L_1}{L}\right) - \frac{\beta}{\alpha}\phi_1 - \frac{P_1}{\alpha}$; $\rho_2 = -\frac{\beta}{\alpha}\phi_1 - \frac{P_2}{\alpha}$; $\vartheta_1 = -\frac{\beta}{\alpha}\phi_1 - \frac{P_1}{\alpha}$; $\vartheta_2 = \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right)\left(\frac{L_2}{L}\right) - \frac{\beta}{\alpha}\phi_1 - \frac{P_2}{\alpha}$

where the doping concentration of the source and the drain are N_s and N_d respectively. The drain bias is V_{DS} with respect to source terminal i.e. $V_S = 0V$.

6.4.2.2. Electric field modeling

(i) The expression for lateral electric field can be formulated by simply differentiating the expression for front surface potential (vide eqs. 6.4.11 and 6.4.12) with respect to lateral coordinate ('y' axis) along the channel and written as:

$$E_{1y}(y) = -\left.\frac{d\varphi_1(x,y)}{dy}\right|_{x=0} = -\eta A\mathrm{e}^{\eta y} + \eta B\mathrm{e}^{-\eta y} - \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right) \qquad \text{for } 0 \le y \le L_1 \quad \text{in region } R_1 \tag{6.4.13}$$

$$E_{2y}(y) = -\frac{d\varphi_2(x,y)}{dy}\bigg|_{x=0} = -\eta C e^{\eta(y-L_1)} + \eta D e^{-\eta(y-L_1)} - \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right) \qquad \text{for } L_1 \leq y \leq L \text{ in region } R_2 \qquad (6.4.14)$$

(ii) The expression for vertical electric field can be formulated by simply differentiating the expression for front surface potential (vide eqs. 6.4.11 and 6.4.12) with respect to vertical coordinate ('x' axis) and written as:

$$E_{1x}(y) = -\frac{d\varphi_1(x,y)}{dx} = -d_{11}(y) - 2xd_{12}(y) \qquad \text{for } 0 \leq y \leq L_1 \qquad (6.4.15)$$

$$E_{2x}(y) = -\frac{d\varphi_2(x,y)}{dx} = -d_{21}(y) - 2xd_{22}(y) \qquad \text{for } L_1 \leq y \leq L \qquad (6.4.16)$$

The overall electric field is a combination of both lateral and transverse electric fields and can be obtained by: $E_{res} = \sqrt{E_x^{\,2} + E_y^{\,2}}$

6.4.2.3. Drain current modeling

As already discussed, the operating principle of TFETs is based on the band-to-band quantum tunneling of carriers through a very thin potential barrier at the source-channel junction. The drain current formulation of TFET has already been covered in the previous section in sufficient details. The same steps are again being repeated in this sub section for the continuity and brevity of understanding. As we know, the classical mathematical solution of this quantum tunneling phenomenon is based on the well defined Kane's model [6.37].

Drain current in a TFET is basically the resultant tunneling current which can be expressed as follows by integrating the tunneling carrier generation rate over the entire volume:

$$I_D = \iiint G(E)dv \qquad (6.4.17)$$

where, G(E) is the energy dependent generation rate of the carriers given by Kane's model dv represents an elemental volume in the tunneling window. This three dimensional scenario can be reduced to a simpler two dimensional analysis by considering the drain current (I_D) per unit width (in A/um). Therefore,

$$I_D = \iint G(E)dxdy \qquad (6.4.18)$$

The expression for carrier generation rate (G (E)) can be written is terms of basic Kane's parameters A_k, B_k and D_k (listed in Table 6.4.1) [6.37]as follows which incorporates the dependence of G(E) on effective mass and carrier lifetime of the holes and electrons.

$$G(E) = A_k E^{D_k} \exp\left(-\frac{B_k}{E}\right) \tag{6.4.19}$$

Fig. 6.4.2 clearly delineates the effective tunneling window existing at the source-channel junction through which charge carriers tunnel from the filled valence band states at the source side to the empty conduction band states in the channel. The channel for the proposed BMASON TFET is considered to be along the y-direction. The allowed tunneling window is basically dependent on minimum tunneling length (y_1) at which tunneling will start and the maximum tunneling length (y_2) at which the tunneling stops.

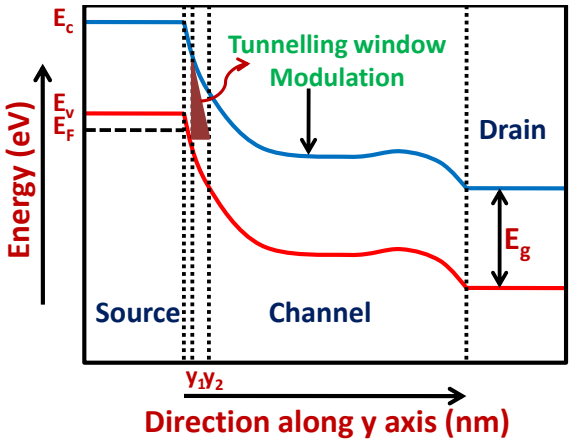

Fig. 6.4.2 Band diagram illustrating tunneling path between the valence band of the source and the conduction band of the channel region.

The total electric field in the channel region is a combination of average (E_{avg}) and local (E_{res}) electric field respectively [6.48]. The average electric field (E_{avg}) is again a direct function of the effective tunneling path ($l_{path} = y_2 - y_1$) i.e. $E_{avg} = \left(E_g / q l_{path}\right)$ and is solely responsible for the tunneling at the source-channel junction. Considering dominant tunneling path [6.21] along the lateral direction of the channel, the drain current expression has been formulated by integrating equation 6.4.18 over the entire channel thickness resulting in the equation below:

$$I_D = q \int_{x_1}^{x_2} \int_{y_1}^{y_2} A_k E E_{avg}^{D_k - 1} \exp\left(-B_k / E_{avg}\right) dxdy \tag{6.4.20}$$

It is evident from Fig. 6.4.2 that the source valence band gets aligned with channel conduction band

at y=y_1 marking the onset of carrier tunneling [6.4]. This point i.e. y_1 can be obtained when the front surface potential will be equal to $(E_g + \Delta E)/q$ i.e. $\varphi_{s1}(y)|_{y=y_1} = \frac{E_g + \Delta E}{q}$, which can be written as:

$$Ae^{\eta y_1} + Be^{-\eta y_1} + \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right)y_1 - \frac{\beta}{\alpha}\phi_1 - \frac{P_1}{\alpha} = \frac{E_g + \Delta E}{q} \tag{6.4.21}$$

Where, E_g is the difference in energy between the conduction and valence bands of the silicon channel (also known as bandgap) and ΔE is the difference between the energy levels of valence band and Fermi level of p-type source.

Eq. (6.4.21) is now solved neglecting the higher order terms to find close form equation of minimum tunneling width given as:

$$y_1 = \frac{E_g + \Delta E + q\frac{\beta}{\alpha}\phi_1 + q\frac{P_1}{\alpha} - qA - qB}{q\eta A - q\eta B + q\frac{\beta}{\alpha}\left(\frac{(\phi_1 - \phi_2)}{L}\right)} \tag{6.4.22}$$

Similar argument suggests that the maximum tunneling width will be at a point y=y_2 where the alignment of the filled valence and empty conduction band is approximately insignificant restricting further tunneling of current. This occurs when the front surface potential becomes equal to $(E_g + \Delta\varphi)/q$ i.e., $\varphi_{s1}(y)|_{y=y_2} = \frac{E_g + \Delta\varphi}{q}$, which can be written as:

$$Ae^{\eta y_2} + Be^{-\eta y_2} + \frac{\beta}{\alpha}\left(\frac{\phi_1 - \phi_2}{L}\right)y_2 - \frac{\beta}{\alpha}\phi_1 - \frac{P_1}{\alpha} = \frac{E_g + \Delta\varphi}{q} \tag{6.4.23}$$

$\Delta\varphi$ is the difference between the valence and conduction bands of the source and the channel which is basically the built-in potential of the junction. Neglecting higher order terms in equation 6.4.23 just as in the previous case, the compact formulation of y_2 can be written as:

$$y_2 = \frac{E_g + \Delta\varphi + q\frac{\beta}{\alpha}\phi_1 + q\frac{P_1}{\alpha} - qA - qB}{q\eta A - q\eta B + q\frac{\beta}{\alpha}\left(\frac{(\phi_1 - \phi_2)}{L}\right)} \tag{6.4.24}$$

As the source is highly doped, the entire tunneling window exists in the channel region only. Finally, an expression for total drain current can now be formulated by performing double integration on the carrier generation rate laterally over the entire tunnel window extending from x_1 to x_2 and vertically over the entire channel thickness and can be written as:

$$I_D = q\int_{y=y_1}^{y=y_2}\int_{x=0}^{x=T_{si}} A_k E \frac{E_g^{D_k-1}}{q^{D_k-1}y^{D_k-1}} \exp\left(-qyB_k/E_g\right) dxdy \tag{6.4.25}$$

6.4.3. Results and discussions

The following results and discussion sub section will focus on the evaluative performance of the proposed BMASON TFET incorporating interface trap charges which becomes an unavoidable issue while considering ultra low dimensional devices. The results shown here are obtained from complex analytical modeling presented and are verified using commercially available *2D TCAD* to validate the accuracy of the proposed model. The simulation realizes tunneling using non local band-to-band model along with the conventional drift-diffusion model. The recombination processes going on are realized by including SRH recombination with Auger effects [6.49] while the localized charges near the interface are invoked using Trap models. Unless otherwise mentioned, the simulation and modeling consider the parameter values as listed in Table 6.4.1.

Table 6.4.1: Parameter Table

Parameters	Value
Substrate doping concentration (p type)	10^{23} m^{-3}
Source doping concentration (p+)	6 x $10^{26}m^{-3}$
Drain doping concentration (n+)	10^{24} m^{-3}
Channel Length	60 nm
Front Oxide thickness (T_{ox})	3 nm
BOX layer thickness (T_{box})	40 nm
Film thickness (T_{Si})	10 nm
V_{DS}	1V
V_{GS}	0.2 V
Kane's Parameter	
A_k	3.5 x 10^{21} $m^{-1/2}V^{-5/2}s^{-1}$
B_k	22.5 x 10^6 V/cm
D_k	2.5 for indirect tunneling
	2 for direct tunneling

The results showing surface potential and electric fields are obtained analytically by solving conventional 2 D Poisson's equation with proper consideration of relevant boundary conditions. Similarly, I-V characteristics have been obtained by exhaustive double integration of the tunneling carrier generation rate based on Kane's Model.

A surface potential based comparative study of the proposed BMASON TFET along with its conventional Single Gate equivalent has been shown in Fig. 6.4.3. The unique feature of the proposed BMASON TFET structure which distinguishes it from a normal single gate SON TFET is the graded Binary Metal Alloy gate electrode. The mole fractions of the constituent metals of this alloy system are continuously graded spatially from the source to the drain end resulting in different values of effective work function at different channel positions.

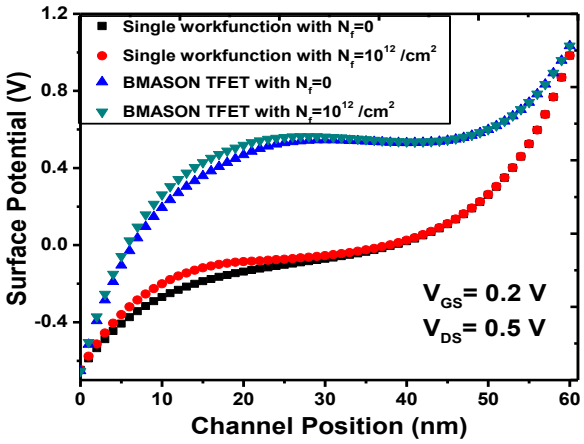

Fig. 6.4.3 Comparative study of surface electrostatic potential profile of conventional and BMASON TFETs considering and without considering interface trapped charges

This continuous spatial variation of gate work function increases the surface potential resulting in an increased band bending and an effective boost in the electric field near the source-channel tunneling junction. It can also be noted from Fig 6.4.3 that the localized interface trapped charges near the source-channel junction is enhancing the band bending, which in turn enhances carrier tunneling making it more advantageous over the case when the localized charges are absent.

Next figure (Fig.6.4.4) illustrates the nature of surface potential profile along channel position of BMASON TFET for different gate-to-source biases (V_{GS}). It can be observed that the the surface potential profile shifts upwards with an increase in the gate bias, thereby enhancing band bending at the source-channel junction. Depending on the presence and absence of localized trapped charges, the entire channel region can be divided into two distinct regions as depicted in Fig. 6.4.4. Region R1 near the source end represents the region affected by localized charges and plays a crucial role as the effective tunneling occurs at the source-channel junction. Region R2 represents the fresh region almost unaffected by trap charges.

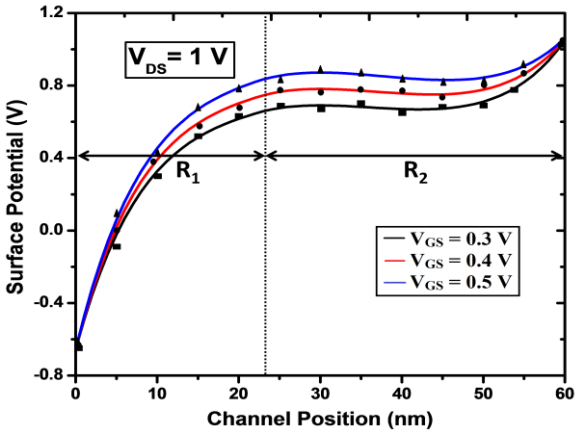

Fig.6.4.4 Variation of surface potential profile along channel position of a BMASON TFET considering different gate biases. TCAD simulation data are represented by symbols.

In addition to applied gate bias, a certain value of drain bias is indeed required to drive the device into ON state [6.47]. Once the TFET is turned ON, the drain bias will not have any significant control on the source-channel junction and thus, will not affect further carrier tunneling. This is illustrated in Fig. 6.4.5 pictorially showing slight change in potential profile at the drain end and almost no change near source end for variations in applied drain bias.

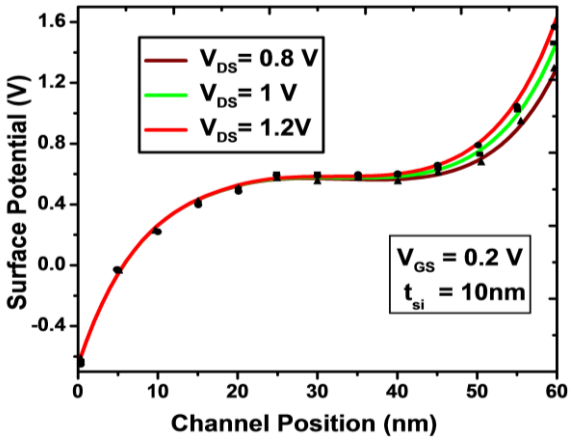

Fig. 6.4.5 Variation of surface potential profile along channel position of a BMASON TFET considering different drain biases. TCAD simulation data are represented by symbols.

Fig. 6.4.6 depicts the nature of variation of lateral electric field in the channel region of a BMASON TFET. It can be very well understood from the said figure that while the TFET is operating in ON state, the presence of trapped charges near the source-channel junction of the BMASON TFET results in an enhanced band bending in sharp contrast with an equivalent

BMASON TFET without any trapped charges. This significant increase in band bending leads to a considerable increase in carrier tunneling.

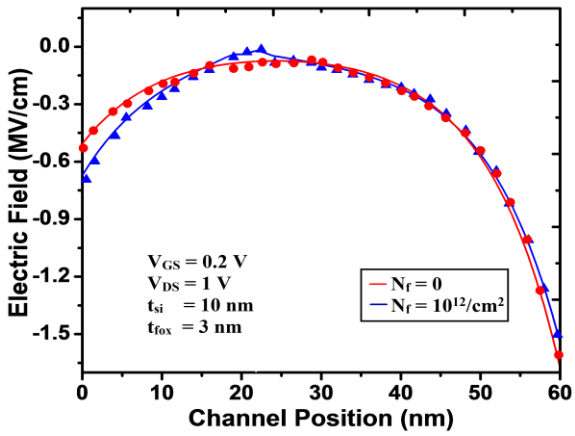

Fig.6.4.6 Variation of lateral electric field (y-component) along channel position of a BMASON TFET considering and without considering interface trapped charges. TCAD simulation data are represented by symbols.

Analysis of surface potential and electric field profiles of the proposed BMASON TFET bear eloquent testimony to the fact that the presence of the interface trapped charges near the source channel junctions results in an enhanced band bending and consequently a boost in the carrier tunneling probability across the source-channel potential barrier, thereby effectively improving drain current performance of the proposed BMASON TFET structure as elucidated in Fig. 6.4.7. The physics behind the current conduction mechanism in TFETs is governed by the phenomenon of band-to-band tunneling of the carriers. Therefore, incorporation of positive trapped charges near the source-channel interface provides an additional aid in the tunneling of negatively charged electrons by attracting the electrons from the filled states in the valence band of the heavily doped source, which in turn results in a momentous enhancement in the tunneling generation rate responsible for a significant boost in drain current. Moreover, if the silicon channel thickness is reduced, the drain current increases as evident from Fig. 6.4.8 describing the drain current versus gate-to-source voltage characteristics of the proposed BMASON TFET incorporating the effects of interface trapped charges. This is primarily attributed by the improved capacitive action of the device body [6.48, 6.50] with a decrease in channel thickness. Akin to this, it can be similarly argued that a reduction in gate oxide thickness provides better capacitive effect on the channel which in turn boosts up device ON current [6.50] as depicted in Fig. 6.4.9.

It must also be noted that a reduction in potential coupling ratio (PCR) can be obtained for a SON structure due to the lower dielectric constant of the underlying BOX (air in case of SON) layer of a SON structure in contrast to the conventional oxide permittivity of a SOI structure. This unique feature attributes to the inherent superiority of SON in subduing harmful SCEs compared to SOI. This has been substantiated by the improved device current performance of the proposed BMASON TFET structure over its BMASOI TFET equivalent as depicted in the inset of Fig. 6.4.9.

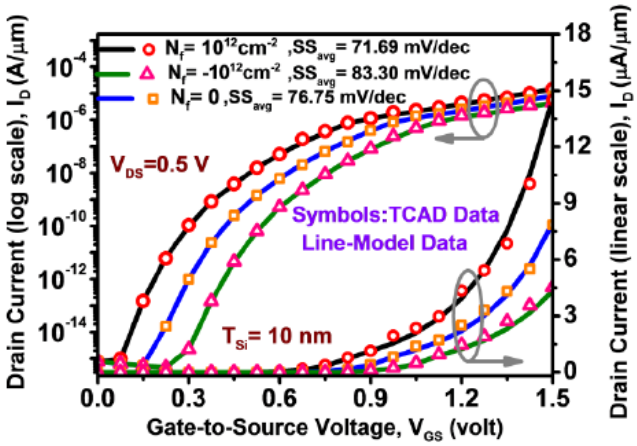

Fig. 6.4.7 Transfer or I_D-V_{GS} characteristics (in both linear and logarithmic scales) of BMASON TFET considering and without considering interface trapped charges at fixed drain bias. TCAD simulation data are represented by symbols.

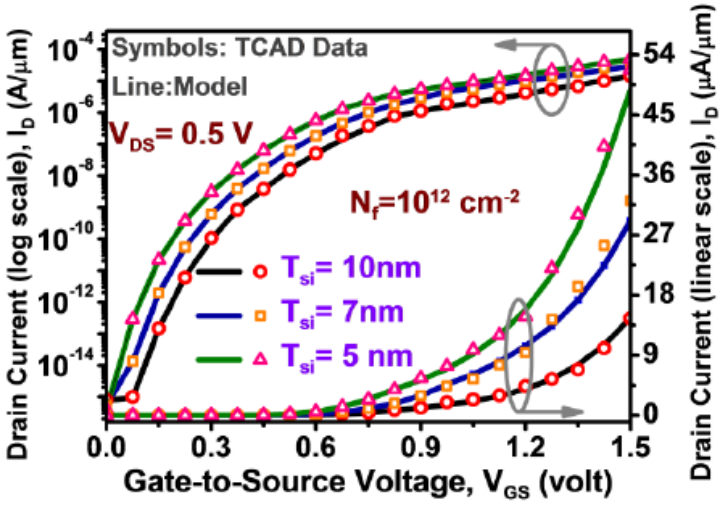

Fig. 6.4.8 Transfer or I_D-V_{GS} characteristics (in both linear and logarithmic scales) of BMASON TFET considering interface trapped charges at fixed drain bias for different channel thicknesses. TCAD simulation data are represented by symbols

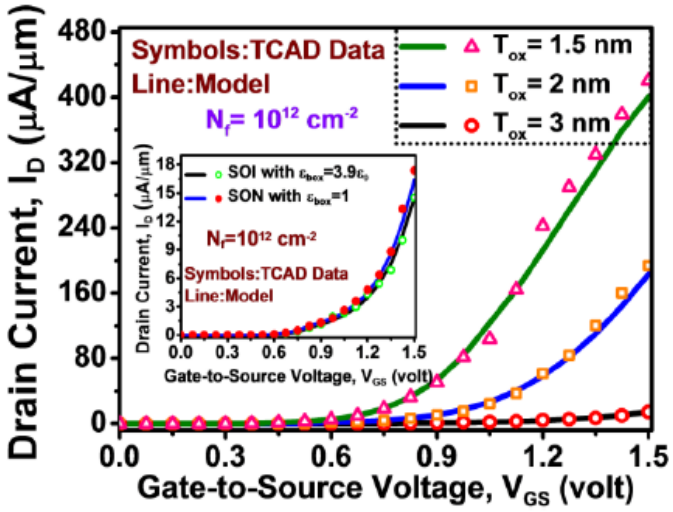

Fig. 6.4.9 Transfer or I_D-V_{GS} characteristics (in linear scales) of BMASON TFET considering interface trapped charges at fixed drain bias for different gate oxide thicknesses. TCAD simulation data are represented by symbols

The output characteristic (in logarithmic scale) of the BMASON TFET under study has now been shown in Fig. 6.4.10 for different values of applied gate voltages. It can be well understood that for a fixed value of gate voltage, the device gets turned ON at a certain drain bias and the current gradually increases on increasing the drain voltage till saturation is reached. It is also evident from the said figure that an increase in the gate bias effectively increases the drain current for obvious reasons of enhanced band bending.

On careful study of the band diagram illustrated in Fig. 6.4.2, it can be inferred that higher tunneling current is achieved from a shorter tunneling path. This understanding has been substantiated in Fig. 6.4.11 which shows the nature of tunneling path variation on varying gate bias applied to the proposed BMASON TFET with interface trapped charges. This study clearly establishes the major role played by the interface trapped charges in significantly enhancing the device current.

In addition to this, the variation of average subthreshold slope of the default structure under consideration (i.e. BMASON TFET with interface trapped charges) for different values of gate lengths has been illustrated in Fig. 6.4.12. The expression of the average sub-threshold slope can be written as :

$$SS_{avg} = \frac{V_T - V_{off}}{\log[I_D(V_T) - I_D(V_{off})]} \tag{6.4.26}$$

Where, V_T represents that particular value of gate bias at which $I_D=10^{-8}$ A/um and V_{off} represents that particular value of gate bias at which I_D starts to flow.

The values of average sub-threshold slope for the proposed BMASON TFET (both with and without considering interface trapped charges) must be noted from Fig. 6.4.7. It becomes evident that the SS_{avg} value of the proposed BMASON TFET structure having positive trapped charge density of $N_f=10^{12}$ cm^{-2} is significantly lower than the SS_{avg} value of the equivalent structure without trapped charges, thereby testifying efficacy of our proposed device structure for low power applications in future.

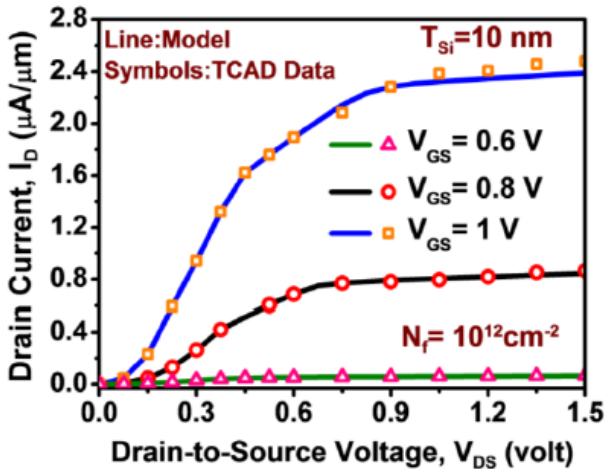

Fig. 6.4.10 Output or I_D-V_{DS} characteristics (in logarithmic scale) of BMASON TFET for different values of gate bias. TCAD simulation data are represented by symbols.

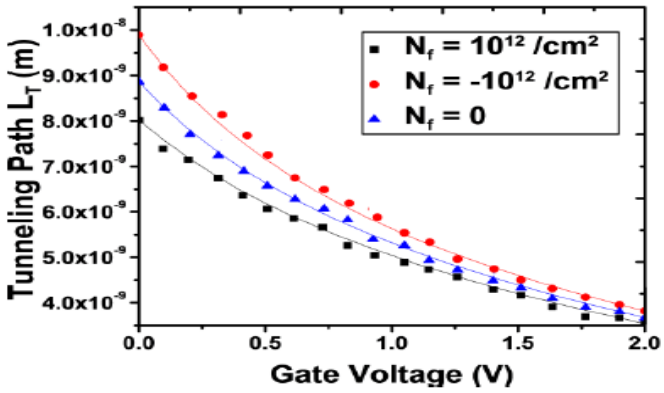

Fig. 6.4.11 Variation of tunneling path with gae-to-source voltage of the proposed BMASON TFET structure considering and without considering interface trapped charges of both polarities

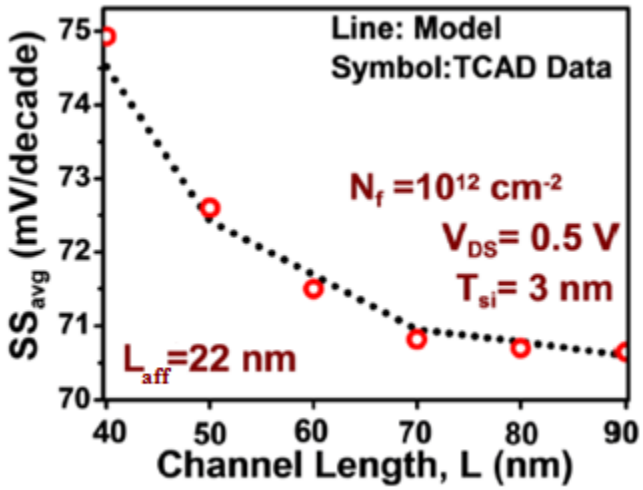

Fig. 6.4.12 Variation of average subthreshold slope with channel length of the proposed BMASON TFET structure. TCAD simulation data are represented by symbols.

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Relevant Publications:

- **Saheli Sarkhel,** Navjeet Bagga and Subir Kumar Sarkar, " A compact analytical model of binary metal alloy silicon-on-nothing (BMASON) tunnel FET with interface trapped charges" in **Journal of Computational Electronics**, Springer, September 2017, Volume 16, Issue 3, pp 704–713.
- **Saheli Sarkhel,** Navjeet Bagga and Subir Kumar Sarkar. "Compact 2D Modeling and Drain Current Performance Analysis of a Work Function Engineered Double Gate Tunnel Field Effect Transistor." In **Journal of Computational Electronics, Springer,** Vol. 15, Issue 1, pp. 104-114, March 2016.
- **Saheli Sarkhel**, Priyanka Saha and Subir Kumar Sarkar, "Parasitic Fringe Capacitance Modeling of Work Function Engineered Double Gate TFET", in the 2nd **IEEE International Conference on** "**Devices for Integrated Circuits (DevIC 2017)**", held at Kalyani Government Engineering College from March 23-24, 2017.
- Navjeet Bagga, **Saheli Sarkhel** and Subir Kumar Sarkar. "Analytical Model for ID-VD characteristics of a Triple Metal Double Gate TFET." In **IEEE International Conference on Computing, Communication and Automation (ICCCA 2016)**, 29th-30th April 2016, Noida.
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Chapter 7

Concluding remarks on the thesis and scope for future work

CHAPTER VII

7.1. Concluding remarks

7.2. Future Scope

7.1. Concluding remarks

Any research work is incomplete without some conclusive statement. The primary motive of this dissertation has been to investigate the unique features associated with the operation of different innovative nano dimensional non-conventional field effect transistors incorporating the novel concept of 'hetero material gate electrode'. The results of the proposed structures presented in the previous chapters are based on exhaustive analytical modeling and are compared with simulation results from available device simulators in order to validate the mathematical accuracy of the proposed models. The overall observations of this thesis work are summarized in this chapter. Some future scopes of this doctoral thesis are also pointed out briefly.

The present boon in the growth of VLSI/ULSI industry is attributed to a large extent by the ever increasing integration density of elementary transistors with reduced device dimensions in accordance to Moore's law. This fanatic pace of miniaturization predicted by Moore results in ultra small device dimensions inviting some inevitable short channel effects like Threshold Voltage Roll Off (TVRO), Drain Induced Barrier Lowering (DIBL), degraded subthreshold-slope, Hot Carrier Effect (HCE) due to high electric field induced impact ionization, enhanced off-state junction leakage current etc. which cumulatively play a major role in severely deteriorating the performance of short channel bulk MOSFETs. These detrimental performance deterrents can be subjugated to a certain extent by adopting several structural and material improvisations (buried oxide engineering, strain engineering, gate engineering or multi-gate structures, gate material engineering etc.) on conventional bulk MOSFETs resulting in non-conventional MOSFETs. The primary focus of this thesis has been on exploring such non-conventional device structures with a view to mitigate the issues related to short channel effects and realize improved device performance.

One such possible alternative to conventional MOS technology is Silicon-on-Insulator (SOI)/ Silicon-on-Nothing (SON) technology. Gate material engineering is yet another fascinating concept where the vertical electric field in the channel at any point can be modified by using two or more

materials with different work functions placed side by side forming a single gate electrode, which in turn adjusts the overall channel electric field resulting in an improved device performance. Chapter 3 presents a Poisson's equation based two-dimensional analytical model of a proposed Dual Material gate strained Fully Depleted SON MOSFET device structure which unambiguously demonstrates that the incorporation of dual material gate concept in strained Silicon-on-Nothing MOSFET introduces a sudden step like feature in the channel surface potential profile (vide Figs. 3.6 and 3.7), thereby subduing several short channel effects. The results obtained have been shown to study a performance comparison of both DMG SOI and SON devices in terms of electric field (vide Fig. 3.8), threshold voltage roll-off (vide Fig. 3.9), mobility enhancement (vide Figs. 3.2 – 3.5) and drain current behavior (vide Figs. 3.10, 3.11 and 3.12) which reveals the improvement in SON structure over its SOI counterpart in effectively subduing the SCEs and having an enhanced current driving capability. Moreover, the incorporation of strain in our present model significantly increases the speed and current driving capability due to a considerable increase in carrier mobility and velocity overshoot effects in strained DMG SOI and DMG SON structures.

Apart from the SOI/SON technologies, gate engineering and gate material engineering are two emerging concepts in order to realize some non-conventional MOSFET devices to overcome device performance degradation induced by inevitable short channel effects. Gate engineering involves more than one gate electrode to control the charge conduction through the channel which effectively increases the current drivability of the devices having multiple gate electrodes.

The concept of gate material engineering can be exploited to an extreme level by considering a binary metal alloy (A_{α} $B_{1-\alpha}$) gate electrode where the individual concentrations of constituent metals are varied continuously from being 100% A at source side to 100 % B at drain side. The vertical field and consequently the overall field in this system will be adjusted by the continuous variation of work function to reduce surface potential asymmetry in nano scale devices. This, in turn, controls the DIBL significantly and improves the device performance by removing the uneven transition of surface potential and surface electric field. This unique concept of using a binary metal alloy as gate electrode can be abbreviated as '***Linearly Graded Gate (LGG)***' or '***Work Function Engineered Gate (WFEG)***' or '***Binary Metal Alloy Gate (BMA gate)***' and can be incorporated into various non-conventional device structures in order to improve their performance further.

Chapter 4 aims to explore the effectiveness of incorporating the novel concept of linearly varying the mole fraction of a binary metal alloy used as gate electrode brainstormed by Sarkar et. al. in multigate MOSFET devices with the primary objective to establish the effectiveness of the 'work function engineered gate' concept in subduing the detrimental SCEs to restrict performance degradation in short channel devices. This purpose has been exploited in different sub sections by incorporating the work function engineered gate concept into different multigate device structures

such as Double Gate (DG) MOSFET, Cylindrical Gate (CG) MOSFET and Quadruple Gate (QG) MOSFET as vividly discussed throughout the chapter.

Section 4.2 of Chapter 4 presents a detailed overview on the various aspects of asymmetricity of a proposed Linearly Graded Asymmetric Double Gate (LGADG) MOS structure to explore its overall performance comparison with its normal DG counterpart based on analytical modeling and MEDICI simulation results in terms of channel potential (vide Figs. 4.2.2, 4.2.3, 4.2.4, 4.2.5 and 4.2.6), channel electric field (vide Fig. 4.2.7), Threshold Voltage Roll-off (vide Figs. 4.2.8 and 4.2.9) and Drain Induced Barrier Lowering (DIBL) (vide Fig. 4.2.10). It can be inferred from careful investigation of the aforementioned figures that device performance gets significantly improved by cleverly incorporating the concept of spatial composition graded binary metal alloy as gate electrode. The detailed study throughout section 4.2 has explored asymmetricity of different device parameters like gate oxide thickness, gate metal work function, gate oxide permittivity and even gate biasing conditions in the front and back gates of the Double Gate MOSFET with a motto to substantiate the remarkable performance superiority of an asymmetric structure in sharp contrast to its symmetric counterpart.

Section 4.3 of Chapter 4 investigates a detailed performance analysis of a proposed Work Function Engineered Gate Cylindrical Gate (WFEG CG) MOS structure to explore its overall performance comparison with its normal CG counterpart based on analytical modeling and MEDICI simulation results in terms of surface potential (vide Fig. 4.3.2), reduced drain end peak electric field (vide Fig. 4.3.3), reduced Threshold Voltage roll off (vide Figs. 4.3.4 and 4.3.5), reduced Drain Induced Barrier Lowering (DIBL) (vide Fig. 4.3.6), enhanced current driving capability (vide Fig. 4.3.7), reduced drain conductance (vide Fig. 4.3.8), enhanced trans-conductance (vide Fig. 4.3.9) and higher voltage gain (vide Fig. 4.3.10). The incorporation of a linearly graded binary metal alloy gate electrode into a cylindrical gate MOSFET improves short channel behavior significantly thereby improving the device scalability to a further extent.

Section 4.4 of Chapter 4 explores a quasi 3D scaling equation based theoretical calculation for the threshold voltage of a Work Function Engineered Gate Quadruple Gate (WFEG QG) MOSFET incorporating quantum mechanical (QM) effects. The obtained analytical results are validated using MEDICI simulated data. The presented comparative study of the proposed WFEG QG MOSFET with respect to a simple QG MOSFET in terms of shift of surface potential minima (Fig. 4.4.2), channel electric field (Fig. 4.4.3), Threshold Voltage Roll-Off (Figs. 4.4.4, 4.4.5 and 4.4.6) and DIBL (Figs. 4.4.7 and 4.4.8) has been illustrated which clearly establishes the superiority of the proposed

WFEG QG MOSFET over its simple QG counterpart in suppressing the harmful SCEs making it a suitable alternative device to continue with the trend of device dimension miniaturization in future.

So far, the alternative non-conventional device structures investigated in this thesis work are primarily junction based devices which face major challenge of formation of ultra-sharp source/drain junctions when the overall device dimension comes down to sub nanometer regime. This bottleneck of junction based devices discussed so far has shifted the interest of research community to yet another novel concept of Junctionless (JL) transistors, which, by the virtue of their junctionless architecture, gets rid of the problems associated with impurity diffusion and ultra sharp junction formation. Chapter 5 of this thesis incorporates the novel concept of work function engineered gate electrode in different junctionless FETs, so as to substantiate the effectiveness of adopting a binary metal gate electrode rather than using a single metal gate electrode.

Section 5.3 of Chapter 5 demonstrates a detailed comparative performance analysis of a proposed Junctionless Work Function Engineered Gate Double Gate (JL WFEG DG MOSFET) with its simple Junctionless Double Gate (JL DG) equivalent based on the in depth analytical modeling. The results obtained are depicted in various figures to establish the superior performance exhibited by the JL WFEG DG MOSFET compared to its normal JL DG counterpart in terms of position of channel central potential minima (vide Figs. 5.3.3 and 5.3.4), drain side peak central electric field (vide Fig. 5.3.5), reduced threshold voltage roll off (vide Fig. 5.3.6) and DIBL (vide Fig. 5.3.7) in order to establish the effectiveness of incorporating the novel concept of linearly graded binary alloy metal gate into a junctionless double gate MOSFET in mitigating unwanted SCEs. The analytical results bear close resemblance with the MEDICI simulated data, thereby validating the accuracy of presented analytical model.

Section 5.4 of Chapter 5 presents a similar study of incorporating the concept of using linearly graded binary metal alloy gate electrode in a cylindrical Junctionless MOSFET structure to reap the dual benefits of work function engineered gate electrode along with the enhanced gate control by a cylindrical (or gate all around) JL MOSFET structure. This section contains a detailed theoretical calculation based on two dimensional Poisson equation in cylindrical coordinates and presents a comparative performance analysis of a Junctionless Workfunction Engineered Gate Cylindrical Gate (JL WFEG CG) MOSFET with respect to a simple Junctionless Cylindrical Gate (JL CG) structure without binary metal alloy gate in terms of position of potential minima (vide Figs. 5.4.2 and 5.4.3), improved threshold voltage roll-off (vide Fig. 5.4.4), better subthreshold behavior (vide Fig. 5.4.5), reduced DIBL (vide Fig. 5.4.6), superior current drivability(vide Figs. 5.4.7, 5.4.8 and 5.4.9) and higher voltage gain (vide Fig. 5.4.10) which bear eloquent testimony to the fact that incorporation of

linearly graded binary alloy metal gate in a JL CG MOSFET improves its performance over its normal JL CG equivalent by subduing various unwanted SCEs. The results obtained analytically bear sufficient resemblance with MEDICI simulated data, thereby authenticating the precision of the presented analytical model.

The progress of this thesis from Chapter 3 to Chapter 5 has been a journey to find a suitable device as a possible alternative to conventional MOSFETs so as to continue with the unhindered pace of device dimension miniaturization as predicted by ITRS. Till now, the research initiatives discussed in this dissertation from chapters 3 to 5 incorporates the concept of linearly graded binary metal alloy gate electrode in various MOSFET structures (considering gate engineering, gate material engineering and even accumulation mode junctionless operation) in order to subdue the harmful SCEs and achieve improved short channel performance. However, the major drawback of conventional MOSFET is the non-scalability of sub-threshold swing (limited to 60mV/dec). This poses a serious limitation of increased device leakage current which in turn increases power consumption and threatens the unimpeded progress of scaling trend in near future. Several research initiatives have been undertaken to search for an alternative solution with a view to innovate suitable substitute of MOSFETs keeping all its benefits intact.

This propelled the semiconductor industry from the domain of conventional MOSFETs to an altogether new transistor namely Tunneling Field Effect Transistors (TFETs) where the conduction of charge carriers in the channel depends on the mechanism of band-to-band tunneling of charge carriers from source valence band to channel conduction band through potential barrier instead of thermionic emission of 'free' carriers from the source into the channel across the potential barrier. This difference in the operating principle of TFETs enables them to break the fundamental restriction of subthrsehold limit of 60 mV/dec (in MOSFET) and achieve subthreshold slope less than this limiting value making TFETs a suitable alternative to MOSFETs for low power, low voltage applications. Thus, TFETs have nowadays become a dominant contributor in the unimpeded progress of microelectronics industry into sub-micron and nanometer regime by exhibiting superior short channel performance and can thus be regarded as a competent alternative to conventional MOSFETs.

In view of this, Chapter 6 attempts to present some research endeavors to incorporate the much discussed novel concept of 'work function engineered' gate electrode into the basic TFET structure in order to realize some improvised TFET structures which can alleviate the short comings of a simple TFET.

Section 6.3 of Chapter 6 presents an initiative to incorporate the concept of work function engineered gate electrode into a Double Gate TFET structure proposing a new device structure of Work Function Engineered Double Gate (WFEDG) TFET and compares its performance with that of a simple DG TFET in order to establish the efficacy of adopting the WFEG concept in TFETs also as evident from the reduced source-channel potential barrier depicted in surface potential profiles (vide Figs. 6.3.3, 6.3.4 and 6.3.5), surface electric fields (vide Figs. 6.3.6, 6.3.7 and 6.3.8) and superior current drivability (vide Figs.6.3.9 to 6.3.15) studied by varying the relative permittivities of gate oxide along with thicknesses of channel and gate oxide. The results obtained from analytical modeling are validated with SILVACO simulated data.

The next section 6.4 of Chapter 6 takes a step further to analytically explore the impact of interface trapped oxide charges (at the oxide-silicon interface near the source end) on the device performance by considering a Binary Metal Alloy SON (BMASON) TFET structure so as to tune the tunneling barrier by suitably modifying the mole fraction of the Binary Metal Alloy used as gate electrode with a view to boost the band-to-band tunneling of carriers resulting in enhanced device current with the simultaneous suppression of unwanted ambipolar effects. Device operation in such ultra nano dimension results in sharp increase in channel electric field which makes Hot Carrier Effect an inevitable issue, which leads to unwanted accumulation of trapped charges at the interface between gate oxide and semiconductor, thereby impacting device performance. On observing the comparative surface potential analysis of the proposed BMASON TFET with conventional Single Gate TFET (SG-TFET) (vide Fig. 6.4.3), it can be seen that potential barrier is much reduced in case of BMASON TFET compared to its SG TFET counterpart. Moreover, it can also be seen from Fig. 6.4.3 that the band bending at source-channel junction and subsequently the rate of carrier tunneling is increased due to the presence of localized trapped charges at the oxide-substrate interface, making it more advantageous over the case when the localized charges are absent. The variation surface potential of BMASON TFET along channel position for various values of V_{GS} (vide Fig. 6.4.4) and V_{DS} (vide Fig. 6.4.5) are also shown. The effects of interface trapped charges are also incorporated in the analytical model and has been studied by varying different device parameters in terms of channel electric field (vide Fig. 6.4.6), device current characteristics (vide Figs. 6.4.7, 6.4.8, 6.4.9 and 6.4.10), tunneling path length (vide Fig. 6.4.11) and subthreshold slope (vide Fig. 6.4.12) to obtain an insight to the Hot Carrier Effects in TFETs. The analytical results are validated with TCAD simulated data to confirm accuracy of our proposed model. The developed analytical model can thus be used to investigate the HCEs in TFETs with linearly graded binary metal alloy gate electrode and in the possible design of memory devices based on the concept of trapped charges.

Various research endeavors elucidated in this doctoral thesis in intricate detailing will provide some valuable insight for the research community of semiconductor devices and pave way for numerous innovative non-conventional device structures suitable for future low power low voltage applications to continue with the unhindered progress of nanoelectronics industry.

7.2. Future Scope

This doctoral thesis reports several research contributions in the area of low dimensional nano scale semiconductor devices. However, semiconductor industry is always evolving to keep pace with the stringent requirements imposed by the ITRS which opens up quite a lot of opportunities to innovate some improvised devices defining the future of semiconductors.

Some possible concepts are being recommended as future research avenues:

- Quantum mechanical effects may be incorporated in the analytical modeling of Tunneling Field Effect Transistors with work function engineered gate electrode for more accurate performance analysis of contemporary ultra low dimensional structures.

- Depletion regions at the source and drain ends may be incorporated in the analytical modeling of Tunneling Field Effect Transistors with work function engineered gate electrode for better modeling accuracy.

- Dielectric pockets near the source-channel and drain-channel junctions may be incorporated in the analytical modeling of Tunneling Field Effect Transistors with work function engineered gate electrode to study their effects on tunneling.

- New gate engineering techniques may be explored to improve performance of FETs.

- Alternative non-conventional device structures may be explored to solve the low ON current issue of contemporary TFETs.