PERFORMANCE IMPROVEMENT OF LOW DIMENSIONAL DEVICES AND EXPLORE SOME OF THEIR APPLICATIONS

THESIS

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CERTIFICATE FROM THE SUPERVISORS

This is to certify that the thesis entitled ***"Performance improvement of low dimensional devices and explore some of their applications"*** *submitted by Shri* ***Anup Sarkar*** *who got his name registered on 11/04/13(D-7/E/291/13) for award of Ph.D. (Engg.) degree of Jadavpur University is absolutely based upon his own work under the supervision of* ***Prof. Subir Kumar Sarkar*** *&* ***Dr.Ankush Ghosh*** *and that neither his thesis nor any part of the thesis has been submitted for any degree/diploma or any other academic award any where before.*

1._____ 2._____

[Prof. Subir Kumar Sarkar] [Dr.AnkushGhosh]

Dedicated to

My parents

Late Anil Kumar Sarkar

Smt. Kalpana Sarkar

For their motivation

&

My wife

Sanchita Sarkar

For her constant support and cooperation

and

My daughter Ishita Sarkar

My son Swastik Sarkar

To spare me for my work

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ABSTRACT

Microelectronics devices with low power have got tremendous importance in our modern lives. Low dimensional devices deals with the performance improvement & miniaturization of ICs. The evolution of miniaturization has produced complex system-on-chip (Soc) in which millions of transistor packed on a single silicon chip through the use of CMOS based ULSI technology platform. This has led to CMOS technology towards the deep sub-50 nm regime. However further miniaturization of MOS Transistors are facing GIDL limit and several unwanted problems like short channel effects (SCEs),Hot carrier effects, Gate-Dielectric reliability etc. arises. Due to the short channel Source/Drain encroachment begins to limit the gate's ability to control the channel and this causes Drain induced barrier lowering (DIBL) effect and threshold voltage roll–off problems. Also the leakage current of a scaled down transistor through the PN junction between the Si Substrate and the Source/Drain region increases which prevents the use of scaled down transistor in low standby power application. Moreover, the parasitic capacitances of transistor may strongly affect the characteristics of CMOS devices. Therefore, the use of planner technology for ULSI circuit becomes more challenging. This has led to researchers to investigate the device technology in two ways- one is SOI-MOSFET, SON-MOSFET, DMDG SON, DMTG SON etc. which are basically Extended CMOS type and another is beyond CMOS devices like SET, spintronics, straintronics etc.

Recently SOI technology has demonstrated promise for nano-CMOS scaling. In SOI a buried oxide layer (BOX) is placed under the Si active layer. This BOX can be seen as a blocking layer to reduce the fringing field effect (Drain Induced electric field) which reduces the lower off state leakage current and parasitic capacitances. SON MOSFET is achieved by replacing BOX layer with unity dielectric, i.e.air. The main advantages of SON MOSFET are their radiation immunity in extreme environment, less power consumption, further downscaling capability, low noise, higher short channel immunity, reduced fringing field effect and faster switching action due to lowest parasitic capacitance and low cost. Higher insulation of channel from thesubstrate with lowest dielectric constant material 'air' at box region, makes it suitable as a device at extreme climatic condition. In a SON structure thresholds voltage is also

much resistive against different SCEs as a result it shows lower threshold voltage roll off and less sub-threshold slope then SOI structure.

Dual-material double gate (DMDG) structures have been developed as a part of multi material gate engineering. In this technology gate electrode consist of either two metals or metal like materials placed in a symmetric manner or a binary metal alloy (A_xB_{1-x}) having linearly graded work functions. The material with higher work function is placed at the source side to get better result.

Now DMDG and Dual material tri-gate coupled with SON MOSFET shows a dramatic improvement over short channel effect than its counterpart which is examined in this thesis.

Among the beyond CMOS devices spintronics based research has become very prominent in the recent times. This makes candidate a venture in the area of spintronics where digital circuits have been designed and explored the feasibility of some real life application using single spin logic circuits like spintronics based RFID system which is ultra-dense, low power consuming and can be used in high speed VLSI/ULSI integrated circuits which is discussed in this thesis.

In straintronics the effect of stress on the magnetic energy of the device, via the magnetostriction property of the free layer is introduced which consumes much less energy and hence is more suitable for Nanomagnetic logic. Nanomagnetic logic can encode the logic bits through their bistable magnetization orientation. So, this logic system can be simultaneously used to process the binary information as well as basic memory building block. Here, the possibilities of designing two basic universal gates are discussed with ultra low power dissipation which can easily be operated from the energy harvesting from the nature.

Straintronics with the combination of MTJ makes the device more ubiquitous, so that input and output parameters can easily be penetrated. This Thesis examines the concept of straintronics switching and the intrinsic magnetic energies of the free layer of the MTJ and to design a three input NOR gate based on the model of the straintronics MTJ combination with a very high figure of merit.

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LIST OF ABBREVIATIONS

SCE: Short Channel Effects.

SOI: Silicon on Insulator.

SON: Silicon on Nothing.

DIBL: Drain Induced Barrier Lowering.

SMTG: Single Material Tri-Gate.

DMTG: Dual Material Tri-Gate.

RFID: Radio Frequecy Identification Device.

NML: Nano Magnetic Logic.

STR: Straintronics.

MTJ: Magneto-Tunnelling Junction.

TMR: Tunnelling Magneto resistance

INTRODUCTION AND ORGANIZATION OF THE THESIS

1.1 Introduction and Motivation

Ever since the invention of transistor, electronic devices envelop the human civilization, and become indispensable in every sphere of life from industrial process control, till automotive and consumer electronics/wireless communication. In the twenty first century people are becoming excessive dependent on process automation and habituated with lavish lifestyle and high speed real-time interconnectivity have been the driving force behind the explosive growth of all industrial processes and consumer electronics. This rapid growth in the field of electronics has been accompanied by constant device miniaturization. Reduction of circuit dimension reduces the overall circuit area, allowing more devices on a single die without negatively impacting the cost of manufacturing. Since the beginning constant miniaturization of electronic device has become the standard option to increase circuit speed, integration density and to reduce the cost and power. The ever-increasing demand for reliable electronic equipment of smaller size and low power requirement has led to the growth of microminiaturized circuits. A popular example of one such circuit, called integrated circuit (IC), is a combination of components like diodes, transistors, resistors, capacitors, and their interconnections, collectively grown into one or more complete circuits with several complex functions being implemented on the same chip. Ever increasing trend of device dimension down-scaling to a quasi-nanometer level allows the researcher's to explore complex integrated systems on a single chip which drastically reduces their volume and power consumption per function, thereby increasing their speed of operation significantly [1.1]. Recent advancements enabled us to incorporate the basic transistors in computer chips ever smaller sizes. While transistors are becoming smaller they are facing a number of challenges in terms of performance improvement and ensuring reliability [1.2]. At the moment the critical dimensions in these devices are just some 60 atoms thick, and further device size reductions will certainly stop at small atomic

dimensions. Consequently, new technologies will be needed for industry to keep pace with Moore's law [1.3], an observation that the number of transistors on a computer chip doubles about every two years, resulting in rapid progress in computers and telecommunications. It is becoming increasingly difficult to continue shrinking electronic devices made of conventional silicon-based semiconductors, called complementary metal-oxide-semiconductor (CMOS) technology.

An additional problem associated with Integrated circuits is that the chips now contain around 2 billion transistors and increasing no. of devices enhances the heating effect of the chip. With today's chips generating around 100 watts per square centimeter are comparable to that of a nuclear reactor. As a result, self-heating has become a fundamental concern that hinders performance and can damage transistors.

New generation portable embedded system smart devices like smart phones, IOTs require lower power to operate, meaning they can be operate for maximum time. The aim of such devices is minimum power for maximum battery life time. In fact, power considerations have been the ultimate design criteria in today's smart devices.

To tackle these issues researchers have taken two approaches. First one is trying to extend CMOS technology till further end [1.4-1.7]. One of these attempts is Silicon on Nothing (SON) technology [1.8-1.10]. The second groups of researchers are searching for an entirely new technology which will replace the existing CMOS technology [1.8-1.11].

The present thesis work has covered to solve the problem in both the ways.

Silicon-on-Insulator (SOI) technology can be considered as a new technology to extend CMOS further [1.12]. This offers a performance as expected from next generation Si technology. Short-channel-effects (SCEs), transistor scalability, and circuit performance are improved by using SOI technology [1.13]. SOI shows superior performance in terms of higher speed, lower power dissipation, higher tolerance to radiation, low values of parasitic capacitances, diminished short channel effects etc over its bulk counterpart, there are some unavoidable issues like short-channel effects (SCE) which arises with SOI devices in nano regime [1.14]. The ITRS report 2009 predicts that development and research on SOI MOS structure will be continued 2024 to achieve devices of dimension

less then 16nm with modified SOI structure. In the last decades, different SOI MOS structure has been proposed through experimental and theoretical hypothesis to realize improved the performance of conventional SOI MOSFET. Some the different proposed improved SOI structures are thin body FD SOI with raised source and drain, Metal Source and Drain FDSOI MOSFET, Metal gate FDSOI, Multiple-Gate FDSOI MOSFET, Ground-Plane FDSOI MOSFET, HALO Doped SOI. Silicon-on-Nothing (SON), an innovative SOI structure suggested and developed very recently, enables fabrication of extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm) super SOI devices, which are capable of quasi-total suppression of SCEs and excellent electrical performances [1.15]. In a SON MOSFET, the buried oxide of simple SOI structure is replaced with air and it has been proven both theoretically and experimentally that with the air-gap, the SCEs of the conventional SOI MOSFETs can be reduced to a further extent [1.16]. Moreover, since the so-called ''nothing'' (or air) layer embedded below the Si active film has lower dielectric permittivity than oxide, the parasitic capacitances between source/drain and substrate are reduced and therefore it is expected that higher circuit speed can be achieved with SON devices [1.17-1.19]. Due to the reduced permittivity of its dielectric (air in case of SON), SON structure reduces fringing field related DIBL or 2D charge sharing effect which is extremely important performance controlling parameter of thin channel FD SOI MOSFET. Along with improved performance SON structure can be combined with different SOI structures in search of improved performance. However, thick buried layer (BL) can be a drawback of SOI MOSFETs due to large positive charge accumulated in the thick BL. But in the case of SON MOSFET, no charge will accumulate in the air-gap [1.20].

Recently, Double Gate (DG) MOSFETs using lightly doped ultra thin layers are becoming popular as a promising option for ultimate scaling of CMOS technology [1.21]. In Double-gate SOI MOSFET, two gates simultaneously control the charge in the thin silicon body, forming two channels for current flow. Due to very small thickness of SOI film, a direct charge coupling invariably exists between the front and back gates [1.22], influencing the terminal characteristics of the device. Gate work function engineered MOSFETs such as Dual-Material gate MOSFET, linearly graded binary alloy gate MOSFET could significantly suppress the various SCEs [1.23-1.26]. But these concepts

have been implemented on 2-D planar MOSFETs till now. But it has always been a prime objective to achieve more and more control of the channel by the gate which could no longer be achieved with the planar MOSFETs. Tri-gate MOSFET shows a much better control over the channel by the gate. Tri-gate structures come with 37% speed enhancement and their power consumption is below 50% as compared to the planar MOSFETs [1.27-1.28].

To incorporate for the first time the advantages of Tri-gate SON structures and to study the potential benefits offered by dual-material gate in this new structure has been proposed to achieve significant control over the SCEs in the second chapter of the present thesis work.

Another group of researcher looking for alternative of technology for the last two decades found several new technologies that are under investigation. These aspirant technologies include, amongst others, resonant tunneling diodes (RTD) [1.29-1.30], single electron device (SED) [1.31-1.32], carbon nanotubes [1.33-1.34], rapid single flux quantum (RSFQ) [1.35], silicon nanowires [1.36], quantum dot cellular automata (QCA) [1.37], single electron transistors [1.38-1.42], and magnetic spin devices [1.43-1.46]. These are the entirely new technology for the next generation of electronics. But none of these technologies has succeeded in replacing the conventional silicon transistors, since the existing material and fabrication technology beyond the realms of the realistic. Moreover, except resonant tunneling devices all the devices are restricted to operate below the room temperature which cannot be used in real life applications.

To overcome these hurdles scientists have explored a novel concept called "Spintronics" [1.47-1.50]. Spintronics is a nanoscale technology in which information is carried not by the electron's charge (as it is in conventional devices) but by the electron's intrinsic spin. This opens new routes for design of new type of devices that are extremely faster, non-volatile, that have negligible boot up time, and also low power consumption [1.51-1.52]. Spintronics are expected to ensure continued adherence to Moore's law in the future. They already play an increasingly significant role in high density data storage, microelectronics, magnetic sensors, quantum computing, biomedical applications, and so on. It was the discovery of giant magneto resistance (GMR) in the early 1980s that initiated spintronic research and resulted in the first

generation of a spintronic device in the form of the spin valve [1.53]. Today, spintronic devices are ubiquitous on the desktop as spin valves play their role as the active element in the read head of most hard disk storage devices. Second-generation spintronic devices, called "Straintronics" will integrate magnetic materials and semiconductor devices to create new flexible devices such as spin transistors and spin logic. These Straintronics devices will not just improve the existing capabilities of electronic transistors, but will have new functionalities enabling future computers to run faster, but consume less power, and have the potential to revolutionize the IT industry as did the development of the transistor several decades ago.

Research on electron spin based phenomena in semiconductors began in 1990 after the first spintronic device; spin Field Effect Transistor, proposed by Datta and Das [1.54-1.55]. However more radical new idea involved using spin of a single electron or 'Single Spin Logic' proposed by S. K. Sarkar et al [1.56]

In this idea of spintronics was presented where information (binary data '1' & '0' for logic circuits) is encoded in the anti-parallel spin of electrons confined in quantum dots placed in magnetic field. . The intrinsic spin of an electron can be of two spin states, which denote as "*spin up*" and "*spin down*". Pauli Exclusion Principle dictates that the quantum mechanical wave function of two paired fermions must be anti-symmetric, no two electrons can occupy the same quantum state, implying that an entangled pair of electrons cannot have the same spin. This property of electron spin is exploited in spintronic devices.

Spin unlike charges has both magnitude and a polarization. It is easy to make spin a bistable quantity-and therefore use it to encode binary bits-by simply placing the electron in a magnetic field. The Hamiltonian describing a single electron in a magnetic field is given by-

$$\mathbf{H}=(\mathbf{p}-q\mathbf{A})^2/2m^*-(g/2)\mu\mathbf{B}.\boldsymbol{\sigma}$$

Where **A** is the vector potential due to magnetic flux density **B**, **μ** is the Bohr magnetron, **g** is the Lande-g factor and **σ** is the Pauli spin matrix. If the magnetic field is in the z-direction then diagonalization of the above Hamiltonian produces two mutually

orthogonal eigen spinors which are +z and –z polarized spins i.e. states whose spin quantization axes are parallel and anti-parallel to the z-directed magnetic field. Thus, spin quantization can become a binary variable and hence the "up" & "down" states of an electron can encode logic 0 &1 respectively or vice versa. These two spin polarization are stable, then the logic device can be switch only by flipping the spin without requiring physical movement of charges. This could save a lot of energy. Thus the spin device has an inherent advantage in terms of energy consumption. The power dissipation of this device per switching event is of a few tens of nano Watt. This device has some other advantages like ultra fast switching times of the order of few picoseconds, extremely high bit density approaching 10 terabits cm^{-2}, non volatile memory, possible room temperature operation, very high noise margin and very low power delay product (~10^{-30}Js) for switching between the logic levels [1.57].

But in spintronics a single spin is very unstable at room temperature as temperature of its operation is ~ 1K. This leads to new dimension of technology called straintronics.

In straintronics the effect of stress on the magnetic energy of the device, via the magnetostriction property of the free layer is introduced [1.58-1.60]. In straintronics tiny nanomagnets are used to encode logic bits with their magnetization orientation. This makes the Nanomagnetic logic (NML) system both non volatile and energy efficient since the magnets have no leakage. Benett clocking [1.61] is used to flip the magnetization orientation of the magnets synchronously. Desired logic gates can be obtained by engineering the dipole interaction between the nanomagnets along with the applied dc bias field. Hence, by wiring with this nano-magnet's linear array any combinational or digital logic circuit can be built up. Other than stress flipping of magnetization orientation of nanomagnets can be done by either current induced magnetic field or spin transfer torque. But stress induced rotation consumes much less energy and hence is more suitable for Nanomagnetic logic clock. For Nanomagnetic logic both single and composite multiferroics are increasingly used mostly to build up high dense data storage and multifunctional devices [1.62]. Composite multiferroics have advantages as high magnetoelectric response and high operating temperature.

Nanomagnets consume very low energy that is 4.2 $\times 10^{-17}$ Joule is consumed per gate operation [1.63]. The candidate has shown through numerical simulation the feasibility of nanomagnetic logic using multiferroics nanomagnets. Nanomagnetic logic can encode the logic bits through their bistable magnetization orientation. So this logic system can be simultaneously used to process the binary information as well as basic memory building block. Straintronics based logic gates differ from traditional gates as it can process and store information simultaneously. It provides minimum energy dissipation in designing of computer architecture by eliminating the need of refresh clock cycles. Non-volatile properties of these gates can improve the system reliability and eliminate the delay of a computer. Moreover NML can increases the logic density by two fold than conventional logic system. So it can act as an associative memory element which has the application in image recovery, pattern recognition and digital signal processing functions. By optimum choice of material (Terfenol-D), energy dissipation can be reduced sufficiently in which logic system can be run by harvesting energy from local surroundings. So in a nutshell, it can be told that it is dense, low power and is capable of higher order signal processing function which can enhance the basic requirements of miniaturization of straintronics devices.

Tunnel magnetoresistance (TMR) in Magneto Junction Tunneling (MTJ) was first invented by Julliere in 1975 in Fe/GeO/Co (soft magnet/nonmagnetic/hard magnet) junction [1.64]. It was observed that the resistance across the MTJ is maximum at the anti parallel magnetization orientation of the two layers, while the low value is observed in the parallel orientation. These high and low resistance, denote the binary logics 0 and 1 in a logic circuit and their ratio is known as Tunnel Magneto resistance (TMR). After this research have been focused to obtain the high value of TMR [1.65-1.70].Soon after this the principle of TMR was used to build magnetic random access memory (MRAM)[1.71-1.76] . It is theoretically proven that the switching energy limit of a charge based logic is $NkTln(1/p)$ where N represents the number of charge carriers, T is the operating temperature, and p is the bit error probability . However, for a magnetic based logic this energy lowers to $kTln(1/p)$ due to the single domain magnetic coupling. Therefore,

magnetic based devices are expected to be N times more energy efficient than the charge-based devices.

Two conventional methods for switching the magnetisation state of the MTJ are Field induced magnetization switching (FIMS) and spin transfer torque (STT) flipping. In FIMS an external magnetic field is used which is generated by a current flow through a nearby wire. This method consumes energy. Due to the high current values, the energy efficiency of this method is very low. Moreover the device need to be wide and the MTJs are susceptible to inter-cell magnetic field interference. The spin transfer torque (STT) switching uses spin-polarized current flow through the device, which increases its scalability with CMOS technologies. Energy consumption is still high in STT.

There is a need to investigate alternative approaches to tackle the energy and reliability issues of the FIMS and STT. Recently electric-field-assisted switching of the MTJ has been proposed. Although it is energy efficient at the interface of MgO/ CoFeB but it still employs an external bidirectional magnetic field for switching. Generating this field can again be power consuming, produces complicated design procedures and needs more space and might lead to inter-field interferences, leading to further scaling. Straintronics based switching is proposed recently as an alternative energy efficient method to switch the state of the MTJ. In straintronics the voltge based switching is achieved instead of static current which makes the straintronics device highly energy efficient than any nanomagnetic logic device.

So far we have discussed, Spintronics as well as straintronics are fundamentally more powerful than the conventional CMOS technology. This makes candidate a venture in the area of spintronics and straintronics presented from chapter 3 to chapter 6.

1.2 Organization of the Thesis

The thesis is divided into seven chapters and its outline is described as given below:

♉**Chapter I** presents the need for device miniaturization. CMOS technology and its future associated with device miniaturization are also discussed including the need for alternative device structures to overcome the shortcomings of CMOS technology. This led to the introduction of SOI, Spintronics and Straintronics devices. It also describes the

fundamental concepts related to SOI/SON, Spintronics and Straintronics devices along with overall analysis of their advantages & disadvantages. Objective of the project and outline of the thesis is given at the end of the chapter.

♉**Chapter II** introduces a newly emerging technology called spintronics. Spintronics is the technology where information (binary data '1' & '0' for logic circuits) is encoded in the anti-parallel spin of electrons confined in quantum dots placed in magnetic field. Spintronic devices unlike simple electronic devices, utilize not only charges but also another property of electron called spin. The aim in such devices is minimum power for maximum battery life time in addition to its capability to incorporate higher density of integration. This chapter contains basic ideas, principles and calculations associated with spin based device called single spin logic. Basic Boolean logic gates are designed here using single spin logic. This chapter shows a real life application of spintronics. A RFID system is designed using single spin logic. The present circuit is much faster than the conventional logic circuits and supports very high-density of integration. In this respect the present work is an early attempt for spin based RFID systems.

♉**Chapter III** introduces second generation of Spintronics called straintronics. Using straintronics based nanomagnetic logic (NML), basic gates can be implemented which is beyond traditional logic. Nanomagnetic logic encodes the logic bits in their magnetization orientation. This makes the logic system both non volatile and energy efficient since the magnets have no leakage. Benett clocking is used to flip the magnetization orientation of the magnets synchronously. Now desired logic gates (NAND) can be obtained by engineering the Dipole interaction among the nanomagnets along with the applied Benett-clocking. Now by wiring with this nano-magnet's linear array, any combinational or digital logic circuit can be built up. Other than stress, flipping of magnetization orientation of nanomagnets can be done by either current induced magnetic field or spin transfer torque (STT). But stress induced rotation consumes much less energy and hence is more suitable for Nanomagnetic logic clock. For Nanomagnetic logic, both single and composite multiferroics are increasingly used

mostly to build up high dense data storage and multifunctional devices. Composite multiferroics have advantages as high magnetoelectric response and high operating temperature. Here the possibility of making four-state NAND gates with the composite multiferroics (Terfenol-D/PZT) are studied in which very low energy that is 4.2 $\times 10^{-17}$ Joule is consumed per gate operation.

♉In **Chapter IV,** author implemented another basic logic gate, 'NOR' using NML with the composite multiferroics consisting of nickel (Ni) and PMN-PT. In this chapter multiferroics nanomagnet consisting of piezoelectric layer (lead magnesium niobate lead titanate-PMN-PT) with a thin magnetostrictive layer (Ni) has been studied. By enlightening the multiferroics functionality with introducing biaxial magnetocrystalline anisotropy in the magnetostrictive layer, a four state NOR gate can be implemented by the linear array of three nanomagnets. Each nanomagnet's magnetization orientation can produce 4-state condition. The peripheral magnets are encoded with input bits, and the central magnet's magnetization orientation is encoded without put bits. This type of NML not only increase the logic density by two fold over the conventional 2 state, but also acts as an associative memory element because of its four distinct minima. It can also be implemented in non-Boolean application such as image recognition and processing.

♉**Chapter V,** the author discusses the concept of straintronics switching and the intrinsic magnetic energies of the free layer of the MTJ and to design a three input NOR gate based on the model of the straintronics MTJ combination. Here lead magnesium niobate lead titanate (PMN-PT) is chosen as piezoelectric material which is the top layer and its thickness is 50nm which ensures the complete transfer of generated strain to the next layer which is much thinner magnetostrictive layer of cobalt of dimension (120×80×6) nm. The bottom layer is a synthetic anti ferromagnet with large anisotropy energy barrier, which is permanently magnetized in the left direction of the easy axis. The layer between ferromagnet and anti ferromagnet is a spacer layer of MgO of thickness 1 nm. It is used for tunneling magneto resistance (TMR) in MTJ structure.

By analyzing the magnetization dynamic of the proposed structure with the second degree control equation a 3-input NOR gate can be built which has a very low energy delay product (24×10^{-30}Js) and which can also be used for basic memory element.

♉ **Chapter VI** concludes the analysis from the thesis which has considerable impact in future low dimensional device research, and such study will open numerous new areas of nanodevice applications.

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Chapter 2

PERFORMANCE ANALYSIS OF HIGH-K DUAL MATERIAL TRI-GATE SON MOSFET

2.1 Introduction:

Researchers have always aimed in achieving cost-effective, miniaturized, high speed and low power consuming devices for VLSI circuit design. Devices with the above features can only be achieved through device downscaling. However, aggressive downscaling results in severe short channel effects (SCE) like drain-induced barrier lowering, hot carrier effects, degradation of Subthreshold characteristics etc. [2.1]. In order to combat such SCEs, innovative as well as renovated technology like Silicon-on-Insulator (SOI) has been proposed [2.2]. SOI shows superior performance in terms of higher speed, lower power dissipation, higher tolerance to radiation, low values of parasitic capacitances, diminished short channel effects etc over its bulk counterpart, there are some unavoidable issues like short-channel effects which arises with SOI devices in nano regime [2.3]. The ITRS report 2015 predicts that development and research on SOI MOS structure will be continued 2024 to achieve devices of dimension less then 14nm with modified SOI structure. In the last decades, different SOI MOS structure has been proposed through experimental and theoretical hypothesis to realize improved the performance of conventional SOI MOSFET. SOI technology is quite immune to the SCEs, however, it suffers from such major drawbacks like Self heating effect, Dynamic floating body effects and parasitic bipolar effects, higher off-current due to a forward biased body-source junction and many more.

Some the different proposed improved SOI structures are thin body FD SOI with raised source and drain, Metal Source and Drain FDSOI MOSFET, Metal gate FDSOI, Multiple-Gate FDSOI MOSFET, Ground-Plane FDSOI MOSFET, HALO Doped SOI. Silicon-on-Nothing (SON), an innovative SOI structure suggested and developed very recently, enables fabrication of extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm) super SOI devices, which are capable of quasi-total suppression of SCEs and excellent electrical performances [2.4]. SON technology retains all the advantages of

SOI technology. It also has some additional advantages such as highest dielectric isolation for the active channel region with "air" as buried layer, Reduced electrostatic coupling through the buried layer, initiates lower power consumption, enhances farther scaling capability, shows low noise, develops higher short channel immunity, delivers faster switching action and reduces cost. In a SON MOSFET, the buried oxide of simple SOI structure is replaced with air and it has been proven both theoretically and experimentally that with the air-gap, the SCEs of the conventional SOI MOSFETs can be reduced to a further extent [2.5]. Moreover, since the so-called ''nothing'' (or air) layer embedded below the Si active film has lower dielectric permittivity than oxide, the parasitic capacitances between source/drain and substrate are reduced and therefore it is expected that higher circuit speed can be achieved with SON devices [2.6-2.8]. Due to the reduced permittivity of its dielectric (air in case of SON), SON structure reduces fringing field related DIBL or 2D charge sharing effect which is extremely important performance controlling parameter of thin channel FD SOI MOSFET. Along with improved performance SON structure can be combined with different SOI structures in search of improved performance. However, thick buried layer can be a drawback of SOI MOSFETs due to large positive charge accumulated in the thick BL. But in the case of SON MOSFET, no charge will accumulate in the air-gap [2.9].

But only SOI/SON could not sufficiently suppress the SCEs. Hence a novel concept, namely gate work function engineering has been introduced. Gate work function engineered MOSFETs such as Dual-Material gate MOSFET; linearly graded binary alloy gate MOSFET could significantly suppress the various SCEs [2.10-2.11]. Recently, Double Gate (DG) MOSFETs using lightly doped ultra thin layers are becoming popular as a promising option for ultimate scaling of CMOS technology [2.12]. In Double-gate SOI MOSFET, two gates simultaneously control the charge in the thin silicon body, forming two channels for current flow. Due to very small thickness of SOI film, a direct charge coupling invariably exists between the front and back gates [2.13], influencing the terminal characteristics of the device. But these concepts have been implemented on 2-D planar MOSFETs till now. But it has always been a prime objective to achieve more and more control of the channel by the gate which could no longer be achieved with the

planar MOSFETs. INTEL's recently introduced tri-gate MOSFETs show a much better control over the channel by the gate. Tri-gate structures come with 37% speed enhancement and their power consumption is below 50% as compared to the planar MOSFETs [2.14].

Considering the advantages of the Tri-gate structure and incorporating the gate work function engineering technology, that is, by introducing a dual-material gate in the tri-gate structure, a novel device namely High-K Dual Material Tri-gate SON MOSFET has been proposed to achieve significant control over the SCEs. The High-K technology is well-known for reducing the gate-oxide leakages and hence highly improves the Subthreshold characteristics of the device [2.15]. To retain the advantages of the SON technology, we have considered SON configuration in our proposed model. The results obtained from analytical modeling are verified using simulation data obtained from ATLAS.

2.2 Literature Survey:

In the last few decades there has been a huge growth of nanoscale semiconductor devices. As traditional CMOS technology has achieved their boundary level, SOI-MOSFET as an extended CMOS technology has been identified as one of the promising technology for enhancing the performance of MOSFET [2.16]. Threshold voltage variation of SOS (silicon on sapphire) MOSFET, with the epitaxial film thickness has been studied first by Sasaki and Togei [2.17] in 1979. After that Sano et. al. [2.18] published the threshold voltage dependency on back gate bias in 1980. In the same time, Worly [2.19] derived an analytical model for the threshold voltage of an SOS transistor in which charge coupling between the front and the back gates are alike SOI MOSFET. In 1983 a new and more accurate threshold voltage model was proposed by H. K.Lim et. al. and depletion approximation I-V model was developed by P. W. Barth et. al [2.20-2.21].

A new n-type and p-type SOI MOSFET structures in which the electrical parameters at the back and the front threshold voltages were described by Ballestra et.al. in 1985 [2.22].

In 1986, Davis et. al. [2.23] showed an improved subthreshold slope of about 50 mV/ decade can be achieved with an n-channel MOSFET fabricated on SOI substrate. Proper derivation of the subthreshold characteristic is a prima facie requirement to design & modeling of a transistor. In 1987, the current-voltage model in subthreshold region for a submicrometer fully depleted SOI MOSFET was developed by Fossum [2.24]. In his study Fossum explained the reason of huge drain current in subthreshold region due to impact ionization at the drain end. In the next year, a charge sharing model was proposed by Veerraghavan and Fossum al. [2.24] which predicted a L -1 threshold voltage dependence. In this model, constant surface potential was assumed to be independent of drain potential. However, this model does not take care of drain induced barrier lowering (DIBL) and the coupling effect between the front and the back gates. So this model is not suitable for modeling of SOI MOSFET.

In 1989, a better two-dimensional analytical threshold voltage model for short channel FDSOI MOSFET, was developed by K K Young [2.25]. That model is based on the soln. of 2D Poisson's eqn. and also has considered the vertical field and lateral field effects under parabolic potential profile approximation. In the same year a novel concept of split-gate structure,was proposed by Shur et. al. [2.26]. This was the originator of idea for the Dual Material gate structure by applying different gate-bias in splitgate.

In 1989, the IBM Research Division started a new research program on design & developing of SOI based CMOS device. [2.27]. For this purpose in the early 1990s, the Advanced Silicon Technology Center (ASTC) of the IBM Microelectronics Division had started to develop SOI based CMOS device.

In 1990, Jason C. S. Woo et. al. developed a thin silicon channel SOI MOSFET model which have gate as well as buried oxide regions. Later, Francis Balestra et. al. suggested an analytical model of thin-film and ultra-thin-film SOI MOSFET consisting of two or three interfaces [2.28].

In 1991, Tokunaga et. al. [2.29], published the relation between subthreshold slopes in submicron n-channel FD SOI MOSFETs with the substrate & Drain bias as well as temperature. He also explained that for a low drain voltage, MOSFET can be represented by a simple capacitor model.

The statistical analysis due to randomness in impurity distribution in both bulk and SOI MOSFET was studied by Chen and Li [2.30] in 1992. Later Brews proposed a empirical scaling rule for [2.31] SOI MOSFET.

In 1993, Guo and Yu [2.32] suggested Green's function technique for the solution of the 2D Poisson's equation in FDSOI MOSFET. In the subsequent year, Tommy C. Hsiao et. al. developed an improved analytical current-voltage model for sub-micrometer FDSOI MOSFET [2.33].

In 1995, Srinivasa R. Banna et. al. developed a quasi-two-dimensional based short-channel threshold voltage model considering the substrate current and other hot-electron effects in low dimensional bulk type MOSFET's [2.34].

Later Yuhua Cheng et. al. developed a modified I-V model for fully depleted SOI MOSFET with deep sub-micrometer channel length [2.35] with the inclusion of various important short channel effects.

In 1997, Long et. al. [2.36] suggested first Dual material gate field effect transistor (DMGFET) where the gate was formed with the two materials of different work functions. In this novel structure, the step up distribution of threshold voltage near drain end in the channel reduces the DIBL with other short chanel effect. In the subsequent year Jeffrey W. Sleight et. al., in 1998, proposed a compact model for circuit simulations with taken care of body depletion condition [2.37] with the flexibility of taking into accounts the transitions behavior between FD and PD during the device operation.

In 2000, a current-voltage model for ultra-short channel SOI MOSFET was proposed by J. B. Roldán et. al. for circuit simulation which includes the velocity overshoot, series resistance and self-heating effects [2.38].

In 2001, M. Youssef Hammad et. al. developed an analytical model for the PDSOI MOSFET incorporating all possibilities of front-back interface coupling. [2.39].

In the next year, T. Ernst et. al., published another compact model with taken care of lateral field penetration in the buried oxide and underlying substrate of FDSOI MOSFET [2.40].

In 2003, the model of FD single gate SOI MOSFET suggested by Kunihiro Suzuki et. al. have analysed the 2-D effects in both SOI and buried-oxide layers [2.41]. This model paved the pathway of short-channel effects on the parameters like channel-doping

concentration, gate oxide and buried-oxide thickness etc. Anurag Chaudhry et. al., in 2004, published a review article narrating all the causes of possible performance degradation of a short channel SOI MOSFET [2.42]. Subsequently, they have suggested a novel device concept of Dual-Material Gate (DMG) SOI MOSFET [2.43] which has better efficiency in dominating SCEs such as drain-induced barrier lowering (DIBL), channel length modulation and hot-carrier effects.

In 2005, G.V. Reddy and M.J. Kumar developed a novel structure called Dual Material Double Gate (DMDG) Fully Depleted SOI MOSFET [2.44] by incorporating the merits of the DMG and DG structures.

In the research paper of Norio Sadachika et. al. [2.45] the surface potential in the MOSFET channel was solved iteratively, with taking into account all relevant device parameters of the SOI MOSFET.

Another revolutionary idea of 2-D potential function perpendicular to the channel FD SOI MOSFET with vertical Gaussian profile was demonstrated by Guohe Zhang et. al. [2.46]. Te-Kuang Chiang, analysed sub-threshold behavior model for the short-channel tri-material gate-stack SOI MOSFET [2.47].

A complete surface-potential-based compact model of Dynamic depletion SOI MOSFET was shown by Weimin Wu et. al. [2.48]. In this paper coupling equations for the front and back surface potentials have been rectified to include the back gate effect.

Despite of all these efforts SOI-MOSFET is not fully immune to SCEs. Hence, some modification of SOI MOSFET structure like Silicon-On-Nothing (SON) MOSFET has been emerged [2.49]. An efficient fabrication technique of SON structure has been proposed by V. Kilchytska et.al.[2.50] through wafer bonding technique.

Jurczak et. al. [2.51] developed a novel concept of Silicon-on-Nothing which is capable of reducing SCEs by incorporating ultra thin layers of oxides and silicon film. SON devices also exhibit excellent threshold voltage roll-off. Gate engineering technique is used in the dual-material gate (DMG) DG MOSFET in which two different materials having different work functions are merged together to form a single gate of a bulk MOSFET [2.52]. In this DMG structure, the work function of the gate material closer to the source is kept higher than that the drain for n-channel DG MOSFETs [2.53]. The device has the same threshold voltage for a reduced doping concentration in the channel region,

yielding better immunity towards mobility degradation and it exhibits higher transconductance. They are also free from the drawbacks like self-heating, high S/D series resistance etc. found in conventional SOI devices. Due to its above mentioned advantages, SON is gradually becoming the fundamental technology for the next generation ULSI era.

2.3 Model Structure:

A new model is proposed with high k dual material tri-gate SON MOSFET. A 3D view of the proposed model is shown in Fig. 2.1. Here the channel length of SON MOSFET is taken as L. Channel width and thickness is considered as w and t_{Si} respectively. Thickness of the high dielectric is t_2 and the thickness of the interfacial SiO_2 layer is t_1. The effective oxide thickness is t_f. Thickness of the buried air layer is t_b. N_a is the uniform channel doping and N_d is the source/drain doping concentration and ϕ_{M1} and ϕ_{M2} is the work functions of the metals M1 and M2.

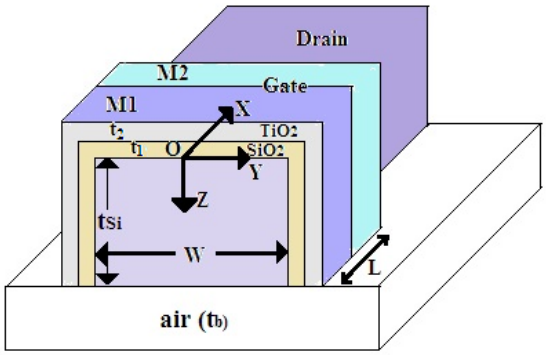

Fig.2.1 3-D cross-sectional view of High K Dual-Material tri-gate SON MOSFET

2.4 Analytical Modeling

We need to consider 3-D Poisson's equation in order to obtain an expression for surface potential of the device. It is assumed that the channel is fully depleted under zero bias, the impurity density and influence of the charge carriers are uniform on the electrostatics of the channel [2.14].

The channel is divided into two regions, Region 1 and Region 2 for the ease of calculation.

$$\frac{\partial^2\phi_j(x,y,z)}{\partial x^2}+\frac{\partial^2\phi_j(x,y,z)}{\partial y^2}+\frac{\partial^2\phi_j(x,y,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{Si}} \tag{2.1}$$

Where j=1 for region1 defined by the boundaries (0≤ x ≤L1, 0≤ z ≤t_{Si}, -w/2≤ y ≤w/2) and j=2 for region 2 defined by the boundaries (L1≤ x ≤L, 0≤ z ≤t_{Si}, -w/2≤ y ≤w/2).Here, ε_{Si} is the permittivity of Si, q is the electronic charge. The x-axis is taken along the channel length, y-axis is taken along channel width, z-axis is taken along the channel thickness.

We need to consider the parabolic potential approximation [2.15] between the lateral gates as we have considered a short channel MOSFET which is as follows:

$$\phi_j(x,y,z)\approx a_{0j}(x,z)+a_{1j}(x,z)y+a_{2j}(x,z)y^2 \tag{2.2}$$

j=1,2 for region 1 and 2 respectively.

For low drain voltages, the potential distribution is parabolic in the z-direction [2.54]. At y=0 we have

$$\phi_j(x,0,z)=a_{0j}(x,z)=\phi_{Sj}(x)+C_{1j}(x)z+C_{2j}(x)z^2 \tag{2.3}$$

$\phi_{Sj}(x)$ being the surface potential for regions 1 and 2.Because of the symmetry in y-direction we have, $a_{1j}(x,z)=0$ (2.4)

Therefore, $a_{2j}(x,z)=(4/w^2)(\phi_{Sj}(x)-a_{0j}(x,z))$ (2.5)

In order to solve equation 1, we need to consider the following boundary conditions

$$\phi_1(0,y,z)=V_{bi} \tag{2.6}$$

$$\phi_2(L,y,z)=V_{bi}+V_{ds} \tag{2.7}$$

Here V_{bi} is the built-in potential towards the source side and V_{ds} is the drain-to-source voltage.

$$\left.\frac{d\phi_j(x,y,z)}{dz}\right|_{y=0,z=0}=\frac{\varepsilon_{Ox}}{\varepsilon_{Si}t_f}\left(\phi_{Sj}(x)-V_{gsj}{}'\right) \tag{2.8}$$

$t_f = t_1+t_2(e_1/e_2)$;

where e_1 is the dielectric constant of SiO_2 layer and e_2 is the dielectric constant of the oxide placed above SiO_2.

Here $V_{gsj}' = V_{gsj} - V_{fbj}$, V_{fbj} is the flat band voltage at the front interface of Region j under Mj, $V_{fbj} = \phi_{Mj} - \phi_{Si}$, ϕ_{Si} is the work function of Si.

$$\left.\frac{d\phi_j(x,y,z)}{dz}\right|_{y=0,z=t_{si}} = \frac{\varepsilon_{air}}{\varepsilon_{Si}t_b}(V_{sub}' - \phi_{Sbj}(x)) \tag{2.9}$$

ϕ_{Sbj} is the potential at the back interface. j=1,2.

$V_{Sub}' = V_{Sub} - V_{fbb}$, V_{Sub} is the substrate bias voltage and is kept fixed at 0V, V_{fbb} is the channel-back interface flat band voltage.

Using equations (2) and (8),

$$C1j(x) = \frac{\varepsilon_{Ox}}{\varepsilon_{Si}t_f}\left(\phi_{Sj}(x) - V_{gsj}'\right) \tag{2.10}$$

Using equations (5),(9) and (10) we get,

$$C2j(x) = \frac{V_{Sub}' - \phi_{S1}(x)\left(1+\frac{C_{Ox}}{C_{Si}}+\frac{C_{Ox}}{C_{air}}\right)+V_{gs1}'\left(\frac{C_{Ox}}{C_{Si}}+\frac{C_{Ox}}{C_{air}}\right)}{t_{Si}^{\,2}\left(1+2\frac{C_{Si}}{C_{air}}\right)} \tag{2.11}$$

C_{Ox} is the oxide capacitance, C_{Si} is the Si channel capacitance, C_{air} is the buried air layer capacitance.

Now, for region 1, the 3-D potential distribution is

$$\phi_1(x,y,z) = \phi_{S1}(x)C + D \tag{2.12}$$

Where, $C=1+g_1z-g_2z^2-g_3zy^2+g_4z^2y^2$ $D=-g_5z+g_6z^2+g_7zy^2-g_8z^2y^2$

$$g_1 = \frac{\varepsilon_{Ox}}{\varepsilon_{Si}t_f},$$

$$g_2 = \frac{\left(1+\frac{C_{Ox}}{C_{Si}}+\frac{C_{Ox}}{C_{air}}\right)}{t_{Si}^{\,2}\left(1+\frac{2C_{Si}}{C_{air}}\right)},$$

$$g_3 = \frac{4}{w^2} g_1 ,$$

$$g_4 = \frac{4}{w^2} g_2 ,$$

$$g_5 = \frac{\varepsilon_{Ox} V_{gs1}{}'}{\varepsilon_{Si} t_f} ,$$

$$g_7 = \frac{4}{w^2} g_5 ,$$

$$g_8 = \frac{4}{w^2} g_6 ,$$

$$g_5{}' = \frac{\varepsilon_{Ox} V_{gs2}{}'}{\varepsilon_{Si} t_f} ,$$

$$g_7{}' = \frac{4}{w^2} g_5{}' ,$$

$$g_6 = \frac{V_{Sub}{}' + V_{gs1}{}' \left(\frac{C_{Ox}}{C_{Si}} + \frac{C_{Ox}}{C_{air}} \right)}{t_{Si}{}^2 \left(1 + \frac{2C_{Si}}{C_{air}} \right)} ,$$

$$g_6{}' = \frac{V_{Sub}{}' + V_{gs2}{}' \left(\frac{C_{Ox}}{C_{Si}} + \frac{C_{Ox}}{C_{air}} \right)}{t_{Si}{}^2 \left(1 + \frac{2C_{Si}}{C_{air}} \right)}$$

Now, for region 2, the 3-D potential distribution is

$$\phi_2 (x, y, z) = \phi_{S2} (x) E + F \tag{2.13}$$

By calculation, E=C,

$$\text{F=} -g_5{}' z + g_6{}' z^2 + g_7{}' z y^2 - g_8{}' z^2 y^2 \tag{2.14}$$

Constants g_5', g_6', g_7' and g_8' are given in Appendix. Using equation (2.12) and (2.13) in equation 1,

$$\frac{d^2\phi_{Sj}(x)}{dx^2} - \alpha\phi_{Sj}(x) = \beta_j \tag{2.15}$$

$$\alpha = \frac{2g_2 + 2g_3 z - 2g_4 z^2 - 2g_4 y^2}{C},$$

$$\beta_1 = \frac{qN_a}{C\varepsilon_{Si}} + \frac{-2g_6 - 2g_7 z + 2g_8 z^2 + 2g_8 y^2}{C} \quad \beta_2 = \frac{qN_a}{C\varepsilon_{Si}} + \frac{-2g_6' - 2g_7' z + 2g_8' z^2 + 2g_8' y^2}{C}$$

The general solution to equation (2.15) is given by

$$\phi_{S1}(x) = M_1 e^{\eta x} + M_2 e^{-\eta x} - \sigma_1 \qquad \text{for region 1}$$

Here, $\sigma_1 = \frac{\beta_1}{\alpha}$ The general solution to equation (2.15) is given by.

$$\phi_{S2}(x) = M_3 e^{\eta(x-L1)} + M_4 e^{-\eta(x-L1)} - \sigma_2$$

Here, $\sigma_2 = \frac{\beta_2}{\alpha}$

Constants M_1, M_2, M_3, M_4can be evaluated using the following boundary conditions. Potentials at the interface of the two different materials M1 and M2 must be continuous [2.8].

Hence, $\phi_1(L1,0,0) = \phi_2(L1,0,0)$ that is, $\phi_{S1}(L1) = \phi_{S2}(L1)$ and

$$\left.\frac{d\phi_1(x,y,z)}{dx}\right|_{x=L1} = \left.\frac{d\phi_2(x,y,z)}{dx}\right|_{x=L1}$$

The Electric field is calculated as $E = -\frac{d\phi_S(x)}{dx}$

The Subthreshold Swing [2.55] (in mV/decade) is

$$S = 2.3V_t\left[\frac{d\phi_{S\min}}{dVgs}\right]^{-1} \tag{2.16}$$

Where $\phi_{S\min}$ is the minimum surface potential.

Parameter	**t_1**	**t_2**	**t_{Si}**	**t_b**	**N_a**
Values	1nm	2nm	10nm	50nm	$1x10^{20}m^{-3}$
Parameter	N_d		ϕ_{M1}	ϕ_{M2}	w
Values	$5x10^{27}m^{-3}$		4.8eV	4.6eV	5nm

Table 2.1. Parameters used for calculation and simulation.

2.5 Results and Discussions

The proposed model has been simulated in ATLAS™ software. Observation of the simulated results is shown in the following figures with discussions. The channel length has been taken as 60nm. For calculation and simulation the ratio L1: L2 of material M1 and M2 has been considering as 1:1.

Fig. 2.**2** shows the variation of surface potential along the channel length for High K Single Material Tri-gate SON MOSFET and High K Double Material Tri-gate SON MOSFET. It can be observed that our proposed model possesses a single step profile which allows a high immunity towards the Drain-induced barrier lowering (DIBL) but the single metal structure does not possess any such step profile and hence it cannot battle the major SCEs. A drain voltage fluctuation can affect the potential minimum of the single metal structure and makes it highly prone to DIBL.

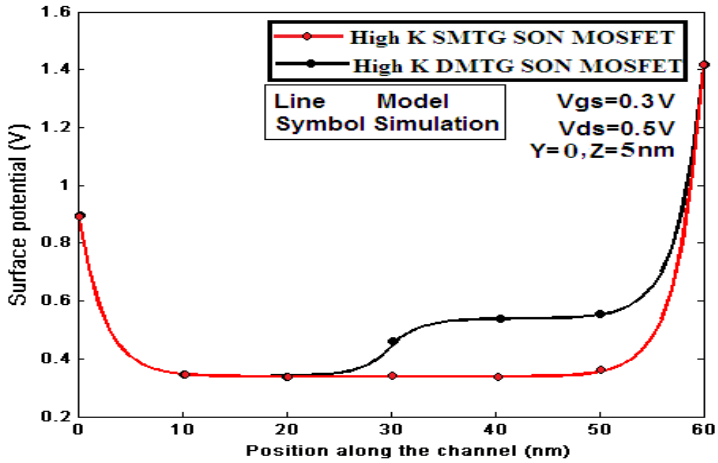

Fig. 2.2 Surface potential variation along the channel length for High K Single Metal Tri-gate and High K Double Metal Tri-gate SON MOSFETs

Fig. 2.**3** presents the variation of electric field along the channel length for High K Single Material Tri-gate SON MOSFET and High K Double Material Tri-gate SON MOSFET. The comparative study between the two structures show that the electric field at the drain side is much reduced for our proposed model compared to its single metal counterpart. This results in reduced Hot Carrier Effect (HCE) in our proposed model. **Fig.** 2.**4** shows the variation of Subthreshold swing along the channel length for different oxides placed above the layer of SiO_2. It can be observed that our proposed model with highest dielectric value of $40\,\varepsilon_0$ (i.e TiO_2) has the best characteristic of Subthreshold swing compared to the lower k value oxides. The analytical results of this section match well with the simulated data.

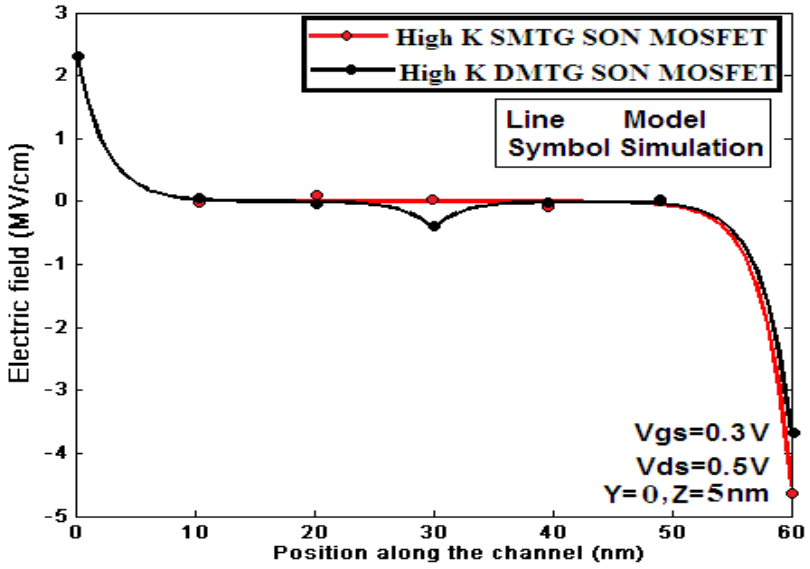

Fig. 2.3**Electric Field variation along the channel length for High K Single Metal Tri-gate and High K Double Metal Tri-gate SON MOSFETs**

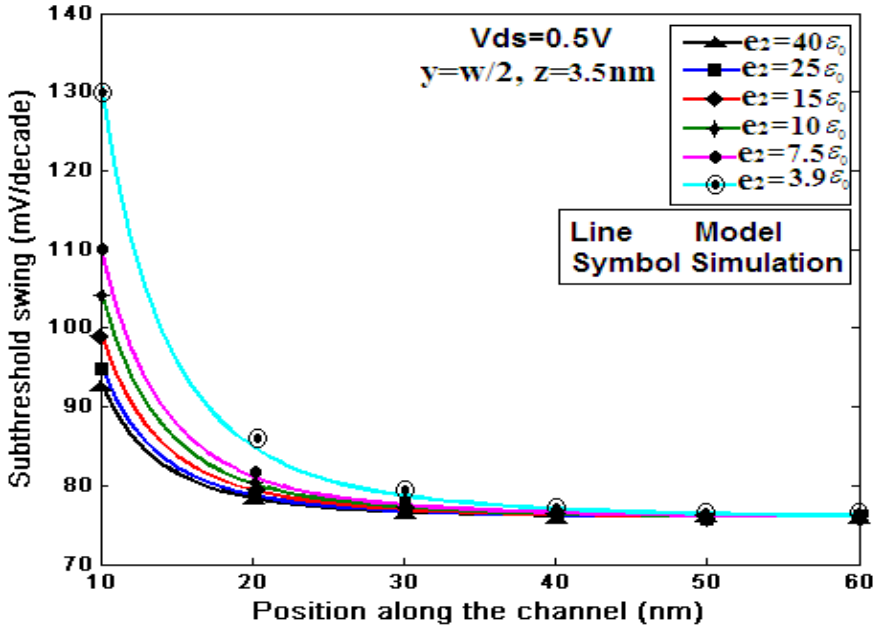

Fig. 2.4Subthreshold Swing variation along the channel length for the proposed model for different oxides placed above SiO_2

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SPINTRONICS DEVICE BASED LOW POWER RFID SYSTEM

3.1 Introduction:

The trend of miniature in future commercial CMOS integrated circuit may scale down to few nm in next decade. The reduction of power dissipation at the same pace is the main challenge in those miniature devices. In fact, reduction of power is the main reason behind the popularity of portable devices like mobile cell, Digital camera, pacemakers etc. in recent time.

The design of such devices is to consume less and less power to increae more battery life time. But the leakage current is more prominent in the nano CMOS devices. Due to this reason several alternative technologies have been emerged during the last two decades. Some of these new technologies are resonant tunneling diodes (RTD) [3.1-3.4], single electron device (SED) [3.5-3.8],carbon nanotubes [3.9-3.12], rapid single flux quantum (RSFQ) [3.13-3.14],silicon nanowires [3.15-3.18], quantum dot cellular automata (QCA) [3.19-3.22],single electron transistors [3.23-3.26], etc.

These are the beyond CMOS devices for the next generation of electronics. But due to limitation of fabrication technology and restricted operational temperature i.e. below room temperature it has not become popular yet like the conventional silicon transistors. Due to continuous research a novel concept "Spintronics", have been evolved in which properties of electron spin plays a key role for designing and developing the devices [3.27-3.34]. In spintronics,unlike conventional charge based devices the electrons' spins are also manipulated within electronic circuits. These devices along with magnetic materials can be used as simultaneous data storage and processing, while consuming lessenergy. So their application lies on versatile field like high density data storage, microelectronics, magnetic sensors, and quantum computing, biomedical devices and so on.

The process of manipulating the spin degree of freedom of an electron to encode, process and deliver information is called'Spintronics' [3.35-3.45]. The spin of the electron can be read by a sensor. Several spintronics based devices like transistor, diodes, stub tuners, solar cells and filters [3.46-3.52] have already been evolved. Emergence of such

spin based devices has created the beginning of anew area of research with spintronics and spin based quantum information processing [3.53]. Early research in this field was mostly focused on developing

Spin based conventional devices such as spin FET, spin BJT [3.47] etc. But these devices are still not advantageous in terms of power dissipation, since spin plays a minor role than charge [3.54].Recently more promising idea using single electron's spin or' Single Spin Logic' have been published by S. Bandyopadhyay et al [3.55].In this logic classical binary bit '1' and '0' are encode by right (up) and left (down) spin polarization of a single electron confined in a quantum dot and placed in a magnetic field.

The Hamiltonian describing a single electron in a magnetic field is The Hamiltonian describing a single electron in a magnetic field is

$$H = (\vec{p} - q\vec{A})^2 / 2m^* - (g/2)\mu_B \vec{B}.\vec{\sigma} \tag{3.1}$$

where $\vec{A}$ is the vector potential due to the magnetic flux density $\vec{B}$.

μ_B is the Bohr magnetron, g is the Lande g-factor, and $\vec{\sigma}$ is the Pauli spin matrix. If the magnetic field is directed in the z-direction $\vec{B} = B\hat{z}$, then diagonalization of the above Hamiltonian immediately generates two mutually orthogonal eigen pairs[1, 0] and [0, 1] which are the +z and –z-polarized spins, i.e. states whose spin Polarization axes are parallel and anti-parallel to the z-directed magnetic field.

Thus, the spin polarization axis can become a binary variable. The "down" (parallel) spin or "up" (anti-parallel) spin states can encode logic bits0 and 1, respectively. These states are not degenerate in energy, but that is not problematic with encoding logic bits. This idea is different from classical transistors. Classical transistors including Spin FET, Spin BJT switch, 'on' state employ physically movement of charges from source or emitter to another region drain or collector. Thus the energy dissipation occurs which can generate heat as well as noise. But here in the new spintronics concept logic bit '1' is represented by right spin polarization and logic bit '0'by left spin polarization which is stable. In such device logic state can be switched by flipping only the spin which avoids the physical movement of charges as well as energy dissipation.

Some energy would still be dissipated due to degenerated two states,but this could be made minimum by designing the magnetic field arbitrarily small. Here the switching

time is not limited by the movement of charges or electrons. It has also another advantage; it will not be effected with stray electric fields unless strong spin-orbit interaction is associated with the property of the host material. Thus, it is immune to natural noise, unlike charges. Moreover, spin polarization can be a relatively stable entity in a quantum dot. Spin flip times in InP quantum have been observed to be less than 100μs and it is found even longer in organic semiconductor quantum dots made of π -conjugated polymers [3.56-3.59]. The stability of the spin polarization is measured as15 ns at 10 K [3.60] inInAs quantum dots. At room temperature, the spin-flip time is reduced to few tenths ps because of spin-phonon coupling [3.61] at room temperature. Spin flip times of several microseconds have been observed for phosphorus donor atoms in silicon at 20 K [3.62] and spin flip times of more than 100 μs have been measured for InP dots at a temperature of 2 K [3.63].

The power dissipated in spintronics device is of a few tens of nano Watt [3.64] per switching. This device has some other advantages like fast switching times of the order of 1 pico second, bit density can be as high as 10 terabits cm-2, non volatile memory, possible room temperature operation, noise margin can be very high and power delay product can be as lowas~10-20 J

In quantum logic gates spin is preferred to charge for encoding 'qubit' [3.26] due to much longer spin coherence time in semiconductor than charge coherence time [3.36]. Now a day's more advanced level technique is available for controlling and manipulating of an electron spin [3.65-3.69].This has made it possible to implement spintronic devices using 'single spin logic'

circuit with both the combinational and sequential circuits .In recent times spintronic devices have applications in the field like security and control [3.70-3.72], communication system [3.73-3.74], watermark image processing[3.75-3.76], cellular automata [3.77-3.78], RFID field and many other applications [3.79-3.80].

3.2 Literture survey

The idea about 'Spintronics' comes after the invention of field 'magneto electronics' which deals with magnetic or magneto resistive effects for sensing or storing information. The huge breakthrough came in 1980s after the discovery of GMR (Giantmagneto resistance). But the idea of magnetic spin polarized transport was given by Mott in1936 [3.81-3.82]. Mott gave the explanation for the unusual behaviour of the ferromagnetic resistance. He told that at low temperature due to very small magnetic scattering, majority and minority spin electrons with magnetic moment parallel and anti parallel to the magnetization direction of a ferromagnet never mixed in the scattering processes. The conductivity of this material can be expressed as the sum of two different spin projections and hence the current in the ferromagnet is spin polarized. This is also known as the two current models and has been further explained by Campbell et al [3.82] in1967 and Fert and Campbell in 1968 [3.83]. At the same time Esaki [3.84] and Kasua-Yanax [3.85] published that that I-V characteristic of a spintronic device could be modified by an applied magnetic field. In 1969 spin Polarized effect in electron photo emitted from gadolinium is invented by Busch [3.86] et al. Tunneling magnetoresistance concept is published by Jullier`e [3.87] In 1975. It is basically change of resistance of Ferromagnetic/insulator/Ferromagnetic junction when the two magnetisation are the parallel R_{Ap} (↑↑) and antiparallel R_p (↑↓) state.

$$\text{TMR}=\frac{\Delta R}{R}=\frac{R_{Ap}-R_p}{R_{Ap}} \tag{3.2}$$

Where TMR corresponding to tunneling magnetoresistance.

It was shown experimentally by Moodera*et al* in 1988 [3.88] and Hao et al in 1990 [3.89] that when unpolarized current is passed across a ferromagnetic semiconductor it is polarised. After this the first spintronic device spin Field Effect Transistor is invented by Datta and Das in 1990 [3.47]. Spin based Bipolar Junction Transistor (Spin-BJT) is

proposed by Flatt´e et al [3.90] in 2001. Several modification about Spin-BJT came in the year 2003 [3.91] and 2005 [3.92].

In spite of being innovative all these spin based transistor use conventional movement of charges for switching [3..93]. Thus these devices are comparable with conventional charge based transistor as MOSFET [3.94- 3.96] in terms of power consumption.

To reduce power significantly spin based devices must switch states by flipping spins of stationary charges. The revolutionary idea about 'Single Spin Logic' is proposed by S. Bandyopadhyay et al [3.55].In such logic classical binary bit '1' and '0' is encoded by clockwise and anticlockwise spin polarization of a single electron which is confined in a magnetic field as a quantum dot. Various Boolean functions can be realized with this quantum dot. Thus they consume energy and generated heat and noise. Here logic '1' is represented by one spin polarization and logic '0' by opposite spin polarization in a stable spin ½ system .So the logic device can be switched only by flipping the spin without requiring physical movement of charges which is very much energy saving. The power dissipation per switching event could be as low as few tens of nano Watt [3.55]. some other advantages of these devices are like ultra fast switching times of the order of few picosecond, extremely high bit density of nearly 10 terabits cm^{-2}, non volatile memory, possibility of room temperature operation with very high noise margin and very good figure of merit in terms of power delay product (~10-20 J) for switching between the logic states.

The two non degenerate spin electrons parallel and antiparallel with the magnetic field encode the classical bit '0' and '1'. The single state spin configuration is formed by exchanging spin with the nearest neighbour. Signal can flow unidirectionally with the help of a three phase clock [3.97] from input to output stage.

3.3 Theory:

3.3.1 Model: Penta-layered structure

The penta-layered structure of a quantum dot consists of a ferromagnet-insulator-Semiconductor-insulator-ferromagnet combination separated by split metal gates as shown in Fig.3.1(a). The wrap-around split Schottky gate is used for the "writing" and"flipping" operations of the quantum dot.For flipping a bit, the spin polarization

should be rotated by180^0. This is achieved by applying a differential potential between the two halves of the split Schottky gates of the quantity ∇V which allows to modulate the total spin splitting energy ∇ such that it will be resonant with the global ac magnetic field B_{ac} of the quantum dot($\nabla = \hbar\omega$ where ω is the frequency of the ac magnetic field) and If the resonance can be hold for a time duration τ such that

$$\mu_B B_{ac} \tau = h/2 \tag{3.3}$$

Then, it will rotate the spin by 180^0, thereby flipping it.

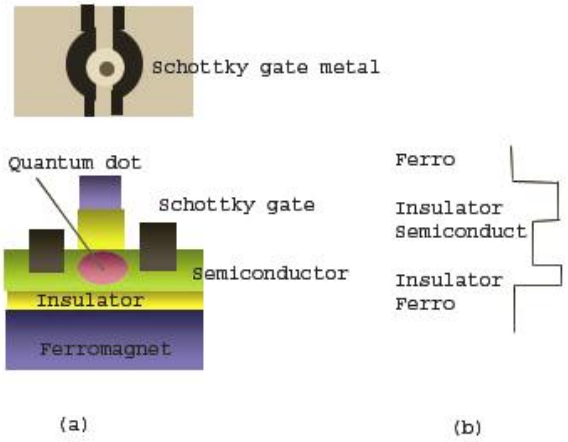


Fig. 3.1 (a) Structure of a gated quantum dot to host a single electron with a well definedspin orientation. The top figure shows the top view and the bottom figure the cross-section.(b) The idealized conduction band energy diagram along the directionperpendicular to the heterointerfaces (at equilibrium).

3.3.2 Read-write technique

To write binary logic bit information in single spin logic, a single electron should be placed as a quantum dot in a magnetic field that will defines the spin quantization axis. The quantum dot will be delineated electrostatically by the wrap-around split Schottky gate in apenta-layered structure consisting of a ferromagnet-insulator-semiconductor-insulator-ferromagnet combination as depicted in Fig. 3.1(a). The wrap-around splitmetal gate is used for the "write" operation. Writing is performed by applying a

positive potential around the wrap-around gate. The applied potential decreases the confinement and hence increases effectively the size of the semiconductor dot. As a result the lower Zeeman level of the dot of the first sub band will be below the Fermi level, while still keeping the higher Zeeman level above the Fermi level. Now from ferromagnet to semiconductor tunnelling effect occurs for a single electron, ferromagnetic layers play a vital role in performing the "reading" and "writing" operations. The conduction band energy diagram of ferromagnet, insulator and semiconductor materials in Fig. 3.1(a) are at equilibrium in the direction normal to the hetero interfaces as shown in Fig. 3.1(b). Since the edge of the conduction band in the dot is above the Fermi level, initially electron can tunnel in the quantum dot. After the application of voltage the conduction band goes below the Fermi level and due to Pauli's Exclusion Principle, tunnelling of a single electron is possible in the dot.This electron's spin is polarized along the desired direction of magnetization of the ferromagnet. Thus, a logic bit is successfully "written". Single spin reading can be performed with a variety of techniques [3.98].The technique stated in ref. [3.99] may be used for electrical detection. This scheme needs the use of ferromagnetic contacts as shown in Fig.3.1 to determine the spin polarization of a target electron.

3.3.3 Basic gate design

Various basic logic gates can be designed by different two dimensional combinations of single electron cells. For implementing logic functions linear array of cells are used. These cells interact only with its nearest cells. A globally weak magnetic field is applied to make the spin polarization of the electronic cell a bi-stable quantity. These cells only interact when they are nearest-neighbors. Due to this interaction any two nearest-neighbor electron cells have antiparallel spin orientations [3.55]. But each cell has a preferred orientation with the help of an external global DC magnetic field. Here the preferred orientation is in upward direction. So any cell will be down ward oriented only either after the interaction with its two nearest-neighbors of upward oriented or by the application of local magnetic field. For wiring linear array of odd number cells are used. The singlet states of the two quantum dot exist when the exchange interaction strength J is larger than the Zeeman spin splitting energy. By this principle any logic

circuits can be realized through appropriate placements of dots [3.55]. These types of designs have been established by exact quantum mechanical calculations by a number of researchers. [3.99-3.101]. Logic bits or information can be propagated from one dot to the next using 3-phase clocking [3.97] unidirectional from the input ports to the output ports. Based on the principle several combinational and sequential logic circuits can be designed as below. In these design "up spin" represents logic bit 1 and "downspin" represents logic bit 0.

NOT gates

For a NOT gate, a linear chain of two electrons (quantum dot) will be required to place in a global magnetic field. This will make a bistable spin polarization. Now due to anti-ferromagnetic properties, array of dots will be arranged in spin 'up' and spin 'down' or vice versa fashion. This ensures that any two of the nearest neighbour electrons have opposite spin. Therefore, if one of the dots can be acted as the input and the other as output, the output will always be the opposite of the input and thus NOT gate will be realised as depicted in Fig.3.3.

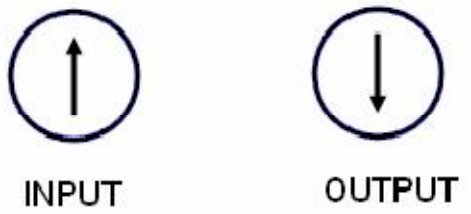


Fig.3.2: Single spin implementation of NOT gate

AND and NAND gates

For two inputs NAND gate a linear array of three cells will be required. The cells will be placed in a global (dc) magnetic field as depicted in Fig.3.3. The two terminal cells can be taken as input port and the middle cell as output port. For both of the inputs being 'spin up' (1) , the output must be spin 'down' (0).If the spin orientation of the two input cells are 'down'(0), then the spin orientation of the output cell must be 'up'. But if one of the inputs is 'up' and the other is 'down', then the output can be in the state between 'up' or 'down' since there two equal possibilities of 'up' and 'down' state. This tie situation can be resolved by applying a global magnetic field in favour of the 'up' spin orientation of

the output. The corresponding spin orientations ensure the truth table of a NAND gate as shown in Fig. 3.3.

The AND gate can be designed from NAND gate by inserting an inverter tothe output of the NAND gate. This requires an additional cell as shown in Fig. 3.4.

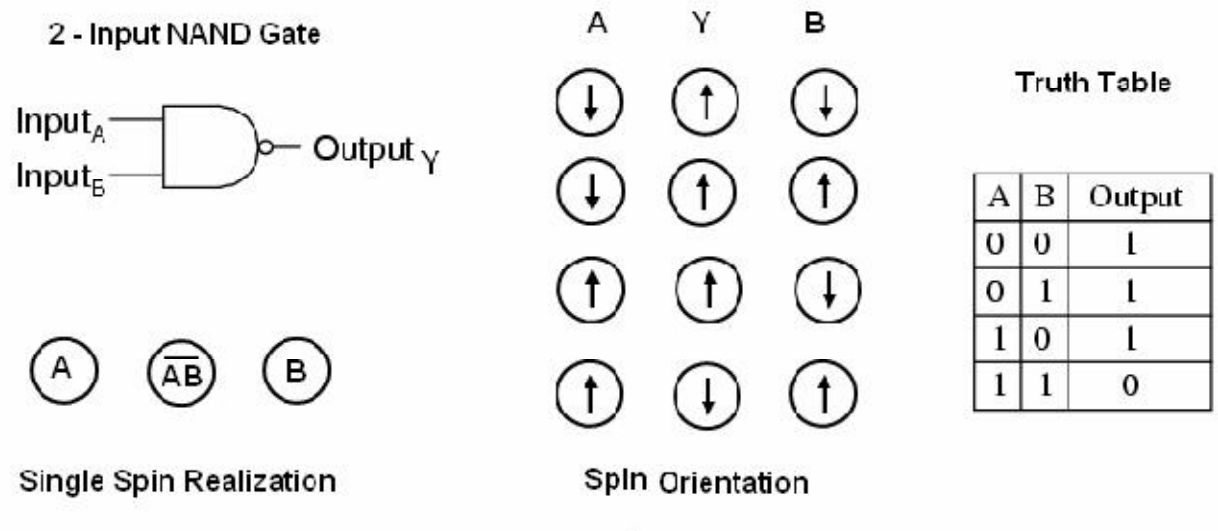


Fig. 3.3: Single spin implementation of NAND gate

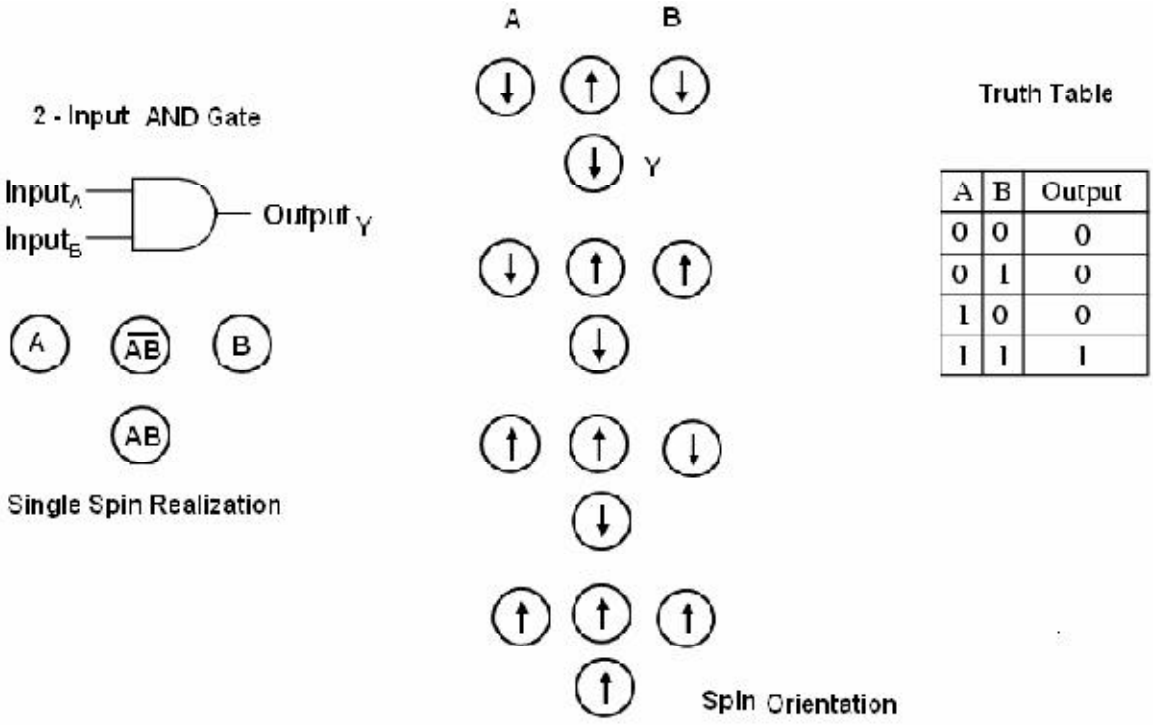


Fig. 3.4: Single spin implementation of AND gate

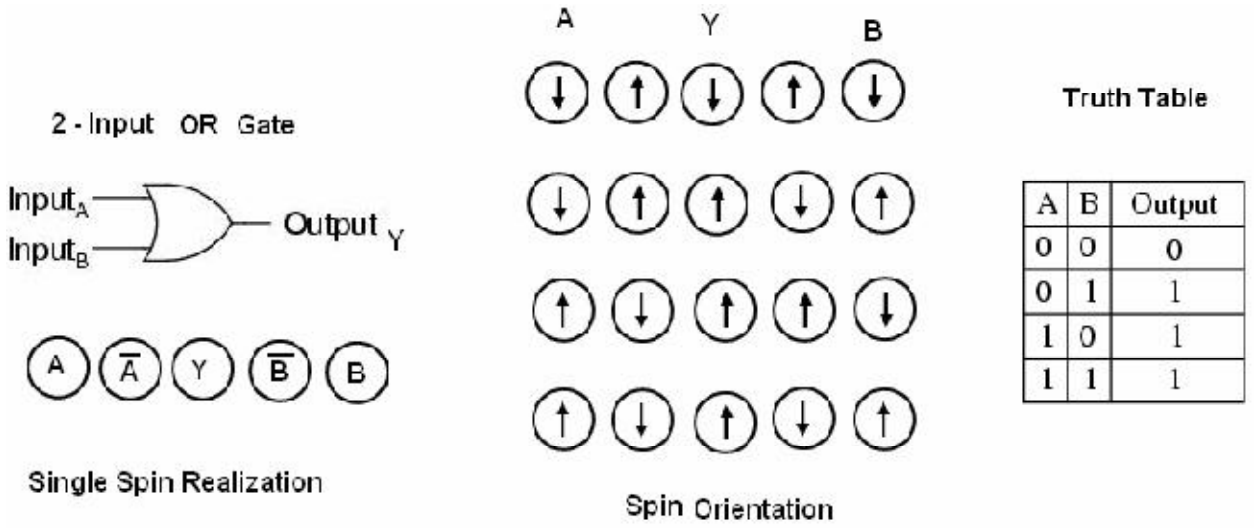
OR and NOR gates

OR gate can be implemented from the universal NAND gate as follows.

By De Morgan's law of Boolean algebra

$\overline{AB} = \overline{A} + \overline{B}$

Where A and B are two binary bits. Therefore from the left hand sideof the equation an OR gate can be realized using NAND gates and inverters asshown in Fig. 3.5 .NOR gate also can be realised by using an extra inverter with the OR gate as in Fig. 3.6.



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 3. 5: Single spin implementation of OR gate

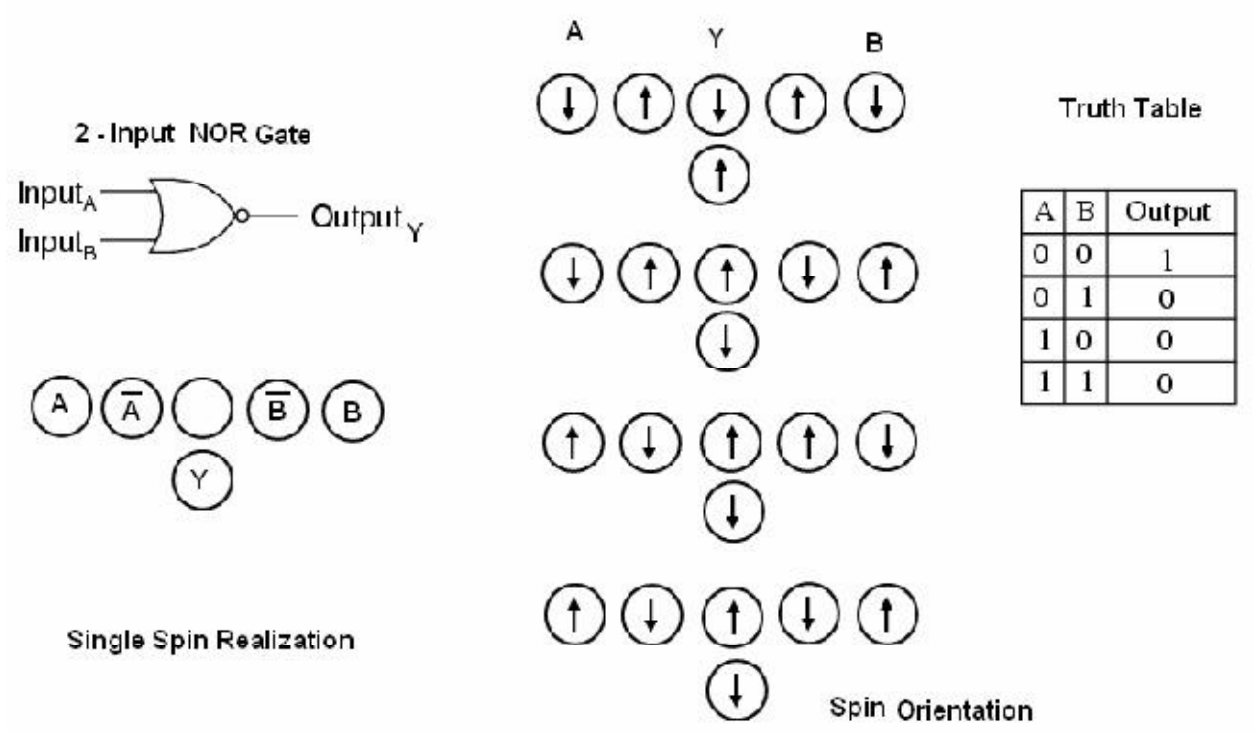


Fig. 3.6: Single spin implementation of NOR gate

3.4 Designing of RFID circuit using Spintronics

3.4.1 Finite State Machine:

Finite State Machine (FSM), is a device that controls functions with the help of simple and accurate design of sequential logic. The idea behind the FSM is that to build up a system such as a machine with electronic controls can only be in a limited (finite) number of states. Finite State Machines also known as Finite State Automation (FSA), at their simplest, are models of the behaviors of a system or a complex object, with a limited number of defined conditions or modes, where mode transitions change with circumstance. Implementation of an FSM involves: (a) states which define behavior and may produce actions, (b) state transitions which are movement from one state to another, (c) rules or conditions which must be met to allow a state transition (d) input events which are either externally or internally generated, which may possibly trigger rules and lead to state transitions. A finite state machine must have an initial state which provides a starting point, and a current state which remembers the product of the last state transition. Received input events act as triggers, which cause an evaluation of some kind of the rules that govern the transitions from the current state to other states. The

best way to visualize a FSM is to think of it as a flow chart or a directed graph of states, there are more accurate abstract modeling techniques that can be used. Many computers and microprocessor chips have, at their hearts, an Finite State Machines the very same design techniques can be used for designing logic circuits or firmware for a microcontroller. In disciplines other than engineering and programming Finite State Machines concepts are used for pattern recognition, artificial intelligence studies, language and behavioural psychology.

3.4.2 RFID:

Radio frequency identification (RFID) systems are an emerging technology to identify a distant object [3.102-3.103]. An RFID system transmits the radio waves containing the unique serial code number of an object wirelessly. Due to its flexibility and ease of operation, RFID technology is conveniently use for automatic operation. It can work without any physical contact or line of sight operation. RFID system can be incorporated with either read only or read/write system. RFID technology ensures high accuracy along with a high level of security [3.102].

RFID system contains of a reader, tag and wireless channel [3.103]. It has a reader consisting of a radio frequency module for two way communication with tags along with a control unit. RFID integrates tags or read the identification information stored in system to detect a remote object by sending radio frequencies which are reflected back and received by the tags together with the information [3.104]. A tag consists of a microchip along with a small antenna and is attached to the object to be located. The microchip contains a unique no. referred to as the Tag ID about the objects it is attached to. The tag of the detected object receives and processes its information on the intercepted signal and then communicate with the sender. Active tags have onboard power supply which have better efficiency with more distant coverage [3.104]. But, the passive tags get power from the received signals transmitted by the master, and they have limited processing capability and a lesser detection range.

Recently bar coding is very much used for automatic identification of an object. Although Barcodes are very cheap, but they can't be reprogrammed along with a limited storage capacity. Magnetic card is also largely used for an object identification. But the

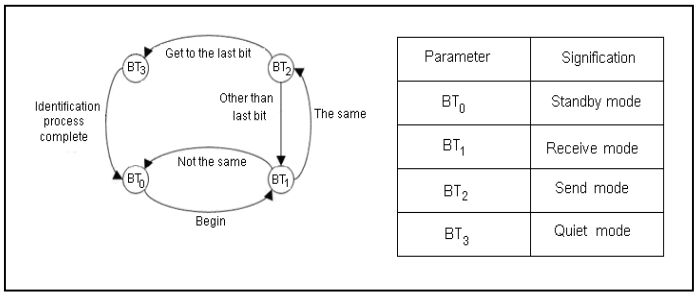
disadvantage associated with it is that it requires physical contact to operate it which is a limitation to target a distant object. To locate a distant object wireless data transfer protocol is required to communicate between card and system which initiates the research of RFID. It is similar to bar code but technologically more advanced. A bar code system consists of a reader and coded labels which are attached to an item, whereas RFID system uses a reader and a tag consisting of a unique serial no. which are attached to the object to be detected. In a RFID system RF signal is used to transfer data through wireless channel from sender to receiver or vice versa. But in barcode system optical signal is used for transferring data and also line of sight is required. RFID technology solves the limitation of barcode system; like, huge amount of data can be stored in a tag, tag is reprogrammable and both way communication is possible between tag and reader, thereby, opening a new era of application.

In view of the above discussion it is clear that the main challenge is to develop a RFID system, which is smaller in size, faster and have low power consumption.These ensure longer working hours between tag and reader of an RFID system. Thus authors are motivated to implement single spin technology based RFID system with ultra low power dissipation so that we can get RFIDs with low tag power but with greater range of operation. For this purpose we shall take the advantage of a popular anti collision protocol (binary tree protocol) scheme.

3.4.3 Anti-collision Binary-tree scheme

Binary Tree Protocol is one of the popular anti-collision protocol [3.105-3.106]. It reduces the average inquiry time by remembering the previous inquiry results. Every tag first completes the enquiring process and then responds to the next reader.

Fig. 3.7 depicts the state diagram of the tag in binary tree scheme. A tag has four states, in which tag will be in one state at one time [3.105].If a tag is neither quit nor killed state then it will shift between sending and receiving state.



Parameter	Signification
BT_0	Standby mode
BT_1	Receive mode
BT_2	Send mode
BT_3	Quiet mode

Fig. 3.7. State diagram of Binary tree scheme

In this protocol, after the identification of the tag it will be eliminated or "killed". Every tag has a unique code number (identification number) and a pointer. This pointer changes accordingly with the ongoing of inquiring tags. In an inquiring process the reader sends an inquiring bit at a time. This bit searches for the tags that has identical bit in it. The matching tag then send their next bit to reader and then the reader sends the remaining bits one by one, while the remaining tags will go to the "quiet" state until one tag has been eliminated and remaining all the tags are reset. When a collision occurs the reader sends a '0' inquiring bit. By this process one tag is identified which is eliminated and other tags are reset followed by a new round of inquiring process. The number of clock cycle required to identify 'n' number of tag is given by,

$$C = 2n\,(t-1) + 3 \qquad (3.4)$$

Where't' denotes the number of inquiring times.

3.5 Implementation

Finite state machine (FSM) is an important module for design of the sequential circuit. The hardware implementation of the FSM consists of a logic block and three latches. The input latch freezes the inputs. The state latch stores the state information. The output latch freezes the outputs. All latches are clocked by the same system clock. The inputs to the logic block are the current state number, fed back via the state latch, and the current inputs that have been frozen by the input latch. The logic block determines the new state number and output pattern as a function of its inputs. The reason the latches are needed is that the logic block, no matter how well designed, will not respond instantly to input

changes. Even worse, when an input changes there is always a risk that the logic block outputs will not change directly to the correct new pattern, but will go through one or more intermediate patterns. Because there is feedback of the state number from the output of the logic block back to its input, if spurious output patterns were allowed back into the inputs the system could become entirely unpredictable.

The FSM implemented here is a dedicated hardware and can only be used for a particular RFID system given in ref. [3.107]. An RFID system typically consists two parts: reader and tags [3.108]. Tags are positive IC chips with unique IDs built in tags, design depends on communication protocols to be used in the system. One popular protocol for this purpose is the binary tree protocol [3.107]. The implementation of this protocol (4-bit ID identification procedure) using spintronic device is shown in Fig. 1. The transition of states is shown in Table 3.1. From the clock cycle 2 to 8, the state changes between T1 and T2, and ends up with T3. This procedure represents successful recognition of a 4-bit ID tag. A 'high' DIFF at clock cycle 13 puts the machine into state T0 which holds until a next 'high' NULL signal arrives.

TABLE 3.1
STATE TRANSITION TABLE

Clock Cycle	State	D1	D2	State transition Condition
1	T2	1	1	DIFF= '0'
2	T1	0	1	NULL= '1'
3	T2	1	1	DIFF= '0'
4	T1	0	1	LSB= '0'
5	T2	1	1	DIFF= '0'
6	T1	0	1	LSB= '0'
7	T2	1	1	DIFF= '0'
8	T3	1	0	LSB= '1'
9	T3	1	0	NULL= '0'
10	T1	0	1	NULL= '1'
11	T2	1	1	DIFF= '0'
12	T1	0	1	LSB= '0'
13	T0	0	0	DIFF= '1'

From the state diagram and the relevant table we have derived the logical expression in a fashion similar to the ref. [3.109]. The implementation of spintronic device based RFID system using binary tree protocol is shown in Fig.3.8. In this scheme, total inquiry process takes 2m(n-1) clock cycles for m tags, where m is the number of tags and n is number of bits. Reader takes 3 additional clock cycles to know that there are no more tags, while inquiring and answering takes (n-1) for each. So total number of required clock pulses is 2m (n-1) + 3. Once it has been entirely finished the tag is killed.

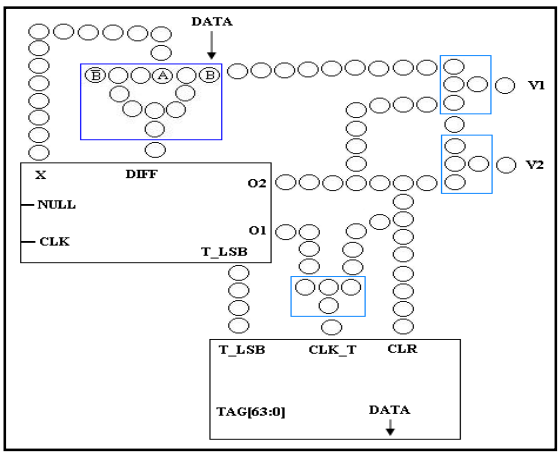


Fig. 3.8. Single spin implementation of binary tree protocol

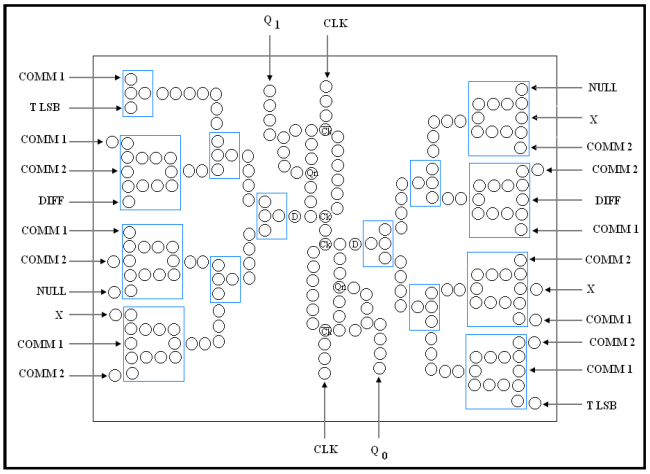


Fig. 3.9. Single spin implementation of state machine in Fig. 3.7

Single spin implementation of the binary tree protocol (the tag end) is shown in Fig. 3.8. For the clarity of the figure the inner circuit is depicted in Figs. 3.9. In table 3.1 the state diagram of the tag's state machine is shown. A tag is shifted between the 'receiving' and

the 'sending' states if it is not at the "quiet" or "killed" state. Fig. 3.10 is the register unit where only one bit can be '1' at any time, making just one of the bits in ID appears at the DATA port of Fig. 3.10. This bit is used for comparing with the receiving inquiring bit.

Different amount of energy is consumed by different tag during the total inquiring process. They also have the equal cost as the operations for them to be recognized remains the same.

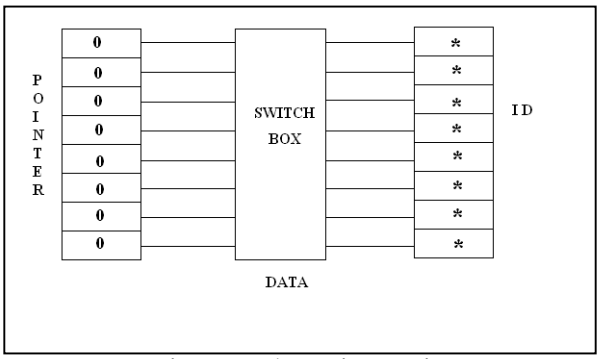


Fig. 3.10. The register unit.

3.6 Operation Principle

Spintronic devices act according to the simple scheme: (i) information is stored (written) into spins as a particular spin orientation (up or down), (ii) the spins, being attached to mobile electrons, carry the information along a wire, and (iii) the information is read at a terminal. Spin orientation of conduction electrons services for relatively long time (nano seconds, compared to tens of femtoseconds during which electron momentum and energy decay), which makes spintronic devices potentially attractive for quantum computing where electron spin would represent a bit (called qubit) of information.

Electron is a small electrically charged body that spins rapidly. Due to spinning of a charged body a magnetic field is generated in a particular direction. In the figure each of circle represents a spin polarized electron confined in a quantum dot. Quantum dots are placed in an externally applied weak magnetic field which is applied to control the

direction of spin of an electron. Nearest neighbor quantum dots are coupled using exchange interaction. Global magnetic field makes polarization in the dots in parallel or antiparallel direction. 'upward' direction may be encode as binary bit '1' and 'down ward' direction may be encode as binary bit '0'. The Spin Polarized Scanning Tunneling Microscope (SPSTM) tips read heads may be used for applying input and getting output from this spintronic device [3.110].

3.7 Results and discussions

Finite State Machine provides an immensely powerful method of implementing sequential (past history dependent) control schemes both in hardware and software. It is a simple and effective artificial intelligence technique for controlling a system and providing the appearance of intelligence. The perceived appearance of intelligence is more important than actual intelligence, and that finite state machines are able to provide this perception. By extending the concept of the FSM and introducing RFID we have designed and implemented spintronics device based Finite state machine as depicted in fig. 3.11. It is observed that the power consumption is significantly lower than the normal CMOS based circuits. Moreover, density of integration of the components is much higher and speed of operation is too high compared to conventional CMOS circuits. In fact the spintronics dream is a seamless integration of electronic, opto-electronic and magneto-electronic multi functionality on a single device that can prefer much more than is possible with today's microelectronic devices. The present work is a tiny effort towards such expectation.

In this present work we have designed RFID system using single electron logic. The present systems are implemented using spintronics device since of their low power consumption, high speed of operation and tinny size. Spintronics device based RFID system has been verified by computer based simulation. Different combinations of simulated signals are fed to the tags so designed. Output of the experiential activities of simulated RFID system are upto the expectation thereby establishing the fact that design is proper. It is sure that present circuit is much faster than the conventional logic circuits and supports very high-density integration. Spin based logic circuits are of course at the

top of the hierarchy. Since these logic circuits (spin based) are classical, rather than quantum mechanical spin coherence is not a concern. Consequently implementing these circuits is far easier than building quantum logic gates employing single electron spin while considerable efforts and research have been conducted in the search for spintronics quantum computers; very little, if any, investment has been made to realize single spin logic. In this respect the present work is an early attempt for spin based digital systems. In order to substantiate our designed spintronic device based RFID system we have made computer simulation

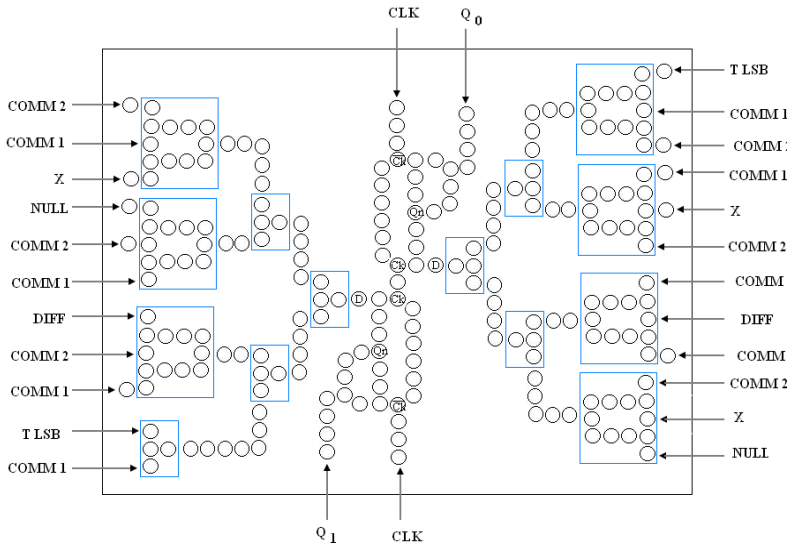


Fig.3.11. Realization of finite state machine by two-dimensional array of spin polarized electron cell (quantam dot)

Comparison of Delay Time

Since switching operation does not associated with any physical charge flow, so there is almost no power dissipation during flipping operations. Actually power dissipation during flipping a single bit can be estimated to be in the order of nano-watt. With a device density of 10^{11} cm^{-2}, we will expect power dissipation in the order of nano Watt [3.111] for an individual gate which is 10^6 times smaller than CMOS/TTL gate(0.01/10-12 mW) [3.112] and 10^3 times smaller than SED gates(~1μW) [3.113].

In InAs quantum dots, spin flip time for a single electron cell has been measured to be about 15 ns at 10K [3.114] which ensure ultra-high speed computing. Propagation

delay time of an individual gate of a spin based device is about 1ps [3.111] which is $12X10^3$ times faster than that of CMOS/TTL gates (12 ns) [3.112] and $6X10^3$ times faster than SED gates (6ns) [3.113]. In room temperature we can expect farther decrease in spin flip time because of spin phonon coupling.

TABLE 3.2
TIME DELAY COMPARISON

Sl. No.	Circuit Name	Propagation Delay time / Gate	Faster (times) with respect to CMOS/TTL
1	CMOS/TTL gates [28]	12 ns	1
2	SED gates [29]	6 ns	2
3	Analyzed SED gates	2 ns	6
4	Spintronics device based gates [19]	1 ps	12000

TABLE 3.3
POWER DISSIPATION COMPARISON

Sl. No.	Circuit Name	Power dissipation / Gate	Consume Power with respect to CMOS/TTL
1	CMOS/TTL gates [28]	0.01 / 10-12 mW	1
2	SED gates [29]	~1μW	10^{-3}

The energy consume by a single quantum dot in a single spin flip can be calculated by Zeeman splitting energy which is $|g\mu_B B|$ [3.114] where μ_B is the Bohr magnetron and B is the flux density of the dc magnetic field. To maintain the antiferromagnetic ordering for the single spin devices this energy must be less than the exchange splitting energy, i.e, $|g\mu_B B| <= 1$ meV as the exchange splitting energy referred in [3.115] is about 1meV. In an InAs quantum dot system the energy dissipation can be calculated by the energy released (or absorbed) when a bit flips which is the energy difference between strong and weak coupling between two consecutive dots.

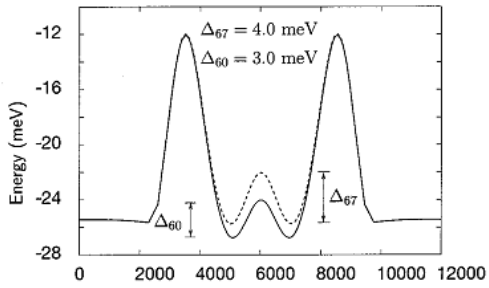


Fig. 3.12. Potential profile for the quantum dot along z in the weak (dashed line), and strong (solid line), coupling regime

Fig.3.12 shows potential profile for a empty double dot in the plane of the heterointerface along Z in the weak coupling V_t=-0.67V and strong coupling V_t=-0.67V.The corresponding interdot barriers Δ_{67} and Δ_{60} , are seen to be 4mV and 3mV respectively. Therefore, the energy dissipated due to transition or flip of logic bit is 1meV=1.61X10^{-22}J.

$|g\mu_B B|$ = 1meV=1.61X10^{-22}J.

Power dissipation/bit flip = E/t = 1.61X10^{-22}/t

t=80ps for InAs and t=200ps for GaAs

Power dissipation/bit flip = E/t =3.0125 PW

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STRAINTRONICS: DESIGNING OF UNIVERSAL GATES (NAND) USING BI-AXIAL ANISOTROPY PROPERTY OF TERFENOL-D

4.1. Introduction:

Low dimensional transistors can operate faster, dissipate less energy and low cost for manufacturing. Down scaling of transistors in ICs make possible to design the devices with nm region gate lengths.However as minimum feature sizes in CMOS scale below 65 nm along with the increase of system frequencies, the static and dynamic power management reduction technique becomes more vital in digital design. In low dimension device the active power is less due to smaller parasitic capacitances in these devices [4.1]. But the leakage power is more prominent at this stage [4.2]. In fact, below 22 nm CMOS scales, managing of standby power dissipation due to various sources of leakage like drain induced barrier lowering (DIBL), weak inversion current, gate tunnelling, gate induced drain leakage (GIDL), , hot carrier effect etc. becomes a great concern in digital circuits. Further, power supply does not scale proportionately with the advancement of new technology [4.2]. Therefore, the increased ratio of supply voltage to channel length in new technology leads to more leakage power dissipation [4.3]. Thus, IC's are facing increased active power dissipation due to growing leakage in new miniature size[4.4]. It is more prominent in low speed [MHz] biomedical devices and environmental sensors [4.5]. Another problem associated with low dimension technologies are high power density of the systems [4.6], which necessitates expensive temperature control packaging of the chips. Finally, the law of Physics will prevent the further miniaturisation of CMOS devices beyond 10 nm [4.7]. In order to maintain the integration density according to Moore's Law and supply the demands of modern digital technologies, the CMOS devices must come in (3-D) chips. Again, there is a possibility of thermal failures for fine-grained 3-D integration due to high leakage power in CMOS devices.[4.8,4.9].There is a need to search alternate technologies for industry to keep up pace with Moore's law [4.10].

This has led to some of the novel design technique of existing CMOS device& circuit in the sub-45 nm CMOS technologies [4.11-4.15].They are like (a) tunnelling FET, (b)

FET with high-K gate dielectrics, (c) FINFET, (d) FET with wraparound (Omega) gates, (e) multi-threshold transistors (MTCMOS), as well as novel architectural techniques like (f) pipelining of circuit blocks for reduced power supply operation, (g) clock gating to reduce clock voltage, and (h) dynamic voltage and frequency scaling (DVFS). However, these alternatives have their limitation to replace the CMOS devices & circuitry as the technology reaches its end of the road.

This has geared the researchers for developing ultra low power switching devices. Another equally strong motivation is the need for elevating extremely energy efficient computing devices to be used in application such as medically implanted processors and distributed remote sensing systems where energy is a payoff. For this reason the electronics industry is looking for new generation devices with unprecedented energy efficiency, which can be used to replace or concurrently with the traditional technology. As a result of this, researchers have been working on various novel device concepts that are incapable to replace charge based CMOS transistors with different physical parameters like electron's spin (magnetism) etc. Recently One such device concept is emerged, where a bi-stable single domain nanomagnet's magnetization orientation can encode a bit of logic as 0 and 1[4.16, 4.17].

This chapter describes research towards the understanding of straintonics multiferroic nano-magnetic based universal Logic gates(NAND), which can process logical information as well as can be used as basic memory elements, while dissipating ultra low energy (2-3 orders of magnitude less than the modern CMOS transistors). The Straintonics based devices are based on: (i) mechanical strain is produced through an applied input voltage at the bottom piezoelectric layer and is transferred to the magnetostrictive layer which rotates the magnetization to the desired angle due to the magneto elastic coupling and (ii) Dipole-coupling) interaction between neighbouring single domain nanomagnet that is yield to propagate unidirectional information and perform desired logic operation. In this section, we will discuss on history of traditional semiconductor devices and another view of magnetism and nano-

magnetic logic in order to instigate the need for such straintonics based logic devices.

4.2. Literature Review

J. Barden, W. Brattain and W. Shockley, invented the first transistor in 1947 and in 1956, they were awarded the 'Nobel Prize' for this great invention that has revolutionized the world and the Electronics industry. The preceded three terminal vacuum tube devices was rapidly replaced by the transistor, which had the disadvantages of large size, slow start up and high power dissipation. By progress on of the IC technology and to keep pace with the Moore's law the number of transistors per unit area has been increased at a predicted rate (doubled in every two years).

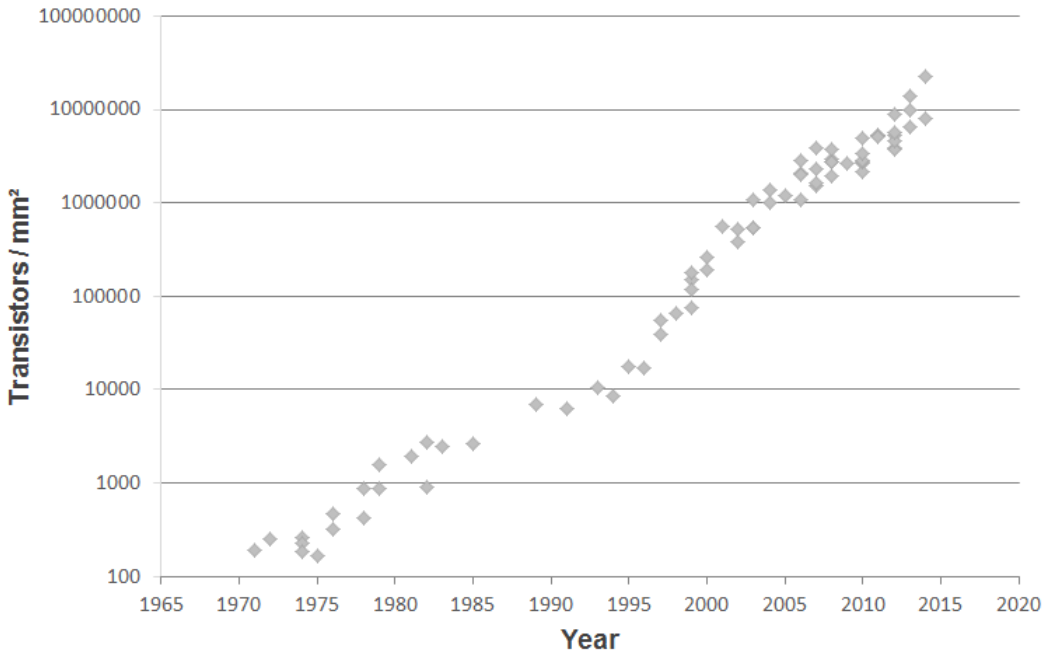


Fig 4.1.The exponential increasing of transistors density on IC based on the Moore's Law [4.18].

When G. Moore made his prediction, there was roughly 32 number of transistors present in a single chip and now a single chip contains approximately half a billion transistors (figure 4.1). This phenomenal growth is possible only due to the technology enabling the miniaturisation of individual transistors. The downscaling of MOSFETs has modernised the electronics industry and has also enabled the practical realization of the complex system on chip we use it at present.

Although the history of semiconductor devices originated as early as from the 1920s, the massive development has occurred after 1960safter the invention of CMOS IC [4.19-4.21]. The fabrication of both n-MOS and *p*-MOS transistors on the same wafer was an important stage in revolutionizing the integrated circuit.

CMOS circuits provide fast switching speed, large density of integration, and very low static power dissipation. These advantages mobilise the miniaturization of MOSFETs with very fast high density integrated circuits.

The next important evolution of MOSFET design is the use of the self-aligned polycrystalline-silicon (poly) gate in the early 80's. The self-alignment of the source and drain to the gate minimizes stray capacitance which provides less signal propagation delay, $\tau = CV/I$ and overall improvement of circuit performance.

Moreover polycrystalline-silicon is a stable and completely compatible material with Silicon technology [4.22]. Polysilicon has properties which match the necessary requirements as a gate material to have an acceptable subthreshold voltage.

As MOSFET channel lengths shrink to sub-micron dimensions the device performance falls due to the high electric field in the channel. This had led to the introduction of lightly doped drain (LDD) MOSFETs in the late70's [4.23]. The lightly doped *n*- region minimizes the electric field and reduces hot carrier injection in the oxide [4.24-4.25].

With the reduction of drain voltages the effect of LDD design subsides. After this heavily doped but very narrow source and drain extensions were introduced to minimize short channel effects without any problems associated with high series resistance [4.26].

Another key direction in the evolution of CMOS design is channel engineering. In this research, various doping schemes have been invented in the history of CMOS technology development. Among these only the retrograde and the halo channel doping are adopted in the deep submicron MOSFETs designs technology.

According to scaling rule, the channel doping increases $k\alpha$ times in every advanced technology generation, to minimize short channel effects. However on the other hand this degrades carrier mobility severely.

The traditional channel doping scheme is not applicable in 100 nm channel length MOSFETs due to short channel effect associated with it. For better device performance in this nano channel length the super steep retrograde (SSR) channel

doping scheme was proposed in early 90's in [4.27]. SSR doping technique enhances current drive by increasing carrier mobility and reducing threshold voltage *VT* [4.28].

For below 100 nm channel length transistors the SSR alone is insufficient to control the short channel effect. To minimise this problem the halo (pocket) doping and the supper halo doping [4.29] were introduced.

50 nm gate length of MOSFETs are possible with 90 nm technology node [4.30] and 25 nm gate length MOSFETs can be produced with 65 nm technology node [4.31]. It has lower subthreshold voltage and a higher drive current (*Ion* = 840 μ A/ μ m). Such 25 nm transistors are able to bear the performance required by the ITRS. In addition to this technological advancement the use of strained silicon based channel to enhance carrier mobility, and introduction of high dielectric materials in place of silicon dioxide as an insulator will improve the performance of the conventional MOSFETs by which researcher can think of beyond the present technology node available.

Apart from the 25 nm gate length MOSFET, researcher have also demonstrated of smaller gate length devices like gate lengths 15 nm [4.32], and 16 nm [4.33], which are designed by hp 45 nm technology node; 14 nm [4.34] by hp32 nm and 6 nm [4.35], 8 nm [4.36] and 10 nm [4.37] are designed by the hp22 nm technology node. All these have been fabricated and reported, delivering promising device performance.

There are, however, continuous demands from the industry and research communities alike, that beyond the 45 nm technology nodes, scaling is challenged by some fundamental limitations like quantum mechanical effects like tunnelling of carriers, the randomness of discrete doping, and excessive power dissipation etc. These have acted as stimulating force to the researcher to change the traditional MOSFETs with some new design concept. As a result some novel device architecture like multiple gate FETs, silicon on insulator (SOI), silicon on nothing (SON) , single electron transistor (SET), Spintronics , straintronics etc. have been evolved.

There is a Buried oxide layer (BOX) under the Si active layer in SOI MOSFET. BOX can act as a blocking layer to minimize the fringing field effect. In this way various

Short channel effects (SCE) like parasitic capacitances, hot carrier effect, self-heating effects (SHE) etc. can be well alleviated [4.38]. However ultra thin Si film is very challenging to achieve as well as it suffers from high S/D resistance. In a SON MOSFET, air is replaced in BOX layer with air for which better threshold voltage roll off and less sub threshold slope can be achieved [4.39]. However accurate current voltage model for SOI/SON technology is still awaited to analyse device ckt. Simulation precisely.

SET's are promising due to their ultra low power and small feature capabilities. But the disadvantages associated with it is low power ability to drive current, low voltage gain, high output impedance and highly prone to affect with background charges. CMOS devices along with SET can constitute hybrid SET-CMOS circuit can eliminate most of these problems.[4.40]

Through continuous research works another group of devices called spintronics have been evolved in the area of low dimentional & low power electronics [4.41]. In traditional charge based devices power dissipation is inversely varies with the switching time. So faster switching dissipates more energy. But in spintronics direction of bistable electron's spin is controlled by a magnetic field. So, here switching means only flipping of electron's spin which eliminates the current induced power dissipation [4.42]. Moreover due to definite direction of magnetic field spintronics devices can be controlled more easily than any charge based devices. But in spintronics a single electron spin is very unstable at room temperature.

This leads to new area of technology like multi spin, straintronics, multiferroics based nanomagnetic logic etc.

4.4. Nano-Magnet

A nanomagnet is a sub micrometric system that exhibits natural magnetic order without any external magnetic field. The small dimension of nanomagnets inhibits the formation of multi-magnetic domains. Below the critical size (~ 100nm) the nanomagnet behaves as a single domain magnet, i.e. the magnitude and direction of magnetization remains uniform throughout the region.

It can be proved from basic physics that for switching a transistor, minimum energy dissipated at a temperature T is NkTln(1/p)[4.16] which is independent of the switching speed. Here Nis the number of information carriers (electrons) in the transistor, k is the Boltzmann constant, and p is the bit error probability. On the contrary the minimum energy dissipated during switching a single domain magnet's magnetization is ~ kTln(1/p) [4.43-4.44]. This reason behind it is that information carriers in a single domain nanomagnet are electron spin (instead of electron charge in a traditional transistor)whose mutual coupling due to the exchange interaction ensures that they rotate in unison like a giant single spin [4.44-4.45]during switching the magnetization. Thus for the same number of information carriers and for the same bit error probability, a transistor will dissipate N times (N≫1) more energy than a magnet So magnet based logic switch becomes intrinsically much more power-efficient than the transistor based switch. Actually it is due to the exchange interaction between spins which is not existed between charges and gives the magnet this advantage. Thus, nanomagnet-based computing has two major advantages over traditional electronics -

(i) Magnets are intrinsically less energy dissipative than transistors.

(ii) Unlike transistors, magnets have no leakage ct. and hence avoid standby power dissipation.

4.4.1: Multiferroics nanomagnet: Straintonics based switching:

Recently, for switching a magnet, a superior energy efficient scheme has been proposed. Here magnetostrictive layer of a multiferroics nanomagnet (Terfenol-D) elastically coupled with the piezoelectric layer (PZT) as shown in Fig.4.2 , can be switched by applying a very low voltage of few mV to the piezoelectric layer [4.46-4.47].

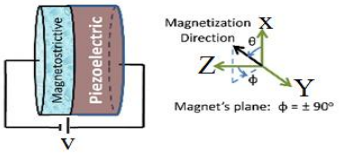


Fig.4.2: piezoelectric- magnetostrictive based straintonics.

This voltage produces Uniaxial strain to the piezoelectric layer and is shifted completely to the much thinner (at least one-fourth) magnetostrictive layer through elastic coupling. This can be achieved uniaxially either by an electric field applied along the direction of expansion or contraction (d_{33} coupling), or by mechanically clamping the multiferroics in one direction and by producing expansion or contraction in perpendicular direction through d_{31} coupling when input voltage is applied across piezoelectric layer. The substrate material is too soft to allow uniaxial expansion or contraction. The uniaxially strain will cause to switch the magnetization to obtain the desired state. In this scheme, energy dissipation occurs about few hundred KT with a delay of 1ns [4.47- 4.48]. This directs it as one of the most energy efficient magnet switching scheme and belongs to within the purview of straintonics.

Although a lot of research publication has been obtained recently, most of them are focused on the conceptual single magnet flipping. In the line to exploit straintonics in universal ICs, piezoelectric materials need to be incorporated with the MTJ structure.

A Magneto tunneling junction (MTJ) structures is compiled of two layers of a ferromagnetic material (a fixed or hard layer and a free or soft layer) separated by a very thin nonconductive tunneling (MgO, Al_2O_3, etc.) barrier. The high and low value of MTJ resistance depends on the magnetization directions of the soft and hard ferromagnetic layers. In MTJ the transport of electrons occurs by spin-dependent tunneling within the majority and minority spin states. For the parallel spin orientations, applying a input voltage across the MTJ causes tunnelling of electrons through the thin barrier with less scattered, resulting a low resistance (R_P) state. In contrast, for the antiparallel spin orientation the resistance is in high (R_{AP}) state. The resistance change is determined by a TMR ratio, which is defined as $\Delta R/R = (R_{AP} - R_P)/R_P$. With the MgO oxide barrier, 500% TMR ratio could be achieved at room temperature and 1000% at 5^0 K [4.48]. TMR ratios between 50% and 150% are found in most of the practical devices. The write operation can be performed by flipping the direction of magnetization of the free layer (the fixed layer cannot be changed) with a suitably applied voltage.

4.4.2: Single domain nanomagnet:

The formation of single domains& multi domains in a magnetic disk is shown in Fig 4.3(a). By reducing the size of the magnetic structure, the probability of realisation of

a single domain magnetic state would be increased due to strong exchange coupling which forces the spins to point in the uni-direction. This occurs typically when the dimensions of a nanomagnet reduces to the size of hundred nanometers or less. In this state magnet can be behaved as a single domain nanomagnet and it has a single well magnitude that equals the saturation magnetization of the ferromagnetic material. The corresponding schematic of a single domain nanomagnet is shown in fig.4.4.

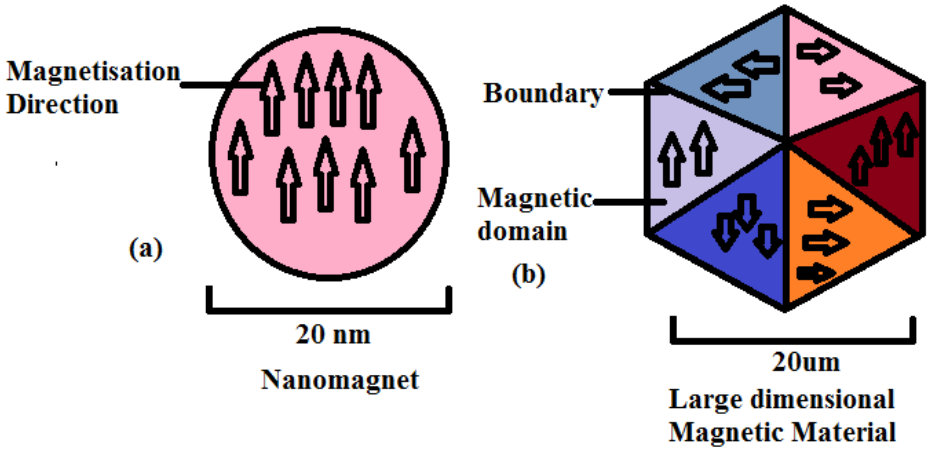


Fig.4.3(a)-(b). Single domain nanomagnet& multiple domain magnet.

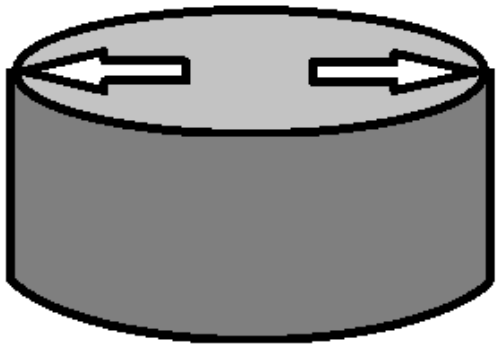


Fig.4.4: single domain nanomagnet indicating bistable direction (easy axis).

For a single domain nanomagnet, the magnetization direction strongly depends on the shape of the nanomagnet. In other sense, a single domain nanomagnet shape plays an important role in the rotation of its magnetization vector to strain and field. This property is called shape anisotropy energy and the ferromagnet always tries to orient themselves in the direction of minimum demagnetizing field. For a circular

shape single domain nanomagnet, its magnetization vector is free to settle in any direction due to absence of any energy barrier for different in-plane magnetization orientations. As a result, its magnetization vector can rotate and settle at any angle in response to a small applied field or stress. However, the same is different for the elliptical shape structures. The elliptical shape nanomagnet prefers to settle magnetization vector along the direction of minimum energy state called "easy axis". Thus for an ellipse, the preferred "easy axis" (left/right state) can encode thelogic"0" or "1" state. The up/down direction is known as the hard axis and an in-plane energy barrier prevents spontaneous switching between the logic low and high states (Fig.4.4).

4.4.3: Propagation of logic bit: The multiferroics nanomagnet wires:

To propagate a bit of information from one magnet to another, a chain of nanomagnet is required. By designing a chain of single domain nanomagnet after a input magnet, a nonmagnetic wire can be implemented. Here the information can propagate through the wire by applying stress at the piezoelectric layer, which causes to remove the energy barrier and subsequently point along their hard axis. Now the magnet settles to the desired stable position after the withdrawal of stress under the influence of the dipole field coupling.

If magnets are arranged so that the joining line with their centers coincides with hard axes, their magnetizations form an anti-ferromagnetic arrangement. If the easy axes coincide with the line joining the centre of then nanomagnets, their magnetizations prefer to orient parallel to each other. Through this operation, the magnetization state of the input nanomagnet can propagates to the output nanomagnet at the end of the chain as shown in fig 4.5.

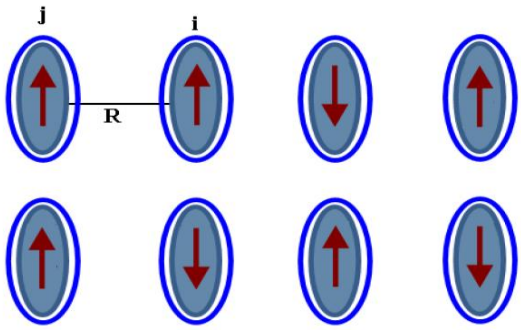


Fig. 4.5.multiferroic nanomagnetic wires chain.

4.4.4: Fundamental concepts about Magnetic parameters:

Some important parameters that indicate the magnetic behavior are [4.49]:

1. The magnetization *M*, defined as the combination of magnetic moments divided by thevolume(V) of magnetic structure:

$$\vec{M} = \frac{\sum m}{V} \tag{4.1}$$

Wherem is magnetic moment and the magnetization (M) in the SI units is A/m.

2. The magnetic susceptibility χ is the magnetization divided by the absolute value of the magnetic field:

$$\chi = \frac{\left|\vec{M}\right|}{\left|\vec{H}\right|} \tag{4.2}$$

The susceptibility is a rank 2 tensor for general magnetic materials.

4. In the spontaneous magnetic material, the Curie temperatures are the highest temperatures at which the magnetization order is still maintained. These are denoted by the Curie temperature T_C and the Neel temperature (T_N) for Ferromagnets and anti ferromagnets including ferrimagnets.

4. The magnetic permeability μ defined as:

$$\mu = \frac{\left|\vec{B}\right|}{\left|\vec{H}\right|} \tag{4.3}$$

Where *B*is the magnetic induction or magnetic flux density or simply *B*field;His measured in Henry per meter (SI) and H is the magnetic field. The magnetic induction in matter depends on the magnetic field intensity *H*and the magnetization *M*, and is given by:

$$\vec{B} = \mu_0(\vec{H} + \vec{M}) \tag{4.4}$$

Where, $\mu_0 = 4\pi \times 10^{-7} (H/m)$ is the permeability in vacuum.

4.4.5. Magnetic Energy

4.4.5.1: Exchange coupling energy

The exchange coupling energy is the interaction responsible for the establishment of magnetic order in magnetic materials. This interaction originates from a quantum effect. The exchange interaction between two spins Si and S_j can be described by the Hamiltonian [4.50].

$$H = -2\xi \vec{S}_i . \vec{S}_j \tag{4.5}$$

Where ξ is the exchange constant, which measures the intensity of this interaction. This is known as the Heisenberg Hamiltonian, and is mostly used for the analysis of many magnetic properties of materials.

The exchange energy can also be written as:

$$E_{ex} = -2\xi \vec{S}_i . \vec{S}_j = -2\xi S^2 \vec{m}_i . \vec{m}_j \tag{4.6}$$

Where the reduced magnetization can be defined as:

$$\vec{m} = \frac{\vec{M}}{\left|\vec{M}\right|} = \frac{\vec{M}}{M_S} \tag{4.7}$$

M_s,is the maximum saturation magnetization and "m" is cosine direction of magnetization vector and $|m| = 1$

If the angle between the two spins or moments of i and j is $\Delta\theta_{i,j}, \left|\Delta\theta_{i,j}\right|$ or $\left|\vec{m}_i, \vec{m}_j\right|$

Therefore, for small $\Delta\theta_{i,j}, \left|\Delta\theta_{i,j}\right|, \left|\vec{m}_i - \vec{m}_j\right|$considering that one can introduce a continuous function *m*, such that $\vec{m}$ is developed around $\vec{r}_j$, the vector of lattice site j as:

$$\vec{m}_j - \vec{m}_i = (r_j . \Delta) m \tag{4.8}$$

Where Δ is the gradient operator and

$$r_j = x_j \hat{\imath} + y_j \hat{\jmath} + z_j \hat{k} \tag{4.9}$$

Therefore, from equation (2.3)

$$E_{ex} = -2\xi S^2 Cos(\Delta\theta) \cong \xi S^2 (\Delta\theta)^2 \tag{4.10}$$

By replacing equation 4.5 in equation 4.7, we have

$$E_{ex} = -\xi S^2 ((\vec{r}_j . \Delta) m)^2 = \xi S^2 [(\vec{r}_j . \vec{\Delta} m_x)^2 + (\vec{r}_j . \vec{\Delta} m_y)^2 + (\vec{r}_j . \vec{\Delta} m_z)^2] \tag{4.11}$$

The equation (4.8) is the exchange energy part of the total energy. One must integrate or sum overj and divide by two to avoid counting the contribution of the pairs of spins twice. In materials with cubic symmetry, the sum of the products of the coordinates of $\vec{r}$ is zero and $\sum_j x_j^{\,2} = \frac{1}{3}\sum_j r_j^{\,2}$ (4.12)

The exchange energy per unit volume can be calculated by dividing eqn. (4.12)by Volume V. In this case $\sum_j r_j^{\,2} = 6a^2$ and we have:

$$\frac{E_{ex}}{V} = \frac{\xi S^2}{a}[(\Delta m_x)^2 + (\Delta m_y)^2 + (\Delta m_z)^2] \quad (4.13)$$

The coefficient in equation (4.10) is the exchange stiffness constant A which varies with the exchange constant ξ and measured in $\frac{J}{m}$

$$A = \frac{n\xi S^2}{a} \quad (4.14)$$

n =1 for a simple cubic lattice, 2 for a bcc lattice and 4 for afcc lattice.

NOTE: This stiffness term is not used in most simulations in this thesis as we assume that for small volumes (~100 nm × 100 nm × 10) considering the strong exchange coupling the spins switch coherently.

4.4.5.2: Magnetostatic shape energy:

The magneto static shape energy is the total magnetic energy of a matter in its own magnetic field.This field is the demagnetization field *dH* . The magnetic field can be taken as that the divergence of the total magnetic induction is zero. Maxwell's equation states that

$$\Delta.\vec{B} = \Delta.\mu_0(\vec{H} + \vec{M}) = 0 \quad (4.15)$$

Therefore [26]:

$$\Delta.\vec{H}_d = -\Delta.\vec{M} \quad (4.16)$$

The magnetostatic energy E_{ms}, indicates the magnetization energy in the demagnetizing field is:

$$E_{ms} = -\frac{1}{2}\mu_0 \oint_V \vec{H}_d.\vec{M}.dv \quad (4.17)$$

Where the integral is performed over V, the volume of the sample. The factor ½ comes due to the fact that this magnetic self-energy arises from the integration of the magnetization with the creating magnetic field.

The magnetostatic energy of ellipsoid shapemagnet is easy to calculate [4.25] as the magnetic field is equal at every point of a magnet. The demagnetizing field is $\vec{H}_d$

$$\vec{H}_d = -N_d \vec{M} \tag{4.18}$$

Where $N_d$is the shape dependent demagnetizing factor. It should be noted that if thenanomagnets have a non-ellipsoidal shape, the demagnetizing field varies across the volume. The magnetostatic energy of an ellipsoid nanomagnetcan be calculated by equation 2.15, with the demagnetizing factors N_i and the components of magnetization M_j along the axes a, b and c is :

$$E_{ms} = -\frac{1}{2}\mu_0 V(N_a {M_a}^2 + N_b {M_b}^2 + N_c {M_c}^2) \tag{4.19}$$

Where $N_a + N_b + N_c = 1$ (4.20)

And a, b and c refer to X, Y and Z direction in the Cartesian coordinate system.

The equation (4.17) can be simplified in the case of ellipsoid to:

$$E_{ms} = -\frac{1}{2}\mu_0 {M_s}^2 V(N_x {m_x}^2 + N_y {m_y}^2 + N_z {m_z}^2) \tag{4.21}$$

Where :

$${m_x}^2 + {m_y}^2 + {m_z}^2 = 1 \tag{4.22}$$

Therefore, we can take normal magnetization with respect to azimutal and polar angle with M_s to simplify equation (4.21) .The fig. 4.2 shows the multi ferroic nanomagnet being considered.

Fig 4.2 depicts the magnetization direction in Cartesian coordinate system. In this work, we consider the magnetostrictive diameters are, a and **b** and its thickness is l.

The demagnetization factors are:

$$N_x = \frac{\pi}{4}\left(\frac{l}{a}\right)\left[1 - \frac{1}{4}\left(\frac{(a-b)}{a}\right) - \frac{3}{16}\left(\frac{(a-b)}{a}\right)^2\right]$$

$$N_y = \frac{\pi}{4}\left(\frac{l}{a}\right)\left[1 + \frac{5}{4}\left(\frac{(a-b)}{a}\right) + \frac{21}{16}\left(\frac{(a-b)}{a}\right)^2\right] \tag{4.23}$$

$$N_z = \frac{\pi}{4}\left(\frac{l}{a}\right)\left[2 + \left(\frac{(a-b)}{a}\right) + \frac{18}{16}\left(\frac{(a-b)}{a}\right)^2\right]$$

The equation 4.21 (for the nanomagnet in Fig 4.2) can be written as:

$$E_{ms} = -\frac{1}{2}\mu_0 V M_s^{\,2}(N_x(Sin(\theta)Cos(\varphi))^2 + N_y(Sin(\theta)Sin(\varphi))^2 + N_z(Cos(\theta))^2 \quad \text{---(4.24)}$$

Where the Nx, Ny and Nz are given by equation 4.24.

The equation 4.24 represents magnetostatic energy of a single-domain nanomagnet

4.4.5.3: UniaxialMagneto crystalline anisotropy energy (E_u):

This is the energy which acts jointly with the shape anisotropy energy to rotate the magnet in the easy axis direction without any stress. The uniaxial Magneto crystalline anisotropy energy E_u can be defined as, $E_u = K_u \sin^2\theta\ V$ .Where K_u is the uniaxial anisotropy coefficient, V is the volume of the nanomagnet. The E_u and E_{sh} creates an energy barrier where maximum energy occurs along the minor axis ($\theta=\pi/2$) and minimum energy occurs along the major axis ($\theta=0, \pi$).

4.4.5.4: Magnetostatic Magnetoelastic energy (stress anisotropy)

The magnetoelastic energy of a magnetostrictive material has an improvement originating from the interaction between the magnetization and the strain $\alpha_i\alpha_j$ or mechanical stress σ. The magnetoelastic energy is the increase in anisotropy energy of a magnetic solid subjected to a stress.

Its expression for a cubic crystal is given by [4.47]:

$$E_{me} = \oint\left[C_1\left(\alpha_1^{\,2}\varepsilon_{xx} + \alpha_2^{\,2}\varepsilon_{yy} + \alpha_3^{\,2}\varepsilon_{zz}\right) + C_2\left(\alpha_1\alpha_2\varepsilon_{xy} + \alpha_2\alpha_3\varepsilon_{yz} + \alpha_3\alpha_1\varepsilon_{zx}\right)\right]dV \text{.....(3.25)}$$

The C-factors are the magneto elastic coupling constants and $\alpha_i\alpha_j$ are the direction cosines.

Magnetostriction is the change in dimensions of a solid when subjected to a change in its magneticstate. It is measured by the relative linear deformation (strain):

$$\varepsilon = \frac{\delta d}{d_0} \qquad (4.26)$$

Where $\delta d = d - d_0$ is the change in linear dimension of the solid due to change in magnetization.

The saturation magnetostriction λ_s is related to the strain generated when the magnetization is changed from saturation magnetization in a perpendicular direction

to saturation magnetization along a given direction. In the case of stress, the stress anisotropy energy $E_{me}$is given by:

$$E_{me} = \int_v \frac{3}{2}\lambda_s \sigma \alpha_i dV \tag{4.27}$$

The σ_i is defined as cosine direction of the applied stress.

4.4.5.5: Dipole coupling energy

Consider Fig.4.5, with two adjacent multiferroic elements in the chain labelled as the and *ith and jth* element.

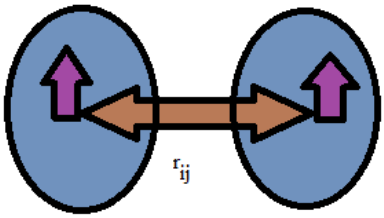


Fig4.6: a dipole-coupled nanomagnet with r_{ij} separation between them. These magnets have magnetizations that subtend polar and azimutal angles of θ_i, ϕ_i and θ_j, ϕ_j respectively, with the positive Z direction and direction of the X-Y plane.

The dipole-dipole interaction energy is [4.47]:

$$E_{dipole-dipole}^{i-j} = \frac{\mu_0 M_s{}^2 V_i V_j}{4\pi \left|\vec{r}_{i-j}\right|^3}\left[\left(\vec{m}_i(t)\vec{m}_j(t)\right) - \frac{3}{\left|\vec{r}_{i-j}\right|^2}\left(\vec{m}_i(t).\vec{r}_{i-j}\right)\left(\vec{m}_j(t).\vec{r}_{i-j}\right)\right] \tag{4.28}$$

Where $\vec{r}_{i-j}$ the vector is distance between the ith and jth magnet and $\vec{m}_i$ is the magnetization of the i_{th} magnet.

4.4. Implementation of universal gates (NAND) with biaxial anisotropy

Nanomagnet with uniaxial anisotropy can exhibit two state, while magnet with biaxial anisotropy can produce four state. By these four states two NAND gates can be characterized which can be utilized for high dense non-Boolean computing applications. Such applications include designing "associative" memory for image reconstruction and pattern recognition and implementation of 4-state nanomagnetic neurons for neuromorphic computing. Possibility of realization of a four-state

universal NAND gate is published in [4.50]. The following section discusses the technique to achieve the biaxial anisotropy in planar nanomagnets.

4.4.1. Achieving Biaxial Anisotropy in Nanomagnets

4.4.1.1: Shape Anisotropy:

Different anisotropic behaviours of a nanomagnet can be achieved by engineering the shape of a magnet as different shape provides different anisotropic behaviours. For example, Super m alloy (Ni80Fe14Mo5) nanomagnet with square, triangular and pentagonal shape can exhibit anisotropy with 4-fold, 6-fold and 10-fold symmetries, respectively[4.45].The anisotropies of these nanomagnets are measured using the Modulated Field Magneto-Optical Anisotropy technique is used to measure the anisotropy energies of these nanomagnets [4.45].

Recently, research paper have been published on the effects of shape anisotropy on concave nanomagnets, with minor variations in parameters such as the width and radius of curvature/concavity giving rise to major, but predictable variations for the direction of the easy axes of magnetization as well as its strength.[4.51]

4.4.1.2: Magneto crystalline Anisotropy

A 4-state memory element can also be implemented with a magnetostrictive layer of a single crystal structure (for example, single-crystal Terfenol-D, Ni), which would exhibit biaxial magneto crystalline anisotropy in the (001) plane. Using molecular beam epitaxy epitaxial films of single-crystal (001) can be grown on a piezoelectric substrate [4.52]. If the lateral dimension of the (001) layer is considerably larger than the thickness, it would be easier for the magnetisation vector to rotate in plane and, therefore makes it possible to lie the magnetization always in the (001) plane. As a result, the "easy" axes of single-crystal multiferroics lie in the ground/unstressed state are $[110]$,$[\bar{1}\bar{1}0]$,$[\bar{1}10]$, and $[1\bar{1}0]$, in Miller notation. Thus, for four possible energy minima, four 2-bit combinations can be represented (00, 01, 11,10), as illustrated in the saddle-shaped curve of Fig. 4.7. The resulting energy minima are obtained along the ±45° and ±135° directions. Therefore, a rotation of +45° is introduced which is equivalent to rotating the Cartesian coordinate axes by an angle of 45° about the axis perpendicular to the nanomagnet plane. In the new coordinate

system, the energy minima occur along the *x*- and *y*-axes (0°, ±90°, ±180°). The bit assignments ($0^0, \pm 90^0, +180^0$) are also shown.

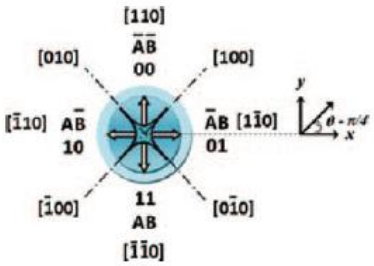


Fig. 4.7: Terfenol-D/PZT multiferroics nanomagnet having a biaxial anisotropy that creates four possible magnetization direction (easy axis) which are encoded as "00(up)," "01(right)," "11(down)" and "10(left)." The bit assignments are shown as $\bar{A}\bar{B}, \bar{A}B, AB$ and $A\bar{B}$.

4.4.2. Clocking/switching scheme of Nanomagnetic Logic (NML):

Despite these intrinsic advantages, nanomagnet–based technology [4.53, 4.17] has been un- able to replace transistor technology because the large extrinsic dissipation associated with the clocking scheme of this nanomagnet. Some such switching methods are:

(i) A current induced magnetic field: In this approach, [4.54] a magnetic field is produced by a current through Ampere's law: $I = \int_C \vec{H}.d\vec{l}$. To flip a magnet, The minimum magnetic field $\vec{H}_{\min}$ will be obtained by equating the magnetic field energy with the energy barrier E_b separating the two stable magnetization directions encoding the bits 0 and 1 in a shape-anisotropic nanomagnet, i.e. $\mu_0 M_S H_{\min} V = E_b$, where $\mu_0$is the permeability of free space, M_S is the saturation magnetization which we assume is 8×10^5A/m (typical value for cobalt), and V is the magnet's volume which we assume is $\sim 120nm \times 80nm \times 6nm$ which ensures that the magnet is in a single-domain state

The energy barrier fixes the equilibrium bit error probability $e^{-E_b/KT}$. For reasonable error rate, $E_b \geq 30KT$, which yields an I_{min} = 6 mA. Now assuming the typical value *R* of the magnet is 1-10 ohms and flipping time

of the magnet, $\Delta t = 1ns$, the energy dissipation $I_{\min}{}^2 R\Delta t = 36 - 360\,fJ \sim 10^7 - 10^8\,kT$.

(ii) Because of angular momentum transfer [4.55]. Recent STT based method dissipates about 10^5-$10^6 kT$ of energy to switch a single-domain nanomagnet for the energy barrier ~ $100kT$ [4.56-4.58].

(iii) ii) **By a spin transfer torque (STT) produced by a spin** polarized **current**: STT is generated by the conduction of spin polarised current through the magnet for switching. Method of switching a magnet by driving a spin-polarized current through it along the hard axis[4.48] or by spin diffusion current [4.53].The magnetization flips in the direction of spin polarization

iii) **A spin polarized current induced domain wall motion**: By this method, a magnet can be switched by inducing domain wall motion [4.59]. The switching of a multi-domain nanomagnet may be possible in the order of ns while dissipating $10^4\,kT$– $10^5 kT$ of energy [4.50]. However, this is still more dissipative than "straintonics" based switching where a multiferroics nanomagnet can be switched with mechanical strain generated by a tiny voltage [4.47,4.61].

4.4.4. Principle of Four-state Nanomagnetic Logic

We can further enhance the multiferroics functionality by incorporating biaxial magnetocrystalline anisotropy in the magnetostrictive layer, enabling it four possible stable magnetization directions ("up", " down", "right", "left") that are chosen to encode four possible 2-bit combinations (00, 11, 01, 10), illustrated in Fig. 4.1.These four directions correspond to the four nos. of easy axis with (degenerate) minimum energy configurations of the multiferroic. Here four-state nanomagnets is implemented by the single crystal structure of the multiferroic element (Terfenol-D). The multiferroics nanomagnets with four state possessing biaxial magnetocrystalline anisotropy can be used to realize four-state universal NAND logic , which can be used to create all other logic gates in digital system. This implemented by applying a clock cycle consisting of a sequence of compressive and tensile stresses to the output nanomagnet keeping middle of the input nanomagnets on each side of it. Therefore, the resultant state of theoutput magnet is obtained by the interaction of its following group of energies: dipole energy due to input

magnets, the applied stress cycle energy and applied dc bias magnetic field energy. The sequence of stress cycle and magnitude & direction of applied dc bias magnetic field determines the necessary condition for NAND logic.

4.4.4. Four-state NAND Logic

4.4.4.1. Theory

To implement realisation of a 4-state NAND gate, consider a linear array of three-nanomagnets is taken (along the *x*-axis) as shown in Figs. 4.8(a–d). A small dc bias magnetic field (pointing 'down') is also applied to obtain necessary logic. The output nanomagnets (EF) are placed in the middle of the input nanomagnet (AB & CD). In this condition, two types of dipole interaction arise. For the first case, dipole interaction prefers an anti ferromagnetic ordering when the magnetizations of both input nanomagnet are along the y- axis (perpendicular).

The second type occurs when the magnetizations are along the *x*-axis. In this case, dipole interaction favours the output magnet a parallel ordering (or ferromagnetic coupling) of adjacent magnetizations. These dipole interactions are interacted, along with a small global magnetic field to realize two universal NAND gates as explained below.

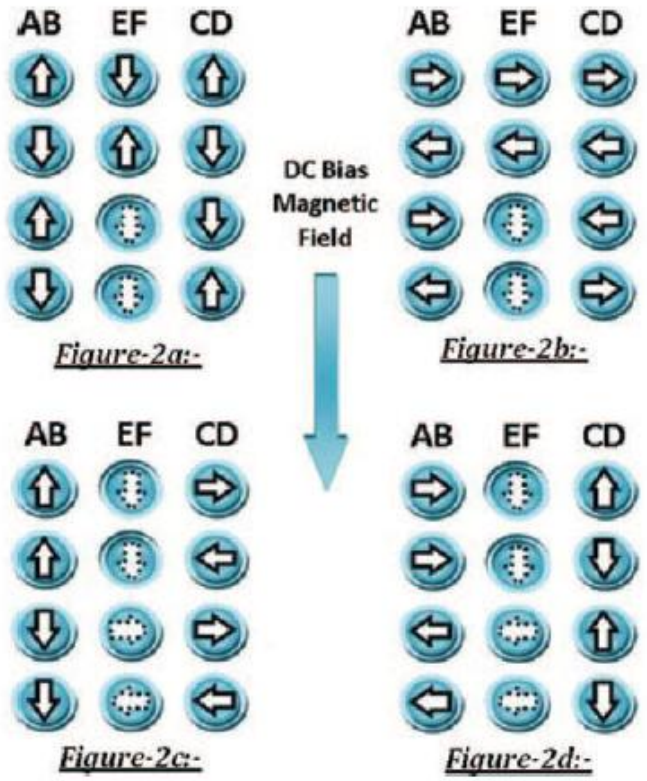


Fig.4.8 (a-d): The linear array of 3 nanomagnets to realize NAND gates. The output magnet EF is placed in the middle of input nanomagnets AB & CD. The dotted lines of the output states are settled finally by the DC bias field.

In the arrangement shown in Fig4.8.(a-d), AB & CD encode two input nanomagnet, while EF encodes output nanomagnet. Four different cases are studied, with each row representing a set of input combination. So for 4 state input bit, only 4×4=16 sets of the input magnetizations are available, producing only sixteen scenarios. The magnetisations of input magnets are fixed with a particular set by some external agent while a sequence of stress cycle (Compression → Relaxation → Tension →Relaxation) is applied in the output magnet encoding the output bit *EF* (described in subsequent chapter) which enables its magnetization to settle into an orientation that is always the NAND function of a combination of the inputs. Thus, the array behaves like a universal NAND gate.

The first case as depicted in Fig.4.8 (a), the magnetization direction of the input magnets is along y axis considering the nanomagnets array belong to x- axis. For " up" or "down" orientation of input magnetizations simultaneously (first two rows

of Fig. 4.8(a), the dipole coupling aligns the "down" or "up" orientation of the output nanomagnet. For the combination of one input is "up" and the other is "down", (third and fourth rows of Fig.4.8(a), the output nanomagnet is in a tied or frustrated state, which can be resolved by applying a global static magnetic field pointing " down" that settles the output magnetization to point "down". The second case is shown in Fig.4.8 (b), where input magnetizations are parallel to the nanomagnet array axis. When both input magnetizations are oriented "right" or "left" (first two rows of Fig. 4.8(b), the dipole coupling respectively brings "right" or "left" orientation of the output nanomagnet. When one input magnetization orients "right" and the other orients "left" (third and fourth rows of Fig. 4.8(b) the output nanomagnet is again in a tied state, and finally orients along downward because of the applied global dc bias field. The third (Fig. 4.8(c) and fourth Fig. 4.8(d)) cases are mixed inputs, where one input magnetization points to +y or –y axis and the other points to +x or –x axis of the array. It will favour a "down/up" or "left/right orientation of the output magnetization. If one of the inputs is "up", the bias field is additive with the dipole field ensuring that the output is "down", while if one of the inputs is " down", the bias field opposes the dipole field, causing the output to point either "left" or "right" depending on the second input.

The input bits (*AB*, *CD*) and the resulting output bit (*EF*), are transferred to a Karnaugh map (K-map) to obtain a simplify logical relation between the inputs and the output. The output table of the K-map is shown in Fig. 4.9.

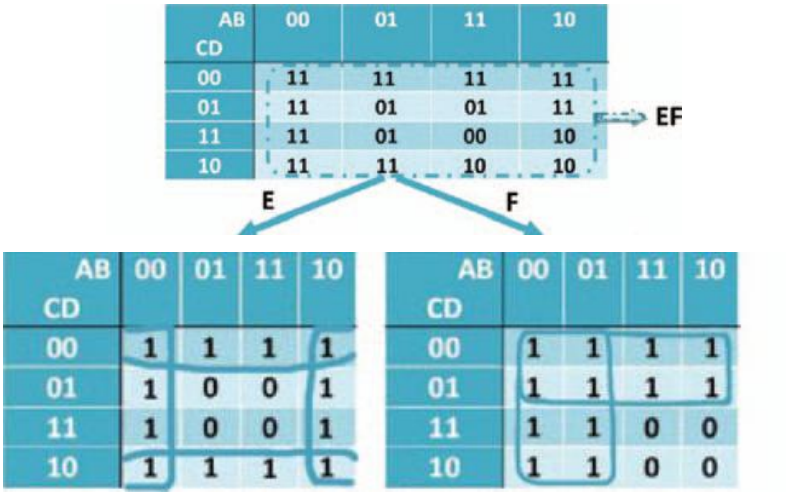


Fig. 4.9: The Karnaugh-Map representation for the relation between the output "EF" with the input "AB" and "CD." Finally we obtain the simplified logical expressions E= $\overline{BD}$ and F= $\overline{AC}$.

On simplification, it yields E= $\overline{BD}$ and F= $\overline{AC}$, which is NAND logic. To generate proper strain cycle a voltage is required to apply across the thickness of the piezoelectric layer. Detailed simulation results confirm that the magnetization of the output magnet always represents the NAND function of the inputs for any possible initial orientation. Strains are generated at the piezoelectric layer via the d_{31}coupling due to applied voltage which results in uniaxial compressive or tensile stress in the45° direction by mechanically clamping contraction or expansion in the direction perpendicular to the 45° direction. An applied electric field along the 45° direction can generate stress in the desired direction via the d_{33} coupling. Simulation is performed on output nanomagnet when its magnetization vector subtends an angle θ_2 with the positive x-axis(assuming a 2-dimensional model with no out-of-plane excursion).

$$E_{total}(\theta_2) = \frac{\mu_0}{4\pi R^3}[M_S^2\Omega^2][-2\cos\theta_2(\cos\theta_3+\cos\theta_1) + \sin\theta_2(\sin\theta_3+\sin\theta_1)] + \frac{K_1\Omega}{4}\cos^2(2\theta_2) - \frac{3}{2}\lambda_{100}\sigma\Omega\cos^2(\theta_2-\frac{\pi}{4}) + \frac{\mu_0}{4\pi}[M_S\Omega]H_{applied}\sin\theta_2 \quad (4.29)$$

Where the first term represents the dipole interaction energy between the output magnet and its neighbours subtending angles θ1 and θ_3 with the positive x-axis, the second term is the magneto crystalline anisotropy energy with $K1$ being the first-order magneto crystalline anisotropy constant, the third term is the stress anisotropy energy due to applied stress along the [100] direction (+45° with the x-axis) with λ_{100} being the magnetostrictive constant in the direction of stress, and the last term is the interaction energy due to the static bias field $H_{applied}$ pointing in the "down or "$\bar{1}\bar{1}0$" direction. Here, μ_0 is the permeability of free space, M_s is the saturation magnetization, Ω is the nanomagnet volume, and R is the distance between the centers of two adjacent nanomagnets. The positive stress (tension) 'σ' is required to rotate the magnetization anti clockwise for negative magnetostrictive coefficient material and the negative stress (compression) 'σ' is required to rotate the

magnetization anti clockwise for positive magnetostrictive co-efficient material [4.29]. The tensile stress σ′ is positive and compressive stress is negative. For each new set of input bits due to change of the orientations of one or both input magnets, the array temporarily goes into an excited state or local ground state. Now the output magnet settles into the new global ground state by the application of sequence of stresses on it in which its orientation is the NAND function of the new inputs. For Terfenol-D nanomagnets the first order magneto crystalline anisotropy constant (K1)<0, the easy axis in the 001 plane lie along the [110][$\bar{1}\bar{1}0$] $1\bar{1}0$][$\bar{1}10$]direction and the hard axis are [100][$\bar{1}00$][$0\bar{1}0$][010] directions assuming 2-D geometry of the nanomagnet which precludes out of plane excursion . Now the applied external clock will rotate ($\pi/4$) about the axis perpendicular to magnets plane which is sufficient to settle the magnet in the new ground state i.e., 0^0, $\pm 90^0$′,180^0.

Now consider the scenario when the entire magnet's magnetization belongs to global ground state i.e along their respective easy axis. Now any changes in the input bits cause the change in the dipole interaction energy between the magnets. Now the output magnet belongs to local energy minimum state (metastable state) and the dipole interaction energy is not so strong to move away from this state. So a change of input bits alone cannot produce a new and desired final output. However, upon applying a stress cycle, the magnetization of the output magnet can be pushed out of the easy axis (metastable state) and after withdrawal of stress, it should finally settle into the desired global ground state. For Terfenol-D, as λ_{100} is positive so a compressive stress (−ve) applied along [100] or $+45^0$ direction tends to rotate the magnetization away from the stress axis i.e., in -45^0or $+135^0$(depending on which is closest to the initial state) directions and a tensile stress rotates the magnetization along the stress axis i.e., either $+45^0$ or -135^0 directions [4.62]. After removing of both compressive and tensile stress cycle, the output magnetization settles into one of two adjacent easy directions depending upon the dipole interaction and static bias magnetic field. By choosing the direction and magnitude of the bias field properly, we can establish that the final output is always the NAND function of the inputs. This is the principle of our universal NAND gate.

To rotate the magnetization through 180°, one needs to apply both a compressive and tensile stress cycle, for producing a +90° rotation by each half-cycle However, applying this stress cycle does not always guarantee to rotate the magnetisation in

opposite state. The ultimate rotation of output magnet is determined uniquely by the states of the two input magnets as will be discussed later.

4.4.5: Role of the bias field magnitude

The dc bias field plays a vital role in determining the output state. In certain cases where the output magnet is in a fastened state as shown in the third and fourth rows in both Fig. 4.8(a) and 4.8(b), under the interaction of dipole coupling from its input magnets. The final output, which is "down" in this case because we have chosen a downward pointing dc bias field.

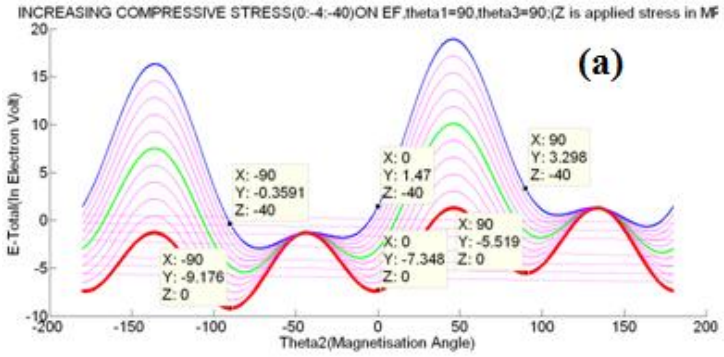
Furthermore, we also need to choose the magnitude of the dc bias magnetic field (~16000 A/m, applied along the -*y* axis) correctly to implement NAND logic. This is the case for all combination of input bits described in Fig. 4.8(c, d), because the dipole field (~25000 A/m) pointing along the magnet's ±*x*-axis (θ = 0° or 180° due to ferromagnetic coupling along the magnet axis) has twice the magnitude of the dipole field (~12500 A/m) acting along the magnet's ±*y*-axis (θ = 90°, 270°, anti-ferromagnetic coupling perpendicular to the magnet axis). This can be understood from the expression for the dipole energy in Equation (4.29), where the 'cosine' term contributes twice as much to the dipole interaction energy as the 'sine' term. For instance, in Fig. 4.8 (c) &(d), the inputs are *AB* = "right/left" and *CD* = "up/down". Therefore, the field experienced by *EF* due to dipole interaction consists of 2 components: H_{AB}~25000 A/m (along +*x* axis for rows 1, 2 and -*x* axis for rows 3, 4) and H_{EF} ~12500 A/m (along -*y* axis for rows 1, 3 and along +*y* axis for rows 2, 4). In the first row of Fig. 4.8(d), the downward dc bias field (~16000 A/m) adds to the upward dipole field due to *CD* (~ -12500 A/m). The resultant field in the -*y* direction (" down"), is +28500 A/m as it is more than the field due to *AB* i.e.25000 A/m along the +*x* direction. The second row (Fig. 4.8(d)) has input *AB* = "right" and *CD* = "down". Consequently, while the dipole field due to *AB* is the same as in the previous case (~25000A/m) while the dipole field experienced by EF due to CD is~12500 A/m and is countered by the dc bias field (+16000 A/m), which also lies along the same direction. Now the net dipole field due to CD on the output *EF* is therefore ~ 3500 A/m along -y direction. So the final settlement of the output magnet will be influenced by the input magnet AB, i.e. along +x direction, meeting the requirement for the NAND logic scheme in this arrangement.

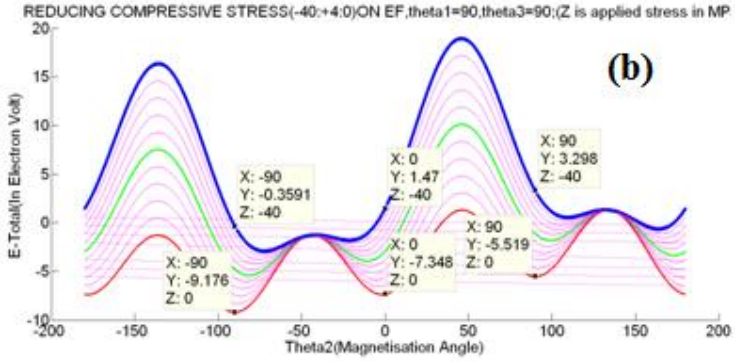
The magnitude of the dc bias field (16000 A/m) is judiciously chosen for the final settlement of the output magnet in our desired direction among the ferromagnetic and anti ferromagnetic coupling of the input magnets. The value of Dc bias field $H_{applied}$, should not be greater than 25000 A/m or less than 12500 A/m so that it cannot dominate on the perpendicular component of dipole field and can dominate only on the parallel component to achieve desired NAND logic. If bias field is taken beyond this limiting value, it will create undesired settlement of output magnet, a deviation from fig. 4.8(c) and 4.8(d), thereby invalidating the NAND logic scheme.

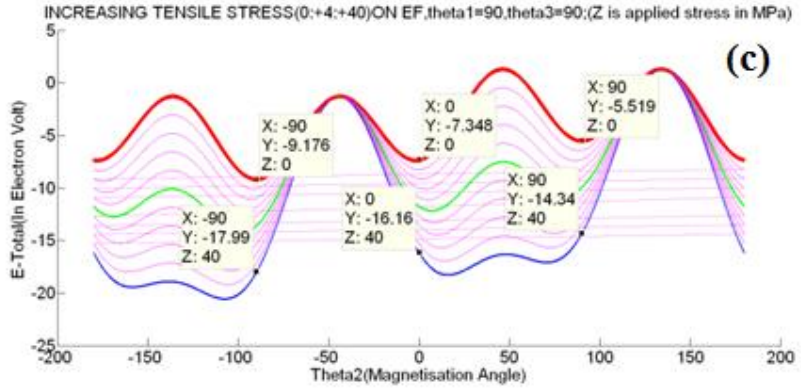
4.5: Numerical Simulations & Results

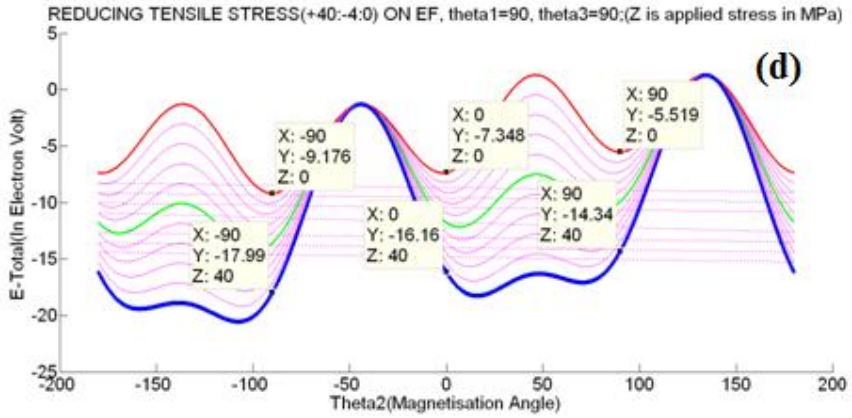
For Matlab simulations, the multiferroic nanomagnets are assumed to be made of two layers: single crystal Terfenol-D and lead-zirconate-titanate (PZT) with the following properties for Terfenol-D: λ_{100} =60 x 10^{-5} , K_1 = -1.75 x 10^5J m-3, M_s= 8 x 10^5A $m^{-1}$and Young's modulus Y =8 x 10^{10}Pa. [4.63] The PZT layer can transfer up to 500 x 10^{-6} strain to the Terfenol-d layer which allows a maximum stress of 40MPa to occur in the Terfenol-d layer.

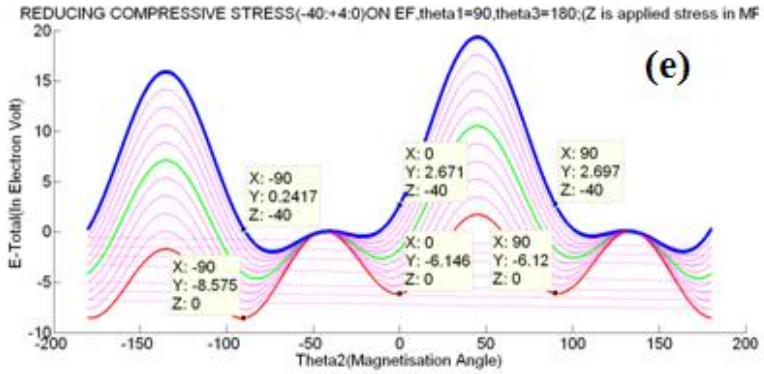
The nanomagnets are assumed to be circular disks with diameter 100 nm and thickness 10 nm, while the centre-to-centre distance between adjacent nanomagnets is 160 nm. The thickness of the piezoelectric layer is taken as 40nm. The above parameters are chosen so that output nanomagnets magnetization can only rotate after the application of required stress cycle only. Behavior of output nanomagnet can be simulated by computing its total energy, E_{total} (θ_2) with a sequence of applied stress cycle: Compression → Relaxation → Tension →Relaxation, in the decreasing or increasing of stresses from zero to 40 MPa and vice-versa. The simulation results are shown in Figure 4.10(a-h).

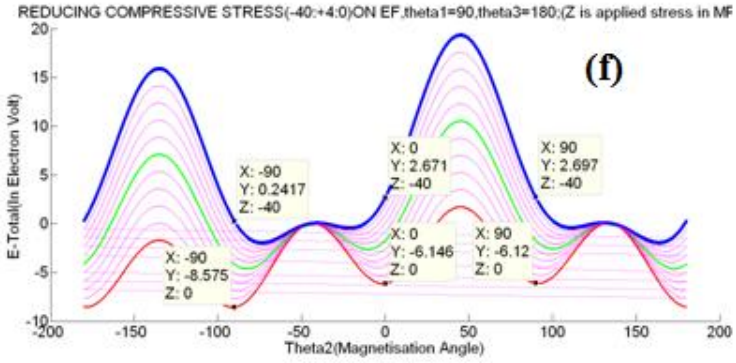

INCREASING COMPRESSIVE STRESS(0:-4:-40)ON EF,theta1=90,theta3=90;(Z is applied stress in MF
(a)
E-Total(In Electron Volt)
Theta2(Magnetisation Angle)
X: -90
Y: -0.3591
Z: -40
X: 0
Y: 1.47
Z: -40
X: 90
Y: 3.298
Z: -40
X: -90
Y: -9.176
Z: 0
X: 0
Y: -7.348
Z: 0
X: 90
Y: -5.519
Z: 0


REDUCING COMPRESSIVE STRESS(-40:+4:0)ON EF,theta1=90,theta3=90;(Z is applied stress in MP
(b)
E-Total(In Electron Volt)
Theta2(Magnetisation Angle)
X: -90
Y: -0.3591
Z: -40
X: 0
Y: 1.47
Z: -40
X: 90
Y: 3.298
Z: -40
X: -90
Y: -9.176
Z: 0
X: 0
Y: -7.348
Z: 0
X: 90
Y: -5.519
Z: 0


INCREASING TENSILE STRESS(0:+4:+40)ON EF,theta1=90,theta3=90;(Z is applied stress in MPa)
(c)
E-Total(In Electron Volt)
Theta2(Magnetisation Angle)
X: -90
Y: -17.99
Z: 40
X: -90
Y: -9.176
Z: 0
X: 0
Y: -16.16
Z: 40
X: 0
Y: -7.348
Z: 0
X: 90
Y: -14.34
Z: 40
X: 90
Y: -5.519
Z: 0


REDUCING TENSILE STRESS(+40:-4:0) ON EF, theta1=90, theta3=90;(Z is applied stress in MPa)
(d)
X: -90
Y: -9.176
Z: 0
X: 0
Y: -7.348
Z: 0
X: 90
Y: -5.519
Z: 0
X: -90
Y: -17.99
Z: 40
X: 0
Y: -16.16
Z: 40
X: 90
Y: -14.34
Z: 40
E-Total(In Electron Volt)
Theta2(Magnetisation Angle)


REDUCING COMPRESSIVE STRESS(-40:+4:0)ON EF,theta1=90,theta3=180;(Z is applied stress in MF
(e)
X: -90
Y: 0.2417
Z: -40
X: 0
Y: 2.671
Z: -40
X: 90
Y: 2.697
Z: -40
X: -90
Y: -8.575
Z: 0
X: 0
Y: -6.146
Z: 0
X: 90
Y: -6.12
Z: 0
E-Total(In Electron Volt)
Theta2(Magnetisation Angle)


REDUCING COMPRESSIVE STRESS(-40:+4:0)ON EF,theta1=90,theta3=180;(Z is applied stress in MF
(f)
X: -90
Y: 0.2417
Z: -40
X: 0
Y: 2.671
Z: -40
X: 90
Y: 2.697
Z: -40
X: -90
Y: -8.575
Z: 0
X: 0
Y: -6.146
Z: 0
X: 90
Y: -6.12
Z: 0
E-Total(In Electron Volt)
Theta2(Magnetisation Angle)

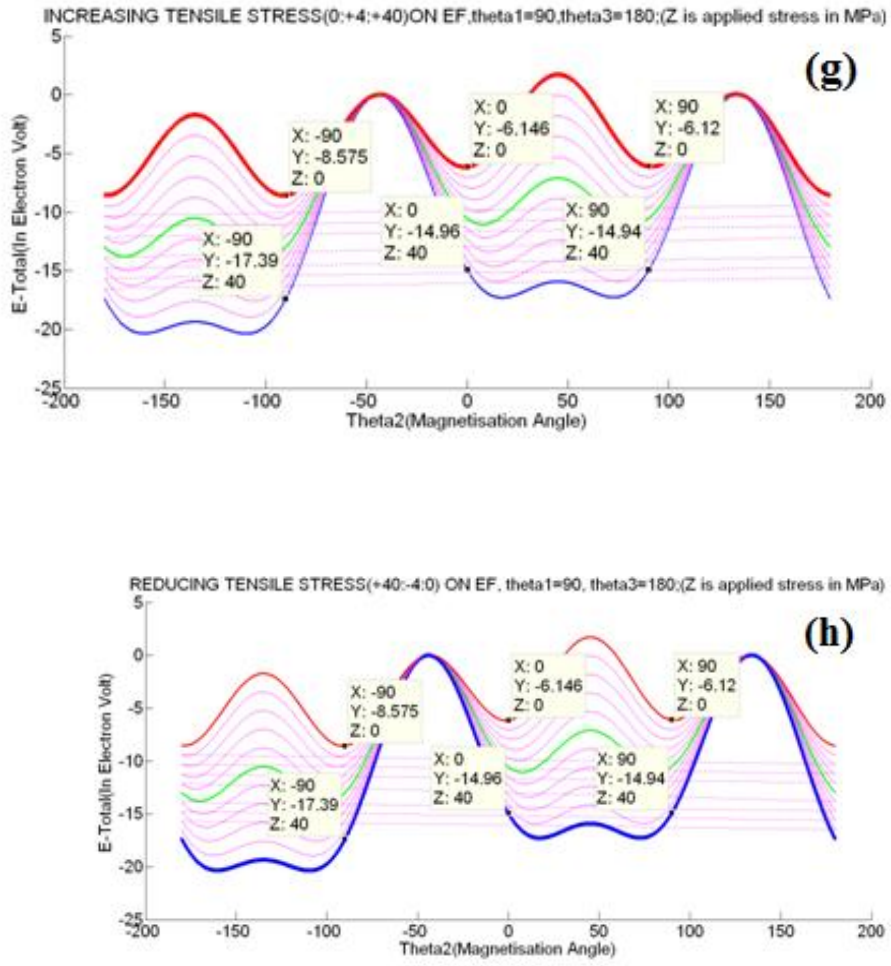


Fig. 4.10(a-d).Energy plots of the output nano magnet (EF) as a function of the magnetization angle θ_2 of the output nano magnet. The initial conditions used are input bits AB = 00, CD = 00, for which output EF = 11. (a) Stage one of the stress cycle in which compressive stress (−ve) is applied at +45_ direction on EF. The energy minima are shown along the minimum and maximum of the stress axis. (b) Upon relaxation of the stress on EF, the closest energy minimum is at −90_ direction. (c) With increasing tensile stress, magnetization rotates nearer to the stress axis. (d) Upon relaxation of tensile stress on EF, the closest energy minimum is at −90_ and therefore the magnetization rotates at that position.

Fig.4.10 (e-h) Represent input bits AB = 00, CD = 10 for which output EF = 11 and is carried under same stress cycle as shown in (a to d).

After the end of stress cycle, Final orientation of the output magnet will always be the new energy minimum nearest to the initial energy minimum which is dependent on the two input states. Here two particular cases have been studied. In the first case, the orientation of the first input magnet (left hand side) is considered as $\theta_1 = +90^0$

and of the second magnet (right hand side) is taken as $\theta_3 = +90^0$. In the second case the values are taken as $\theta_1 = +90^0$ and $\theta_3 = +180^0$. Now after simulation, we obtain the dynamics of output magnet as depicted in Figure 4.8. Here we observe for both the cases that final orientation of output magnet i.e. θ_2 is always settled at our desired logic level which is the minimum energy state and is equal to -90^0 confirming the NAND logic. In this case output is independent of the initial value and is dependent only the values of input only. The result can be verified for all other 14 different cases to obtain the output according to NAND logic.

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Chapter 5

STRAINTRONICS: IMPLEMENTATION OF PMN-PT/NI BASED NOR GATE WITH BIAXIAL ANISOTROPY

5.1. Introduction

The complementary metal-oxide semiconductor (CMOS) Based technologies faces the challenges when they are miniaturized to below 100-nm feature sizes, which are becoming the barrier to design nanodevices: (i) Standby power due to leakage ct. keeps increasing with the channel lengths decreasing and also due to the power supply which does not scale down proportionately; [5.1] (ii) The power density increases drastically [5.2] as density of transistors increases in the IC to keep at pace with the Moore's law;[5.3] (iii) Battery technologies have not been develop at par with the advancing power demands due to downscaling of ICs[5.4]The above mentioned problems generate the few micro-amperes of power from millimeter-sized circuits to operate. For this reason researchers are now in continuous searching on alternate technology.

Recently nanomagnet based switching technology have created a lot of attraction to the researcher due to its high energy efficiency [5.5] and nonvolatility. Among the many methods available, straintronics based switching supersedes all in terms of energy and speed [5.6-5.7]. Detail analyses have been discussed on the static and dynamic responses of the straintronics switching.[5.8-5.10]. The aim of straintronics study lies on the understanding of basic properties of solids on the nanoscale with structural dynamics of the crystal lattice. Nanoscale physics deals with the elastic, thermal or structural properties of nanostructures. It specifically covers both applied and fundamental problems. Examples are the coupling of strain fields of piezoelectric material to other phenomena, e.g. magnetism or ferroelectricity, respectively. These issues can be tackled by generating tailored strain fields by the application of input voltage in a piezoelectric material. This piezoelectric strain can manipulate the magnetization of the magnetostrictive element through magnetoelastic effect. Nanomagnets, need to be controlled in a desired way for the use of non-volatile memory applications. Here the functional generation and application of coherent strain on magnetostrictive material to change its magnetization orientation is referred as

Straintronics. Experimental demonstrations of the strain-assisted magnetization switching are already shown [5.11-5.13].

So, nanomagnetic logic (NML) is an emerging area for energy efficient computing in which logic bits are encoded by the single-domain nanomagnets according to their magnetization orientations .This logic system becomes non-volatile as well as power efficient due to absence of any leakage in the magnet. Logic operations are synchronised with a "clock" that flips the magnetization orientations of the magnets to produce desired output in response to one or more inputs. By analysing the dipole interactions between nearby magnets, different types of logic gates can be implemented. These gates can then be connected through" logical wire "appropriately with Dipole coupled magnet arrays to implement any sequential or combinational digital circuits. In some logic circuit NOR gate is preferred as it requires at least one input being true to make the output false, where NAND requires both to be true. This chapter discusses the design methodology of straintronics based 4 state universal (NOR) gate which can be used to process digital information as well as basic memory element.

5.2. Literature survey:

A multiferroics material contains at least two ferroic properties: ferroelectricity, ferromagnetism and ferroelasticity.[5.14] Multiferroic materials, can produce magnetoelectric effect through the coupling interaction. In 1894 the magnetoelectric effect was first pointed out by Curie, when he predicted that a body with asymmetric molecular structure placed in a magnetic field might become polarized .[5.15] However the progress was slow until 1958, when Landau and Lifshitz have published their research about magnetoelectric effect based on crystal symmetry[5.16]. The existence of magnetoelectric coupling in chromium oxide Cr_2O_3 was first predicted by Dzyaloshinskii [5.17], which was later established experimentally by Astrov [5.18] in the 1960s. But the coupling was very small to use it practically. Many single-phase magnetoelectric natural materials have been extensively studied in [5.19–5.22], but few of them have been observed with an intrinsic magnetoelectric effect with a low coupling strength at room temperature. In search of this multiferroic composites composed of ferroelectric materials and ferromagnetic materials attract attention to the researcher due

to their high magnetoelectric coefficients at room temperature. Piezoelectric strain ε can be generated in the ferroelectric phase with the input electric field E, which can change the magnetization M of the ferromagnetic phase. Early research on magnetoelectric composites was performed by van Suchtelen at Phillips Laboratories in Netherlands in the 1970s [5.23]. He prepared $BaTiO_3$-$CoFe_2O_4$ ceramic composites by solidification of eutectic compositions in the Fe-Co-Ti-Ba-O form. Bulk magnetoelectric composites research geared at the starting of the 21st century, when Tb1-xDyxFe2 (Terfenol-D) was developed by the Naval Ordnance Laboratory in United States as a ferromagnetic material with giant magnetostriction. In 2001, the magnetoelectric effect was shown by Ryu et al. in their first developed composite 2-2 type structure Pb (Zr, TiO_3 (PZT) and Terfenol-D disks [5.24]. In 2003, Terfenol-D and piezoelectric ceramics based magnetoelectric devices was reported by Dong [5.25- 5.26]. From 2007 research have been started on investigating thin film ferromagnetic/bulk piezoelectric multiferroic heterostructures after the invention of strain-mediated magnetization manipulation in a multiferroic $La0.67Sr0.33MnO_3/BaTiO_3$ heterostructure by Eerenstein et al [5.27]. Further research develops magnetic anisotropy energy change due to generated piezoelectric strain in $Ni/Pb(ZrxTi1-x)O_3$ ($x \sim 0.3$) [5.28] and $CoFe_2O_4/Pb(Mg_1/3Nb_2/3)0.7Ti0.3O_3$ [5.29] multiferroic composites. In 2011, Wu et al first published the research paper on magnetoelectric effect in $Ni/[Pb(Mg_1/3Nb_2/3)O_3](1-x)-[PbTiO_3]x$ (PMN-PT) ($x \approx 32\%$) which is basically magnetic thin film ferromagnetic/bulk piezoelectric multiferroic heterostructure [5.30], [5.31], [5.32] . This type of magnetization change in Ni thin film due to induced strain is ideal for the design of straintronics based logic gates and memory. Later, Hu et al published simulation results on high-density straintronics based random access memory operating at room temperature with ultra low power dissipation in Ni/PMN-PT heterostructures [5.33] which is more efficient than conventional flash-NAND and MRAM. In 2012, Hockel et al reported the change of magnetization orientation in a micron-sized Ni ring structure due to strain generated and transferred by bulk PMN-PT substrate [5.34]. This is the first experimental report of magnetic behavior of the nanomagnetic structures on a bulk piezoelectric substrate. After this in 2013 Buzzi et al published 180° magnetization switching in single domain Ni elliptical shaped nanomagnets (150nm × 100nm × 10nm) on bulk PMN-PT substrate [5.35].

On the other hand straintronics devices are basically developed with magnetostriction effect. It was George Joule who first discovered the Magnetostriction effect in 1842 (1842; 1884). This begins the magnetoelastic effect of a ferromagnetic material due to the any external magnetic field . Isotropic and anisotropic magnetostriction are the two fields of magnetostriction and is known as Joule, 1884 effects. The isotropic magnetostriction coefficient is basically indicates change in body shape in omni directions and is measured as $\omega = \Delta V / V$. Whereas anisotropic magnetostriction coefficient $\lambda = \Delta l / l$ describes unidirectional changes in body size towards the direction of the applied magnetic field. The physics behind the anisotropic magnetostriction of a ferromagnetic material is the switching of the magnetization direction due to any external magnetic field. This rotation generates internal strain in the material structure and, consequently, its elastic deformation or alternately a generated strain can cause rotation by generating an external magnetic field. Anisotropic magnetostriction value is significantly greater than volume magnetostriction ($\lambda \gg \omega$), so usually when assessing the value of magnetostriction ω is not considered. Anisotropic magnetostriction or magnetostriction depends on the crystallographic saturized magnetisation direction. it is denoted by magnitude of saturation magnetostriction λ_s. For cubic crystals, saturation magnetostriction is denoted by λ_{100} and λ_{111}. For isotropic single phase polycrystalline cubic materials, saturation magnetostriction λ_s can be estimated by measurements of λ_{100} and λ_{111} of a single crystal having the same composition as the polycrystal [5.36].

The relation between magnetostriction coefficient with the external field $\lambda(H)$ is established by magnetization curve, which is also related with the magnetic anisotropy energy.

In nanocrystalline ferromagnetic layer there is a possibility of the coexistence of crystalline and amorphous phases. Then the effective macroscopic magnetostriction λ_{eff} can be obtained from the average value of the crystalline (λ_{cr}) and amorphous magnetostriction (λ_{am}).

In Modern technology, it is permissible to have ferromagnetic, nanocrystalline and nanocomposite layers of different compositions. These variations in structural features of the layers play a significant role on MS properties. The details of MS properties of amorphous and nanocrystalline structures are described in [5.37]. straintronics devices are basically developed with magnetostriction effect. Here the effects of both forward

and reverse magnetostriction are used. Fig. 1. Depicts the characteristic of ferromagnetic layers with the influence of a constant applying magnetic field and a tensile stress.

It is clear that for direct magnetostriction, the strength of the external magnetic field can cause magnetic saturation in the layer with the relative deformation λ_s. For reverse magnetostriction, any mechanical deformation of the layer with 180 ° domain area in perpendicular plane towards the magnetic anisotropy axis causes only domain rotation without affecting the layer magnetisation. This rotation in the magnetic state is of particular interest in connection with the magnetoresistive [5.38] or magneto impedence effects [5.39] in the field of straintronics.

Since nanomagnets have been proposed as the building block of next generation digital systems, this paper paved the pathway towards magnetoelectric universal logic devices with ultra-low power consumption.

5.3. Material selection:

5.3. 1 .Multiferroic

Multiferroics are defined as materials that exhibit more than one of the following ferroic properties:

- ferromagnetism -- a magnetisation that can be changed by an applied magnetic field,
- ferroelectricity -- an electric polarisation that is switchable by an applied external electric field, and
- ferroelasticity -- a deformation that can cause strain by an applied stress. The term magnetoelectric multiferroics is usually used to describe the material which are simultaneously ferromagnetic and ferroelectric [5.40]

The formation of a ferroic order or polarized electric or magnetic material is formed with the breaking of a symmetry spatial inversion or time reversal. For example, ferroelectrics are electrically polarized when the symmetry of spatial inversion is broken and ferromagnets develop magnetic behavior after the time reversal is broken. The polarization P and magnetization M are used for electric and magnetic parameters for ferroelectrics or ferromagnets respectively. This leads to the familiar switching and storing of magnetic bits in a memory using magnetic fields.

Ferroics are usually described by their parameters under space inversion and time reversal like the following table. In a polar ferroelectric when the symmetry is broken operation of space inversion anti symmetric is formed by reversing the direction of polarization while the magnetization remains invariant. So ferromagnets and ferroelastics which are non-polar remain time invariant under space inversion. On the other hand when the time-reversal anti symmetric is formed, it alters the sign of M without changing the sign of P. Therefore ferromagnets are only time variant under time reversal.

Table 5.1:

	Space-inversion symmetric	**Space-inversion antisymmetric**
Time-reversal symmetric	Ferroelastic	Ferroelectric
Time-reversal antisymmetric	Ferromagnetic	Magnetoelectric Multiferroic

Materials belong to 2nd row 2nd column which have both the properties are called magnetoelectric multiferroics since they are both ferromagnetic and ferroelectric.

The most important property of multiferroics is that they can be coupled such that one ferroic property can be controlled with the associative field of the other. For example in Ferroelastic ferroelectrics, an electric field can manipulate a shape change or a pressure can induce a voltage which is basically piezoelectric material. In ferroelastic ferromagnets magnetic field can induce pressure or vice versa which are basically piezomagnetic behavior. Magnetoelectric multiferroics are attracted to researcher as it can manipulate the magnetism with an electric field which have lower energy requirements than their magnetic counterparts.

Multiferroic materials can exhibit multiple ferroic orders that are being potentially used for spintronics, high-density data storage and magnetoelectric transducers [5.41]. Basically multiferroics have generally been defined as single-phase materials. Recently a

number of composite multiferroics consisting of ferromagnetic and piezoelectric materials supersede the single-phase multiferroics due to high magnetoelectric response and high operating temperatures [5.42-5.43]. The multiferroic materials studied in this research is a two-phase system consisting of a piezoelectric layer in contact with a thin ferromagnetic layer. In such system, electrical and magnetic coupling occurs through elastic interaction and is called magnetoelectric effect [5.44]. When a DC voltage is applied to the piezoelectric layer, the generated strain is elastically transferred to the magnetostrictive layer and causes a change in its orientation of magnetization[5.45-5.46]. So, Electric field-induced magnetization switching in multiferroics are getting attention to the researcher for designing of ultra-low-energy computing devices in beyond CMOS technology. Multiferroics containing bistable nanomagnets are very suitable for storing as well as processing of digital information.

5.3. 2. Piezoelectric material: PMN-PT vs PZT

Piezoelectric materials are increasingly used as a means for electro-mechanical coupling in small scale systems. As an active piezoelectric material, Lead zirconate titanate $Pb_xZr_{1-x}TiO_3$ (PZT) (PZT) is used in the majority of such energy conversion devices reported in the literature [5.47-5.53] as well as our previous chapter. PZT based NOR gate is also discussed in [5.54].

In our model ,single crystal $xPb(Mg_{1/3}Nb_{2/3})$-$(1-x)PbTiO_3$ or PMN-PT is used due to its better electro-mechanical coupling co-efficients, better sensitivity ,higher S/N ratio [5.55-5.56] . The single crystal PMN-PT can be grown by modified Bridgman technique or the solid-state single crystal growth technique. This material exhibit better piezoelectric properties (e.g.d_{33}=3500 pC/N, d_{31}=-1200 pC/N, k33=0.95 etc.) that considerably surpass the PZT material by a factor of 4 to 5 [5.57]. Moreover the PMN-PT material posse's higher piezoelectric constant and lower damping which can increase the output power efficiency [5.58]. PMN-PT have very high piezoelectric constant and electromechanical coupling factor than PZT and can be grown epitaxially as single crystal piezoelectric material. It is shown that devices with PMN-PT and PZT with the same dimension, the output voltage, output power and power density of the PMN-PT device superseded the PZT device performance [5.59]. Moreover, PMN-PT material is compatible with silicon

micromachining process, so miniaturization and integration of devices is possible with traditional Si technology [5.60]. In consequence the integration is possible in the nanodevices in the harvesting stage as well as with the traditional electronic circuit.

5.3.3. Magnetostrictive material (Ni nanomagnet)

Nickel is taken as magnetostrictive material as it can be switched with a very low voltage as it has the lowest energy barrier as depicted in fig. 5.1[5.61].

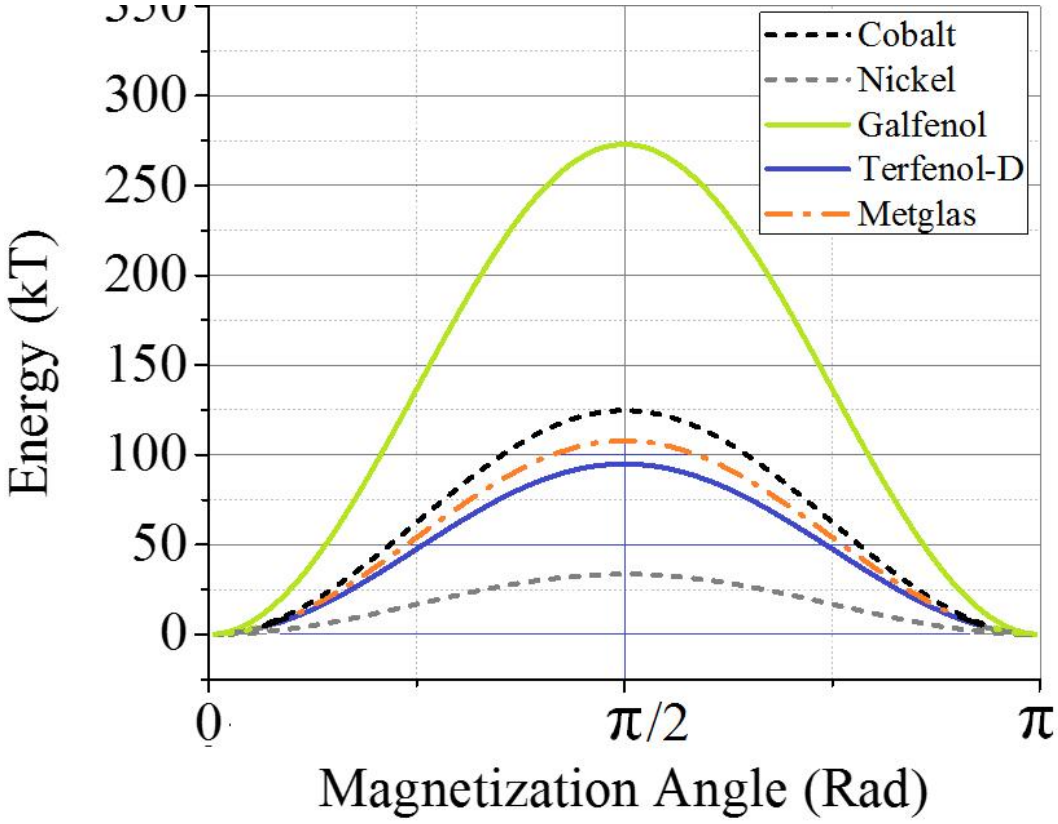

Fig. 5.1: Comparison of free layer energy barrier among different common magnetostrictive material. Galfenol has the highest and Nickel has the lowest energy barrier.

Moreover a 4-state device can be implemented with the single crystal Ni which would have biaxial magnetocrystalline anisotropy property in the (001) plane. Molecular beam epitaxy (MBE) [5.62] method can be employed for the growth of Epitaxial films of single-crystal (001) Ni on a suitable substrate. The crystal structure for Ni (fcc) is depicted in Fig. 5.2(a). If the lateral dimension of the (001) Ni layer is considerably sufficiently larger

than the lateral dimensions, it would be energetically favours the magnetization to lie always in the (001) plane i.e. in the lowest energy state. As a result, the "easy" axes of single-crystal Ni in the unstressed state are 110, $1\bar{1}0, \bar{1}\bar{1}0, \bar{1}10$, in Miller notation. Thus, there are four possible energy minima states which can be encoded by 2-bit combinations as 00, 01, 11, 10, as shown in the saddle-shaped curve of Fig. 5.2(b). The resulting 4 stable states occur along the ±90° and ±180° directions. The bit assignments ($AB, \bar{A}B, A\bar{B}, \bar{A}\bar{B}$) are also shown.

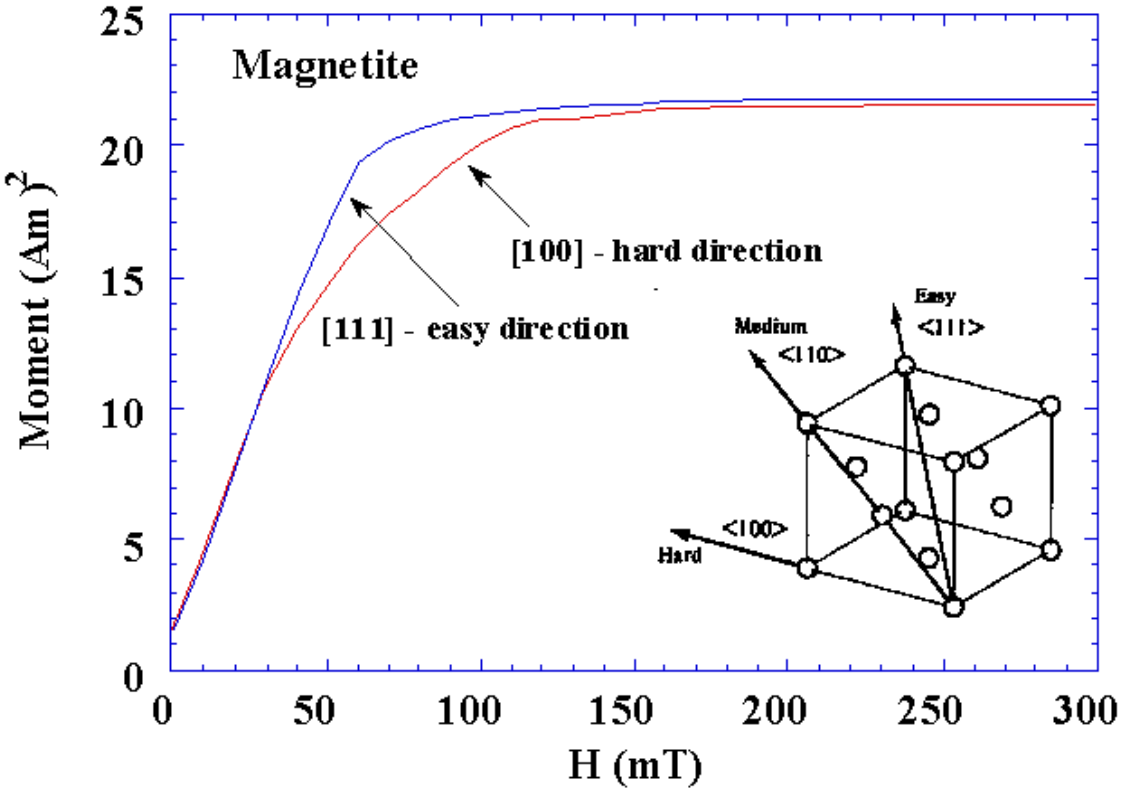

Fig.5.2(a): Crystal structure of Ni nanomagnet

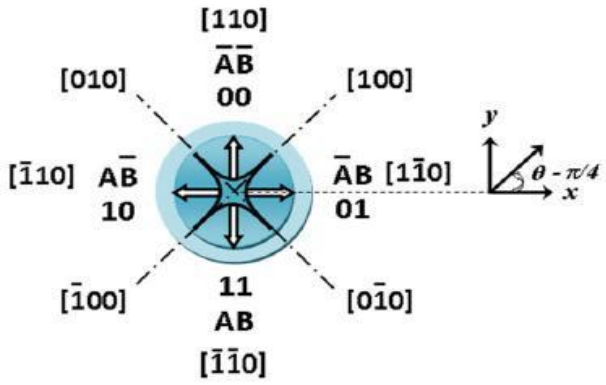

Fig. 5.2(b): Ni/PMN-PT multiferroic nanomagnet having a biaxial anisotropy that creates four possible magnetization directions (easy axis) which are encoded as "00(up)", "01(right)", "11(down)" and "10(left)". The bit assignments are shown as $\overline{A}\overline{B}, \overline{A}B, AB$ and $A\overline{B}$.

5.5. STRAINTRONICS BASED SWITCHING PRINCIPLE

Recently, a very energy-efficient switching scheme of nanomagnetic logic was proposed [5.63], in which an applied voltage can generate mechanical strain which is able to rotate the magnetization of a magnetostrictive layer. It can be implemented by applying a tiny voltage to a multiferroic nanomagnet consisting of two electro-mechanically coupled piezoelectric and magnetostrictive layers (Fig. 5.3) [5.16]. The applied voltage generates strain in the piezoelectric layer which is propagated entirely to the nanomagnet layer through magneto-elastic coupling if the latter layer is much thiner than the former [5.63]. This strain can rotate the magnetization of the magnetostrictive layer of multi domain nanomagnet by a desired angle and has been published in recent paper [5.64]. Normally, strain can rotate the magnetization of an isolated magnet by up to hard axis because it moves the energy minimum of the magnet from the easy to the hard axis due to Villari effect. However, if the strain is withdrawn at the right moment, as soon as the rotation to the hard axis has been reached, the magnetization will continue to rotate and the final magnetization will settle up to the nearest easy axis , thus completes rotation by an angle of 180° [5.65] for two state magnets and 90^0 for four state magnets [5.66].

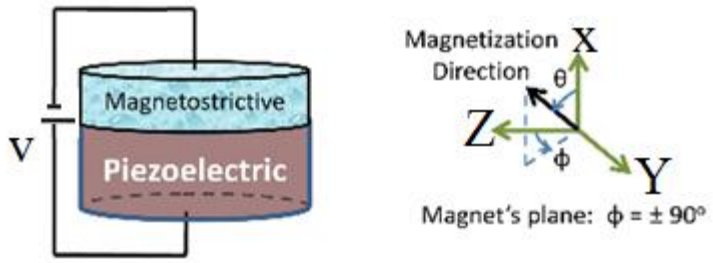

Fig. 5.3: A piezoelectric-magnetostrictive heterostructures and axis alignment of its magnetisation vector.

5.5. Theory of 4 States NOR Gate

In a Multiferroic nanomagnet generally the piezoelectric layer has been taken as 4 times thicker than magnetostrictive layer. In such nanomagnet electro-magnetic effect arises due to coupling of electric and magnetic field through magnetoelastic interaction [5.67-5.69]. As a tiny voltage is applied to the piezoelectric layer, the generated strain due to change in shape is totally transferred to the magnetostrictive layer (due to thin layer) making a change in its magnetization direction.

Here Nickel (Ni) is taken as magnetostrictive material which has 3 unique axes in terms of magnetization direction. It has easy axis along the <111> direction, a medium axis along the <110> direction and hard axis along the <100> direction as shown in fig.5.2. Now if Ni crystal is cut along '001' plane which is the X-Y plane of Ni nanomagnet, then easy axis is the <110>direction and hard axis is along the <100> direction. Here easy axis lies in the same direction, as medium axis for the entire crystal depicted in fig. 5.2.The easy axis of a single crystal Ni nanomagnet in (001) plane are the [110], $[\bar{1}\ \bar{1}\ 0]$, $[1\ \bar{1}\ 0]$ and $[\bar{1}\ 1\ 0]$ directions and the hard axis are the$[100]$,$[\bar{1}00]$,$[010]$,$[0\bar{1}0]$directions. Now these Four stable directions are encoded by two bit combinations like (00, 01, 10, 11), which are the four ground states of the multiferroic nanomagnet. When stress is applied, this would result in energy minima in ±45° and ±135° directions due to Villari effect. So a rotation of +45° is introduced, by rotating the Cartesian co-ordinate axis, by an angle of $(\theta-\pi/4)$, about the axis normal to magnet's plane by the applied stress. In the

new system energy minima would lie along the direction of X and Y axis, (θ=0°, ±90°, ±180°), where θ is the angle of magnetization direction with the X axis.

5.6. Implementation

The proposed gate can be realized with a linear array of three multiferroic nanomagnets as depicted in fig.5.4 (a-d), wherein direction of array gets along x axis. Thus the two input bits are encoded by peripheral magnets AB & CD and the output bits with central magnet EF, which is placed in between of the input nanomagnets. With the application of a DC magnetic field in upward direction, the composite 4-state input bits can produce (4×4) =16 possible combinations, producing sixteen distinct states. Assuming fixed magnetization of input magnets, output magnet's magnetization orientation can be changed by a stress cycle and with an externally applied static magnetic field with upward direction. In this case the NOR function output always can be obtained from combination of all possible sets of the inputs. Thus array behaves like a universal NOR Gate.

By transferring input bits (AB,CD) and the resulting output bits (EF) into corresponding K-map as shown in Fig.5.5, we get E= $\overline{B+D}$ and F= $\overline{A+C}$ which confirms the NOR operation.

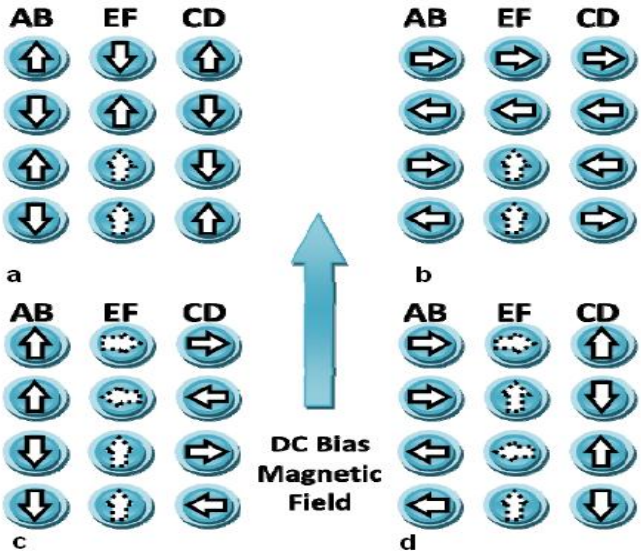

Fig. 5.4- (a-d): Here it is shown that the combination of the three nanomagnet array with a static bias magnet field in up-word direction. Here the two input nanomagnets "AB", "CD" are kept on both sides of the output nanomagnet "EF". The dotted arrows represents the cases where the bias field influenced the output state .The output magnet "EF" is always the NOR function of the input magnet "AB" and "CD".

CD \ AB	00	01	11	10
00	11	01	00	10
01	01	01	00	00
11	00	00	00	00
10	10	00	00	10

EF

CD \ AB	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

CD \ AB	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

Fig. 5.5: The Karnaugh-Map representation of the output "EF" as a function of input "AB" and "CD". Finally the simplified logical expressions "E= $\overline{B+D}$ **" and "F=** $\overline{A+C}$ **" is obtained.**

5.7. Simulation Results and Discussion

Simulation analysis is performed by using the following energy equation

$$E_{total}(\theta_2) = \frac{\mu_0}{4\pi R^3}[M_s{}^2V^2][-2\cos\theta_2(\cos\theta_3+\cos\theta_1)+\sin\theta_2(\sin\theta_3+\sin\theta_1)]+\frac{K_1V}{4}\cos^2(2\theta_2)$$
$$-\frac{3}{2}\lambda_{100}\sigma V\cos^2(\theta_2-\frac{\pi}{4})-\frac{M_sV}{4\pi}B_{applied}\sin\theta_2 \quad \text{.....(5.1)}$$

Here θ_2 is the angle of output magnetization vector (EF) with (+ve) X axis, θ_1 and θ_3 are the angles of input magnetization vectors (AB & CD) with (+ve) X axis).

In the energy equation, 1st term represent the dipole interaction energy between the output magnet with its neighboring input magnets. The 2nd term represents the magneto crystalline anisotropy energy with K_1 being the first order magneto crystalline anisotropy constant. The 3rd term is the stress anisotropy energy due to stress **σ** applied along the [100] direction with λ_{100} being the magnetostrictive constant in that direction, and the 4th term is the energy due to external static bias magnetic field $B_{applied}$ pointing in the up [110] direction, whereas μ_0 is the permeability of free space and M_s is the saturation magnetization,V is the volume of the nanomagnet and R is the centre to centre distance between two adjacent nanomagnet. Here the stress **σ** is positive and negative for tension and compression respectively as Ni have positive magnetostriction coefficient.

The input magnet's magnetisation orientation can create 16 nos of new set of input bits. A sequence of stresses (tensile and compressive) is applied on the output magnet with each orientation of input magnets. This, along with dipole interaction and proper bias field, drives the output magnet in a new ground state wherein its orientation is the NOR function of the inputs for all the 16 cases.

The orientation of output magnet due to input magnets is shown in Fig. 5.4-(a-d). In Fig. 5.4(a) for the first two rows, output magnet favours antiferromagnetic ordering (down and up) due to inherent property of magnets. But for the 3rd and 4th rows, the output magnet is in a tied state. It can be resolved by applying a global static magnetic field those points in 'up', bringing the output magnetization to point 'up'.

Again for fig.5.4 (b), output magnet of the first two rows follows ferromagnetic ordering (right or left) due to natural tendency of magnets. In the next two rows the frustrated output magnet, due to the external global dc magnetic field, follows the 'up' direction.

In the case of Figs. 5.4(c) and 5.4(d), there are two mixed inputs. One input magnet points either up or down and the other points either left or right with reference to the array axis. If either of the inputs is 'down', the bias field adds to the dipole field, ensuring the output is 'up'.

If one of the input is 'up', the bias field opposes the dipole field, causing to settle final output to point either 'left' or 'right' depending on the 2nd input. Now the dipole field along ±x axis is 1.86mT and the dipole field along ±y axis is 0.93mT. For this dc bias field is judiciously taken as 1.25 mT(applied along the +y-axis), so that desired o/p can be achieved in case of mixed inputs combinations. In this case when one of the input favours the dc bias field along+y axis (2.18mT), it overcomes the dipole field due to ferromagnetic coupling alone (1.86mT along ±x-axis) and it settles in 'up' direction. Now when bias field counters one of the inputs, it becomes .32mT, so the ferromagnetic coupling (±x-axis or $\boldsymbol{\theta}_{2=} \pm 180^0$) favours upon the antiferromagnetic coupling (±y-axis or $\boldsymbol{\theta}_{2=} \pm 90^0$) and it settles along the direction of the 2nd input. This is very much desired to achieve NOR logic. For simulations, multiferroic nano magnets are consisting of two layers. Single crystal Nickel and lead magnesium niobate-lead titanate (PMN-PT) with the following properties for Ni, λ_{100}= - 2×10^{-5}, K1= - 5.5×10^{3} Jm^{-3}, M_s=$5.85\times10^{5}Am^{-1}$, Young's modulus Y=2×10^{11} Pa [5.17].

The PMN-PT layer used here is composed of 85.9% PMN, 15.1% PT with 2.5% Sr doped (model S250141). It can transfer up to 500×10^{-6} strain to the Ni layer, which allows a maximum stress of 100 MPa in the Ni layer. The nanomagnet used for analytical simulation is taken as circular disc with radius 50nm and thickness of 10nm, while the centre to centre separation is 160nm. The above parameters restrict the dipole interaction energy (8.484k T) to overcome the barrier of magneto crystalline anisotropy energy (21kT). The switching is possible only when stress is applied (stress anisotropy energy 56 kT) in the magnetostrictive Ni due to a transferred strain of 500×10^{-6} from PMN-PT

layer. This is desirable to obtain NOR logic as well as to avoid spontaneous switching without the application of stress cycle.

180^0 switching of nanomagnet is possible with the application of both tensile and compressive stress cycle successively. Each stress cycle produces a 90^0 rotation. The reason behind this is that a tensile stress applied in the direction [100] rotates the magnetization of Ni in either the -45^0 or the $+135^0$direction. The final o/p is always closest to the initial state. The compressive stress rotates the magnetization to either the -135^0 or $+45^0$ state which is also nearest to the initial state. But the states of two input magnets uniquely determine the final amount of rotation. So for the entire stress cycle, it may not always perform a 180^0 rotation of output magnet. Now we can analyze the behavior of output magnet's behavior as depicted in Fig.5.4 (a) to (d) by performing MATLAB simulation on equation (1) with the application of tension-relaxation-compression-relaxation stress cycle in increment/decrement of 10Mpa stress up to maximum amplitude of 100Mpa. The results are obtained as shown in Fig.5.5.

At the end of stress cycle, the output magnet will always settles at new energy minimum nearest to the initial energy minimum which is always the NOR function of the inputs for all 16 possible states. Here we have analyzed one particular case in which input magnets have magnetization states AB='01' and CD='00' and output magnet EF is taken initially in the '10' state as shown in fig.5.6 (a-d).

Tensile and compressive stress cycles are applied to the output nanomagnet along [100] direction as Fig 5.6(a) to 5.6(d). Tensile stress applied to the nanomagnet causes output magnetization to rotate towards $\sim+135^0$and settles into $\sim+115^0$ as shown in fig.5.6 (a). This is because tensile stress along $+45^0$ directions on negative magnetostrictive material like Ni causes to rotate the magnetization towards either the $+135^0$ or -45^0 direction depending on which is closer to the initial orientation. In the present case $+135^0$ is closer to the initial orientation, so magnetization rotates from $+90^0$ to $\sim +135^0$ and finally settles into $\sim+115^0$.

In the next stage the stress on output magnet EF is reduced to zero and as a result the output magnet's magnetization settles into initial orientation, i.e. at $+90^0$ as expected in Fig.5.6 (b). Followings this, a compressive stress is applied to 'EF' at $+45^0$, that rotates the

magnetization from ~90^0 to~+20^0(towards +$45^0$and tilted towards 0^0) as in Fig.5.6(c).This is due to the fact that ferromagnetic couplings favours over the antiferromagnetic coupling by a factor 2, as can be easily inferred from dipole energy term in equation (1). Subsequently, when stress on 'EF' is released to zero, the final output state of the magnet settles into 0^0,under the influence of both dipole interaction energy and bias field as expected. Thus the end of stress cycle, the output 'EF'='00' is realized, which shows successful NOR operation as in fig.5.6 (d).

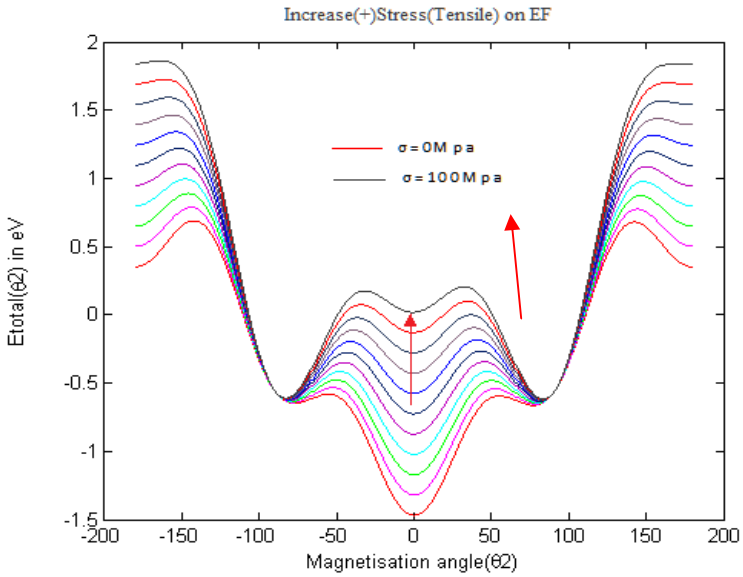

Fig.5.6(a)

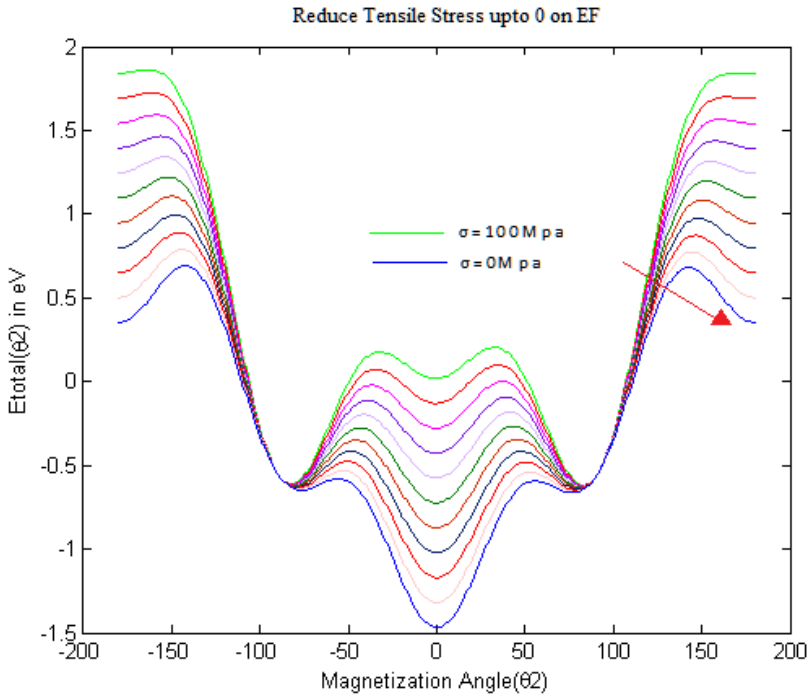

Fig 5.6 (b)

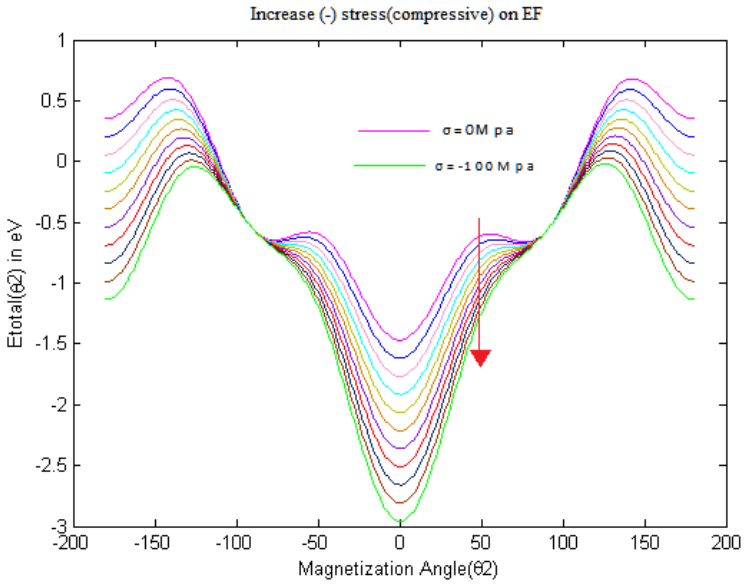

Fig. 5.6(c)

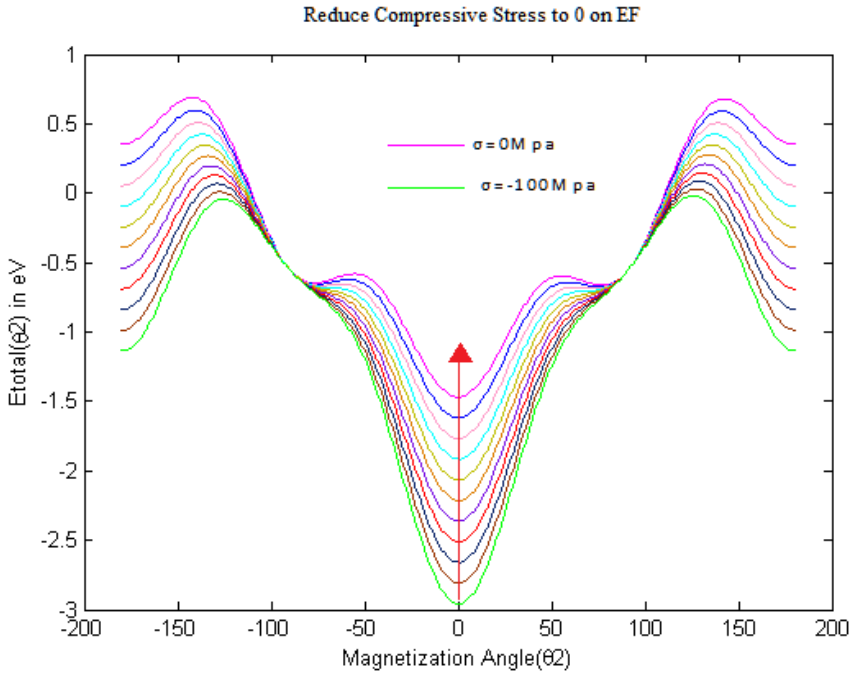

Fig5.6(d)

Fig.5.6 (a-d): Simulation of the output nanomagnet's (EF) energy as a function of the magnetization angle θ_2 of the output nanomagnet. The initial conditions used are input bits AB=01, CD=00, for which output EF=10; Fig.4a: Stage one of the stress cycle in which tensile stress(+ve)is applied along +45° direction on EF where the energy minimum occurs towards $+135^0$ and settles into $+115^0$. Fig. 4b: After relaxation of the stress on EF, the nearest energy minimum is at +90° direction. Fig. 4c: With increasing compressive stress (-ve), magnetization rotates towards $+45^0$ and settles at $+20^0$. Fig. 4d: Upon relaxation of compressive stress on EF, the nearest energy minimum is at 0°, and therefore the magnetization rotates and finally settles at that position.

5.8. Energy dissipation for switching

The value of d_{31} constant of PMN-PT piezoelectric is 1300 pm/v [5.70], accordingly it would require an electric field of 4 KV/cm. assuming maximum strain at PMN-PT layer is 500ppm, it can transfer maximum stress of 100MPa in the nanomagnet. Now the voltage generated due to the applied stress is governed by the eqn $v = (\sigma . t_{piezo}) / \gamma d_{31}$ -(5).

So for 40nm thickness a voltage pulse of ±16mv will be required to generate successive tension and compression stress cycle. The relative permittivity of PMN-PT layer is

1000[5.71], so for 100nm diameter capacitance of the PMN-PT layer is ≅1.75fF. The energy dissipated during charging of the capacitance abruptly with square wave pulse is ½ CV^2 for an event. So for four state event total energy of $2CV^2$ will be dissipated per gate operation. The total energy dissipation is ≅215kT and is considerably lower than conventional CMOS technology.

There is some additional internal power dissipation in the magnet caused by Gilbert damping constant. But it is comparatively negligible as long as switching frequency belongs to 100 MHz to 1 GHz [5.72].

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STRAINTRONICS-MAGNETIC TUNNELING JUNCTION BASED 3 INPUT UNIVERSAL LOGIC GATE (NOR) WITH HIGH EFFICIENCY

6.1 Introduction:

During the years, an interface of piezoelectricity and magnetostriction has been used in order to generate a magnetic field when the device is subject to an external electric voltage or vice versa [6.1-6.3]. This is achieved by combining a piezoelectric layer (Pmn-Pt) with a magnetostrictive layer so as to generate and transfer mechanical strain to the latter. Most of the researches are based on the change of magnetisation in the magnetostrictive layer due to magneto-electric effect by sensing a voltage change across piezoelectric as shown in Fig. 1a. This principle is widely used in sensor design. Recently, researches focus on the principle of using an applied voltage across piezoelectric to assist the flipping of the magnetization vector in a magnetostrictive layer in the desired direction [6.3-6.7]. This is the basis of the straintronics principle,

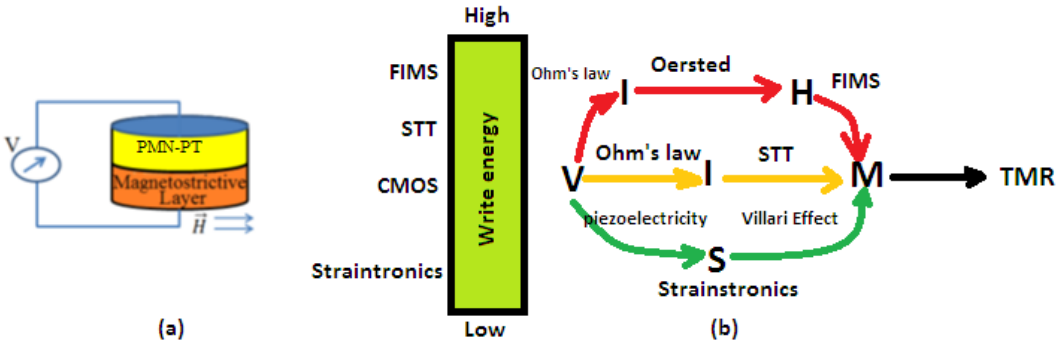


Fig. 6.1 – (a) schematic diagram of the magneto-electric effect; due to applied magnetic field, a voltage is detected across the device, (b) comparative diagram between straintronics, CMOS, FIMS and STTbased switching.

Where basically voltage controlled switching is performed to avoid high static currents like FIMS and STT based magnetic switching. The corresponding

diagrams are shown as in Fig.6.1 (a-b).In spite of being a charge based, CMOS devices dissipate less energy than FIMS and STT due to technological advancement of it.

Straintronics based logic gates differ from traditional gates as it can process and store information simultaneously. It provides minimum energy dissipation in designing of computer architecture by eliminating the need of refresh clock cycles. Non-volatile properties of these gates can improve the system reliability and eliminate the delay of a computer.

However the digital logic gates should followall the requirements as referred in [6.8-6.9]. For this reason proposed universal gate in [6.10-6.11] may not be suitable in all IC's. Moreover, all the non-volatile nanomagnetic based logic gates are supposed o be inferior than CMOS based logic in terms of energy-delay product. Straintronics based two inputs universal NOR gate with single magnet flipping have been described in previous chapter. However, in order to use straintronics effectively, piezoelectric needs to be interfaced with the MTJ. Moreover in a digital IC 3-input logic gates are preferred than the 2-input gates for simplification of the ckt [6.12]. In this section we thoroughly explore the merits of a 3-input NOR gate based on Piezoelectric-MTJ straintronics structure.

We will first discuss the principle of straintronics by analysing the process of magnetization flipping in the device. Next, the concept of various parameters like intrinsic and stress energies, energy barrier of a straintronics device will be introduced. Lastly, we will investigate the figure of merits in terms of Energy-Delay product of a 3-input NOR gate which is designed by interfacing PMN-PT piezoelectric with the magnetostrictive material (Cobalt). The proposed 3-input gate structure is based on principle of straintronics, which are very energy efficient as well as fast and hence can provide more functionality on a chip area.

6.2 Literature Survey

During the past few decades, several billion dollars have been invested in research to discover the new beyond CMOS logic devices as CMOS technology was inevitable to

be replaced by the new ones at nearly 100 nm technology nodes. A plenty of new devices like single electron transistors [6.13], quantum dots [6.14], nanowires [6.15], spin transistors [6.16], plasma transistors [6.17], and phonon devices [6.18] have been emerged due to outcome of this research. But they are lagging the versatile features of CMOS to replace it totally due to technological advancement during the so many years. A more scientific approach is to discover the new X technology which can be interfaced with the existing CMOS technology to accelerate the growth of VLSI chips according to demand of electronics industry. The main objective of CMOS+X technology are to overcome the limitation of CMOS devices which are: i) Volatility of charge based CMOS technology. So periodic refresh cycle is needed to dissipate extra power in CMOS based memory; ii)In nanoscale size CMOS's static leakage currents is predominant which can cause power dissipation even in idle condition and also posing difficulties in dense 3-D packaging of Ics; iii) CMOS's reliability decreases as technology node reduce [6.19] due to power and ground voltage fluctuations, static leakage current etc.; and iv) On-chip memory devices SRAM use 10 transistors per cell to minimise read error which are very large; This is the motivation behind the research to find out new CMOS+X technology to overcome the above obstacles. The magnetic-based logic and memory [6.20, 6.21] have energy advantages due to inherent data retention capability, the use of magnetic tunneling junction (MTJ), has been the topic of research in the past years. The potentiality of this technology can open new era of designing logic circuits and memory to overcome the barrier of CMOS-based technology.

Tunnel magneto resistance (TMR) in MTJ was first invented by Julliere in 1975 in Fe/GeO/Co (soft magnet/nonmagnetic/hard magnet) junction [6.22]. It was observed that the resistance across the MTJ is maximum at the antiparallel magnetization orientation of the two layers, while the low value is observed in the parallel orientation. These high and low resistance, denote the binary logics 0 and 1 in a logic circuit. Soon after this the principle of TMR was used to build magnetic random access memory (MRAM) [6.23-6.25]. It is theoretically proven that the switching energy limit of a charge based logic is $NkTln(1/p)$ where *N represents the* number of charge carriers, T is the operating temperature, and p is the bit error probability [6.20]. However, for a magnetic based logic this energy lowers to $kTln(1/p)$ due to the single domain magnetic coupling. Therefore, magnetic based

devices are expected to be N times more energy efficient than the charge-based devices.

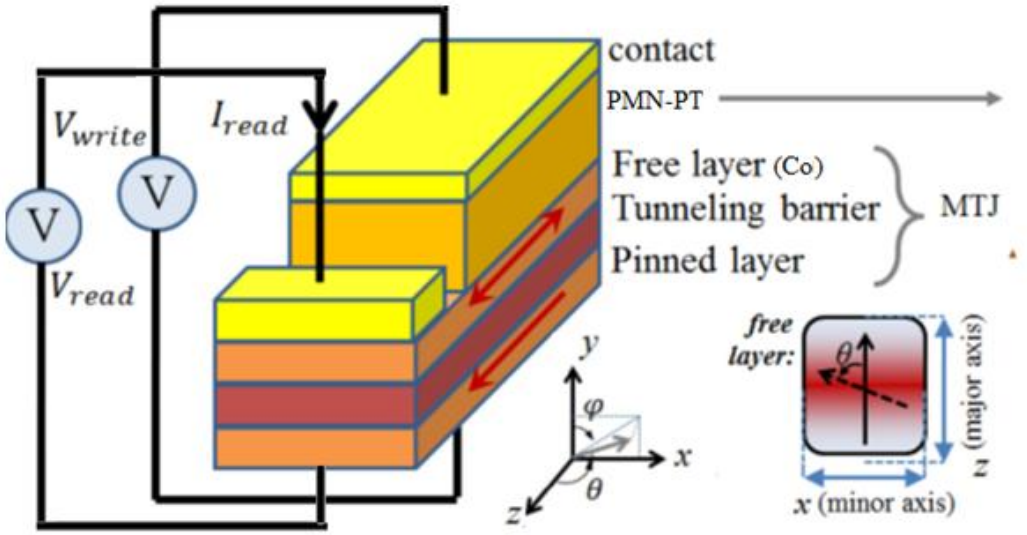
Two conventional methods for switching the magnetisation state of the MTJ are Field induced magnetization switching (FIMS)[6.26] and spin transfer torque (STT) [6.27-6.30] flipping. In FIMS an external magnetic field is used which is generated by a current flow through a nearby wire. This method consumes a energy. Due to the high current values, the energy efficiency of this method is very low. Moreover the device need to be wide and the MTJs are susceptible to inter-cell magnetic field interference. The spin transfer torque (STT) switching uses spin-polarized current flow through the device, which increases its scalability with CMOS technologies. Energy consumption is still high in STT.

There is a need to investigate alternative approaches to tackle the energy and reliability issues of the FIMS and STT. Recently electric-field-assisted switching of the MTJ [6.31-6.33] has been proposed. Although it is energy efficient at the interface of MgO/ CoFeBbut it still employs an external bidirectional magnetic field for switching. Generating this field can again be power consuming, produces complicated design procedures and needs more space and might lead to inter-field interferences, leading to further scaling. Straintronics based switching is proposed recently [6.34-6.38] as an alternative energy efficient method to switch the state of the MTJ. In straintronics the voltage based switching is achieved instead of static current which makes the straintronics device highly energy efficient than any nanomagnetic logic device. It is also observed that the energy-speed trade-off of the straintronics MTJ is 10^5times better than its STT peer.[6.39]

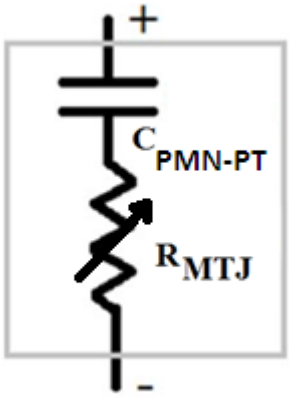
6.3 THEORY

6.3.1The straintronics-based magnetic tunneling junction

Straintronics is designed with the interface of a magnetostrictive material with a piezoelectric layer PMN-PT. An applied voltage cum stress can rotate the magnetization vector and thus changes the state of the nanomagnet. In recent paper this method of switching of magnetization vector in single magnet using this approach has been published [6.34].



(a)



(b)

Fig.6.2(a): Straintronics-MTJ (STJ) based general structure. (b) Equivalent ckt. of STJ

The general structure of a STJ comprising a piezoelectric material interfacing with a free layer of the MTJ. The digital storage MTJ is formed by placing a tunnel barrier and a free layer below the small pinned layer. The MTJ acts as a variable resistance. The PMN-PT, placed on top of the MTJ, can behave as a parallel plate capacitance. The fringing effects are negligible due to the large plane interface of the piezoelectric and the free layer. Hence, the STJ can be described by an equivalent electrical model of a resistance-capacitance (RC) circuit. The piezoelectric in the STJ is comprised of Lead-magnesium–niobate-lead-titanate ($Pb(Mg1/3Nb_2/3)O_3$– $PbTiO_3$ or PMN-PT).

Straintronics device as depicted in Fig.6.2(a) is a combination of 4-layers beside contact layer. The first layer is a thicker layer of piezoelectric PMN-PT. It is more than 4 times thicker than nanomagnetic layer. The second layer is a thin layer of soft magnet, whose magnetization will rotate and decide the digital logic '0'or logic '1' state. The next layer is comprised of very thin layer of insulator MgO (1 nm) required for Tunnelling Magneto Resistance (TMR). The bottom layer is a Synthetic Antiferromagnet (SAF) with very high anisotropy energy. It is permanently magnetized in one direction say, –Z direction of the easy axis. For digital logic '1', TMR is high and magnetization of soft or free layer remains anti-parallel(AP) with the magnetization of hard or fixed layer and for digital logic '0' it remains parallel (P) with the magnetization of fixed layer. The device is a cylindrical ellipse with its minor and major axis lie on Z-X plane in Z and X direction respectively as shown in Fig.6.2(a). The equivalent electrical circuit of the STR cell is shown in fig.6.2(b).

6.3.2 Straintonics principle

In the absence of any external voltage, the free layer's magnetization vector settles along the major axis due to the energy minimum. The magnetization or digital logic state of the device (P or AP) can be detected by sending a current through the MTJ and sensing the resistance level as high(1) or low(0).

An applied voltage across the PMN-PT generates an electric field$E=V_a/d$, where $Va$is the supply voltage, and $d$is the thickness of the PMN-PT.

MTJ and PMN-PT can be modelled in electrical circuit as a variable resistance, and a parallel plate capacitance. The MTJ's conductance is defined as [6.35]:

$$R_{MTJ} = [R_{min} + \frac{1}{2}(R_{\max} - R_{\min}) \times (1 - \cos\theta)]$$

where, G_P is the high conductance in low resistance state, in which free and fixed layers have parallel magnetization orientation; G_{AP} is the low conductance in high resistance state, in which they have parallel orientation; and θ is the angle of the magnetization vector of the free layer with respect to the major axis.

The relationship between the *E*-field and its resulting strain is related by the modified Hooke's law for piezoelectricity: $\{S\}=s\{\mathrm{p}\}+d^t\{E\}$

Where, *s* is the compliance matrix, p is stress, and *d*is the 3×3 piezoelectric effect's tensor. Here PMN-PT is used as the piezoelectric layer, in which the d31 coefficient converts the electric field along the *x*-axis to a strain in the *y*-*z* plane.

The Piezoelectric is chosen to be four times thicker than the free nano-magnet (NM) with a large plane interface to assure that the strain can almost completely transfer to the NM.

6.3.3. Stress anisotropy energy in the NM

In the absence of any stress, the intrinsic magnetic energy of the device is mainly dominated by shape anisotropy and uniaxial anisotropy. The total intrinsic magnetic energy of the free layer is given by:

Total energy of a nanomagnet can be obtained by the Energy equation

$$E = E_{Sh} + E_u + E_\sigma \quad \text{.....(6.1)}$$

E_{sh}=shape anisotropy energy = $$\frac{\mu_0}{2} V M_s^2 \begin{bmatrix} N_z Cos^2\varphi(t) Sin^2\theta(t) + N_x Sin^2\varphi(t) \\ Sin^2\theta(t) + N_y Cos^2\theta(t) \end{bmatrix}$$

$$= \frac{\mu_0}{2} V M_s^2 \times N_{Sh}(\theta, \Phi) \quad \text{.....(6.2)}$$

where, θ(t)=Polar angle, ϕ(t)=azimuthal angle,

N_x,N_y &N_z=De magnetization factor along X, Y & Z direction respectievely.

V=volume of the nanomagnet

E_u=crystal anisotropy energy = $[K_u Sin^2\theta(t)]V$.....(6.3)

where K_u= uniaxial crystal anisotropy constant.

E_o=stress anisotropy energy= $\frac{3}{2}\lambda_s\sigma V[1-\sin^2\theta(t)\sin^2\varphi(t)]$.....(6.4)

where λ_s =magnetostriction co-efficient

= 20ppm & σ = applied stress on the nanomagnet.

$\theta(t)$ = angle between the magnetisation vector with the major axis

(θ,φ) = De magnetization factor .In fact, Nscan be defined as

$(\theta,\varphi) = N_X Sin^2\theta Sin^2\varphi + N_Y Cos^2\theta + N_Z Sin^2\theta Cos^2\varphi$ ---------- (6.5)

Which assumes its maximum and minimum along the y-axis and z-axis, respectively, and has a saddle point along the x-axis. The parameters Nx, Ny, and $Nz$are shape dependent parameters.

Typically, for a thin layer, we have: $Nz>>Ny$,x. When the device is a cylindrical rectangular, these parameters are defined by the following expressions, in which a, b, and $l$are the magnet's major axis, minor axis, and thickness:

$$N_Z = \frac{\Pi}{4}\left(\frac{l}{a}\right)[1-\frac{1}{4}(\frac{a-b}{a})-\frac{3}{16}(\frac{a-b}{a})^2] \text{----------(6.6)}$$

$$N_X = \frac{\Pi}{4}\left(\frac{l}{a}\right)[1+\frac{5}{4}(\frac{a-b}{a})+\frac{21}{16}(\frac{a-b}{a})^2] \text{----------(6.7)}$$

$$N_Y = 1-(N_Z+N_X) \text{----------(6.8)}$$

The magnetic energy level of free layer is therefore, a function of the orientation of magnetization vector, which is shown in Fig.6.2 (a). Magnetization vector mainly stays in the z-x plane due to the shape anisotropy energy. Furthermore, within this plane, an energy barrier exists between the minor axis and the major axis of the

device, as demonstrated in Fig. 6.3 (at Stress =*0*). This makes the preferred orientations of the free layer's magnetization vector orientations like parallel or anti parallel with the pinned layer in the absence of an external stress. Here the energy barrier is material dependent and among the common magnetostrictive materials, Nickel shows the lowest energy barrier due to its low Msvalue which is easily perturbed by noise while Galfenol has the highest level of energy barrier in which energy dissipation is very high. To balance this cobalt has been chosen as magnetostrictive material.

When a stress, σ, is applied into the magnetostrictive material, the stress anisotropy energy density, $E\sigma$, due to the Villari effect, is given by the eqn.(6.4).

At the time, when applied stress σ=0, the magnetization vector tends to retain its orientation along the major axis (P orientation state or AP orientation state) due to the energy barrier. As we apply voltage across the PMN-PT, it generates an electric field that converts into strain, 'S', where S = (ΔL/L) and ΔL = change of the length L. This physical change of length in PMN-PT layer transfers a stressσ (mechanical energy) to the magnet. Now, depending on the polarity of the input voltage, an energy minimum is created along minor X-axis due to Villari-effect as in fig.(4). This will allow the magnetization to rotate towards minor X-axis i.e. in energy minimum position. Whenever magnetization rotates towards minor axis, then after judicial withdrawal of stress, magnetization can settle towards opposite state.

The potential profile of a straintronics MTJ based 3-input NOR gate is shown in Fig.6.3 and its corresponding logic in table 6.1.The plot shows that the anisotropy energy barrier of a nanomagnet can be inverted by the applied voltages (stress) at the input terminal, so that the new minimum energy position comes at minor axis ($\theta=90^0$)from major axis($\theta=0^0$ or 180).

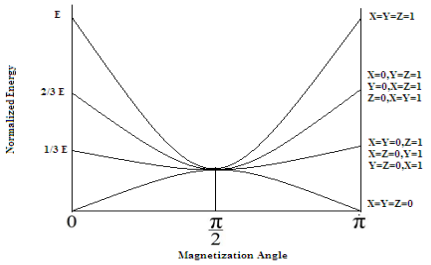


Fig.6.3: Variation of Energy profile of a 3 input NOR Gate with the applying voltage or stress.

Now, for any one or more combination of input voltage, if the input layer voltages is greater than critical voltage then the switching of soft layer will be occurred to get our desired logic operation as shown in logic table 1.The dimension of the cylindrical elliptical nanomagnet is taken as (120×80×6)nm, so that Barkhausen effect is negligible and it can behave as a single domain nanomagnet. PMN-PT is taken as piezoelectric layer and the E field along y-axis, converted to strain in z-x plain through d_{31} coefficient. The anisotropy energy barrier of this nanomagnet is 95kT.In this energy barrier magnet's spontaneous switching error probability becomes e^{-95}, which is very low. Hence the retention time of the magnet for 1THz frequency will be = $2.77x10^{41}$ years, which is almost non-volatile.

Table 6.1.Logic Table.

XYZ	TMR	OUT	Switches?
000	H	1	NO
001	L	0	YES
010	L	0	YES
011	L	0	YES
100	L	0	YES
101	L	0	YES
110	L	0	YES
111	L	0	YES

Cobalt is taken as the ferromagnetic free layer for our simulations. The STJ has the shape of an ellipse, like in Fig. 6.1, having major and minor axes of a=120nm and b=80 nm, respectively. The thickness ratio of the PMN-PT to the free layer is at least 4:1, which can provide a large plane interface in order to ensure a perfect transfer of strain. The values of a and $b$are chosen such that the free layer acts as a single-domain nanomagnet [6.36]. High endurance of the PMN-PT can be achieved since the applied pulse across the piezoelectric is unipolar [6.37].

6.4 IMPLEMENTATION

In this work a 3- input NOR gate is designed as depicted in Fig.6.4. Here 3-inputs A, B and C, are applied at the piezoelectric layer, which can generate stress for each of the inputs. The fourth input terminal, 'Set' is required to switch or set the soft layer antiparallel to that of the hard layer, and it is required only when the magneto resistance of the MTJ is low. By taking the value of read current the high or low state of the magneto resistance can be measured.

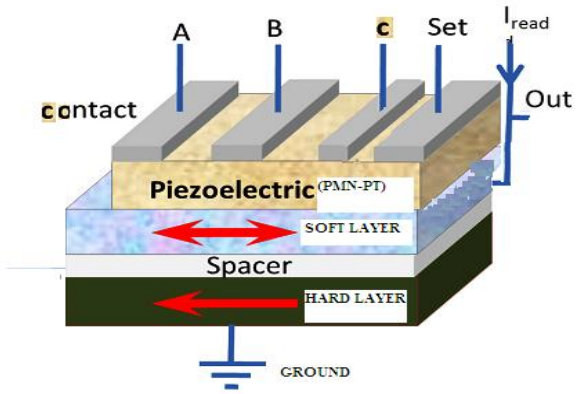


Fig.6.4. Proposed structure of 3- input NOR Gate.

Here, PMN-PT is taken as piezoelectric material which is the top layer and its thickness is 50nm.The next layer is ferromagnetic layer of cobalt of dimension (120×80×6) nm. The bottom layer is a synthetic anti ferromagnet with large anisotropy energy barrier, which is permanently magnetized in the left direction of the easy axis. The layer between ferromagnet and anti ferromagnet is a spacer layer of MgO of thickness 1 nm. It is used for tunneling magneto resistance (TMR) in MTJ structure.

6.5 RESULT AN DISCUSSION

It can be proved from magnetic susceptibility model that critical voltage needed for switching the magnetization of the nanomagnet is [6.38]

$$Vc= \frac{\left(\mu_0/2 \quad Ms^2\left(N_x - N_y\right)+K_u\right)t_{PMN-PT}}{3/2\lambda_s \gamma d_{31}} \quad \text{.....(6.9)}$$

Where t_{PMN-PT} is the thickness of piezoelectric layer, γ is the Young's modulus of the soft magnet (cobalt) = 2.09×10^{11}Pa.d_{31} is the piezoelectric effect coefficient =-3000pm/V (6.39), K_u=uniaxial anisotropy coefficient=450J/m^3 for Cobalt [6.38).

Therefore, for the proposed magnet the critical voltage for filliping the magnetization is 41.4mV.

Now any voltage above the critical voltage will rotate the magnetization vector towards minor axis. The desired result will be obtained if the applied stress can be withdrawn within the time period of successful pulse width.

Capacitance generated at piezoelectric surface is C=1.7fF for the proposed dimension.

For our simulation input is taken as 0.1V, so that sufficient noise margin can be achieved during the application of stress.

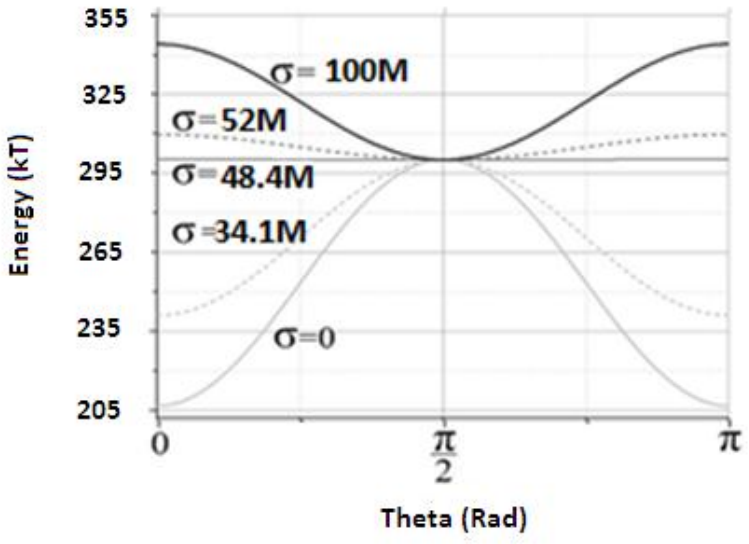


Fig. 6.5 (a) Energy profile of the proposed nanomagnet with the application of stress.

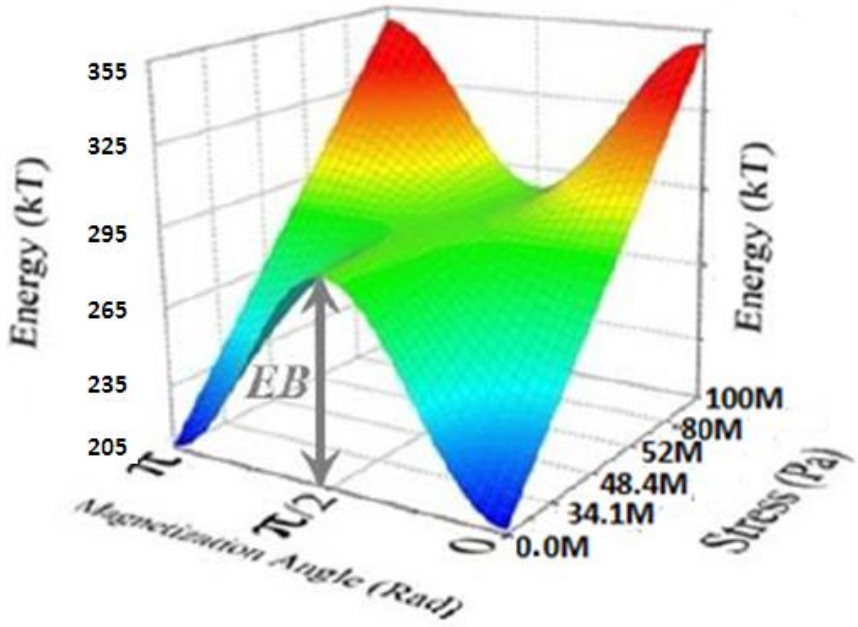


Fig. 6.5 (b) 3-D simulation view of the Energy profile of the proposed nanomagnet with the applied stress.

From the energy diagram of Fig.6.5, it is understood that energy barrier of the nanomagnet decreases and becomes zero with the application of applied stress increases at the level of critical stress (σ=48.4M) [Because at this level of applied stress, stress anisotropy energy ($\frac{3}{2}\lambda_s \sigma V$) becomes equal to the barrier energy as depicted in the fig 6.5. (a) & (c)].

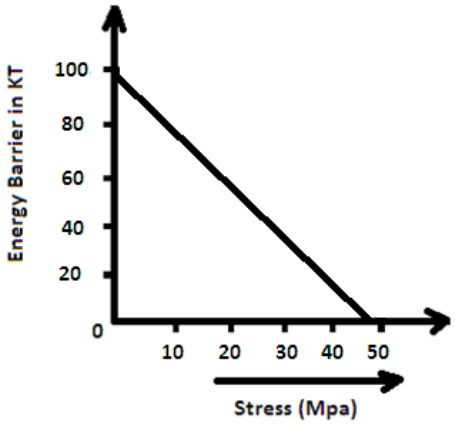


Fig.6.5(c). Linear variation of energy barrier with the applied stress

Magnetization dynamic of a nanomagnet can be best described by LLG equation:

$$\frac{\overrightarrow{dM}}{dt} = K\left(\overrightarrow{M}\times\overrightarrow{H}\right) + \frac{K\alpha}{M_s}\left(\overrightarrow{M}\times\overrightarrow{H}\right)\times M \quad \text{.....(6.10)}$$

Where K= $\frac{\gamma_0}{1+\alpha^2}$, α is the Gilbert Damping factor and γ_0 being the gyromagnetic ratio,

H= $\frac{1}{\mu_0 V M_s}(\overrightarrow{\partial E}/\overrightarrow{\partial m})$ = effective field due to the total magnetic energy

Simplifying the above eqn, in terms of spherical coordinates with $\theta$and φdefined in Fig 6.2 of, we have:

$$\frac{d\theta}{dt} = K(H\varphi + \alpha H\theta) \quad \text{.....(6.11)}$$

$$\frac{d\varphi}{dt} = \frac{K}{Sin\theta}(\alpha H\varphi - H\theta) \quad \text{.....(6.12)}$$

where, $H\varphi$and $H\theta$will be expressed as:

$H\varphi$=−

$$\frac{1}{\mu_0 V M_s}.\frac{1}{\sin\theta}\left(\frac{dE}{d\varphi}\right) \quad \text{.....(6.13)}$$

$$H\theta = -\frac{1}{\mu_0 V M_S}\left(\frac{dE}{d\theta}\right) \quad \text{.....(6.14)}$$

By combining the energies and incorporating the effective fields together, we have:

$H\varphi$=−A

$$[\frac{\mu_0}{2}M_s{}^2V(N_z - N_x) + \frac{3}{2}\lambda_s\sigma V]\sin\theta\sin 2\varphi \quad \text{.....(6.15)}$$

$$\mathrm{H}_\theta = -\mathrm{A}[\frac{\mu_0}{2}M_s{}^2V(N_x\sin^2\varphi + N_z\cos^2\varphi - N_y) - \frac{3}{2}\lambda_s\sigma V\sin^2\varphi + K_u V]\sin 2\theta \quad \text{.....(6.16)}$$

Where A= $\frac{1}{\mu_0 V M_s}$

The numerical model is obtained by solving eqns.(11) and (12) into (15) and (16), by the software. Hence, the accuracy of the LLG model comes at the price of the lower speed of simulation.

Although the switching time of magnetization vector can be calculated from LLG equation, but it requires rigorous mathematical computation which is very time consuming. A simplified dynamic model by taking second degree control equation

for damping (6) can be used to analysis the magnetization dynamic of the system by the equation is,

$$\frac{d^2\theta}{dt^2}+2\zeta\omega_0\frac{d\theta}{dt}+\omega_0^2\theta=0 \quad \text{.....(6.17)}$$

where ζ = general damping factor =

$$\frac{\alpha\left(M1+M2\right)}{\sqrt{4\left(1+\alpha^2\right)M_1M_2-\alpha^2\left(M1+M2\right)^2}},$$

ω_0 = natural frequency of oscillation =

$$\frac{\sqrt{4\left(1+\alpha^2\right)M_1M_2-\alpha^2\left(M1+M2\right)^2}}{2} \quad \text{.....(6.18)}$$

ω_d = damped frequency of oscillation = $\omega_0\sqrt{1-\zeta^2}$ ..... (6.19)

Values of M_1& M_2 depend on material properties and applied stress

By solving the equation it can be obtained that

$$\theta\left(t\right)=\frac{\Pi}{2}-\frac{\Pi}{2}e^{-\zeta\omega_0 t}\cos(\omega_d t) \quad \text{..... (6.20)}$$

which is depicted in Fig.6.6. From the graph it can be interpreted that minimum delay time for magnetization to align at minor axis is =0.7ns. Now, relaxation delay for cobalt to settle at the final stage after withdrawal of stress is approx. 2.06ns [6.38].

So total delay time of magnetization to settle at opposite state τ =2.76ns.

Now energy delay product =Eτ=24×10^{-27}Js, which is less than CMOS based logic gate.

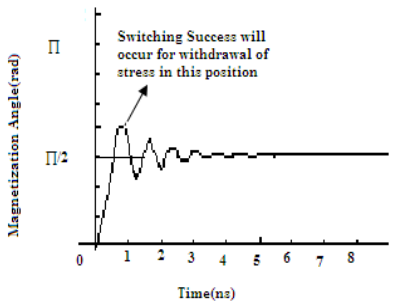


Fig. 6.6.Switching graph of magnetization vector with respect to time with 0.1V input.

6.6.1. Realization of STJ-MOS based 3 input NOR Gate

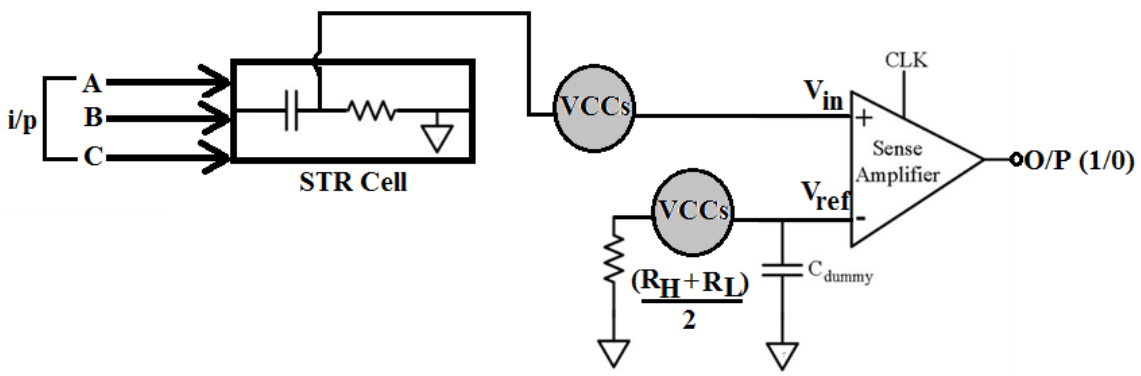


Fig. 6.7.STJ-MOS based 3 input NOR gate

Fig. 6.7 shows the practical realisation of a 3 input STJ-MOS based NOR gate. Here one CMOS based sense amplifier is used for obtaining the output. Input voltage (V_{in}) of the amplifier is generated by flowing current from a NMOS based voltage controlled current source through STR cell. The resistance of the STR cell is high (R_H) or low (R_L) depending upon the antiparallel or parallel orientation of the soft magnet. Reference voltage (V_{ref}) is generated by passing current through a reference resistance ($R_{ref}= R_H+ R_L/2$). C_{dummy} is used for the clock signal used for the amplifier. By using dynamic latched topology the amplifier can dissipate 24fj with 1V supply input and 106 ps delay [6.40]. So it is neither energy nor a speed blockage for the system.

Due to non-volatile property of STR cell this type of device can be used to process logic bit as well as to build basic memory element.

6.6.2. Performance Comparison with CMOS Based Device

Here ultra-low power dissipation occurs due to absence of physical current flow during switching. During the flipping of a single bit power dissipation can be estimated in the order of Auto Joule ($E = \frac{1}{2}CV^2$, where c=1.7 fF, V=0.1V). Where as in modern CMOS based device it is of the order of Pico Joule only [6.41]. Moreover switching time for flipping a bit in Straintronics based device is in the order of Nano second with error probability of 10^{-6} (6.42), which is also comparable to CMOS device.

Table .6.2. Performance comparison with CMOS

Device Type	Power Dissipation	Propagation delay	Switchingsuccess probability
CMOS	pJ	12ns	100%
Straintronics	aJ	2.76ns	99.99%

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CONCLUDING REMARKS AND FUTURE SCOPE

7.1. Concluding Remarks

The present thesis contains the theoretical investigations of Performance improvement of low dimensional devices and explores some of their applications. Further the present thesis also provides the principle, device details and applications of power efficient devices called spintronic devices. The outcome of these studies is summed up here in this chapter. These results may provide fundamental information in the development of future devices in the low dimensional structures.

A novel device structure namely High-K Dual Material Tri-gate SON MOSFET has been proposed in **Chapter 2.** The present work highlights the effect of Gate work function engineering and High k incorporation in a tri-gate SON MOSFET. The High-K technology is well-known for reducing the gate-oxide leakages and hence highly improves the Subthreshold characteristics of the device. To retain the advantages of the SON technology, we have considered SON configuration in our proposed model. The results obtained from analytical modeling are verified using simulation data obtained from ATLAS. The proposed model is found to exhibit an upgraded immunity towards the various short channel effects like DIBL, HCE and Subthreshold slope characteristics. In our model we have observed that best subthreshhold slope i.e 80 mv/decade can be obtained in the channel length of less than 30 nm with the use of high K dielectric TiO_2. Also a comparative study of the surface potential and electric field features has been carried out in both DMTG High K SON MOSFET and SMTG High K SON MOSFET. Our proposed model is found to possess reduction of electric field about 1 MV/cm compared to its SMTG counterpart. The analytical and simulated values validate our proposed model. Due to these upgraded performance DMTG SON is considered as a promising device technology for the next generation ULSI era.

Chapter 3 deals with a newly developed promising technology called spintronics. The Science and Technology of manipulating the spin degree of freedom of a single charge carrier to encode, process and deliver information is called spintronics. The

main objective of this novel technology is the device miniaturization to reduce power consumption, and to improve device speed. An RFID system with Anti-collision Binary-tree scheme is implemented here using single spin logic. The designed RFID system based on spin-polarized electrons would be very fast, consume very low power and inexpensive due to ultra-dense integration. Comparisons table in Chapter 3 depicted delay and power consumption of the various semiconductor technology are provided here to substantiate our model. From the table it appears that the spin based circuits are at least more than 12000 times faster compared to CMOS/TTL circuits and more than 6 times faster compared to SED based similar circuits. It also dissipates 2 pw power which is much lower compare to mw and μw level of power dissipation for CMOS/TTL & SED based circuits. So considering the modern advancement of the manufacturing technology and nano-lithography, we can expect that for survival of fittest, this spintronic technology is going to revolutionize the world of microelectronic technology. However, viable spintronic devices require efficient injection of spin polarized electrons into nonmagnetic materials, minimization of the spin dephesing, ability of spin control during transport and finally efficient spin electron. Although some of these requirements have been successfully demonstrated, spintronics devices still await an experimental confirm of the predicted theoretical expectation.

Chapter 4 deals with a new model of straintronics with using the Magnetostrictive property of the material. Here magnetoelastic property of the piezoelectric (PZT) is used along with the magnetostrictive property of the material (Terfenol-D). Biaxial magnetocrystalline anisotropy property of the Terfenol-D is used to devise the basic logic gates. It has four possible stable states in magnetization orientation which is known as easy axis. By using this property the authors theoretically examine the possibility of low power universal NAND gates. A linear array of 3 nanomagnets is used in which peripheral magnets are encoded with input bits (AB & CD) and the central magnet's magnetization orientations are encoded with output bits (EF). Numerical simulation's result confirms that the four-state out-put bit is the Boolean NAND function of the input bits when the array reaches its stable state. An alternating voltage pulse of amplitude ±0.111 volt applied to the piezoelectric layer of the output nanomagnet generating alternating tensile and compressive stress in its magnetostrictive layer. This stress along with the dipole interaction between the

magnets and the static bias field drives the output magnets to the correct ground state which is the NAND function of the inputs. For the system the gate operation is executed by dissipating only 4.2×10^{-7} J of energy. With such low amount of energy dissipation logic system can be run by harvesting energy from the local surroundings and can be very useful for future nanodevices, especially for medical implanting devices.

In **chapter 5** the candidate theoretically analyzed the possibility of straintronics based ultra low power 4-state NOR gate by using three numbers of composite multiferroics based nanomagnets (PMN-PT/Ni) placed in a linear array. In some logic circuit NOR gate is preferred as it requires at least one input being 'ON' to make the output 'OFF', where NAND requires both the inputs to be 'ON'. So average energy dissipation will be less for the NOR switch. This chapter discusses the design methodology of straintronics based 4 state universal (NOR) gate which can be used to process digital information as well as basic memory element. Each nanomagnet's magnetization orientation can produce 4-state condition. The peripheral magnets are encoded with input bits, and the central magnet's magnetization orientation is encoded with output bits. By enlightening the multiferroics functionality with introducing biaxial magneto crystalline anisotropy in the magnetostrictive layer, a possibility of making four-state NOR can gate be implemented by the linear array of three nanomagnets. Numerical simulation result confirms that an alternating voltage pulse of ±16 mV is required to apply at the piezoelectric layer of the magnets for complete switching of state. Here desired combination of the Input bits, drives the output into the global ground state which is the NOR function of the input bits. In our model single crystal PMN-Pt is taken as piezoelectric material which is more sensitive and gate operation is executed with ultra low energy dissipation of ≈215 kT which is less dissipative than the PZT based Gates. This type of NML not only increase the logic density by two fold over the conventional 2 states, but also act as an associative memory element because of its four distinct minima. It can also be implemented in non-Boolean application such as image recognition and processing. So these types of straintronics device can face the challenges for miniaturization of devices. However, there are some challenges associated to build up straintronics switching. They are fabrication challenges,

difficulties in retaining piezoelectricity in small scales, to generate uniaxial stress and to transfer strain accordingly.

Chapter 6 deals with Straintronics-MTJ based basic device, where MTJ based NML gates can process the Boolean operation as well as store the output data in the form of magnetisation state. Therefore, it can be used as a both logic circuits as well as basic memory elements. Straintronics combined with MTJ make the IC ubiquitous for convenient access of In/Out or Read/Write data. The proposed 3 input NML based NOR gate comprised of a single domain ferromagnet, magneto elastically coupled to the piezoelectric layer PMN-PT with the required MTJ structure. The non-volatile voltage controlled logic gate can fulfill all the logic requirements of a gate, while dissipating ultra-low energy during switching of bits, with very fast response including high dense logic functionality per unit area. In our model the proposed gate has an energy delay product of 24×10^{-30} Js which is much better than CMOS based gates. Although the error probability in CMOS gate is less than the straintronics based device, but it is volatile. So STR –MTJ based device can be used to build-up as a basic building block for basic gates as well as non-volatile memories with a high frequencies .Cobalt can be the perfect material for this case due to their fast response and tolerable noise margin. Furthermore, due to low applied voltages, the STR-MTJ allows digital logic gates to operate synchronously with FIMS or STT based logic gates. The proposed 3 input gate structure is based on principle of straintronics, which are very energy efficient as well as fast and hence can provide more functionality on a chip area.

7.2. Future Scope

The research work of us has enlightened about some possible movement and improvement of extended CMOS as well as beyond CMOS technology as a future nanoelectronics application. However there is always some room for improvement with the advancement of technology. Further research on future aspect can be taken as follows:

- DMTG SON MOSFET is a promising device in future application with improved performance over existing MOS technology. However, prior to fabrication CMOS circuit design necessitates the accurate electrical modeling

of non-classical devices for predicting the behavior of various electrical parameters.

This requires exact solution of the basic semiconductor equation i.e., Poisson's equation, continuity equation, current transport equation and other related equations through accurate numerical analysis. To get the exact solution is difficult for nano-scale devices where 3- dimensional effects are to be accounted in modeling. Thus, further research to obtain an accurate analytical model can be taken. Furthermore, in nano scale regime, the process variation has also major impact on the device behavior.

- Spintronics along with straintronics based research includes ultra large-scale and high throughput solution based processing for low- cost devices with possible room temperature operation and compatible with existing technology, which will make these circuits a potential candidate for the future emerging applications.