AN ALTERNATIVE STUDIES ON ALL OPTICAL FREQUENCY ENCODED DIBIT BASED DIGITAL CIRCUITS USING REFLECTED SEMICONDUCTOR OPTICAL AMPLIFIER AND ADD/DROP MULTIPLEXER

THESIS SUBMITTED BY

BITAN GHOSH

DOCTOR OF PHILOSOPHY (ENGINEERING)

DEPARTMENT OF INSTRUMENTATION & ELECTRONICS ENGINEERING
JADAVPUR UNIVERSITY
SALT LAKE CAMPUS, KOLKATA - 700106,
WEST BENGAL, INDIA
YEAR 2025

Dedicated to……

My Parents, Wife and Daughter

JADAVPUR UNIVERSITY
SALTLAKE CAMPUS
KOLKATA-700106, INDIA

INDEX No.- 98/22/E

Title of the thesis:

AN ALTERNATIVE STUDIES ON ALL OPTICAL FREQUENCY ENCODED DIBIT BASED DIGITAL CIRCUITS USING REFLECTED SEMICONDUCTOR OPTICAL AMPLIFIER AND ADD/DROP MULTIPLEXER

Name, Designation & Institution of the Supervisors:

Prof. Ardhendu Ghoshal, Professor,
Department of Instrumentation & Electronics Engineering,
Jadavpur University, Saltlake Campus,
Kolkata - 700106, West Bengal, India.

&

Dr. Partha Pratim Sarkar,
Assistant Professor, ECE Department, UIT,
The University of Burdwan,
Burdwan - 713104, West Bengal, India.

List of Publications:

Journal Publications:

1. **Bitan Ghosh**, Partha Pratim Sarkar and Prof. Ardhendu Ghoshal "Design of dibit based all optical frequency encoded controlled full subtractor using optical switches." *Journal of Optics* 53.1 (2024): 610-621.
2. **Bitan Ghosh** and Partha Pratim Sarkar "Simulative study of all-optical frequency encoded dibit-based controlled multiplexer and de-multiplexer using optical switches." *Journal of Optics* 48.3 (2019): 365-374.
3. Smita Hazra, **Bitan Ghosh** and Partha Pratim Sarkar "Alternative approach to design all-optical frequency-encoded D and T flip-flops using semiconductor optical amplifier." *Journal of Optics* 48.3 (2019): 375-383.
4. **Bitan Ghosh**, Niladri Halder, Dibyendu Roy and Partha Pratim Sarkar "An alternative approach to realize all optical frequency encoded integrated AND-OR logic gate with control input using optical switches and its simulative verification." *International Journal of Computer Sciences and Engineering* 07.spcl01 (2019): 88-93.
5. **Bitan Ghosh**, Partha Pratim Sarkar and Sourangshu Mukhopadhyay "A novel approach to realize of all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches with simulated verification." *Optics and Spectroscopy* 124.3 (2018): 337-342.
6. Partha Pratim Sarkar, **Bitan Ghosh**, Sankar Narayan Patra and Sourangshu Mukhopadhyay "A new scheme of an all optical frequency encoded dibit based latch with its simulated result." *Journal of Optical Technology* 84.9 (2017): 631-634.
7. Partha Pratim Sarkar, **Bitan Ghosh**, and Sankar Narayan Patra "Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using

a reflective semiconductor optical amplifier and an add/drop multiplexer." *Journal of Optical Technology* 83.4 (2016): 257-262.

Book Chapter:

1. "*Simulative approach to realize all optical-frequency-encoded dibit-based integrated logic gates: controlled and/or logic gates by optical switches.*" (Chapter 7, Pages 142-163) By **Bitan Ghosh** and Dr. Partha Pratim Sarkar in **Contemporary Developments in High-Frequency Photonic Devices (1st Edition, 2019**, **Hershey, PA: IGI Global Publisher)**.

Conference Papers/ Presentations:

1. *"A novel approach to design all optical frequency encoded digital full adder using reflected semiconductor optical amplifier and add/drop multiplexer."* By Smita Hazra, **Bitan Ghosh**, Dibyendu Roy, Niladri Halder, Sayanananda Sengupta, Dr. Jishan Mehedi & Dr. Partha Pratim Sarkar, in **1st International Conference on Recent Trends on Electronics & Computer Science (ICRTECS 2019)**, at NIT Silchar, Assam-788010, on 18th -19th March, 2019.
2. *"An alternative approach to realize all optical frequency encoded integrated AND-OR logic gate with control input using optical switches and its simulative verification."* By **Bitan Ghosh**, Smita Hazra, Niladri Halder, Dibyendu Roy, Partha Pratim Sarkar, in **1st International Conference on Innovations in Computer Science(ICICS-2018)**, at Computer Science Department, The University of Burdwan, West Bengal – 713104, on 21st – 22nd December, 2018.
3. *"New scheme of all optical frequency encoded dibit based de-multiplexer with simulated verification."* By **Bitan Ghosh**, Partha Pratim Sarkar, Smita Hazra, Sourangshu Mukhopadhyay and Sankar Narayan Patra, in **International Conference**

on Modeling, Computing and Technological Innovations (ICMCTI-2017), at UIT, The University of Burdwan, West Bengal – 713104, on 23-25th March, 2017.

4. *“A novel approach to realize of all optical frequency encoded dibit based multiplexer using optical switches.”* By **Bitan Ghosh**, Partha Pratim Sarkar, Smita Hazra, Sourangshu Mukhopadhyay and Sankar Narayan Patra, in **International Conference on Modeling, Computing and Technological Innovations (ICMCTI-2017)**, at UIT, The University of Burdwan, West Bengal – 713104, on 23-25th March, 2017.
5. *“Realization of all optical frequency encoded dibit based XOR and XNOR logic gates using RSOA with MATLAB verification”* By **Bitan Ghosh**, Partha Pratim Sarkar, Smita Hazra, Subhendu Biswas, Sourangshu Mukhopadhyay and Sankar Narayan Patra, on **International Conference on Applications of Mathematics to Nonlinear Sciences (AMNS-2016)**, at Association of Nepalese Mathematicians in America and Nepal Mathematical Society; Department of Mathematics, Tribhuvan University and Mathematics Group, Department of Natural Sciences, Kathmandu University, Kathmandu, Nepal, INDIA, on 26th-29th May, 2016.
6. “*Realization of all optical frequency encoded dibit based OR and NOR logic gates with simulated verification.”* By Partha Pratim Sarkar, **Bitan Ghosh**, Smita Hazra, Sankar Narayan Patra and Sourangshu Mukhopadhyay, in **International Conference on Advancement of Computer Communication and Electrical Technology (ACCET-2016)**, at MCET, West Bengal – 742102, on 21st – 22nd October, 2016, online published by **CRC Press/ Balkema, Taylor & Francis Group, 2017**.
7. *“An alternative approach of all optical frequency encoded DIBIT based latch along with simulated verification.”* By Partha Pratim Sarkar, **Bitan Ghosh**, Sankar Narayan Patra and Sourangshu Mukhopadhyay, in **International Conference on Computational Science and Engineering (ICCSE 2016)**, at RCC-IIT, Kolkata,

West Bengal - 700015, on 4th - 6th October 2016, online published by **CRC Press/ Balkema, Taylor & Francis Group, 2017**.

8. *"A new scheme of all optical dibit AND logic and NAND logic gate using reflected semiconductor optical amplifier and add/drop multiplexer*." By **Bitan Ghosh**, Partha Pratim Sarkar and Sourangshu Mukhopadhyay, in **National Conference on Materials, Devices and Circuits in Communication Technology (MDCCT-2014)**, at IETE Burdwan Sub Centre and Department of Physics, The University of Burdwan. West Bengal - 713104, on February, **2014**.
9. "*Alternative way of solution of unemployment of young generations especially for the engineers.*" by **Bitan Ghosh** and Partha Pratim Sarkar at 21st W.B. State Science & Technology Congress, pp – 248, on 20th – 21st February, **2014**, The University of Burdwan. West Bengal - 713104, **and won the best paper award.**

"Statement of Originality"

I **Bitan Ghosh** registered on **12/05/2022** do hereby declare that this thesis entitled **"AN ALTERNATIVE STUDIES ON ALL OPTICAL FREQUENCY ENCODED DIBIT BASED DIGITAL CIRCUITS USING REFLECTED SEMICONDUCTOR OPTICAL AMPLIFIER AND ADD/DROP MULTIPLEXER"**, contains literature survey and original research work done by the undersigned candidate as part of Doctoral studies.

All information in this thesis have been obtained and presented in accordance with existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I have fully cited and referred all materials and results that are not original to this work.

I also declare that I have checked this thesis as per the "Policy on Anti Plagiarism, Jadavpur University, 2019", and the level of similarity as checked by iThenticate software is 1 %.

Signature of Candidate: Bitan Ghosh

Date : 12.09.2024

Certified by Supervisor(s):

(Signature with date, seal)

1. Ardhendu Ghoshal 25/09/2024

Ex. Professor
Dept. of Instrumentation & Electronics Engg.
Jadavpur University
Salt Lake 2nd Campus
Kolkata-106

2. Partha Pratim Sarkar.
12/09/24

Assistant Professor
Department of ECE,
University Institute of Technology
The University of Burdwan

CERTIFICATE FROM THE SUPERVISORS

This is to certify that the thesis entitled "**AN ALTERNATIVE STUDIES ON ALL OPTICAL FREQUENCY ENCODED DIBIT BASED DIGITAL CIRCUITS USING REFLECTED SEMICONDUCTOR OPTICAL AMPLIFIER AND ADD/DROP MULTIPLEXER**", submitted by **Shri Bitan Ghosh**, who got his name registered on 12/05/2022 for the award of Ph. D. (Engineering) degree of Jadavpur University under the supervision of **Prof. Ardhendu Ghoshal**, Professor, Department of Instrumentation & Electronics Engineering, Jadavpur University and **Dr. Partha Pratim Sarkar**, Assistant Professor, ECE Department, UIT, The University of Burdwan, is completely based upon his own work and the thesis or any part of the thesis has not been submitted for any degree or diploma or any other academic award anywhere before.

Ardhendu Ghoshal
25/09/2024

Prof. Ardhendu Ghoshal,
Ex. Professor,
Department of Instrumentation &
Electronics Engineering,
Jadavpur University, Saltlake Campus,
Kolkata – 700106.

Ex. Professor
Dept. of Instrumentation & Electronics Engg.
Jadavpur University
Salt Lake 2nd Campus
Kolkata-106

Partha Pratim Sarkar.
12.09.2024

Dr. Partha Pratim Sarkar,
Assistant Professor, ECE Department,
UIT, The University of Burdwan,
Burdwan - 713104.

Assistant Professor
Department of ECE,
University Institute of Technology
The University of Burdwan

Acknowledgements

I would like to thank my supervisors Prof. Ardhendu Ghoshal, Professor, Department of Instrumentation & Electronics Engineering, Jadavpur University and Dr. Partha Pratim Sarkar, Assistant Professor, ECE Department, UIT, The University of Burdwan, under whose guidance I did this work. They were always there to listen and give me advice for their kind guidance, support, and helpful advices. Their feedback and comments were also invaluable for the writing of this report. I would like to expand my gratitude and respect for their warm co-operation towards completion of this project work. Also I would like to acknowledge all the teaching and non-teaching staffs, specially my research colleagues. As a whole which gave me an opportunity to commence this work, which in turn gave me a touch of real life project implementation. Besides I acknowledge Dr. Sankar Narayan Patra, Associate Professor, Department of Instrumentation and Electronics Engineering, Jadavpur University, for extending his full support to complete my thesis work. I would like to convey my regards to my parents and other members of my extended family for their encouragement. Finally, I express my love to my daughter Briti Ghosh and my wife Snigdha Ghosh to complete my project work.

Bitan Ghosh 12.09.24

Bitan Ghosh,
Department of Instrumentation & Electronics Engineering,
Jadavpur University, Salt lake Campus, Kolkata - 700106,
West Bengal, India.
Year 2025.

Abstract

Optics plays a crucial role in information and data processing due to its inherent parallelism and numerous other advantages. Compared to electronics, optics offers significant benefits in terms of speed and efficiency for super-fast computation and data processing. Over the past few decades, several all-optical data processors have been proposed based on Boolean logic. Optical systems and logic devices using optical switches have proven to be more efficient than their electronic counterparts in terms of speed, accuracy, and other aspects. Various types of all-optical methods have been suggested for implementing optical logic and arithmetic processors and devices. To realize these optical systems, certain optical switches such as those based on non-linear materials, electro-optic materials, optical bi-stable materials, optical filters, optical converters, beam splitters, and Semiconductor Optical Amplifier (SOA) based optical switches are required. Several encoding principles can be used to implement all-optical logic and arithmetic devices, including intensity, polarization, spatial, phase, and frequency encoding. Among these, frequency encoding is the most reliable and accurate. In optical computing and data processing, high speed is paramount. The frequency encoding/decoding technique uses different frequencies to represent different states of information, which remain consistent during reflection, refraction, and absorption. In this encoding technique, the '0' logic state is represented by ν_1 frequency and the '1' logic state is represented by ν_2 frequency. This thesis employs reflected semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM) optical switches to develop all-optical logic gates and circuits using frequency encoding. The dibit representation technique, which represents digital '0' logic state as [0][1] and digital '1' logic state as [1][0], is highly accurate and promising for data processing, reducing bit error problems by increasing the signal-to-noise ratio and supporting high parallelism. The presence of frequencies side by side $[\upsilon_1][\upsilon_2]$ indicates digital logic state '0', while $[\upsilon_2][\upsilon_1]$ indicates digital logic state '1'. Using ADM and

RSOA optical switches, we have developed all-optical, frequency-encoded, dibit-based integrated AND/NAND and OR/NOR logic gates with control input, XOR and XNOR logic gates, multiplexer and de-multiplexer circuits and controlled full subtractor circuit. These dibit-based systems using frequency encoding are expected to be significantly more advantageous than conventional logic gate-based optical systems. All proposed schemes have been verified through proper simulation experiments, with results aligning perfectly with the expected characteristics.

Contents

Chapter 1:

Chapter 2:

Chapter 3:

Chapter 4:

Chapter 5:

Chapter 6:

Chapter 7:

CHAPTER-1

An alternative studies on all optical frequency encoded dibit based digital circuits using optical switches: **An Introduction.**

1.1 Advantages of optics

Optics has emerged as a viable and promising contender in the realm of information and data processing, proving to be a lucrative alternative to conventional electronic systems owing to its inherent advantages. Scientists worldwide have proposed various schemes involving all optical logic gates, optical digital memory units, and a range of all optical processors for logic, algebraic, and arithmetic operations, as well as image processing, in the past few decades. Numerous methodologies have been put forth for the implementation of these optical logic and arithmetic processors and devices, necessitating the use of optical components such as non-linear material based switches, optical bi-stable switches, optical filters, electro-optic material-based switches, optical converters, beam splitters, and reflected semiconductor optical amplifier (RSOA) based optical switches. Additionally, certain logic gates have been realized by exploiting the four-wave mixing characteristics of semiconductor optical amplifiers (SOAs) in conjunction with mechanisms like polarization shift keying and tri-state operation logic.

Optics has emerged as a viable alternative for achieving high-speed communication with a notable combination of high bit rates, low bit error rates, and an elevated signal-to-noise ratio. The response time in optical communication networks holds paramount importance in facilitating rapid communication. To address the escalating volume of daily data traffic, there is a critical need to augment both the transmission link capacity and the switching network speed at the nodes.

The twentieth century marked the era of electronics, witnessing a transformative shift towards electronic communication and data processing with the advent of electrons. However, as the century drew to a close, scientists and technologists encountered significant challenges inherent in electronic systems, particularly pertaining to operational speed. Some of these issues include the Von-Neumann bottleneck, cross-talk, susceptibility to external electric, magnetic, and electromagnetic fields, among others. Electronic systems are constrained by limits such as the GHz speed ceiling, the sub-micron scale challenges in VLSI technology leading to dielectric breakdown, hot carriers, and the short-channel effect, which adversely affect device reliability.

Optics presents a solution to these challenges. In optical systems, photons serve as carriers of optical signals, offering numerous advantages over electronics, including:

1. Photons, being charge less particles with no rest mass, adhere to Bose-Einstein statistics and sometimes follow the classical Poisson distribution. This characteristic eliminates issues like cross-talk and interaction with other charged particles.
2. Optics exhibits a high degree of inherent parallelism, providing low-loss transmission and a broader bandwidth compared to electronics.
3. Unlike electronic systems confined to Boolean algebra, photonic systems allow the encoding of binary, ternary, quaternary, decimal, hexadecimal, or even multi-valued data with optical signals, offering diverse encoding systems.
4. Optical interconnections and integrated circuits are impervious to electromagnetic interference and immune from electrical short circuits.
5. Optical systems are compact, lightweight, and cost-effective to manufacture.

In addition to these advantages, optics proves highly suitable as an information carrier, surpassing the limitations of traditional electronics.

1.2 History and applications of photonics

The term 'photonics' emerged in the late 1960s to describe a field of research aimed at utilizing light for tasks traditionally associated with electronics, such as telecommunications and information processing.

The history of photonics traces back to early developments in optics and has evolved through significant scientific and technological advancements. Here’s a detailed overview:

A. Early Developments in Optics

1. Ancient and medieval optics

I. Ancient civilizations, such as the Greeks and Egyptians, studied the properties of light and lenses.

II. In the 10th century, Arab scientist Alhazen (Ibn al-Haytham) made significant contributions with his work on optics, particularly the Book of Optics, which detailed theories on vision, reflection, and refraction.

2. Renaissance and enlightenment

In the 17th century, key figures like Isaac Newton and Christiaan Huygens developed foundational theories. Newton's work on the nature of light and color, and Huygens' wave theory of light, laid crucial groundwork for modern optics.

B. 19th Century

1. Electromagnetic theory of light

I. James Clerk Maxwell’s equations (1860s) unified electricity, magnetism, and light, showing that light is an electromagnetic wave.

II. Heinrich Hertz later confirmed Maxwell's theory by demonstrating the existence of electromagnetic waves.

C. 20th Century

1. Quantum theory of light

Max Planck's work on blackbody radiation (1900) and Albert Einstein's explanation of the photoelectric effect (1905) introduced the concept of light quanta (photons).

These developments led to the birth of quantum mechanics, fundamentally changing our understanding of light.

2. Invention of the laser

I. Theodore Maiman built the first operational laser in 1960, based on the theoretical work of Charles Townes and Arthur Schawlow.

II. Lasers became a cornerstone of photonics, finding applications in communication, medicine, and various technologies.

3. Development of Fiber Optics

In the 1960s and 1970s, scientists like Charles K. Kao and George Hockham developed low-loss optical fibers, revolutionizing telecommunications by enabling high-speed data transmission over long distances.

D. Late 20th to 21st Century

1. Integration and advancements in photonic devices

I. The development of integrated photonic circuits in the 1980s and 1990s allowed for the miniaturization and increased functionality of photonic devices.

II. Photonic crystals and meta-materials, researched extensively in the 2000s, further enhanced control over light propagation and interaction.

2. Current trends and future directions

I. Ongoing research in silicon photonics aims to integrate photonic devices with electronic circuits, enhancing data processing speeds and efficiency.

II. Advances in quantum photonics explore the use of photons for quantum computing and secure communication.

III. The development of new materials, such as graphene and other two dimensional materials, promises further innovations in photonic devices and applications.

The history of photonics is marked by a series of groundbreaking discoveries and technological advancements that have profoundly impacted various fields. From early optical theories to the invention of lasers and the development of fiber optics, photonics continues to evolve, driving innovation and enabling new possibilities in science and technology. In brief, this field took root with the invention of the laser in 1960. Between 1985 and 1995, numerous research groups laid the groundwork for optical devices, connectors, and systems in pursuit of optical computing. Leveraging optics for digital logic operations presented a compelling opportunity for advancement, given its advantages over electronics. Today, it's evident that optics can surpass electronic systems in certain aspects. While modern computers boast robust processing power, operating at speeds of several giga-hertz with electronic transistors, microelectronics fabrication technology can further enhance performance. However, there remains a demand for faster machines to tackle numerical problems and real-time pattern recognition, yet the Von Neumann bottleneck constrains the speed of high performance electronic computers due to architectural issues. This bottleneck limits data exchange rates between processing units and memory significantly, exacerbated by electrical connectors' bandwidth limitations. Optical channels offer a larger bandwidth and robust interconnection capabilities, promising to overcome these limitations. Optics presents solutions surpassing those seen in polymer waveguides within printed circuit boards. Free-space optical propagation enables signals to travel to and from chips through numerous channels, facilitating entire operations. Advancements in high-speed semiconductor based optical switching and polymer waveguide systems offer hope for achieving optical terahertz speeds in computation and data processing. This thesis aims to explore novel optical interconnection methods and optical processors suitable for optical computing, pushing towards super fast computing objectives.

Applications of photonics

Photonics is the study and application of generating, controlling and detecting photons, the fundamental particles of light. It has a wide range of applications across various fields due to its ability to manipulate light in innovative and highly efficient ways. Here are some key applications of photonics:

A. Telecommunications: Optical fibers and photonic devices form the backbone of modern high speed internet and data transmission systems.

B. Medicine: Photonics enables advanced diagnostic techniques (e.g., optical coherence tomography), laser surgery, and medical imaging.

C. Manufacturing: Lasers are used for precision cutting, welding, and additive manufacturing (3D printing).

D. Consumer electronics: Photonic technologies are integral to devices like DVD players, smart-phones, and digital cameras.

E. Sensing and imaging: Photonics is essential in applications ranging from environmental monitoring to space exploration.

1.3 Literature survey

Optical computing has enjoyed a prominent position in the research realm for six decades[1.1]. John Caulfield delineates three distinct phases of this research period concerning electronics. The initial phase reflects a time of ‘ignorance and underestimation’ regarding electronics. The second phase marks an era of ‘awakening and fear of inferiority’, while the final phase represents a ‘realistic acceptance’ that optical computing and electronics are enduring collaborators[1.2]. In its nascent stages, the field of optical computation witnessed a surge of theoretical and conceptual explorations, sparked by the groundbreaking invention of the laser in the 1960s, leading to the inception of a new era in optical computing. The enthusiasm among researchers was palpable, resulting in numerous theoretical and conceptual works transitioning into tangible laboratory realizations. The period spanning from 1980 to 2000 is often referred to as the golden age of optical computing, marked by the design of innovative optical processors for practical applications. However, the field's growth decelerated in the past decade due to challenges such as the unavailability of nonlinear materials and alignment issues, dampening hopes for a super fast ‘all optical computer’. Nevertheless, ongoing dedication from scientists has spurred advancements in diverse subfields like nano-photonics, bio-photonics, opto-fluidics, femto-second nonlinear optics, optical quantum cryptography, and optical quantum computing[1.3-1.4]. Optical processors play an indispensable role in this domain, classified into two types based on input data nature: analog optical computing and digital optical computing[1.5]. Several publications have delved into the significance of optical processors, categorizing them as Optical Analog Processors (OAPs) and optical digital Processors (ODPs), the two major groups. The collective efforts and commitment of scientists have led to significant progress across these areas, although a comprehensive review of all contributors remains a challenging endeavor, given the breadth of this diverse field. Nonetheless, this discussion aims to elucidate the fundamental principles of digital optical processors and provide a concise overview of this promising domain.

Nonlinear optics, governed by intensity controlled higher order nonlinear susceptibility, plays a crucial role in the design of Optical Limiting Gates (OLGs). Parameters such as intensity dependent refractive indices, and intensity controlled transmittance and reflectance, serve as key thresholds in OLG design. Nonlinear materials must exhibit a smaller relaxation time of nonlinearity coupled with a larger magnitude of nonlinear susceptibility. The effectiveness of nonlinear interaction is determined by the energy density of the interacting beams. Consequently, OLGs can be designed with high conversion efficiency for a given low input energy by reducing the dimension of the interaction region, thereby increasing energy density at the expense of structural confinement of the nonlinear material's interaction region. Various structural confinement techniques have led to the development of different OLG design technologies, including Fabry-Perot cavity-based OLGs and waveguide or fiber optics-based OLGs.

Numerous strategies have been proposed for implementing all-optical logic gates utilizing highly nonlinear optical fibers (HNLFs). The utilization of HNLFs offers the advantage of processing ultrafast optical signals, leveraging the femto-second response of the Kerr effect in silica. To enhance flexibility and simplify configurations, various logic operations have been suggested. However, integrating HNLFs can be challenging due to their larger size. To circumvent integration difficulties, efforts have been made to maximize logic operations within the same configuration using HNLF-based schemes.

Yuji Miyoshi, Kensuke Ikeda, and others introduced and demonstrated all-optical differential logic gates with a uniform configuration using a nonlinear optical loop mirror (NOLM) operating at speeds of 40 Gbit/s, featuring multi-periodic transfer functions. The NOLM's transfer function relies on the differential phase shift of two coherent interfering beams, determined by the differential length of the NOLM and the refractive index change induced by intensity dependent input signals. However, processing speed limitations arise from dispersion and unwanted nonlinear effects in HNLFs.

Soma Dutta and colleagues[1.6] proposed an all optical approach for high speed (far beyond GHz range) optical logic gates and memories. Their approach leveraged frequency encoding techniques, ensuring that coded information (0, 1) remains unaltered during transmission, contribute better noise free transmission and high signal-to-noise (S/N) ratio. This type of optical logic gates, latches and flip-flops enable the implementation of various digital operations like multiplexers, de-multiplexers, and multivibrators.

Bijon Ghosh[1.7] introduced all optical dibit based logic gates, detailing different types of logic gates, combinational and sequential logic circuits and devices using various encoding and decoding techniques. While many existing optical gates are not purely optical due to relying on SOA-based switches driven by electrical current,

This approach leverages frequency encoding and dibit representation techniques to optimize the organization of all optical operations. Frequency encoding involves using different frequencies to represent distinct pieces of information, allowing for efficient multiplexing and de-multiplexing of data signals. By assigning unique frequencies to different data streams, this technique enables simultaneous transmission and processing of multiple signals without interference.

The dibit representation technique further enhances this system by using pairs of bits (dibits) to represent data. This method increases the signal-to-noise ratio, ensuring more reliable and accurate data transmission. The dibit representation also facilitates high speed operations and reduces bit error rates, making the system more robust and efficient. This not only ensures reliable and accurate operations but also addresses bit error concerns by enhancing the signal-to-noise ratio, fostering parallelism, and facilitating ultra fast operational speeds, while also enabling the development of tri-state and quaternary state logic operations within compact all optical devices.

1.4 Different types of arithmetic and logical operations with optical switching technology

Over the past two decades, significant research efforts have been directed towards information processing using optical techniques. Recently, optical computation has emerged as a new addition to this field[1.8-1.9]. Optical systems can be designed, simulated, or analyzed for optical computation purposes, offering both potential advantages and some drawbacks. Optical processors operate fundamentally as two-dimensional parallel systems, boasting high space-bandwidth products. They allow optical signals to propagate through separate channels without interaction and enable parallel transmission without interference or cross-talk. The inherent parallelism of optics has proven beneficial in computation and arithmetic data processing, leading to successful contributions in these areas. Various operational schemes for arithmetic data processing have been documented by different researchers in recent years. Optical technologies play crucial roles in wide and local area networks, facilitating different types of all optical logic and algebraic operations[1.10] as reported by many scientists and researchers. Notably, some researchers have recently introduced all optical dibit based logic gates primarily leveraging the nonlinearity of semiconductor optical amplifiers (SOAs)[1.11].

1.5 Several encoding principles used for all optical logic operations

To implement optical logic and arithmetic processors, the key aspect is encoding the optical system. Various encoding systems are employed to develop optical logic systems, depending on characteristics like light intensity, polarization, phase change, frequency, etc. Leveraging these light properties, several popular optical encoding systems have been created. These consist of spatial, intensity, phase, polarization and frequency encoding principles, among others. Different light intensities represent logic states '1' and '0' respectively[1.12-1.14] in the intensity encoding method. For instance, if '2I' intensity of light signifies logic state '1', then 'I' intensity of light or no light indicates logic state '0'. This encoding method utilizes certain nonlinear materials as switches. In the case of isotropic materials, the well-established Kerr non-linearity equation can be employed as

$$n = n_0 + n_2 I \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(1.1)}$$

In this context, 'n' signifies the refractive index of the specific nonlinear material, where 'n_0' stands for a fixed linear refractive index, 'n_2' represents the nonlinear correction term and 'I' denotes the intensity of light traversing throughout the material. For example, several nonlinear materials (NLMs) functioning as optical switches include pure silica glass (SiO2), carbon disulfide (CS2), gallium arsenide (GaAs), among others. These materials exhibit this form of nonlinearity and adhere to the Kerr nonlinearity equation.

In the polarization encoding principle[1.15-1.16], unpolarized light signifies digital low logic state '0', while digital high logic state '1' is represented by polarized light. The digital low and high logic states are denoted by the light signal's intensity level for executing the various boolean logic operations, where a non-linear material works as a switching element. Hence, maintaining a constant intensity level of the light signal is crucial for representing any logic state. However, the signal's intensity can fluctuate during long distance optical signal communication, causing issues for logic processors reliant on signal intensity levels for detection. This challenge can be mitigated by employing polarization based encoding/decoding techniques. Wang et al.[1.17] proposed the use of optical polarization based encoding systems for implementing logic families. Here, a polarization alignment of optical beams is encoded as digital low logic state '0', while its orthogonal arrangement of polarization is designated as digital high logic state '1' in this encoding technique. Nevertheless, polarization alignments may modify due to various factors, potentially leading to bit errors in information processing.

In the phase encoding principle[1.18-1.22], two distinct phases of light are encoded as logic state '1' and logic state '0', respectively. In the optical phase encoding process, a co-sinusoidal light signal represented as Acosωt denotes logic state '1'. Introducing a phase of π in a cosinusoidal light signal Acosωt using a phase modulator signifies logic state '0'. During the decoding process, if the output wave's phase is zero concerning a reference signal Acosωt, the output bit is '1'. Conversely, if the output wave's phase is π concerning a reference signal Acosωt, the output bit is '0'.

In spatial encoding[1.23-1.26], two distinct pixels are arranged with opaque and transparent sub-cells, representing the logic high state '1' and logic low state '0' in a 2-D plane. In the course of opto-electronic switching technique using suitable nonlinear materials, the input signal bits are produced, which can limit the processing speed of the system. Pixel-based operations can encounter interference and diffraction effects, potentially altering the expected output image pattern and leading to bit error issues. Additionally, as output results are derived using a decoding mask and the encoding and decoding technologies differ, designing sequential or combinational logic circuits with spatial encoding becomes unfeasible.

Overall, the frequency encoded technique offers a novel and potentially advantageous approach to implementing boolean logic, particularly in specialized applications where noise resistance, analog compatibility, and parallel processing are critical, wherein the frequency of light remains constant during signal transmission[1.27-1.29]. If ν_1 frequency represents '0' logic state and ν_2 frequency represents '0' logic state, these ν_1 and ν_2 frequencies remain unchanged throughout data transmission. Many successful all optical logic operations and devices have been developed using these encoding techniques[1.30-1.31].

1.6 Advantages of frequency encoding technique over other encoding principles

Frequency remains unaltered during reflection, refraction, absorption, etc., owing to its inherent characteristics. In optical computation, photons are deemed more suitable as information carriers than electrons, not only due to their super-fast speed but also for various other aspects of digital and analog information processing. Consequently, photonic systems have the potential to replace electronic systems successfully. However, optical data processing cannot always follow conventional methodologies as seen in electronics. Researchers and technologists are deeply engaged in overcoming speed related challenges to realize all optical logic, arithmetic, and algebraic operations using Boolean mechanisms.

Numerous reports highlight the progress of different optical logical systems, where various logic gates serve as fundamental units. However, the implementation of various optical boolean logic systems using intensity coding technique faces many challenges[1.32-1.34]. In intensity coding, the presence of an optical signal represents '1' while its absence indicates '0'. However, decreasing light intensity over an optical path can lead to issues where the intensity drops below the reference level for '1' and enters the level for '0', posing encoding problems. Similarly, polarization encoding has drawbacks, where changes in polarization during transmission and propagation can cause implementation issues for optical logic gates. Spatial encoding faces interference and diffraction effects, altering expected image patterns and resulting in bit error problems.

Boolean systems have inherent limitations in a wide range of data processing scenarios, necessitating various proposals for different encoding techniques to implement Boolean logic gates. While the mentioned encoding techniques have loss related problems, the frequency encoded technique stands out as advantageous. This technique treats the presence of specific light frequencies as logic states '1' and '0', with the frequencies remaining unaltered throughout data transmission. Frequency encoding is more reliable, with advantages such as a very low bit error ratio (BER), parallel transmission of multiple data through a single optical channel, and stability in long distance communication, making it a preferred choice for developing super fast optical processors.

1.7 Dibit representation technique

The dibit representation technique involves symbolizing a digit using two consecutive bit positions. In this method, if A = 0 and B = 0 (i.e., [0][0]), it signifies the digit '0'. Similarly, if A = 0 and B = 1 (i.e., [0][1]), it represents the digit '1'; if A = 1 and B = 0 (i.e., [1][0]), it indicates the digit '2'; and if A = 1 and B = 1 (i.e., [1][1]), it signifies the digit '3'. The key advantage of dibit representation lies in its ability to facilitate ternary, quaternary, octal, and decimal operations with optics. In some papers, a slight modification to the dibit representation concept has been proposed. Here, the two positions are coded using two different frequencies, such as υ_1 = 195 THz and υ_2 = 193 THz. In this setup, υ_1 represents digital low logic state '0', while υ_2 represents the digital high logic state '1'. Consequently, the logic state '0' is depicted as [0][1] whereas the logic state '1' is shown as [1][0] in this dibit representation technique. So the existence of two frequencies side by side like, [υ_1][υ_2], indicates logic state '0', while [υ_2][υ_1] represents logic state '1'. The introduction of dibit representation in optics for logical operations was pioneered by S. Mukhopadhyay[1.35]. This technique not only ensures reliable and accurate operations but also aids in reducing bit error problems by increasing the signal-to-noise ratio. Furthermore, it enables a high degree of parallelism and ultra fast operational speeds. The dibit representation technique enhances system performance in several ways. First, it ensures reliable and accurate operations by providing a stable and consistent method for representing data. This stability helps to reduce bit error problems by increasing the signal-to-noise ratio, thereby improving the clarity and integrity of the transmitted signal.

In addition to enhancing reliability, the dibit representation technique also enables a high degree of parallelism. By allowing multiple bits to be processed simultaneously, it increases the efficiency and speed of data processing operations. This capability is particularly beneficial in applications requiring ultra fast operational speeds, as it allows for quicker data transmission and processing, ultimately leading to better overall system performance. A high degree of parallelism refers to the ability of a system to perform many operations or tasks simultaneously. This is accomplished by breaking tasks down into smaller sub-tasks that can be executed simultaneously across multiple processors or processing units. The greater the number of tasks that can be executed in parallel, the higher the degree of parallelism. High parallelism is advantageous because it can significantly enhance computational efficiency and speed, allowing for more rapid data processing and problem solving. This is particularly important in areas such as large scale scientific simulations, big data analytics, and real-time processing systems, where the demand for processing power is substantial. By leveraging parallelism, these systems can handle complex computations and large volumes of data more effectively.

1.8 Basic characteristics of semiconductor optical amplifier (SOA)

A semiconductor optical amplifier (SOA) is an optoelectronic device capable of amplifying an input light signal under appropriate operating conditions. Figure 1.1 illustrates a simple diagram of a basic SOA device.

The input signal is amplified by the active region of the device, typically driven by an external biasing as the pumping source for amplification. A built-in waveguide confines the signal wave within the active region, although the optical confinement is limited. It results in some signal leakage into the neighboring lossy cladding space. As a result, the output signal is mixed with noise that is inherent to the amplification method and cannot be entirely removed. Furthermore, the reflective properties of the device facets lead to ripples in the gain spectrum.

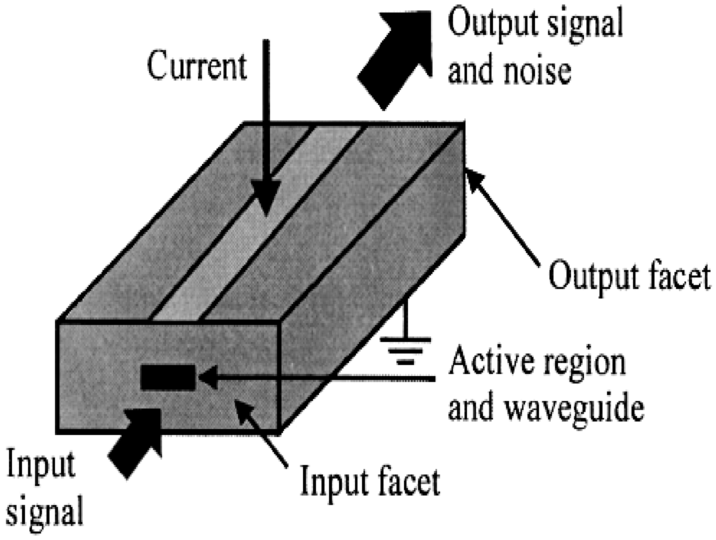


Figure 1.1: Schematic diagram of an SOA.

The electrons, also known as carriers, in a semiconductor optical amplifier, are introduced from an external source into the active region. These energized electrons occupy specific energy states in the conduction band (CB) and create holes in the valence band (VB) of the active region material. The semiconductor allows for three radiative mechanisms, illustrated in figure 1.2 for a material with a two-level energy band structure.

In stimulated absorption, a photon of incident light with sufficient energy can prompt a carrier transition from the valence band to the conduction band. However, this process is inefficient as the incident photon is absorbed.

When a photon of appropriate energy strikes the semiconductor, it triggers stimulated recombination between a CB carrier and a VB hole, releasing energy in the form of a coherent, identical photon (same phase, frequency, and direction as the inducing photon). This stimulated photon can further induce similar transitions, leading to optical gain when the injected current generates a population inversion, favoring stimulated emission over absorption.

On the other hand, spontaneous emission involves the recombination of a electron of conduction band with a hole of valence band keeping the non-zero probability per unit time. As a result, a photon with random phase and direction emits with a wide range of frequencies. These spontaneously emitted photons contribute noise and reduce the available carrier population for optical gain, a process inherent to amplification in SOAs, making noiseless SOAs unachievable.

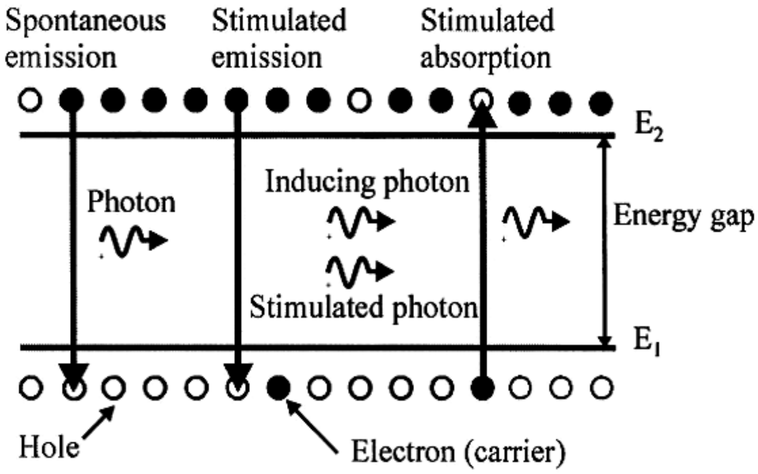


Figure 1.2: Spontaneous and Stimulated processes.

1.9 Optical switches for conducting frequency encoded logic system

Many scientists utilized various optical switches, such as SOA based wavelength converters, optical filters, add/drop multiplexers and optical prisms, to develop all-optical frequency encoded logic and arithmetic processors. The SOA is among the most commonly used devices for ultrafast signal processing, largely due to its well-established and commercially available technology. The effectiveness of ultrafast signal processing hinges on harnessing the advantageous features of SOAs. In this introductory chapter, we will briefly review the basic properties of SOAs, their key features, and their applications as ultrafast nonlinear switches.

1.10 Fundamentals characteristics of SOA

Semiconductor optical amplifier is the full form of SOA. The basic configuration of an SOA is very easy and it has some match with semiconductor laser diodes. But SOA is dissimilar from semiconductor laser diodes due to its anti-reflected (AR) coating on both surfaces and it is also used as structure of the waveguide. The active layer is surrounded as a gain medium to minimize the reflection at both surfaces and it can either be the types of bulk, quantum well, or quantum dots. The optical gain of the SOA can be calculated from the below equation.

$$g(w) = -\frac{\omega}{cn}\int_{k=0}^{k=\propto} D(k)[Im(\chi^{(1)}(k))]dk$$

$$= \frac{\omega}{cn\varepsilon_0}\int_{k=0}^{k=\propto} D(k)\frac{h\gamma_{CV}|\mu_{cv}|^2}{h^2(\omega_{cv}(k)-\omega)^2+h^2\gamma_{CV}^2}(f_c(k)-f_v(k))dk \ldots\ldots\ldots\ldots \quad (1.2)$$

Here, ‘c’ is the velocity of light, ‘ω’ is the light wave angular frequency, ‘ε_0’ is the vacuum dielectric constant, ‘n’ is the refractive index, ‘D(k)’ is the density of state expressed in terms of wave number ‘k’, ‘ω_{cv}(k)’ is wave number dependent transition frequency between conduction-band and valance-band, ‘γ_{CV}’ is the de-phasing time and ‘f_c’, ‘f_v’ are the fermi-dirac distribution functions. In the development of SOA, how to get large output saturation power, small noise and polarization insensitive gain is the primary concern. Due to reduced population inversion, the output power saturation takes place for the intense optical power since it consumes the population inversion carriers. If we use the SOA at an output power above saturation power, then it cannot be getting good way for arbitrary pattern modulation. And it is known as the pattern effect. The equation of saturation power is given by

$$\rho_s = Ch\omega \frac{d\omega}{\Gamma} \frac{1}{g_d \tau} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(1.3)}$$

Where ‘d’ is the thickness of active layer, ‘C’ is the fiber chip coupling efficiency, ‘ω’ is the width of active layer, ‘g_d‘ is differential gain, ‘Γ’ is the optical confinement factor, ‘τ’ is carrier life time and ‘$\frac{d\omega}{\Gamma}$’ corresponds to the mode cross section. The above equation helps us to calculate the saturation power and also gives us the dependency knowledge of the gain of this device with different structural aspects. So, several types of SOA have been developed with different shapes.

1.11 SOA as an ultra fast non-linear optical switch

SOA is performing as an ultra-fast non-linear intermediate. The electron-hole pair density depends upon the non-linear refractive index, which changes in accordance with the optical gain due to the current injection process.

Types of non-linearities in SOA: There are four types of non-linearities are found in SOA.

A. Cross-gain modulation (XGM): Occurs due to gain saturation in an SOA (illustrated in figure 1.3).

B. Cross-phase modulation (XPM): Occurs alongside XGM when two optical signals are concurrently present in the SOA.

C. Self-phase modulation (SPM)

D. Four-wave mixing (FWM)

The process gives high conversion efficiency and a high signal-to-noise ratio. A Mach-Zehnder, Michelsen, or Sagnac interferometer configuration incorporated on a single chip, which is used to convert phase modulation to intensity modulation. These three common interferometers are shown in figure 1.4.

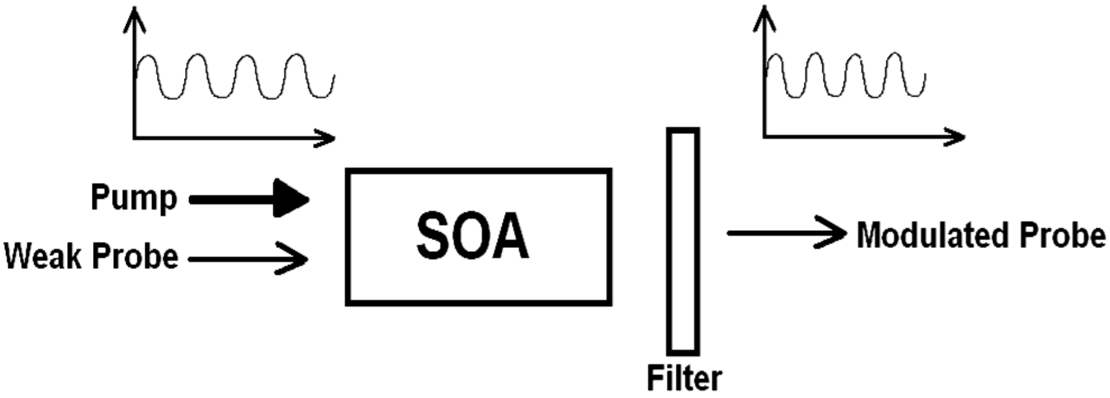


Figure 1.3: Simple wavelength converter using XGM in an SOA.

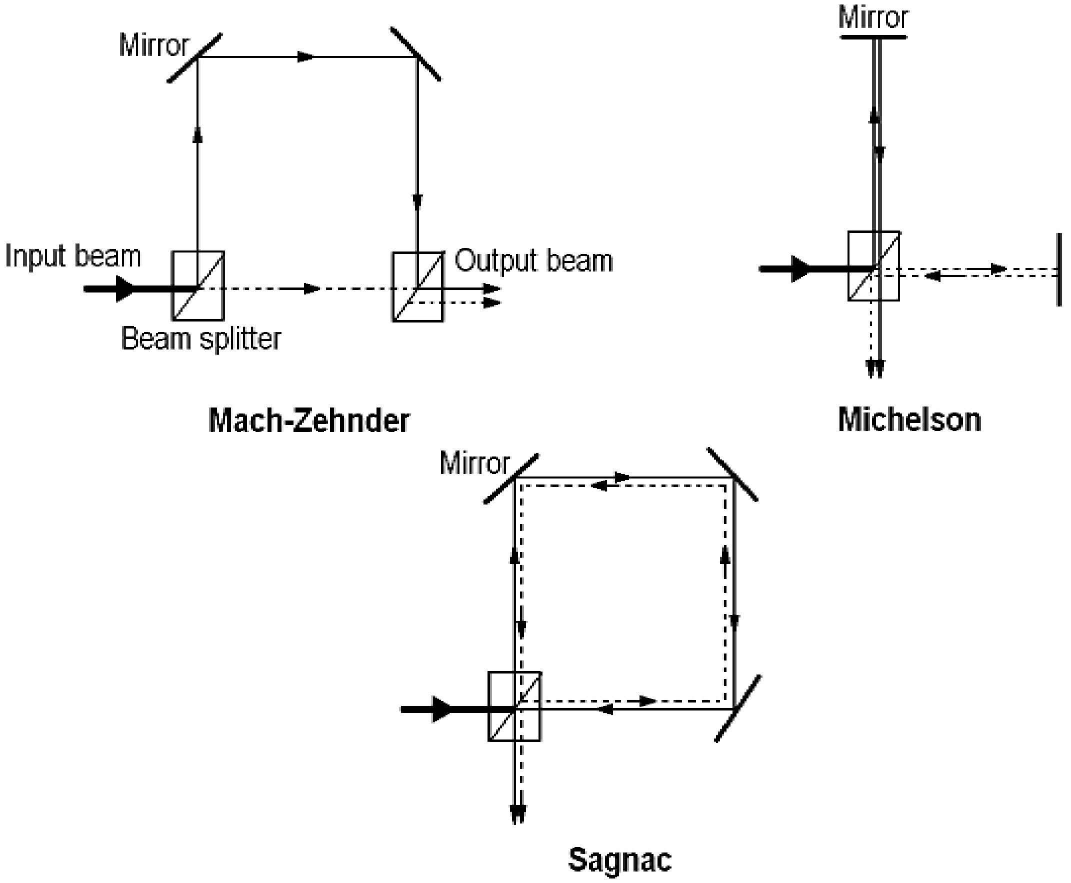


Figure 1.4: Common interferometers used in SOA functional applications.

SOA is also known for four-wave mixing (FWM) type optical non-linear effects. FWM has been used as a technique for performing wavelength conversion due to its good conversion efficiency and high-speed response for wavelength division multiplexing (WDM) networks. The FWM technique involves injected signals commonly known as pump and probe beams of light, which can originate from two single-wavelength distributed feedback (DFB) lasers.

Signal characteristics:

Pump signal: Typically has higher power compared to the probe signal.

Probe signal: Has lower power compared to the pump signal.

Signal type: Both pump and probe signals are CW (continuous wave).

1.12 Frequency conversion utilizing Non-linear Polarization Rotation (NPR) of probe beam in SOA

The basic property of SOA is non-linear polarization rotation of the probe beam, caused by optically induced non-linear refractive index in the bulk SOA due to intense pump beams of light. This alters the SOA's optical properties, modifying the probe beam's intensity and state of polarization (SOP). A polarization beam splitter (PBS) measures the non-linear rotation as an intensity difference, as shown in figure 1.5.

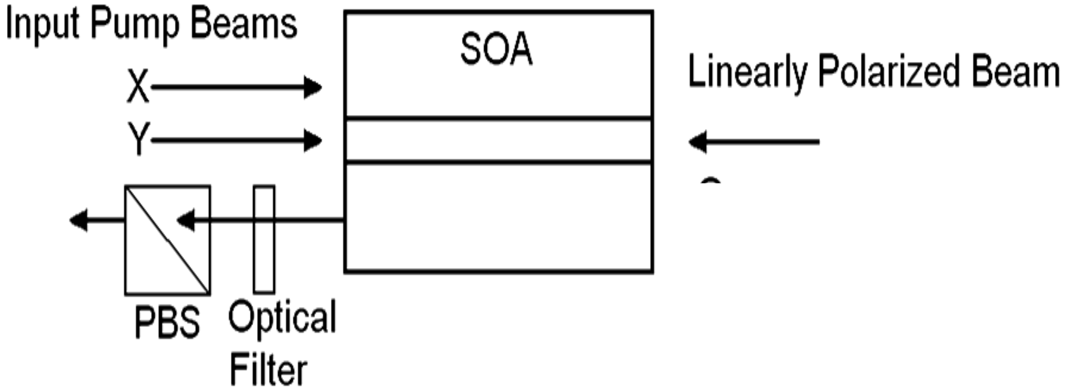


Figure 1.5: Frequency conversion of probe beam by NPR method of SOA.

For the first case, the SOA is biased with suitable current, and 'X' and 'Y' input pump beams are adjusted to proper power levels. A linearly polarized weak probe beam 'Z' (ν_0 frequency) is coupled with the pump beams in SOA. The polarizer is aligned such that no light is obtained at output 'O' when no input beams or only one pump beam is there. Light is obtained at 'O' only when both pump beams 'X' and 'Y' are present. Alternatively, a single pump beam with intensity equal to the sum of both pump beams can change the probe beam's polarization, allowing it to be used as a control beam to transmit the probe beam from input to output.

1.13 Working principle of Add/Drop multiplexer using SOA

The operational concept of an add/drop multiplexer (ADM) involves the selection of a specific light wavelength while avoiding interference with neighboring wavelengths. Various types of add/drop multiplexers have been developed, employing different optical devices[1.36-1.40], some utilize grating filters and circulators, while others rely on alternative light wave technologies.

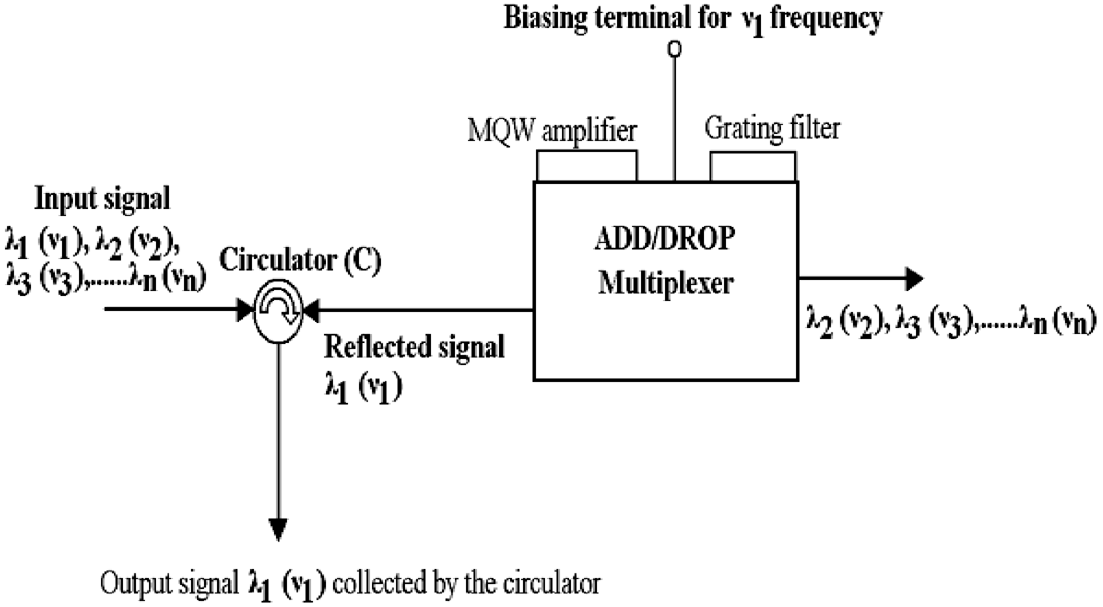


Figure 1.6: SOA based ADD/DROP multiplexer.

The tuning of filters is achieved by adjusting the biasing input current into the Semiconductor Optical Amplifier (SOA). This process involves reflecting the desired wavelength through the filter, which is then amplified by the Multiple Quantum Wells (MQW), while a circulator directs the amplified wavelength in the required direction. Concurrently, other wavelengths parallel to the selected one at the input pass through the SOA made filter. This approach enables the separation of the beam of light of a specific wavelength by the function of ADM from a range of beams of light of different wavelengths.

The scheme of configuration is depicted in figure 1.6. For illustration, the SOA must be finely adjusted or tuned at the appropriate biasing current to isolate a specific frequency ν_1 from a data series containing frequencies ν_1, ν_2, ν_3, …ν_n. This adjustment ensures that all frequencies pass through the Add/Drop Multiplexer (ADM), while only the ν_1 frequency is reflected by the SOA and collected by the circulator within the system.

1.14 Working function of wavelength converter using SOA

The phenomenon of wavelength conversion[1.41-1.47], relying on the Cross-Gain Modulation (XGM) property of Semiconductor Optical Amplifiers (SOAs), stems from the saturation of gain. This occurs when a weak continuous wave (CW) type beam of light called probe beam at a definite wavelength interacts with a powerful pump beam (at some other definite wavelength) of light are projected together into the input of the SOA. When the amplifier is biased at an appropriate current level, the probe beam exhibits strong characteristics due to Cross-Gain Modulation (XGM) in the Semiconductor Optical Amplifier (SOA)[1.48-1.50], leading to what can be termed as wavelength conversion. XGM-based wavelength conversion employs two fundamental schemes. First one is the co-propagating scheme and second one is the counter-propagating scheme. Both the pump beams and probe beams of lights are introduced from the same side of the SOA in the co-propagating method. But, the two types of beams of lights are injected in different opposite directions manually in the counter-propagating method.

The first method typically offers superior performance in noise control. In this process, a weak continuous wave (CW) type of probe beam of light of λ_1 wavelength and a powerful pump beam of λ_2 wavelength are inserted into the input ports of the amplifier. In the device, an anti-reflective surface or layer is present for λ_1 wavelength near the input side and an extremely reflective surface or layer for λ_2 wavelength near the output end. In the setup, the powerful pump beam delivers its entire power to the weak probe beam, effectively amplifying the strength of probe beam when it exits from the output terminal of the device. This process is illustrated in figure 1.7. If either of the beams is absent at the input side, no conversion occurs.

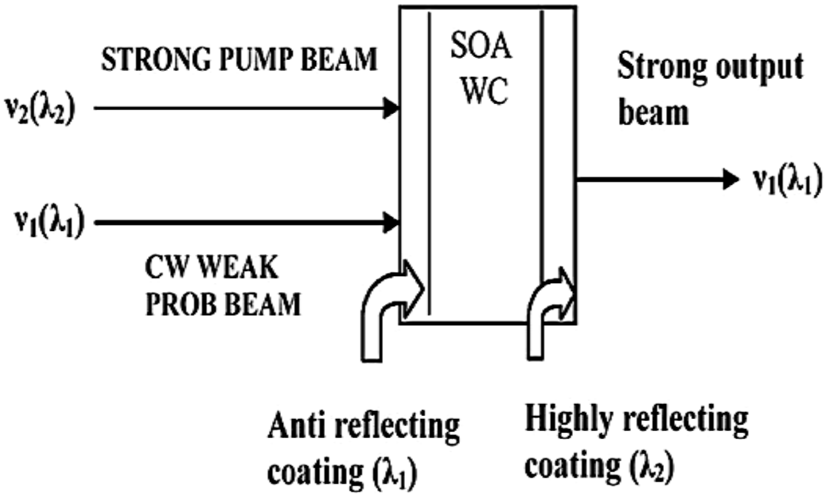


Figure 1.7: Schematic diagram of SOA type wavelength converter.

1.15 SOA working as a polarization-switch (PSW)

SOA could be implemented as a polarization switch. The properties of polarization and gain saturation of SOA may be used for designing the non-linear polarization switching device. A strained bulk SOA, two laser sources of different frequencies, one polarization beam splitter (PBS), an attenuator, three polarization controllers (PC_1, PC_2 and PC_3) and a power meter are used for implementing this switching system. The whole schematic diagram of PSW is drawn in figure 1.8. PC_1, PC_2 and PC_3 control the probe beam (which is a weak continuous wave laser of beam of light of ν_1 frequency), the pump beam (which is a highly powerful beam of light of ν_2 frequency) and the output beam of light correspondingly. Now, the probe beam of light is applied to one input port of SOA through an attenuator for reducing the power of input probe beam (-15 dBm). The direction of linearly polarized probe beam of light is tuned by PC_1 in such a way that the direction of polarization of the input probe beam of light be around 45^0 to the direction of SOA surface of incidence. Next, there is a PBS, which is combined with the output light beam of SOA. Due to the splitter, the output beam of light coming from SOA is divided into two parts. One part is the horizontal polarization component (H) of the beam of light and another one is the vertical polarization component (V) of the beam of light. Finally, the vertical component of the output of SOA comes at port-1 and the horizontal component of beam of light of the output of SOA comes at port-2 correspondingly. Actually, the optical field of linearly polarized light separates the two modes of wave as transverse electric field (TE) and transverse magnetic field (TM) components. They transmit through SOA alone when there is absent of pump beam. This transmission should be amplified by the biasing effect introduced in SOA. Then the value of the maximum gain of TE and TM modes are approximately the same due to the biasing current value (162 mA). Thus, the state of polarization of output beam of SOA is oriented by the PC_3. Therefore, the beam of light becomes zero at the output port-1. That means there is no vertical component of the output beam of SOA. As a result, maximum power is delivered with the horizontal component of beam of light of the output of SOA at port-2.

Basically, semiconductor optical amplifier shows the property of polarization dependent gain-saturation scheme. This character causes the change in different refractive index for TE and TM due to very much strong pump type beam is present.

So one can say probe type beam of light will appear at port-2 and it is called ON-state situation when the pump type beam is absent. But, the probe type beam of light will not be available at port-2 and it is called OFF-state situation when the pump type beam of specific intensity is there. Obviously, the status of port-1 will be opposite with respect to port-2. Therefore, power will develop at port-1 when the pump type beam of light is there in SOA.

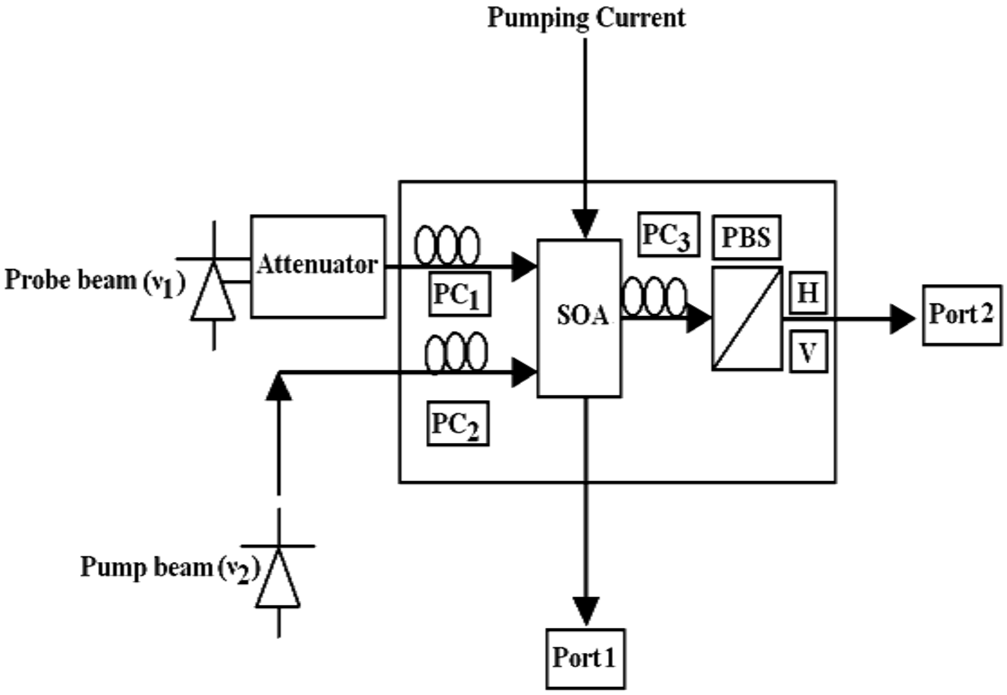


Figure 1.8: Schematic diagram of SOA working as a polarization switch.

1.16 Aim of the research work

The research objective is to create innovative frequency encoded all optical dibit based digital logic gates[1.51-1.52], memory cells, registers, counters, and related components. We plan to assess the performance of these gates and digital circuits through analytical methods and computer simulations. MATLAB/SIMULINK software will be utilized to study the entire operations, enabling us to simulate and analyze the behavior of the proposed optical systems comprehensively.

Developing frequency encoded, all optical dibit based digital logic gates and associated components represent a significant contribution to the advancement of optical computing technology. Optical computing offers potential advantages such as high speed data processing and low power consumption compared to traditional electronic computing. By harnessing frequency encoding techniques, we aim to enhance the efficiency and reliability of data processing within optical systems.

These innovations have the potential to revolutionize computing architectures by overcoming current limitations of electronic devices, such as speed bottlenecks and energy inefficiencies. The implementation of frequency encoded logic gates and components can pave the way for faster and more efficient data handling in various applications, including telecommunications, data centers, and scientific computing.

Moreover, our research not only focuses on developing these components but also on evaluating their performance through rigorous analytical methods and computer simulations. This approach ensures that the proposed optical systems meet stringent performance criteria and can be optimized for real world applications.

In essence, our goal is to pioneer advancements in optical computing technology by introducing novel frequency encoded all optical dibit based digital logic gates and components, thereby pushing the boundaries of what is currently achievable in data processing capabilities.

By developing frequency encoded all optical dibit based digital logic gates and associated components, we aim to contribute to the advancement of optical computing technology. These gates and circuits will be designed to operate using frequency encoding techniques, ensuring efficient and reliable data processing within optical systems. The performance analysis conducted through analytical methods and computer simulations will provide valuable insights into the functionality, efficiency, and potential improvements of these optical components.

1.17 Developing a research plan

This project is decomposed in five main stages:

1. The first stage states design and realization of new scheme of all optical frequency encoded dibit based XOR & XNOR logic gates along with the simulated result. After designing of these gates, the mathematical model will be designed. Then the result will be compared with the truth table of the logic gates.
2. The second stage states a new approach of all optical frequency encoded dibit based digital multiplexer circuit using optical switches like add-drop multiplexer and reflected semiconductor optical amplifier and its realization with simulated verification.
3. The third stage discusses about the all optical frequency encoded dibit based de-multiplexer type digital combinational circuit with simulated validation. Checking of the result of the mathematical model with the logic of the circuits will be done in the end.
4. The fourth stage states a different approach to understand all optical frequency encoded integrated AND-OR/NAND-NOR logic gates using optical switches with control dibit input with its simulative result and the graphical result will be verified with the logic of the logic gates.
5. The fifth or final stage will consist of the propose of dibit based all optical frequency encoded controlled full subtractor combinational logic circuit with optical switches. The result should be verified with the logic of the digital circuit after designing the mathematical model of this circuit. The designing and realization of more all optical digital circuits will be done in future also.

1.18 Techniques involved in solving the problem

In the proposed research, various all optical semiconductor optical amplifier (SOA) based switches such as Reflected Semiconductor Amplifier (RSOA) and Add Drop Multiplexer (ADM) will be analyzed using MATLAB/SIMULINK software. These blocks will serve as building blocks for developing different logic gates, which will also be studied through simulation using this software. This simulation work is believed to be novel and has not been reported to the best of our knowledge. The utilization of these switching blocks will pave the way for the future development of optical logic and arithmetic units.

Additionally, the concept of optical dibit representation will be explored. This innovative technique leverages the inherent properties of light to encode information, offering the advantage of high-speed operation due to the rapid propagation and switching capabilities of optical signals. By representing data using optical dibits, we can enhance the efficiency and performance of various logic and computational circuits.

The primary objective of this exploration is to implement frequency encoded all optical dibit based XOR and XNOR logic gates. These gates are fundamental components in digital circuits, performing essential logical operations. By utilizing optical dibit representation, these logic gates can operate at significantly higher speeds compared to their electronic counterparts.

In addition to the XOR and XNOR gates, an integrated AND-OR logic gate with a control input will be developed. This versatile gate can perform multiple logical functions based on the control input, providing greater flexibility and functionality in optical computing systems.

Furthermore, the project aims to design and implement controlled multiplexer and de-multiplexer circuits. These circuits are crucial for routing and managing data in complex optical networks, enabling efficient communication and data processing.

To achieve these implementations, optical switches such as the reflected semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM) will be utilized. The RSOA is known for its ability to amplify and switch optical signals with high precision and speed, while the ADM allows for the selective addition and removal of specific wavelength channels in a dense wavelength division multiplexing system.

By leveraging these optical components, the versatility and potential of optical computing technologies will be showcased, demonstrating their capability to advance the field of high speed, high efficiency computing. This exploration not only highlights the advantages of optical dibit representation but also underscores the critical role of advanced optical switches in the development of next generation optical circuits and systems.

This version provides more context and detail about the significance and objectives of exploring optical dibit representation and the specific implementations planned, emphasizing the advantages and potential of optical computing technologies.

1.19 Simulation method of ADD/DROP multiplexer and RSOA

Here, simulink tools of MATLAB (R2008a) simulation software are used for simulation of reflected semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM).

In case of mathematical model of ADM, shown in figure 1.9, two different signals are considered as input. Where each of the input signals is considered with its own frequency and power. Here, the input of optical signal beam ‘A’ is taken as the frequency of 5×10^{14} Hz with power 5×10^{2} watt again for the other optical signal beam ‘B’, the frequency is considered as 10^{10} Hz and power as 60 watt. These inputs are generated using constant blocks from the simulink library. The values of these blocks can be adjusted, allowing the frequency and power to be modified according to the required input signals. These blocks are connected to the ADM main unit through four manual switches, labeled as Manual Switch 1, 2, 3, and 4, respectively. Additionally, another block labeled as Biasing Current is connected to the main ADM unit. Here the value of biasing current is considered as logic state ‘1’ for frequency ν_2 with wavelength (λ_2) and logic state ‘0’ for frequency ν_1 with wavelength (λ_1). In the main ADM block, two MATLAB functions have been programmed and written in 'C' language, which are not displayed here, are responsible for selecting the appropriate output at the output terminal. If the biasing current is taken as logic state ‘1’, the optical signal beam ‘A’ with its power and frequency will come at the output as a dropped signal or reflected signal, and the power and frequency of optical signal beam ‘B’ is transmitted (here it is blocked). Now, if the biasing current is chosen as logic state ‘0’, then, the opposite incident happens. This phenomenon completely validates the operational function of ADM.

Again, in case of mathematical model of RSOA, shown in figure 1.10, strong pump beam is considered with the wavelength of 1200 nm with power of 10^{5} watt and weak probe beam is taken with the wavelength 1550 nm with power of 5×10^{3} watt. These wavelengths and power are simulated by constant blocks, whose values are changeable, taken from simulink library. These blocks are connected with the RSOA main unit with four conventional switches. In main RSOA block, two MATLAB functions with two multiport switches are used. Again, these functions are properly programmed by means of ‘C’ language for getting the proper output at the output terminal. At this output terminal, both the wavelength of the probe beam (1550 nm) and the power of the pump beam (10^5 watts) are present. This phenomenon fully supports the function of optical RSOA.

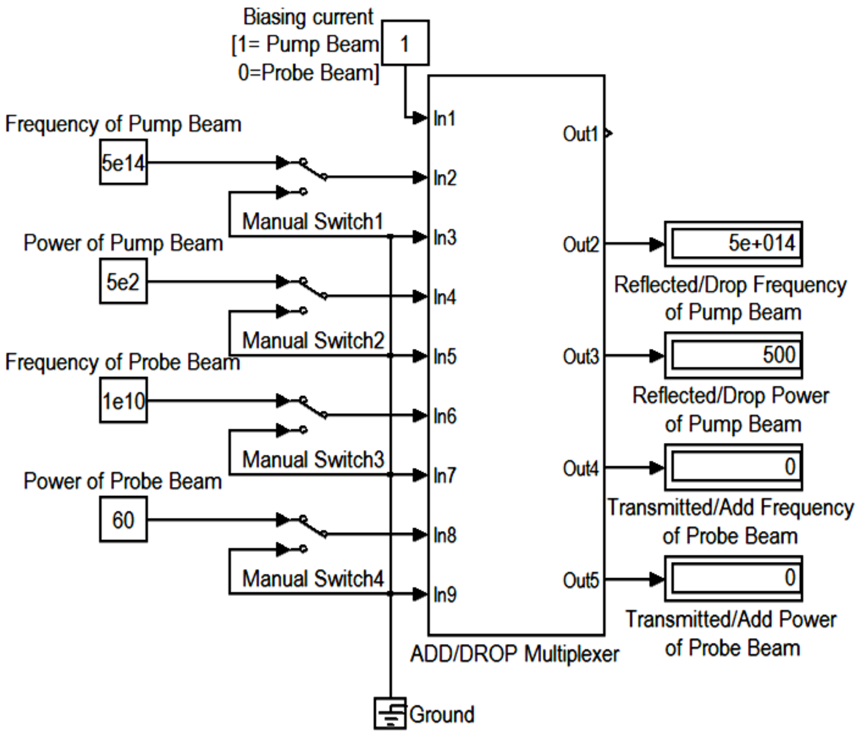


Figure 1.9: Mathematical model of ADM.

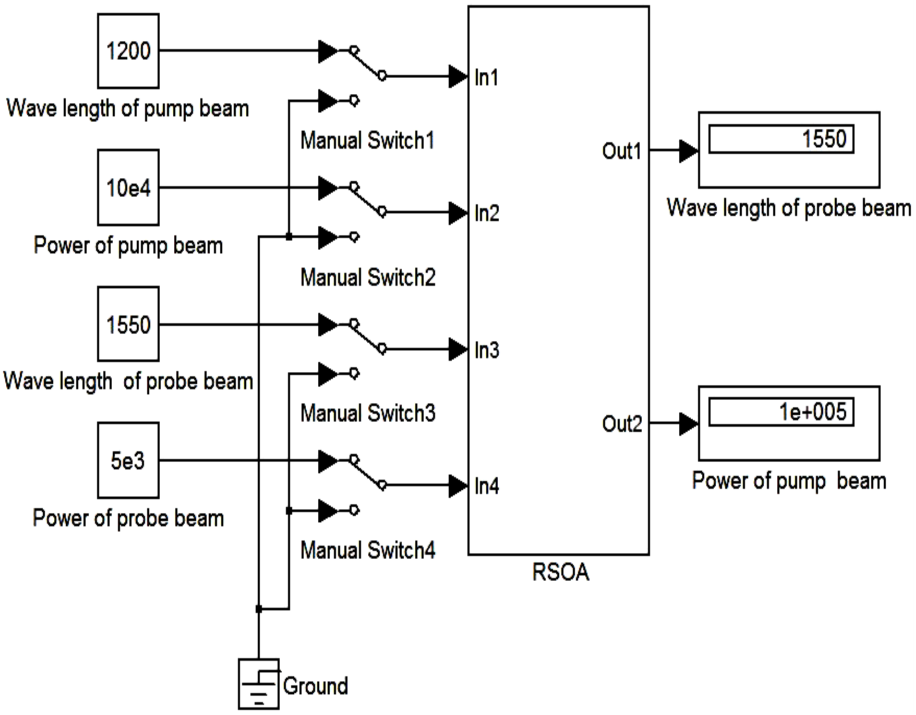


Figure 1.10: The mathematical model of RSOA block.

References

[1.1]. P. S. Lopatinaa_ and V. V. Krishtop, “Distribution of induced birefringence in a lithium niobate crystal in an inhomogeneous external electric field.” J. Opt. Technol. **7**7(6), 399-400 (2010).

[1.2]. J. N. Roy, A. K. Maiti, D. Samanta, S. Mukhopadhyay, “Tree-net architecture for integrated all-optical arithmetic operations and data comparison scheme with optical nonlinear material.” Optical Switching and Networking, 4(3-4), 231–237 (2007).

[1.3]. S. Mukhopadhyay, “An optical conversion system: From binary to decimal and decimal to binary.” Optics Communications (The Netherlands), 76(5-6), 309-312 (15 May, 1990).

[1.4]. Y. Miyoshi, K.Ikeda, H. Tobioka, T. Inoue, S. Namiki, K. Kitayama, “Ultrafast all-optical logic gate using a nonlinear optical loop mirror based multi-periodic transfer function.” Optics Express, 16(4), 2570-2577 (2008).

[1.5]. T. Yatagai, “Optical space-variant logic gate based on spatial encoding technique.” Optics Letters, 11(4), 260-262 (1986).

[1.6]. S. Dutta and S. Mukhopadhyay, “All optical frequency encoding method for converting a decimal number to its equivalent binary number using tree architecture.” Presented and Published in the proceedings of International Conference Of Optics and Photonics (ICOP- 2009), Chandigar, 31st Oct. to 2nd Nov. (2009).

[1.7]. B. Ghosh and S. Mukhopadhyay, “A novel realization of all optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124(21) 4813-4815 (2013).

[1.8]. S. Dutta, S. Mukhopadhyay, “Alternating approach of implementing frequency encoded all-optical logic gates and flip flop using semiconductor optical amplifier.” Optik - Int. J. Light Electron Opt. (2010).

[1.9]. A. K. Ghosh, et al. “Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic.” Optics & Laser Technology, 44(5), 1583-1592 (2012).

[1.10]. B. Ghosh and S. Mukhopadhyay, “A novel realization of all optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124(21), 4813-4815 (2013).

[1.11]. M. J. Connelly, “Semiconductor optical amplifiers.” Springer Science & Business Media, 2007.

[1.12]. X. Wang, et al. “Range intensity coding under triangular and trapezoidal correlation algorithms for 3D super-resolution range gated imaging.” SPIE Security+ Defence. International Society for Optics and Photonics, 2016.

[1.13]. V. Cakmak, et al. “Diffusion-weighted MRI of pulmonary lesions: Comparison of apparent diffusion coefficient and lesion-to-spinal cord signal intensity ratio in lesion characterization.” Journal of Magnetic Resonance Imaging, 45(3), 845-854 (2017).

[1.14]. Y. Wang, et al. “32QAM photonic vector signal generation utilizing a single-drive intensity MZM without pre-coding technique.” Optical Fiber Communication Conference, Optical Society of America, 2016.

[1.15]. R. W. Haushalter, and R. C. Haushalter. “Rare earth down converting phosphor compositions for optically encoding objects and methods and apparatus relating to same.” U.S. Patent No. 9,651,496. 16 May 2017.

[1.16]. S. Preradovic and A. Menicanin, “Printed 3-D stacked chipless RFID tag with spectral and polarization encoding capacity.” Electronics Technology (ISSE), 2016 39th International Spring Seminar, IEEE, 2016.

[1.17]. J. Wang, et al. “Experimental demonstration of polarization encoding quantum key distribution system based on intrinsically stable polarization-modulated units.” Optics express, 24(8), 8302-8309 (2016).

[1.18]. P. Kumar, et al. “Double random phase encoding based optical encryption systems using some linear canonical transforms: Weaknesses and countermeasures.” Linear canonical transforms, Springer, New York, 367-396 (2016).

[1.19]. N. Rawat, “Single-Pixel Based Double Random-Phase Encoding Technique.” Computational Intelligence, Cyber Security and Computational Models, Springer, Singapore, 43-54 (2016).

[1.20]. G. Hu, et al. “Securing image information using double random phase encoding and parallel compressive sensing with updated sampling processes.” Optics and Lasers in Engineering, 98, 123-133 (2017).

[1.21]. H. Liu, et al. “Phase angle encoded upconversion luminescent nanocrystals for multiplexing applications.” Nanoscale, 9(4), 1676-1686 (2017).

[1.22]. D. Lu, et al. “An interference-based optical authentication scheme using two phase-only masks with different diffraction distances.” Optics and Lasers in Engineering, 89, 40-46 (2017).

[1.23]. R. T. Constable, et al. “Accelerated MRI with nonlinear spatial encoding gradients.” U.S. Patent No. 9,229,081, 5 Jan, 2016.

[1.24]. M. A. Thomas, et al. “2-D MR Spectroscopy Combined with 2-D/3-D Spatial Encoding.” eMagRes (2016).

[1.25]. B. Plainchont, et al. “Achieving high resolution and optimizing sensitivity in spatial frequency encoding NMR spectroscopy: from theory to practice.” Physical Chemistry Chemical Physics, 18(33), 22827-22839 (2016).

[1.26]. J. Zhu, et al. “Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination.” Optics express, 24(25), 28549-28560 (2016).

[1.27]. S. Dutta and S. Mukhopadhyay, “All optical frequency encoding method for converting a decimal number to its equivalent binary number using tree architecture.” International Conference Of Optics and Photonics (ICOP-2009), Chandigar, 31st Oct. - 2nd Nov. (2009).

[1.28]. D. Agrawal and J. S. Yadav, “Investigation of the Effectiveness of Modulation Technique for Wireless Communication with QPSK base Encoding.’ 2017.

[1.29]. S. Ma and L. Bo, “A phase retrieval algorithm based on color-frequency encoding for fringe reflection technique.” Eighth International Symposium on Advanced Optical Manufacturing and Testing Technology (AOMATT-2016), International Society for Optics and Photonics, 2016.

[1.30]. H. Zhang, et al. “Selective addressing of solid-state spins at the nanoscale via magnetic resonance frequency encoding.” arXiv preprint arXiv: 1610.06630 (2016).

[1.31]. J. Lee, et al. “Two qubit gate operation using the frequency encoding technique.” Bulletin of the American Physical Society (2017).

[1.32]. B. Knobnob, et al. “Dark–bright optical solitons conversion via an optical add/drop filter for signals and networks security applications.” Optik-International Journal for Light and Electron Optics, 121(19), 1743-1747 (2010).

[1.33]. E. A. M. Fagotto, et al. “All-optical demultiplexing of quaternary amplitude signals with fiber-based optical gates.” Summer Topical Meeting, LEOSST'09.IEEE/LEOS.IEEE (2009).

[1.34]. S. K. Chandra and S. Mukhopadhyay, “All optical alternative approach of conducting NAND and NOR logic gates with phase encoding principle.” Optik-International Journal for Light and Electron Optics, 123(11), 1022-1025 (2012).

[1.35]. S. Mukhopadhyay, “Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems,” Appl. Opt. 31(23), 4622–4627 (1992).

[1.36]. M. G. Saber, et al. “A Compact Silicon Photonic Add-Drop Multiplexer with Misaligned Sidewall Bragg Gratings in a MZI.” CLEO: Science and Innovations, Optical Society of America (2017).

[1.37]. S. Wang, et al. “On-chip reconfigurable optical add-drop multiplexer for hybrid wavelength/mode-division-multiplexing systems.” Optics Letters, 42(14), 2802-2805 (2017).

[1.38]. M. G. Saber, et al. “A CMOS Compatible Ultra-Compact Silicon Photonic Optical Add-Drop Multiplexer with Misaligned Sidewall Bragg Gratings.” IEEE Photonics Journal (2017).

[1.39]. X. Chen, et al. “Demonstration of few-mode compatible optical add/drop multiplexer for mode-division multiplexed superchannel.” Journal of Lightwave Technology, 31(4), 641-647 (2013).

[1.40]. P. Wolff, et al. “Electrical add/drop multiplexer with pass through port related applications.” U.S. Patent No. 9,479,258, 25 Oct. 2016.

[1.41]. S. Singh, et al. “Design and analysis of all-optical up-and down-wavelength converter based on FWM of SOA-MZI for 60 Gbps RZ data signal.” Photonic Network Communications, 1-10 (2017).

[1.42]. D. Fitsios, et al. “Dual SOA-MZI Wavelength Converters Based on III-V Hybrid Integration on a $\mu {\rm m} $-Scale Si Platform.” IEEE Photonics Technology Letters, 26(6), 560-563 (2014).

[1.43]. Y. Mao, et al. “Broad-band all-optical wavelength conversion of differential phase-shift keyed signal using an SOA-based nonlinear polarization switch.” Chinese Physics Letters, 33(3), 034204 (2016).

[1.44]. R. Matsumoto, et al. “A Novel Wavelength Converter for PAM Signal based on XGM in cascaded SOAs.” Asia Communications and Photonics Conference, Optical Society of America (2015).

[1.45]. C. Qin, et al. “Polarization dependence of patterning effects in quantum well semiconductor optical amplifier-based wavelength conversion.” Optica Applicata, 45(2), (2015).

[1.46]. R. Matsumoto, et al. “Pattern-independent wavelength conversion of PAM signals in SOAs.” Opto Electronics and Communications Conference (OECC), 2016 International Conference on Photonics in Switching (PS),21st IEEE (2016).

[1.47]. P. P. Baveja, et al. “All-optical semiconductor optical amplifier-based wavelength converters with sub-mW pumping.” IEEE Photonics Technology Letters, 25(1), 78-80 (2013).

[1.48]. P. P. Sarkar, B. Ghosh, S. N. Patra, “Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer.” Journal of Optical Technology, 83(4), 257–262 (2016).

[1.49]. B. Ghosh, et al. “A Novel Approach to Realize of All Optical Frequency Encoded Dibit Based XOR and XNOR Logic Gates Using Optical Switches with Simulated Verification.” Optics and Spectroscopy, 124(3), 337-342 (2018).

[1.50]. S. Saha, S. Biswas, S. Mukhopadhyay, “Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach–Zehnder interferometer-based semiconductor optical amplifier.” IET Optoelectronics, 11(5), 201-207 (2017).

[1.51]. B. Sarkar, et al. “All-optical method of generation of Phase Shift Keying data using optical pockels crystal.” Journal of Optics, 53(2), 1623-1628 (2024).

[1.52]. H. Chen, et al. “Simple and reconfigurable all-optical logic gate.” Optics and Laser Technology, 170(110297), 1-6, (2024).

CHAPTER-2

A new method of realization with simulation process to implement all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches.

Abstract

Over the past few decades, optics has demonstrated significant potential for performing parallel logic, arithmetic, and algebraic operations, thanks to its incredibly fast communication and computation speeds. Numerous researchers have proposed various logical and sequential operations utilizing all optical frequency encoding techniques. Here, the authors have proposed the all optical dibit representation technique with the advantages of high speed operation and also the reducing bit error problem. Implementing this fact, we have projected all optical frequency encoded dibit based XOR and XNOR logic gates using add/drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA) type optical switches. The functionality of these optical gates has been confirmed through accurate simulations conducted using simulink tools of MATLAB (R2008a) software.

Work reported in this chapter was published in:

i. **Bitan Ghosh**, Partha Pratim Sarkar and Sourangshu Mukhopadhyay “A novel approach to realize of all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches with simulated verification." Optics and Spectroscopy 124.3 (2018): 337-342.

ii. "Realization of all optical frequency encoded dibit based XOR and XNOR logic gates using RSOA with MATLAB verification" By **Bitan Ghosh**, Partha Pratim Sarkar, Smita Hazra, Subhendu Biswas, Sourangshu Mukhopadhyay and Sankar Narayan Patra, on International Conference on Applications of Mathematics to Nonlinear Sciences (AMNS-2016), at Association of Nepalese Mathematicians in America and Nepal Mathematical Society; Department of Mathematics, Tribhuvan University and Mathematics Group, Department of Natural Sciences, Kathmandu University, Kathmandu, Nepal, INDIA, on 26th-29th May, 2016.

2.1 Introduction

Basically, photon can be used for super-fast information processing[2.1], due to its very high speed of operation. So, it is an appropriate information transporter than electron. Different types of encoding techniques are needed for implementing the all optical logic and arithmetic devices[2.2]. Various types of encoding techniques are frequency encoding[2.3-2.5], intensity encoding, phase encoding, spatial encoding, polarization encoding etc. In general, the frequency of a light beam remains constant and unaffected during processes such as reflection, refraction, and absorption. So, frequency encoding technique is the most consistent encoding technique. In this encoding technique, two different frequencies of light beams represent the two different states of information at the time of data computation[2.6-2.8] and encoding process. If, frequency of light beam of a specific value is considered as digital logic state '0' then, frequency of light beam of another value will be treated as digital logic state '1'. For this reason, if υ_1 frequency of light beam is considered as digital logic state '0' then υ_2 frequency of light beam will be treated as digital logic state '1'.

Now, the dibit representation technique[2.9] can be done to represent a digital logic state by two consecutive bit positions. So, the digital logic state '0' is represented as dibit logic state <0><1> and digital logic state '1' is represented as dibit logic state <1><0> respectively. These two positions may be considered as two different frequencies. That means, the occurrence of the two frequencies of light beams side by side $<\upsilon_1><\upsilon_2>$ represents the digital low logic state '0' and $<\upsilon_2><\upsilon_1>$ does the same as the digital high logic state '1'. This technique in optics for logical operation was first proposed by S. Mukhopadhyay[2.10]. Here, the authors have projected all optical frequency encoded dibit based XOR and XNOR logic gates using add/drop multiplexer[2.11] and reflected semiconductor optical amplifier[2.12] type optical switches and developed the dibit representation with appropriate dibit checking facility.

Already, dibit based logic gates are exploited in few papers, reporting in different journals. Dibit-based logic gates have already been utilized in several studies, which have been published in various journals. But in this chapter authors have proposed new concept of implementing frequency encoded all optical dibit based XOR and XNOR logic gates with a novel modification of dibit checking unit, which prevents the inappropriate input to enter into the dibit based logic gates. As the inputs in the form of dibit logic state and are the improper inputs in case of dibit system then, the dibit checking unit restricts those inputs to operate. These facilities provide the advantage the reliability of the logic gates.

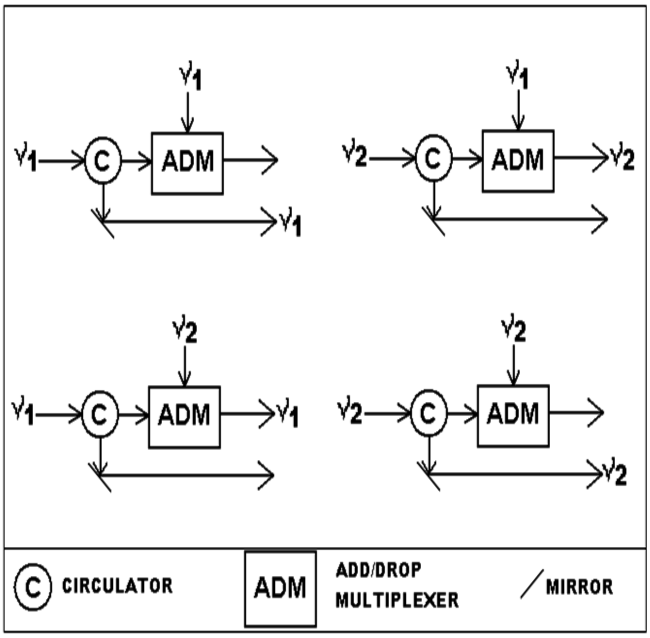


Figure 2.1: Block diagram of ADM block.

Add/drop multiplexer (ADM) is a frequency selective optical switching device. When this optical switching device is biased with a specific biasing then it opposes the specific frequency of light beam and passes other frequency of light beam. Opposite incident happens if the biasing changes, which is shown in figure 2.1. Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device[2.13-2.16], where a weak probe beam of light of frequency say, υ_1 and a strong pump beam of light of frequency say, υ_2 are inserted to the input terminals (shown in figure 2.2). Then this switch will provide the output light beam in form of frequency of probe beam (say, υ_1 frequency) and the power of the pump beam. In this manner, it could be developed into highly promising optical devices for performing various all-optical logical operations[2.17-2.18].

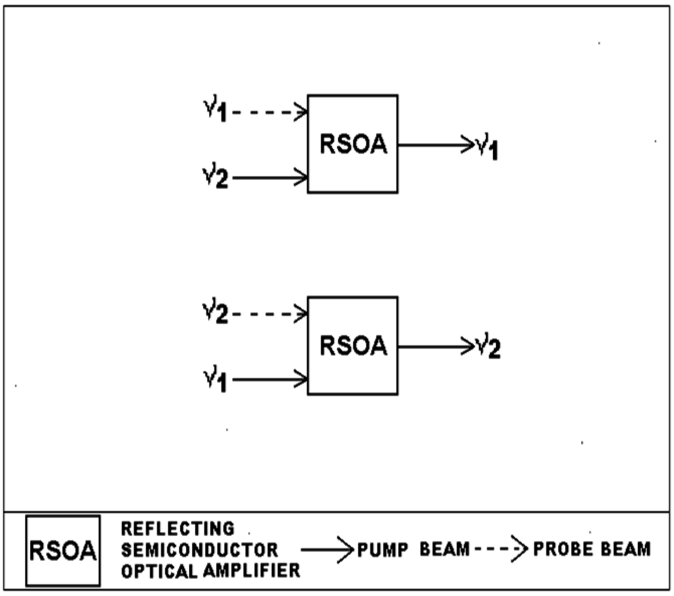


Figure 2.2: Block diagram of RSOA block.

2.2 Scheme of realization of frequency encoded dibit based XOR & XNOR logic gates

In figure 2.3, for realizing the dibit based two inputs XOR gate the input channels are considered as ‘A’ and ‘B’ respectively. These two input terminals ‘A’ and ‘B’ are subdivided further as ‘A′’ and ‘A′′’, ‘B′’ and ‘B′′’ correspondingly to provide inputs as dibit form to the system.

Initially, υ_1 and υ_2 frequencies of light are given to the input channels of ‘A′’, ‘A′′’ and ‘B′’, ‘B′′’ simultaneously. It checks the real dibit input combinations because there is a real dibit checking provision by ADM_1 with $RSOA_1$ and ADM_4 with

RSOA$_3$ blocks. The light beam of υ_1 frequency coming from ‘A′’ acts as biasing terminal of ADM$_1$. So, the light beam of υ_2 frequency coming from ‘A′′’ passes through the ADM$_1$. Therefore, dibit input <0><1> or <υ_1><υ_2> frequencies of light are injected in form of probe beam and pump beam respectively at channel ‘A’ section to RSOA$_1$. So, υ_1 frequency of light beam comes out from RSOA$_1$ as output. By the same way, υ_1 frequency of light beam also comes out from RSOA$_3$ as output for the given dibit input <υ_1><υ_2> or input <0><1> to channel ‘B’ section. Now, output of RSOA$_1$, i.e. υ_1 frequency of light goes to RSOA$_2$ as pump beam because ADM$_2$ is biased by υ_2 frequency of light beam. But RSOA$_2$ will not act due to absence of probe beam. Now, one part of this light beam goes to RSOA$_4$ as pump beam with υ_1 frequency, but there is a fixed light beam as probe beam of υ_2 frequency. So, υ_2 frequency of light beam comes from RSOA$_4$ as output and this light beam goes to RSOA$_5$ as a pump beam. Now, from RSOA$_3$ υ_1 frequency of light is passed by ADM$_5$ and comes as a probe beam of RSOA$_5$. For this reason $\upsilon 1$ frequency of light beam comes out from RSOA$_5$ and goes directly to ‘Y_1'’ of output terminal ‘Y’. Now one part of this υ_1 frequency of light beam goes to ADM$_7$. As this block is biased by υ_2 frequency, so, it passes the light beam of υ_1 frequency and is connected with the pump beam port of RSOA$_6$ but there is a fixed light beam of υ_2 frequency at the probe beam terminal of RSOA$_6$. For that reason υ_2 frequency of light beam comes out from RSOA$_6$ and goes to ‘Y_1''’ of output terminal ‘Y’. So, we may get dibit output <υ_1><υ_2> (or <0><1> or digital logic state ‘0’) at the output terminal ‘Y’ (or, at output terminals ‘Y_1'’ and ‘Y_1''’ respectively) for given dibit inputs of <υ_1><υ_2> or <0><1> and <υ_1><υ_2> or <0><1> or, digital logic state combination ‘0’ and ‘0’ at input terminals ‘A’ and ‘B’ respectively. This output is satisfied by XOR logic for the digital logic state input combination ‘0’ and ‘0’ which provides ‘0’ output (shown in table 2.1). Now, if we use this dibit output bits at ‘Y_2'’ and ‘Y_2''’ terminals in reverse way as shown in figure 2.3, then we may get the dibit output <υ_2><υ_1> or <1><0> or digital logic state ‘1’ at the output terminal. This dibit output is satisfied by XNOR logic for the digital logic state input combination ‘0’ and ‘0’ at both input terminals.

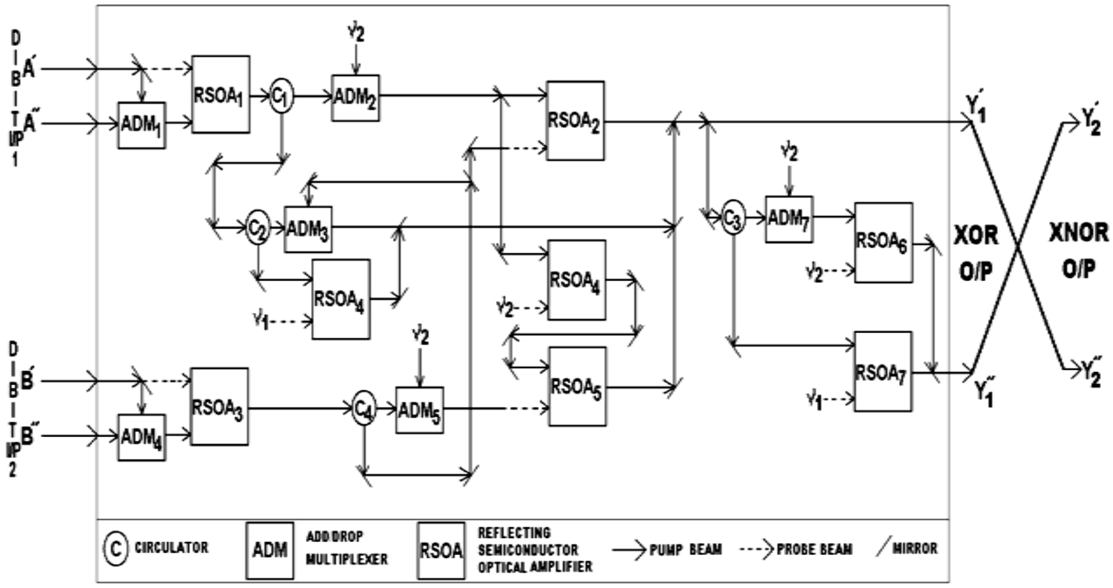


Figure 2.3: Block diagram of the dibit based XOR & XNOR logic gates.

Secondly, υ_1 and υ_2 frequencies of light beam are given to the input channels of ‘A'’, ‘A''’ but υ_2 and υ_1 frequencies of light are inserted to the ‘B'’, ‘B''’ input channels. Now both the inputs will be checked for true dibit combinations. So, υ_1 and υ_2 frequencies of light beam are come from $RSOA_1$ and $RSOA_3$ respectively. Since, ADM_2 is biased by υ_2 frequencies of light beam, output of $RSOA_1$ i.e. υ_1 frequency of light goes to $RSOA_2$ as pump beam. As the previous combination, one part of this light beam of υ_1 frequency goes to $RSOA_5$ as a pump beam. But the $RSOA_5$ will not work as there is no probe beam. Now, υ_2 frequency of light beam, which is coming from $RSOA_3$, is reflected by ADM_5 and comes as a probe beam of $RSOA_2$. This υ_2 frequency of light beam comes out from $RSOA_2$ and goes to ‘Y_1'’ of output terminal ‘Y’. Now, one part of this light beam goes to ADM_7 and as per property of ADM the light beam is reflected by ADM_7 and is connected to pump beam port of $RSOA_7$. But, a constant light beam of υ_1 frequency is present at the probe beam terminal of RSOA$_7$. So, υ_1 frequency of light beam comes out from RSOA$_7$ and goes to ‘Y_1''’ of output terminal ‘Y’. Thus, we may obtain dibit output $<\upsilon_2><\upsilon_1>$ or <1><0> or digital logic state ‘1’ at the output terminal ‘Y’ (combination of ‘Y_1'’ and ‘Y_1''’) for given dibit inputs of $<\upsilon_1><\upsilon_2>$ or <0><1> and $<\upsilon_2><\upsilon_1>$ or <1><0> or, digital logic state combination ‘0’ and ‘1’ at input terminals ‘A’ and ‘B’ respectively and this is also satisfied by XOR logic (shown in table 2.1). Now if we use this dibit output bits at ‘Y_2'’ and ‘Y_2''’ terminals in reverse way, then we may get the dibit output $<\upsilon_1><\upsilon_2>$ or <0><1> or digital logic state ‘0’ at the output terminal, which satisfies the XNOR logic.

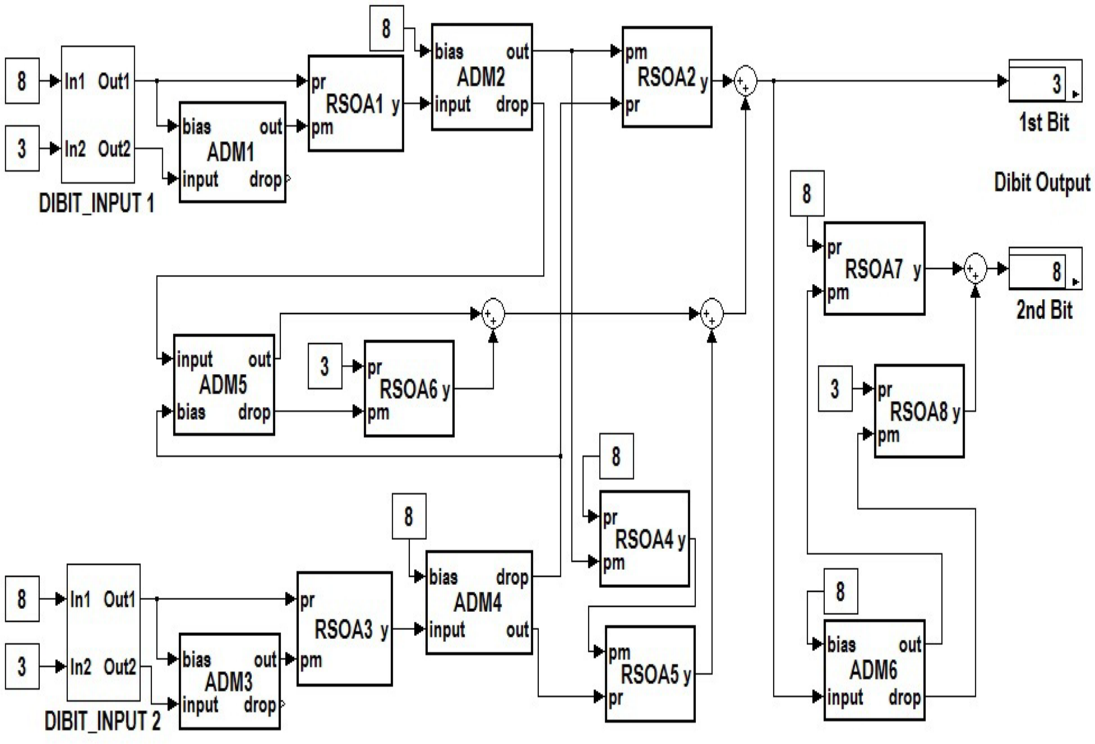
Thirdly, υ_2 and υ_1 frequencies of light beam are injected to the input channels of ‘A'’, ‘A''’ but υ_1 and υ_2 frequencies of light are applied to the ‘B'’, ‘B''’ input channels. But, after the dibit checking of both the inputs, υ_2 and υ_1 frequencies of light beam come from RSOA$_1$ and RSOA$_3$ respectively. The υ_2 frequency of light beam is reflected by the ADM$_2$ (biased by υ_2 frequency) and goes to the input terminal of ADM$_3$ and passed by ADM$_3$ as there is no biasing input and goes directly to ‘Y_1'’ of output terminal ‘Y’. Besides this, from RSOA$_3$ υ_1 frequency of light is passed by ADM$_5$ and comes as a probe beam of RSOA$_5$. But the RSOA$_5$ will not work as there is no pump beam of RSOA$_5$. Now, the part of the light beam of υ_2 frequency coming from ADM$_3$, goes properly as pump beam to RSOA$_7$ (with constant probe beam of υ_1 frequency) and this υ_1 frequency of light beam will come to the ‘Y_1''’ of output terminal ‘Y’. Again, we may find the dibit output $<\upsilon_2><\upsilon_1>$ or <1><0> or digital logic state ‘1’ at the output terminal ‘Y’ with the combination of ‘Y_1'’ and ‘Y_1''’ channels for given dibit inputs of $<\upsilon_2><\upsilon_1>$ or <1><0> and $<\upsilon_1><\upsilon_2>$ or <0><1> or, digital logic state combination ‘1’ and ‘0’ at input terminals ‘A’ and ‘B’ respectively, satisfying the XOR logic. But if we use this dibit output bits at ‘Y_2'’ and ‘Y_2''’ terminals in reverse way, then we may get the dibit output <υ_1><υ_2> or <0><1> or digital logic state ‘0’ at the output terminal, satisfying the XNOR logic.

Finally, if we insert υ_2 and υ_1 frequencies of light beam to the input channels of ‘A'’, ‘A''’ and ‘B'’, ‘B''’ simultaneously then light beams of υ_2 frequency will come from both RSOA$_1$ and RSOA$_3$ after suitable checking of input dibit combinations. Now, both the light beams are reflected by ADM$_2$ and ADM$_5$ as these ADMs are biased by υ_2 frequency. Then the light beams are coming to the input terminal of the ADM$_3$ and as probe beam of RSOA$_2$ respectively. But the RSOA$_2$ will not work properly for absence of pump beam. But, the part of the light beam of υ_2 frequency, reflected by ADM$_5$, acts as biasing input of ADM$_3$. So, the input light beam at the input terminal of ADM$_3$ is reflected and is coming at the pump beam port of RSOA$_4$. As presence of the light beam of υ_1 frequency at the probe beam input port of RSOA$_4$, the beam of light of υ_1 frequency is coming from RSOA$_4$ as output and goes to the ‘Y_1'’ of output terminal ‘Y’. Again, one part of this light beam goes through ADM$_7$ and as pump beam of RSOA$_6$ (with constant probe beam of υ_2 frequency). So, υ_2 frequency of light beam comes out from RSOA$_6$ and goes to ‘Y_1''’ of output terminal ‘Y’. Thus, we may get dibit output <υ_1><υ_2> or <0><1> or digital logic state ‘0’ at the output terminal ‘Y’ for given dibit inputs of <υ_2><υ_1> or <1><0> and <υ_2><υ_1> or <1><0> or, digital logic state combination ‘1’ and ‘1’ at input terminals ‘A’ and ‘B’ respectively. Finally, these outputs are satisfied by truth table of XOR logic (shown in table 2.1). Again, if we use this dibit output bits at ‘Y_2'’ and ‘Y_2''’ terminals in reverse way as shown in figure 2.3, then we may obtain the dibit output <υ_2><υ_1> or <1><0> or digital logic state ‘1’ at the output terminal, satisfying the XNOR logic also.

2.3 Simulation process of frequency encoded dibit based XOR & XNOR logic gates

For the simulation process here, MATLAB (R2008a) software have been used to frequency encoded all optical dibit XOR & XNOR logic gates with dibit checking using RSOA and ADM respectively. Simulating diagram is drawn in such a way that, the dibit inputs and outputs are easily recognized and are labeled by the names as "DIBIT_INPUT 1" and "DIBIT_INPUT 2" for inputs and "Dibit Output" for output. The dibit inputs and output are consisted of two sub-parts and are labeled by "1st Bit" and "2nd Bit" respectively. Using the software, the RSOA block units are appropriately programmed and is written by 'C' language coding for getting the appropriate output at the output port, shown in figure 2.4 and figure 2.5. Here, two inputs viz. "pr" (probe beam) and "pm" (pump beam) and the output by "y" in RSOA blocks. The RSOA blocks are designed in such a way that, the signal of probe beam comes out at the output of RSOA with the presence of both the signals at pump and probe beam ports. If we consider the light beam of pump and probe beams as say "3 peta Hz" or, the beam of light of υ_1 frequency or, digital low logic state "0" and "8 peta Hz" or, the beam of light of υ_2 frequency or, digital high logic state "1" correspondingly at the input terminals of RSOA, then we obtain output as "8 peta Hz" or, the beam of light of υ_2 frequency or, digital high logic state "1" at the output terminal of these blocks. Here, the value of the output unit changes if the values of the pump beam and probe beam respectively are altered accordingly.

The ADM block has been designed so that when a sequence of frequencies is applied to its input terminal, it allows all other frequencies to pass through and drops a particular frequency depending upon the biasing. Now, if the biasing is changed then the frequency of the dropped terminal change accordingly. Here, for particular biasing at "bias" terminal, this block drops one frequency coming from "input" terminal to "drop" terminal and passes other frequencies to "out" terminal if the input frequencies are present at the ADM unit, represented by "8 peta Hz" or, the beam of light of υ_2 frequency or, digital high logic state "1" and "3 peta Hz" or, the beam of light of υ_1 frequency or, digital low logic state "0". If the value of biasing is changed, opposite incident happens. Now these types of two block units of optical switches are joined together and keeping the same design using the block diagram of all optical dibit based XOR & XNOR logic gates (shown in figure 2.3).



Frequency 3 = ν_1 = D.S = 0, Frequency 8 = ν_2 = D.S = 1
D.S.= Digital State, pr = Probe Beam, pm = Pump Beam
ADM = Add/Drop Multiplexure, RSOA = Reflected Semiconductor Optical Amplifier

Figure 2.4: Simulation model of the dibit based XOR logic gate.

Now, considering <3><8> as digital logic states '0' and <8><3> as digital logic states '1', if <8><3> and <8><3> are applied at the two dibit input terminals of the simulated model, we get <3><8> at the output terminal of this simulated block. Similarly, for the input combinations <3><8> and <3><8>, the output repeats the same value i.e. <3><8>. But at the output we get <8><3> for the dibit inputs <3><8> and <8><3> and for the dibit inputs <8><3> and <3><8>.

Finally, this simulative functional model fully satisfies the truth table of all optical dibit based XOR logic gate, which is shown in table 2.1.

By the same way, simulink tools of MATLAB (R2008a) software have been used for simulation model of the dibit based XNOR logic gate. Here, by the same encoding technique, if we apply <8><3> and <8><3> to the dibit input terminals, we get <8><3> at the output terminal. Similarly, we get same dibit output as <8><3> for the dibit inputs <3><8> and <3><8>. But, for the rest all possible combinations of dibit inputs like, <3><8> and <8><3>, <8><3> and <3><8>, we get <3><8> as dibit output. So, this simulated block fully satisfies the truth table of frequency encoded all optical dibit based XNOR logic gate, which is shown in table 2.1.

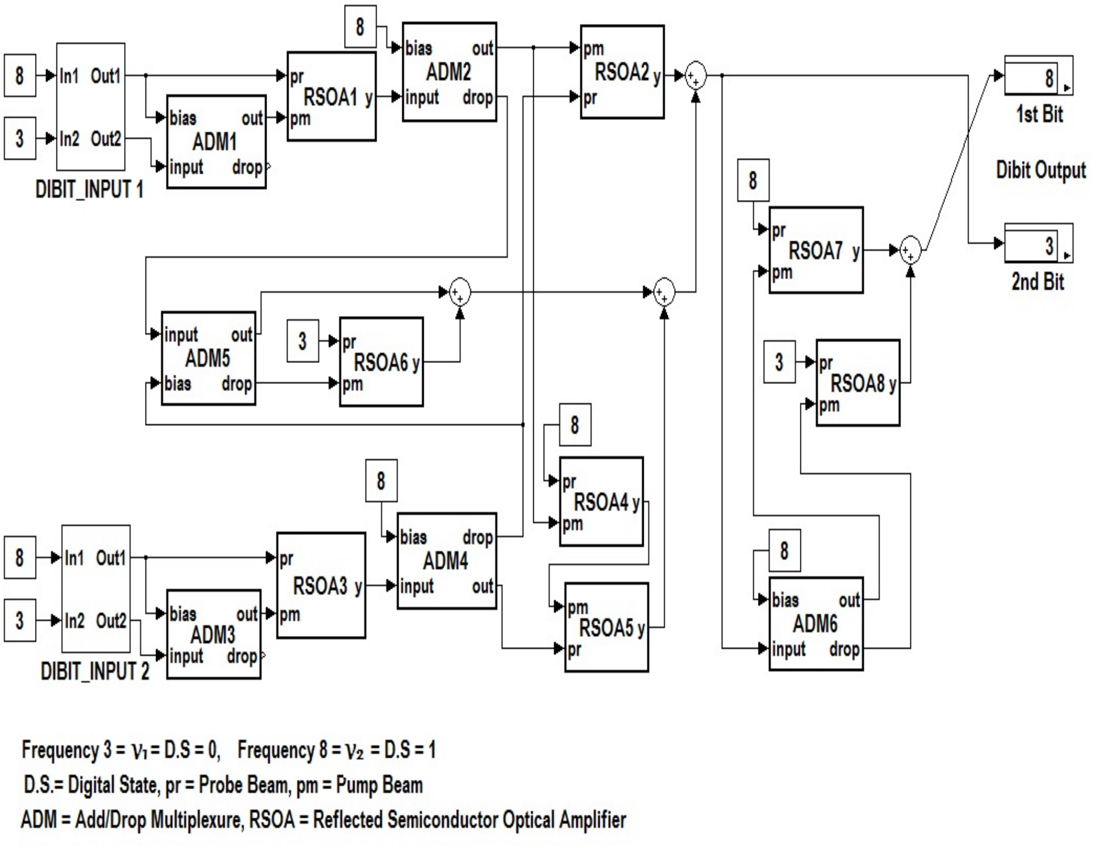


Figure 2.5: Simulation model of the dibit based XNOR logic gate.

2.4 Results and discussion

Dibit Input 1		Digital form	Dibit Input 2		Digital form	Dibit XOR Output		Digital form	Dibit XNOR Output		Digital form
A'	A''	A	B'	B''	B	Y_1'	Y_1''	Y_1	Y_2'	Y_2''	Y_2
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1

Table 2.1: Truth table of dibit based optical XOR & XNOR logic gates.

All the results obtained from the simulation processes for XOR and XNOR logic gates align perfectly with their respective truth tables. This alignment validates the accuracy and reliability of the simulation outcomes. Consequently, we have compiled a comprehensive table (table 2.1) that consolidates all the findings related to optical frequency encoded dibit-based XOR and XNOR logic gates. This combined table serves as a convenient reference, encapsulating the behavior of both logic gates in one place.

Here’s a breakdown of the key points:

A. Simulation results and truth tables alignment

(a) The simulation processes for XOR and XNOR logic gates have been meticulously conducted.

(b) The results from these simulations have been compared against the standard truth tables for XOR and XNOR gates.

(c) The outcomes from the simulations match the expected results as per the truth tables, confirming the correctness of the simulations.

B. Optical frequency encoded dibit based logic gates

(a) The logic gates in problem are based on optical frequency encoding, specifically utilizing dibits (pairs of bits).

(b) This encoding technique is applied to both XOR and XNOR gates, allowing for the representation and processing of binary data in optical form.

C. Combined table (table 2.1)

(a) To streamline the presentation of the results, a combined table (table 2.1) has been created.

(b) This table consolidates the simulation results for both XOR and XNOR gates, providing a comprehensive overview.

(c) The combined table facilitates easy comparison and reference, ensuring that all relevant data is accessible in one location.

In essence, the combined table (table 2.1) showcases the confirmed and validated outcomes for optical frequency encoded dibit-based XOR and XNOR logic gates, reflecting the fidelity of the simulation processes against the theoretical truth tables.

2.5 Conclusions

To realize the all optical operations, advantages of frequency encoding as well as dibit representation technique are exploited here. This mechanism is a reliable, authentic operation and it also causes the reduction in bit-error problem with better signal to noise ratio. Again, the dibit inspection process reduces errors on wrong dibit input states. Using this mechanism, we can expect a high degree of parallelism with ultra-fast operational speed. This encoding technique aids in the implementation of all optical logical operations, ensuring accurate and dependable results. With the realization and the simulated results and observation of the above logic gates using optical switches, these logic gates can be used for preparing all optical computational devices like adder/sub-tractor, correlation and sequence detector etc. So, it supports an ultra-high speed operation and exhibit a real time operation with high reliability.

References

[2.1]. S. Mukhopadhyay, “Role of optics in super-fast information processing”, Indian J. Phys., 84 (8), 1069-1074 (2010).

[2.2]. S. K. Garai and S. Mukhopadhyay, “A method of optical implementation of frequency encoded different logic operations using second harmonic& difference frequency generation techniques in non-linear material.” Optik-International Journal for Light and Electron Optics, 121 (8), 715-721 (2010).

[2.3]. P. P. Sarkar, B. Satpati and S. Mukhopadhyay, “New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors.” Journal of Optics, 42 (4), 360-366 (2013).

[2.4]. P. P. Sarkar, B. Ghosh and S. N. Patra, “Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer.” Journal of Optical Technology 83 (4), 257-262 (2016).

[2.5]. S. Dutta and S. Mukhopadhyay, “Alternating approach of implementing frequency encoded all-optical logic gates and flipflop using semiconductor optical amplifier.” Optik-International Journal for Light and Electron Optics, 122 (12), 1088-1094 (2011).

[2.6]. A. K. Ghosh, A. Bhattacharya, M. Raul and A. Basuray, “Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic.” Optics & Laser Technology, 44 (5), 1583-1592 (2012).

[2.7]. B. Ghosh, R. R. Pal and S. Mukhopadhyay, “An all-optical integrated system for implementing arithmetic operation in 2’s complement method with the active participation of non-linear material based switches.” Indian J. Phys. 84 (8), 1101-1109 (2010).

[2.8]. H. Q. Jin, J. R. He, Z. B. Cai, J. C. Liang and L. Yi, “Analytical traveling wave and soliton solutions of the generalized non autonomous nonlinear Schrödinger equation with an external potential.” Indian Journal of Physics, 87 (12), 1243-1250 (2013).

[2.9]. B. Ghosh and S. Mukhopadhyay, “A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124 (21), 4813-4815 (2013).

[2.10]. S. Mukhopadhyay, “Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems.” Appl. Opt, 31 (23), 4622-4623 (1992).

[2.11]. A. N. Z. Rashed, “Optical Add Drop Multiplexer (OADM) Based on Dense Wavelength Division Multiplexing Technology in Next Generation Optical Networks.” International Journal of Multimedia & Ubiquitous Engineering, 7 (1), 1-14 (2012).

[2.12]. H. Kim, et al. “Degradation characteristics of red light-emitting CuInS2/ZnS quantum dots as a wavelength converter for LEDs.” Electrochemical and Solid-State Letters, 14 (10), K55-K57 (2011).

[2.13]. P. Singh, S. Kar and V. K. Jain, “Performance of all-optical WDM network in presence of four-wave mixing, optical amplifier noise, and wavelength converter noise.” Fiber and Integrated Optics, 26(2), 79-97 (2007).

[2.14]. Abd El–Naser A. Mohammed, et al. “Optical Add Drop Multiplexers with UW-DWDM Technique in Metro Optical Access Communication Networks.” Nonlinear Optics, Quantum Optics: Concepts in Modern Optics, April, 42(2), 145-159 (2011).

[2.15]. P. P. Sarkar, B. Satpati and S. Mukhopadhyay, “Analytical and simulative studies on optical NOR and controlled NOR logic gates with semiconductor optical amplifier.” Optik-International Journal for Light and Electron Optics, 125(3), 1333-1336 (2014).

[2.16]. L. Q. Guo and M. J. Connelly, “A poincare approach to investigate nonlinear polarization rotation in semiconductor optical amplifiers and its applications to all optical wavelength conversion.” Proc. of SPIE, 6783(678325), 1–5 (2007).

[2.17]. I. Kang, et.al, “All-optical XOR and XNOR operations at 86.4 Gb/s using a pair of semiconductor optical amplifier Mach-Zehnder interferometers,” Opt. Express 17, 19062-19066 (2009).

[2.18]. B. Ghosh, S. Biswas and S. Mukhopadhyay, “A novel method of all-optical wavelength encoded logic and inhibitor operations with dibit representation technique.” Optik-International Journal for Light and Electron Optics, 4(126), 483-489 (2015).

CHAPTER-3

A new approach to realize an all optical frequency encoded dibit based digital multiplexer circuit using optical switches with simulated verification.

Abstract

Optics is considered a highly promising option because of its extremely high communication and computation speed. Consequently, numerous logical and sequential operations have been proposed by various researchers using all optical frequency encoding techniques. In this chapter, the authors introduce an all optical dibit representation technique, which offers the benefits of high speed operation and reduced bit error rates. Leveraging this approach, we propose an all optical frequency encoded dibit based multiplexer, utilizing optical switches such as the reflected semiconductor optical amplifier and add/drop multiplexer. The functionality of this system has been validated and conducted by the software MATLAB (R2008a).

Work reported in this chapter was published in:

i. “A novel approach to realize of all optical frequency encoded dibit based multiplexer using optical switches.” By **Bitan Ghosh**, Partha Pratim Sarkar, Smita Hazra, Sourangshu Mukhopadhyay and Sankar Narayan Patra, in International Conference on Modeling, Computing and Technological Innovations (ICMCTI-2017), at UIT, The University of Burdwan, West Bengal – 713104, on 23-25th March, 2017.

3.1 Introduction

Photon can be used for super fast information processing, due to its very high speed of operation. So, it is an appropriate information transporter than electron. Now, implementation of the all optical logic and arithmetic devices[3.1-3.2] needs different types of encoding techniques like, frequency encoding[3.3-3.4], intensity encoding, phase encoding[3.5-3.6], spatial encoding, polarization encoding[3.7] etc. Among all these encoding principles frequency coding technique is the best technique, as under reflection, refraction, absorption processes the frequency parameter of a particular light beam remains constant. During encoding, two distinct states of information can be represented by two different frequencies using the frequency encoding or decoding technique. The existence of a definite frequency of beam of light is considered as digital low logic state ‘0’ and another definite frequency of light beam is presented as digital high logic state ‘1’. Here, if light beam of υ_1 frequency is considered as digital logic state ‘0’ then υ_2 frequency of light beam is treated as digital logic state ‘1’.

The dibit representation technique[3.8] allows the representation of a digital logic state using two consecutive bit positions. Therefore, the digital logic state ‘0’ is represented as dibit logic state [0][1] and digital logic state ‘1’ is represented as dibit logic state [1][0] respectively. These two bit positions may be considered as two different frequencies. In this context, the presence of frequencies $[\upsilon_1][\upsilon_2]$ indicates the digital low logic state '0', while $[\upsilon_2][\upsilon_1]$ indicates the digital high logic state '1'.

Here, authors have proposed all optical frequency encoded dibit based digital multiplexer (MUX) circuit, which selects a specific dibit input from two different dibit inputs, with the help of add/drop multiplexer (ADM)[3.9] and reflected semiconductor optical amplifier (RSOA)[3.10] type optical switches and also developed the dibit representation with appropriate dibit checking facility, which prevents the inappropriate input to enter into the dibit based circuit. For example, if the input is in the form of dibit logic state [0][0] and [1][1], the dibit checking unit restricts those inputs to operate as these are the improper inputs in case of dibit system.

These facilities offer significant advantages in both time management and the overall reliability of the digital circuit. Time management benefits arise from streamlined processes and optimized workflows facilitated by these tools or resources. They enable tasks to be completed more efficiently, reducing turnaround times and enhancing productivity.

Moreover, the increased reliability of the digital circuit results from the consistent and accurate performance enabled by these facilities. By ensuring that operations are conducted under controlled and predictable conditions, they minimize errors and mitigate risks associated with circuit malfunction or failure. This reliability is crucial in maintaining consistent operation and performance standards, contributing to the overall effectiveness and dependability of the digital circuit in various applications[3.11-3.15].

Add/drop multiplexer (ADM) is a frequency selective optical switching device. If this device is biased by a specific biasing then it only does not pass the specific frequency of beam of light and passes other frequency of beam of light. Opposite incident happens if the biasing current changes. Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device, where a weak probe beam of light of frequency say, υ_1 and a strong pump beam of light of frequency say, υ_2 are inserted to the input terminals. Then this switch will provide the output light beam in form of frequency of probe beam (say, υ_1 frequency) and the power of the pump beam. Therefore they could be established as very promising optical devices for conducting many all optical logical operations[3.16-3.18].

3.2 Scheme of realization of frequency encoded all optical dibit based multiplexer

Here, 2×1 MUX is considered having two data input channels as ‘A’ and ‘B’ respectively for realizing the dibit based MUX, in figure 3.1. From left side of the diagram, the two input channels or terminals i. e. ‘A’ and ‘B’ are separated further to provide inputs of light beams in dibit form and are denoted as ‘A′’ and ‘A′′’, ‘B′’ and ‘B′′’ in that order. And a selection channel is considered as ‘S’ (subdivided into ‘S′’ and ‘S′′’) for providing dibit selection line.

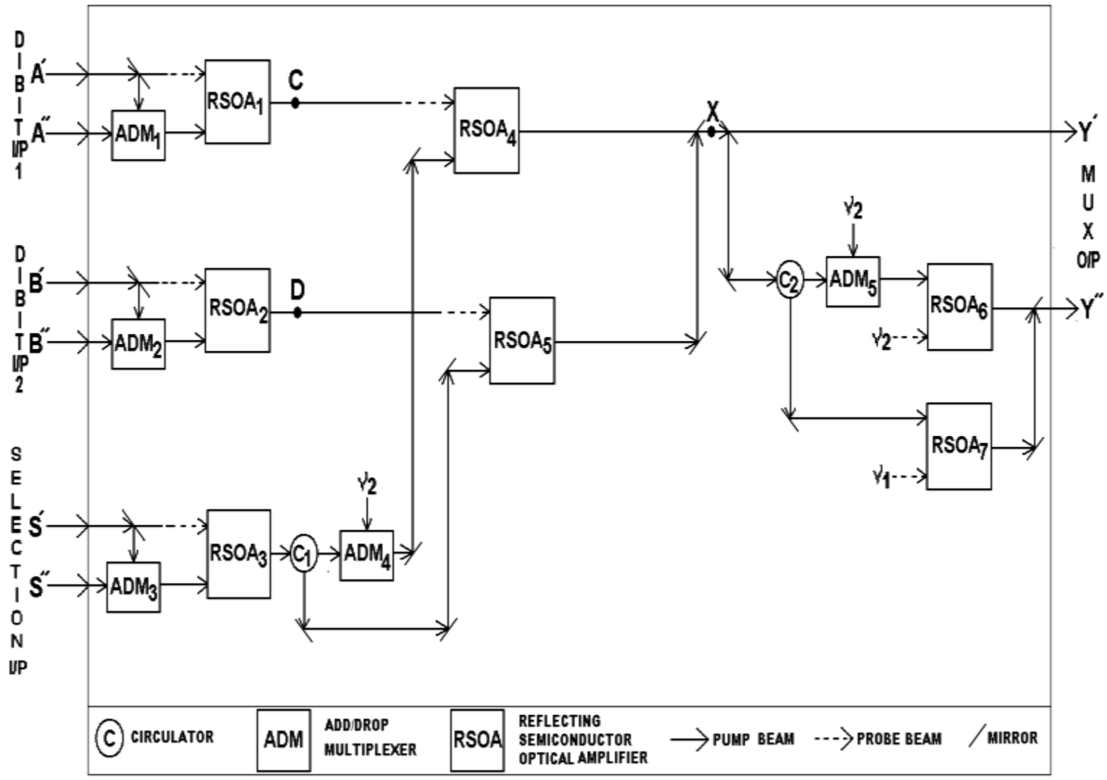


Figure 3.1: Block diagram of Frequency encoded dibit based multiplexer.

At first, [υ_1][υ_2] frequencies or dibit input [0][1] are given to the input channels of ‘A′’, ‘A′′’, ‘B′’, ‘B′′’ and ‘S′’, ‘S′′’ simultaneously. Since, there is a real dibit checking provision by ADM_1 with $RSOA_1$, ADM_2 with $RSOA_2$ and ADM_3 with $RSOA_3$ blocks, it checks the real dibit input combinations respectively. For channel ‘A’, the light beam of υ_1 frequency coming from ‘A′’ acts as biasing terminal of ADM_1. So, the light beam of υ_2 frequency coming from ‘A′′’ passes through the

ADM1. So, υ_1 and υ_2 frequencies of light beam come to the probe beam and pump beam of RSOA$_1$. So, light beam of υ_1 frequency comes out from RSOA$_1$ as output (at point ‘C’). By the same way, light beam of υ_1 frequency also comes out from RSOA$_2$ as output (at point ‘D’) for the given dibit input [υ_1][υ_2] or [0][1] to channel ‘B’ section. At the selection channel ‘S’, υ_1 frequency of light beam also comes out from RSOA$_3$ and this light goes to the input of ADM$_4$, biased by υ_2 frequency. So light beam of υ_1 frequency passes through it and comes out as pump beam to RSOA$_4$.

Due to the absence of pump beam to RSOA$_5$, this block does not work. Now, from point C, υ_1 frequency of light goes in form of probe beam to RSOA$_4$. With the presence of both beams, RSOA$_4$ provides υ_1 frequency of light beam as output and goes directly to ‘Y′’ of output terminal. Now from point ‘X’, one part of this light beam goes to ADM$_5$, biased by beam of light of υ_2 frequency. So, the beam of light of υ_1 frequency is passed through ADM$_5$ and goes to pump beam port of RSOA$_6$. But a constant beam of light of υ_2 frequency is present at the probe beam port of RSOA$_6$. So, the beam of light of υ_2 frequency comes out from RSOA$_6$ (RSOA$_7$ does not work as there is no pump beam) and goes to ‘Y′′’ of output terminal. So, we may get dibit MUX output [υ_1][υ_2] or [0][1] or digital logic state ‘0’ at the output terminal ‘Y′’ and ‘Y′′’ respectively for given dibit inputs of [υ_1][υ_2] or [0][1] and [υ_1][υ_2] or [0][1] or, digital logic state combination ‘0’ and ‘0’ at input terminals both ‘A’ and ‘B’ respectively using dibit selection input [υ_1][υ_2] or [0][1] or, digital logic state ‘0’ at channel ‘S’. Similarly if we consider the inputs as [υ_1][υ_2] or digital logic ‘0’ at channel ‘A’ and [υ_2][υ_1] or digital logic ‘1’ at channel ‘B’, keeping same dibit selection input, we get the output in form of [υ_1][υ_2] or [0][1] at the output terminal ‘Y′’ and ‘Y′′’ respectively. Now if we change the dibit inputs as [υ_2][υ_1] or digital logic ‘1’ at channel ‘A’ and [υ_1][υ_2] or digital logic ‘0’ at channel ‘B’, keeping same dibit selection input as [υ_1][υ_2] or [0][1] or, digital logic state ‘0’, then we get υ_2 frequency as probe beam to RSOA$_4$. Due to the presence of pump beam, RSOA$_4$ provides υ_2 frequency to the output channel ‘Y′’. Now, from point ‘X’ a part of the beam of light of υ_2 frequency comes to ADM$_5$, which is also biased by the beam of light of υ_2 frequency. Therefore, it reflects the beam of light of υ_2 frequency in the form of pump beam of RSOA$_7$. Then, we get υ_1 frequency to output channel ‘Y′′’ from RSOA$_7$. Similarly if we consider the inputs as [υ_2][υ_1] or digital logic ‘1’ at channel ‘A’ and [υ_2][υ_1] or digital logic ‘1’ at channel ‘B’, keeping same dibit selection input, we get the output in form of [υ_2][υ_1] or [1][0] at the output terminal ‘Y′’ and ‘Y′′’ respectively. So we can say the dibit MUX output changes depending to the value of first dibit input of channel ‘A’ i.e. this circuit selects the channel ‘A’ as dibit input. This operation is satisfied by MUX logic for the dibit selection input as [υ_1][υ_2] or [0][1] or, digital logic state ‘0’ (shown in table 3.1).

Now, if we change the dibit selection input to [υ_2][υ_1] or [1][0] or, digital logic state ‘1’ at the selection channel ‘S’, then υ_2 frequency of light beam comes out from RSOA$_3$ and this light goes to the input of ADM$_4$, biased by υ_2 frequency. So light beam of υ_2 frequency is reflected by ADM$_4$ and comes as pump beam to RSOA$_5$. As there is no light beam in the path of pump beam of RSOA$_4$, this block does not work. If [υ_1][υ_2] frequencies or dibit input [0][1] or digital low logic state ‘0’ are set to the input terminals of ‘A′’, ‘A′′’ and ‘B′’, ‘B′′ concurrently. Therefore, light beam of υ_1 frequency comes out from RSOA$_1$ as output (at point ‘C’). By the same way, light beam of υ_1 frequency also comes out from RSOA$_2$ as output (at point ‘D’). Here, with the presence of pump beam, RSOA$_5$ provides υ_1 frequency of light beam coming from RSOA$_2$ as output and goes directly to ‘Y′’ of output terminal and one part of this light beam from point ‘X’ goes to ADM$_5$, biased by υ_2 frequency. The light beam with a frequency of υ_1 passes through and reaches the RSOA$_6$ as a pump beam, while there is a constant probe beam with a frequency of υ_2 and this υ_2 frequency comes out from RSOA$_6$ and goes to ‘Y′′’ of output channel. Similarly, if we consider the inputs as [υ_2][υ_1] or digital logic ‘1’ at channel ‘A’ and [υ_1][υ_2] or digital logic ‘0’ at channel ‘B’, keeping same dibit selection input, we get the output in form of [υ_1][υ_2] or [0][1] at the output terminal ‘Y′’ and ‘Y′′’ respectively. Now if we change the dibit inputs as [υ_1][υ_2] or digital logic ‘0’ at channel ‘A’ and [υ_2][υ_1] or digital logic ‘1’ at channel ‘B’, keeping same dibit selection input as [υ_2][υ_1] or [1][0] or, digital logic state ‘1’, then we get υ_2 frequency as probe beam to RSOA$_5$. Due to the presence of pump beam RSOA$_5$ provides υ_2 frequency to the output channel ‘Y′’. Now, from point ‘X’ a part of beam of light of υ_2 frequency comes to ADM$_5$, which is also biased by beam of light of υ_2 frequency. Thus, the optical switch reflects the beam of light of υ_2 frequency in form of pump beam of RSOA$_7$. Then, we get υ_1 frequency to output channel ‘Y′′’ from RSOA$_7$. Similarly, if we consider the inputs as [υ_2][υ_1] or [1][0] at channel ‘A’ and [υ_2][υ_1] or [1][0] at channel ‘B’, keeping same dibit selection input, we get the output in form of [υ_2][υ_1] or [1][0] at the output terminal ‘Y′’ and ‘Y′′’ respectively. So we can say the dibit MUX output changes depending to the value of second dibit input of channel ‘B’ i.e. this circuit selects the channel ‘B’ as dibit input. This operation is satisfied by MUX logic for the dibit selection input as [υ_2][υ_1] or [1][0] or, digital logic state ‘1’ (shown in table 3.1).

3.3 Simulation process of frequency encoded dibit based multiplexer

Simulink tools of MATLAB (R2008a) software have been used for simulation of frequency encoded all optical dibit multiplexer using RSOA and ADM (shown in figure 3.1). Here, “DIBIT_DATA_INPUT 1”, “DIBIT_ DATA_INPUT 2” and “SELECTION_DIBIT_INPUT” units are used for applying dibit inputs and selection line and we get output from “Dibit MUX Output” unit, which is consisted of two consecutive bit positions “1st Bit” and “2nd Bit” respectively. Now, each of the RSOA blocks is properly programmed with ‘C’ language according to the RSOA mechanism. There are two inputs namely, “pr” (probe beam) and “pm” (pump beam) and the output named by “y” in RSOA blocks. If, for say “3 peta Hz” or, light beam of υ_1 frequency or, digital low logic state “0” and “8 peta Hz” or, light beam of υ_2 frequency or, digital high logic state “1” represent the inputs of pump and probe beam ports, as a result, we get “8 peta Hz” or, light beam of υ_2 frequency or, digital high logic state “1” at the output terminal of these blocks. The value of the output changes if the values of the pump beam and probe beam are altered accordingly. Also ADM has been simulated such a way that, it obeys the proper mechanism of ADM. Now if ADM is biased by a particular light beam frequency, say “3 peta Hz” = υ_1 = digital logic state “0” at “bias” terminal, then this block drops the frequency coming from “input” terminal to “drop” terminal and passes other frequency, say “8 peta Hz” = υ_2 = digital logic state “1” to “out” terminal. If the value of biasing is changed, opposite incident happens. Now the two types of block of units have been coupled together and complete the design of the circuit as per the block diagram of all optical dibit based digital MUX circuit (shown in figure 3.1). Now, consider the dibit form [3][8] as digital logic states ‘0’ and dibit form [8][3] as digital logic states ‘1’.

For example, if [8][3] and [3][8] are applied at the two dibit input units and [8][3] is inserted as selection unit of the simulated model, we get [3][8] at the “Dibit MUX Output” unit of this simulated block according to the value at “DIBIT_ DATA_INPUT 2” , which is shown in figure 3.2. But if [3][8] is applied as selection unit, we may get [8][3] at the “Dibit MUX Output” unit according to the value of

"DIBIT_ DATA_INPUT 1". Therefore, this simulative functional model fully satisfies the truth table of all optical dibit based MUX, which is shown in table 3.1.

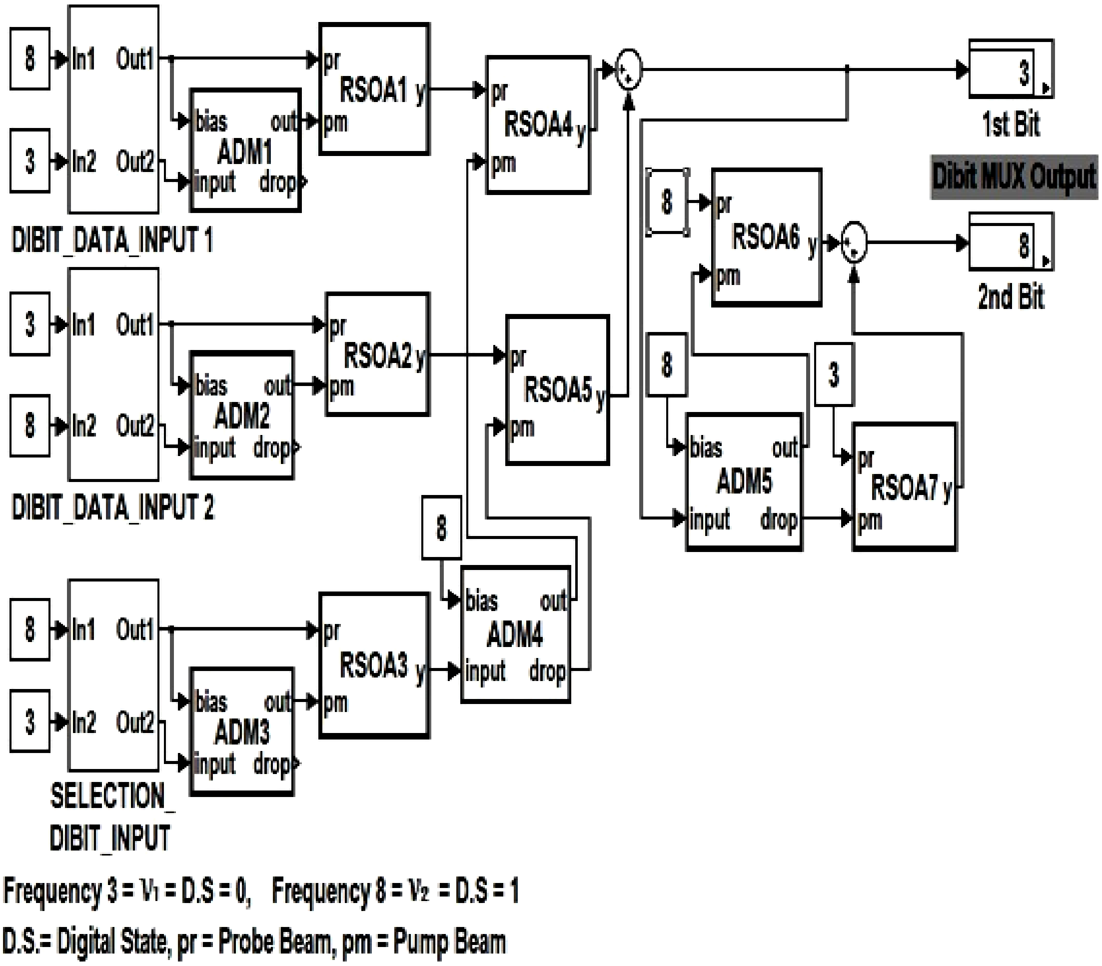


Figure 3.2: Simulation model of the dibit based multiplexer.

3.4 Results and discussion

All outcomes derived from the simulation processes concerning the multiplexer logic align with the truth table for the specific combinational logic circuit. This validation process reinforces our confidence in the accuracy of the simulation results. Consequently, to effectively present these findings, we have included a comprehensive combined table (table 3.1) and a graphical representation (depicted in figure 3.3). These tools illustrate the operation of an all-optical frequency-encoded dibit-based multiplexer, demonstrating how it processes inputs in both dibit and digital formats to generate corresponding outputs. By utilizing both a tabular and visual approach, we not only validate the functionality of the multiplexer but also provide a clear representation of its performance characteristics. This ensures clarity and completeness in demonstrating how the multiplexer handles inputs and produces outputs in various operational scenarios.

First Dibit MUX Input (Channel A)		In digital form	Second Dibit MUX Input (Channel B)		In digital form	Dibit Selection input (Channel S)		In digital form	Dibit MUX Output (Channel Y)		In digital form
A′	A′′	A	B′	B′′	B	S′	S′′	S	Y′	Y′′	Y
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1

Table 3.1: Truth table of dibit based all optical multiplexer.

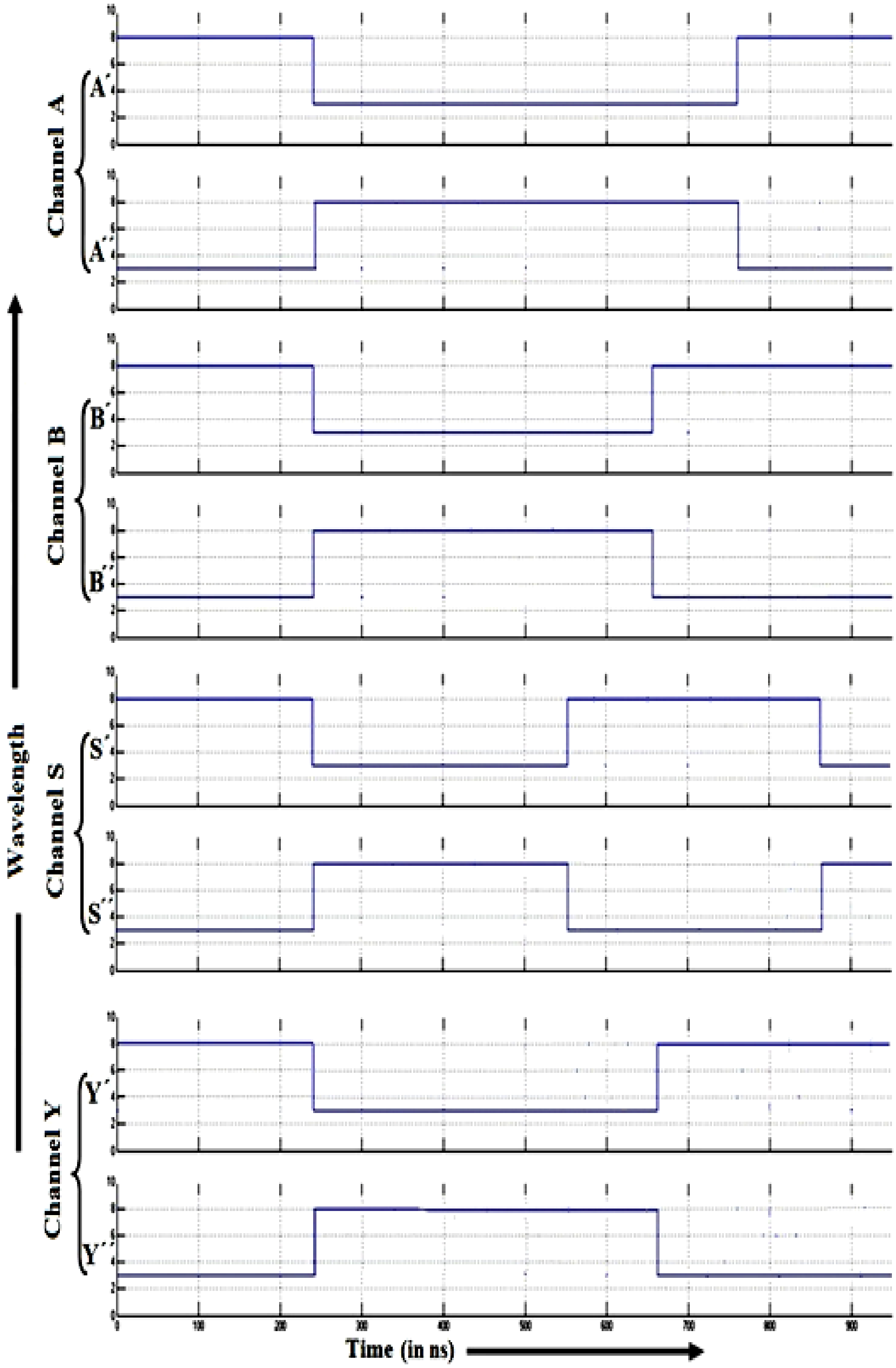


Figure 3.3: Graphical representation of all optical dibit based multiplexer.

3.5 Conclusions

In this context, the benefits of frequency encoding process and also the dibit representation process are utilized to implement the all optical digital circuit operations. These techniques give us not only a trustworthy and practical operation but also it cancel out the bit error problem with better high signal to noise ratio. Besides, the dibit checking block reduces errors on incorrect dibit input states. Using this technique, one also can expect a high degree of parallelism with very fast operational speed. This encoding technique helps for implementation of the all-optical logical operations with faithful and reliable results. With the realization of all optical frequency encoded dibit based combinational type digital multiplexer circuit using ADM and RSOA types optical switches with the simulated results, could be utilized to prepare other types of all optical computational circuits and devices.

References

[3.1]. A. K. Das and S. Mukhopadhyay, “General approach of spatial input encoding for multiplexing and Demultiplexing”, Opt Engineering (USA), 43(1), 126–131 (2004).

[3.2]. S. Sen, S. K. Pal, and S. Mukhopadhyay. “A new scheme of using electro-optic crystal cut obliquely in both sides for reducing its half wave voltage.” Journal of Optics, 2(43), 154-158 (2014).

[3.3]. Connelly, Michael J. "Dynamic model of slow light in a tensile-strained semiconductor optical amplifier." Optical and Quantum Electronics, 46(10), 1247-1252 (2014).

[3.4]. S. K. Garai and S. Mukhopadhyay, “A method of optical implementation of frequency encoded different logic operations using second harmonic& difference frequency generation techniques in non-linear material.” Optik-International Journal for Light and Electron Optics, 121 (8), 715-721 (2010).

[3.5]. S. K. Chandra, P. P. Sarkar, S. Biswas, and S. Mukhopadhyay, “All-optical phase encoded 4-to-1 phase multiplexer using four wave mixing in semiconductor optical amplifier.” Optik, 125(23), 6953-6957 (2014).

[3.6]. S.H.Sun, H.Q. Ma, J.J.Han, L.M.Liang, C.Z. Li, “Quantum key distribution based on phase encoding in long-distance communication fiber”, Optics Letters, 35(8), 1203-1205 (2010).

[3.7]. H. J. Dorren, Daan Lenstra, Yong Liu, Martin, T. Hill, Giok-Djan Khoe, “Nonlinear polarization rotation in semiconductor optical amplifiers: theory and application to all-optical flip-flop memories.” IEEE Journal of Quantum Electronics, 39(1), 141-148 (2003).

[3.8]. B. Ghosh and S. Mukhopadhyay, “A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124 (21), 4813-4815 (2013).

[3.9]. S. Biswas and S. Mukhopadhyay, “An all optical scheme of secured cryptographic communication encoded with decimal data.” Optik, 124(16), 2376-2378 (2013).

[3.10]. B. Sarkar and S. Mukhopadhyay, “An all-optical feedback loop based frequency encoded data-storing unit by EDFA.” Computational Science and Engineering: Proceedings of the International Conference on Computational Science and Engineering (Beliaghata, Kolkata, India, 4-6 October 2016), CRC Press, 2016.

[3.11]. N. Q. Ngo, “Design of an optical temporal integrator based on a phase-shifted Bragg grating in transmission,” Opt. Lett. 32, 3020–3022 (2007).

[3.12]. Mandal, Dhoumendra, et al. “Design of all-optical binary half and full subtractor with frequency encoded data.” International Conference on Fibre Optics and Photonics. Optical Society of America, 2016.

[3.13]. K. Datta, D. Mukhopadhyay, and P. Dutta, “Design of a Binary to BCD Converter Using 2-Dimensional 2-Dot 1-Electron Quantum Dot Cellular Automata.” Procedia Computer Science, 70, 153-159 (2015).

[3.14]. Y. Miyoshi, K. Ikeda, H. Tobioka, T. Inoue, S. Namiki and K. Kitayama, “Ultrafast all-optical logic gate using a nonlinear optical loop mirror based multi-periodic transfer function”, Optics Express, 16(4), 2570-2577 (2008).

[3.15]. J. N. Roy, A. K. Maiti, D. Samanta and S. Mukhopadhyay, “Tree-net architecture for integrated all-optical arithmetic operations and data comparison scheme with optical nonlinear material”, Optical Switching and Networking, 4 (3-4), 231–237 (2007).

[3.16]. S. K. Chandra, S. Biswas and S. Mukhopadhyay. "Phase-encoded all-optical reconfigurable integrated multilogic unit using phase information processing of four-wave mixing in semiconductor optical amplifier." IET Optoelectronics, 10(1), 1-6 (2016).

[3.17] Zhu, Jiangping, et al. “Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination.” Optics express, 24(25), 28549-28560 (2016).

[3.18]. Y. Gao, Y. Dai, C. Shu, S. He, “Wavelength interchange of phase-shift-keying signal.” IEEE Photon. Technol. Lett. 22(11), (2010).

CHAPTER-4

Simulative experiment of all optical frequency encoded dibit based controlled de-multiplexer using ADM and RSOA.

Abstract

Optics is already recognized as a promising candidate for its ultra fast speed in communication and computation. As a result, numerous authors have proposed various logical, combinational, and sequential circuit operations using all-optical frequency encoding techniques. In this context, the authors have introduced a dibit scheme, which reduces bit error issues and offers the advantage of high speed operation. Building on this, we propose an all optical frequency encoded dibit based multiplexer and de-multiplexer, utilizing optical switches such as add/drop multiplexers and reflected semiconductor optical amplifiers. The functionality has been validated through appropriate simulations using simulink software.

Work reported in this chapter was published in:

i. **Bitan Ghosh** and Partha Pratim Sarkar "Simulative study of all-optical frequency encoded dibit-based controlled multiplexer and de-multiplexer using optical switches." Journal of Optics 48.3 (2019): 365-374.

ii. "New scheme of all optical frequency encoded dibit based de-multiplexer with simulated verification." By **Bitan Ghosh**, Partha Pratim Sarkar, Smita Hazra, Sourangshu Mukhopadhyay and Sankar Narayan Patra, in International

Conference on Modeling, Computing and Technological Innovations (ICMCTI-2017), at UIT, The University of Burdwan, West Bengal – 713104, on 23-25th March, 2017.

4.1 Introduction

Photon can be used for super-fast information processing, due to its very high speed of operation. So, it is more suitable information carrier than electron. Thus, realization of all optical different logical and arithmetical digital devices[4.1-4.2] desire different encoding techniques like, frequency[4.3-4.6], intensity[4.7], phase[4.8], spatial[4.9] and polarization encodings[4.10]. As we know from previous chapters that, the frequency encoding technique is the best technique for encoding purpose the time of frequency encoding. So, the two different frequencies of beam of light represent two different states of information. Here, the presence of a light beam of υ_1 frequency is considered as digital low logic state '0' and another light beam of υ_2 frequency is treated as digital high logic state '1'. Now, the dibit representation technique[4.11-4.13] can now be used to represent a digital logic state through two consecutive bit positions. Therefore, dibit logic state <0><1> represents the digital logic state '0' and dibit logic state <1><0> represents digital logic state '1' respectively. Now, if we apply frequency encoding principle then these two bit positions may be considered as two different frequencies. Therefore, the presence of the two different frequencies of beam of light together like, $<\upsilon_1><\upsilon_2>$ represents the digital low logic state '0' and $<\upsilon_2><\upsilon_1>$ is considered as the digital high logic state '1'.

Here, the authors have introduced distinct type of combinational digital circuit, called de-multiplexer (De-MUX). This circuit is designed using an innovative approach that relies entirely on optical dibit based technology. This technique harnesses the inherent properties of light to facilitate both data processing and transmission, presenting potential benefits in terms of speed and efficiency over conventional electronic approaches. Light, as a medium, allows for rapid transmission of information due to its high speed and ability to carry large amounts of data over long distances with minimal attenuation or loss. By utilizing light, this method holds promise for enhancing the speed of data transfer and reducing energy consumption, thereby improving overall efficiency in communication networks. Compared to traditional electronic methods which rely on electrons moving through conductors, optical techniques can operate at higher frequencies and with lower signal degradation, making them suitable for high-bandwidth applications such as telecommunications and data centers. Thus, leveraging light for data processing and transmission represents a significant advancement in technology with the potential to revolutionize how information is handled and transmitted in various sectors. System gets input form a dibit input port and sends the data to one of many dibit output ports.

Again, we proposed appropriate dibit checking unit, which prevents the inappropriate inputs (like <0><0> or <1><1>) to enter into the dibit based circuit to increase the reliability of the digital circuit. This scheme is designed by all optical switches like add/drop multiplexer (ADM)[4.14-4.17] and reflected semiconductor optical amplifier (RSOA)[4.18-4.22]. The ADM is a sophisticated optical switching device that selectively handles different frequencies of light. When a light beam of a specific frequency is used to bias the ADM, the device becomes capable of isolating and reflecting this particular frequency from the input signal. Consequently, the ADM captures the targeted frequency and prevents it from continuing along the transmission path. Meanwhile, all other frequencies of the light beam pass through the ADM without interruption. This selective filtering process allows the ADM to efficiently manage and route optical signals, making it a critical component in optical communication networks where precise control over signal frequencies is required. Opposite incident happens if the biasing input changes.

Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device. If a beam of light with υ_1 frequency as weak probe beam and another beam of light with υ_2 frequency as strong pump beam are applied to the input terminals of the RSOA. Then this switch will give the beam of light of υ_1 frequency with the power of the pump beam. Thus, they could be identified as highly valuable optical switches for executing numerous all-optical logical operations.

The range of saturation power in non-linear material based semiconductor optical amplifier is quite wide and may be utilized in the range of 5 – 20 dBm. So this proposed simulated representation likely to substitute optical fiber based amplifier [4.23-4.24], used as network components. This power handling capacity can be considered as one of the major advantages for our proposed model.

4.2 Scheme of realization of frequency encoded dibit based de-multiplexer

For example, 1×2 De-MUX scheme is considered having one data input line as ‘A’, subdivided into ‘A′’ and ‘A′′’, for providing dibit input for realizing the dibit based De-MUX, in figure 2 with a selection line ‘S’, subdivided further as ‘S′’ and ‘S′′’ to provide dibit selection input using the blocks of all optical switches like add/drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA).

Now, <υ_1><υ_2> or <0><1> or digital logic state ‘0’ are given to the input line <A′><A′′> and selection line <S′><S′′> simultaneously. Since, there is a dibit checking unit by ADM_1 with $RSOA_1$ and ADM_2 with $RSOA_2$ blocks, they check the real dibit input combinations respectively. The light beam of υ_1 frequency coming from ‘A′’ acts as biasing terminal of ADM_1. Now, the light beam of υ_2 frequency coming from ‘A′′’ passes through the ADM_1. Therefore, υ_1 and υ_2 frequencies of light beam come to the probe beam and pump beam of $RSOA_1$ respectively. Then light beam of υ_1 frequency comes out from $RSOA_1$ at point ‘C’ and goes as probe beam to $RSOA_3$. By the same way, due to the presence of dibit checking blocks comprising ADM_2 with $RSOA_2$, the light beam of υ_1 frequency also comes out from $RSOA_2$ at point ‘D’. Afterward, light beam of υ_1 frequency comes out as pump beam to $RSOA_3$ after passing through ADM_3 as it is biased by υ_2 frequency. Though, one part of the light beam coming from point ‘C’, enter as probe beam to $RSOA_4$, but this block does not work due to the absence of pump beam to $RSOA_4$. With the presence of both beams, $RSOA_3$ provides light beam of υ_1 frequency as output at point ‘E’ and goes directly to ‘X′’ of output terminal. Now from point ‘E’, another part of the light beam goes to ADM_4, which is biased by beam of light of υ_2 frequency. So, it allows the beam of light of υ_1 frequency and goes to the pump beam terminal of $RSOA_5$ with a fixed beam of light of υ_2 frequency to the probe beam of $RSOA_5$. Threfore, light beam of υ_2 frequency comes out from $RSOA_5$ ($RSOA_6$ does not work as there is no pump beam) and goes to ‘X′′’ of output terminal. So, we may get dibit De-MUX output <υ_1><υ_2> or <0><1> or digital logic state ‘0’ at the first dibit De-MUX output terminal ‘X’ for given dibit selection input <υ_1><υ_2> or <0><1> or, digital logic state ‘0’ at selection line ‘S’. Similarly if we consider the input as <υ_2><υ_1> or <1><0> or digital logic ‘1’ at input line ‘A’ and keeping same dibit selection input, we get the output in form of <υ_2><υ_1> or <1><0> at the first dibit De-MUX output terminal ‘X′’ and ‘X′′’ respectively. So we can say, this De-MUX scheme choose the dibit output path as terminal ‘X’ (DE MUX O/P 1) as per the selection input as <υ_1><υ_2> or <0><1> actually, digital logic state ‘0’, shown in figure 4.1. These operations are satisfied by De-MUX logic for this particular dibit selection input which is shown in table 4.1.

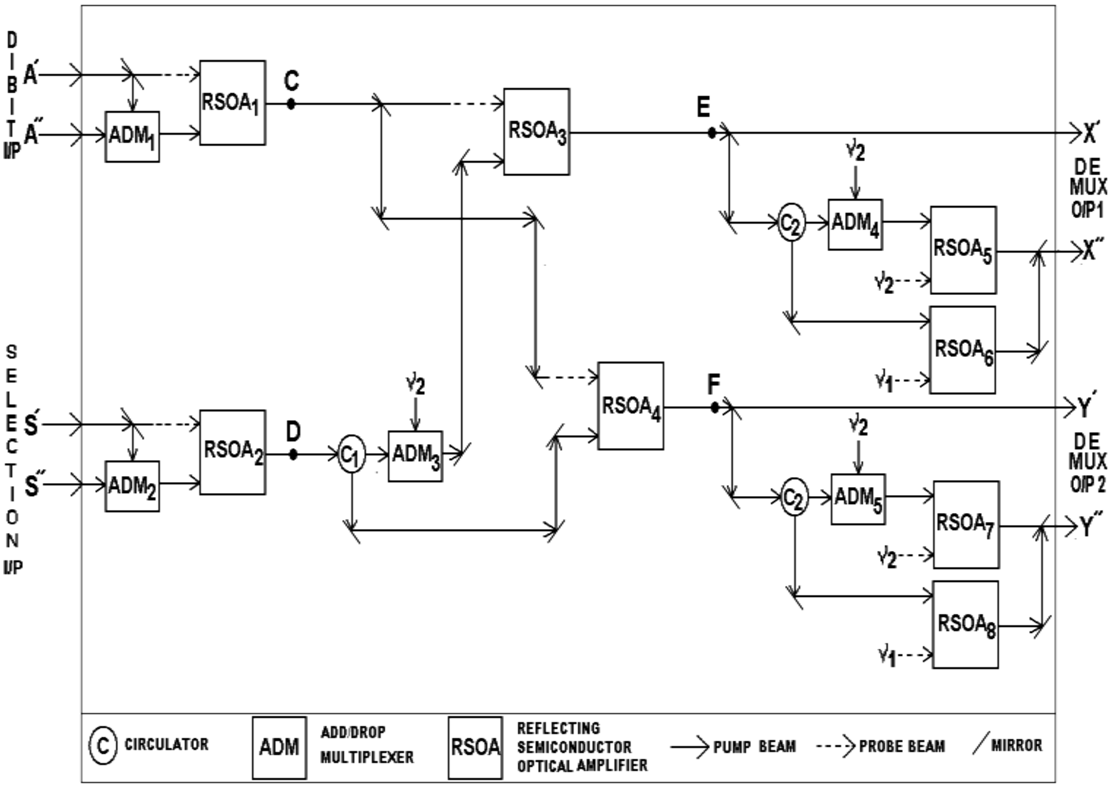


Figure 4.1: Block diagram of Frequency encoded dibit based de-multiplexer.

Next, we change the selection input as <υ_2><υ_1> or <1><0> or digital logic ‘1’ at selection line ‘S’ and apply the dibit De-MUX input as <υ_1><υ_2> or <0><1> or digital logic ‘0’ at input line ‘A’. After passing dibit checking blocks, we get light beam of υ_1 frequency at point ‘C’ coming from RSOA$_1$ and light beam of υ_2 frequency at point ‘D’ coming from RSOA$_2$. Subsequently, light beam of υ_2 frequency comes out as pump beam to RSOA$_4$ after reflected by ADM$_3$ as it is biased by υ_2 frequency. Besides this, the light beam coming from point ‘C’, enter as probe beam to RSOA$_3$, but this block does not work due to the absence of pump beam to RSOA$_3$. Now one part of the light beam coming from RSOA$_1$ enters as probe beam to RSOA$_4$. By means of the presence of both beams, RSOA$_4$ provides light beam of υ_1 frequency as output at point ‘F’ and goes directly to ‘Y′’ of output terminal. Now from point ‘F’, another part of the light beam goes to ADM$_5$, biased by υ_2 frequency. Therefore, it transmits a light beam at frequency υ_1, serving as the pump beam for RSOA$_7$, while maintaining a constant probe beam at frequency υ_2. For that reason, light beam of υ_2 frequency comes out from $RSOA_7$ ($RSOA_8$ does not work as there is no pump beam) and goes to 'Y′′' of output terminal. So, we may get dibit De-MUX output <υ_1><υ_2> or <0><1> actually, digital logic state '0' at the second dibit De-MUX output terminal 'Y' for given dibit selection input <υ_2><υ_1> or <1><0> actually, digital logic state '1' at selection line 'S'. Similarly if we consider the input as <υ_2><υ_1> or <1><0> or digital logic '1' at input line 'A' and keeping same dibit selection input, we get the output in form of <υ_2><υ_1> or <1><0> at the second dibit De-MUX output terminal 'Y′' and 'Y′′' respectively. Finally, this De-MUX scheme choose the dibit output path as terminal 'Y' (DE MUX O/P 2) using the selection input as <υ_2><υ_1> or <1><0> actually, digital logic state '1', which is shown in figure 4.1. These operations are fully satisfied also by De-MUX logic for the specific dibit selection line, which is shown in table 4.1.

4.3 Simulation process of frequency encoded dibit based de-multiplexer

To simulate the frequency-encoded all-optical dibit de-multiplexer, depicted in figure 4.1, MATLAB's simulink tools from the R2008a software version were utilized. In figure 4.2, the components labeled as "DIBIT_DATA_INPUT" and "SELECTION_DIBIT_INPUT" are employed to input dibit data and selection line information, respectively. Outputs are obtained from units labeled "Dibit De-MUX Output 1" or "Dibit De-MUX Output 2," depending on the specific operations of the de-multiplexer. Each output unit comprises two consecutive bit positions identified as "1st Bit" and "2nd Bit." These positions correspond to the respective output states generated by the de-multiplexer's operations. This simulation setup allows for detailed analysis and verification of how the de-multiplexer processes input dibit signals and selection lines, providing clear output results for each bit position as specified.

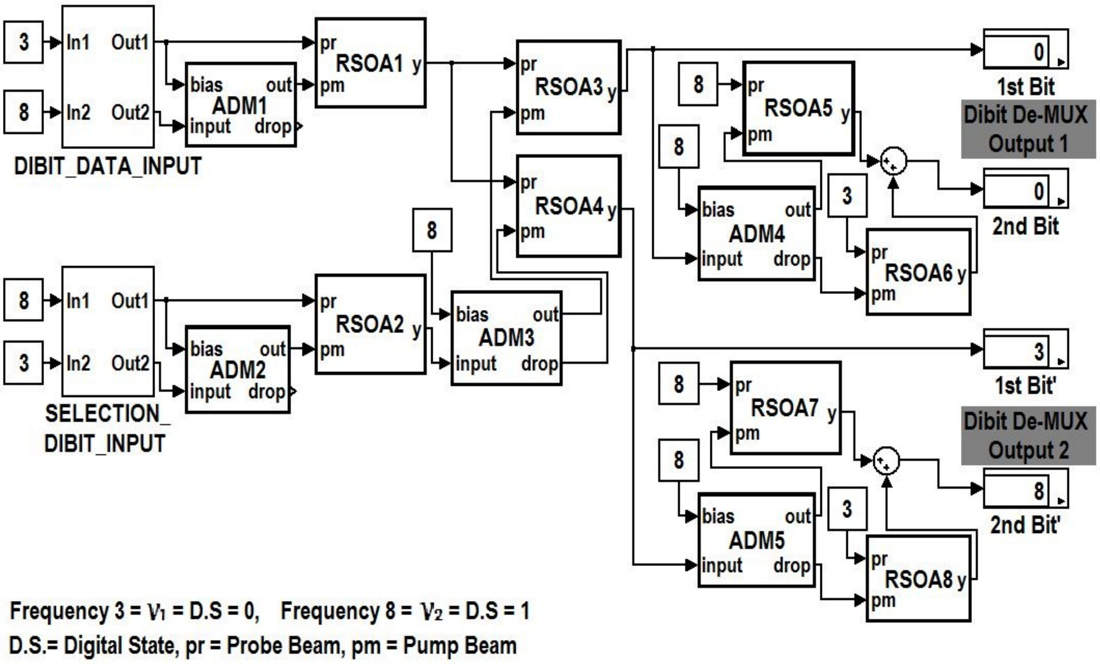


Figure 4.2: Simulation model of the dibit based de-multiplexer.

The RSOA blocks are properly programmed with MATLAB code according to the RSOA mechanism. There are namely, “pr” (probe beam), “pm” (pump beam) and “y” for providing two inputs and output in RSOA blocks. For example, if say “3 peta Hz” or, beam of light of υ_1 frequency or, digital low logic state “0” and “8 peta Hz” or, beam of light of υ_2 frequency or, digital high logic state “1” correspondingly are applied to the pump beam and probe beam terminals, then we get “8 peta Hz” or, beam of light of υ_2 frequency or, digital high logic state “1” at the output terminal of these blocks. Again, the ADM blocks have been simulated with MATLAB code as per the proper mechanism of ADM. For example, if ADM block is biased using “bias” terminal by a particular light beam frequency, say “3 peta Hz” = υ_1 = digital logic state “0”, then this block drops the frequency coming from “input” terminal to “drop” terminal and passes other frequency, like “8 peta Hz” = υ_2 = digital logic state “1” to “out” terminal.

Maintaining the similarity of the block diagram of all optical dibit based De-MUX (shown in figure 4.1), these RSOA and ADM blocks have been connected in proper way, considering the dibit form [3][8] as digital logic states ‘0’ and dibit form [8][3] as digital logic states ‘1’. If [3][8] and [8][3] are applied at the dibit input unit and selection unit respectively then we get [3][8] at the “Dibit De-MUX Output 2” unit of this simulated block according to the value at “DIBIT_ DATA_INPUT”. In the simulated model, according to the encoding technique, "Dibit De-MUX Output 1" indicates that [0][0] is interpreted as NULL. But if [3][8] is applied as selection unit, we may get [3][8] at the “Dibit De-MUX Output 1” unit according to the value of “DIBIT_ DATA_INPUT” whereas “Dibit De-MUX Output 2” shows [0][0] assumes to be NULL value. So, this simulative verification fully satisfies the truth table of all optical dibit based De-MUX, which is shown in table 4.1.

4.4 Results and discussion

Dibit De-MUX Input (Channel A)		In digital form	Dibit Selection input (Channel S)		In digital form	First Dibit De-MUX Output (Channel X)		In digital form	Second Dibit De-MUX Output (Channel Y)		In digital form
A'	A''	A	S'	S''	S	X'	X''	X	Y'	Y''	Y
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	×	×	×
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	×	×	×	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	×	×	×
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	×	×	×	$\upsilon_2[1]$	$\upsilon_1[0]$	1

Table 4.1: Truth table of dibit based all optical de-multiplexer.

The de-multiplexer logic is validated through a truth table derived from comprehensive simulation processes of the combinational logic circuit. This process ensures that all possible scenarios and outcomes are accounted for and verified. To present these findings effectively, a consolidated table (referred to as table 4.1) and a graphical representation (depicted in figure 4.3) are employed.

These tools serve to illustrate the functionality of an all optical frequency encoded dibit based de-multiplexer, showcasing how it processes inputs in both dibit and digital formats, along with selection lines, to produce corresponding outputs. This integrated approach not only validates the logic circuit's operation but also provides a clear visual and tabular representation of its performance characteristics and capabilities.

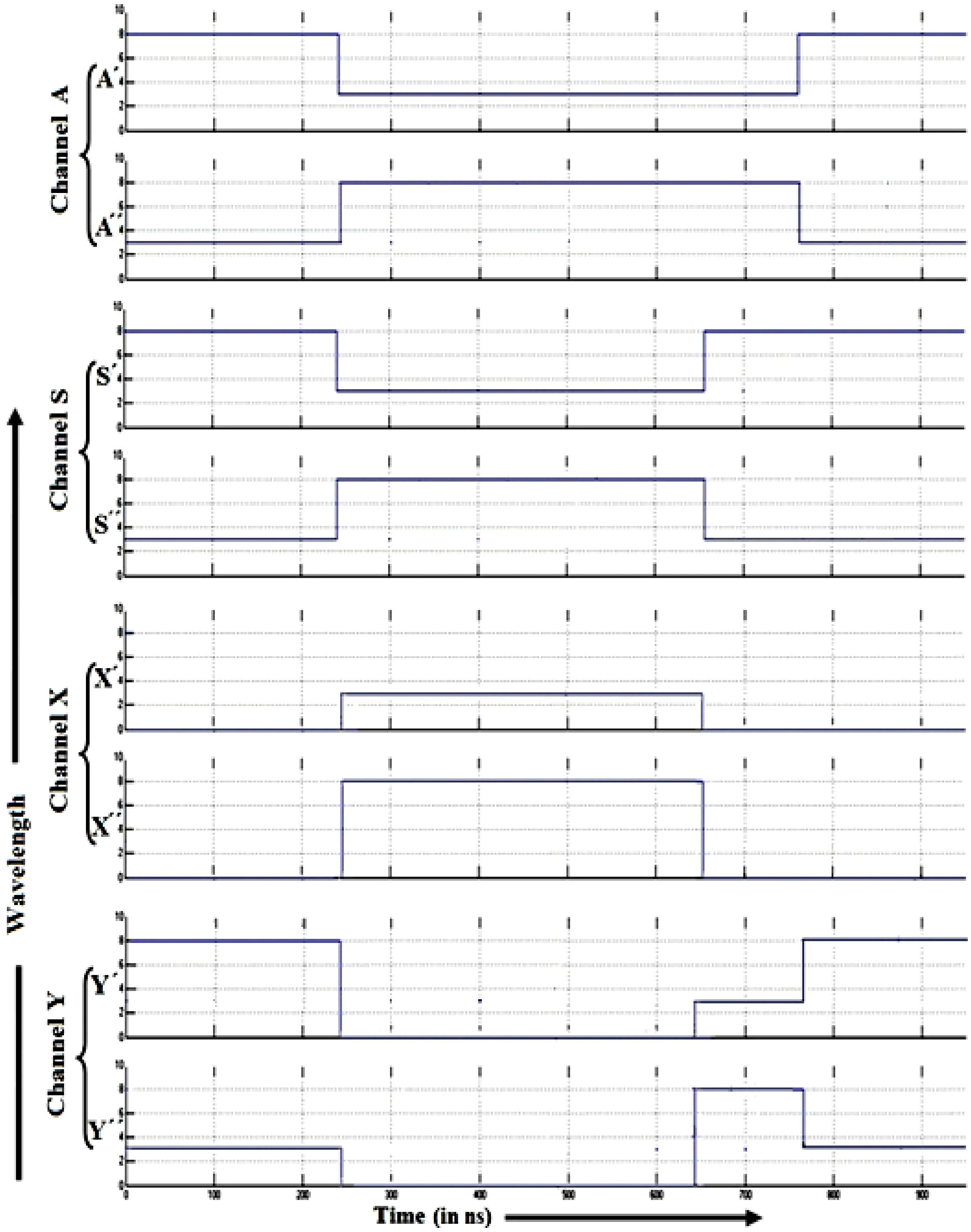


Figure 4.3: Graphical representation of all optical dibit based de-multiplexer.

4.5 Conclusions

Here, the advantages of dibit representation as well as frequency encoding technique are subjugated to realize the all optical operation. In this technique the dibit control input reduces errors on incorrect dibit input states. Using this system, one can expect a high degree of parallelism also due to dibit based system with very fast operational speed. This dibit based frequency encoding technique helps for realization of the all optical logical and combinational operation with realistic and reliable outcomes.

This implementation of the de-multiplexer scheme through optical switches, validated via simulation, opens pathways for the development of other all optical computational devices. This achievement underscores its capability for achieving high speed and dependable operation. By leveraging optical switches, this scheme enables efficient and rapid data routing and manipulation solely through light signals, bypassing the limitations of traditional electronic methods. This approach not only enhances processing speeds but also ensures reliable performance, crucial for applications demanding swift and accurate data handling, such as optical networks and data centers. Consequently, the demonstrated effectiveness of this de-multiplexer scheme paves the way for advancements in all optical computing technologies, promising to redefine the landscape of information processing and communication systems with its speed and operational robustness.

References

[4.1]. S. Mukhopadhyay, “Role of optics in super-fast information processing.” Indian Journal of Physics, 84(8), 1069–1074 (1010).

[4.2]. A. K. Ghosh, A. Bhattacharya, M. Raul, A. Basuray, “Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic.” Optics & Laser Technology, 44(5), 1583–1592 (2012).

[4.3]. P. P. Sarkar, S. Mukhopadhyay, “All optical frequency encoded NAND logic operation along with the simulated result.” Journal of Optics, 43(3), 177–182 (2014).

[4.4]. B. Ghosh, S. Mukhopadhyay, “A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124(21), 4813–4815 (2013).

[4.5]. P. P. Sarkar, B. Ghosh, S. N. Patra, S. Mukhopadhyay, “A new scheme of an all optical frequency encoded dibit based latch with its simulated result.” Journal of Optical Technology, 84(9), 631–634 (2017).

[4.6]. P. P. Sarkar, B. Satpati, S. Mukhopadhyay, “New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors.” Journal of Optics, 42(4), 360–366 (2013).

[4.7]. V. Çakmak, F. Ufuk, N. Karabulut, “Diffusion‐weighted MRI of pulmonary lesions: Comparison of apparent diffusion coefficient and lesion‐to‐spinal cord signal intensity ratio in lesion characterization.” Journal of Magnetic Resonance Imaging, 45(3), 845-854 (2017).

[4.8]. G. Hu, et al. “Securing image information using double random phase encoding and parallel compressive sensing with updated sampling processes.” Optics and Lasers in Engineering, 98, 123-133 (2017).

[4.9]. J. Zhu, et al. “Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination.” Optics express, 24(25), 28549-28560 (2016).

[4.10]. C. Taraphdar, T. Chattopadhyay, J. N. Roy, “Polarization encoded all-optical ternary Max gate.” 4th International Conference on Computers and Devices for Communication, Kolkata, India, December 2009, 1–4 (2009).

[4.11]. S. Mukhopadhyay, “Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems.” Applied optics, 31(23), 4622-4623 (1992).

[4.12]. P. P. Sarkar, et al. “Realization of all-optical frequency-encoded dibit-based OR and NOR logic gates with simulated verification.” in Guha, D. (Ed.), Chakraborty, B. (Ed.), Dutta, H. (Ed.): Computer, Communication and Electrical Technology, CRC Press, 2017, 1st edn., 153-158 (2017).

[4.13]. B. Ghosh, S. Biswas, S. Mukhopadhyay, “A novel method of all-optical wavelength encoded logic and inhibitor operations with dibit representation technique.” Optik-International Journal for Light and Electron Optics, 126(4), 483-489 (2015).

[4.14]. I. S. Amiri, et al. “Nanometer bandwidth soliton generation and experimental transmission within nonlinear fiber optics using an add-drop filter system.” Journal of Computational and Theoretical Nanoscience, 12(2), 221-225 (2015).

[4.15]. S. Chen, et al. “Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon.” IEEE Photonics Technology Letters, 28(17), 1874-1877 (2016).

[4.16]. J. Wang, L. R. Chen, “Low crosstalk Bragg grating/Mach-Zehnder interferometer optical add-drop multiplexer in silicon photonics.” Optics express, 23(20), 26450-26459 (2015).

[4.17]. Mansoor, R., Koziel, S., Sasse, H., Duffy, A.: ‘Crosstalk suppression bandwidth optimisation of a vertically coupled ring resonator add/drop filter’, IET Optoelectronics, 2015, 9, (2), pp. 30-36, doi: 10.1049/iet-opt.2014.0059.

[4.18]. P. P. Sarkar, B. Ghosh, S. N. Patra, “Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer.” Journal of Optical Technology, 83(4), 257–262 (2016).

[4.19]. B. Ghosh, et al. “A Novel Approach to Realize of All Optical Frequency Encoded Dibit Based XOR and XNOR Logic Gates Using Optical Switches with Simulated Verification.” Optics and Spectroscopy, 124(3), 337-342 (2018).

[4.20]. S. Saha, S. Biswas, S. Mukhopadhyay, “Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach–Zehnder interferometer-based semiconductor optical amplifier.” IET Optoelectronics, 11(5), 201-207 (2017).

[4.21]. S. Singh, S., et al. “Photonic processing of all-optical Johnson counter using semiconductor optical amplifiers.” IET Optoelectronics, 11(1), 8-14 (2016).

[4.22]. J. Tanida and Y. Ichioka, “Optical logic array processor using shadowgrams.” Journal of the Optical Society of America, 73(6), 800-809 (1983). M. Connelly, “Semiconductor optical amplifiers and their applications.” University of Limerick (2003).

[4.23]. M. Connelly, “Semiconductor optical amplifiers and their applications.” University of Limerick (2003).

[4.24]. D. K. Gayen, et al. “All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach–Zehnder interferometer.” Journal of Computational Electronics, 14(1), 129-138 (2015).

CHAPTER-5

Designing of all optical frequency encoded dibit based integrated type AND-OR/NAND-NOR logic gate using optical switches with simulated result.

Abstract

Optics is increasingly recognized as a promising information carrier for the understanding of digital logic circuits and optical systems. It is used for optical computations and processors for super fast speeds. This is implemented by the semiconductor optical amplifier based optical switches. Some optical logic gates work based on frequency conversion process of certain non-linear devices. The non-linear type device such as semiconductor optical amplifier is seen like a very hopeful and dependable optical device to realize different optical digital logic systems. With advancements in technology, there is a growing need for compact and integrated device designs. In this context, the authors propose the designing of optical frequency encoded integrated type AND-OR/NAND-NOR logic gate, which is controlled by an input. This approach enables a single circuit to execute multiple logic operations by utilizing two type of optical switches specifically, the reflected semiconductor optical amplifier in combination with add/drop multiplexer. The proposed scheme or, design for all-optical frequency encoded integrated type logic gates with control inputs has been successfully validated through appropriate simulation techniques.

Work reported in this chapter was published in:

i. **Bitan Ghosh**, Niladri Halder, Dibyendu Roy and Partha Pratim Sarkar "An alternative approach to realize all optical frequency encoded integrated AND-OR logic gate with control input using optical switches and its simulative verification." International Journal of Computer Sciences and Engineering 07.spcl01 (2019): 88-93.

5.1 Introduction

For tremendous swift information processing[5.1], photon can be considered a more effective information carrier than an electron. Numerous all optical logic gates[5.2], flip-flops[5.3], bi-stable multivibrators, latches etc are developed with optics[5.4]. The optical switching device like semiconductor optical amplifier (SOA)[5.5] is recognized as a very much hopeful optical device for performing various all optical[5.6] logic implementations[5.7]. This optoelectronic device can amplify an input beam of light signal the active region of the material when operated under appropriate conditions[5.8]. In the semiconductor, three radiative mechanisms can occur. When incident light with sufficient photon energy strikes the semiconductor, then it can excite a carrier from the valence band to the conduction band via stimulated absorption. This process is lossy because the incident photon is absorbed. When a photon with the appropriate energy interacts with the semiconductor, it induces stimulated recombination between a carrier in conduction band and a hole in valence band. Thus, the carrier releases its energy in the form of a photon. This newly emitted photon will be identical to the previous inducing photon in terms of phase[5.9], frequency and direction, indicating a coherent interaction. Both the incident and stimulated photon can trigger further stimulate. A population inversion process occurs when incident ray is adequately high. As a result, the carrier concentration in the conduction band is greater than the concentration in the valence band. At this stage, the probability of stimulated emission exceeds that of stimulated absorption, leading to optical gain for the semiconductor. A carrier of conduction band has a non-zero probability per unit time to spontaneously recombine with a hole of valence band, emitting a photon with random phase[5.10] and direction during the spontaneous emission process. The photons emitted spontaneously cover a wide range of frequencies and primarily contribute as noise. They also decrease the population of carriers available for optical gain. This spontaneous emission is a direct byproduct of the amplification process.

An SOA can function as an ultra-fast nonlinear medium. As photo-excitation increases, absorption decreases and can turn negative at high excitation levels, leading to changes in the refractive index. One of the major drawbacks of the SOA for ultra-fast signal processing is its slow response due to carrier recombination.[5.11].

For implementing[5.12] the optical logic gates and arithmetic devices, there are spatial encoding[5.13], polarization encoding, frequency encoding[5.14], intensity encoding and phase encoding[5.15] types of encoding principles are needed. As the frequency of beam[5.16] of light remains unaffected and constant after reflection, refraction, absorption etc, the frequency encoding principle[5.17] is the most suitable one among all other encoding principles[5.18].

The reflected semiconductor optical amplifier amplifies and processes optical signals, facilitating rapid switching and signal conversion. Meanwhile, the add/drop multiplexer type optical switches allow for selective routing and combination of optical signals, thereby enabling the circuit to perform different logic functions based on the configuration of the switches. This integration not only enhances the versatility and efficiency of the circuit but also simplifies the overall design by consolidating multiple logic functions into a single, compact unit.

5.2 Background

Two distinct frequencies are used to represent two unlike states of information in the frequency encoding or decoding technique[5.19] during data computation[5.20]. In general, the existence of a specific beam of light of frequency is interpreted as the '1' digital high logic state, while another particular frequency represents the '0' digital low logic state. All optical schemes are designed by all optical switches[5.21] like add/drop multiplexer (ADM)[5.22] and reflected semiconductor optical amplifier (RSOA). Add/drop multiplexer[5.23] (ADM) is a frequency choosy optical switching device. If it is biased by a light beam of particular frequency then the particular frequency of light beam is reflected by ADM[5.24] from input and passes all other frequency of light beam. Opposite incident happens if the biasing input changes. Now, reflected semiconductor optical amplifier (RSOA)[5.25] is another optical switching device[5.26]. It has two inputs. If a weak beam of light as probe beam with particular frequency, say υ_1 and a powerful beam of light as pump beam with another frequency say, υ_2 are inserted[5.27] then, this switch[6.28] will give output as the beam of light of υ_1 frequency (that is frequency of the light of probe beam) with the power of the light of pump beam. So this principle is very useful to implement various all optical logic devices and arithmetical data operations[5.29].

The dibit representation[5.30] has the advantage of the possibility of implementing ternary, quaternary, octal and decimal operations with the help of optics. This technique can be done to represent a digit by two consecutive bits. These two bits may be considered like υ_1 = 195 THz and υ_2 = 193 THz frequencies. Now if we denote the optical beam of light of υ_1 frequency = digital low logic state ‘0’ and the optical beam of light of υ_2 frequency = digital high logic state ‘1’ then by the dibit system this digital low logic state ‘0’ is represented as [0][1] and digital high logic state ‘1’ is denoted as [1][0] respectively. Thus, the two frequencies together [υ_1][υ_2] represents the digital low logic state ‘0’ and similarly [υ_2][υ_1] represents the digital high logic state ‘1’. Here, the authors have projected an new technique for understanding the all optical frequency encoded dibit based integrated type AND/NAND and OR/NOR logics with controlled input for selecting particular logic operation using RSOA and ADM. This scheme is successfully implemented on integrated AND and OR logic operations with a single circuit just altering one switch. Additionally, the truth tables have been validated with the simulation results.

5.3 Realization of the integrated AND-OR logic gate

At first, the scheme will be divided into three units for realization of the integrated design of two input AND and OR logic using optical switches. They are controlling dibit input unit, controlling logic unit and controlling dibit output unit.

A. Controlling dibit input unit

Here, the two input terminals are ‘A’ and ‘B’. These two channels are divided further as ‘A′’ and ‘A′′’, ‘B′’ and ‘B′′’ respectively to provide dibit inputs. In this single bit transformation one optical light beam of frequency υ_1 or digital ‘0’ is treated as $<\upsilon_1><\upsilon_2>$ or <0><1> in case of dibit representation technique. Similarly, optical light beam of frequency υ_2 or digital logic state ‘1’ is considered as $<\upsilon_2><\upsilon_1>$ or <1><0> for dibit system. The block diagram of controlling dibit input unit is shown in figure 5.1. Here, the authors have developed the controlling dibit input unit, providing the actual or effective dibit, i. e. this system allows the input in form of dibit $<\upsilon_1><\upsilon_2>$ or <0><1> or digital ‘0’ and dibit $<\upsilon_2><\upsilon_1>$ or <1><0> or digital ‘1’. The system can reject to operate for any other formation.

Now for this reason, if we apply $<\upsilon_1><\upsilon_1>$ (or, <0><0>) to ‘A′’ and ‘A′′’, then, from ‘A′’ terminal, one part of light beam of υ_1 frequency acts as a biasing of ADM_1 and other part acts as probe beam of $RSOA_1$. Now, from ‘A′′’ terminal, light beam of υ_1 frequency goes to the input of ADM_1, so ADM_1 restricts to penetrate the light beam of υ_1 frequency, since υ_1 frequency acts as a biasing of ADM_1. Therefore, $RSOA_1$ has no pump beam, as output of ADM_1 connected to pump beam terminal of $RSOA_1$. So, there is no light beam at the ‘A’ terminal. This is shown in the first combination for the channel ‘A’ in table 5.1. Again, if we apply <υ_2><υ_2> (or, <1><1>) to ‘A´’ and ‘A´´’ then, from ‘A´’ terminal, one part of light beam of υ_2 frequency acts as a biasing of ADM$_1$ and other part acts as probe beam of RSOA$_1$. Now, from ‘A´´’ terminal, light beam of υ_2 frequency goes to the input of ADM$_1$, so ADM$_1$ restricts to penetrate the light beam of υ_2 frequency as υ_2 frequency acts as a biasing of ADM$_1$. Therefore, RSOA$_1$ has no pump beam. So, there is no light beam at the ‘A’ terminal. Also this is shown in the fourth combination for the channel ‘A’ in table 5.1.This principle of operation will be applicable for ‘B’ terminal also. When we apply <υ_1><υ_1> (or, <0><0>) to ‘B´’ and ‘B´´’, then, one part of light beam of υ_1 frequency from ‘B´’ terminal, acts as a biasing of ADM$_2$ and other part acts as probe beam of RSOA$_2$. Now, the light beam of υ_1 frequency from ‘B´´’ terminal goes to the input of ADM$_2$, so ADM$_2$ blocks to penetrate the light beam of υ_1 frequency, since υ_1 frequency acts as a biasing of ADM$_2$. Therefore, RSOA$_2$ has no pump beam, as output of ADM$_2$ connected to pump beam terminal of RSOA$_2$. So, there is no light beam at the ‘B’ terminal. This is demonstrated in the initial combination for channel 'B' in table 5.1. Again, if we apply <υ_2><υ_2> (or, <1><1>) to ‘B´’ and ‘B´´’ then, from ‘B´’ terminal, one part of light beam of υ_2 frequency acts as a biasing of ADM$_2$ and other part acts as probe beam of RSOA$_2$. Now, from ‘B´´’ terminal, light beam of υ_2 frequency goes to the input of ADM$_2$, so ADM$_2$ restricts to penetrate the light beam of υ_2 frequency as υ_2 frequency acts as a biasing of ADM$_2$. Therefore, RSOA$_2$ has no pump beam. So, there is no light beam at the ‘B’ terminal. Also it is shown in the fourth combination for the channel ‘B’ in table 5.1.

But, if we apply <υ_1><υ_2> (or, <0><1>) to ‘A´’ and ‘A´´’, then, from ‘A´’ terminal, one part of light beam of υ_1 frequency act as a biasing of ADM$_1$ and other part acts as probe beam of $RSOA_1$. Now, from ‘A′′’ terminal, light beam of υ_2 frequency goes to the input of ADM_1, so ADM_1 passes the light beam of υ_2 frequency. So, $RSOA_1$ has the pump beam of υ_2 frequency. As we know that, frequency of the output beam of RSOA is same as the frequency of the probe beam when pump beam is present. So, there is a light beam of υ_1 frequency (or, digital ‘0’) at ‘A’. This is shown in the second combination for the channel ‘A’ in table 5.1. This operational principle will also apply to the 'B' terminal. When we apply <υ_1><υ_2> (or, <0><1>) to ‘B′’ and ‘B′′’, then, from ‘B′’ terminal, one part of light beam of υ_1 frequency act as a biasing of ADM_2 and other part acts as probe beam of $RSOA_2$. Now, from ‘B′′’ terminal, light beam of υ_2 frequency goes to the input of ADM_2, so ADM_2 passes the light beam of υ_2 frequency. So, $RSOA_2$ has the pump beam of υ_2 frequency. So, there is a light beam of υ_1 frequency (or, digital state ‘0’) at the ‘B’ terminal. Also it is shown in the second combination for the channel ‘B’ in table 5.1. Now, if we apply <υ_2><υ_1> (or, <1><0>) to ‘A′’ and ‘A′′’ then, from ‘A′’ terminal, one part of light beam of υ_2 frequency act as a biasing of ADM_1 and other part acts as probe beam of $RSOA_1$. Now, from ‘A′′’ terminal, light beam of υ_1 frequency goes to the input of ADM_1, so ADM_1 passes the light beam of υ_1 frequency. So, $RSOA_1$ has the pump beam of υ_1 frequency. So, there is a light beam of υ_2 frequency (or, digital state ‘1’) at the ‘A’ terminal. It is shown in the third combination for the channel ‘A’ in table 5.1. Similarly, this process will be applicable for ‘B’ terminal also. When we apply <υ_2><υ_1> (or, <1><0>) to ‘B′’ and ‘B′′’ then, from ‘B′’ terminal, one part of light beam of υ_2 frequency act as a biasing of ADM_1 and other part acts as probe beam of $RSOA_1$. Now, from ‘B′′’ terminal, light beam of υ_1 frequency goes to the input of ADM_2, so ADM_2 passes the light beam of υ_1 frequency. So, $RSOA_2$ has the pump beam of υ_1 frequency. So, there is a light beam of υ_2 frequency (digital ‘1’) at ‘B’ channel. Also it is shown in the third combination for the channel ‘B’ in table 5.1.

Therefore, this unit restricts those unwanted inputs, like <υ_1><υ_1> (or, <0><0>) and <υ_2><υ_2> (or, <1><1>) to perform, because they are not the proper inputs as per logical representations of dibit and it checks the real dibit input combinations, like <υ_1><υ_2> (or, <0><1>) and <υ_2><υ_1> (or, <1><0>), which are shown in table 5.1. So it can be said that the inputs are controlled before entering to the system and reduces bit error problem at input terminals, coming from the channels.

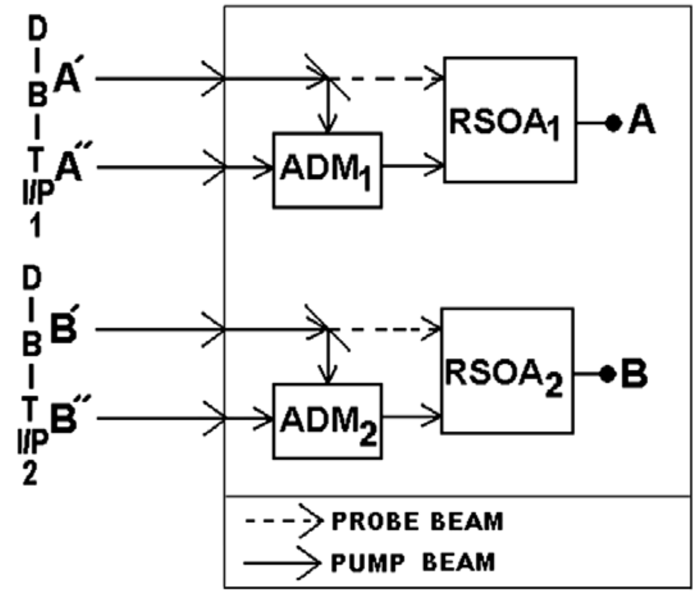


Figure 5.1: Block diagram of controlling dibit input unit.

1st Dibit Input		Controlled single bit form for Channel A	2nd Dibit Input		Controlled single bit form for Channel B
A′	A′′	A	B′	B′′	B
υ_1 (0)	υ_1 (0)	×	υ_1 (0)	υ_1 (0)	×
υ_1 (0)	υ_2 (1)	υ_1 (0)	υ_1 (0)	υ_2 (1)	υ_1 (0)
υ_2 (1)	υ_1 (0)	υ_2 (1)	υ_2 (1)	υ_1 (0)	υ_2 (1)
υ_2 (1)	υ_2 (1)	×	υ_2 (1)	υ_2 (1)	×

Table 5.1: Truth table of controlling dibit input unit.

B. Controlling logic unit

The controlling logic unit shown in figure 5.2 utilizes two input terminals 'A' and 'B', a control input terminal 'C', and one controlled output terminal 'Y'. Now, this scheme of unit provides output as AND as well as OR logic depending upon the control input states of light beam of υ_1 (or digital state ‘0’) and υ_2 (or digital state ‘1’) frequencies.

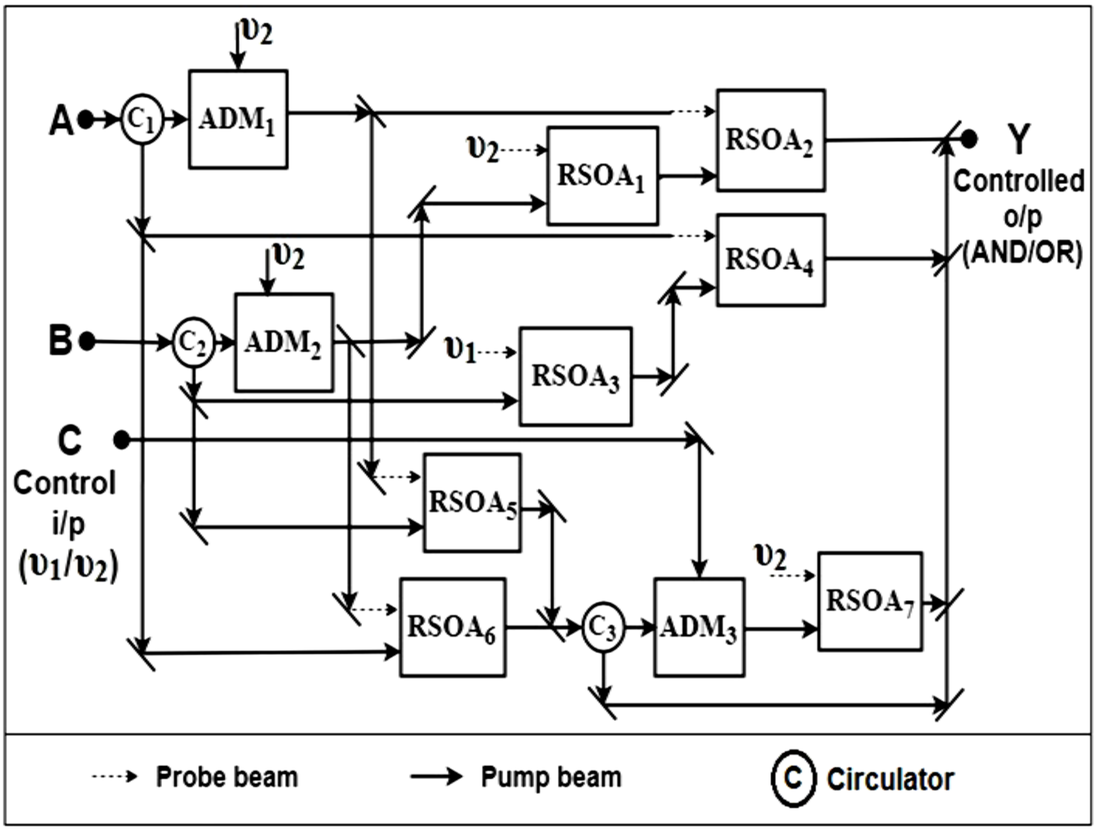


Figure 5.2: Block diagram of controlling logic unit.

I. Controlling logic unit acts as AND logic gate

Considering control input terminal ‘C’ as light beam of υ_1 frequency (or digital state ‘0’), at first, if light beam of υ_1 frequency (or digital state ‘0’) is given to both the input terminals of ‘A’ and ‘B’ at the same time for realizing this scheme. So, light beam of υ_1 frequency, coming from terminal ‘A’ is passed by ADM_1 because ADM_1 is biased by υ_2 frequency and this light beam of υ_1 frequency goes as probe beam of $RSOA_2$ and one part of this beam is coming as probe beam of $RSOA_5$. Again, light beam of υ_1 frequency, coming from terminal ‘B’ is passed by ADM_2 as it is biased by υ_2 frequency and the first part of this light beam goes as probe beam of $RSOA_6$ but other part acts as pump beam of $RSOA_1$, which has constant probe beam of υ_2

frequency. Therefore, $RSOA_1$ provides light beam of υ_2 frequency, which will act as pump beam of $RSOA_2$. So, $RSOA_2$ will give light beam of υ_1 frequency (or digital state '0') to the controlled output terminal 'Y' because light beam of υ_1 frequency is present as probe beam of $RSOA_2$. But $RSOA_5$ does not work as there is no pump beam coming from circulator 'C_2'. Similarly, $RSOA_3$ (with constant probe beam of υ_1 frequency) does not work as there is no pump beam coming from circulator 'C_2'. Since $RSOA_3$ does not work then $RSOA_4$ does not work. Again $RSOA_6$ does not have any pump beam coming from circulator 'C_1'. So $RSOA_6$ does not work. Though light beam of υ_1 frequency coming from control input terminal 'C', acts as a biasing of ADM_3, ADM_3 does not provide any light beam because $RSOA_5$ and $RSOA_6$ do not work. As there is no pump beam of $RSOA_7$ (with constant probe beam of υ_2 frequency) coming from ADM_3, $RSOA_7$ does not work. So, only $RSOA_2$ will give light beam of υ_1 frequency (or digital state '0') to the controlled output terminal 'Y'. It is theoretically satisfied by the first input combination of truth table of AND logic gate, which is given in the table 5.2.

Now, light beam of υ_1 (or digital state '0') frequency is given to the input terminal of 'A' and υ_2 (or digital state '1') frequency is given to the input terminal of 'B'. By the similar way, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 (biased by υ_2 frequency) and the light beam goes as probe beam of $RSOA_2$ and other part of this beam is coming as probe beam of $RSOA_5$. Now, $RSOA_1$ (with constant probe beam of υ_2 frequency) has no pump beam coming from ADM_2. So, $RSOA_1$ does not provide pump beam of $RSOA_2$. Therefore, $RSOA_2$ does not work. But, light beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 because ADM_2 is biased by υ_2 frequency and one part of the reflected beam comes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$

gives light beam of υ_1 frequency, which will act as pump beam of $RSOA_4$. But $RSOA_4$ doesn't work as the lack of probe beam of $RSOA_4$ coming from circulator 'C_1'. Now, other part of the reflected beam of ADM_2 comes as pump beam of $RSOA_5$. Thus, $RSOA_5$ provides light beam of υ_1 frequency because light beam of υ_1 frequency (coming from ADM_1) is present as probe beam of $RSOA_5$. But $RSOA_6$ neither has probe beam coming from ADM_2 nor has pump beam coming from circulator 'C_1'. Therefore, $RSOA_6$ does not work. Now, the light beam coming from $RSOA_5$ is entering to the ADM_3 which is biased by υ_1 frequency, coming from control input terminal 'C'. So, light beam of υ_1 frequency coming from $RSOA_5$ is reflected by ADM_3. As there is no pump beam of $RSOA_7$ (with constant probe beam of υ_2 frequency) coming from ADM_3, $RSOA_7$ does not work. Only the reflected light beam of υ_1 frequency (or digital state '0') coming from circulator 'C_3' goes to the controlled output terminal 'Y', which is theoretically satisfied by the second input combination of AND logic gate (truth table is given in the table 5.2).

Next, light beam of υ_2 (or digital state '1') and υ_1 (or digital state '0') frequencies are inserted to the input channels of 'A' and 'B' respectively. Therefore, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 (biased by υ_2 frequency) and this beam goes as probe beam of $RSOA_4$ and other part of the reflected beam from circulator 'C_1' comes as pump beam of $RSOA_6$. Now, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 (biased by υ_2 frequency) and one part of this light beam propagates as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Thus, $RSOA_1$ provides light beam of υ_1 frequency as pump beam of $RSOA_2$. Here, $RSOA_2$ has no probe beam coming from ADM_1. So, $RSOA_2$ does not work. Now, the other part of the light beam of υ_1 frequency, coming from ADM_2, goes as probe beam of $RSOA_6$. Since light beam of υ_2 frequency is present as pump beam, $RSOA_6$ gives light beam of υ_1 frequency. Whereas, $RSOA_3$ (with constant light beam of υ_1 frequency) has no pump beam coming from circulator 'C_2', $RSOA_3$ does not work. So, $RSOA_4$ does not work as there is no pump beam coming from $RSOA_3$. Again, $RSOA_5$ neither has probe beam coming from ADM_1 nor has pump beam coming from circulator 'C_2'. Therefore, $RSOA_5$ does not work. So, the light beam of υ_1 frequency from $RSOA_6$ goes to the ADM_3 (biased by υ_1 frequency, coming from control input terminal 'C'). As a result, light beam of υ_1 frequency is reflected by ADM_3. Since there is no pump beam of $RSOA_7$ coming from ADM_3, $RSOA_7$ does not work. But reflected light beam of υ_1 frequency (or digital state '0') coming from ADM_3 via circulator 'C_3' goes to the controlled output terminal 'Y'. It is fulfilled by the third input combination in the AND logic gate truth table (shown in table 5.2).

Lastly, light beam of υ_2 frequency (or digital state '1') is inserted to both the input terminals of 'A' and 'B' at the same time. So, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 which is biased by υ_2 frequency and the first part of this light beam goes as probe beam of $RSOA_4$ and the other part of the reflected beam comes as pump beam of $RSOA_6$. Again, light beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 and one part of the reflected beam comes as pump beam of $RSOA_5$. Whereas the other part of this reflected light comes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ provides light beam of υ_1 frequency, which will proceed as pump beam of $RSOA_4$. As a result, $RSOA_4$ provides light beam of υ_2 frequency. As there is no pump beam of $RSOA_1$ (with constant light beam of υ_2 frequency) $RSOA_1$ does not work. So $RSOA_2$ has no pump beam (no probe beam also) thus it does not work. Again, $RSOA_5$ does not have probe beam coming from ADM_1 and $RSOA_6$ does not have probe beam coming from ADM_2. Therefore, both the $RSOA_5$ and $RSOA_6$ do not work. So there is no input to the ADM_3 and obviously ADM_3 does not work though light beam of υ_1 frequency coming from control input terminal ‘C’, acts as a biasing of ADM_3. Thus, with constant light beam of υ_2 frequency $RSOA_7$ does not work as there is no pump beam coming from ADM_3. So the light beam of υ_2 frequency (or digital state ‘1’) coming from $RSOA_4$ goes to the controlled output terminal ‘Y’. It is satisfied by the fourth input combination of truth table of AND logic gate (given in the table 5.2).

Controlled single bit (or Digital form) input at channel ‘A’	Controlled single bit (or Digital form) input at channel ‘B’	Control input single bit (or Digital form) at terminal ‘C’	Controlled output (or Digital form) at terminal ‘Y’
A	B	C	Y
$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_1(0)$
$\upsilon_1(0)$	$\upsilon_2(1)$		$\upsilon_1(0)$
$\upsilon_2(1)$	$\upsilon_1(0)$		$\upsilon_1(0)$
$\upsilon_2(1)$	$\upsilon_2(1)$		$\upsilon_2(1)$

Table 5.2: Truth table of controlling logic unit acts as AND logic gate.

In this manner, after examining the logic output at the controlled output terminal 'Y' for these four input combinations, we can conclude that the logic output completely conforms to the truth table of the AND logic gate, with the control input terminal 'C' receiving a constant light beam of frequency υ_1 (or digital state '0'). This is illustrated in table 5.2.

II. Controlling logic unit acts as OR logic gate

Here, at first, light beam of υ_1 frequency (or digital state ‘0’) is inserted to both the inputs of ‘A’ and ‘B’ terminals simultaneously, maintaining control input terminal ‘C’ of constant light beam of υ_2 frequency (or digital state ‘1’). Thus, light beam of υ_1 frequency, coming from terminal ‘A’ is passed by ADM_1 (biased by υ_2 frequency) and goes as probe beam of $RSOA_2$ and another part of this beam arrives as the probe beam for $RSOA_5$. Similarly, light beam of υ_1 frequency, coming from terminal ‘B’ is passed by ADM_2 (biased by υ_2 frequency) and the first part of this light beam goes as probe beam of $RSOA_6$. But other part acts as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_1$ provides light beam of υ_2 frequency, which will act as pump beam of $RSOA_2$. So, $RSOA_2$ will give light beam of υ_1 frequency. $RSOA_5$ does not work due to absent of pump beam coming from circulator 'C_2'. And $RSOA_6$ is stop for the absence of pump beam coming from circulator 'C_1'. Therefore, no light beam is present at the input of ADM_3, even when a light beam of frequency υ_2 arrives from the control input terminal 'C', serving as a bias for ADM_3. Therefore, ADM_3 does not provide any light beam for the pump beam of $RSOA_7$ (with constant light beam of υ_2 frequency). So, $RSOA_7$ does not work. Again, $RSOA_3$ (with constant probe beam of υ_1 frequency) does not work as there is no pump beam coming from circulator 'C_2'. Since $RSOA_3$ does not work then $RSOA_4$ does not work. Therefore, light beam of υ_1 frequency (or digital state '0') from $RSOA_2$ goes to the controlled output port 'Y'. It is satisfied by the first input combination of truth table of OR logic gate, which is given in the table 5.3.

Now, light beam of υ_1 (or digital '0') and υ_2 (or digital '1') frequencies are inserted to the inputs of 'A′' and 'B′' respectively. By the similar way, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 and one part goes as probe beam of $RSOA_2$ and other part of this beam is coming as probe beam of $RSOA_5$. A light beam with a frequency of υ_2 from terminal 'B' is reflected by ADM_2, which is biased by the υ_2 frequency. Part of this reflected light beam serves as the pump beam for $RSOA_3$, which has a constant probe beam with a frequency of υ_1. So, $RSOA_3$ gives light beam of υ_1 frequency, which will act as pump beam of $RSOA_4$. But $RSOA_4$ doesn't work as the absence of the probe beam coming from circulator 'C_1'. Now, other part of the reflected beam of ADM_2 comes as pump beam of $RSOA_5$. Thus, $RSOA_5$ provides light beam of υ_1 frequency because light beam of υ_1 frequency is present as probe beam of $RSOA_5$. Now, the beam, coming from $RSOA_5$, proceeds to the ADM_3 which is biased by υ_2 frequency, coming from control input terminal ‘C’. So, light beam of υ_1 frequency is passed by ADM_3 and goes as pump beam of $RSOA_7$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_7$ provides light beam of υ_2 frequency. As $RSOA_1$ (with constant light beam of υ_2 frequency) does not have any pump beam, So $RSOA_1$ does not generate any light beam as pump beam of $RSOA_2$. Therefore, $RSOA_2$ does not work. Only light beam of υ_2 frequency (or digital state ‘1’) coming from $RSOA_7$ propagates to the controlled output channel ‘Y’. This is satisfied by the second input combination of truth table of OR logic gate, which is given in the table 5.3.

Next, light beam of υ_2 (or digital logic state ‘1’) and υ_1 (or digital logic state ‘0’) frequencies are inserted to the inputs of ‘A’ and ‘B’ respectively. Therefore, light beam of υ_2 frequency, coming from terminal ‘A’ is reflected by ADM_1 which is biased by υ_2 frequency and the part of this light beam comes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Now, light beam of υ_1 frequency, coming from terminal ‘B’ is passed by ADM_2 which is biased by υ_2 frequency and the part of this light beam propagates as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Thus, $RSOA_1$ provides light beam of υ_1 frequency as pump beam of $RSOA_2$. As there is no probe beam of $RSOA_2$ coming from ADM_1, it does not work. Again, as $RSOA_3$ (with constant light beam of υ_1 frequency) has no pump beam coming from circulator ‘C_2’, $RSOA_3$ does not work. So, $RSOA_4$ does not work as there is no pump beam coming from $RSOA_3$. Whereas, $RSOA_3$ (with constant light beam of υ_1 frequency) has no pump beam coming from circulator ‘C_2’, $RSOA_3$ does not work. So, $RSOA_4$ does not work as there is no pump beam coming from $RSOA_3$. Again, $RSOA_5$ neither has probe beam coming from

ADM_1 nor has pump beam coming from circulator 'C_2'. Therefore, $RSOA_5$ does not work. Now, other part of the beam, coming from ADM_2, goes as probe beam of $RSOA_6$. Since there is a light beam of υ_2 frequency is present as pump beam coming from circulator 'C_1', $RSOA_6$ gives light beam of υ_1 frequency to the ADM_3 (biased by υ_2 frequency, coming from control input terminal 'C'). As a result, light beam of υ_1 frequency is passed by ADM_3 and proceeds as pump beam of $RSOA_7$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_7$ provides light beam of υ_2 frequency (or digital state '1') to the controlled output terminal 'Y'. It is satisfied by the third input combination of truth table of OR logic gate (shown in table 5.3).

Finally, light beam of υ_2 frequency (or digital state '1') is set to both the input channels of 'A' and 'B' simultaneously. Thus, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 (biased by υ_2 frequency) and the part of this beam comes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Again, light beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 and one part of the reflected beam comes as pump beam of $RSOA_5$. While another part of the reflected light beam enters as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ provides light beam of υ_1 frequency, which will proceed as pump beam of $RSOA_4$. As a result, $RSOA_4$ gives the light beam of υ_2 frequency. Since there is no pump beam of $RSOA_1$ (with constant light beam of υ_2 frequency) $RSOA_1$ does not work. Therefore $RSOA_2$ has no pump beam as well as no probe beam therefore it does not work. Again, $RSOA_5$ does not have probe beam coming from ADM_1 so $RSOA_5$ does not work. And $RSOA_6$ does not have probe beam coming from ADM_2. Therefore, $RSOA_6$ does not work. So there is no input to the ADM_3 and obviously ADM_3 does not work though light beam of υ_1 frequency coming from control input terminal 'C', acts as a biasing of ADM_3. So, $RSOA_7$ (with constant light beam of υ_2 frequency) does not work as there is no pump beam coming from ADM_3. So the light beam of υ_2 frequency (or digital state '1') coming from $RSOA_4$ goes to the controlled output terminal 'Y'. It is fully satisfied by the fourth input combination of truth table of OR logic gate (given in the table 5.3).

In this way, we can say that, the logic output coming from the controlled output terminal 'Y' satisfies the truth table of OR logic gate after analyzing four input combinations for control input terminal 'C' as constant light beam of υ_2 frequency (or digital state '1'), shown in table 5.3.

Controlled single bit (or Digital form) input at channel 'A'	Controlled single bit (or Digital form) input at channel 'B'	Control input single bit (or Digital form) at terminal 'C'	Controlled output (or Digital form) at terminal 'Y'
A	B	C	Y
$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_2(1)$	$\upsilon_1(0)$
$\upsilon_1(0)$	$\upsilon_2(1)$		$\upsilon_2(1)$
$\upsilon_2(1)$	$\upsilon_1(0)$		$\upsilon_2(1)$
$\upsilon_2(1)$	$\upsilon_2(1)$		$\upsilon_2(1)$

Table 5.3: Truth table of controlling logic unit acts as OR logic gate.

C. Controlling dibit output unit

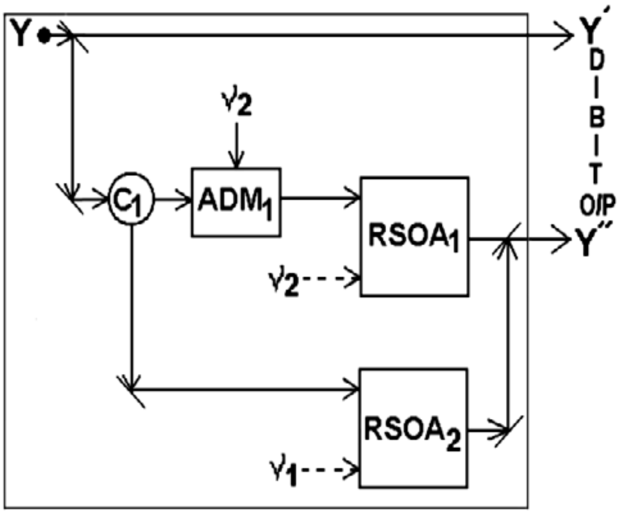


Figure 5.3: Block diagram of controlling dibit output unit.

Once we obtain the output from the controlling logic unit at terminal 'Y,' we can proceed to the controlling dibit output unit. The block diagram of controlling dibit output unit is shown in figure 5.3.

Now, if light beam of υ_1 frequency (or, digital state ‘0’) is present at ‘Y’ terminal, then this beam goes directly to the ‘Y′′ and we can get light beam of υ_1 frequency (or, digital logic state ‘0’) at ‘Y′′ output terminal. And the other part of the light beam of υ_1 frequency from ‘Y’ terminal is passed by ADM$_1$, which is biased by υ_2 frequency and goes as pump beam of RSOA$_1$. But a constant probe beam of υ_2 frequency is present in RSOA$_1$. So, we can get light beam of υ_2 frequency (digital ‘1’) at ‘Y′′′ output terminal. RSOA$_2$ (with constant light beam of υ_1 frequency) does not work, since there is no pump beam of RSOA$_2$ coming from circulator ‘C$_2$’. This is shown in second last row in table 5.4.

Single bit (or Digital form) at terminal ‘Y’	Controlled dibit output	
Y	Y′	Y′′
υ_1 (0)	υ_1 (0)	υ_2 (1)
υ_2 (1)	υ_2 (1)	υ_1 (0)

Table 5.4: Truth table of controlling dibit output unit.

By the same way, if light beam of υ_2 frequency (or, digital state ‘1’) is present at ‘Y’ terminal, then this light beam goes directly to the ‘Y′′ output terminal and we can get light beam of υ_2 frequency (digital ‘1’) at ‘Y′′ terminal. Other part of the light beam of υ_2 frequency from ‘Y’ terminal is reflected by ADM$_1$, which is biased by υ_2 frequency and goes as pump beam of RSOA$_2$. But we can get light beam of υ_1 frequency (or, digital logic state ‘0’) at ‘Y′′′ output terminal as there is a constant probe beam of υ_1 frequency. RSOA$_1$ (with constant light beam of υ_2 frequency) does not work, since there is no pump beam of RSOA$_1$ coming from ADM$_1$. It is shown in last row in table 5.4.

Therefore, if light beam of υ_1 frequency (or, digital state ‘0’) and υ_2 frequency (or, digital state ‘1’) are present at ‘Y’ terminal then we get output as <υ_1><υ_2> (or, <0><1>) and <υ_2><υ_1> (or, <1><0>) at ‘Y′’ and ‘Y′′’ terminals respectively. This is shown in table 5.4.

Finally, the overall scheme of the integrated type AND and OR logic gates with the controlling input is shown in the figure 5.4.

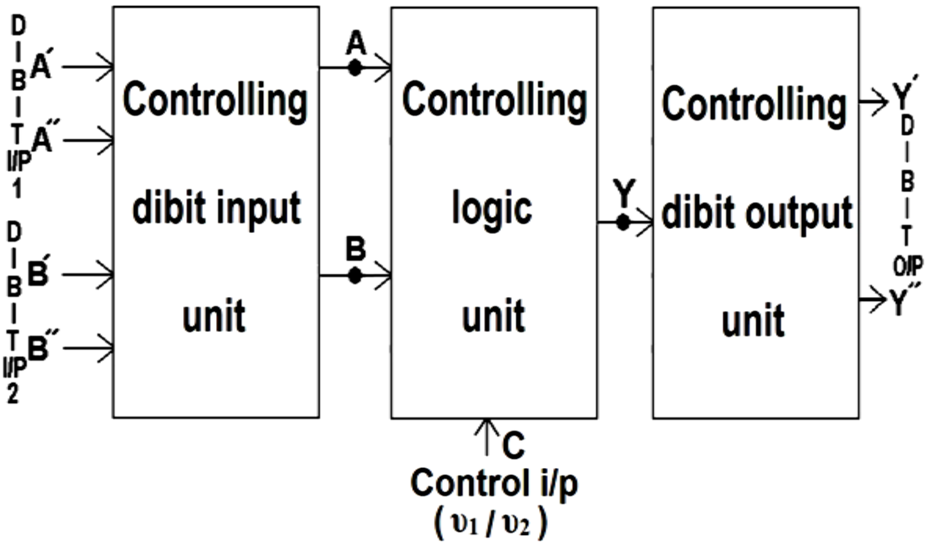


Figure 5.4: Block diagram of dibit based integrated two input AND-OR logic gate.

5.4 Realization of the integrated NAND-NOR logic gate

Now, if the dibit output is swapped between terminals 'Y′' and 'Y′′', the behavior of the logic gates changes. Specifically, the AND logic output will function as a NAND logic output, and the OR logic output will operate as a NOR logic output, shown in figure 5.5. This transformation leverages the advantages of the dibit representation technique, allowing for more versatile logic gate operations by simply interchanging the outputs.

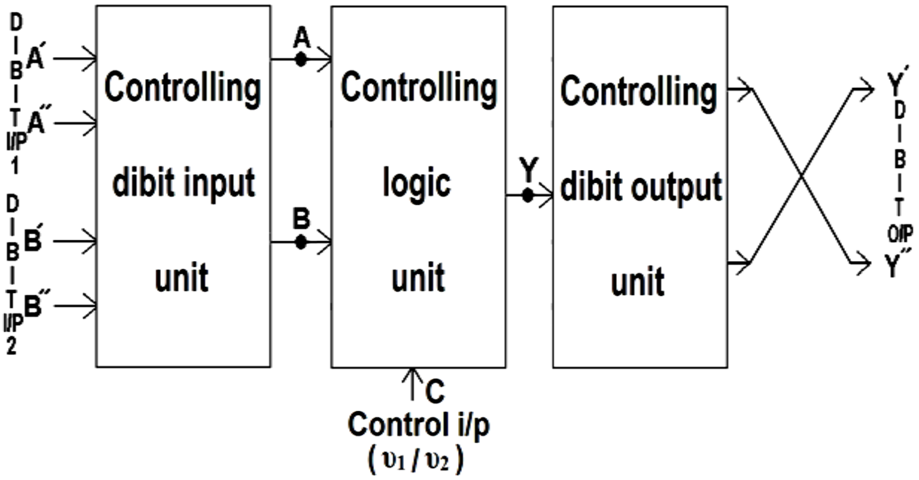


Figure 5.5: Block diagram of dibit based integrated two input NAND-NOR logic gate.

5.5 Simulation of the integrated AND-OR logic gate

MATLAB (R2008a) simulink tools have been used for simulation of the above dibit based integrated type two input AND and OR logic gates with a controlling input using RSOA and ADM types optical switches. “DIBIT I/P 1”, “DIBIT I/P 2”, “Control i/p” and “ DIBIT O/P” terminals are used for applying proper inputs and getting proper output. In simulation process, for providing the two frequency states, υ_1 frequency (or, digital state ‘0’) and υ_2 frequency (or, digital state ‘1’) are represented by ‘3’ and ‘8’ respectively. Maintaining the similarity of the block diagram (shown in figure 5.4) simulative model of the integrated scheme when acts as AND logic gate is shown in figure 5.6 keeping control input as υ_1 frequency or ‘3’. Another simulative model of the integrated scheme when acts as OR logic gate is also shown in figure 5.7 keeping control input as υ_2 frequency or ‘8’. Here, a particular dibit input combination (<8> <3> and <3> <8>) is used for showing the simulation process of the integrated scheme.

Now, each of the RSOA blocks is properly programmed according to the RSOA mechanism with two terminals “pr” for probe beam and “pm” for pump beam and “y” as output line in RSOA blocks. According to the theory of RSOA, if the input beams of light of pump beam and probe beam are treated as say “3 peta Hz” or, the beam of light of υ_1 frequency or, digital low logic state “0” and “8 peta Hz” or, the beam of light of υ_2 frequency or, digital high logic state “1” correspondingly, after that we get “8 peta Hz” = υ_2 = digital “1” at the output line of these blocks. The state of the output alters if pump beam and probe beam are changed consequently.

Furthermore, the ADM block has been simulated to adhere to the correct operational principles of ADM. Now, if ADM is biased by a particular light beam frequency, say “3 peta Hz” = υ_1 = digital logic state “0” at “bias” terminal, then this block drops the frequency coming from “input” terminal to “drop” terminal and passes other frequency, say “8 peta Hz” = υ_2 = digital logic state “1” to “out” terminal. If the biasing is changed, opposite incident happens. Internally, RSOA and ADM blocks have been connected in proper way for modeling three internal units (subsystems) of the ‘controlling dibit input unit’, ‘controlling logic unit’ and ‘controlling dibit output unit’ of the simulative model, shown in figures 5.8, 5.9 and 5.10 correspondingly, ensuring consistency in the theoretical block diagrams in figures 5.1, 5.2 and 5.3 respectively.

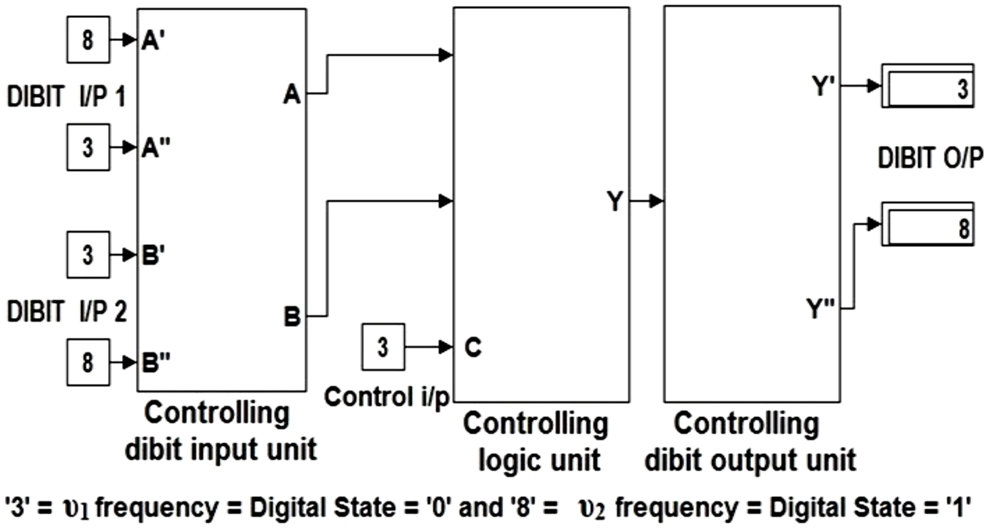
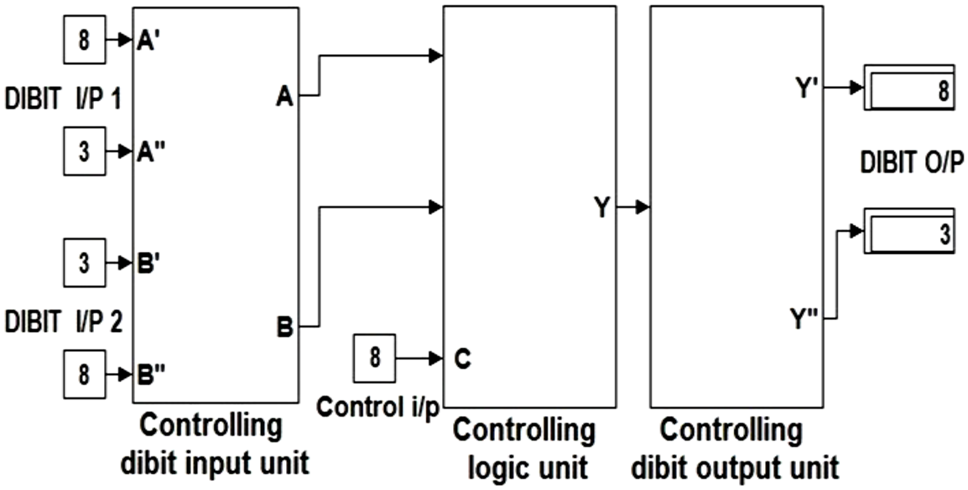
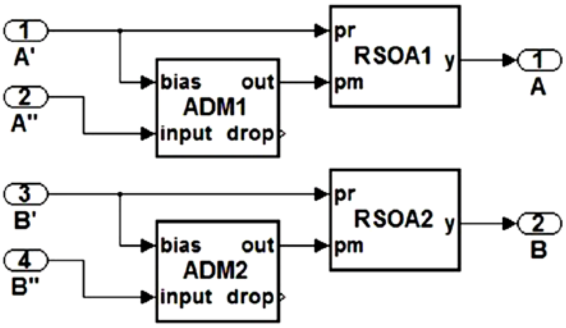


Figure 5.6: Simulative model of the integrated scheme when acts as AND logic gate.



'3' = υ_1 frequency = Digital State = '0' and '8' = υ_2 frequency = Digital State = '1'

Figure 5.7: Simulative model of the integrated scheme when acts as OR logic gate.



pr = Probe Beam, pm = Pump Beam

Figure 5.8: Internal simulative model of the controlling dibit input unit (subsystem).

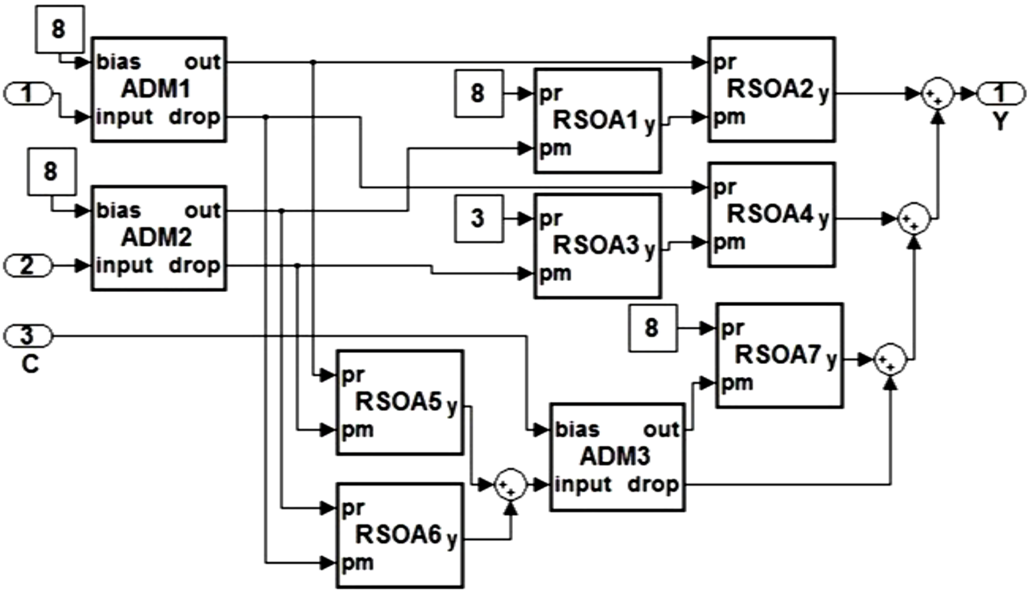


Figure 5.9: Internal simulative model of the controlling logic unit (subsystem).

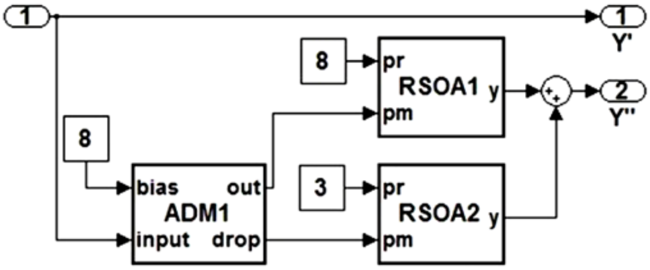


Figure 5.10: Internal simulative model of the controlling dibit output unit (subsystem).

5.6 Simulation of the integrated NAND-NOR logic gate

Maintaining the similarity of the block diagram (shown in figure 5.5), simulative model of the integrated scheme when acts as NAND logic gate is shown in figure 5.11 keeping control input as υ_1 frequency or ‘3’. Figure 5.12 illustrates another simulation model of the integrated scheme functioning as a NOR logic gate, with the control input set to υ_2 frequency or '8'. Here, “DIBIT O/P” are swapped between terminals 'Y′' and 'Y′′' of the figure 5.6 and figure 5.7 to get controlling dibit outputs for NAND and NOR logic gates respectively, keeping same dibit input combination (<8> <3> and <3> <8>).

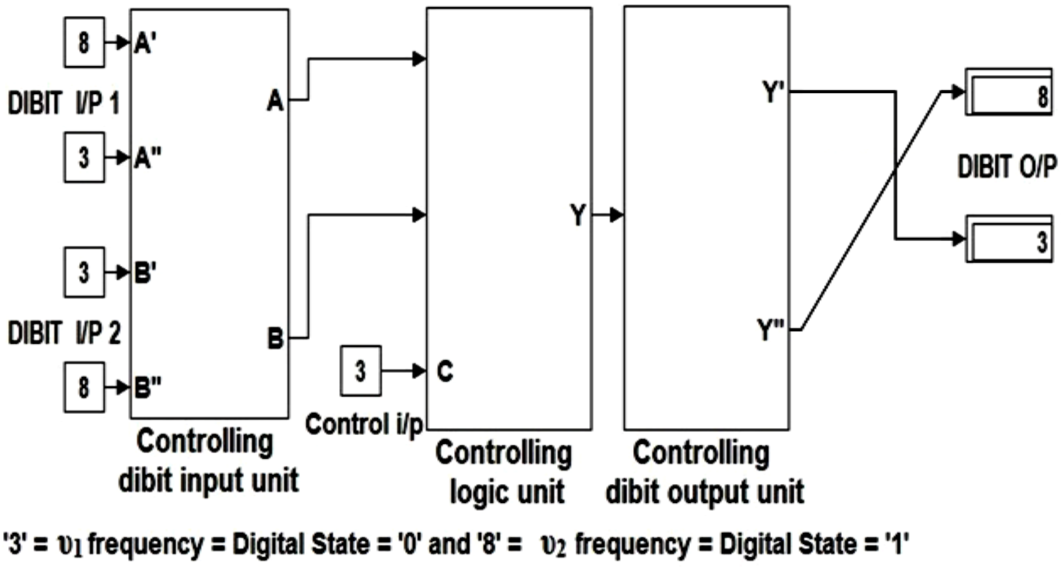
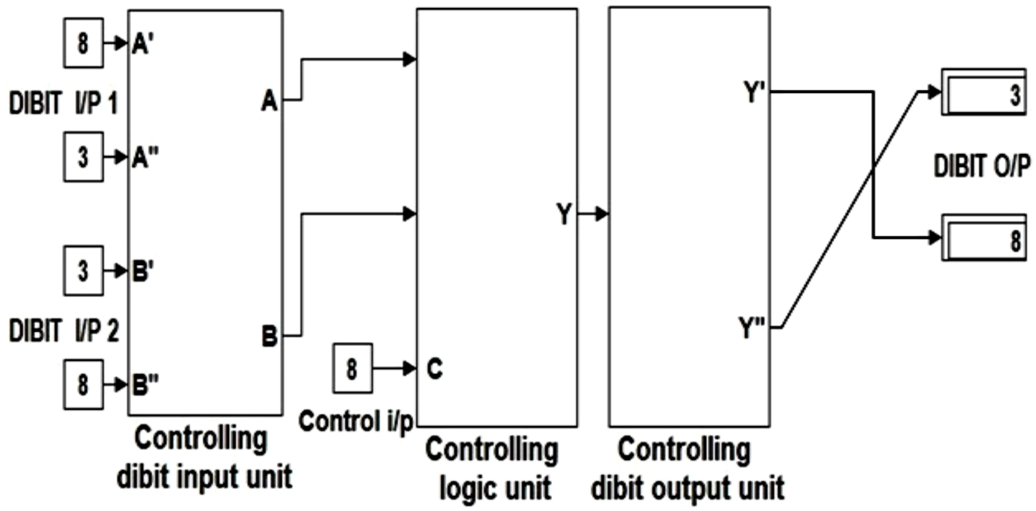


Figure 5.11: Simulative model of the integrated scheme when acts as NAND logic gate.



'3' = υ_1 frequency = Digital State = '0' and '8' = υ_2 frequency = Digital State = '1'

Figure 5.12: Simulative model of the integrated scheme when acts as NOR logic gate.

5.7 Results and discussion

Now, any input combination must be taken into consideration for satisfying the above integrated scheme of all optical digital circuit. For example, if we apply <8><3> and <3><8> are inserted at the two dibit input lines and ‘3’ is inserted as control input then we can get <3><8> at the dibit output terminal (shown in figure 5.6). By this way, we can see that, this model satisfies truth table of AND logic which is shown in table 5.2. But, when ‘8’ is inserted as control input then we can get <8><3> at the dibit output terminal (shown in figure 5.7). So, we can say that, this model satisfies truth table of OR logic which is shown in table 5.3. This integrated scheme can also be satisfied by the other input combinations of the truth tables of respective AND and OR logic gates. By the same way, this scheme can also be satisfied for NAND and NOR logics shown from figure 5.11 and figure 5.12 respectively.

5.8 Future research directions

The simulative verification mentioned refers to a method where logic gates (like AND and OR gates) with control inputs are tested and validated using simulation techniques. These gates are fundamental components in digital circuitry, and their correct functioning is crucial for building more complex arithmetic and logic devices.

By ensuring that these gates perform correctly in simulations, engineers can use them as building blocks to develop and verify the performance of other digital devices. This approach is particularly useful in frequency encoding principles, where information is encoded in the frequency of signals.

In the context of optical computation, simulative verification becomes significant for implementing various schemes of all optical integrated logic and arithmetic circuits. Optical computing leverages light signals instead of traditional electronic signals, promising faster processing speeds and potentially lower energy consumption.

The ability to simulate and verify these optical logic and arithmetic circuits lays the ground-work for constructing advanced optical computers. Engineers envision a future where multiple all optical digital devices and circuits can be combined to create sophisticated optical computers capable of handling complex computations efficiently. Thus, the accurate simulation and verification of basic components like logic gates are essential steps towards realizing these advanced optical computing systems.

5.9 Conclusions

The dibit representation technique mentioned is highly regarded for its accuracy and reliability in digital signal processing. It effectively mitigates bit error problems by improving the signal-to-noise ratio, thereby ensuring robust performance even in noisy environments. Additionally, this technique facilitates a high degree of parallelism, allowing multiple operations to be conducted simultaneously.

In the context of logic operations, specifically using optical circuits, the interchangeability of dibit outputs between terminals 'Y´' and 'Y´´' introduces a significant advantage. When the dibit outputs are swapped between these terminals, the logical operations performed by AND and OR gates transform into NAND and NOR operations, respectively. This interchangeability leverages the properties of the dibit representation technique to effectively achieve different logical outcomes without needing separate physical components for each logic type.

Furthermore, the presence of control inputs in these optical logic circuits enhances their flexibility. These inputs enable users to select specific logic operations within the integrated scheme of all optical logic circuits. This capability is crucial for adapting the circuit's behavior to different computational tasks or changing operational requirements without physically altering the circuit configuration.

In summary, the dibit representation technique not only enhances accuracy and reliability in signal processing but also enables versatile logic operations in all optical circuits through simple reconfiguration of dibit outputs and utilization of control inputs. This makes it a powerful tool for advancing optical computing technologies with improved performance and functionality.

References

[5.1]. A. K. Ghosh, A. Bhattacharya, M. Raul and A. Basuray, “Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic.” Optics & Laser Technology, 44(5), 1583–1592 (2012).

[5.2]. S. Dey and S. Mukhopadhyay, “Approach of implementing phase encoded quantum square root of NOT gate.” Electronics Letters, 53(20), 1375-1377. (2017).

[5.3]. D. K. Gayen, T. Chattopadhyay and K.E. Zoiros, “All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach–Zehnder interferometer.” Journal of Computational Electronics, 14(1), 129-138 (2015).

[5.4]. I. S. Amiri, et al. “Nanometer bandwidth soliton generation and experimental transmission within nonlinear fiber optics using an add-drop filter system.” Journal of Computational and Theoretical Nanoscience, 12(2), 221-225 (2015).

[5.5]. B. Sarkar and S. Mukhopadhyay, “An all optical scheme for implementing an integrated Pauli’s X, Y and Z quantum gates with optical switches.” Journal of Optics, 46(2), 143-148 (2017).

[5.6]. P. P. Sarkar, B. Ghosh, S. N. Patra and S. Mukhopadhyay, “A new scheme of an all optical frequency encoded dibit based latch with its simulated result.” Journal of Optical Technology, 84(9), 631–634 (2017).

[5.7]. S. Dutta and S. Mukhopadhyay, “All optical frequency encoding method for converting a decimal number to its equivalent binary number using tree architecture.” Optik - International Journal for Light and Electron Optics, 122(2), 125-127 (2011).

[5.8]. V. Çakmak, F. Ufuk and N. Karabulut, “Diffusion-weighted MRI of pulmonary lesions: Comparison of apparent diffusion coefficient and lesion-to-spinal cord signal intensity ratio in lesion characterization.” Journal of Magnetic Resonance Imaging, 45(3), 845-854 (2017).

[5.9]. S. K. Chandra and S. Mukhopadhyay, “All optical alternative approach of conducting NAND and NOR logic gates with phase encoding principle.” Optik-International Journal for Light and Electron Optics, 123(11), 1022-1025 (2012).

[5.10]. J. Wang and L. R. Chen, “Low crosstalk Bragg grating/Mach-Zehnder interferometer optical add-drop multiplexer in silicon photonics.” Optics express, 23(20), 26450-26459 (2015).

[5.11]. S. Dey and S. Mukhopadhyay, “Implementation of all-optical Pauli-Y gate by the integrated phase and polarisation encoding.” IET Optoelectronics, 12(4), 176-179 (2018).

[5.12]. S. Dey and S. Mukhopadhyay, “A method of generation of sharp peaked parabolic and hyper parabolic optical pulses by the use of Pockels effect for long distance communication.” Journal of Optics, 47(3), 272-277 (2018).

[5.13]. S. Saha, S. Biswas and S. Mukhopadhyay, “Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach–Zehnder interferometer-based semiconductor optical amplifier.” IET Optoelectronics, 11(5), 201-207 (2017).

[5.14]. S. Dutta and S. Mukhopadhyay, “Alternating approach of implementing frequency encoded all-optical logic gates and flip-flop using semiconductor optical amplifier.” Optik - International Journal for Light and Electron Optics, 122(12), 1088-1094 (2011).

[5.15]. G. Hu, et al. “Securing image information using double random phase encoding and parallel compressive sensing with updated sampling processes.” Optics and Lasers in Engineering, 98, 123-133. (2017).

[5.16]. P. P. Sarkar, et al. “Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer.” Journal of Optical Technology, 83(4), 257–262 (2016).

[5.17]. B. Ghosh, et al. “A Novel Approach to Realize of All Optical Frequency Encoded Dibit Based XOR and XNOR Logic Gates Using Optical Switches with Simulated Verification.” Optics and Spectroscopy, 124(3), 337-342 (2018).

[5.18]. J. Zhu, et al. “Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination.” Optics express, 24(25), 28549-28560 (2016).

[5.19]. S. K. Garai and S. Mukhopadhyay, "A method of optical implementation of frequency encoded different logic operations using second harmonic & difference frequency generation techniques in non-linear material." Optik-International Journal for Light and Electron Optics, 121(8), 715-721 (2010).

[5.20]. S. K. Garai and S. Mukhopadhyay, "All-optical frequency encoded binary half subtractor using periodically poled lithium niobate waveguide and reflecting semiconductor optical amplifier." Optics and Photonics Letters, 3(1), 15-22 (2010).

[5.21]. P. P. Sarkar, B. Satpati and S. Mukhopadhyay, "New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors." Journal of Optics, 42(4), 360-366 (2013).

[5.22]. S. Chen, et al. "Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon." IEEE Photonics Technology Letters, 28(17), 1874-1877 (2016).

[5.23]. R. Mansoor, et al. "Crosstalk suppression bandwidth optimisation of a vertically coupled ring resonator add/drop filter." IET Optoelectronics, 9(2), 30-36 (2015).

[5.24]. A. N. Z. Rashed, et al. "Optical Add Drop Multiplexer (OADM) Based on Dense Wavelength Division Multiplexing Technology in Next Generation Optical Networks." International Journal of Multimedia & Ubiquitous Engineering, 7(1), 1-14 (2012).

[5.25]. P. P. Sarkar and S. Mukhopadhyay, "All optical frequency encoded NAND logic operation along with the simulated result." Journal of Optics, 43(3), 177-182 (2014).

[5.26]. H. Kim, et al. “Degradation characteristics of red light-emitting CuInS2/ZnS quantum dots as a wavelength converter for LEDs.” Electrochemical and Solid-State Letters, 14(10), K55-K57 (2011).

[5.27]. K. Y. Wang A. C. Foster, “Ultralow power continuous-wave frequency conversion in hydrogenated amorphous silicon waveguides.” Optics letters, 37(8), 1331-1333 (2012).

[5.28]. S. P. Singh, S. Kar and V. K. Jain, “Performance of all-optical WDM network in presence of four-wave mixing, optical amplifier noise, and wavelength converter noise.” Fiber and Integrated Optics, 26(2), 79-97 (2007).

[5.29]. S. Singh, et al. “Photonic processing of all-optical Johnson counter using semiconductor optical amplifiers.” IET Optoelectronics, 11(1), 8-14 (2016).

[5.30]. B. Ghosh and S. Mukhopadhyay, “A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124(21), 4813-4815 (2013).

CHAPTER-6

Design and simulation of a dibit based all optical frequency encoded controlled full subtractor using optical switches.

Abstract

Data has become one of the most valuable and sought after assets in the modern world. At the same time, the speed of data communication remains a critical concern in current technology. Since light is the fastest medium for transmission, photonic communication has become a key area of interest, with proven effectiveness. Utilizing this technology, researchers have already proposed designs for all optical digital logic gates and various other devices. In this manuscript, the authors present an all optical, frequency encoded, dibit based, digitally controlled full subtractor utilizing a reflected semiconductor optical amplifier (RSOA) and an add/drop multiplexer (ADM). The proposed dibit based system offers superior performance compared to conventional electronic circuits, featuring a lower signal-to-noise ratio. As a dibit-based digital circuit, the proposed all-optical full subtractor prevents unnecessary inputs, enhancing security. The operation of this all optical device has been verified using MATLAB R2017(a) simulation software.

Work reported in this chapter was published in:

i. **Bitan Ghosh**, Partha Pratim Sarkar and Prof. Ardhendu Ghoshal "Design of dibit based all optical frequency encoded controlled full subtractor using optical switches." Journal of Optics, 53.1 (2024): 610-621.

6.1 Introduction

In last few decades speed related problems are happening in the field of information processing, communication etc. To overcome such problem photon can be used for superfast information processing element. There are many types of encoding techniques for designing the all optical logical or arithmetic devices[6.1-6.2]. The different kind of encoding techniques are there like frequency encoding[6.3-6.6], phase encoding[6.7], intensity encoding[6.8], spatial encoding[6.9], polarization encoding[6.10] etc.

The frequency encoding technique is the most compatible among the various encoding techniques, as the frequency of the light beam remains constant and unaffected by reflection, refraction, absorption, and other processes. In the frequency encoding technique, two different frequencies can represent two distinct states during the data computation and encoding process. One specific value of frequency is considered as digital high state or ‘1’ and another frequency is considered as digital low state or ‘0’. Following this logic, optical light beam having frequency ‘ν_1’ treated as digital low state or ‘0’ similarly optical light beam having frequency 'ν_2’ treated as digital high state or ‘1’.

Again, digital logic state can be expressed by two successive bit positions, in the dibit representation technique[6.11-6.12]. So the digital low state or ‘0’ is expressed as dibit low logic state [0][1] and the digital high state or ‘1’ is express as dibit high logic state [1][0] subsequently. These two states can be represented by two distinct frequencies. That claims the existence of two frequencies together like, $[\nu_1][\nu_2]$ expressed the digital low logic state ‘0’ and $[\nu_2][\nu_1]$ presented the digital logic high state ‘1’. This process in optics for logical operation was first proposed by S. Mukhopadhyay[6.13]. Subtractor performs the subtraction operation in between any two numbers. Subtractors are utilized in digital systems for logical and arithmetic operations. In this manuscript, the authors propose an all optical, frequency encoded half subtractor based full subtractor employing optical switches, an add/drop multiplexer (ADM), and a reflected semiconductor optical amplifier (RSOA). Additionally, this circuit is designed with an appropriate dibit checking capability.

Previously, dibit based digital logic gates are have been used in few papers, for various journals. But in this chapter a new idea of construction regarding dibit based frequency encoded all optical half subtractor based full subtractor have been proposed with a dibit checking facility, which will oppose the incorrect inputs to the dibit based logic gates. The dibit logic states [0][0] and [1][1] will consider as wrong input, so the dibit verifying block will counter those wrong inputs to enter. This feature will enhance the reliability of the logic gates.

6.2 Optical switches

Add drop multiplexer[6.14-6.16] which is a frequency selective optical switching device. It has four ports: input, biasing, output, and drop. The output and drop operations of this device depend on the biasing applied to it. When a specific bias is applied to the device, it reflects the light beam with the same frequency as the bias, while allowing the other beam to pass through. Similarly, when the biasing is changes the alternate operation happens. Additionally, if no biasing is applied to this device, it will not function.

Another optical switching device is reflected semiconductor optical amplifier (RSOA)[6.17-6.21]. It has basically three ports two input ports and one output port. In two input ports there, one is probe beam and another one is pump beam. Basically, the probe beam is weak and the probe beam is strong, when power is concerned. If two light wave having different frequencies (say ν_2, ν_1) given to the input ports of the device then the device will provide output having the frequency of probe beam and the power of the pump beam i.e. high power with low frequency. In this way these two devices may be used to develop different all-optical logical operations[6.22-6.25]. Reflecting semiconductor optical amplifier[6.26-6.36] is the most valuable optical switch, that can be used to design various optical circuits.

6.3 Realization of dibit based all optical frequency encoded full subtractor

In figure 6.1, the basic block diagram of dibit based all optical frequency encoded full subtractor is shown. Here, the all optical full subtractor is sub divided into three blocks, 'Block 1', 'Block 2', 'Block 3' respectively. Block 1 have <A'>, <A''>, <B'> and <B''> four input ports for taking two dibit inputs and two output ports <OUT_1> and <OUT_2> respectively. There are three input ports <IN_1>, <C'>, <C''>, also having three output ports in which first and second are <Y1'>, <Y1"> for giving the dibit difference output and the third one is <OUT_3> in block 2. The last block, block 3 have two input ports, <IN_1>, <IN_2> and two output ports <Y2'>, <Y2"> for providing dibit borrow output. The internal circuitry of block 1, block 2 and block 3 is shown in figure 6.2, figure 6.3 and figure 6.4 respectively.

At first, light beam of different frequencies (say ν_1 and ν_2) are given to the dibit input ports of block 1 <A'><A">, <B'><B">) and the dibit input ports of block 2 <C'><C">, respectively. As this scheme of all optical full subtractor circuit have the ability of dibit examine facility at the input side, it will scan the inputs by the ADM_1, $RSOA_1$, ADM_2, $RSOA_2$, ADM_{11} and $RSOA_{12}$ blocks respectively. Here, light beam having frequency ν_1 is flowing from input port <A'>, which is the biasing light beam of ADM_1 and also the probe beam of $RSOA_1$. Another one input is$\nu_2$coming from input port <A"> is directly feed to the ADM_1. As per working principle of ADM, here ADM_1 is biased by the light beam of ν_1 frequency, so it will pass the light beam having frequency of ν_2 and directly feed to the RSOA$_1$ as pump beam. Now, as per working function of RSOA, as the probe beam and pump beam inputs of RSOA$_1$ are the light beam of ν_1 and ν_2 frequencies respectively, so the output of RSOA$_1$ will be the light beam having frequency ν_1. Similarly, the light beam of ν_1 frequency will also come out from RSOA$_2$ and RSOA$_{12}$, because in the input ports <B'><B"> of block 1 and <C'><C"> of block 2, the inputs are similar as the input ports <A'> and <A"> say <ν_1><ν_2>.

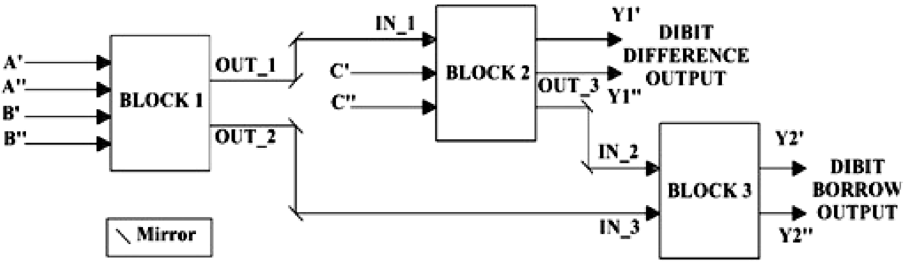


Figure 6.1: Basic block diagram of dibit based all optical frequency encoded full subtractor.

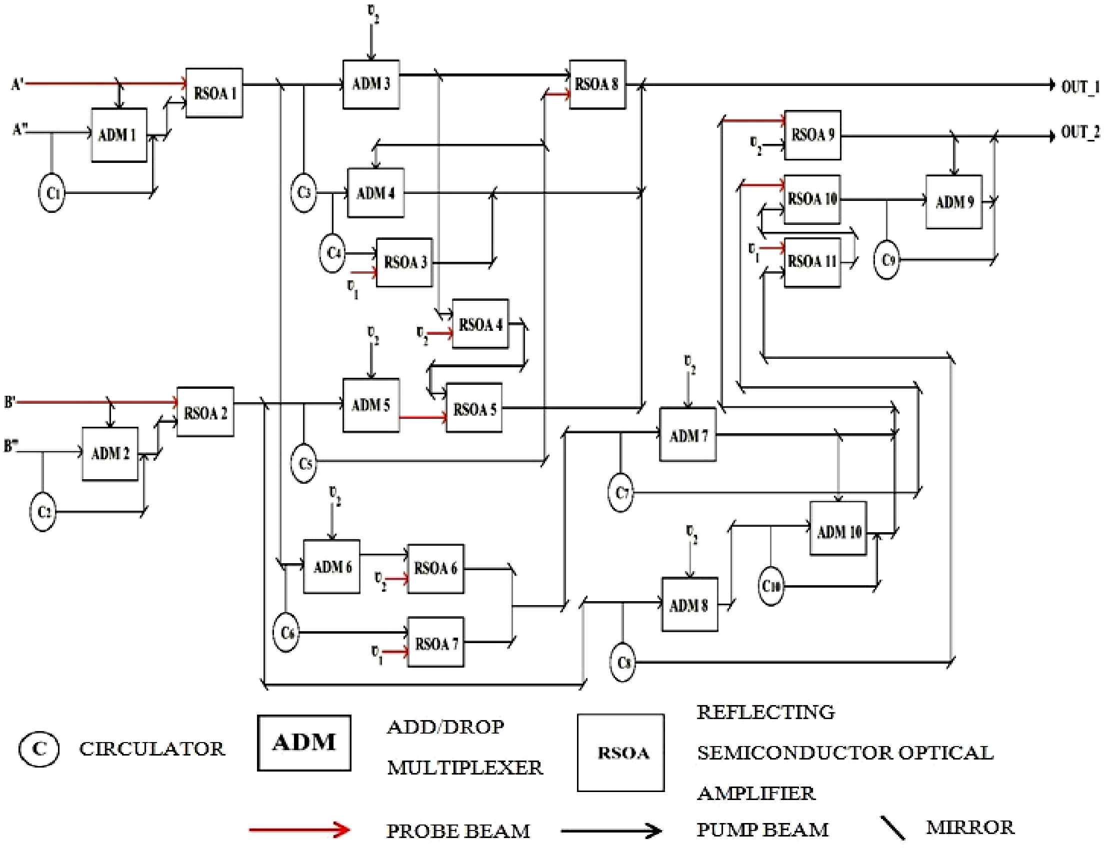


Figure 6.2: Internal block diagram of block 1.

At this moment the outputs of $RSOA_1$, $RSOA_2$ and $RSOA_{12}$ i.e., the light beam having frequency ν_1 is feed to the ADM_3, ADM_5, ADM_6 and ADM_8 in block 1 and ADM_{14}, ADM_{17} in block 2. As previously mentioned, the ADM blocks are biased with light beam having frequency ν_2 so the light beam having frequency ν_1 is passed through the ADM blocks. In block 1, further the light beam having frequency ν_1 will feed to $RSOA_4$ as pump beam, in $RSOA_5$ as probe beam, in $RSOA_6$ as pump beam and in $RSOA_8$ as pump beam in block 1. In $RSOA_4$ ν_2 is feed as the probe beam so the $RSOA_4$ give the output of light beam having frequency ν_2 the output of $RSOA_4$ is feed to the $RSOA_5$ as the pump beam and the probe beam of $RSOA_5$ is ν_1 (previously said), so the output of $RSOA_5$ will be ν_1 and the light beam is travels towards the output port OUT_1. As there is no probe beam is feed to the $RSOA_8$ so it will not in operation. In $RSOA_6$ light beam having frequency ν_2 is feed as probe beam, so the output of the $RSOA_6$ will be light beam having frequency ν_2 and directly injected to the input of ADM_7. As ADM_7 is biased with light beam having frequency ν_2, so ADM_7 will drop the input light beam having frequency ν_2 through circulator C_7 and directly feed to the $RSOA_{10}$ as probe beam. In this logical combination $RSOA_{10}$ have no pump beam so it will not function. In ADM_{10} light beam having frequency ν_1 is feed as input from the output of ADM_8 which is previously said, as in ADM_{10} no biasing is given, so it will pass the light beam having frequency ν_1 and feed to the $RSOA_9$ as the probe beam, also the pump beam is the light beam having frequency ν_2 so the output of $RSOA_9$ will be the light beam having frequency ν_1, which is further travels to the output port OUT_2 of block 1. Output port OUT_1 of block 1 is directly connected to input port IN_1 of block 2, so the light beam having frequency ν_1 is feed to the ADM_{12} and ADM_{15} in block 2. As previously mentioned, the ADM blocks are biased with light frequency ν_2 for this reason the ADM blocks will pass the light beam having frequency ν_1. Like block 1 similarly in block 2 $RSOA_{14}$ will give output light beam having frequency ν_2 and that will be injected to the $RSOA_{15}$ as pump beam so $RSOA_{15}$ give output light beam having frequency ν_1 because the probe beam of $RSOA_{15}$ will be the light beam having frequency ν_1 coming from the output of ADM_{14} (as said previously). The output of $RSOA_{15}$ is feed to the output terminal <Y1'> and the input of ADM_{20} which is biased with the light beam having frequency ν_1 so ADM_{20} will pass the light beam having frequency ν_1 and feed to the $RSOA_{22}$ as a pump beam, also the probe beam of $RSOA_{22}$ is the light beam having frequency ν_2 so, the output of the $RSOA_{22}$ will be the light beam having frequency $\nu_{2.}$ The output will be directly connected to another output terminal, which is <Y1">.

Finally, in the dibit difference output ports <Y1'> and <Y1"> the output will be in dibit form $<\nu_1>$ and $<\nu_2>$ or in digital logic '0' and '1' respectively which is satisfying the truth table of the full subtractor. $RSOA_{18}$ will not in operation because there is no probe beam in this logical combination. Again, similarly like block 1 in $RSOA_{16}$ the probe beam having frequency ν_2 so, the output of the $RSOA_{16}$ will be ν_2 and feed to the ADM_{16}. ADM_{16} is biased with a light beam having frequency ν_2 so, it will drop the input through circulator C_{16} and feed to the $RSOA_{20}$ as probe beam as there is no pump beam in this logical combination in $RSOA_{20}$ so, $RSOA_{20}$ will not in operation. Again, similarly like block 1 the output of ADM_{17} is feed to the input of ADM19 as ADM_{19} have no biasing in this logical combination so it will pass the input beam to the output having frequency ν_1 which is injected to the $RSOA_{19}$ as probe beam. Already the pump beam of $RSOA_{19}$ is given which is having frequency ν_2. So, the output of $RSOA_{19}$ will be the light beam having frequency ν_1. The output of $RSOA_{19}$ is feed to the output port OUT_3 of block 2.

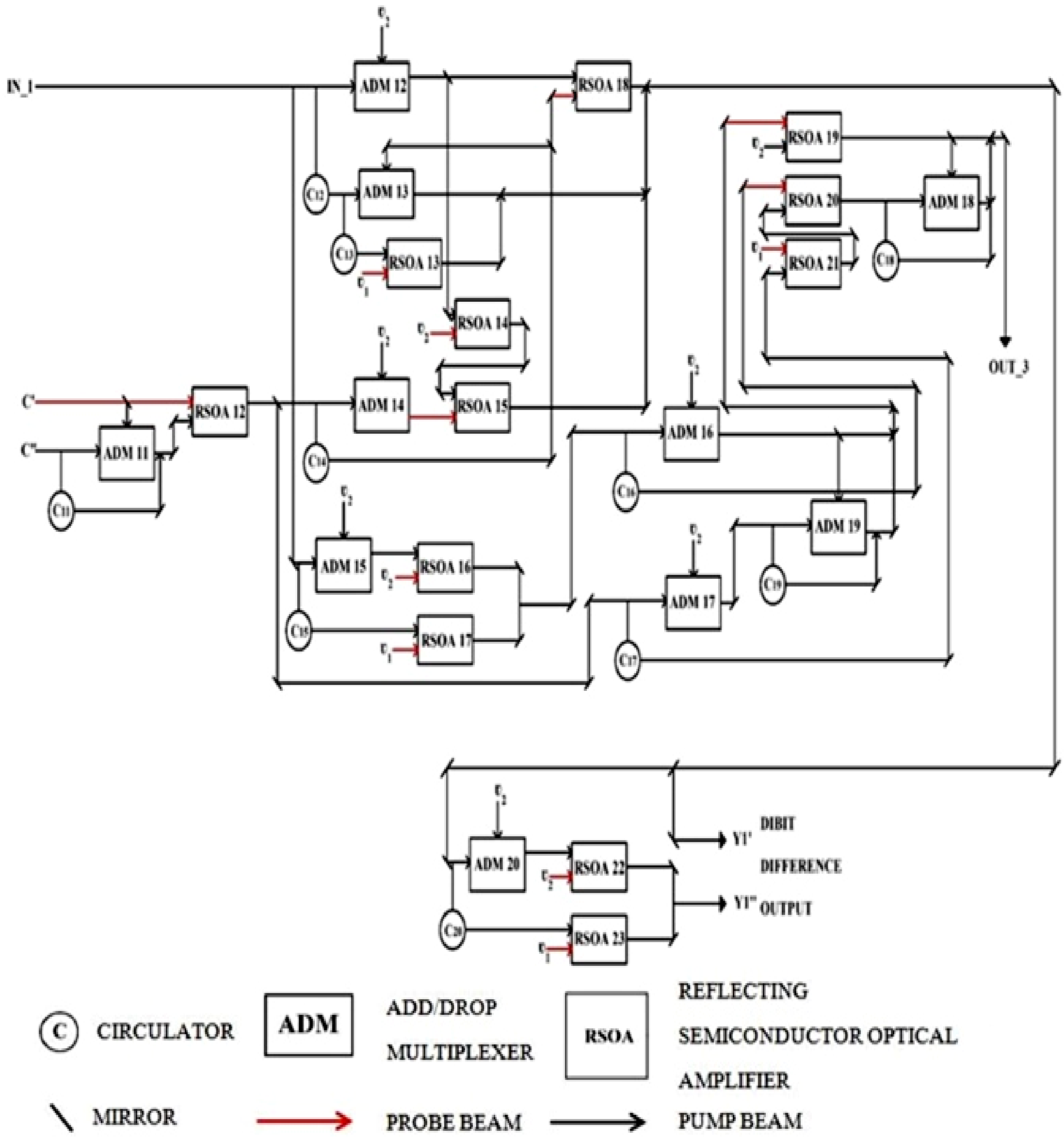


Figure 6.3: Internal block diagram of block 2.

Now, in block 3 there are two input ports IN_1 and IN_2 which are directly connected to the output ports OUT_2 of block 1 and OUT_3 of block 2. Now in the both output ports the output will be light beam having frequency ν_1. So, the light beam having frequency ν_1 is injected to the ADM$_{21}$ and ADM$_{22}$. Both the ADM blocks are biased with the light beam having frequency ν_2 so, both the ADM blocks will pass the input light beam having frequency ν_1. Now, the output of ADM$_{21}$ is feed to the RSOA$_{24}$ and in RSOA$_{25}$ as pump beam. Also, the output of ADM$_{22}$ is injected to the RSOA$_{26}$ as probe beam. Already the probe beam of RSOA$_{24}$ is given having frequency of ν_2. So, the output of the $RSOA_{24}$ will be ν_2 and it will be injected to the $RSOA_{26}$ as pump beam, the output of the $RSOA_{26}$ will be light beam having frequency ν_1. The output of the $RSOA_{26}$ is feed to the ADM_{23} which is biased with light beam having frequency ν_1 so the ADM_{23} will drop the input signal through the circulator C_{23} and travels towards the output terminal <Y2'>. From the output terminal <Y2'> one part of the light beam having frequency $\nu_1$injected to the ADM_{24} which is biased with the light beam having frequency ν_2 so it will pass the input light beam and feed to the $RSOA_{27}$ as pump beam. Already the probe beam of $RSOA_{27}$ is given having frequency ν_2 so, the output of $RSOA_{27}$ will be the light beam having frequency ν_2 and it will travel towards the output terminal <Y2">. As there is no probe beam present in this logical combination so $RSOA_{25}$ will not in operation. Finally, at the dibit borrow output ports <Y2'> and <Y2">, the output will be in dibit form or in digital logic '0' and '1', respectively, in accordance with the truth table of the full subtractor. Truth table of full subtractor is shown in table 6.1.

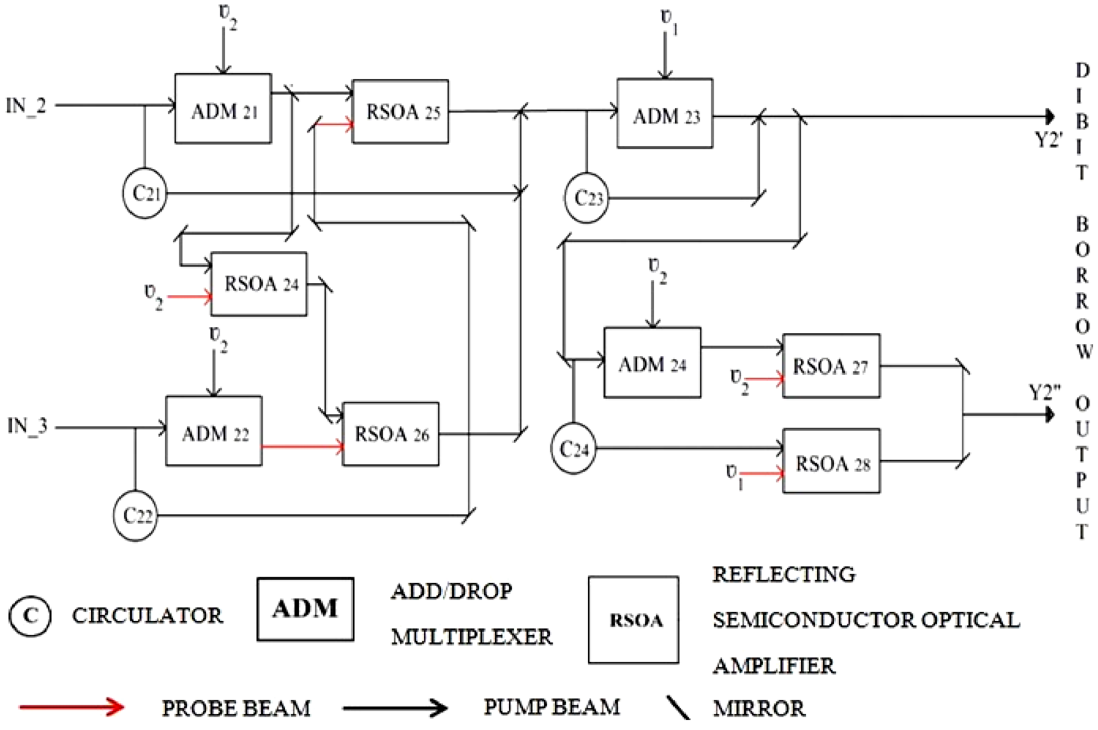


Figure 6.4: Internal block diagram of block 3.

Secondly, in the dibit input terminals of block 2 <C’> and <C”> the input signal is changed to <ν_2>, <ν_1> but the other inputs <A’>, <A”>, <B’> and <B”> are remains unchanged so the output of block 1 is same as the previous combination i.e., from OUT_1 and OUT_2 light beam having frequency ν_1 will come out.

Dibit Input 1		Digital Form	Dibit Input 2		Digital Form	Dibit Input 3		Digital Form	Dibit Difference Out		Digital Form	Dibit Borrow Output		Digital Form
A’	**A”**		**B’**	**B”**		**C’**	**C”**		**Y1’**	**Y1”**		**Y2’**	**Y2”**	
ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0
ν_1	ν_2	0	ν_1	ν_2	0	ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1
ν_1	ν_2	0	ν_2	ν_1	1	ν_1	ν_2	0	ν_2	ν_1	1	ν_2	ν_1	1
ν_1	ν_2	0	ν_2	ν_1	1	ν_2	ν_1	1	ν_1	ν_2	0	ν_2	ν_1	1
ν_2	ν_1	1	ν_1	ν_2	0	ν_1	ν_2	0	ν_2	ν_1	1	ν_1	ν_2	0
ν_2	ν_1	1	ν_1	ν_2	0	ν_2	ν_1	1	ν_1	ν_2	0	ν_1	ν_2	0
ν_2	ν_1	1	ν_2	ν_1	1	ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0
ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1

Table 6.1: Truth table of dibit based all optical frequency encoded full subtractor.

In block 2, the output from ADM_{12} is same as the previous combination and injected to the $RSOA_{18}$ and $RSOA_{14}$ as pump beam but probe beam of $RSOA_{14}$ is already given i.e., the light beam having frequency ν_2 so, the output of the $RSOA_{14}$ will be ν_2 and connected to the $RSOA_{15}$ as pump beam but no probe beam is present of $RSOA_{15}$ in this combination for this reason $RSOA_{15}$ will not work. As in the input ports of block 2 the inputs are changed so the input of ADM_{14} will be the light beam having frequency ν_2 also the ADM_{14} is biased with light beam having frequency ν_2 so the input light beam will drop through circulator C_{14} and feed to the $RSOA_{18}$ as probe beam. Now the output of the $RSOA_{18}$ will be light beam having frequency ν_2 which is connected to the output port <Y1’> and to the ADM_{20} as input, but the ADM_{20} will biased with the light beam having frequency ν_2 so ADM_{20} will drop the input light beam through circulator C_{20} and connected to the $RSOA_{23}$ as pump beam but probe beam of $RSOA_{23}$ is already given which is having frequency ν_1 so the output of $RSOA_{23}$ will be light beam having frequency ν_1 and connected to the output port

<Y1”>. So, the dibit difference output for this combination will be <ν_2>, <ν_1> i.e., in digital logic ‘1’ which satisfies the truth table of full subtractor.

Also, the probe beam of RSOA$_{20}$ is similar as the previous combination i.e., the light beam having frequency ν_2. As the input changed of block 2 so the input of ADM$_{17}$ will be changed and the changed input will be light beam having frequency ν_2, also the ADM$_{17}$ will be biased with light beam having frequency ν_2 so, the input light beam is dropped through circulator C$_{17}$ and feed to the RSOA$_{21}$ as pump beam. Already the probe beam of RSOA$_{21}$ is given i.e., the light beam having frequency ν_1 so, the output of RSOA$_{21}$ will be light beam having frequency ν_1. Now the output of RSOA$_{21}$ is connected to the RSOA$_{20}$ as pump beam so the output of the RSOA$_{20}$ will be light beam having frequency ν_2. As there is no biasing given to the ADM$_{18}$ so the input of ADM$_{18}$ which is the output of RSOA$_{20}$ is travels towards the output port of block 2 OUT_3.

In block 3, the inputs will be light beams having frequency ν_1, ν_2 respectively to the input ports IN_2 and IN_3. So, the pump beam of RSOA$_{25}$ and RSOA$_{26}$ are same as the previous combination which are ν_1, ν_2 respectively. Now the input of ADM$_{22}$ will be the light beam having frequency ν_2 also, the ADM$_{22}$ will be biased with the light beam ν_2 so, the input will drop through circulator C$_{22}$ and feed to the RSOA$_{25}$ as probe beam, so the output of RSOA$_{25}$ will be the light beam having frequency ν_2 which is connected to the input of ADM$_{23}$. ADM$_{23}$ will be biased with the light beam having frequency ν_1 so, ADM$_{23}$ will pass the input light beam and the output of ADM$_{23}$ is connected to the output port Y2’ and input of ADM$_{24}$. Again, ADM$_{24}$ will bias with the light beam having frequency ν_2 so, the input will drop through circulator C$_{24}$ and feed to the RSOA$_{28}$ as pump beam. Already the probe beam of RSOA$_{28}$ is the light beam having frequency ν_1. So, the output of RSOA$_{28}$ will be the light beam having frequency ν_1 and connected to the output port <Y2”>. In block 3, as the dibit borrow output terminal <Y2’> and <Y2”> are the light beam of ν_2 and ν_1 frequencies respectively, they satisfy the truth table of the full subtractor.

Based on the above analytical discussion, we can conclude that the outputs will satisfy the truth table of the all-optical full subtractor in every digital logic combination.

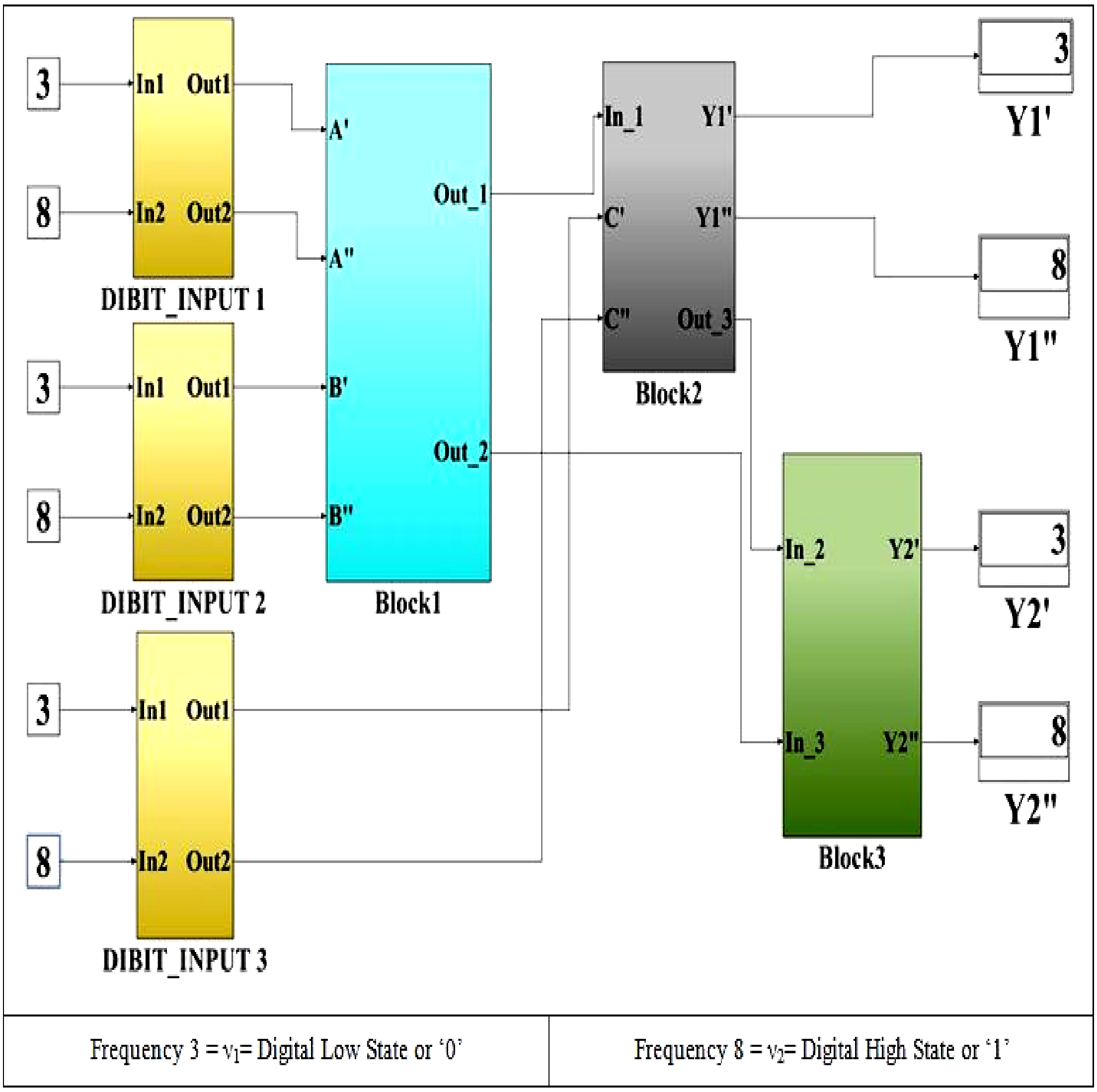


Figure 6.5: Simulative model of dibit based all optical frequency encoded full subtractor for 1st digital logic combination.

6.4 Simulation process of dibit based all optical frequency encoded full subtractor

MATLAB (R2017a) simulation software is used here for simulation of dibit based all optical frequency encoded full subtractor with dibit examine expertness using add drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA) respectively. Here three blocks are used for dibit signal implementation and checking which are DIBIT_INPUT 1, DIBIT_INPUT 2 and DIBIT_INPUT 3 also, the output of the blocks are connected to another blocks BLOCK1 and BLOCK2 respectively, considering two back-to-back bits i.e., 1st bit and 2nd bit respectively. Reflected semiconductor optical amplifier blocks are programmed properly with ‘C’ language for selecting the exact output on the output terminal. In RSOA block there are two input terminals, which are ‘pr’, ‘pm’ respectively and a output terminal ‘y’. The RSOA blocks are designed such that when both inputs, the pump beam and the probe beam, are present, the output will be the probe beam. Consider the pump beam as ‘3 peta Hz’ or, ‘ν_1 frequency’ or, digital low state ‘0’ and the probe beam as ‘8 peta Hz’ or, ‘ν_2 frequency’ or, digital high state ‘1’. Then the output of the RSOA blocks will be ‘8 peta Hz’ or, ‘ν_2 frequency’ or, digital high state ‘1’. If the values of the pump beam and probe beam shuffled with each other then the output will change. The simulative model is illustrated in figure 6.5. Also, the internal blocks of block 1, block 2 and block 3 are exposed in figure 6.6, figure 6.7 and figure 6.8 correspondingly.

Now, Add-drop multiplexer blocks are fabricated in such a way that, if an array of frequencies is applied on the input port of these blocks, then the blocks will drop a specific frequency based on the biasing and allow all other frequencies to pass through. The drop frequency will change respectively if the biasing frequency will change. In these blocks, for a distinct frequency at ‘bias’ port will drop one frequency arriving from ‘input’ port to ‘drop’ port and passes other frequencies to ‘out’ port. Consider, the frequency ‘8 peta Hz’ = ν_2 = digital high state ‘1’ and frequency ‘3’ peta Hz = ν_1= digital low state ‘0’ are present at ‘input’ and ‘bias’ terminal respectively, then the output of the ADM block is ‘8’ peta Hz = ν_2 = digital high state ‘1’. Now, by connecting these two blocks as per block diagram to fabricate the dibit based all optical frequency encoded full subtractor.

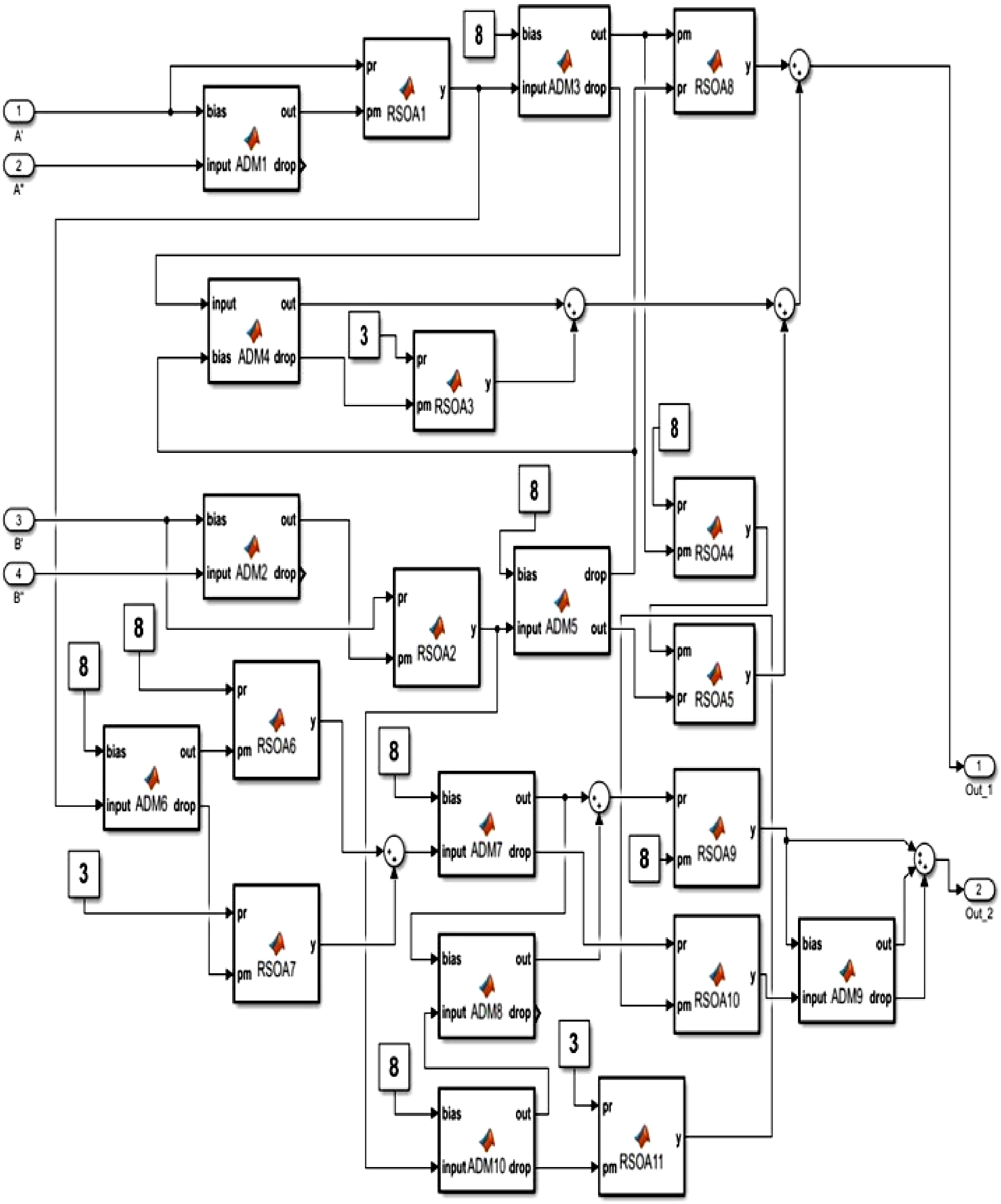
If firstly digital low state or ‘0’ as <3><8> and <8><3> as digital high state or ‘1’ are enforced on the three dibit input terminals then the outputs will be <3><8> or digital low state or ‘0’ in both the output ports shown in figure 6.5.

Secondly, if digital low state or ‘0’ as <3><8> and <8><3> as digital high state or ‘1’ are enforced on two dibit input terminals and digital high state or ‘1’ as <8><3> and <3><8> as digital low state or ‘0’ on the third dibit input ports then the output will be <8><3> or digital high state or ‘1’ in both the output ports and so on.

Finally, if digital high state or ‘1’ as <8><3> is applied in the all-input ports then the output will be digital high state or ‘1’ as <8><3> in both the dibit output ports. Ultimately, the truth table of dibit based all optical frequency encoded full subtractor which is shown in table 6.1, will ensure with this simulative model.

6.5 Results and discussion

The results, which are coming out from simulation action are relevant to full subtractor and the results satisfies the truth table of full subtractor which is shown in table 6.1. For the 1st and 2nd digital logic combination, (say <3><8> = digital low state = ν_1= ‘0’in the three input terminals along with <3><8> = digital low state = ν_1= ‘0’in the two input terminals and in the third input terminal <8><3> = digital high state = ν_2 = ‘1’ respectively) the inputs and the outputs of the simulink model is shown in figure 6.5 and figure 6.9 subsequently.



Frequency 3 = ν_1= Digital Low State or '0'

pr = Probe beam

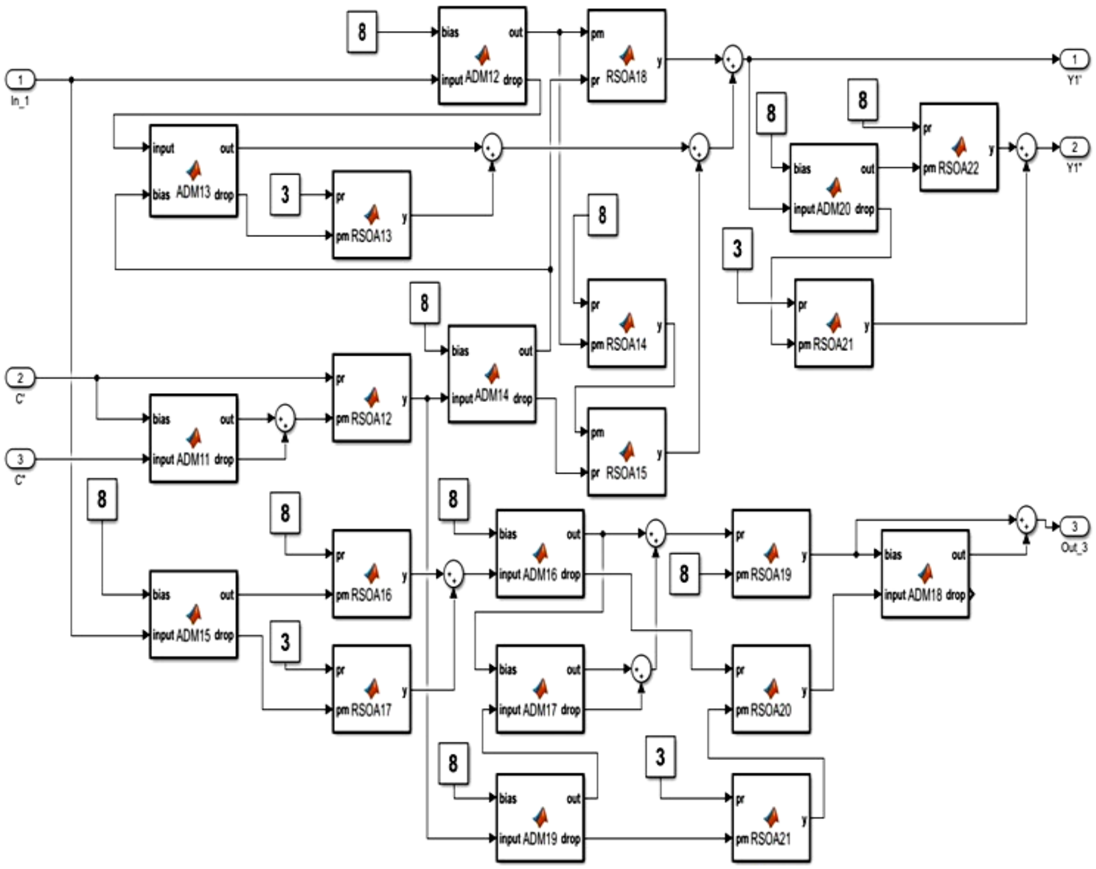
pm = Pump beam

Frequency 8 = ν_2= Digital High State or '1'

ADM = Add/drop Multiplexer

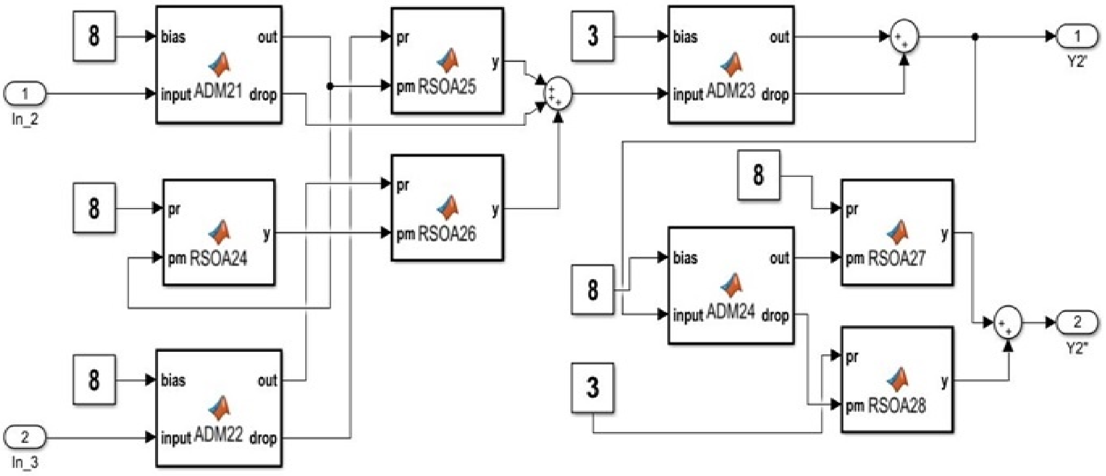
RSOA = Reflected Semiconductor Optical Amplifier

Figure 6.6: Internal simulative model of block 1.



Frequency 3 = ν_1 = Digital Low State or '0'
Frequency 8 = ν_2 = Digital High State or '1'
pr = Probe beam
ADM = Add/drop Multiplexer
pm = Pump beam
RSOA = Reflected Semiconductor Optical Amplifier

Figure 6.7: Internal simulative model of block 2.



Frequency 3 = ν_1 = Digital Low State or '0'
Frequency 8 = ν_2 = Digital High State or '1'
pr = Probe beam
ADM = Add/drop Multiplexer
pm = Pump beam
RSOA = Reflected Semiconductor Optical Amplifier

Figure 6.8: Internal simulative model of block 3.

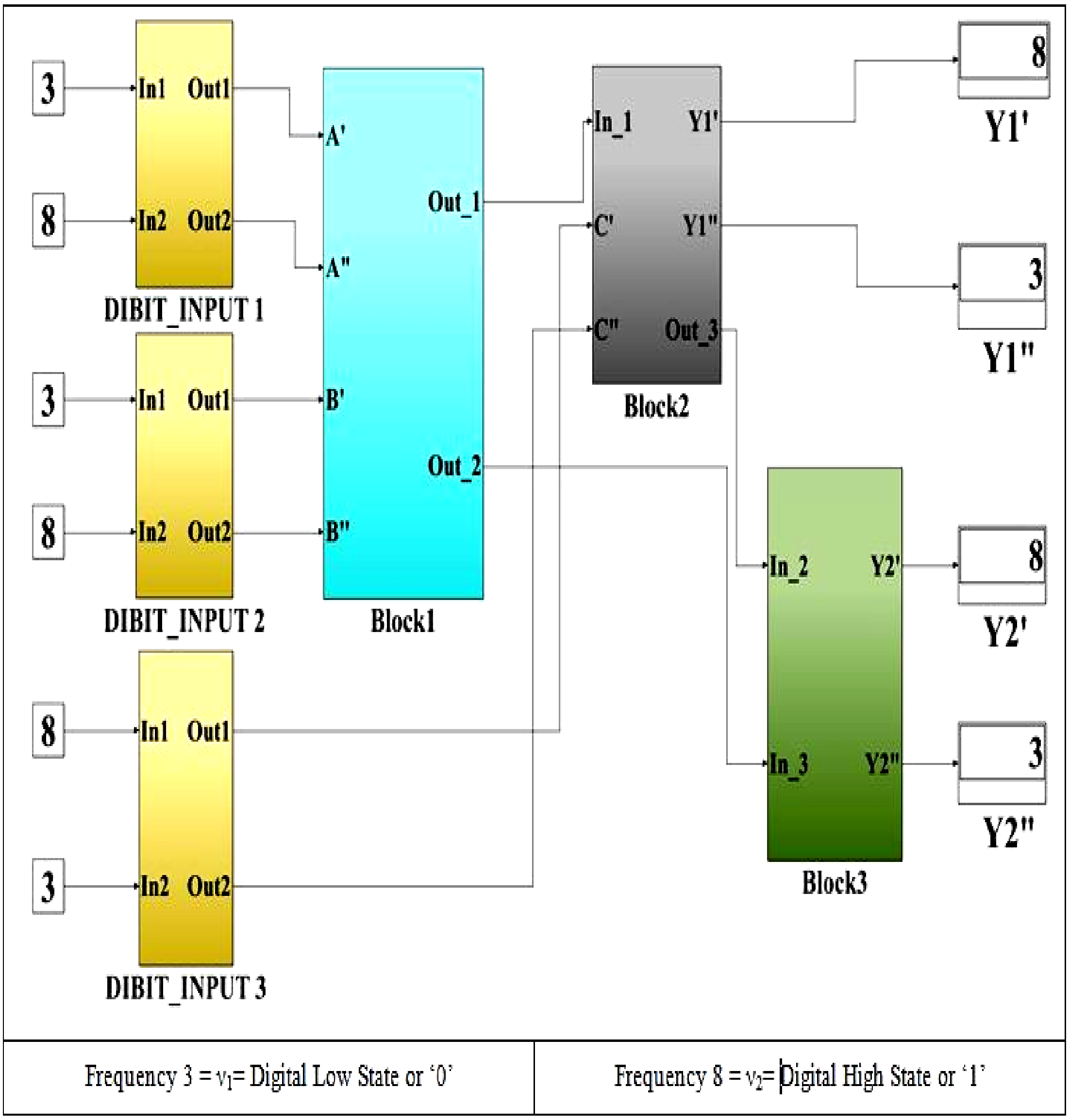


Figure 6.9: The simulink model of dibit based all optical frequency encoded full subtractor for 2nd digital logic combination.

Also, the graphical outputs of the simulated results for various input combinations are shown collectively in figure 6.10. The '1st Dibit Input', '2nd Dibit Input', 'Dibit Borrow Input', 'Dibit Difference Output', and 'Dibit Borrow Output' are graphically depicted to represent the digital states according to the truth table in table 6.1. Thus, this is clear that the simulink model will working properly and providing the desired outputs which are properly satisfy the truth table of full subtractor.

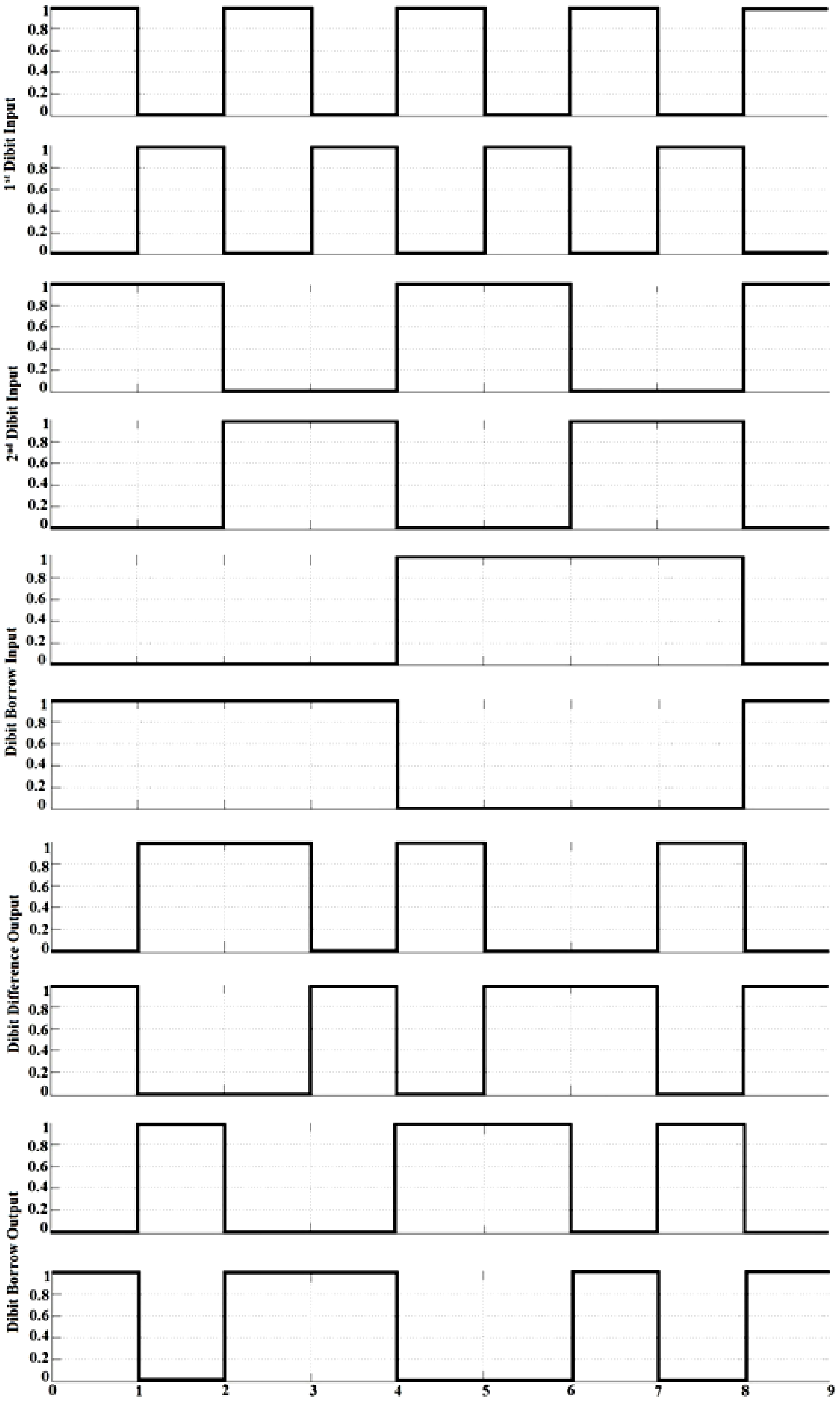


Figure 6.10: Graphical output of the simulated result.

6.6 Conclusions

The superiority of frequency encoding technique and dibit depiction processes are described here to understand the all optical operations. This process is reliable and efficient, effectively eliminating bit errors by achieving a high signal-to-noise ratio. The dibit checking capability reduces incorrect dibit input states. Implementing this process can result in a high degree of accuracy and significantly increased operational speed. The frequency encoding technique may provide honest and decent result also helps for arranging the all optical logical applications. Using optical switches, the design of all optical dibit based frequency encoded full subtractor and the simulated authentication may be used for developing all optical computers. Again this dibit based all optical full subtractor may be sued as comparator. Finally, it concludes that this all optical full subtractor can operate with drastic speed, high accuracy in real time operation.

References

[6.1]. S. Mukhopadhyay, “Role of optics in super-fast information processing.” Indian J. Phys. 84(8), 1069-1074 (2010).

[6.2]. A. K. Ghosh, A. Bhattacharya, M. Raul, A. Basuray, “Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic.” Optics & Laser Technology, 44(5), 1583-1592 (2012).

[6.3]. P. P. Sarkar, S. Mukhopadhyay, “All optical frequency encoded NAND logic operation along with the simulated result.” J. Opt. 43(3), 177-182 (2014).

[6.4]. B. Ghosh, S. Mukhopadhyay, “A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device.” Optik-International Journal for Light and Electron Optics, 124(21), 4813-4815 (2013).

[6.5]. P. P. Sarkar, B. Ghosh, S. N. Patra, S. Mukhopadhyay, “A new scheme of an all optical frequency encoded dibit based latch with its simulated result.” J. Opt. Technol. 84(9), 631-634 (2017).

[6.6]. P. P. Sarkar, B. Satpati, S. Mukhopadhyay, “New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors.” J. Opt. 42(4), 360-366 (2013).

[6.7]. V. Cakmak, F. Ufuk, N. Karabulut, “Diffusion-weighted MRI of pulmonary lesions: Comparison of apparent diffusion coefficient and lesion-to-spinal cord signal intensity ratio in lesion characterization.” Journal of Magnetic Resonance Imaging, 45(3), 845-854 (2017).

[6.8]. G. Hu, D. Xiao, Y. Wang, T. Xiang, Q. Zhou, “Securing image information using double random phase encoding and parallel compressive sensing with updated sampling processes.” Optics and Lasers in Engineering, 98, 123-133 (2017).

[6.9]. J. Zhu, P. Zhou, X. Su, Z. You, “Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination.” Optics express, 24(25), 28549-28560 (2016).

[6.10]. C. Taraphdar, T. Chattopadhyay, J. N. Roy, “Polarization encoded all-optical ternary Max gate.” 4th International Conference on Computers and Devices for Communication, Kolkata, India, December, 1-4 (2009).

[6.11]. B. Ghosh, S. Biswas, S. Mukhopadhyay, “A novel method of all-optical wavelength encoded logic and inhibitor operations with dibit representation technique." Optik-International Journal for Light and Electron Optics, 126, 483-489 (2015).

[6.12]. P. P. Sarkar, S. Hazra, B. Ghosh, S. N. Patra, S. Mukhopadhyay, "Realization of all-optical frequency-encoded dibit-based OR and NOR logic gates with simulated verification." Guha, D. (Ed.), Chakraborty, B. (Ed.), Dutta, H. (Ed.), Computer, Communication and Electrical Technology, CRC Press, 1st edn. 153-158 (2017).

[6.13]. S. Mukhopadhyay, "Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems." Applied optics, 31 (23), 4622-4623 (1992).

[6.14]. I. S. Amiri, S. E. Alavi, M. Bahadoran, A. Afroozeh, H. Ahmad, "Nanometer bandwidth soliton generation and experimental transmission within nonlinear fiber optics using an add-drop filter system." Journal of Computational and Theoretical Nanoscience, 12(2), 221-225 (2015).

[6.15]. S. Chen, Y. Shi, S. He, D. Dai, "Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon." IEEE Photonics Technology Letters, 28 (17), 1874 -1877 (2016).

[6.16]. J. Wang, L. R. Chen, "Low crosstalk Bragg grating/Mach-Zehnder interferometer optical add-drop multiplexer in silicon photonics." Optics express, 23(20), 26450-26459 (2015).

[6.17]. P. P. Sarkar, B. Ghosh, S. N. Patra, "Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer." J. Opt. Technol. 83(4), 257-262 (2016).

[6.18]. B.Ghosh, et al. “A Novel Approach to Realize of All Optical Frequency Encoded Dibit Based XOR and XNOR Logic Gates Using Optical Switches with Simulated Verification.” Optics and Spectroscopy, 124(3), 337-342 (2018).

[6.19]. S. Saha, S. Biswas, S. Mukhopadhyay, “Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach–Zehnder interferometer-based semiconductor optical amplifier.” IET Optoelectronics, 11(5), 201-207 (2017).

[6.20]. S. Singh, et al. “Photonic processing of all-optical Johnson counter using semiconductor optical amplifiers.” IET Optoelectronics, 11(1), 8-14 (2016).

[6.21]. D. K. Gayen, T. Chattopadhyay, K. E. Zoiros, “All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach–Zehnder interferometer.” Journal of Computational Electronics, 14(1), 129-138 (2015).

[6.22]. Q. Cheng, et al. “Demonstration of the feasibility of large-port-count optical switching using a hybrid Mach–Zehnder interferometer–semiconductor optical amplifier switch module in a recirculating loop.” Optics letters, 39(18), 5244-5247 (2014).

[6.23]. K. Maji, K. Mukherjee, A. Raja, “An alternative method for implementation of frequency-encoded logic gates using a terahertz optical asymmetric demultiplexer (TOAD).” Journal of computational electronics, 18(4), 1423-1434 (2019).

[6.24]. M. Mandal, S. Mukhopadhyay, “Photonic scheme for implementing quantum square root controlled Z gate using phase and intensity encoding of light.” IET optoelectronics, 15(1), 52-60 (2021).

[6.25]. K. Mukherjee, et al. “All-optical soliton based universal logic NOR utilizing a single reflective semiconductor optical amplifier (RSOA).” Photonic Network Communications, 43(2), 101-108 (2022).

[6.26]. K. Mallick, et al. “Bidirectional OFDM-MMWOF transport system based on mixed QAM modulation format using dual mode colorless laser diode and RSOA for next generation 5-G based network.” Optical Fiber Technology, 64, 102562 (2021).

[6.27]. A. S. Das, A.S. Patra, “Bidirectional transmission of 10 Gbit/s using RSOA based WDM-PON and optical carrier suppression scheme.” Journal of Optical Communications, 35(3), 239-243 (2014).

[6.28]. K. Mallick, et al. “Bidirectional hybrid OFDM based Wireless-over-fiber transport system using reflective semiconductor amplifier and polarization multiplexing technique.” AEU-International Journal of Electronics and Communications, 96, 260-266 (2018).

[6.29]. G. C. Mandal, et al. “A full-duplex WDM hybrid fiber-wired/fiber-wireless/fiber-VLC/fiber-IVLC transmission system based on a self-injection locked quantum dash laser and a RSOA.” Optics Communications, 427, 202-208 (2018).

[6.30]. G. C. Mandal, et al. “Next-generation bidirectional triple-play services using RSOA based WDM radio on free-space optics PON.” Optics Communications, 411, 138-142 (2018).

[6.31]. G. C. Mandal, et al. “Bidirectional and simultaneous transmission of baseband and wireless signals over RSOA based WDM /radio-over-fiber passive optical network using incoherent light injection technique.” AEU-International Journal of Electronics and Communications, 80, 193-198 (2017).

[6.32]. A. S. Das, A.S. Patra, “RSOA-based full-duplex WDM-PON for 20 Gbps transmission in two channels over a long-haul SMF using external modulation scheme.” Journal of Optical Communications, 36(3), 231-235 (2015).

[6.33]. J. K. Rakshit, J. N. Roy, "All-optical ultrafast switching in a silicon microring resonator and its application to design multiplexer/demultiplexer, adder/subtractor and comparator circuit." Optica Applicata, 46(4), 517-539 (2016).

[6.34]. J. K. Rakshit, J. N. Roy, "Design of all-optical universal shift register using nonlinear microring resonators." Journal of Computational Electronics, 15, 1450-1461 (2016).

[6.35]. D. Nath, et al. "Photocurrent generation under forward bias with interfacial tunneling of carrier at pentacene/F16CuPc heterojunction photodetector." Journal of Alloys and Compounds, 815, 152401 (2020).

[6.36]. J. K. Rakshit, J. N. Roy, "Silicon micro-ring resonator-based all-optical digital-to-analog converter." Photonic Network Communications, 34(1), 84-92 (2017).

Chapter 7

Overall conclusions and directions for future research.

Abstract

Optics has played a significant role in logic and data processing for several decades. The fields of optical computation and communication continue to advance, showing promising growth. Despite numerous research proposals and advancements already reported, there remain many opportunities to fully harness the advantages of optics. This chapter provides a comprehensive conclusion of the entire thesis and explores the potential directions for future research.

7.1 Introduction

The use of optical signals in logic and data processing began in the mid-1970s. Since then, optics has emerged as a promising candidate in the fields of optical computing and optical communications. The study of optical computing spans multidisciplinary areas across both science and technology. Scientists and researchers worldwide are continuously working to integrate optics into computing, leading to rapid growth in the implementation of various optical systems. This progress has been facilitated by the introduction of different techniques and optical materials, expanding the field's applications significantly.

In optical parallel computation, optical switches play a crucial role, with optical nonlinear material based switches being used in many systems. All optical logic gates are the fundamental building blocks of any optical digital logic circuit. Previous chapters have discussed new approaches using frequency encoding methods for all optical normal and dibit based logic and arithmetic units. These schemes offer very high operational speeds, controlled input-output for reducing bit error and can be fabricated in compact volumes as integrated in nature. For this reason, it makes them highly promising for future superfast processing applications.

7.2 Overall conclusions of the thesis

The continuous demand for higher computational speeds drives ongoing research for efficient optical systems. Optical logic gates and memory units are fundamental components of these optical processors and systems. In this thesis, I have explored dibit based all optical logic gates, combinational digital circuits, integrated approaches and arithmetic circuits. Conclusions for each specific scheme are provided in their respective chapters. These all optical schemes can potentially offer real time operational speeds. The frequency encoding and decoding technique, which has several advantages, has been utilized in the development of the aforementioned all optical logic units.

In chapter 1 of this thesis, a brief history of optical computation, communication systems and photonics and its applications are discussed, along with the current status in these fields. This chapter outlines the advantages and disadvantages of optics and details the principles of the frequency encoding technique, highlighting its benefits over other encoding methods. Additionally, the basics of the dibit representation technique are briefly explained. The fundamental operation of the semiconductor optical amplifier (SOA) is thoroughly examined. The chapter also covers the basics of simulated performance studies of SOA based optical switches for optical data processing.

In chapter 2, the authors have detailed an all optical dibit representation technique, which offers the advantages of high speed operation and reduced bit error rates. Expanding on this concept, all optical frequency encoded dibit based XOR and XNOR logic gates are proposed, utilizing optical components like add/drop multiplexers (ADM) and reflected semiconductor optical amplifiers (RSOA). The operation of these gates has been verified through accurate simulations conducted using MATLAB simulation software version R2008a.

In chapter 3, combinational optical logic circuit, specifically a multiplexer, based on all optical frequency encoded dibit representation using ADM and RSOA optical switches is elaborated upon, including simulated experiments.

Similarly, in chapter 4, the operation of an all optical frequency encoded dibit based de-multiplexer is discussed, employing the same optical switches with appropriate simulations. These schemes are useful for various combinational optical circuit designs.

In chapter 5, the advantages of the dibit based system, including proper dibit input checking units and integrated logic gates, are presented. This chapter discusses the implementation of all optical AND-OR/NAND-NOR logic gates with control inputs using the dibit based technique, along with their respective simulation processes. In the realm of optical computation, simulation verification is crucial for implementing various schemes of all optical integrated logic and arithmetic circuits.

In chapter 6, the design development of an all optical dibit based frequency encoded full subtractor is presented, along with its simulated validation, which could be utilized for developing all optical computers. Additionally, this dibit based all optical full subtractor can function as a comparator. This chapter concludes that this all optical full subtractor can operate with exceptional speed and high accuracy in real-time operations.

Finally, chapter 7 presents the general conclusions drawn from the research and outlines the potential future directions for further development. It summarizes the key findings, emphasizing the advantages and implications of the all optical dibit based techniques and their applications. Additionally, the chapter discusses potential improvements, unexplored areas, and new possibilities for expanding the scope of this work, providing a comprehensive overview of how these advancements can impact the field of optical computing and beyond.

7.3 Future scope of research

Since the end of the 21st century, numerous research works have been reported on using optical signals for data computing. This thesis simulates various all optical approaches for implementing different optical systems. While we have reached our initial targets, much work remains for future investigations.

1. There are possibilities to physically and experimentally implement all proposed works in the laboratory.

2. Many other combinational building blocks yet to be proposed can be implemented in future works.

3. Sequential logic units can be developed.

4. Different types of frequency encoded all optical tri-state and quaternary logic processors, nano-photonic processors, and high-end memory units may be implemented in future works. Therefore, I believe there is significant scope remaining for my future research.

The simulative verification mentioned involves testing and validating logic systems with control inputs using simulation techniques. These schemes are essential components in digital circuitry, and their proper functioning is critical for constructing more complex arithmetic and logic devices. By confirming that these systems work correctly in simulations, engineers can use them as foundational elements to develop and verify the performance of other digital devices. This approach is especially useful in frequency encoding principles, where information is encoded in the frequency of signals.

In optical computation, simulative verification is crucial for implementing various schemes of all optical integrated logic and arithmetic circuits. Optical computing uses light signals instead of traditional electronic signals, offering faster processing speeds and potentially lower energy consumption. Simulating and verifying these optical logic and arithmetic circuits is foundational for building advanced optical computers. Engineers foresee a future where multiple all optical digital devices and circuits can be combined to create sophisticated optical computers capable of efficiently handling complex computations. Therefore, accurately simulating and verifying basic components like logic gates are essential steps toward realizing these advanced optical computing systems.

Integrated dibit based optical digital circuits represent a significant advancement in the field of photonics and optical computing. Here are some potential future scopes and applications for this technology:

1. High speed data transmission

I. Telecommunications: Dibit based circuits can enhance the speed and efficiency of data transmission in optical fiber networks, supporting the growing demand for bandwidth.

II. Data centers: They can improve the performance of data centers by providing faster data processing and transmission capabilities.

2. Optical computing

I. High performance computing: Integrated optical circuits can significantly increase the speed of computation by leveraging the properties of light, such as parallelism and high frequency operation.

II. Quantum computing: They can be used in the development of quantum computing systems, which rely on optical components for qubit manipulation and information processing.

3. Energy efficiency

I. Reduced power consumption: Optical circuits typically consume less power compared to electronic circuits, making them ideal for applications where energy efficiency is crucial.

II. Green technology: They can contribute to the development of environmentally friendly technologies by reducing the carbon footprint of computing and data transmission.

4. Miniaturization and integration

I. Compact designs: Dibit based optical circuits can be integrated into smaller, more compact devices, supporting the trend towards miniaturization in electronics and photonics.

II. Integration with existing technologies: These circuits can be integrated with existing silicon based technologies, allowing for hybrid systems that leverage both electronic and optical components.

5. Improved signal processing

I. Higher bandwidth: Optical circuits can handle higher bandwidths, enabling faster and more efficient signal processing.

II. Reduced interference: Optical signals are less susceptible to electromagnetic interference, improving the reliability and quality of signal processing.

6. Emerging applications

I. 5G and beyond: The technology can support the high data rates and low latency requirements of next generation wireless communication systems.

II. Internet of things (IoT): Optical circuits can enhance the connectivity and performance of IoT devices by providing high speed, reliable communication links.

III. Artificial intelligence (AI): They can be used in AI hardware accelerators, improving the speed and efficiency of AI algorithms.

7. Research and development

I. Advanced materials: Research into new materials and fabrication techniques can further enhance the performance and capabilities of dibit based optical circuits.

II. New architectures: Developing new circuit architectures and designs can optimize the performance and expand the range of applications for these circuits.

8. Healthcare and bio-photonics

I. Medical imaging: Optical circuits can improve the resolution and speed of medical imaging techniques, such as optical coherence tomography (OCT).

II. Bio-sensing: They can be used in advanced biosensors for early detection and monitoring of diseases.

In summary, the future scope of integrated dibit based optical digital circuits is vast, with potential applications in telecommunications, signal processing, computing, healthcare and beyond with energy efficient way. Continued research and development in the field of photonics and optical computing can unlock new possibilities of technological enhancement and drive hi-tech advancements across various industries in near future.

7.4 Challenges and considerations in optical computing

Optical computing, which uses light instead of electrical signals to perform computations, presents a promising alternative to traditional electronic computing due to its potential for higher speed and lower power consumption.

However, it also faces several limitations and challenges, especially when it comes to implementing real-time applications.

1. Material limitations

I. Availability and cost: The materials required for efficient optical computing, such as photonic crystals and nonlinear optical materials, can be expensive and difficult to source.

II. Performance: The optical properties of materials can vary, affecting the performance and reliability of optical components.

2. Integration with existing technologies

I. Compatibility: Integrating optical components with existing electronic systems can be challenging due to differences in signal processing and transmission methods.

II. Interfacing: Effective interfaces between optical and electronic components are required to ensure seamless communication and data transfer.

3. Fabrication challenges

I. Precision: Manufacturing optical components with the precision required for high speed computation is complex and requires advanced techniques.

II. Scalability: Scaling up production while maintaining quality and performance is a significant hurdle.

4. Heat management

I. Thermal effects: Optical components can generate heat, which needs to be managed to maintain performance and prevent damage.

II. Cooling solutions: Effective cooling solutions must be developed to handle the heat produced by densely packed optical circuits.

5. Signal loss and noise

I. Attenuation: Optical signals can weaken as they travel through a medium, leading to potential data loss.

II. Noise: External factors can introduce noise into optical systems, affecting signal clarity and accuracy.

6. Design complexity

I. Circuit design: Designing complex optical circuits requires advanced knowledge and sophisticated design tools.

II. Algorithm development: Developing algorithms that can efficiently utilize the capabilities of optical computing requires a deep understanding of both optics and computation.

7. Standardization

I. Lack of standards: The field of optical computing lacks widely accepted standards, making it difficult to ensure compatibility and interoperability between different systems and components.

8. Economic and market factors

I. Investment: Significant investment is needed to develop and commercialize optical computing technologies.

II. Market adoption: Convincing industries to adopt optical computing over established electronic systems can be challenging.

9. Environmental considerations

I. Sustainability: The environmental impact of producing and disposing of optical materials needs to be considered.

II. Energy consumption: While optical computing has the potential to reduce energy consumption, the overall environmental benefits depend on the entire lifecycle of the technology.

Addressing these challenges requires multidisciplinary collaboration among researchers, engineers, and industry stakeholders to advance the development and implementation of optical computing systems.

Appendices

Table A.1: SI prefixes

Factor	Name	Symbol		Factor	Name	Symbol
10^{24}	yotta	Y		10^{-1}	deci	d
10^{21}	zetta	Z		10^{-2}	centi	c
10^{18}	exa	E		10^{-3}	milli	m
10^{15}	peta	P		10^{-6}	micro	µ
10^{12}	tera	T		10^{-9}	nano	n
10^{9}	giga	G		10^{-12}	pico	p
10^{6}	mega	M		10^{-15}	femto	f
10^{3}	kilo	k		10^{-18}	atto	a
10^{2}	hecto	h		10^{-21}	zepto	z
10^{1}	deka	da		10^{-24}	yocto	y

Table A.2: Greek Alphabet

Letter	Name		Letter	Name
Α α	Alpha		Ν ν	Nu
Β β	Beta		Ξ ξ	Xi
Γ γ	Gamma		Ο ο	Omicron
Δ δ	Delta		Π π	Pi
Ε ε	Epsilon		Ρ ρ	Rho
Ζ ζ	Zeta		Σ σ/ς	Sigma
Η η	Eta		Τ τ	Tau
Θ θ	Theta		Υ υ	Upsilon
Ι ι	Iota		Φ ϕ	Phi
Κ κ	Kappa		Χ χ	Chi
Λ λ	Lambda		Ψ ψ	Psi
Μ μ	Mu		Ω ω	Omega

List of Acronyms

ADM	**Add/drop multiplexer**
AR	**Anti-reflected**
BER	**Bit error ratio**
DFM	**Distributed feedback**
FWM	**Four wave mixing**
MQW	**Multiple quantum wells**
NLM	**Non-linear material**
PBS	**Polarization beam splitters**
RSOA	**Reflected semiconductor optical amplifier**
SOA	**Semiconductor optical amplifier**
SPM	**Self-phase modulation**
TE	**Transverse electric field**
TM	**Transverse magnetic field**
WDM	**Wavelength-division multiplexed**
XGM	**Cross gain modulation**
XPM	**Cross phase modulation**

My published journals related to thesis work.

J Opt
https://doi.org/10.1007/s12596-023-01237-3

RESEARCH ARTICLE

Design of dibit-based all-optical frequency encoded controlled full subtractor using optical switches

Bitan Ghosh[1] · **Debojyoti Batabyal**[1] · **Priyanka Biswas**[2] · **Niladri Halder**[1] ·
Dibyendu Roy[1] · **Partha Pratim Sarkar**[1] · **Ardhendu Ghoshal**[3]

Received: 28 February 2023 / Accepted: 19 May 2023

Abstract Nowadays, data is one of the most valuable and demanding items for the human world. On the other hand, the data communication speed is also a concern of modern technology. As light is the fastest element for transmission, the photonic communication is one of the major stakes which already has been proved. Using this technology, the design of all-optical digital logic gates and other different devices has already been proposed. In this manuscript, the authors have proposed an all-optical frequency encoded dibit-based digital controlled full subtractor using reflected semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM). The proposed dibit-based system may provide better performance compared to other conventional electronic circuits as well as the signal-to-noise ratio is also low here. As this proposed all-optical full subtractor is controlled dibit-based digital circuit, it does not allow any unnecessary input to the circuit. For this reason, the device may operate with better security. This all-optical device's operation is also verified using MATLAB R2017(a) simulation software.

Keywords Frequency encoding principle · Dibit representation technique · Dibit logic state · Reflected semiconductor optical amplifier · Add/drop multiplexer · Simulink

Introduction

In last few decades, speed-related problems are happening in the field of information processing, communication, etc. To overcome such problems, photon can be used for superfast information processing element. There are many types of encoding techniques for designing the all-optical logical or arithmetic devices [1, 2]. The different kind of encoding techniques are there like frequency encoding [3–6], phase encoding [7], intensity encoding [8], spatial encoding [9], polarization encoding [10] etc.

The most compatible technique is the frequency encoding technique among the other encoding techniques because the frequency of light beam remains constant and uninfluenced after reflection, refraction, absorption etc. At the data computation and encoding process, two different states can be represented by two different frequencies in frequency encoding technique. One specific value of frequency is considered as digital high state or '1', and another frequency is considered as digital low state or '0'. Following this logic, optical light beam having frequency 'ν_1' is treated as digital low state or '0', and similarly, optical light beam having frequency 'ν_2' is treated as digital high state or '1'.

Again, digital logic state can be expressed by two successive bit positions, in the dibit representation technique [11–13]. So the digital low state or '0' is expressed as dibit logic state (0)(1), and the digital high state or '1' is expressed as dibit logic state (1)(0) subsequently. These two states can be permitted to express by the two different frequencies. That claims the existence of two frequencies side by side $(\nu_1)(\nu_2)$ expressed the digital low state or '0' and $(\nu_2)(\nu_1)$ does the same for digital logic high or '1'. This process in optics for logical operation was first proposed by S. Mukhopadhyay et al. Subtractor performs the subtraction operation in between any two numbers. Subtractor is used on

✉ Partha Pratim Sarkar
pratim34@gmail.com

[1] Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan, India

[2] Department of Physics, University of Burdwan, Burdwan, India

[3] Department of Instrumentation and Electronics Engineering, Jadavpur University, Kolkata, India

digital systems for logical and arithmetical operation. Now, the authors have proposed all-optical frequency encoded half subtractor-based full subtractor using optical switches, add/drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA). Also, this circuit is designed with suitable dibit checking capability.

Previously, dibit-based digital logic gates have been used in few papers, for various journals. But in this paper, a new idea of construction regarding dibit-based frequency encoded all-optical half subtractor-based full subtractor has been proposed with a dibit checking facility, which will oppose the incorrect inputs to the dibit-based logic gates. The inputs like dibit logic states (0)(0) and (1)(1) will consider as wrong input, so the dibit verifying block will counter those wrong inputs to enter. This feature will give support the reliability of the logic gates.

Add drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA)

Add drop multiplexer [14–16] is a frequency selective optical switching device. It has four ports, input biasing, output and drop. The output and drop operation of this device depend on the biasing given on the device; if a particular biasing is given on the device, then the device reflects the particular light beam having the same frequency with the biasing and the another one passes through the device. Similarly, when the biasing changes, the alternate operation happens, and it shown in Fig. 1a.

Also, if no biasing is given to this device, then the device does not work. Another optical switching device is reflected semiconductor optical amplifier (RSOA) [17–21]. It has basically three ports, two input ports and one output port. In two input ports there, one is probe beam, and another one is pump beam. Basically, the probe beam is weak, and the probe beam is strong, when power is concerned. If two light wave having different frequencies (say ν_2, ν_1) given to the input ports of the device, then the device will provide output having the frequency of probe beam and the power of the pump beam, i.e. high power with low frequency. In this way, these two devices may be used to develop different all-optical logical operations [22–25]. Block diagram of reflecting semiconductor optical amplifier [26–36] is shown in Fig. 1b.

Realization of Dibit-Based All-Optical Frequency Encoded full Subtractor

In Fig. 2, the basic block diagram of dibit-based all-optical frequency encoded full subtractor is shown. Here, the all-optical full subtractor is subdivided into three blocks, ‘Block 1’, ‘Block 2’ and ‘Block 3’, respectively. Block 1 has < A’ > , < A’’ > , < B’ > and < B’’ > four input ports for taking two dibit inputs and two output ports < OUT_1 > and < OUT_2 >, respectively. There are three input ports < IN_1 > , < C’ > < C’’ > , also having three output ports in which first and second are < Y1’ > and < Y1″ > for giving the dibit difference output, and the third one is < OUT_3 > in Block 2. The last block, Block 3, has two input ports, < IN_1 > and < IN_2 >, and two output ports < Y2’ > and < Y2″ > for providing dibit borrow output. The internal circuitry of block 1, block 2 and block 3 is shown in Figs. 3, 4 and 5, respectively.

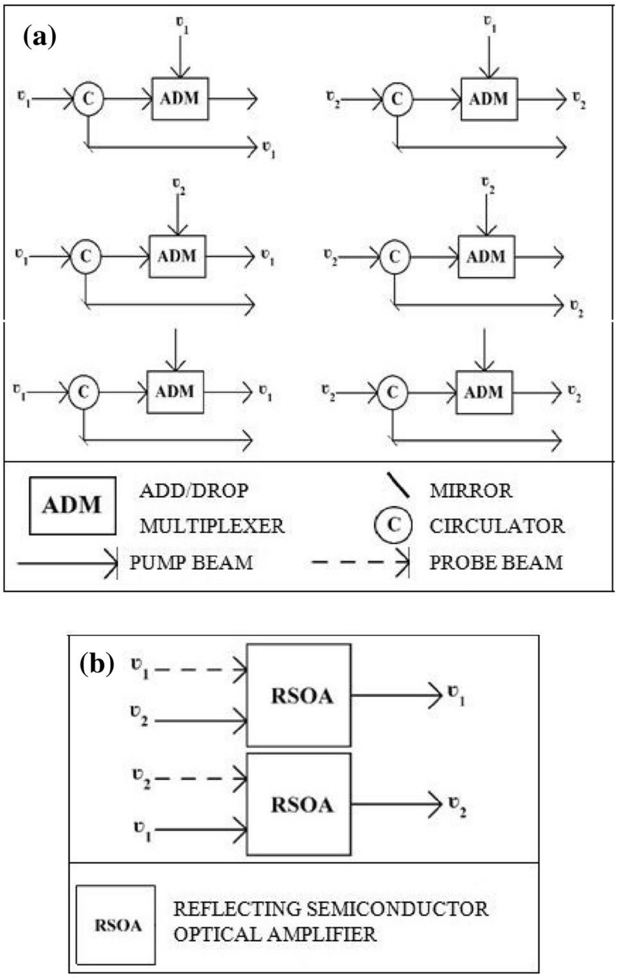


Fig. 1 **a** Basic block diagram of ADM. **b** Basic block diagram of RSOA

At first, light beam of different frequencies (say ν_1 and ν_2) is given to the dibit input ports of block 1 (< A’ > and < A” >), (< B’ > and < B” >) and the dibit input ports of block 2 (< C’ > and < C” >), respectively. As this scheme of all-optical full subtractor circuit has the ability of dibit examine facility at the input side, it will scan the inputs by the ADM$_1$, RSOA$_1$, ADM$_2$, RSOA$_2$, ADM$_{11}$ and RSOA$_{12}$

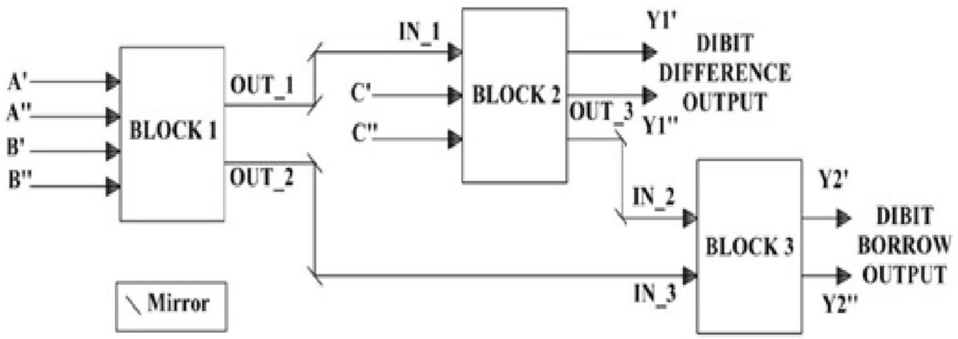


Fig. 2 Basic block diagram of dibit-based all-optical frequency encoded full subtractor

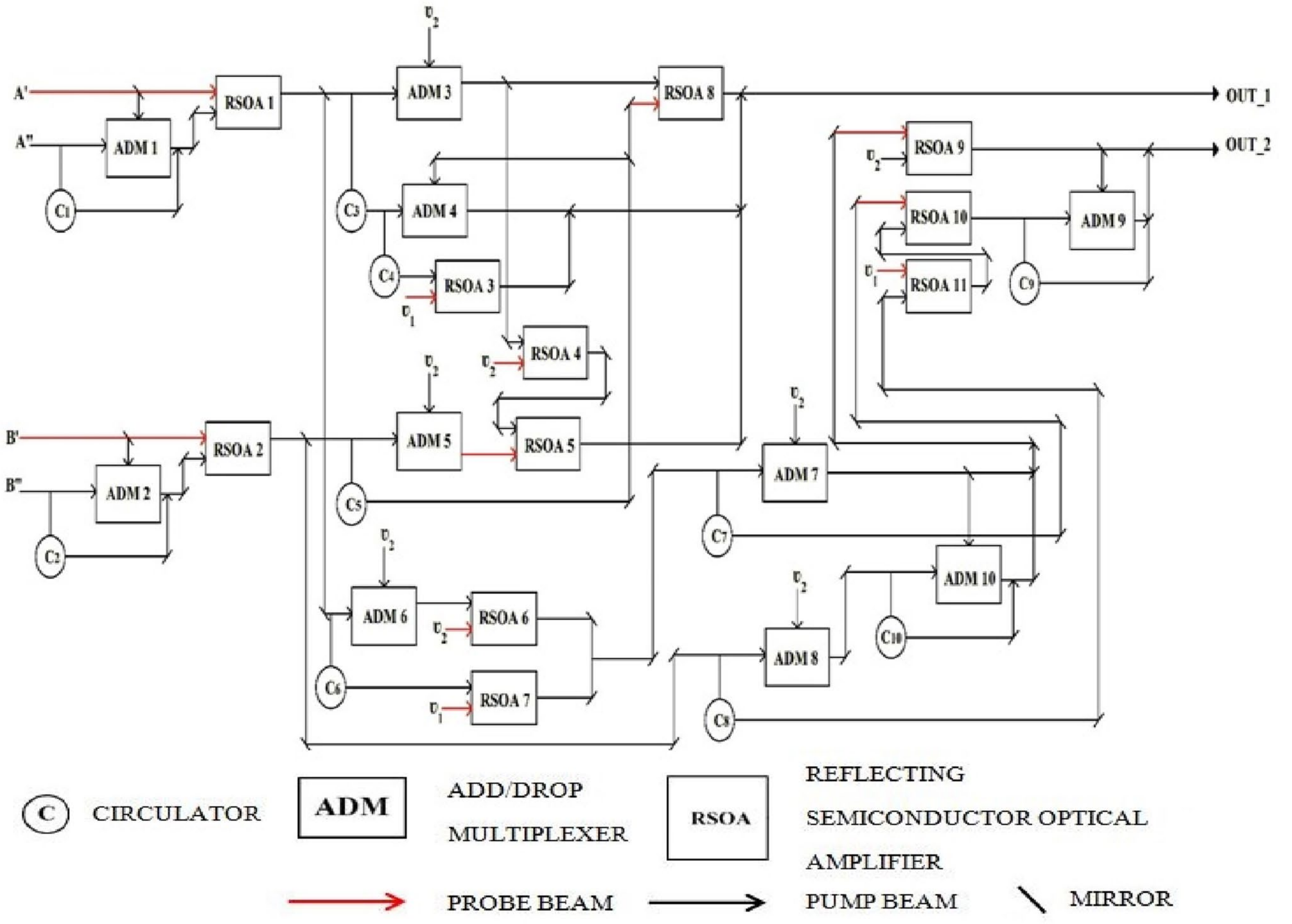


Fig. 3 Internal blocks of block 1

blocks, respectively. Here, light beam having frequency ν_1 is flowing from input port (A'), which is the biasing light beam of ADM$_1$ and also the probe beam of RSOA$_1$. Another one input is ν_2 coming from input port (A'') which is directly feed to the ADM$_1$. As per working principle of ADM, here, ADM$_1$ is biased by the light beam of ν_1 frequency, so it will pass the light beam having frequency of ν_2 and directly feed to the RSOA$_1$ as pump beam. Now, as per working function of RSOA, as the probe beam and pump beam inputs of RSOA$_1$ are the light beam of ν_1 and ν_2 frequencies, respectively, so the output of RSOA$_1$ will be the light beam having frequency ν_1. Similarly, the light beam of ν_1 frequency will also come out from RSOA$_2$ and RSOA$_{12}$, because in the input ports < (B'), (B'') > of block 1 and < (C'), (C'') > of block 2, the inputs are similar as the input ports (A') and (A'') say ($\nu_{1,}$ ν_2).

At this moment, the outputs of RSOA$_1$, RSOA$_2$ and RSOA$_{12}$, i.e. the light beam having frequency 'ν_1' is feed to

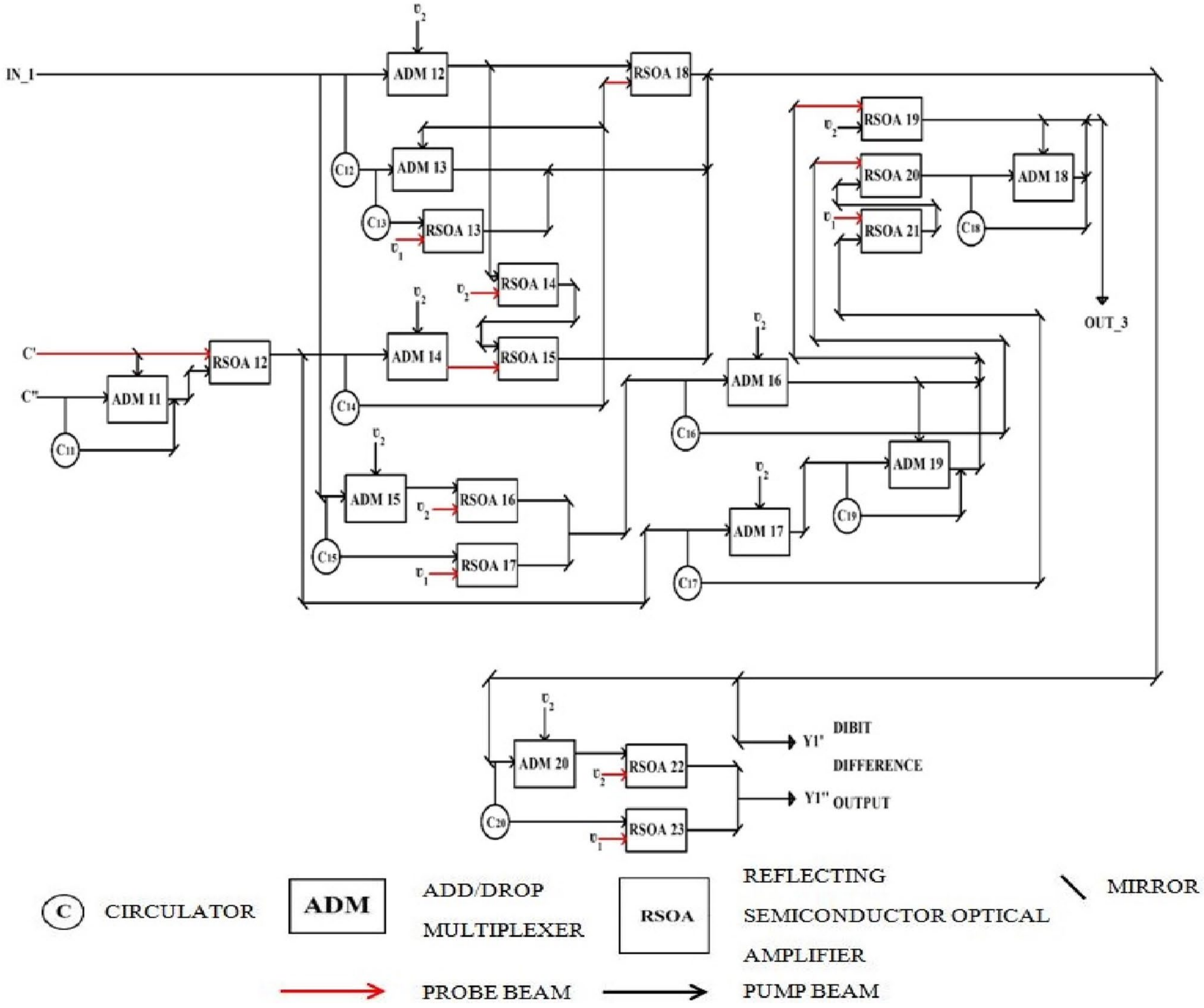


Fig. 4 Internal blocks of block 2

the ADM$_3$, ADM$_5$, ADM$_6$ and ADM$_8$ in block 1 and ADM$_{14}$ and ADM$_{17}$ in block 2. As previously mentioned, the ADM blocks are biased with light beam having frequency ν_2 so the light beam having frequency ν_1 is passed through the ADM blocks. In block 1, further the light beam having frequency ν_1 will feed to RSOA$_4$ as pump beam, in RSOA$_5$ as probe beam, in RSOA$_6$ as pump beam and in RSOA$_8$ as pump beam in block 1. In RSOA$_4$, ν_2 is feed as the probe beam so the RSOA$_4$ give the output of light beam having frequency ν_2, and the output of RSOA$_4$ is feed to the RSOA$_5$ as the pump beam and the probe beam of RSOA$_5$ are ν_1 (previously said), so the output of RSOA$_5$ will be ν_1, and the light beam travels towards the output port OUT_1. As no probe beam is feed to the RSOA$_8$, it will not be in operation. In RSOA$_6$, light beam having frequency ν_2 is feed as probe beam, so the output of the RSOA$_6$ will be light beam having frequency ν_2 and directly injected to the input of ADM$_7$. As ADM$_7$ is biased with light beam having frequency ν_2, ADM$_7$ will drop the input light beam having frequency ν_2 through circulator C$_7$ and directly feed to the RSOA$_{10}$ as probe beam. In this logical combination, RSOA$_{10}$ has no pump beam, so it will not function. In ADM$_{10}$, light beam having frequency ν_1 is feed as input from the output of ADM$_8$ which is previously said; as in ADM$_{10}$, no biasing is given, so it will pass the light beam having frequency ν_1 and feed to the RSOA$_9$ as the probe beam, and also the pump beam is the light beam having frequency ν_2 so the output of RSOA$_9$ will be the light beam having frequency ν_1, which further travels to the output port OUT_2 of block 1. Output port OUT_1 of block 1 is directly connected to input port IN_1 of block 2, so the light beam having frequency ν_1 is feed to the ADM$_{12}$ and ADM$_{15}$ in block 2. As previously mentioned, the ADM blocks are biased with light frequency ν_2; for this reason, the ADM blocks will pass the light beam having frequency ν_1. Like

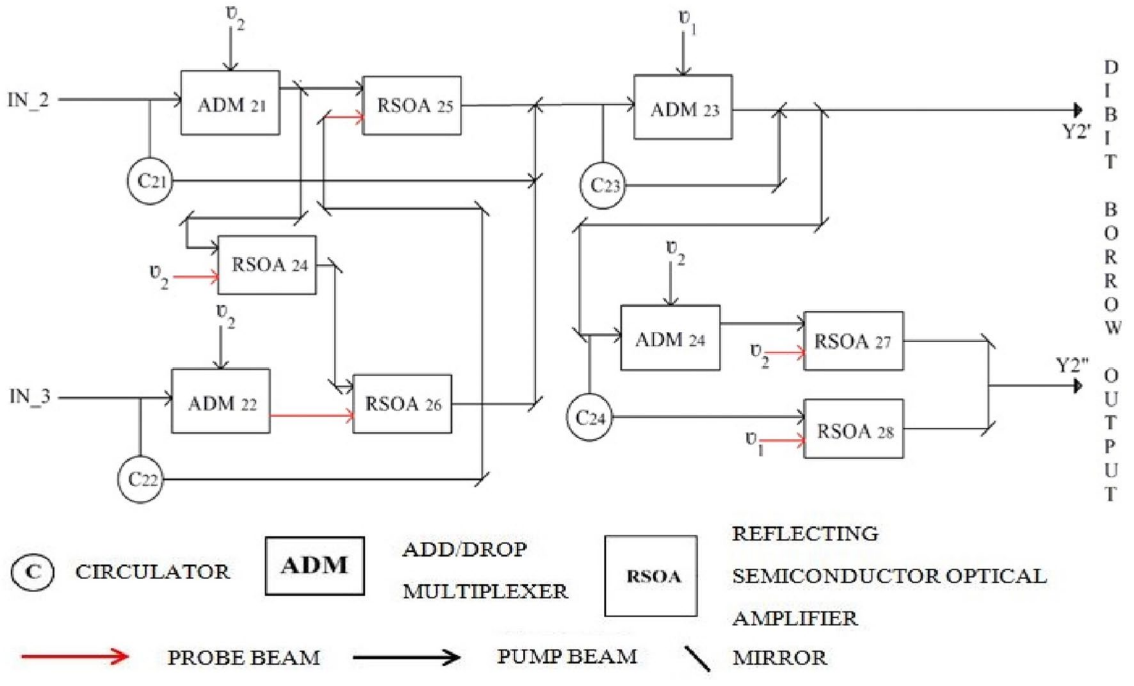


Fig. 5 Internal structure of block 3

block 1, similarly in block 2, RSOA$_{14}$ will give output light beam having frequency ν_2 and that will be injected to the RSOA$_{15}$ as pump beam so RSOA$_{15}$ gives output light beam having frequency ν_1 because the probe beam of RSOA$_{15}$ will be the light beam having frequency ν_1 coming from the output of ADM$_{14}$ (as said previously). The output of RSOA$_{15}$ is feed to the output terminal Y1' and the input of ADM$_{20}$ which is biased with the light beam having frequency ν_1 so ADM$_{20}$ will pass the light beam having frequency ν_1 and feed to the RSOA$_{22}$ as a pump beam; also the probe beam of RSOA$_{22}$ is the light beam having frequency ν_2, so the output of the RSOA$_{22}$ will be the light beam having frequency $\nu_{2.}$ The output will be directly connected to another output terminal Y1".

Finally, in the dibit difference output ports $< Y1' >$ and $< Y1'' >$, the output will be in dibit form $<\nu_1>$ and $<\nu_2>$ or in digital logic '0' and '1', respectively, which is satisfying the truth table of the full subtractor. RSOA$_{18}$ will not be in operation because there is no probe beam in this logical combination. Again, similarly like block 1 in RSOA$_{16}$, the probe beam has frequency ν_2, so the output of the RSOA$_{16}$ will be ν_2 and feed to the ADM$_{16}$. ADM$_{16}$ is biased with a light beam having frequency ν_2, so it will drop the input through circulator C$_{16}$ and feed to the RSOA$_{20}$ as probe beam; as there is no pump beam in this logical combination in RSOA$_{20}$, RSOA$_{20}$ will not be in operation. Again, similarly like block 1, the output of ADM$_{17}$ is feed to the input of ADM19 as ADM$_{19}$ have no biasing in this logical combination; so it will pass the input beam to the output having frequency $\nu_1$which is injected to the RSOA$_{19}$ as probe beam. Already the pump beam of RSOA$_{19}$ is given which is having frequency ν_2. So, the output of RSOA$_{19}$ will be the light beam having frequency ν_1. The output of RSOA$_{19}$ is feed to the output port OUT_3 of block 2.

Now, in block 3, there are two input ports IN_1 and IN_2 which are directly connected to the output ports OUT_2 of block 1 and OUT_3 of block 2. Now in the both output ports, the output will be light beam having frequency ν_1. So, the light beam having frequency ν_1 is injected to the ADM$_{21}$ and ADM$_{22}$. Both the ADM blocks are biased with the light beam having frequency ν_2, so both the ADM blocks will pass the input light beam having frequency ν_1. Now, the output of ADM$_{21}$ is feed to the RSOA$_{24}$ and in RSOA$_{25}$ as pump beam. Also, the output of ADM$_{22}$ is injected to the RSOA$_{26}$ as probe beam. Already the probe beam of RSOA$_{24}$ is given having frequency of ν_2. So, the output of the RSOA$_{24}$ will be ν_2, and it will be injected to the RSOA$_{26}$ as pump beam, and the output of the RSOA$_{26}$ will be light beam having frequency ν_1. The output of the RSOA$_{26}$ is feed to the ADM$_{23}$ which is biased with light beam having frequency ν_1 so the ADM$_{23}$ will drop the input signal through the circulator C$_{23}$ and travels towards the output terminal Y2'. From the output terminal Y2', one part of the light beam having frequency ν_1 injected to the ADM$_{24}$ which is biased with the light beam having frequency ν_2 so it will pass the input light beam and feed to the RSOA$_{27}$ as pump beam. Already the probe beam of $RSOA_{27}$ is given having frequency ν_2, so the output of $RSOA_{27}$ will be the light beam having frequency ν_2, and it will travel towards the output terminal Y2″. As there is no probe beam present in this logical combination, $RSOA_{25}$ will not be in operation. Finally, in the dibit borrow output ports Y2' and Y2″, the output will be in dibit form $<\nu_1>$ and $<\nu_2>$ or in digital logic '0' and '1', respectively, which is satisfying the truth table of the full subtractor. Truth table of full subtractor is shown in Table 1.

Secondly, in the dibit input terminals of block 2 < C' > and < C" >, the input signal is changed to $<\nu_2>$ and $<\nu_1>$ but the other inputs < A' >, < A" >, < B' > and < B" > remain unchanged, so the output of block 1 is same as the previous combination, i.e. from OUT_1 and OUT_2 light beam having frequency ν_1 will come out.

In block 2, the output from ADM_{12} is same as the previous combination and injected to the $RSOA_{18}$ and $RSOA_{14}$ as pump beam but probe beam of $RSOA_{14}$ is already given, i.e. the light beam having frequency ν_2; so the output of the $RSOA_{14}$ will be ν_2 and connected to the $RSOA_{15}$ as pump beam but no probe beam is present of $RSOA_{15}$ in this combination for this reason $RSOA_{15}$ will not work. As in the input ports of block 2, the inputs are changed, so the input of ADM_{14} will be the light beam having frequency ν_2; also the ADM_{14} is biased with light beam having frequency ν_2; so the input light beam will drop through circulator C_{14} and feed to the $RSOA_{18}$ as probe beam. Now, the output of the $RSOA_{18}$ will be light beam having frequency ν_2 which is connected to the output port Y1' and to the ADM_{20} as input, but the ADM_{20} will biased with the light beam having frequency ν_2; so ADM_{20} will drop the input light beam through circulator C_{20} and connected to the $RSOA_{23}$ as pump beam but probe beam of $RSOA_{23}$ is already given which is having frequency ν_1; so the output of $RSOA_{23}$ will be light beam having frequency ν_1 and connected to the output port Y1″. So, the dibit difference output for this combination will be $<\nu_2>$ and $<\nu_1>$, i.e. in digital logic '1' which satisfies the truth table of full subtractor.

Also, the probe beam of $RSOA_{20}$ is similar as the previous combination, i.e. the light beam having frequency ν_2. As the input is changed for block 2, the input of ADM_{17} will be changed, and the changed input will be light beam having frequency ν_2; also the ADM_{17} will be biased with light beam having frequency ν_2, so the input light beam is dropped through circulator C_{17} and feed to the $RSOA_{21}$ as pump beam. Already the probe beam of $RSOA_{21}$ is given, i.e. the light beam having frequency ν_1, so the output of $RSOA_{21}$ will be light beam having frequency ν_1. Now, the output of $RSOA_{21}$ is connected to the $RSOA_{20}$ as pump beam so the output of the $RSOA_{20}$ will be light beam having frequency ν_2. As there is no biasing given to the ADM_{18}, the input of ADM_{18} which is the output of $RSOA_{20}$ travels towards the output port of block 2 OUT_3.

In block 3, the inputs will be light beams having frequency ν_1 and ν_2, respectively, to the input ports IN_2 and IN_3. So, the pump beam of $RSOA_{25}$ and $RSOA_{26}$ is same as the previous combination which are ν_1 and ν_2, respectively. Now, the input of ADM_{22} will be the light beam having frequency ν_2; also, the ADM_{22} will be biased with the light beam ν_2, so the input will drop through circulator C_{22} and feed to the $RSOA_{25}$ as probe beam, so the output of $RSOA_{25}$ will be the light beam having frequency ν_2 which is connected to the input of ADM_{23}. ADM_{23} will be biased with the light beam having frequency ν_1, so ADM_{23} will pass the input light beam, and the output of ADM_{23} is connected to the output port Y2' and input of ADM_{24}. Again, ADM_{24} will bias with the light beam having frequency ν_2, so the input will drop through circulator C_{24} and feed to the $RSOA_{28}$ as pump beam. Already the probe beam of $RSOA_{28}$ is the light beam having frequency ν_1. So, the output of $RSOA_{28}$ will be the light beam having frequency ν_1 and connected to the output port Y2″. In block 3, as the dibit borrow output terminal (Y2' and Y2″) are the light beam of ν_2 and ν_1 frequencies, respectively, they satisfy the truth table of the full subtractor.

Now from the above analytical discussion, we can conclude that in each and every digital logic combination, the

Table 1 Truth table of dibit-based all-optical frequency encoded full subtractor

Dibit input 1		Digital form	Dibit input 2		Digital form	Dibit input 3		Digital form	Dibit difference out		Digital form	Dibit borrow output		Digital form
A'	A"		B'	B"		C'	C"		Y1'	Y1"		Y2'	Y2"	
ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0
ν_1	ν_2	0	ν_1	ν_2	0	ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1
ν_1	ν_2	0	ν_2	ν_1	1	ν_1	ν_2	0	ν_2	ν_1	1	ν_2	ν_1	1
ν_1	ν_2	0	ν_2	ν_1	1	ν_2	ν_1	1	ν_1	ν_2	0	ν_2	ν_1	1
ν_2	ν_1	1	ν_1	ν_2	0	ν_1	ν_2	0	ν_2	ν_1	1	ν_1	ν_2	0
ν_2	ν_1	1	ν_1	ν_2	0	ν_2	ν_1	1	ν_1	ν_2	0	ν_1	ν_2	0
ν_2	ν_1	1	ν_2	ν_1	1	ν_1	ν_2	0	ν_1	ν_2	0	ν_1	ν_2	0
ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1	ν_2	ν_1	1

outputs will satisfy the truth table of the all-optical full subtractor.

Simulation process of dibit-based all-optical frequency encoded full subtractor

MATLAB (R2107a) simulation software is used here for simulation of dibit-based all-optical frequency encoded full subtractor with dibit examine expertness using add drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA), respectively. Here, three blocks are used for dibit signal implementation and checking which are DIBIT_INPUT 1, DIBIT_INPUT 2 and DIBIT_INPUT 3; also, the output of the blocks are connected to another blocks BLOCK1 and BLOCK2, respectively, considering two back-to-back bits, i.e. 1st bit and 2nd bit, respectively. Reflected semiconductor optical amplifier blocks are programmed properly with 'C' language for selecting the exact output on the output terminal. In RSOA block, there are two input terminals, which are 'pr' and 'pm', respectively, and a output terminal 'y'. The RSOA blocks are fabricated in such a fashion that when the both inputs of the block, pump beam and probe beam, then the output will be the probe beam. Consider the pump beam and probe beam are '3 peta Hz' = ν_{1} = digital low state '0' and '8 peta Hz' = ν_{2} = digital high state '1', respectively, then the output of the RSOA blocks will be '8 peta Hz' = ν_{2} = digital high state '1'. If the values of the pump beam and probe beam shuffled with each other, then the output will change. The Simulink model is shown in Fig. 6. Also, the internal blocks of block 1, block 2 and block 3 are shown in Figs. 7, 8 and 9, respectively.

Now, Add drop multiplexer blocks are fabricated in such a way that if an array of frequencies is applied on the input port of these blocks, then the blocks will drop a particular frequency conditional to the biasing and pass all other frequencies. The drop frequency will change, respectively, if the biasing frequency will change. In these blocks, a distinct frequency at 'bias' port will drop one frequency arriving from 'input' port to 'drop' port and passes other frequencies to 'out' port. Consider, the frequency '8 peta Hz' = ν_{2} = digital high state '1' and frequency '3' peta Hz = ν_{1} = digital low state '0' are present at 'input' and 'bias' terminal, respectively; then, the output of the ADM block is '8' peta

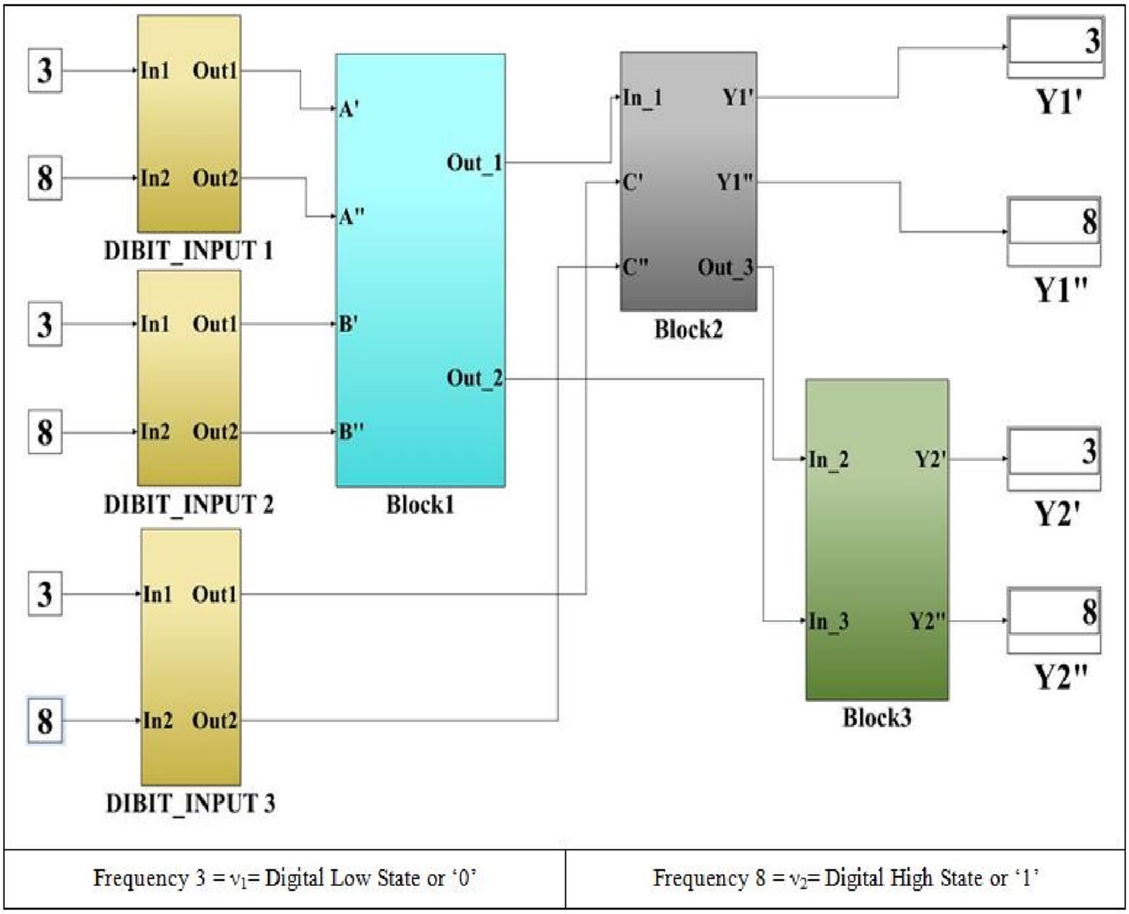


Fig. 6 Simulink model of dibit-based all-optical frequency encoded full subtractor for first digital logic combination

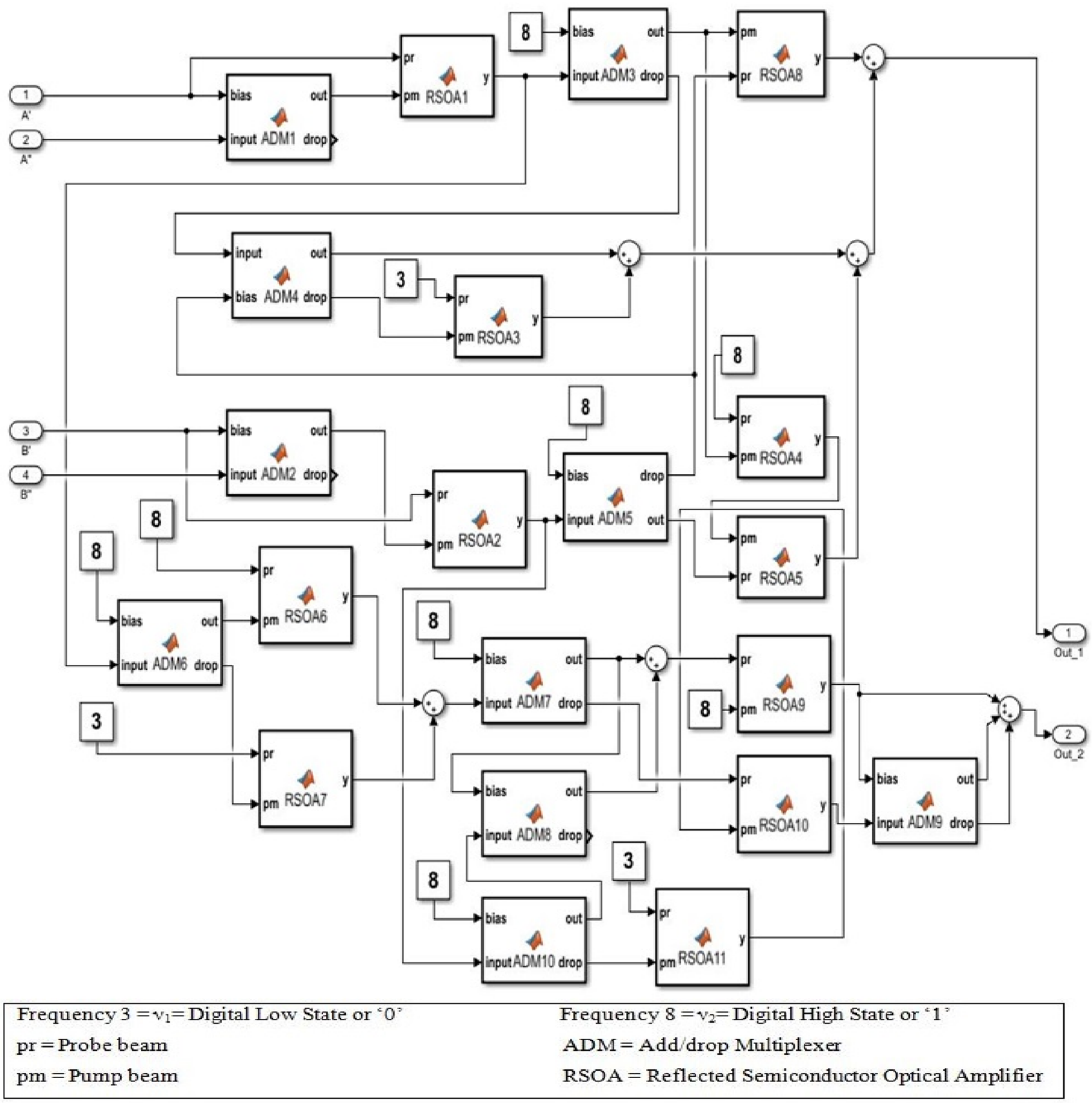


Fig. 7 Internal blocks of block 1 of Simulink model

Hz = ν_2 = digital high state '1'. Now, connecting these two blocks as per block diagram fabricates the dibit-based all-optical frequency encoded full subtractor.

If firstly digital low state or '0' as <3> <8> and <8> <3> as digital high state or '1' are enforced on the three dibit input terminals, then the outputs will be <3> <8> or digital low state or '0' in both the output ports shown in Fig. 6

Secondly, if digital low state or '0' as <3> <8> and <8> <3> as digital high state or '1' are enforced on two dibit input terminals and digital high state or '1' as <8> <3> and <3> <8> as digital low state or '0' on the third dibit input ports, then the output will be <8> <3> or digital high state or '1' in both the output ports and so on..

Finally, if digital high state or '1' as <8> <3> is applied in the all-input ports, then the output will be digital high state or '1' as <8> <3> in both the dibit output ports. Ultimately, the truth table of dibit-based all-optical frequency encoded full subtractor which is shown in Table 1 will ensure with this Simulink model.

Results and discussion

The results, which are coming out from simulation action, are relevant to full subtractor, and the results satisfy the truth table of full subtractor which is shown in Table 1. For the first and second digital logic combination, (say <3> <8> = digital low state = ν_1 = '0'in the three input terminals along with <3> <8> = digital low state = ν_1 = '0'in the two input terminals and in the third

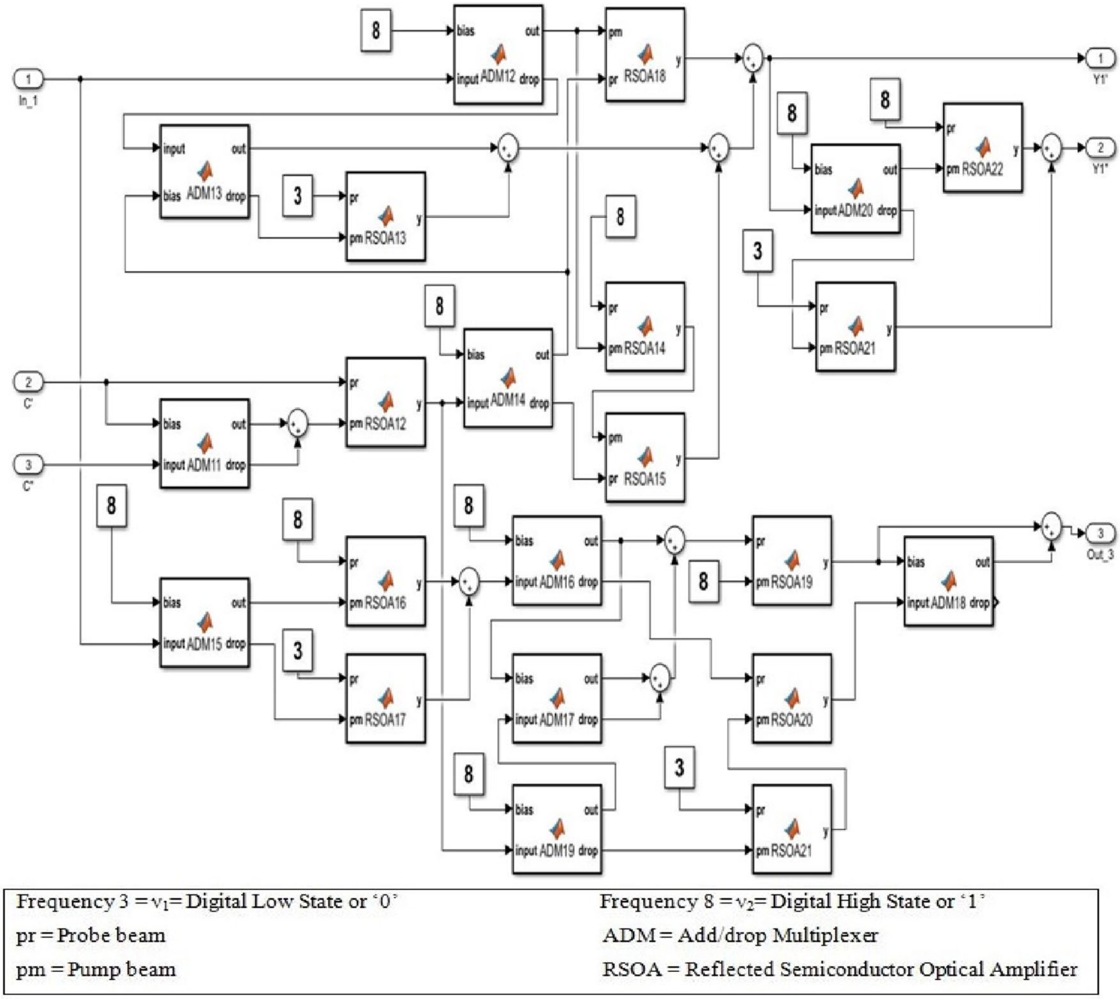


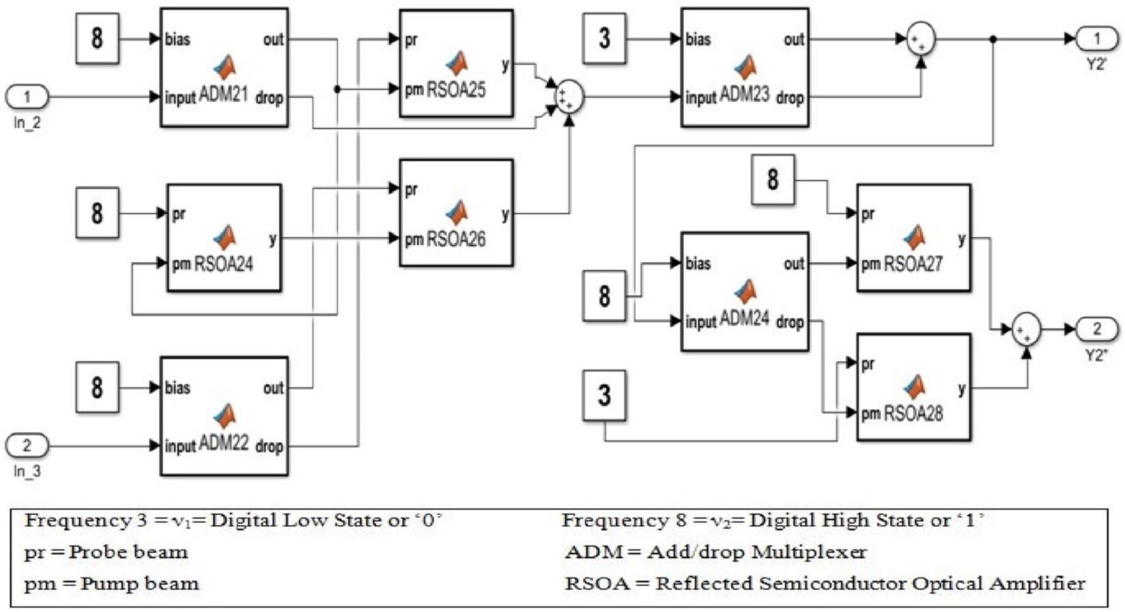
Fig. 8 Internal blocks of block 2 of Simulink model

input terminal $<8>$ $<3>$ = digital high state = ν_2 = '1', respectively), the inputs and the outputs of the Simulink model is shown in Figs. 6 and 10 subsequently.

Also, the graphical outputs of the simulated results for various input combinations are shown collectively in Fig. 11. Here, '1st Dibit Input', '2nd Dibit Input', 'Dibit Borrow Input', 'Dibit Difference Output' and 'Dibit Borrow Output' are shown in graphical way to indicate the digital states according to the truth table of Table 1, and this is clear that the Simulink model will work properly and provide the desired outputs which properly satisfy the truth table of full subtractor.

Conclusions

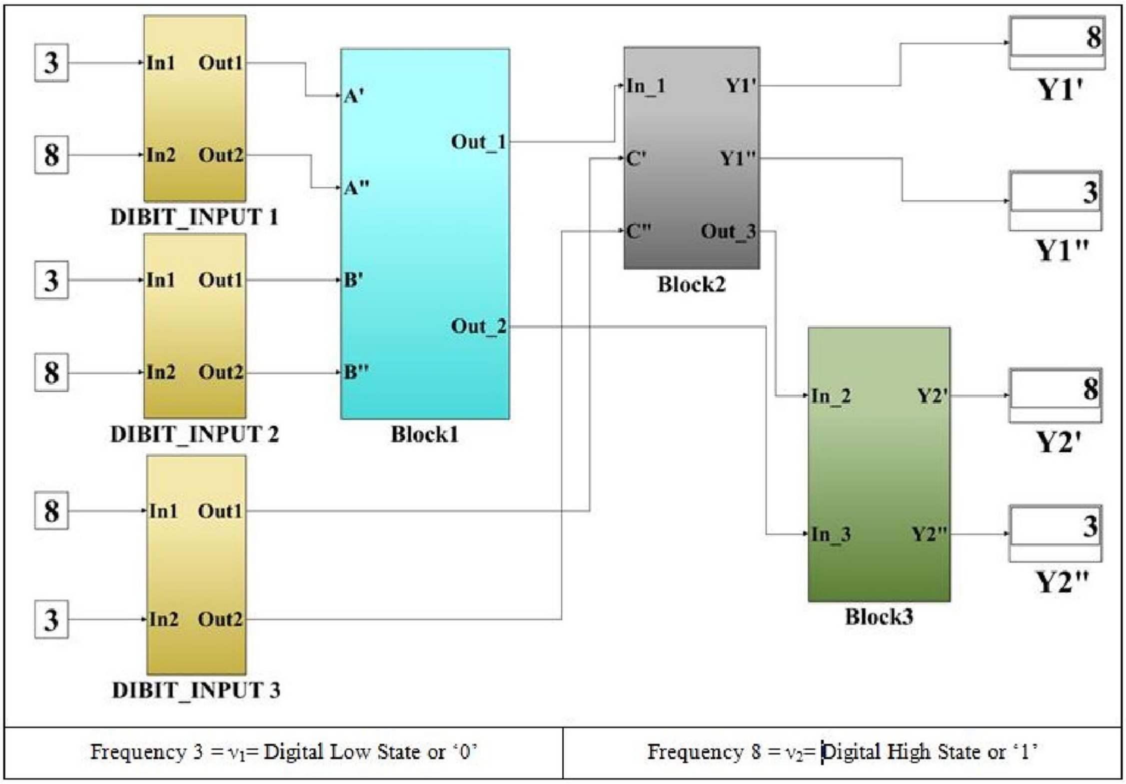
The superiority of frequency encoding technique and dibit depiction processes are described here to understand the all-optical operations. This process is truthful, affectionate and also it will eliminate the bit error problem by developing high signal-to-noise ratio. Now, the dibit checking capability will curtail the wrong states of dibit inputs. Applying this process, it may provide high degree of affinity and enhance drastic working speed. The frequency encoding technique may provide honest and decent result and also helps for arranging the all-optical logical applications. Using optical switches, the design of all-optical dibit-based frequency encoded full subtractor and the simulated authentication may be used for developing all-optical computer. Again this dibit-based all-optical full subtractor may be used as comparator. Finally, it concludes that this all-optical full subtractor can operate with drastic speed, high accuracy in real-time operation.



Frequency 3 = ν_1= Digital Low State or '0'
pr = Probe beam
pm = Pump beam

Frequency 8 = ν_2= Digital High State or '1'
ADM = Add/drop Multiplexer
RSOA = Reflected Semiconductor Optical Amplifier

Fig. 9 Internal blocks of block 3 of Simulink model

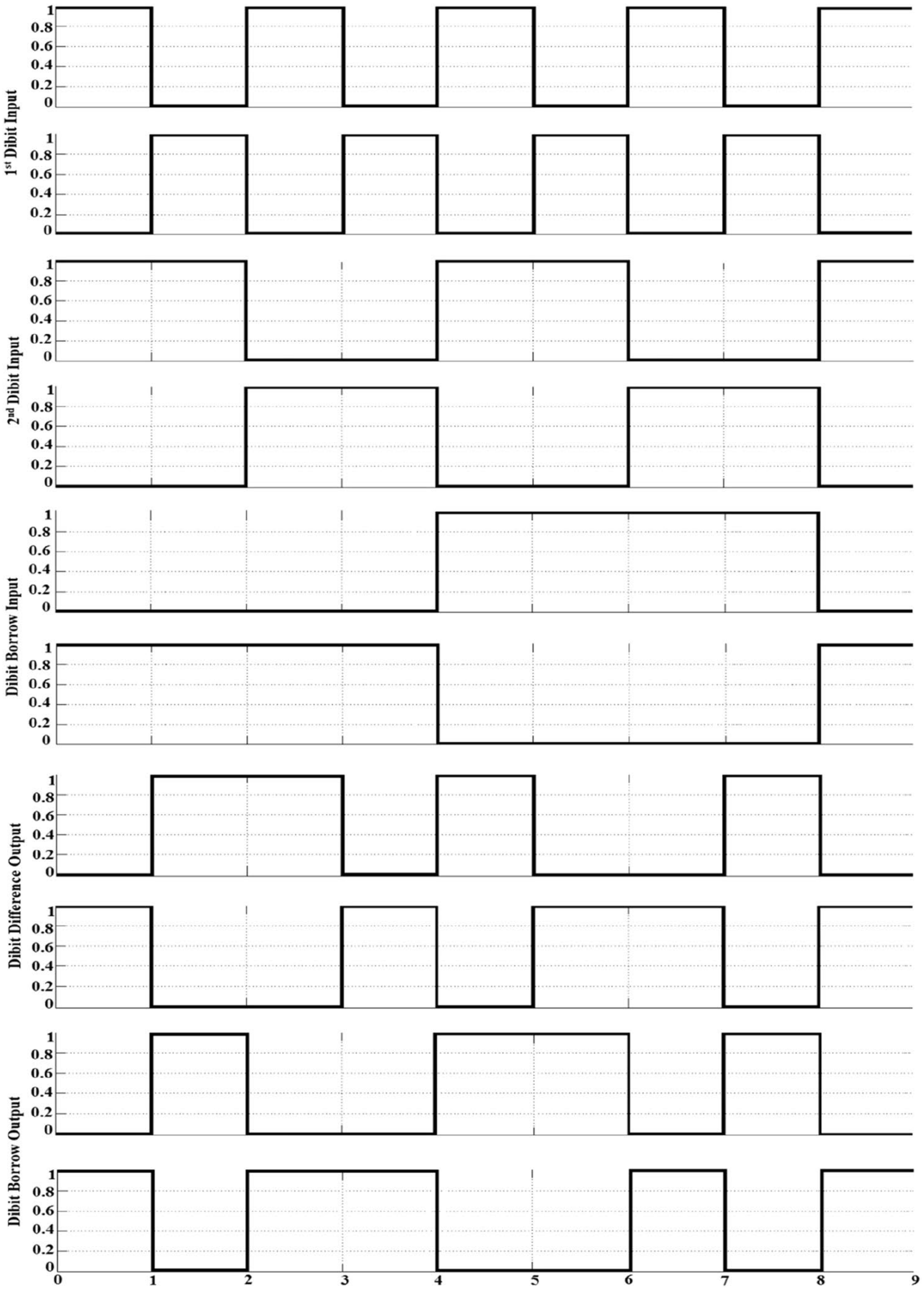


Frequency 3 = ν_1= Digital Low State or '0'

Frequency 8 = ν_2= Digital High State or '1'

Fig. 10 Simulink model of dibit-based all-optical frequency encoded full subtractor for second digital logic combination

Fig. 11 Graphical output of the simulated result



References

1. S. Mukhopadhyay, Role of optics in super-fast information processing. Indian J. Phys. **84**(8), 1069–1074 (2010)
2. A.K. Ghosh, A. Bhattacharya, M. Raul, A. Basuray, Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic. Opt. Laser Technol. **44**(5), 1583–1592 (2012)
3. P.P. Sarkar, S. Mukhopadhyay, All optical frequency encoded NAND logic operation along with the simulated result. J. Opt. **43**(3), 177–182 (2014)
4. B. Ghosh, S. Mukhopadhyay, A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device. Optik Int. J. Light Electron Opt. **124**(21), 4813–4815 (2013)
5. P.P. Sarkar, B. Ghosh, S.N. Patra, S. Mukhopadhyay, A new scheme of an all optical frequency encoded dibit based latch with its simulated result. J. Opt. Technol. **84**(9), 631–634 (2017)

6. P.P. Sarkar, B. Satpati, S. Mukhopadhyay, New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors. J. Opt. **42**(4), 360–366 (2013)
7. V. Cakmak, F. Ufuk, N. Karabulut, Diffusion-weighted MRI of pulmonary lesions: comparison of apparent diffusion coefficient and lesion-to-spinal cord signal intensity ratio in lesion characterization. J. Magn. Reson. Imaging **45**(3), 845–854 (2017)
8. G. Hu, D. Xiao, Y. Wang, T. Xiang, Q. Zhou, Securing image information using double random phase encoding and parallel compressive sensing with updated sampling processes. Opt. Lasers Eng. **98**, 123–133 (2017)
9. J. Zhu, P. Zhou, X. Su, Z. You, Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination. Opt. Express **24**(25), 28549–28560 (2016)
10. C. Taraphdar, T. Chattopadhyay, J. N. Roy, Polarization encoded all-optical ternary Max gate. In: 4th International Conference on Computers and Devices for Communication, Kolkata, India, December, 1–4 (2009)
11. S. Mukhopadhyay, Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems. Appl. Opt. **31**(23), 4622–4623 (1992)
12. P.P. Sarkar, S. Hazra, B. Ghosh, S.N. Patra, S. Mukhopadhyay, Realization of all-optical frequency-encoded dibit-based OR and NOR logic gates with simulated verification, in *Computer, Communication and Electrical Technology*. ed. by D. Guha, B. Chakraborty, H. Dutta (CRC Press, Boca Raton, 2017)
13. B. Ghosh, S. Biswas, S. Mukhopadhyay, A novel method of all-optical wavelength encoded logic and inhibitor operations with dibit representation technique. Optik Int. J. Light Electron Opt. **126**, 483–489 (2015)
14. I.S. Amiri, S.E. Alavi, M. Bahadoran, A. Afroozeh, H. Ahmad, Nanometer bandwidth soliton generation and experimental transmission within nonlinear fiber optics using an add-drop filter system. J. Comput. Theor. Nanosci. **12**(2), 221–225 (2015)
15. S. Chen, Y. Shi, S. He, D. Dai, Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon. IEEE Photonics Technol. Lett. **28**(17), 1874–1877 (2016)
16. J. Wang, L.R. Chen, Low crosstalk Bragg grating/Mach-Zehnder interferometer optical add-drop multiplexer in silicon photonics. Opt. Express **23**(20), 26450–26459 (2015)
17. P.P. Sarkar, B. Ghosh, S.N. Patra, Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer. J. Opt. Technol. **83**(4), 257–262 (2016)
18. B. Ghosh et al., A novel approach to realize of all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches with simulated verification. Opt. Spectrosc. **124**(3), 337–342 (2018)
19. S. Saha, S. Biswas, S. Mukhopadhyay, Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach-Zehnder interferometer-based semiconductor optical amplifier. IET Optoelectron. **11**(5), 201–207 (2017)
20. S. Singh et al., Photonic processing of all-optical Johnson counter using semiconductor optical amplifiers. IET Optoelectron. **11**(1), 8–14 (2016)
21. D.K. Gayen, T. Chattopadhyay, K.E. Zoiros, All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach-Zehnder interferometer. J. Comput. Electron. **14**(1), 129–138 (2015)
22. Q. Cheng et al., Demonstration of the feasibility of large-port-count optical switching using a hybrid Mach-Zehnder interferometer–semiconductor optical amplifier switch module in a recirculating loop. Opt. Lett. **39**(18), 5244–5247 (2014)
23. K. Maji, K. Mukherjee, A. Raja, An alternative method for implementation of frequency-encoded logic gates using a terahertz optical asymmetric demultiplexer (TOAD). J. Comput. Electron. **18**(4), 1423–1434 (2019)
24. M. Mandal, S. Mukhopadhyay, Photonic scheme for implementing quantum square root controlled Z gate using phase and intensity encoding of light. IET Optoelectron. **15**(1), 52–60 (2021)
25. K. Mukherjee et al., All-optical soliton based universal logic NOR utilizing a single reflective semiconductor optical amplifier (RSOA). Photon Netw. Commun. **43**(2), 101–108 (2022)
26. K. Mallick et al., Bidirectional OFDM-MMWOF transport system based on mixed QAM modulation format using dual mode colorless laser diode and RSOA for next generation 5-G based network. Opt. Fiber Technol. **64**, 102562 (2021)
27. A.S. Das, A.S. Patra, Bidirectional transmission of 10 Gbit/s using RSOA based WDM-PON and optical carrier suppression scheme. J. Opt. Commun. **35**(3), 239–243 (2014)
28. K. Mallick et al., Bidirectional hybrid OFDM based Wireless-over-fiber transport system using reflective semiconductor amplifier and polarization multiplexing technique. AEU Int. J. Electr. Commun. **96**, 260–266 (2018)
29. G.C. Mandal et al., A full-duplex WDM hybrid fiber-wired/fiber-wireless/fiber-VLC/fiber-IVLC transmission system based on a self-injection locked quantum dash laser and a RSOA. Opt. Commun. **427**, 202–208 (2018)
30. G.C. Mandal et al., Next-generation bidirectional triple-play services using RSOA based WDM radio on free-space optics PON. Opt. Commun. **411**, 138–142 (2018)
31. G.C. Mandal et al., Bidirectional and simultaneous transmission of baseband and wireless signals over RSOA based WDM /radio-over-fiber passive optical network using incoherent light injection technique. AEU Int. J. Electr. Commun. **80**, 193–198 (2017)
32. A.S. Das, A.S. Patra, RSOA-based full-duplex WDM-PON for 20 Gbps transmission in two channels over a long-haul SMF using external modulation scheme. J. Opt. Commun. **36**(3), 231–235 (2015)
33. J.K. Rakshit, J.N. Roy, All-optical ultrafast switching in a silicon microring resonator and its application to design multiplexer/demultiplexer, adder/subtractor and comparator circuit. Opt. Appl. **46**(4), 517–539 (2016)
34. J.K. Rakshit, J.N. Roy, Design of all-optical universal shift register using nonlinear microring resonators. J. Comput. Electron. **15**, 1450–1461 (2016)
35. D. Nath et al., Photocurrent generation under forward bias with interfacial tunneling of carrier at pentacene/F16CuPc heterojunction photodetector. J. Alloy. Compd. **815**, 152401 (2020)
36. J.K. Rakshit, J.N. Roy, Silicon micro-ring resonator-based all-optical digital-to-analog converter. Photon Netw. Commun. **34**(1), 84–92 (2017)

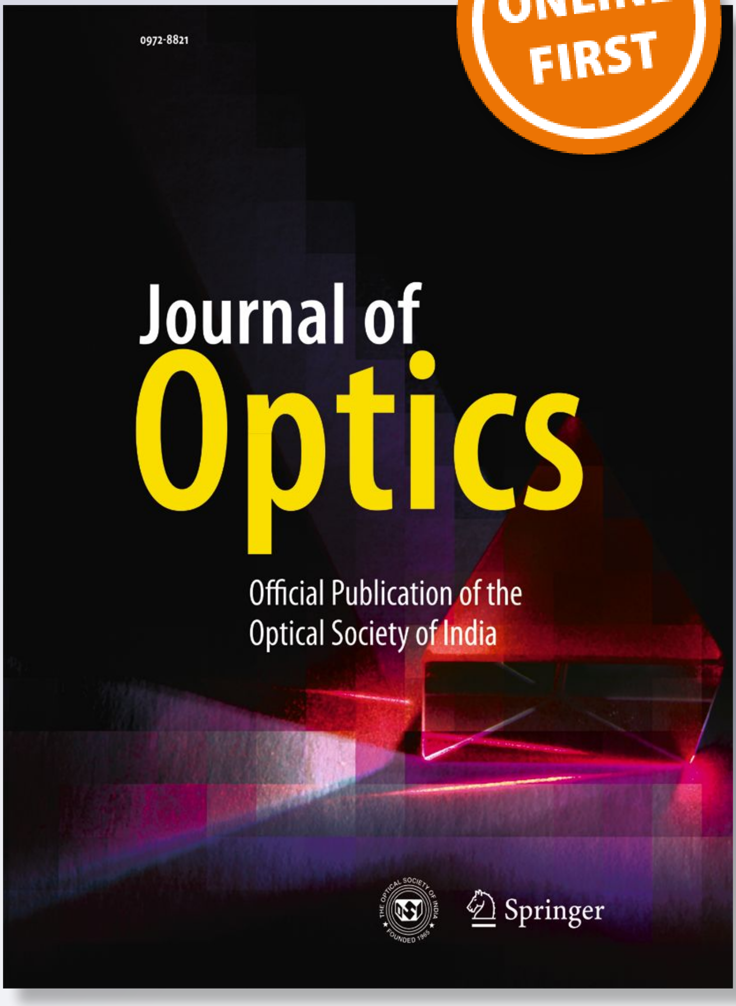
Simulative study of all-optical frequency encoded dibit-based controlled multiplexer and de-multiplexer using optical switches

Bitan Ghosh, Smita Hazra & Partha Pratim Sarkar

Journal of Optics

ISSN 0972-8821

J Opt
DOI 10.1007/s12596-019-00547-9



Springer

J Opt
https://doi.org/10.1007/s12596-019-00547-9

RESEARCH ARTICLE

Simulative study of all-optical frequency encoded dibit-based controlled multiplexer and de-multiplexer using optical switches

Bitan Ghosh[1] · **Smita Hazra**[1] · **Partha Pratim Sarkar**[1]

Received: 28 September 2018 / Accepted: 4 July 2019

Abstract Optics is already established as potential candidate due to its super-fast speed in communication and computation. Therefore, different logical, combinational and sequential circuit operations using all-optical frequency encoding technique have been proposed by several authors. Here, the authors have projected dibit scheme, which reduces the bit error problem and gives the benefit of high-speed operation. Exploiting this fact, here we have proposed all-optical frequency encoded dibit-based multiplexer and de-multiplexer, using the optical switches like add/drop multiplexer and reflected semiconductor optical amplifier. The operation of it has been verified through proper simulation using MATLAB (R2008a).

Keywords Frequency encoding principle · Dibit representation technique · Dibit logic state · Reflected semiconductor optical amplifier · Add/drop multiplexer · Simulink

Introduction

Photon can be used for super-fast information processing, due to its very high-speed operation. So, it is more suitable information carrier than electron. Thus, realization of all-optical different logical and arithmetical digital devices [1, 2] desires different encoding techniques like frequency [3–6], intensity [7], phase [8], spatial [9] and polarization encodings [10]. Among all these encoding principles, frequency encoding principle is most reliable technique because frequency of light beam remains unaffected under reflection, refraction, absorption, etc. At the time of frequency encoding, two different frequencies represent two different states of information. Here, presence of υ_1 frequency of light beam is considered as digital logic state ‘0’ and υ_2 frequency is treated as digital logic state ‘1.’

Now, the dibit representation technique [11–13] can be done to represent a digital logic state by two consecutive bit positions. Therefore, dibit logic state <0> <1> represents the digital logic state ‘0’ and dibit logic state <1> <0> represents digital logic state ‘1,’ respectively. Now, if we apply frequency encoding principle then these two bit positions may be considered as two different frequencies. Therefore, the presence of the two frequencies $<\upsilon_1> <\upsilon_2>$ represents the digital logic state ‘0’ and $<\upsilon_2> <\upsilon_1>$ does the same as the digital logic state ‘1.’

Here, the authors have proposed two different combinational digital circuits like multiplexer (MUX) and de-multiplexer (De-MUX) using all-optical dibit-based technique. First one selects one of several dibit input lines and forwards the selected input into a dibit output line, whereas the second one that takes a dibit input line and routes it to one of several dibit output lines. Again, we proposed appropriate dibit checking unit, which prevents the inappropriate inputs (like <0> <0> or <1> <1>) to enter into the dibit-based circuit to increase the reliability of the digital circuit.

These two schemes are designed by all-optical switches like add/drop multiplexer (ADM) [14–17] and reflected semiconductor optical amplifier (RSOA) [18–22]. Add/drop multiplexer (ADM) is a frequency choosy optical

---

✉ Partha Pratim Sarkar
pratim34@gmail.com

Bitan Ghosh
bitanghosh87@gmail.com

[1] Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan, West Bengal 713104, India

switching device. If it is biased by a light beam of particular frequency then the particular frequency of light beam is reflected by ADM from input and passes all other frequency of light beam. Opposite incident happens if the biasing input changes. Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device, where a weak probe beam with particular frequency (υ_1 frequency) and a strong pump beam with another frequency (say, υ_2 frequency) are inserted to the input terminals of RSOA. Then, this switch will give light beam of υ_1 frequency with power of the pump beam. Therefore, they could be recognized as very useful optical switches for implementing many all-optical logical operations.

The range of saturation power in SOA-based block may be used in the range of 5–20 dBm, which is quite wide range. For this reason, the proposed simulated model expected to replace OFA (optical fiber amplifier) [23]-based network components. This power handling capacity can be considered as one of the major advantages in case our proposed model.

Scheme of realization of frequency encoded dibit-based multiplexer

Here, 2 × 1 MUX is considered having two data input lines as 'A' and 'B,' respectively, for realizing the dibit-based MUX. These two lines, i.e., 'A' and 'B,' are further divided as 'A′' and 'A″,' 'B′' and 'B″,' respectively, to provide dibit inputs. And a selection line is considered as 'S' (subdivided into 'S′' and 'S″') for providing dibit selection line (shown in Fig. 1).

At first, <υ_1> <υ_2> frequency or dibit input <0> <1> is given to all the input lines of <A′> <A″>, <B′> <B″> and <S′> <S″> simultaneously. Since there is a dibit checking unit by ADM_1 with $RSOA_1$, ADM_2 with $RSOA_2$ and ADM_3 with $RSOA_3$ blocks, it checks the real dibit input combinations, respectively. So, it can be said the inputs are controlled before entering to the system. For input line 'A,' the light beam of υ_1 frequency coming from 'A′' acts as biasing terminal of ADM_1. So, the light beam of υ_2 frequency coming from 'A″' passes through the ADM_1. Thus, υ_1 and υ_2 frequencies of light beam come as probe beam and pump beam of $RSOA_1$, respectively. So, the light beam of υ_1 frequency comes out from $RSOA_1$ as output to the 'C' point. By the same way, for dibit input <υ_1> <υ_2> or <0> <1> to line 'B,' light beam of υ_1 frequency also comes out from $RSOA_2$ to the 'D' point. At the selection line 'S,' light beam of υ_1 frequency comes out from $RSOA_3$ and goes to the input of ADM_4 which is biased by υ_2 frequency. So, the light beam of υ_1 frequency passes through it and comes out as pump beam to $RSOA_4$. Due to the absence of pump beam to $RSOA_5$, this block does not work. Therefore, no beam is coming from point 'D' to the point 'X.' But, light beam of υ_1 frequency goes to $RSOA_4$ as probe beam from point 'C.'

With the presence of both beams, $RSOA_4$ provides υ_1 frequency as output and goes directly to 'Y′' of output terminal. Now, one part of this light beam from point 'X' goes to ADM_5, biased by υ_2 frequency. So, it passes light beam of υ_1 frequency and goes as pump beam of $RSOA_6$, but there is a constant probe beam of υ_2 frequency. For that reason, light beam of υ_2 frequency comes out from $RSOA_6$ and goes to 'Y″' of output terminal. ($RSOA_7$ does not work as there is no pump beam.) So, we may get dibit MUX output <υ_1> <υ_2> or <0> <1> or digital logic state '0' at the output terminal 'Y′' and 'Y″,' respectively, coming from input line 'A' for given dibit inputs of <υ_1> <υ_2>-or <0> <1> and <υ_1> <υ_2> or <0> <1> or, digital logic states '0' and '0' at input lines both 'A' and 'B,' respectively, using dibit selection input <υ_1> <υ_2>-or <0> <1> or digital logic state '0' at selection line 'S.' Similarly if we consider the inputs as <υ_1> <υ_2> or digital logic '0' at input line 'A' and <υ_2> <υ_1> or digital logic '1' at input line 'B,' keeping same dibit selection input at selection line 'S,' we get the output in the form of <υ_1>-<υ_2> or <0> <1> at the output line <Y′> <Y″> again, coming from input line 'A.'

Next, if we change the dibit inputs as <υ_2> <υ_1> or digital logic '1' at input line 'A' and <υ_1> <υ_2> or digital logic '0' at input line 'B,' keeping same dibit selection input as <υ_1> <υ_2> or <0> <1> actually, digital logic state '0' at selection line 'S,' then we get υ_2 frequency as probe beam to $RSOA_4$. Due to the presence of pump beam, $RSOA_4$ provides υ_2 frequency to the output line 'Y′.' Now, from point 'X' a part of υ_2 frequency of light beam comes to ADM_5, which is biased by υ_2 frequency. So, it reflects υ_2 frequency in the form of pump beam of $RSOA_7$. Then, we get υ_1 frequency to output line 'Y″' from $RSOA_7$. Similarly, if we consider the inputs as <υ_2> <υ_1> or digital logic '1' at input line 'A' and <υ_2> <υ_1> or digital logic '1' at input line 'B,' keeping same dibit selection input, we get the output in the form of <υ_2> <υ_1> or <1> <0> at the output terminal 'Y′' and 'Y″,' respectively. So, we can say the dibit MUX output changes depending to the value of first dibit input of channel 'A,' i.e., this circuit selects the input line 'A' as dibit input. This operation is satisfied by MUX logic for the dibit selection input as <υ_1> <υ_2>-or <0> <1> actually, digital logic state '0' (shown in Table 1).

Now, if we change the dibit selection input to <υ_2>-<υ_1> or <1> <0> or, digital logic state '1' at the selection line 'S,' then υ_2 frequency of light beam comes out from $RSOA_3$ and this light goes to the input of ADM_4, biased by υ_2 frequency. So, the light beam of υ_2 frequency is reflected by ADM_4 and comes as pump beam to $RSOA_5$.

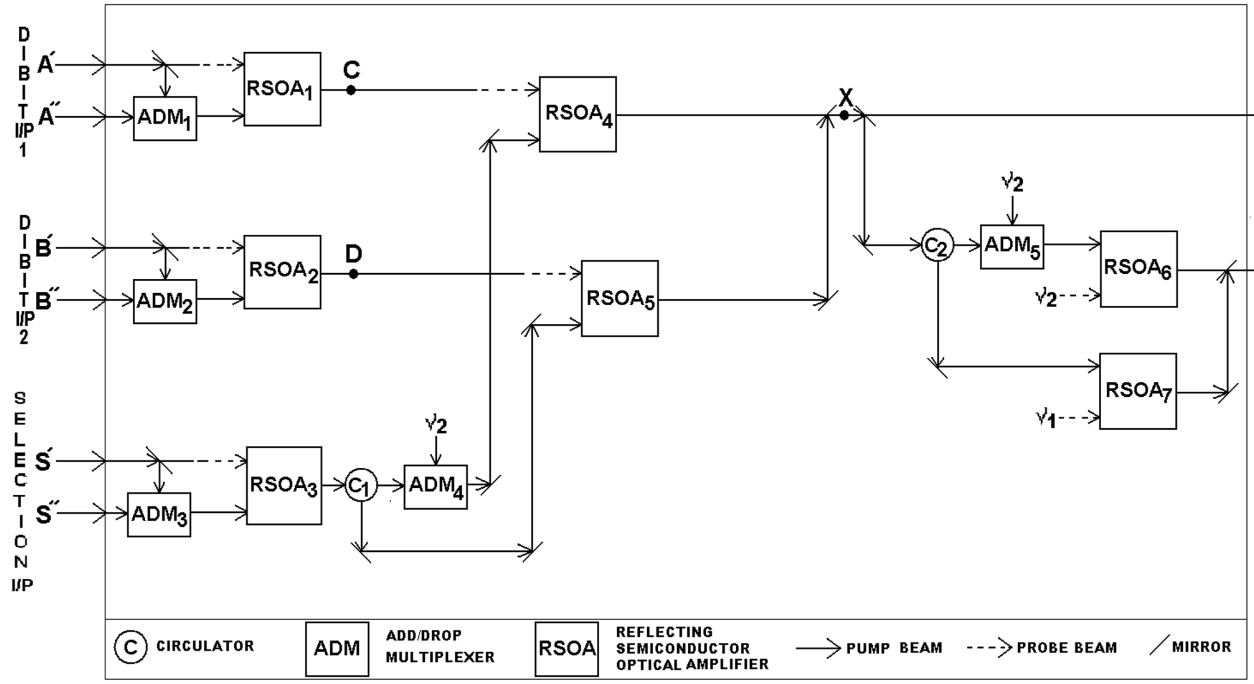


Fig. 1 Block diagram of frequency encoded dibit-based multiplexer

As there is no light beam in the path of pump beam of RSOA$_4$, this block does not work. Now, <υ_1> <υ_2> frequencies or dibit input <0> <1> or digital logic '0' are given to the input lines of <A′> <A″> and <B′> <B″> simultaneously. So, the light beam of υ_1 frequency comes out from RSOA$_1$ as output (at point 'C'). By the same way, the light beam of υ_1 frequency also comes out from RSOA$_2$ as output (at point 'D'). Here, with the presence of pump beam, RSOA$_5$ provides light beam of υ_1 frequency coming from RSOA$_2$ as output and goes directly to 'Y′' of output terminal and from point 'X' one part of this light beam goes to ADM$_5$, biased by υ_2 frequency. So, it passes light beam of υ_1 frequency and goes as pump beam of RSOA$_6$, but there is a constant probe beam of υ_2 frequency and this light beam of υ_2 frequency comes out from RSOA6 and goes to 'Y″' of output line. Similarly, if we consider the inputs as <υ_2> <υ_1> or digital logic '1' at input line 'A' and <υ_1> <υ_2> or digital logic '0' at input line 'B,' keeping same dibit selection input, we get the output in the form of <υ_1> <υ_2> or <0> <1> at the output line <Y′> <Y″>, respectively. Now if we change the dibit inputs as <υ_1> <υ_2> or digital logic '0' at input line 'A' and <υ_2> <υ_1> or digital logic '1' at input line 'B,' keeping same dibit selection input as <υ_2> <υ_1> or <1> <0> actually, digital logic state '1,' then we get υ_2 frequency as probe beam to RSOA$_5$. Due to the presence of pump beam, RSOA$_5$ provides υ_2 frequency to the output line 'Y′.' Now, from point 'X,' a part of υ_2 frequency of light beam comes to ADM$_5$, which is biased by υ_2 frequency. So, it reflects υ_2 frequency in the form of pump beam of RSOA$_7$. Then, we get υ_1 frequency to output line 'Y″' from RSOA$_7$. Similarly, if we consider the inputs as <υ_2> <υ_1> or <1> <0> at input line 'A' and <υ_2> <υ_1> or <1> <0> at input line 'B,' keeping same dibit selection input, we get the output in the form of <υ_2> <υ_1> or <1> <0> at the output line <Y′> <Y″>, respectively. So, we can say that the dibit MUX output changes depending to the value of second dibit input line 'B,' i.e., this circuit selects the input line 'B' as dibit input. This operation is satisfied by MUX logic for the dibit selection input as <υ_2> <υ_1> or <1> <0> actually, digital logic state '1' (shown in Table 1).

Scheme of realization of frequency encoded dibit-based de-multiplexer

For example, 1 × 2 De-MUX scheme is considered having one data input line as 'A,' subdivided into 'A′' and 'A″,' for providing dibit input for realizing the dibit-based De-MUX, in Fig. 2 with a selection line 'S,' subdivided further as 'S′' and 'S″' to provide dibit selection input using the blocks of all-optical switches like add/drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA).

Now, <υ_1> <υ_2> or <0> <1> or digital logic state '0' is given to the input line <A′> <A″> and selection line <S′> <S″> simultaneously. Since there is a dibit checking unit by ADM$_1$ with RSOA$_1$ and ADM$_2$ with RSOA$_2$ blocks, they check the real dibit input combinations, respectively. The light beam of υ_1 frequency coming from ‘A′’ acts as biasing terminal of ADM$_1$. Now, the light beam of υ_2 frequency coming from ‘A″’ passes through the ADM$_1$. Therefore, υ_1 and υ_2 frequencies of light beam come to the probe beam and pump beam of RSOA$_1$, respectively. Then, light beam of υ_1 frequency comes out from RSOA$_1$ at point ‘C’ and goes as probe beam to RSOA$_3$. By the same way, due to the presence of dibit checking blocks comprising ADM$_2$ with RSOA$_2$, the light beam of υ_1 frequency also comes out from RSOA$_2$ at point ‘D.’ Afterward, light beam of υ_1 frequency comes out as pump beam to RSOA$_3$ after passing through ADM$_3$ as it is biased by υ_2 frequency. Though one part of the light beam coming from point ‘C’ enters as probe beam to RSOA$_4$, this block does not work due to the absence of pump beam to RSOA$_4$. With the presence of both beams, RSOA$_3$ provides light beam of υ_1 frequency as output at point ‘E’ and goes directly to ‘X′’ of output terminal. Now from point ‘E,’ another part of the light beam goes to ADM$_4$, biased by υ_2 frequency. So, it passes light beam of υ_1 frequency and goes as pump beam of RSOA$_5$, but there is a constant light of probe beam of υ_2 frequency. For that reason, light beam of υ_2 frequency comes out from RSOA$_5$ (RSOA$_6$ does not work as there is no pump beam) and goes to ‘X″’ of output terminal. So, we may get dibit De-MUX output <υ_1> <υ_2> or <0> <1> or digital logic state ‘0’ at the first dibit De-MUX output terminal ‘X’ for given dibit selection input <υ_1> <υ_2> or <0> <1> or digital logic state ‘0’ at selection line ‘S.’ Similarly, if we consider the input as <υ_2> <υ_1> or <1> <0> or digital logic ‘1’ at input line ‘A’ and keeping same dibit selection input, we get the output in the form of <υ_2> <υ_1> or <1> <0> at the first dibit De-MUX output terminal ‘X′’ and ‘X″,’ respectively. So, we can say that this De-MUX scheme chooses the dibit output path as terminal ‘X’ (DE-MUX O/P 1) as per the selection input as <υ_1> <υ_2>- or <0> <1> actually, digital logic state ‘0,’ shown in Fig. 2. These operations are satisfied by De-MUX logic for this particular dibit selection input which is shown in Table 2.

Next, we change the selection input as <υ_2> <υ_1>- or <1> <0> or digital logic ‘1’ at selection line ‘S’ and apply the dibit De-MUX input as <υ_1> <υ_2>- or <0> <1> or digital logic ‘0’ at input line ‘A.’ After passing dibit checking blocks, we get light beam of υ_1 frequency at point ‘C’ coming from RSOA$_1$ and light beam of υ_2 frequency at point ‘D’ coming from RSOA$_2$. Subsequently, light beam of υ_2 frequency comes out as pump beam to RSOA$_4$ after reflected by ADM$_3$ as it is biased by υ_2 frequency. Besides this, the light beam coming from point ‘C,’ enters as probe beam to RSOA$_3$, but this block

Table 1 Truth table of dibit-based all-optical multiplexer

First dibit MUX input (Channel A)		In digital form	Second dibit MUX input (Channel B)		In digital form	Dibit selection input (Channel S)		In digital form	Dibit MUX output (Channel Y)		In digital form
A′	A″	A	B′	B″	B	S′	S″	S	Y′	Y″	Y
υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0
υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0
υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1
υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1
υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0
υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1
υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0
υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1

does not work due to the absence of pump beam to RSOA$_3$. Now one part of the light beam coming from RSOA$_1$ enters as probe beam to RSOA$_4$. By means of the presence of both beams, RSOA$_4$ provides light beam of υ_1 frequency as output at point 'F' and goes directly to 'Y′' of output terminal. Now from point 'F,' another part of the light beam goes to ADM$_5$, biased by υ_2 frequency. So, it passes light beam of υ_1 frequency and goes as pump beam of RSOA$_7$, but there is a constant probe beam of υ_2 frequency. For that reason, light beam of υ_2 frequency comes out from RSOA$_7$ (RSOA$_8$ does not work as there is no pump beam) and goes to 'Y″' of output terminal. So, we may get dibit De-MUX output <υ_1> <υ_2> or <0> <1> actually, digital logic state '0' at the second dibit De-MUX output terminal 'Y' for given dibit selection input <υ_2> <υ_1> or <1> <0> actually, digital logic state '1' at selection line 'S.' Similarly if we consider the input as <υ_2> <υ_1> or <1> <0> or digital logic '1' at input line 'A' and keeping same dibit selection input, we get the output in the form of <υ_2> <υ_1> or <1> <0> at the second dibit De-MUX output terminal 'Y′' and 'Y″,' respectively. Finally, this De-MUX scheme choose the dibit output path as terminal 'Y' (DE-MUX O/P 2) using the selection input as <υ_2> <υ_1> or <1> <0> actually, digital logic state '1,' which is shown in Fig. 2. These operations are fully satisfied also by De-MUX logic for the specific dibit selection line, which is shown in Table 2.

Simulation process of frequency encoded dibit-based multiplexer

MATLAB version R2008a software has been used for simulation of all-optical frequency encoded dibit multiplexer using optical switches (shown in Fig. 1). In Fig. 3, 'DIBIT_DATA_INPUT 1,' 'DIBIT_ DATA_INPUT 2' and 'SELECTION_DIBIT_INPUT' units are used for applying dibit input lines and selection line, respectively, and we get output line from 'Dibit MUX Output' unit, which is consisted of two consecutive bit positions '1st Bit' and '2nd Bit,' respectively. Now, each of the RSOA blocks is properly programmed according to the RSOA mechanism. There are two inputs 'pr' for probe beam and 'pm' for pump beam and the output 'y' in RSOA blocks. According to the theory of RSOA, if pump beam and probe beam are considered as say '3 peta Hz' = υ_1 = digital logic state '0' and '8 peta Hz' = υ_2 = digital logic state '1,' respectively, then we get '8 peta Hz' = υ_2 = digital logic state '1' at the output terminal of these blocks. The output changes if pump beam and probe beam are altered accordingly. Also, ADM block has been simulated such a way that, it obeys the proper mechanism of ADM. Now if ADM is biased by a particular light beam frequency, say '3 peta Hz' = υ_1 = digital logic state '0' at 'bias' terminal, then this block drops the frequency coming from 'input' terminal to 'drop' terminal and passes other frequency, say '8 peta Hz' = υ_2 = digital logic state '1' to 'out' terminal. If the biasing is changed, opposite incident happens.

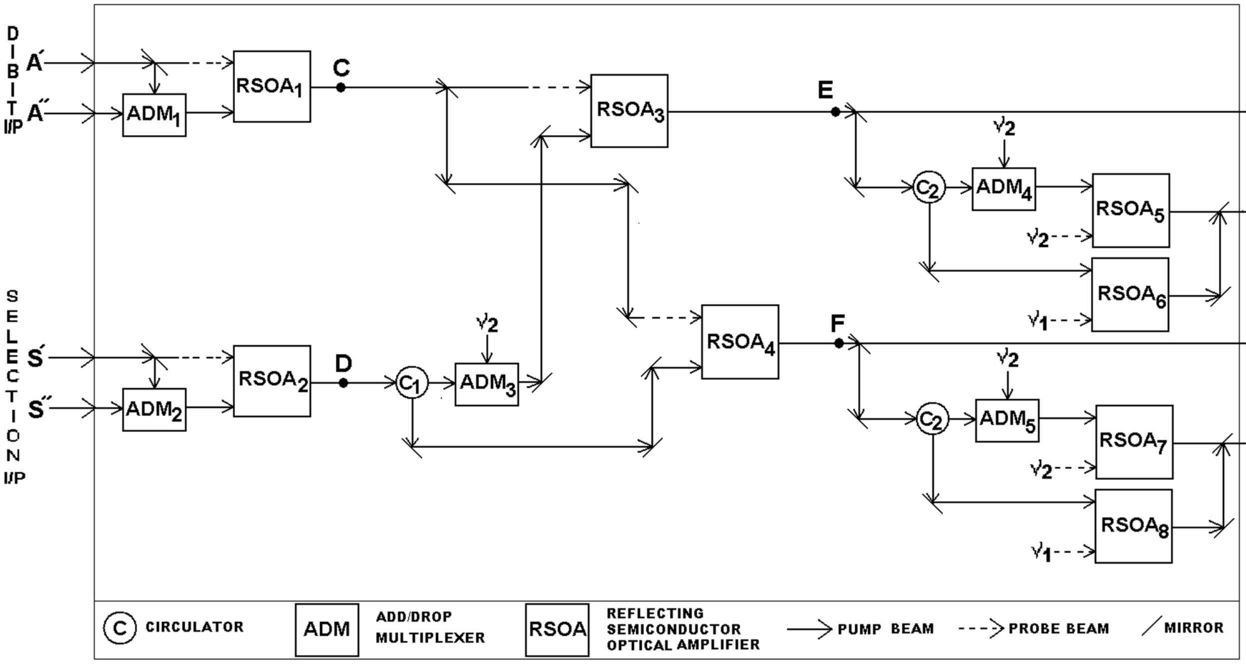


Fig. 2 Block diagram of frequency encoded dibit-based de-multiplexer

Table 2 Truth table of dibit-based all-optical de-multiplexer

Dibit De-MUX Input (Channel A)		In digital form	Dibit selection input (Channel S)		In digital form	First dibit De-MUX output (Channel X)		In digital form	Second dibit De-MUX output (Channel Y)		In digital form
A′	A″	A	S′	S″	S	X′	X″	X	Y′	Y″	Y
υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0	υ_1 [0]	υ_2 [1]	0	×	×	×
υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1	×	×	×	υ_1 [0]	υ_2 [1]	0
υ_2 [1]	υ_1 [0]	1	υ_1 [0]	υ_2 [1]	0	υ_2 [1]	υ_1 [0]	1	×	×	×
υ_2 [1]	υ_1 [0]	1	υ_2 [1]	υ_1 [0]	1	×	×	×	υ_2 [1]	υ_1 [0]	1

By this way, RSOA and ADM blocks have been connected maintaining the similarity of the block diagram of the MUX scheme (shown in Fig. 1) considering the dibit form <3> <8> as digital logic states '0' and dibit form <8> <3> as digital logic states '1.'

For example, if <8> <3> and <3> <8> are applied at the two dibit input lines and <8> <3> is inserted as selection line of the simulated model, we get <3> <8> at the 'Dibit MUX Output' line of this simulated block according to the value at 'DIBIT_ DATA_INPUT 2,' which is shown in Fig. 3. If <3> <8> is applied as selection line, we get <8> <3> at the 'Dibit MUX Output' line according to the value of 'DIBIT_ DATA_INPUT 1.' Therefore, this simulative model fully satisfies the truth table of the MUX scheme, which is shown in Table 1.

Simulation process of frequency encoded dibit-based de-multiplexer

Again, for simulation of frequency encoded all-optical dibit de-multiplexer (shown in Fig. 2), simulink tools of the same software have been used. In Fig. 4, 'DIBIT_DATA_INPUT' and 'SELECTION_DIBIT_INPUT' units are used for applying dibit input line and selection line, respectively, and we get output from 'Dibit De-MUX Output 1' or 'Dibit De-MUX Output 2' lines as per the operations of de-multiplexer. All the output lines are consisted of '1st Bit' and '2nd Bit.'

Maintaining the similarity of the De-MUX scheme (shown in Fig. 2), these RSOA and ADM blocks have been connected in proper way (shown in Fig. 4), considering the dibit form <3> <8> as digital logic states '0' and dibit form <8> <3> as digital logic states '1.' If <3> <8> and <8> <3> are applied at the dibit input line and selection line, respectively, then we get <3> <8> at the 'Dibit De-MUX Output 2' line of this simulated block according to the value at 'DIBIT_ DATA_INPUT.' While 'Dibit De-MUX Output 1' shows <0> <0> assumes to be NULL as per the encoding technique for this simulated model.

Again, if <3> <8> is applied as selection unit, we get <3> <8> at the 'Dibit De-MUX Output 1' unit according to the value of 'DIBIT_ DATA_INPUT,' whereas 'Dibit De-MUX Output 2' shows <0> <0> assumes to be NULL value. So, this simulative verification entirely satisfies the truth table of the De-MUX scheme, which is shown in Table 2.

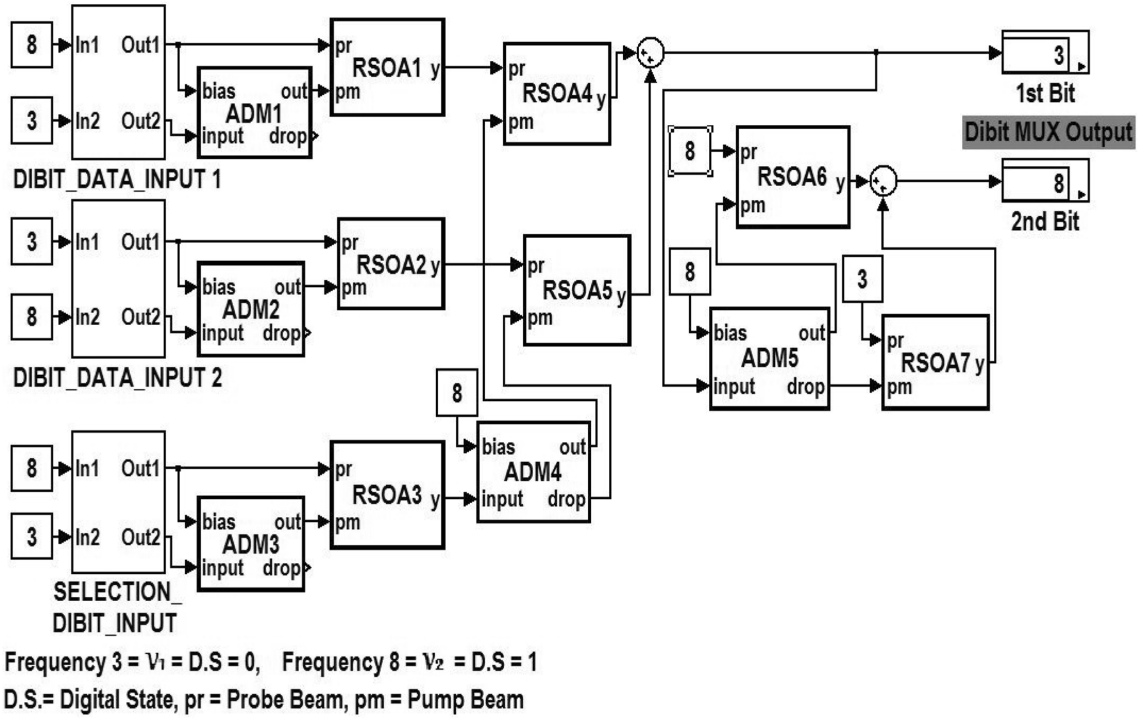


Fig. 3 Simulation model of the dibit-based multiplexer

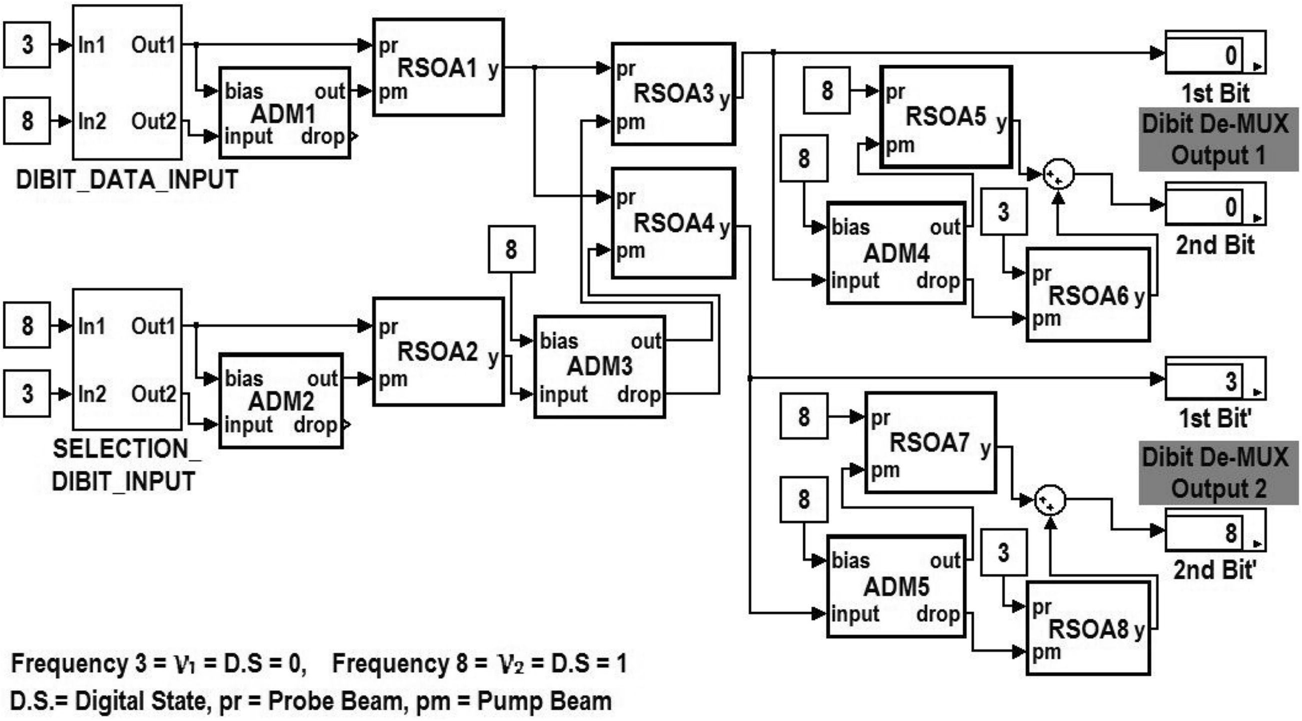


Fig. 4 Simulation model of the dibit-based de-multiplexer

Results and discussion

All the results, getting from the simulation processes, related to multiplexer logic are satisfied by truth table and graphical representation (shown in Fig. 5) for the concern combinational logic circuit and that is why we insert a combined table (Table 1) for all-optical frequency encoded dibit-based multiplexer, providing dibit as well as digital form of input and output.

Also, the de-multiplexer logic is satisfied by truth table and graphical representation (shown in Fig. 6) for the concern combinational logic circuit by getting all the results from the simulation processes. So, we put a combined table (Table 2) for dibit-based de-multiplexer to provide dibit as well as digital form of input, selection line and output.

Conclusions

Here, the advantages of dibit representation as well as frequency encoding technique are subjugated to realize the all-optical operations. In this technique, the dibit control input reduces errors on incorrect dibit input states. Using this system, one can expect a high degree of parallelism also due to dibit-based system with very fast operational speed. This dibit-based frequency encoding technique helps for realization of the all-optical logical and combinational operations with realistic and reliable outcomes. With the realization of these two schemes using optical switches and with the simulated verification, could be used for preparing other all-optical computational devices. Therefore, it exhibits a high-speed and reliable operation.

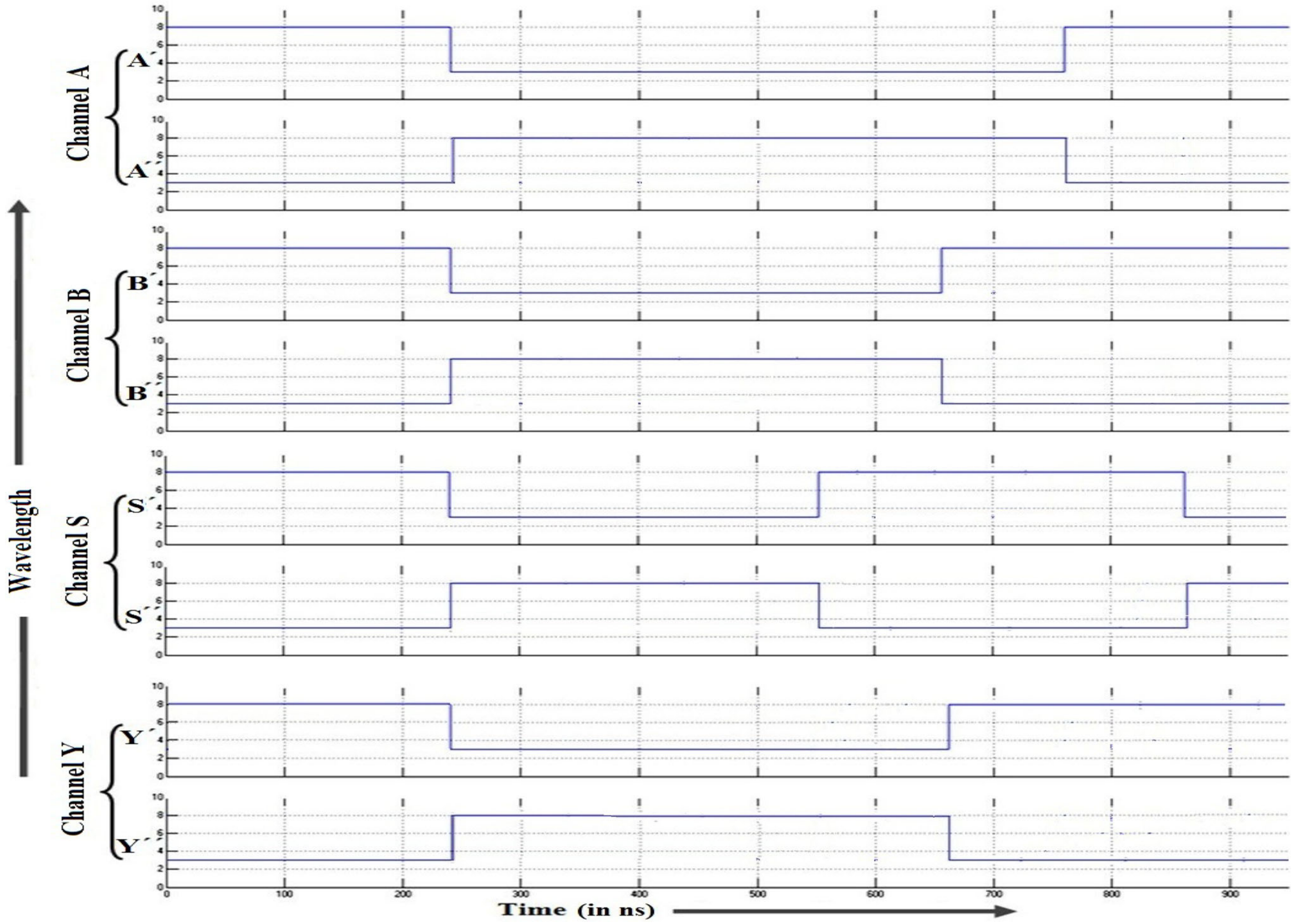


Fig. 5 Graphical representation of all-optical dibit-based multiplexer

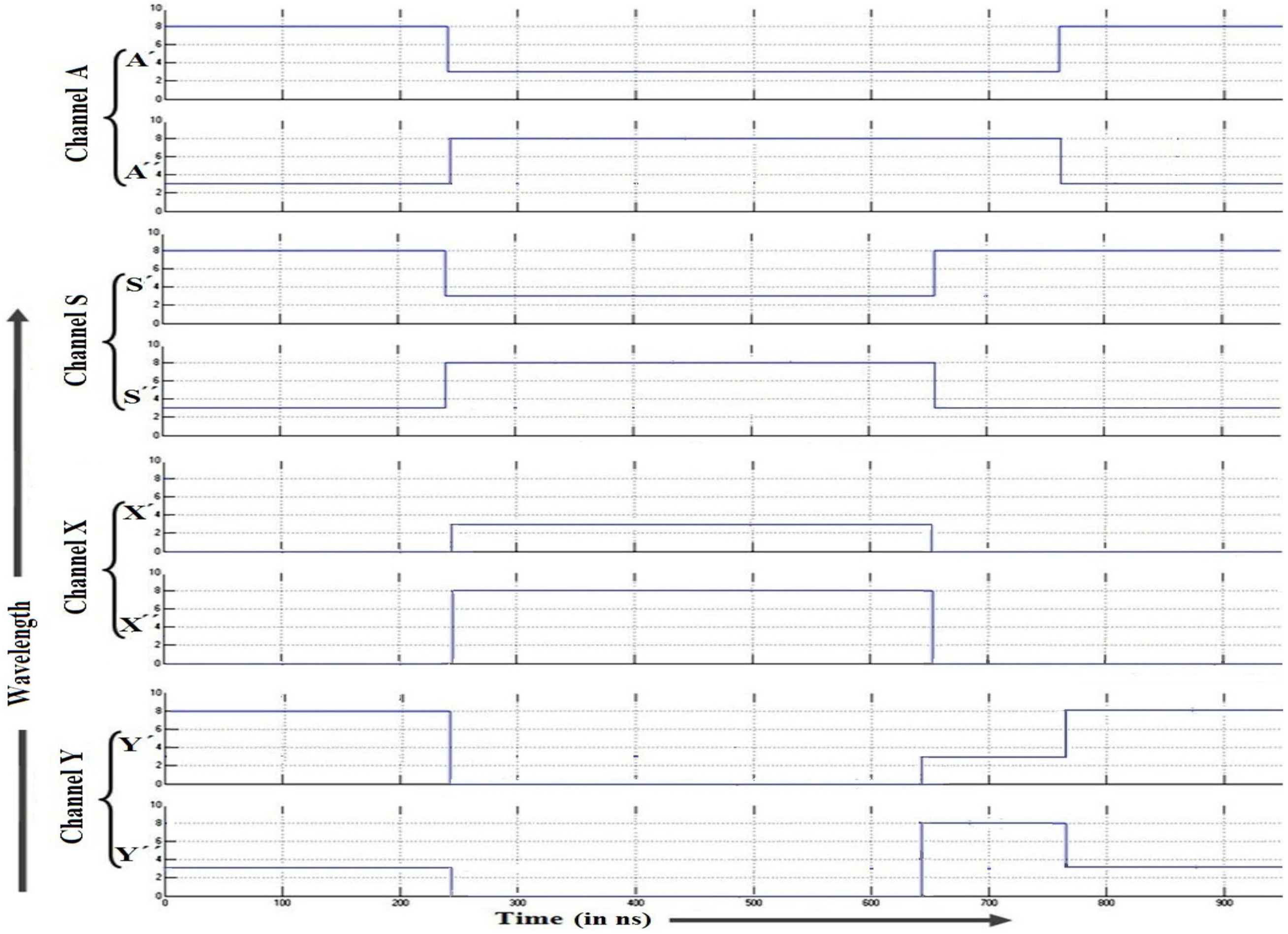


Fig. 6 Graphical representation of all-optical dibit-based de-multiplexer

References

1. S. Mukhopadhyay, Role of optics in super-fast information processing. Indian J. Phys. **84**(8), 1069–1074 (2010). https://doi.org/10.1007/s12648-010-0101-4
2. A.K. Ghosh, A. Bhattacharya, M. Raul, A. Basuray, Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic. Opt. Laser Technol. **44**(5), 1583–1592 (2012). https://doi.org/10.1016/j.optlastec.2011.11.044
3. P.P. Sarkar, S. Mukhopadhyay, All optical frequency encoded NAND logic operation along with the simulated result. J. Opt. **43**(3), 177–182 (2014). https://doi.org/10.1007/s12596-014-0197-6
4. B. Ghosh, S. Mukhopadhyay, A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device. Opt. Int. J. Light Electron Opt. **124**(21), 4813–4815 (2013). https://doi.org/10.1016/j.ijleo.2013.02.035
5. P.P. Sarkar, B. Ghosh, S.N. Patra, S. Mukhopadhyay, A new scheme of an all optical frequency encoded dibit based latch with its simulated result. J. Opt. Technol. **84**(9), 631–634 (2017). https://doi.org/10.1364/JOT.84.000631
6. P.P. Sarkar, B. Satpati, S. Mukhopadhyay, New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors. J. Opt. **42**(4), 360–366 (2013). https://doi.org/10.1007/s12596-013-0133-1
7. V. Çakmak, F. Ufuk, N. Karabulut, Diffusion-weighted MRI of pulmonary lesions: comparison of apparent diffusion coefficient and lesion-to-spinal cord signal intensity ratio in lesion characterization. J. Magn. Reson. Imaging **45**(3), 845–854 (2017). https://doi.org/10.1002/jmri.25426
8. G. Hu, D. Xiao, Y. Wang, T. Xiang, Q. Zhou, Securing image information using double random phase encoding and parallel compressive sensing with updated sampling processes. Opt. Lasers Eng. **98**, 123–133 (2017). https://doi.org/10.1016/j.optlaseng.2017.06.013
9. J. Zhu, P. Zhou, X. Su, Z. You, Accurate and fast 3D surface measurement with temporal-spatial binary encoding structured illumination. Opt. Express **24**(25), 28549–28560 (2016). https://doi.org/10.1364/oe.24.028549
10. C. Taraphdar, T. Chattopadhyay, J.N. Roy, *Polarization encoded all-optical ternary Max gate*. 4th International Conference on Computers and Devices for Communication, Kolkata, India, December 2009, p. 1–4
11. S. Mukhopadhyay, Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems. Appl. Opt. **31**(23), 4622–4623 (1992). https://doi.org/10.1364/AO.31.004622
12. P.P. Sarkar, S. Hazra, B. Ghosh, S.N. Patra, S. Mukhopadhyay, Realization of all-optical frequency-encoded dibit-based OR and NOR logic gates with simulated verification, in *Computer,*

Communication and Electrical Technology, 1st edn., ed. by D. Guha, B. Chakraborty, H. Dutta (CRC Press, Boca Raton, 2017), pp. 153–158. https://doi.org/10.1201/9781315400624-30

13. B. Ghosh, S. Biswas, S. Mukhopadhyay, A novel method of all-optical wavelength encoded logic and inhibitor operations with dibit representation technique. Opt. Int. J. Light Electron Opt. **126**(4), 483–489 (2015). https://doi.org/10.1016/j.ijleo.2014.09.015
14. I.S. Amiri, S.E. Alavi, M. Bahadoran, A. Afroozeh, H. Ahmad, Nanometer bandwidth soliton generation and experimental transmission within nonlinear fiber optics using an add-drop filter system. J. Comput. Theor. Nanosci. **12**(2), 221–225 (2015). https://doi.org/10.1166/jctn.2015.3721
15. S. Chen, Y. Shi, S. He, D. Dai, Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon. IEEE Photonics Technol. Lett. **28**(17), 1874–1877 (2016). https://doi.org/10.1109/LPT.2016.2574459
16. J. Wang, L.R. Chen, Low crosstalk Bragg grating/Mach–Zehnder interferometer optical add-drop multiplexer in silicon photonics. Opt. Express **23**(20), 26450–26459 (2015). https://doi.org/10.1364/OE.23.026450
17. R. Mansoor, S. Koziel, H. Sasse, A. Duffy, Crosstalk suppression bandwidth optimisation of a vertically coupled ring resonator add/drop filter. IET Optoelectron. **9**(2), 30–36 (2015). https://doi.org/10.1049/iet-opt.2014.0059
18. P.P. Sarkar, B. Ghosh, S.N. Patra, Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer. J. Opt. Technol. **83**(4), 257–262 (2016). https://doi.org/10.1364/JOT.83.000257
19. B. Ghosh et al., A novel approach to realize of all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches with simulated verification. Opt. Spectrosc. **124**(3), 337–342 (2018). https://doi.org/10.1134/S0030400X1803013X
20. S. Saha, S. Biswas, S. Mukhopadhyay, Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach–Zehnder interferometer-based semiconductor optical amplifier. IET Optoelectron. **11**(5), 201–207 (2017). https://doi.org/10.1049/iet-opt.2016.0078
21. S. Singh, S. Kaur, R. Kaur, R.S. Kaler, Photonic processing of all-optical Johnson counter using semiconductor optical amplifiers. IET Optoelectron. **11**(1), 8–14 (2016). https://doi.org/10.1049/iet-opt.2015.0106
22. D.K. Gayen, T. Chattopadhyay, K.E. Zoiros, All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach-Zehnder interferometer. J. Comput. Electron. **14**(1), 129–138 (2015). https://doi.org/10.1007/s10825-014-0632-6
23. M. Connelly, *Semiconductor Optical Amplifiers and Their Applications* (University of Limerick, Limerick, 2003)

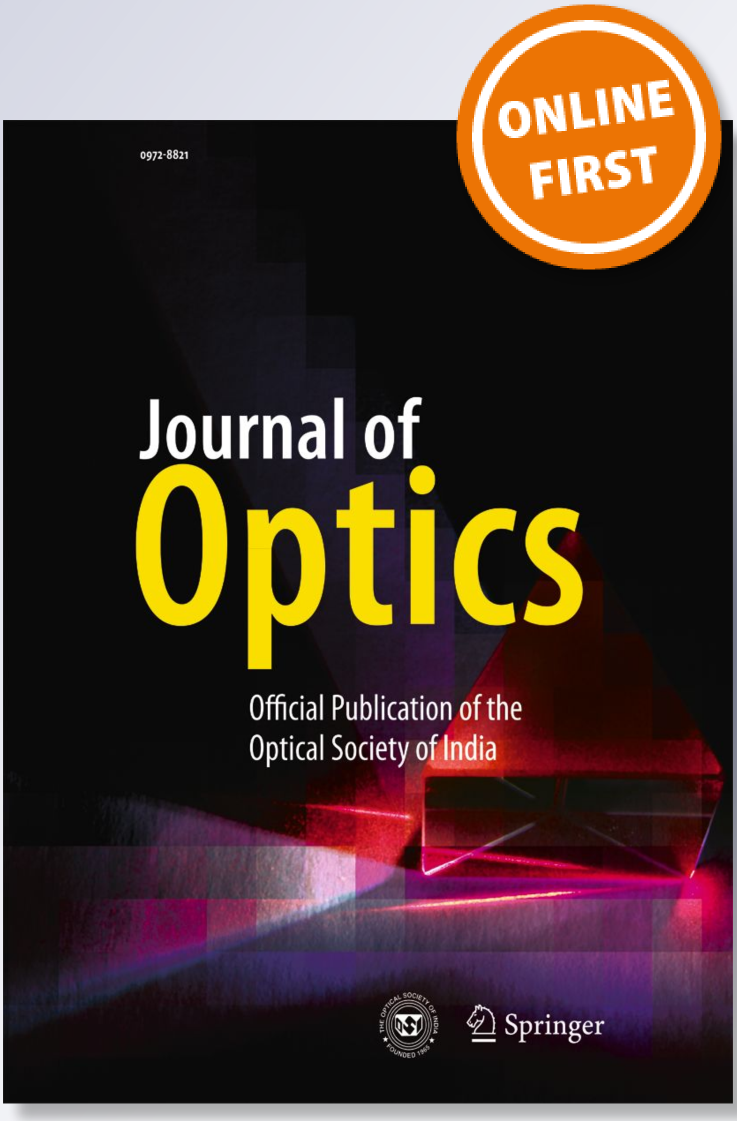
Alternative approach to design all-optical frequency-encoded D and T flip-flops using semiconductor optical amplifier

Smita Hazra, Bitan Ghosh & Partha Pratim Sarkar

Journal of Optics

ISSN 0972-8821

J Opt
DOI 10.1007/s12596-019-00548-8



J Opt
https://doi.org/10.1007/s12596-019-00548-8

RESEARCH ARTICLE

Alternative approach to design all-optical frequency-encoded D and T flip-flops using semiconductor optical amplifier

Smita Hazra[1] · **Bitan Ghosh**[1] · **Partha Pratim Sarkar**[1]

Received: 28 September 2018 / Accepted: 4 July 2019

Abstract In the present scenario of all-optical communication, the design of the optical switch, optical router, optical synchronization, reference clock, optical latches, etc., becomes very essential. Moreover, the matched, combined operation of all these optical components with the existing network is also necessary. In these fields, semiconductor optical amplifier (SOA) technology is very suitable, because of its high-speed switching capacity, as well as good amplification factor, high extinction ratio and high integration potential. SOA does the entire processing in optical domain, without any electronic conversion, including all-optical wavelength conversion, wavelength separation, regeneration, frequency encoding with in-line amplification, in optical domain (photon-level interaction). In this paper, a noble idea on the all-optical D flip-flop and T flip-flop using SOA is proposed.

Keywords Wavelength conversion · Cross-gain modulation · Probe beam · Pump beam · Semiconductor optical amplifier · Latches

✉ Partha Pratim Sarkar
pratim34@gmail.com

Smita Hazra
smhp2007@gmail.com

Bitan Ghosh
bitanghosh87@gmail.com

[1] Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan, West Bengal 713104, India

Introduction

Optics has shown its enormous potentiality to be used in digital information processing, data computation and image processing [1, 2]. In this perspective, optical switches have a significant role in performing the high-speed (THz) operation [3–5]. In this scenario, semiconductor optical amplifier (SOA) is an important optical switch which can do the processing in THz range [6, 7]. SOA acts with co-propagating and counter-propagating nature of beam. SOA has an immense potential to exploit as amplifier, frequency convertor, self-phase modulator. SOA does the entire processing in optical domain, without any electronic conversion, including all-optical wavelength conversion, regeneration, wavelength selection, booster and in-line amplification and mid-span spectral inversion in optical domain (photon-level interaction). SOA follows different topologies. For beam interaction, SOA considers two input beams, and the output is provided based on interactions of input beams, by following anyone among the techniques of cross-gain modulation (XGM), cross-phase modulation (XPM), four-wave mixing (FWM), and self-phase modulation (SPM). The use of SOA becomes very popular, because of simple structure and less cost. In this proposed configuration, cross-gain modulation process (XGM) has been used, to pass or hold the input data, with the same wavelength but with the energy of strong input pump signal wavelength. The value of conversion efficiency is defined as the ratio of refractive index of output beam to the refractive index of input pump wave.

The range of saturation power in SOA-based block may be used in the span of 5–20 dBm, which is quite wide range. For this reason, the proposed simulated model expected to replace OFA (optical fiber amplifier)-based network components. This power handling capacity can be considered as one of the major advantages in case of our proposed model.

Operational characteristics of SOA as frequency encoder

Out of four basic topologies, frequency encryption is based on the cross-gain modulation (XGM) character of SOA which is derived from gain saturation phenomenon. Here, a weak CW probe beam (at a specific wavelength) and a strong pump beam (at another specific wavelength) of light are inserted simultaneously into the SOA. At critical value of biasing current inside the amplifier, the probe beam is selected as a strong beam output from the SOA because of XGM characteristics. Thus, one can refer this incidence as wavelength conversion as well as frequency encryption. There are two types of basic schemes used in XGM-based frequency encryption, first one is co-propagating scheme and second one is counter-propagating scheme. In the first scheme, the pump and probe beams are inserted from the same side of the SOA, and in the second scheme, pump and probe beams are manually inserted from opposite directions into the SOA. Out of these two, co-propagating scheme has better noise performance. For beam interaction, a weak CW probe light of wavelength λ_2 and a strong pump beam of wavelength λ_1 are inserted into the input terminals of the SOA having an anti-reflecting

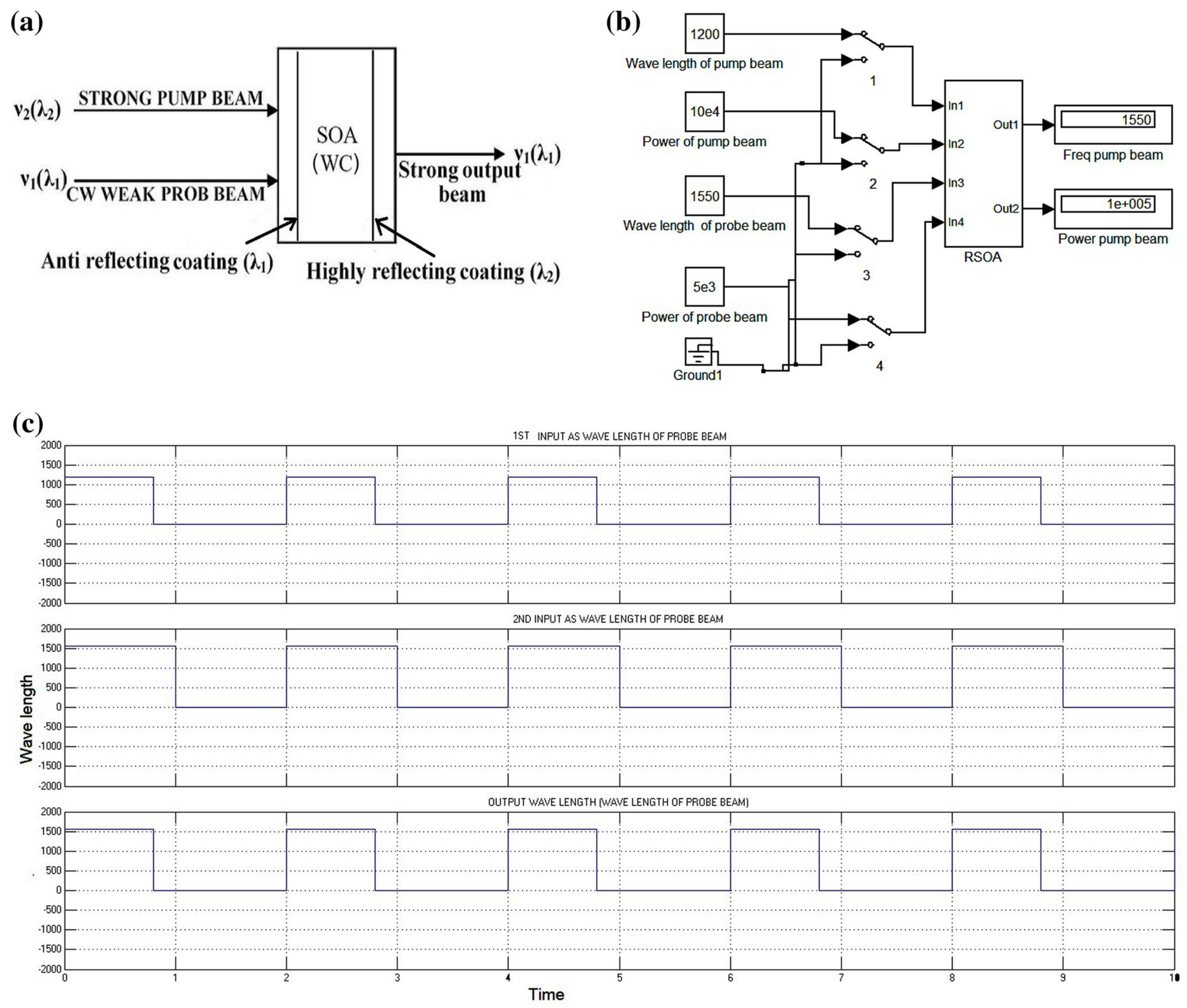


Fig. 1 **a** Input–output state with energized ray path. **b** Simulative model of wavelength conversion. **c** Simulated outcome of wavelength conversion for probe beam. **d** Simulated outcome of power conversion from pump beam

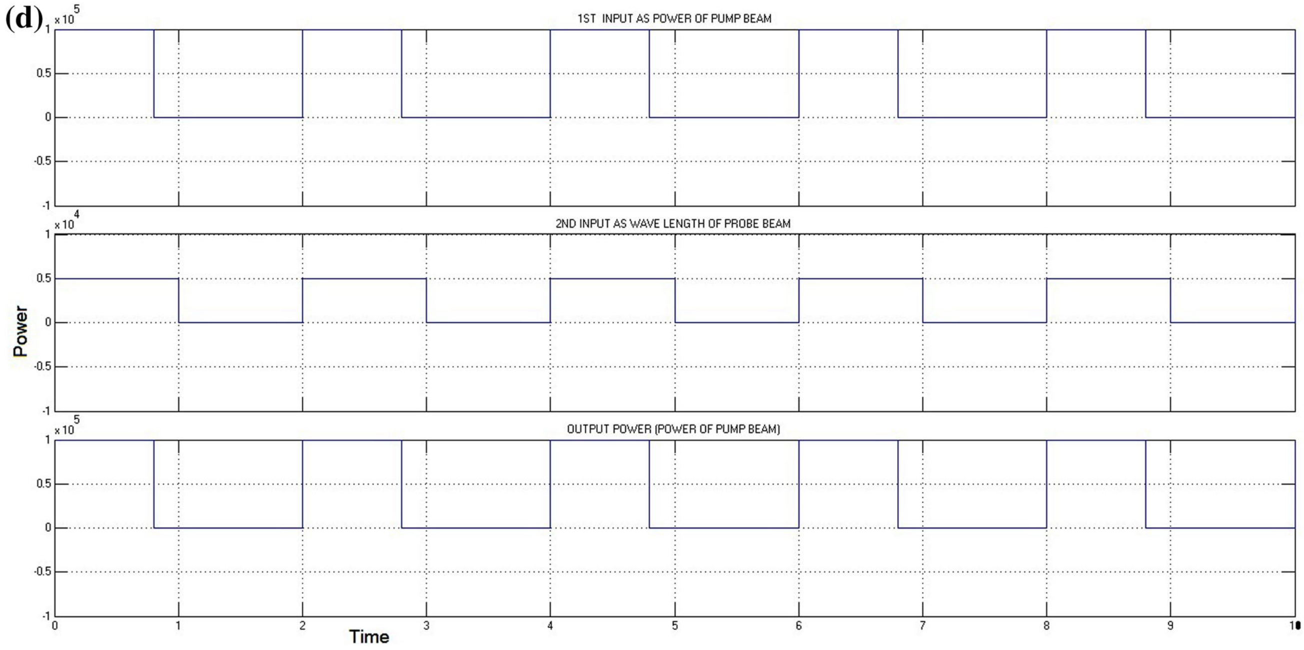
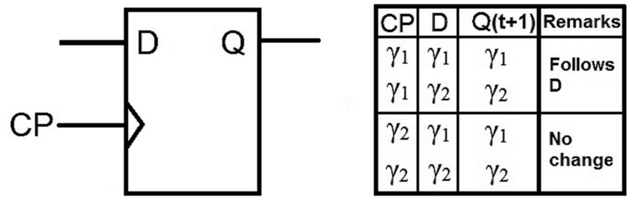


Fig. 1 continued



CP	D	Q(t+1)	Remarks
γ_1	γ_1	γ_1	Follows D
γ_1	γ_2	γ_2	
γ_2	γ_1	γ_1	No change
γ_2	γ_2	γ_2	

Fig. 2 Block diagram with transition table of D flip-flop

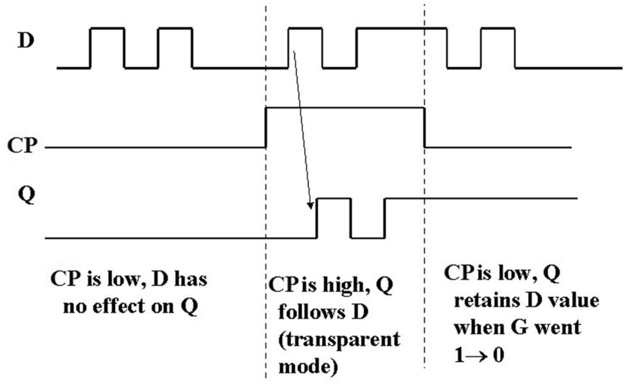


Fig. 3 Timing diagram of D flip-flop

surface at its input side for λ_2 (the corresponding frequency value is γ_2) and a highly reflecting surface for λ_1 (the corresponding frequency value is γ_1), at the output terminal. In this situation, the total power is transferred from the strong pump beam to the weak probe beam, and thus, the weak probe beam being a stronger one (rather being

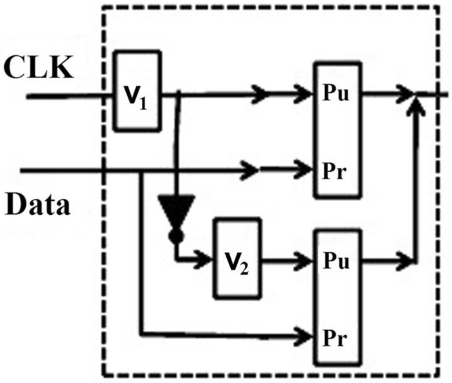


Fig. 4 Clock-enabled active high (γ_1) input section using frequency-encoded SOA

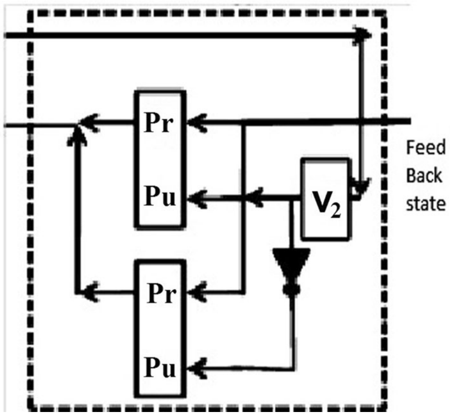


Fig. 5 Clock-enabled active low (γ_2) input section using frequency-encoded SOA

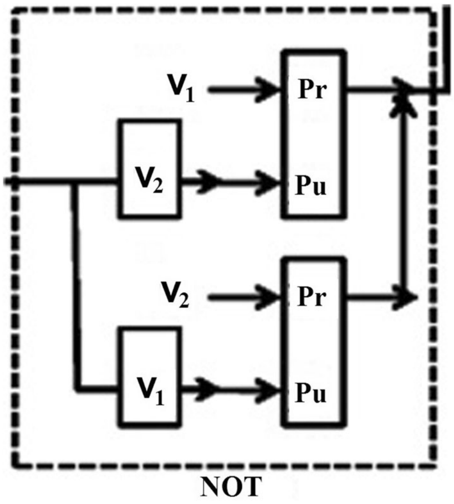


Fig. 6 Subsection for single NOT operation using frequency-encoded SOA

amplified) comes to the output terminal. It provides not only amplification but also frequency encryption in form of desired frequency profile. The scheme is shown in Fig. 1a. If no pump beam exists at the input terminal, no conversion is allowed at the output terminal. These types of switching devices are very much effective in modern communication, where one light signal is switched by another light signal.

Here, in this communication, the authors use the cross-gain modulation character of SOA. A weak CW probe beam light of wavelength say, $\lambda_1 = 1550$ nm with signal power say $= 5 \times 10^3$ W and a strong pump beam of wavelength $\lambda_2 = 1200$ nm with signal power $= 10 \times 10^4$ W are injected to the input terminals of a properly biased SOA. The strong pump beam transfers its total power to the weak probe beam, and then, the weak probe beam becomes stronger and comes out to the output terminal (i.e., at the output it provides the wavelength of the probe beam, here $\lambda_1 = 1550$ nm and the power of the pump beam, here 10×10^4 W), so that the SOA acts as proper wavelength converter. This scheme is shown in Fig. 1b. Also, MATLAB-simulated outcomes for the wavelength conversion for probe beam (1550 nm) and cross-gain modulation from the pump beam (10×10^4 W) are represented in Fig. 1c, d, respectively [8–11].

Principle of D latch

Latch is an input device that is used to hold one-bit information [12–15]. D latch is a device that captures or latches the logic state given on the changes on data (D) line, when the given clock pulse is high. It retains the previous logic state when the clock pulse is low. The block diagram of the D flip-flop with transition table is shown in Fig. 2. This is a very essential digital storage for the realization of one-bit storage, delay, etc. Here, the timing diagram and the truth table for D latch are explained by taking two wavelength values λ_1 (corresponds to frequency γ_1) and λ_2 (corresponds to frequency γ_2) shown in Figs. 2 and 3. Here, frequency γ_1 corresponds to high state and frequency γ_2 corresponds to low state. In the truth table and timing diagram, CP stands for clock pulse input, D stands for data input, Q for output of latch considered.

Implementation of all-optical D latch using SOA block

In this present paper, for the all-optical communication, this essential storage is proposed to design using frequency-encoded SOA. Here, in this schematic, there are four subblocks: They are two clock-enabled input sections (active high and active low) and two sections of NOT gates. Say the frequency of the clock cycle is γ_1 and γ_2. When the clock is at γ_1 state, the subsection shown in Fig. 4 becomes active. As a result, the data given on D line (if it is not matched with γ_1) are passed through the SOA 1 as probe beam and SOA 2 remains inactive (the schematic of active low is shown in Fig. 5); otherwise, for the same state of D and clock state, SOA 2 will be activated and generated the output probe beam. At this clock state γ_1, SOA 3 and SOA 4 will not be activated, as they are biased only for clock state γ_2. So the combination of SOA 1 and SOA 2 is known as clock-enabled active high. The output probe beam from the active high is fed into the next section as pump beam. The next section is a NOT gate combination. The schematic of NOT gate combination is shown in Fig. 6. Depending on the frequency of the output probe beam from the previous section, γ_1 or γ_2, the relevant frequency-encoded SOA that is either SOA 5 or SOA 6 will be activated, by the selective γ_1 or γ_2 filter. As it is connected at pump beam so the other state that is the probe beam frequency is the output. Naturally to hold the exact state of data line, the output probe beam from this NOT combination (SOA 5 and SOA 6) is treated as the pump beam for the next NOT combination (SOA 7 and SOA 8). The data are passed.

Now to retain (or latch) the data in the next clock state that is at γ_2, the data line or the input line will be replaced by feedback line. Because according to the operating principle of D latch in this state, no new updating will be there rather the holding of the previous state. The SOA 3 or SOA 4 becomes active depending on the frequency state of feedback input. The output from the clock-enabled active low state is then fed to the pump beam of first NOT gate section. So output is again the NOT of previous state output. Then, it is passed through another NOT gate section

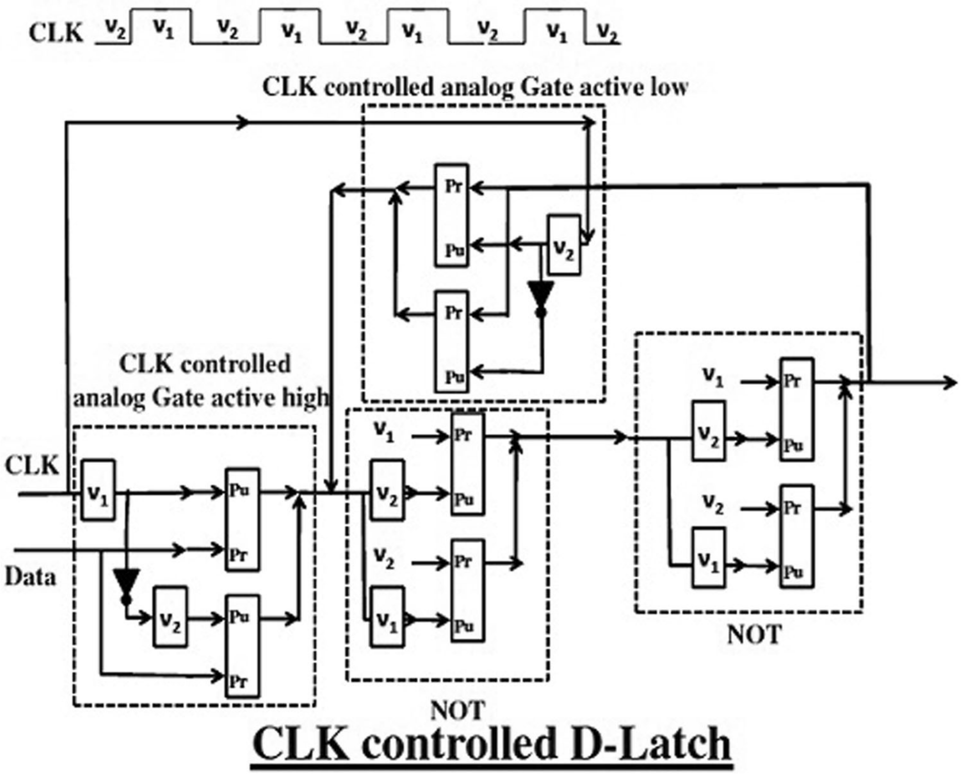


Fig. 7 Four subsections of the schematic of clock-enabled D latch using frequency-encoded SOA

Table 1 The output of the clock-enabled D latch

CLK	Data	SOA 1	SOA 2	O/P	SOA 3	SOA 4	O/P	SOA 5	SOA 6	O/P	SOA 7	SOA 8	Output (latched data)
γ_1	γ_1	Off	On	γ_1	Off	Off	–	Off	On	γ_2	On	Off	Latched
	γ_2	On	Off	γ_2	Off	Off	–	On	Off	γ_1	Off	On	
γ_2	γ_1	Off	Off	–	On (γ_1)	Off	γ_1	Off	On	γ_2	On	Off	No changed
	γ_2	OFF	Off	–	Off	On (γ_2)	γ_2	On	Off	γ_1	Off	On	

and the output is just equivalent to the data, given in the previous clock state. The purpose of the D latch is completed, again the changeover of stored data will happen at the next high clock state. The total schematic of D latch is shown in Fig. 7. The above proposal which is discussed to pass or retain the data to fulfil the criteria of D flip-flop are shown in Table 1.

MATLAB-simulated results of the clock-enabled D latch

The graphical output for the D flip-flop, using MATLAB, is shown in Fig. 8.

Principle of Toggle flip-flop

The T flip-flop has two possible values. When $T = 0$, the flip-flop does a hold. A hold means that the output is kept the same as it was before the clock edge. When $T = 1$, the flip-flop does a Toggle, which means the output is negated after the clock edge, compared to the value before the clock edge. Here, the timing diagram and the truth table for T latch are explained by taking two wavelength values λ_1 (corresponds to frequency γ_1) and λ_2 (corresponds to frequency γ_2) shown in Figs. 9 and 10. Thus, in a T flip-flop, one can either maintain the current state's value for another cycle or can Toggle the value (negate it) at the next clock edge.

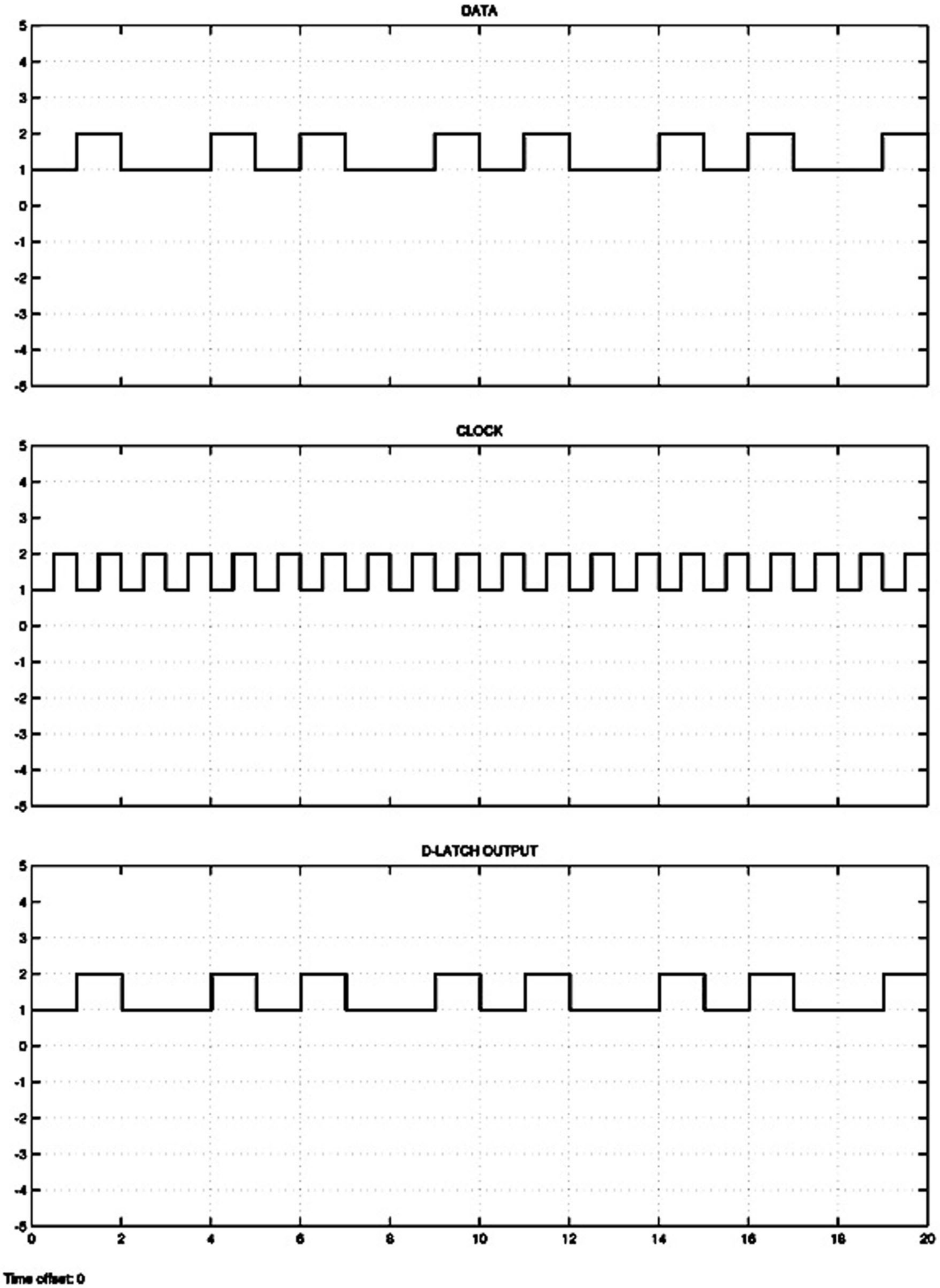
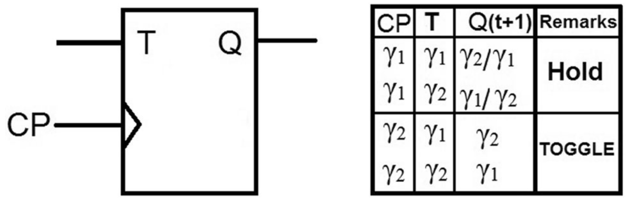


Fig. 8 Simulink output of timing diagram for D flip-flop



CP	T	Q(t+1)	Remarks
γ_1	γ_1	γ_2/γ_1	Hold
γ_1	γ_2	γ_1/γ_2	
γ_2	γ_1	γ_2	TOGGLE
γ_2	γ_2	γ_1	

Fig. 9 Block diagram with transition table of T flip-flop

Implementation of all-optical T flip-flop by SOA

The basics of T flip-flop are programmed using two D latches and NOT gate. This is shown in Fig. 11. Two D latches are connected in cascade but with opposite clock states. Say the clock cycles or states are expressed in terms γ_1 and γ_2. The D latches are designed in such a way that they act as active high that is changes output at clock state γ_1 and latches at clock state γ_2. So at clock state γ_1, the D latch 1 is active, D latch 2 remains inactive (because of clock state γ_2); rather, it remains in the previous output. So it latches or retains the previous state (γ_2 or γ_1). That means the outcome is latched or holds data.

Now when the clock is in γ_2 state, D latch 1 remains inactive but D latch 2 becomes active. Then, these data are inverted and passed toward the input. According to the principle of T flip-flop here, the data are either stored or toggled according to two different clock states. This is explained in Table 2.

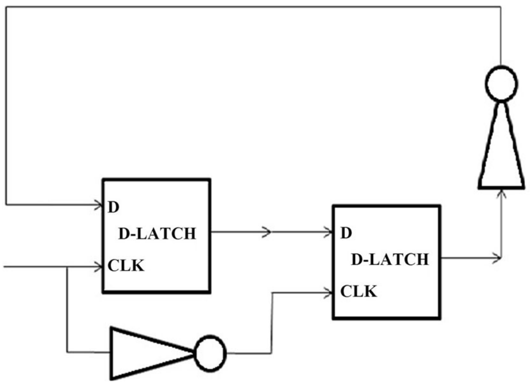


Fig. 11 Schematic diagram of Toggle flip-flop

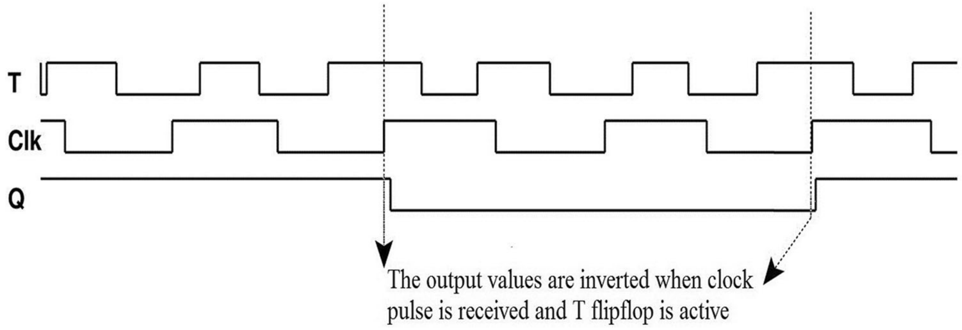
Simulated results of the clock-enabled T flip-flop

The graphical output for the T flip-flop, using MATLAB, is shown in Fig. 12.

Conclusions

The result of the above-mentioned proposed schemes to realize optical D latch and T latch in all-optical domains is verified using MATLAB software. Here, advantages of frequency encoding as well as cross-gain modulation techniques are exploited to realize the all-optical operations. This technique gives not only a reliable and realistic operation but also it supports to hold or change the input data according to applied clock states. This encoding technique will help for implementation of memory device,

Fig. 10 Timing diagram of T flip-flop



The output values are inverted when clock pulse is received and T flipflop is active

Table 2 The output of the clock-enabled T flip-flop

Clock	Data input	D latch 1	Clock (NOT)	D latch 2	Output	Inverted output	Remarks
γ_1	γ_1	c	γ_2	Latched	Hold	γ_2/γ_1	Hold
	γ_2	γ_2		Latched	Hold	γ_1/γ_2	
γ_2	γ_1	Latched	γ_1	γ_1	Reset	γ_2	Toggle
	γ_2	Latched		γ_2	Reset	γ_1	

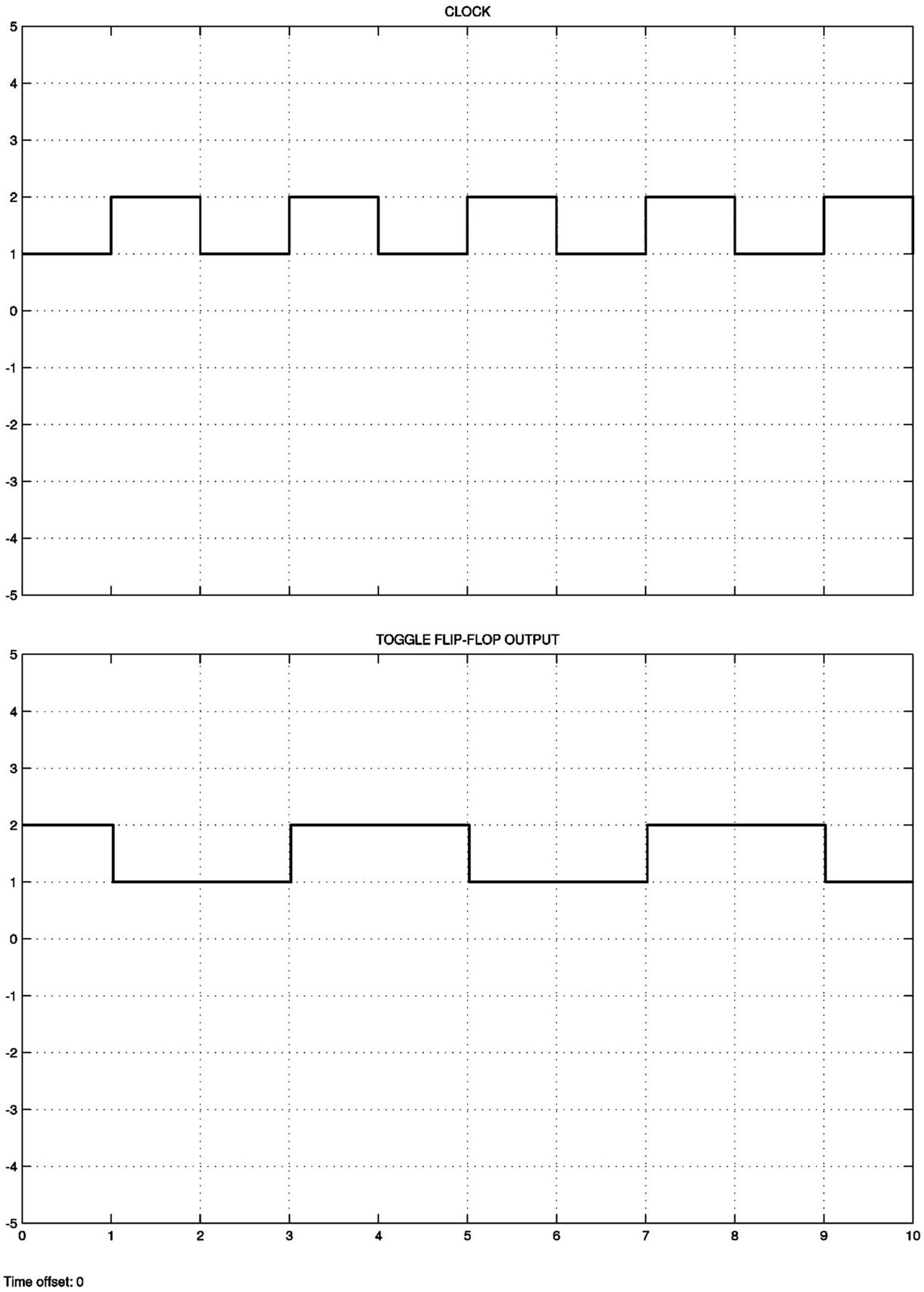


Fig. 12 Simulink output of timing diagram for T flip-flop

data encryption using parity bit, in all-optical domain, with faithful and reliable results.

References

1. A.K. Ghosh et al., Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic. Opt. Laser Technol. **44**(5), 1583–1592 (2012). https://doi.org/10.1016/j.optlastec.2011.11.044
2. P.P. Sarkar, B. Ghosh, S.N. Patra, Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer. J. Opt. Technol. **83**, 257–262 (2016). https://doi.org/10.1364/JOT.83.000257
3. S. Mukhopadhyay, Role of optics in super-fast information processing. Indian J. Phys. **84**(8), 1069–1074 (2010)
4. B. Ghosh, R.R. Pal, S. Mukhopadhyay, An all-optical integrated system for implementing arithmetic operation in 2's complement method with the active participation of non-linear material based switches. Indian J. Phys. **84**(8), 1101–1109 (2010). https://doi.org/10.1007/s12648-010-0105-0
5. P.P. Sarkar, B. Satpati, S. Mukhopadhyay, Verification of all optical frequency encoded OR logic operation with its simulated result. Int. J. Electron. Commun. Technol. **4**(1, Spl 1), 86–88 (2013)
6. S. Chen, Y. Shi, S. He, D. Dai, Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon. IEEE Photonics Technol. Lett. **28**(17), 1874–1877 (2016). https://doi.org/10.1109/LPT.2016.2574459
7. B. Ghosh et al., A novel approach to realize of all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches with simulated verification. Opt. Spectrosc. **124**(3), 337–342 (2018). https://doi.org/10.1134/S0030400X1803013X
8. S. Saha, S. Biswas, S. Mukhopadhyay, Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach-Zehnder interferometer-based semiconductor optical amplifier. IET Optoelectron. **11**(5), 201–207 (2017). https://doi.org/10.1049/iet-opt.2016.0078
9. J. Wang, L.R. Chen, Low crosstalk Bragg grating/Mach-Zehnder interferometer optical add-drop multiplexer in silicon photonics. Opt. Express **23**(20), 26450–26459 (2015). https://doi.org/10.1364/OE.23.026450
10. L.Q. Guo, M.J. Connelly, A poincare approach to investigate nonlinear polarization rotation in semiconductor optical amplifiers and its applications to all-optical wavelength conversion. Proc. SPIE **6783**(678325), 1–5 (2007)
11. P.P. Sarkar, B. Satpati, S. Mukhopadhyay, New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors. J. Opt. **42**(4), 360–366 (2013). https://doi.org/10.1007/s12596-013-0133-1
12. S. Zhang, Z. Li, Y. Liu, R. Geldenhuys, H. Ju, D. Lenstra, G.D. Khoe, J.S. Dorren, Optical shift register based on an optical flip-flop memory with a single active element. in *31st European Conference on Optical Communication*, 2005. ECOC 2005, vol. 232, pp. 233–234 (2005)
13. Y. Liu, M.T. Hill, H. de Waardt, G.D. Khoe, D. Lenstra, H.J.S. Dorren, All-optical flip-flop memory based on two coupled polarisation switches. Electron. Lett. **38**, 904–906 (2002). https://doi.org/10.1049/el:20020640
14. D.K. Gayen, T. Chattopadhyay, K.E. Zoiros, All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach-Zehnder interferometer. J. Comput. Electron. **14**(1), 129–138 (2015). https://doi.org/10.1007/s10825-014-0632-6
15. M. Connelly, *Semiconductor optical amplifiers and their applications* (University of Limerick, Limerick, 2003)

JCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Vol.7, Special Issue.1, Jan 2019 E-ISSN: 2347-2693

An alternative approach to realize all optical frequency encoded integrated AND-OR logic gate with control input using optical switches and its simulative verification.

B. Ghosh[1], N. Halder[2], D. Roy[3], S. Hazra[4], S. Mukherjee[5], PP. Sarkar[6*]

[1, 2, 3, 4, 6]Department of Electronics and Communication Engineering, University Institute of Technology,
University of Burdwan, Burdwan, West Bengal, India
[5]Department of AEIE, Murshidabad College of Engineering & Technology, Murshidabad, West Bengal, India

Corresponding Author: pratim34@gmail.com

Abstract— Optics has been recognizing as a good probable signal for realization of logic circuits, digital optical systems for optical communication and computation using optical switching devices for the utilization of super fast speed. Some optical logic gates can operate on the basis of frequency conversion process of some nonlinear materials. Semiconductor optical amplifier is recognized as a very promising and reliable optical device for implementing various all optical logical operations. Recently, more and more advanced technology should be needed to design compact and integrated version of devices. Here the authors have proposed an alternative approach to realize frequency encoded all optical integrated AND - OR logic gate with control input by which a single circuit operates on different logics using reflected semiconductor optical amplifier and add/drop multiplexer type optical switches. Again, this scheme of all optical frequency encoded integrated logic gate using optical switches with controlling input is successfully verified by proper simulation technique.

Keywords—Semiconductor Optical Amplifier, Reflected Semiconductor Optical Amplifier, Add/Drop Multiplexer, Pump Beam, Probe Beam

I. INTRODUCTION

Photon can be used as more suitable information carrier than electron in super-fast information processing, due to its very high speed of operation. For realization of all optical different logical and arithmetical digital devices [1] need different encoding techniques like, frequency [2], intensity, phase, spatial and polarization encodings [3]. Frequency encoding principle is the most reliable technique because frequency of light beam remains unchanged under reflection, refraction, absorption etc. At the time of frequency encoding, two different frequencies of light beams represent two different states of information. Here, presence of light beam of υ_1 frequency is treated as digital logic state '0' and light beam of υ_2 frequency is considered as digital logic state '1'. Now, optical switches like add/drop multiplexer (ADM) [4-7] and reflected semiconductor optical amplifier (RSOA) [8-11] are used to design all optical circuits. Add/drop multiplexer (ADM) is a frequency selecting optical switching device. If ADM is biased by a light beam of particular frequency then the particular frequency of light beam is reflected by ADM if it is coming from input and passes all other frequency of light beam. Opposite incident happens if the biasing is changed. Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device, where a weak probe beam with a frequency and a strong pump beam with another frequency are inserted to the input terminals of RSOA. Then this switch will give light beam of frequency of probe beam with power of the pump beam. Therefore RSOA and ADM could be recognized as very useful optical switches for implementing many all optical logical operations.

Here, the authors have proposed a different approach to realize frequency encoded integrated AND-OR logic gate with a control input for selecting particular logic operation with the help of RSOA and ADM. This scheme is successfully implemented on integrated AND-OR logic operations with a single circuit just altering the control input. Also the truth tables have been verified with the simulation result.

The paper is organized as follows, Section I contains the introduction, Section II contains the Scheme of realization of the integrated logic gate, Section III contains the Simulation process of the scheme of integrated logic gate, Section IV contains Results and Discussion and section V mentions conclusions.

II. SCHEME OF REALIZATION OF THE INTEGRATED LOGIC GATE

Here, Two input terminals 'A' and 'B', control input terminal 'C' and one controlled output terminal 'Y' are used to implement the controlling logic unit, which is shown in Figure 1. Now, this scheme of unit provides output as AND as well as OR logic depending upon the control input states of light beam of υ_1 (or digital state '0') and υ_2 (or digital state '1') frequencies.

A. Scheme acts as AND logic gate

Here, light beam of υ_1 frequency (or digital state '0') is applied to the control input terminal 'C' for realizing this scheme acts as AND logic gate.

1) At first, light beam of υ_1 frequency (or digital state '0') is given to both the input terminals of 'A' and 'B'. So, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 because ADM_1 is biased by υ_2 frequency and this light beam of υ_1 frequency goes as probe beam of $RSOA_2$ and one part of this beam is coming as probe beam of $RSOA_5$. Again, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 as it is biased by υ_2 frequency and one part of this beam goes as probe beam of $RSOA_6$ but other part acts as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_1$ provides light beam of υ_2 frequency, which will act as pump beam of $RSOA_2$. So, $RSOA_2$ will give light beam of υ_1 frequency (or digital state '0') to the controlled output terminal 'Y' because light beam of υ_1 frequency is present as probe beam of $RSOA_2$. But $RSOA_5$ does not work as there is no pump beam coming from circulator 'C_2'. Similarly, $RSOA_3$ (with constant probe beam of υ_1 frequency) does not work as there is no pump beam coming from circulator 'C_2'. Since $RSOA_3$ does not work then $RSOA_4$ does not work. Again $RSOA_6$ does not have any pump beam coming from circulator 'C_1'. So $RSOA_6$ does not work. Though light beam of υ_1 frequency coming from control input terminal 'C', acts as a biasing of ADM_3, ADM_3 does not provide any light beam because $RSOA_5$ and $RSOA_6$ do not work. As there is no pump beam of $RSOA_7$ (with constant probe beam of υ_2 frequency) coming from ADM_3, $RSOA_7$ does not work. Actually, some particular RSOA or ADM blocks do not work for respective input combinations. So, only $RSOA_2$ will give light beam of υ_1 frequency (or digital state '0') to the controlled output terminal 'Y'. It is theoretically satisfied by the first input combination of truth table of AND logic gate, which is given in the Table 1.

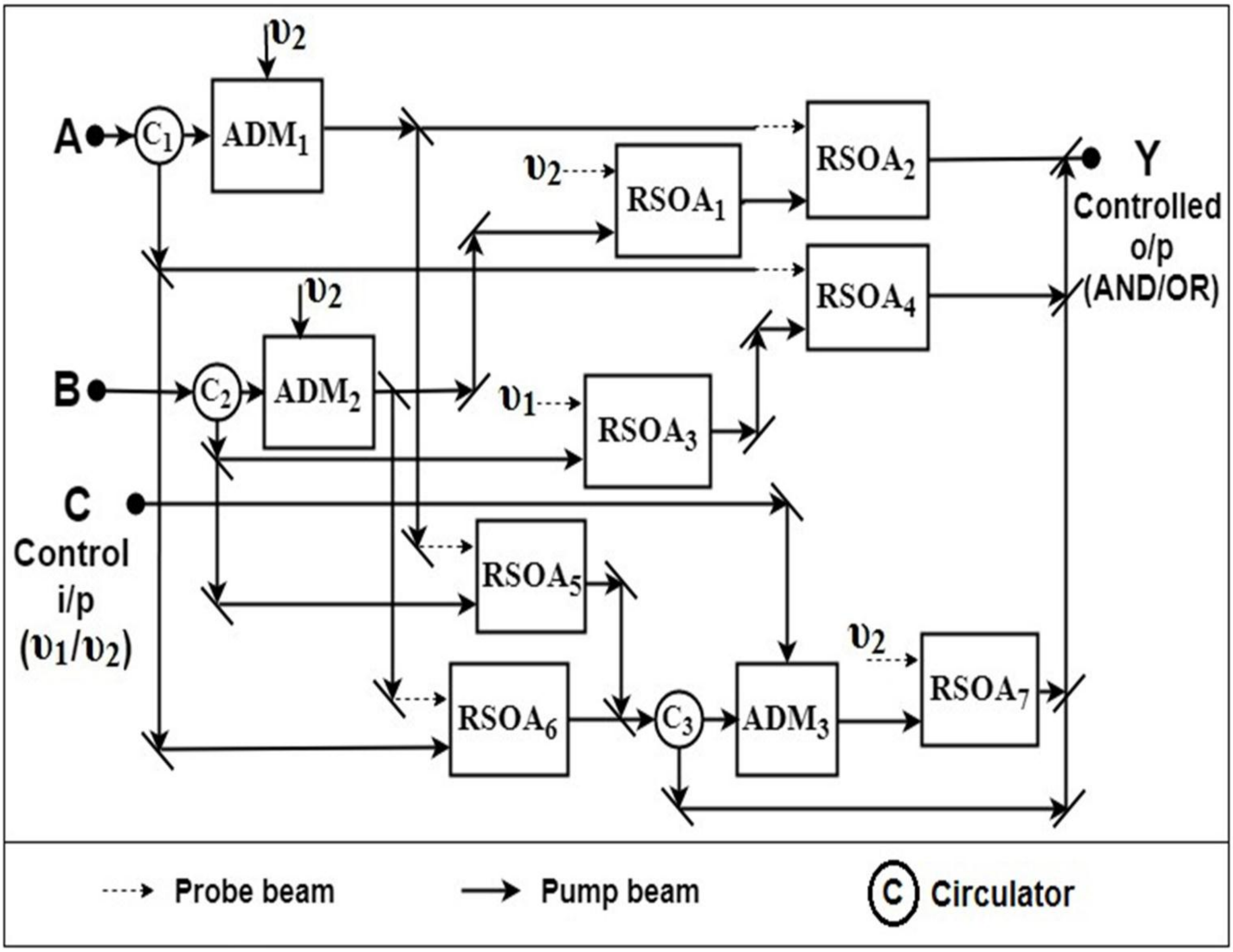


Figure 1. Block diagram of the scheme of integrated logic gate

2) Now, light beam of υ_1 (or digital state '0') and υ_2 (or digital state '1') frequencies are given to the input channels of 'A' and 'B' respectively. By the similar way, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 and goes as probe beam of $RSOA_2$ and other part of this beam is coming as probe beam of $RSOA_5$. But, light beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 (biased by υ_2 frequency) and one part of this reflected beam goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ gives light beam of υ_1 frequency, which will act as pump beam of $RSOA_4$. Now, other part of the reflected beam of ADM_2 comes as pump beam of $RSOA_5$. Thus, $RSOA_5$ provides light beam of υ_1 frequency because light beam of υ_1 frequency is present as probe beam of $RSOA_5$. Now, this beam is entering to the ADM_3 which is biased by υ_1 frequency, coming from control input terminal 'C'. So, light beam of υ_1 frequency (or digital state '0') is reflected by ADM_3 and goes to the controlled output terminal 'Y'. Other RSOAs and ADMs do not work for absence of sufficient light beams.

3) Here, light beam of υ_2 (or digital state '1') and υ_1 (or digital state '0') frequencies are inserted to the input channels of 'A' and 'B' respectively. Therefore, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 (biased by υ_2 frequency) and this beam goes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Now, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 (biased by υ_2 frequency) and one part of this beam goes as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Thus, $RSOA_1$ provides light beam of υ_1 frequency as pump beam of $RSOA_2$. But, other part of the beam, coming from ADM_2, goes as probe beam of $RSOA_6$. Since light beam of υ_2 frequency is present as pump beam, $RSOA_6$ gives light beam of υ_1 frequency to the ADM_3 (biased by υ_1 frequency, coming from control input terminal 'C'). As a result, light beam of υ_1 frequency (or digital state '0') is reflected by ADM_3 and goes to the controlled output terminal 'Y'. Other RSOAs and ADMs do not work for lack of proper light beams.

4) Lastly, light beam of υ_2 frequency (or digital state '1') is given to both the input channels of 'A' and 'B' simultaneously. So, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM_1 which is biased by υ_2 frequency and one part of this beam goes as probe beam of $RSOA_4$ and other part of the reflected beam comes as pump beam of $RSOA_6$. Again, light beam of υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 and one part of the reflected beam comes as pump beam of $RSOA_5$. Whereas other part of this reflected beam goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ provides light beam of υ_1 frequency, which will proceed as pump beam of $RSOA_4$. As a result, $RSOA_4$ provides light beam of υ_2 frequency (or digital state '1') to the controlled output terminal 'Y' because light beam of υ_2 frequency is present as probe beam of $RSOA_4$. Other RSOAs and ADMs do not work due to absence of sufficient light beams though light beam of υ_1 frequency coming from control input terminal 'C', acts as a biasing of ADM_3.

Table 1. Truth table of the scheme acts as AND logic gate

First input (or Digital form) at channel 'A'	**Second input (or Digital form) at channel 'B'**	**Control input (or Digital form) at terminal 'C'**	**Controlled output terminal 'Y'**
$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_1(0)$	$\upsilon_1(0)$
$\upsilon_1(0)$	$\upsilon_2(1)$		$\upsilon_1(0)$
$\upsilon_2(1)$	$\upsilon_1(0)$		$\upsilon_1(0)$
$\upsilon_2(1)$	$\upsilon_2(1)$		$\upsilon_2(1)$

By this way, after observing the logic output from the controlled output terminal 'Y' for these four input combinations, we can say that, the logic output fully satisfies the truth table of AND logic gate, for control input terminal 'C' as constant light beam of υ_1 frequency (or digital state '0'). This is shown in Table 1.

B. Scheme acts as OR logic gate

For this case, light beam of υ_2 frequency (or digital state '1') is inserted to the control input terminal 'C' for realizing this scheme works as OR logic gate.

1) Here, at first, light beam of υ_1 frequency (or digital state '0') is given to both the input channels of 'A' and 'B' simultaneously. Thus, light beam of υ_1 frequency, coming from terminal 'A' is passed by ADM_1 (biased by υ_2 frequency) and goes as probe beam of $RSOA_2$ and another part of this beam is coming as probe beam of $RSOA_5$. Similarly, light beam of υ_1 frequency, coming from terminal 'B' is passed by ADM_2 (biased by υ_2 frequency) and one part of this beam goes as probe beam of $RSOA_6$. But other part acts as pump beam of $RSOA_1$, which has constant probe beam of υ_2 frequency. Therefore, $RSOA_1$ provides light beam of υ_2 frequency, which will act as pump beam of $RSOA_2$. So, $RSOA_2$ will give light beam of υ_1 frequency. $RSOA_5$ does not work due to absent of pump beam coming from circulator 'C_2'. And $RSOA_6$ is stop for the absence of pump beam coming from circulator 'C_1'. So, there is no light beam for the input of ADM_3 even if light beam of υ_2 frequency coming from control input terminal 'C', which acts as a biasing of ADM_3. Therefore, ADM_3 does not provide any light beam for the pump beam of $RSOA_7$ (with constant light beam of υ_2 frequency). So, $RSOA_7$ does not work. Again, $RSOA_3$ (with constant probe beam of υ_1 frequency) does not work as there is no pump beam coming from circulator 'C_2'. Since $RSOA_3$ does not work then $RSOA_4$ does not work. Therefore, light beam of υ_1 frequency (or digital state '0') from $RSOA_2$ goes to the controlled output terminal 'Y'. It is satisfied by the first input combination of truth table of OR logic gate, which is given in the Table 2.

2) Now, light beam of υ_1 (or digital state '0') and υ_2 (or digital state '1') frequencies are inserted to the input channels of 'A′ and 'B' respectively. Then, υ_1 frequency, coming from terminal 'A' is passed by ADM_1 and one part goes as probe beam of $RSOA_2$ and other part is coming as probe beam of $RSOA_5$. But, υ_2 frequency, coming from terminal 'B' is reflected by ADM_2 which is biased by υ_2 frequency and one part goes as pump beam of $RSOA_3$, which has constant probe beam of υ_1 frequency. So, $RSOA_3$ gives light beam of υ_1 frequency, which will act as pump beam of $RSOA_4$. Now, other part of the reflected beam of

ADM$_2$ comes as pump beam of RSOA$_5$. Thus, RSOA$_5$ provides υ_1 frequency because υ_1 frequency is present as probe beam of RSOA$_5$. Now, the beam, coming from RSOA$_5$, proceeds to the ADM$_3$ which is biased by υ_2 frequency, coming from control input terminal 'C'. So, υ_1 frequency is passed by ADM$_3$ and goes as pump beam of RSOA$_7$, which has constant probe beam of υ_2 frequency. Therefore, RSOA$_7$ provides υ_2 frequency (or digital state '1') to the controlled output terminal 'Y'. Other RSOAs and ADMs do not work for absence of sufficient light beams.

3) Next, light beam of υ_2 (or digital state '1') and υ_1 (or digital state '0') frequencies are inserted to the input channels of 'A' and 'B' respectively. Therefore, light beam of υ_2 frequency, coming from terminal 'A' is reflected by ADM$_1$ which is biased by υ_2 frequency and one part goes as probe beam of RSOA$_4$ and other part comes as pump beam of RSOA$_6$. Now, υ_1 frequency, coming from terminal 'B' is passed by ADM$_2$ which is biased by υ_2 frequency and one part of this beam goes as pump beam of RSOA$_1$, which has constant probe beam of υ_2 frequency. Thus, RSOA$_1$ provides υ_1 frequency as pump beam of RSOA$_2$. But, other part of the beam, coming from ADM$_2$, goes as probe beam of RSOA$_6$. Since there is a light beam of υ_2 frequency is present as pump beam, RSOA$_6$ gives υ_1 frequency to the ADM$_3$ (biased by υ_2 frequency, coming from control input terminal 'C'). As a result, υ_1 frequency (or digital state '0') is passed by ADM$_3$ and proceeds as pump beam of RSOA$_7$, which has constant probe beam of υ_2 frequency. Therefore, RSOA$_7$ provides υ_2 frequency (or digital state '1') to the controlled output terminal 'Y'. Remaining RSOAs and ADMs do not work for lack of proper light beams.

4) Finally, light beam of υ_2 frequency (or digital state '1') is set to both the input channels of 'A' and 'B' simultaneously. Thus, υ_2 frequency, coming from terminal 'A' is reflected by ADM$_1$ (biased by υ_2 frequency) and one part of this beam goes as probe beam of RSOA$_4$ and other part of the reflected beam comes as pump beam of RSOA$_6$. Again, υ_2 frequency, coming from terminal 'B' is reflected by ADM$_2$ and one part of the reflected beam comes as pump beam of RSOA$_5$. While another part of this reflected beam goes as pump beam of RSOA$_3$, which has constant probe beam of υ_1 frequency. So, RSOA$_3$ provides υ_1 frequency, which will proceed as pump beam of RSOA$_4$. As a result, RSOA$_4$ provides υ_2 frequency (or digital state '1') to the controlled output terminal 'Y' because υ_2 frequency is present as probe beam of RSOA$_4$. Other RSOAs and ADMs do not work for lack of sufficient light beams despite the fact that light beam of υ_2 frequency coming from control input terminal 'C', acts as a biasing of ADM$_3$.

In this way, the logic output coming from the controlled output terminal 'Y' satisfies the truth table of OR logic gate after analysing four input combinations for control input terminal 'C' as constant light beam of υ_2 frequency (or digital state '1') which is shown in Table 2.

Table 2. Truth table of the scheme acts as OR logic gate

First input (or Digital form) at channel 'A'	**Second input (or Digital form) at channel 'B'**	**Control input (or Digital form) at terminal 'C'**	**Controlled output terminal 'Y'**
υ_1 (0)	υ_1 (0)	υ_2 (1)	υ_1 (0)
υ_1 (0)	υ_2 (1)		υ_2 (1)
υ_2 (1)	υ_1 (0)		υ_2 (1)
υ_2 (1)	υ_2 (1)		υ_2 (1)

III. SIMULATION PROCESS OF THE SCHEME OF INTEGRATED LOGIC GATE

MATLAB (R2008a) simulink tools have been used for simulation of all optical frequency encoded integrated two input AND-OR logic gate with a control input using optical switches (RSOA and ADM). "I/P 1", "I/P 2", "Control i/p" and " O/P" terminals are used for applying proper inputs and getting proper output. In simulation process, for providing the two frequency states, υ_1 frequency (or, digital state '0') and υ_2 frequency (or, digital state '1') are represented by '3' and '8' respectively. Maintaining the similarity of the block diagram (shown in Figure 1) simulative model of the integrated scheme when acts as AND logic gate is shown in Figure 2 keeping control input as υ_1 frequency or '3'. Another simulative model of the integrated scheme when acts as OR logic gate is also shown in Figure 3 keeping control input as υ_2 frequency or '8'.

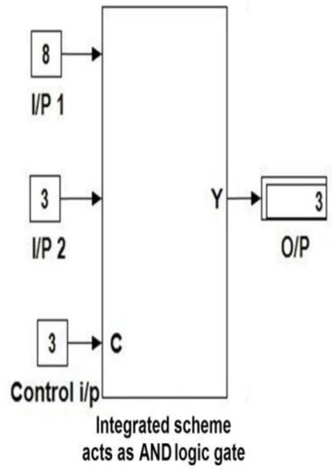


Figure 2. Simulative model of the integrated scheme when acts as AND logic gate

At first, each of the RSOA blocks is properly programmed according to the RSOA mechanism. There are two inputs "pr" for probe beam and "pm" for pump beam and the output "y" in RSOA blocks. According to the theory of RSOA, if we represent pump beam as "3 peta Hz" = υ_1 = digital logic state "0" and probe beam as "8 peta Hz" = υ_2 = digital logic state "1" for understanding the simulation process, then we get "8 peta Hz" at the output terminal of RSOA blocks. The output changes if pump beam and probe beam are altered accordingly.

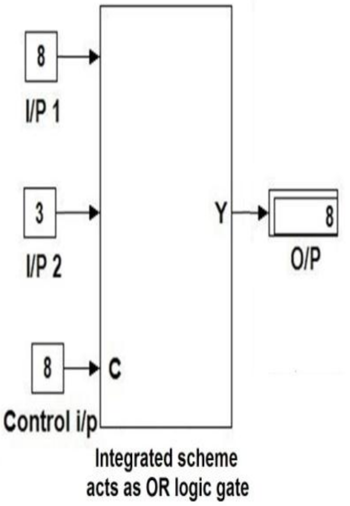


Figure 3. Simulative model of the integrated scheme when acts as OR logic gate

Also, ADM block has been simulated such a way that, it obeys the proper mechanism of ADM. Now, if ADM is biased by a particular light beam frequency, say “3 peta Hz” = υ_1 = digital logic state “0” at “bias” terminal, then this block drops the frequency coming from “input” terminal to “drop” terminal and passes other frequency, say “8 peta Hz” υ_2 = digital logic state “1” to “out” terminal. If the biasing is changed, opposite incident happens.

Finally, RSOA and ADM blocks have been connected in proper way for modelling of the simulative model, which are shown in Figure 4, maintaining the similarity of the theoretical block diagrams in Figure 1.

IV. RESULTS AND DISCUSSION

Now, any input combination must be taken into consideration for satisfying the above integrated scheme of all optical digital circuit. If we apply ‘8’ & ‘3’ at “I/P 1” & “I/P 2”, and ‘3’ is inserted to “Control i/p” then we can get ‘3’ at the “O/P” (shown in Figure 2). So, this integrated simulative model satisfies truth table of AND logic which is shown in Table 1. But, when ‘8’ is inserted to “Control i/p” then we can get ‘8’ at the “O/P” (shown in Figure 3). Therefore, we can say that, this integrated model satisfies truth table of OR logic which is shown in Table 2. This integrated simulative model can also be satisfied by the other input combinations of the truth tables of respective AND and OR logic gates.

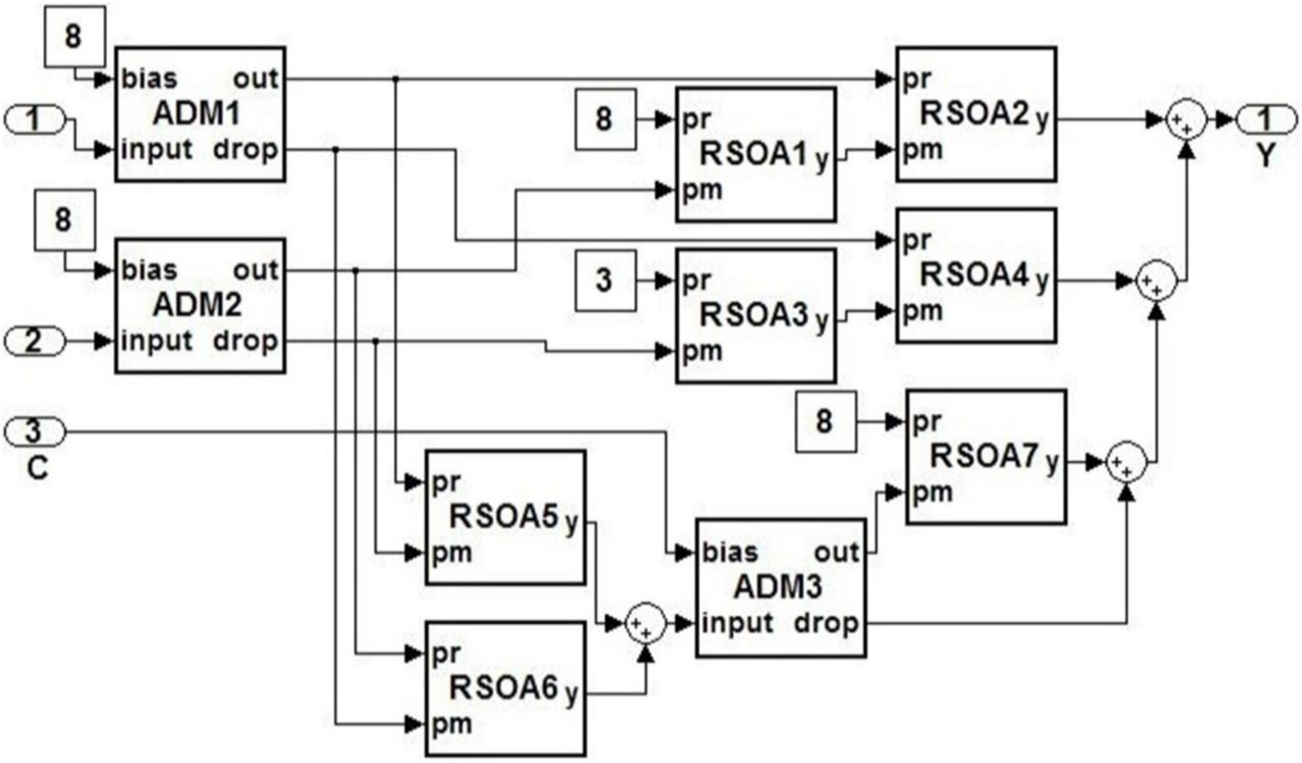


Figure 4. Internal simulative model of the integrated scheme

V. CONCLUSIONS

The simulative verification satisfies this integrated AND-OR logic gate with control input. For that reason its functionality can be utilized directly or indirectly for developing and verifying the performances of other optical frequency encoded digital arithmetic and logic circuits. Also, one can implement various schemes of all optical integrated logic and arithmetic circuits using this technique for optical computation. With the advancement of circuit integration complexity, it may be easy to construct advanced optical computer by combining several all optical digital devices or circuits in near future. The control input provides the opportunity for selecting particular logic operation of the integrated scheme of all optical logic circuits.

REFERENCES

[1] Vinita, "A Comprehensive Review of Recent Advancement in Optical Communication Networks", International Journal of Computer Sciences and Engineering, Vol.6, Issue.9, pp.617-626, 2018.

[2] B. Ghosh, et al. "A Novel Approach to Realize of All Optical Frequency Encoded Dibit Based XOR and XNOR Logic Gates Using Optical Switches with Simulated Verification", Optics and Spectroscopy, Vol.124, Issue.3, pp.337-342, 2018.

[3] C. Taraphdar, T. Chattopadhyay, J.N. Roy, "Polarization encoded all-optical ternary Max gate", In the Proceedings of the 4th International Conference on Computers and Devices for Communication, Kolkata, India, pp.1–4, 2009.

[4] I.S. Amiri, S.E. Alavi, M. Bahadoran, A. Afroozeh, H. Ahmad, "Nanometer bandwidth soliton generation and experimental transmission within nonlinear fiber optics using an add-drop filter system", Journal of Computational and Theoretical Nanoscience, Vol.12, Issue.2, pp.221-225, 2015.

[5] S. Chen, Y. Shi, S. He, D. Dai, "Compact eight-channel thermally reconfigurable optical add/drop multiplexers on silicon", IEEE Photonics Technology Letters, Vol.28, Issue.17, pp.1874-1877, 2016.

[6] J. Wang, L.R. Chen, "Low crosstalk Bragg grating/Mach-Zehnder interferometer optical add-drop multiplexer in silicon photonics", Optics express, Vol.23, Issue.20, pp.26450-26459, 2015.

[7] R. Mansoor, S. Koziel, H. Sasse, A. Duffy, "Crosstalk suppression bandwidth optimisation of a vertically coupled ring resonator add/drop filter", IET Optoelectronics, Vol.9, Issue.2, pp.30-36, 2015.

[8] S. Saha, S. Biswas, S. Mukhopadhyay, "Optical scheme of conversion of a positionally encoded decimal digit to frequency encoded Boolean form using Mach–Zehnder interferometer-based semiconductor optical amplifier", IET Optoelectronics, Vol.11, Issue.5, pp.201-207, 2017.

[9] S. Singh, S. Kaur, R. Kaur, R.S. Kaler, "Photonic processing of all-optical Johnson counter using semiconductor optical amplifiers", IET Optoelectronics, Vol.11, Issue.1, pp.8-14, 2016.

[10] D.K. Gayen, T. Chattopadhyay, K.E. Zoiros, "All-optical D flip-flop using single quantum-dot semiconductor optical amplifier assisted Mach–Zehnder interferometer", Journal of Computational Electronics, Vol.14, Issue.1, pp.129-138, 2015.

[11] Q. Cheng, A. Wonfor, J.L. Wei, R.V. Penty, I.H. White, "Demonstration of the feasibility of large-port-count optical switching using a hybrid Mach–Zehnder interferometer–semiconductor optical amplifier switch module in a recirculating loop", Optics letters, Vol.39, Issue.18, pp.5244-5247, 2014.

Authors Profile

Mr. B Ghosh pursed Bachelor of Engineering from University Institute of Technology, University of Burdwan, Burdwan in 2011 and Master of Engineering from University of Burdwan in 2014. He is currently pursuing Ph.D. and working as Part–time Guest Lecturer in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, since 2014. He has published around 10 research papers in peer-reviewed journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE. His main research work focuses on Optical computation, Semiconductor optical amplfier and photonics. He has 5 years of teaching experience and 3 years of Research Experiences.

Mr. N Halder pursed Master of Engineering from IIT, Kharagpur in year 2011. He is currently pursuing Ph.D. also working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan since 2012. He has published around 10 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and international conferences. His main research work focuses on Image Processing and Sensors. He has 6 years of teaching experience and 4 years of Research Experiences.

Dr. D Roy pursed Ph.D. from IIT, Kharagpur and currently working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan since 2012. He has published around 20 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE. His main research work focuses on Nanoelectronics and Microelectronics. He has 6 years of teaching experience and 6 years of Research Experiences.

Mr. S Hazra pursed Master of Technology from University of Burdwan in 1999. She is currently pursuing Ph.D. and working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan since 2002. She has published around 5 research papers in reputed international journals including Thomson Reuters (SCI & Web of Science) and international conferences. Her main research work focuses on Semiconductor optical amplfier and photonics. She has 19 years of teaching experiences.

Mr. S Mukherjee pursed Master of Technology. He is currently pursuing Ph.D. and working as Assistant Professor & HOD in Department of Applied Electronics and Instrumentation Engineering, Murshidabad College of Engineering & Technology, Murshidabad. His main research work focuses on Optical computation, Semiconductor optical amplfier and photonics. He has 8 years of teaching experience and 2 years of Research Experiences.

Dr. PP Sarkar pursed Ph.D from Jadavpur University. He has been currently working as Assistant Professor in Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, Burdwan since 2008. He has published around 15 research papers in peer-reviewed international journals including Thomson Reuters (SCI & Web of Science) and conferences including IEEE. He is also a reviewer of different reputed Journals & Conferences. His main research work focuses on Parrallel computing, optics and photonics. He has 17 years of teaching experience and 10 years of Research Experiences.

ISSN 0030-400X, Optics and Spectroscopy, 2018, Vol. 124, No. 3, pp. 337–342. © Pleiades Publishing, Ltd., 2018.

NONLINEAR
AND QUANTUM OPTICS

A Novel Approach to Realize of All Optical Frequency Encoded DIBIT Based XOR and XNOR Logic Gates Using Optical Switches with Simulated Verification[1]

B. Ghosh[a], **S. Hazra**[a], **N. Haldar**[a], **D. Roy**[a], **S. N. Patra**[b], **J. Swarnakar**[c],
P. P. Sarkar[a,*], **and S. Mukhopadhyay**[d]

[a] *Department of Electronics and Communication Engineering, University Institute of Technology,*
The University of Burdwan, Burdwan, West Bengal, 713104 India
[b] *Department of Instrumentation Science, Jadavpur University, Kolkata, West Bengal, 700032 India*
[c] *Department of ECE, North Eastern Hill University, Shillong, Meghalaya, 793022 India*
[d] *Department of Physics, The University of Burdwan, Burdwan, West Bengal, 713104 India*
**e-mail: pratim34@gmail.com*

Received April 4, 2017

Abstract—Since last few decades optics has already proved its strong potentiality for conducting parallel logic, arithmetic and algebraic operations due to its super-fast speed in communication and computation. So many different logical and sequential operations using all optical frequency encoding technique have been proposed by several authors. Here, we have keened out all optical dibit representation technique, which has the advantages of high speed operation as well as reducing the bit error problem. Exploiting this phenomenon, we have proposed all optical frequency encoded dibit based XOR and XNOR logic gates using the optical switches like add/drop multiplexer (ADM) and reflected semiconductor optical amplifier (RSOA). Also the operations of these gates have been verified through proper simulation using MATLAB (R2008a).

DOI: 10.1134/S0030400X1803013X

INTRODUCTION

Basically, photon can be used for super-fast information processing [1], due to its very high speed of operation. So, it is an appropriate information transporter than electron. Different types of encoding techniques are needed for implementing the all optical logic and arithmetic devices [2]. Various types of encoding techniques are frequency encoding [3–5], intensity encoding, phase encoding, spatial encoding, polarization encoding etc. Generally, frequency of light beam always remains unchanged and unaffected in the cases of reflection, refraction, absorption etc. So, frequency encoding technique is the most consistent encoding technique. In the frequency encoding technique, two different states of information can be represented by two different frequencies at the time of data computation [6–8] and encoding process. If, frequency of light beam of a specific value is considered as digital logic state '0' then, frequency of light beam of another value will be treated as digital logic state '1'. For this reason, if v_1 frequency of light beam is considered as digital logic state '0' then v_2 frequency of light beam will be treated as digital logic state '1'.

Now, the dibit representation technique [9] can be done to represent a digital logic state by two consecutive bit positions. So, the digital logic state '0' is represented as dibit logic state $\langle 0\rangle\langle 1\rangle$ and digital logic state '1' is represented as dibit logic state $\langle 1\rangle\langle 0\rangle$ respectively. These two positions may be considered as two different frequencies. That means, the occurrence of the two frequencies side by side $\langle v_1\rangle\langle v_2\rangle$ represents the digital logic state '0' and $\langle v_2\rangle\langle v_1\rangle$ does the same as the digital logic state '1'. This technique in optics for logical operation was first proposed by S. Mukhopadhyay [10]. Here, the authors have proposed all frequency encoded dibit based XOR and XNOR logic gates with the help of all optical switches like add/drop multiplexer [11] and reflected semiconductor optical amplifier [12] developing the dibit representation with appropriate dibit checking facility.

Already, dibit based logic gates are exploited in few papers, reporting in different journals. But in this paper authors have proposed new concept of implementing frequency encoded all optical dibit based XOR and XNOR logic gates with a novel modification of dibit checking unit, which prevents the inappropriate input to enter into the dibit based logic gates. As the inputs in the form of dibit logic state $\langle 0\rangle\langle 0\rangle$ and

---

[1] The article is published in the original.

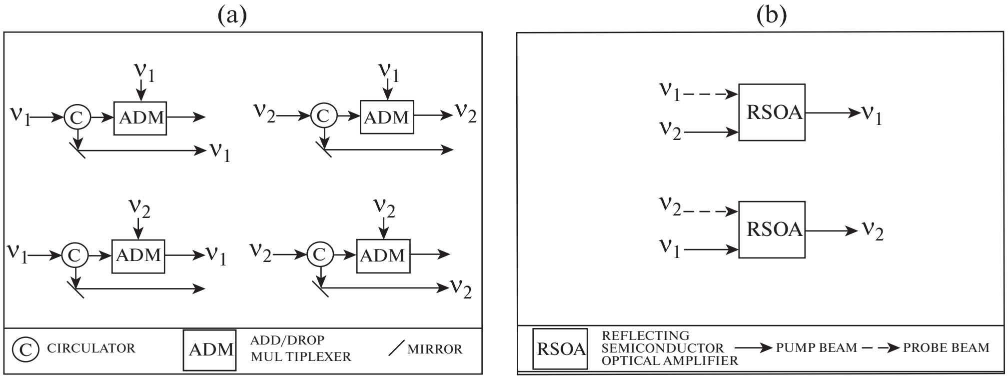


Fig. 1. Block diagram of ADM (a) and RSOA (b).

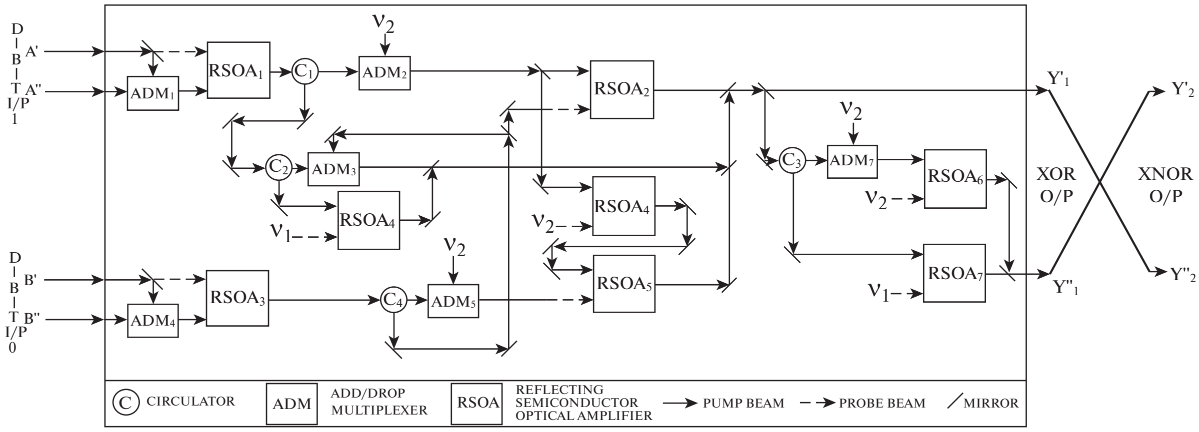


Fig. 2. Block diagram of Frequency encoded dibit based XOR and XNOR logic gates.

$\langle 1\rangle\langle 1\rangle$ are the improper inputs in case of dibit system then, the dibit checking unit restricts those inputs to operate. These facilities provide the advantage the reliability of the logic gates.

Add/drop multiplexer (ADM) is a frequency selective optical switching device. If it is biased with a particular biasing then it reflects the particular frequency of light beam and passes other frequency of light beam. Opposite incident happens if the biasing changes, which is shown in Fig. 1a. Now, reflected semiconductor optical amplifier (RSOA) is another optical switching device, where a weak probe beam of light of frequency say, ν_1 and a strong pump beam of light of frequency say, ν_2 are inserted to the input terminals (shown in Fig. 1b). Then this switch will provide the output light beam in form of frequency of probe beam (say, ν_1 frequency) and the power of the pump beam. By this way, it could be established as very promising optical devices for conducting many all optical logical operations.

SCHEME OF REALIZATION OF FREQUENCY ENCODED DIBIT BASED XOR AND XNOR LOGIC GATES

In Fig. 2, for realizing the dibit based two inputs XOR gate the input channels are considered as ‘A’ and ‘B’ respectively. These two channels i. e. ‘A’ and ‘B’ are subdivided further as ‘A'’ and ‘A''’, ‘B'’ and ‘B''’, respectively to provide dibit inputs.

Initially, ν_1 and ν_2 frequencies of light are given to the input channels of ‘A'’, ‘A''’ and ‘B'’, ‘B''’ simultaneously. It checks the real dibit input combinations because there is a real dibit checking provision by ADM$_1$ with RSOA$_1$ and ADM$_4$ with RSOA$_3$ blocks. The light beam of ν_1 frequency coming from ‘A'’ acts as biasing terminal of ADM$_1$. So, the light beam of ν_2 frequency coming from ‘A''’ passes through the ADM$_1$. Therefore, dibit input $\langle 0\rangle\langle 1\rangle$ or $\langle \nu_1\rangle\langle \nu_2\rangle$ frequencies of light are injected in form of probe beam and pump beam respectively at channel ‘A’ section to RSOA$_1$. So, ν_1 frequency of light beam comes out from RSOA$_1$ as output. By the same way, ν_1 frequency of light beam

Table 1. Truth table of dibit based optical XOR and XNOR logic gates

Dibit Input 1		Digital form	Dibit Input 2		Digital form	Dibit XOR Output		Digital form	Dibit XNOR Output		Digital form
A'	A"	A	B'	B"	B	Y_1'	Y_1''	Y_1	Y_2'	Y_2''	Y_2
$v_1[0]$	$v_2[1]$	0	$v_1[0]$	$v_2[1]$	0	$v_1[0]$	$v_2[1]$	0	$v_2[1]$	$v_1[0]$	1
$v_1[0]$	$v_2[1]$	0	$v_2[1]$	$v_1[0]$	1	$v_2[1]$	$v_1[0]$	1	$v_1[0]$	$v_2[1]$	0
$v_2[1]$	$v_1[0]$	1	$v_1[0]$	$v_2[1]$	0	$v_2[1]$	$v_1[0]$	1	$v_1[0]$	$v_2[1]$	0
$v_2[1]$	$v_1[0]$	1	$v_2[1]$	$v_1[0]$	1	$v_1[0]$	$v_2[1]$	0	$v_2[1]$	$v_1[0]$	1

also comes out from $RSOA_3$ as output for the given dibit input $\langle v_1\rangle\langle v_2\rangle$ or input $\langle 0\rangle\langle 1\rangle$ to channel ‘B’ section. Now, output of $RSOA_1$, i.e. v_1 frequency of light goes to $RSOA_2$ as pump beam because ADM_2 is biased by v_2 frequency of light beam. But $RSOA_2$ will not act due to absence of probe beam. Now, one part of this light beam of v_1 frequency goes to $RSOA_4$ as pump beam, but there is a constant probe beam of v_2 frequency. So, v_2 frequency of light beam comes from $RSOA_4$ as output and this light beam goes to $RSOA_5$ as a pump beam. Now, from $RSOA_3$ v_1 frequency of light is passed by ADM_5 and comes as a probe beam of $RSOA_5$. For this reason v_1 frequency of light beam comes out from $RSOA_5$ and goes directly to ‘Y_1'’ of output terminal ‘Y’. Now one part of this v_1 frequency of light beam goes to ADM_7. As this block is biased by v_2 frequency, so, it passes v_1 frequency of light beam and goes to $RSOA_6$ as pump beam but there is a constant light of probe beam of v_2 frequency. For that reason v_2 frequency of light beam comes out from $RSOA_6$ and goes to ‘Y_1''’ of output terminal ‘Y’. So, we may get dibit output $\langle v_1\rangle\langle v_2\rangle$ (or $\langle 0\rangle\langle 1\rangle$ or digital logic state ‘0’) at the output terminal ‘Y’ (or, at output terminals ‘Y_1'’ and ‘Y_1''’, respectively) for given dibit inputs of $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ and $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ or, digital logic state combination ‘0’ and ‘0’ at input terminals ‘A’ and ‘B’, respectively. This output is satisfied by XOR logic for the digital logic state input combination ‘0’ and ‘0’ which provides ‘0’ output (shown in Table 1). Now, if we use this dibit output bits at ‘Y_2'’ and ‘Y_2''’ terminals in reverse way as shown in Fig. 2, then we may get the dibit output $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ or digital logic state ‘1’ at the output terminal. This dibit output is satisfied by XNOR logic for the digital logic state input combination ‘0’ and ‘0’ at both input terminals.

Secondly, v_1 and v_2 frequencies of light beam are given to the input channels of ‘A'’, ‘A"’ but v_2 and v_1 frequencies of light are inserted to the ‘B'’, ‘B"’ input channels. Now both the inputs will be checked for true dibit combinations. So, v_1 and v_2 frequencies of light beam are come from $RSOA_1$ and $RSOA_3$ respectively. Since, ADM_2 is biased by v_2 frequencies of light beam, output of $RSOA_1$ i.e. v_1 frequency of light goes to $RSOA_2$ as pump beam. As the previous combination, one part of this light beam of v_1 frequency goes to $RSOA_5$ as a pump beam. But the $RSOA_5$ will not work as there is no probe beam. Now, v_2 frequency of light beam, which is coming from $RSOA_3$, is reflected by ADM_5 and comes as a probe beam of $RSOA_2$. This v_2 frequency of light beam comes out from $RSOA_2$ and goes to ‘Y_1'’ of output terminal ‘Y’. Now, one part of this light beam goes to ADM_7 and reflected by ADM_7 and goes to $RSOA_7$ as pump beam. But there is a constant probe beam of v_1 frequency. So, v_1 frequency of light beam comes out from $RSOA_7$ and goes to ‘Y_1''’ of output terminal ‘Y’. Thus, we may obtain dibit output $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ or digital logic state ‘1’ at the output terminal ‘Y’ (combination of ‘Y_1'’ and ‘Y_1''’) for given dibit inputs of $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ and $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ or, digital logic state combination ‘0’ and ‘1’ at input terminals ‘A’ and ‘B’ respectively and this is also satisfied by XOR logic (shown in Table 1). Now if we use this dibit output bits at ‘Y_2'’ and ‘Y_2''’ terminals in reverse way, then we may get the dibit output $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ or digital logic state ‘0’ at the output terminal, which satisfies the XNOR logic.

Thirdly, v_2 and v_1 frequencies of light beam are injected to the input channels of ‘A'’, ‘A"’ but v_1 and v_2 frequencies of light are applied to the ‘B'’, ‘B"’ input channels. But, after the dibit checking of both the inputs, v_2 and v_1 frequencies of light beam come from $RSOA_1$ and $RSOA_3$ respectively. The v_2 frequency of light beam is reflected by the ADM_2 (biased by v_2 frequency) and goes to the input terminal of ADM_3 and passed by ADM_3 as there is no biasing input and goes directly to ‘Y_1'’ of output terminal ‘Y’. Besides this, from $RSOA_3$ v_1 frequency of light is passed by ADM_5 and comes as a probe beam of $RSOA_5$. But the $RSOA_5$

will not work as there is no pump beam of $RSOA_5$. Now, the part of the light beam of v_2 frequency coming from ADM_3, goes properly as pump beam to $RSOA_7$ (with constant probe beam of v_1 frequency) and this v_1 frequency of light beam will come to the 'Y_1''' of output terminal 'Y'. Again, we may find the dibit output $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ or digital logic state '1' at the output terminal 'Y' with the combination of 'Y_1'' and 'Y_1''' channels for given dibit inputs of $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ and $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ or, digital logic state combination '1' and '0' at input terminals 'A' and 'B' respectively, satisfying the XOR logic. But if we use this dibit output bits at 'Y_2'' and 'Y_2''' terminals in reverse way, then we may get the dibit output $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ or digital logic state '0' at the output terminal, satisfying the XNOR logic.

Finally, if we insert v_2 and v_1 frequencies of light beam to the input channels of 'A'', 'A''' and 'B'', 'B''' simultaneously then light beams of v_2 frequency will come from both $RSOA_1$ and $RSOA_3$ after suitable checking of input dibit combinations. Now, both the light beams are reflected by ADM_2 and ADM_5 as these ADMs are biased by v_2 frequency. Then the light beams are coming to the input terminal of the ADM_3 and as probe beam of $RSOA_2$ respectively. But the $RSOA_2$ will not work properly for absence of pump beam. But, the part of the light beam of v_2 frequency, reflected by ADM_5, acts as biasing input of ADM_3. So, the input light beam at the input terminal of ADM_3 is reflected and is coming as the pump beam of $RSOA_4$. As presence of the probe beam of v_1 frequency, the v_1 frequency of light beam is coming from $RSOA_4$ as output and goes to the 'Y_1'' of output terminal 'Y'. Again, one part of this light beam goes through ADM_7 and as pump beam of $RSOA_6$ (with constant probe beam of v_2 frequency). So, v_2 frequency of light beam comes out from $RSOA_6$ and goes to 'Y_1''' of output terminal 'Y'. Thus, we may get dibit output $\langle v_1\rangle\langle v_2\rangle$ or $\langle 0\rangle\langle 1\rangle$ or digital logic state '0' at the output terminal 'Y' for given dibit inputs of $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ and $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ or, digital logic state combination '1' and '1' at input terminals 'A' and 'B' respectively. Finally, these outputs are satisfied by truth table of XOR logic (shown in Table 1). Again, if we use this dibit output bits at 'Y_2'' and 'Y_2''' terminals in reverse way as shown in Fig. 2, then we may obtain the dibit output $\langle v_2\rangle\langle v_1\rangle$ or $\langle 1\rangle\langle 0\rangle$ or digital logic state '1' at the output terminal, satisfying the XNOR logic also.

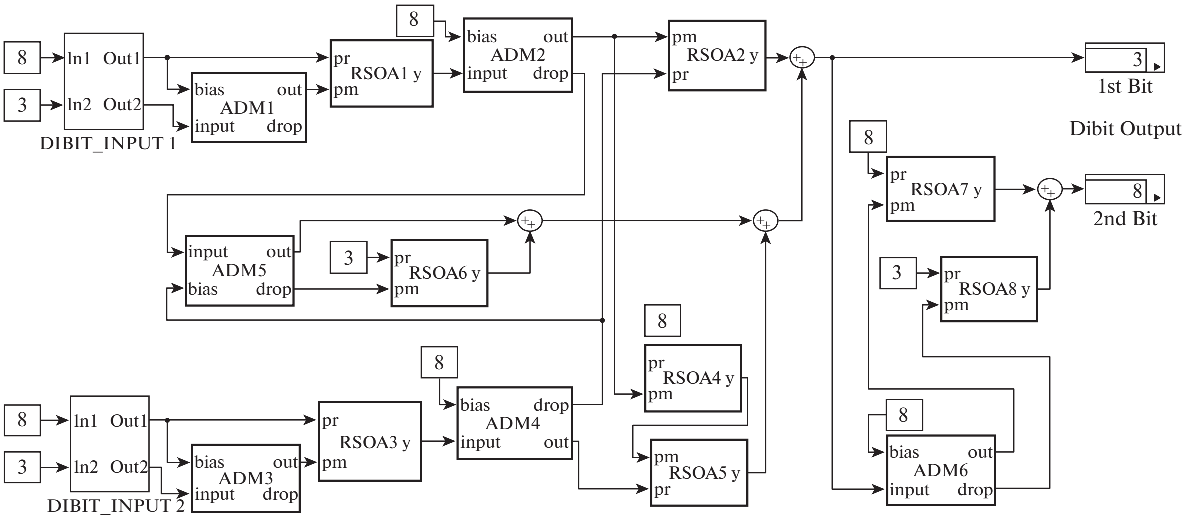
SIMULATION PROCESS OF FREQUENCY ENCODED DIBIT BASED XOR AND XNOR LOGIC GATES

For the simulation process here, MATLAB (R2008a) software have been used to frequency encoded all optical dibit XOR and XNOR logic gates with dibit checking using RSOA and ADM respectively. "DIBIT_INPUT 1" and "DIBIT_INPUT 2" are used for implementing dibit input signals and we get output signal from "Dibit Output" unit, which is consisted of two consecutive bit, i.e. "1st Bit" and "2nd Bit", respectively. Now, the RSOA blocks are properly programmed with 'C' language for choosing the proper output at the output terminal, shown in Figs. 3 and 4. Here, two inputs viz. "pr" (probe beam) and "pm" (pump beam) and the output by "y" in RSOA blocks. The RSOA blocks are designed such a way that the probe beam comes out at the output of RSOA when both the inputs in form of pump beam and probe beam are available. If pump beam and probe beam are considered as say "3 peta Hz" = v_1 = digital logic state "0" and "8 peta Hz" = v_2 = digital logic state "1" respectively at the input terminals of RSOA, here we obtain "8 peta Hz" = v_2 = digital logic state "1" at the output terminal of these blocks. The value of the output unit changes if the values of the pump beam and probe beam respectively are altered accordingly.

Again, ADM block has been simulated such a way that, if a sequence of frequencies is applied at the input terminal of ADM block, it passes all other frequencies and drops a particular frequency depending upon the biasing. Now, if the biasing is changed then the frequency of the dropped terminal change accordingly. Here, for particular biasing at "bias" terminal, this block drops one frequency coming from "input" terminal to "drop" terminal and passes other frequencies to "out" terminal if the input frequencies are present at the ADM unit, say "8 peta Hz" = v_2 = digital logic state "1" and "3 peta Hz" = v_1 = digital logic state "0". If the value of biasing is changed, opposite incident happens. Now these two blocks are connected maintaining the similarity of the block diagram of all optical dibit XOR and XNOR logic gates (shown in Fig. 2).

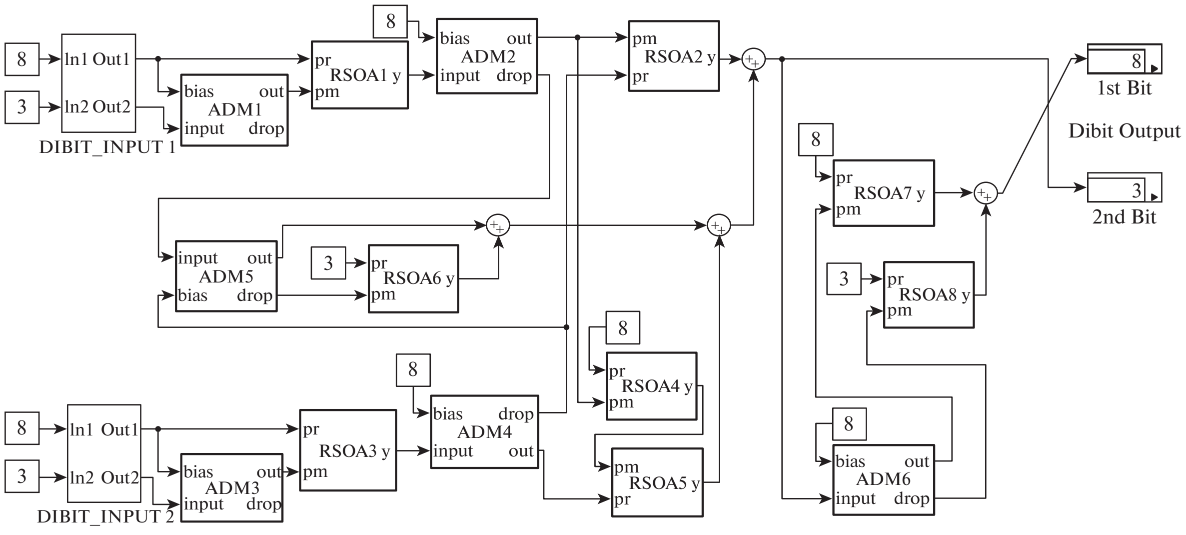
Now, considering $\langle 3\rangle\langle 8\rangle$ as digital logic states '0' and $\langle 8\rangle\langle 3\rangle$ as digital logic states '1', if $\langle 8\rangle\langle 3\rangle$ and $\langle 8\rangle\langle 3\rangle$ are applied at the two dibit input terminals of the simulated model, we get $\langle 3\rangle\langle 8\rangle$ at the output terminal of this simulated block. Similarly, for the input combinations $\langle 3\rangle\langle 8\rangle$ and $\langle 3\rangle\langle 8\rangle$, the output repeats the same value, i.e. $\langle 3\rangle\langle 8\rangle$. But at the output we get $\langle 8\rangle\langle 3\rangle$ for the dibit inputs $\langle 3\rangle\langle 8\rangle$ and $\langle 8\rangle\langle 3\rangle$ and for the dibit inputs $\langle 8\rangle\langle 3\rangle$ and $\langle 3\rangle\langle 8\rangle$.

Finally, this simulative functional model fully satisfies the truth table of all optical dibit based XOR logic gate, which is shown in Table 1.



Frequency 3 = ν_1 = D.S = 0, Frequency 8 = ν_2 = D.S = 1
D.S. = Digotal State, pr = Probe Beam, pm = Pump Beam
ADM = Add/DropMultiplexure, RSOA = Reflected Semiconductor Optical Amplifier

Fig. 3. Simulation model of the dibit based XOR logic gate.



Frequency 3 = ν_1 = D.S = 0, Frequency 8 = ν_2 = D.S = 1
D.S. = Digotal State, pr = Probe Beam, pm = Pump Beam
ADM = Add/DropMultiplexure, RSOA = Reflected Semiconductor Optical Amplifier

Fig. 4. Simulation model of the dibit based XNOR logic gate.

By the same way, Simulink tools of MATLAB (R2008a) software have been used for simulation model of the dibit based XNOR logic gate. Here, by the same encoding technique, if we apply ⟨8⟩⟨3⟩ and ⟨8⟩⟨3⟩ to the dibit input terminals, we get ⟨8⟩⟨3⟩ at the output terminal. Similarly, we get same dibit output as ⟨8⟩⟨3⟩ for the dibit inputs ⟨3⟩⟨8⟩ and ⟨3⟩⟨8⟩. But, for the rest all possible combinations of dibit inputs like, ⟨3⟩⟨8⟩ and ⟨8⟩⟨3⟩, ⟨8⟩⟨3⟩ and ⟨3⟩⟨8⟩, we get ⟨3⟩⟨8⟩ as dibit output. So, this simulated block fully satisfies the truth table of frequency encoded all optical dibit based XNOR logic gate, which is shown in Table 1.

RESULTS AND DISCUSSION

All the results, getting from the simulation processes, related to XOR and XNOR logic gates are satisfied by truth tables for the concern logic gates and that's why we insert a combined table (Table 1) for all optical frequency encoded dibit based XOR and XNOR logic gates.

CONCLUSIONS

To realize the all optical operations, advantages of frequency encoding as well as dibit representation technique are exploited here. This mechanism is a trustworthy, faithful operation and it supports reduction of bit error problem by increasing high signal to noise ratio. Again, the dibit checking process reduces errors on wrong dibit input states. Using this mechanism, we can expect a high degree of parallelism with ultra-fast operational speed. This encoding technique helps for implementation of the all-optical logical operations with faithful and reliable results. With the realization of all optical frequency encoded dibit based XOR and XNOR logic gates using optical switches and with the simulated verification, these logic gates can be used for preparing all optical computational devices like adder/sub-tractor, correlation and sequence detector etc. So, it supports an ultra-high speed operation and exhibit a real time operation with high reliability.

REFERENCES

1. S. Mukhopadhyay, Indian J. Phys. **84**, 1069 (2010).
2. S. K. Garai and S. Mukhopadhyay, Optik (Munich, Ger.) **121**, 715 (2010).
3. P. P. Sarkar, B. Satpati, and S. Mukhopadhyay, J. Opt. **42**, 360 (2013).
4. P. P. Sarkar, B. Ghosh, and S. N. Patra, J. Opt. Technol. **83**, 257 (2016).
5. S. Dutta and S. Mukhopadhyay, Optik (Munich, Ger.) **122**, 1088 (2011).
6. A. K. Ghosh, A. Bhattacharya, M. Raul, and A. Basuray, Opt. Laser Technol. **44**, 1583 (2012).
7. B. Ghosh, R. R. Pal, and S. Mukhopadhyay, Indian J. Phys. **84**, 1101 (2010).
8. H. Q. Jin, J. R. He, Z. B. Cai, J. C. Liang, and L. Yi, Indian J. Phys. **87**, 1243 (2013).
9. B. Ghosh and S. Mukhopadhyay, Optik (Munich, Ger.) **124**, 4813 (2013).
10. S. Mukhopadhyay, Appl. Opt. **31**, 4622 (1992).
11. A. N. Z. Rashed, Int. J. Multimedia Ubiquitous Eng. **7**, 1 (2012).
12. H. Kim et al., Electrochem. Solid-State Lett. **14** (10), K55 (2011).

SPELL: OK

Journal of
Optical Technology

A new scheme of an all optical frequency encoded dibit based latch with its simulated result

P. P. SARKAR,[1,4] **B. GHOSH,**[1,5] **S. N. PATRA,**[2,6] **AND S. MUKHOPADHYAY**[3,7]

[1]*Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, West Bengal-713104, India*
[2]*Department of Instrumentation Science, Jadavpur University, Kolkata-700032, West Bengal, India*
[3]*Department of Physics, University of Burdwan, West Bengal-713104, India*
[4]*e-mail: pratim34@gmail.com*
[5]*e-mail: bitanghosh87@gmail.com*
[6]*e-mail: sankar.journal@gmail.com*
[7]*e-mail: sourangshu2004@gmail.com*

Received 9 August 2016; Opticheskiĭ Zhurnal ***84****, 66–70 (September 2017)*

Super fast all optical memory and optical logic gates are the basic building blocks for optical computation and communication systems. Realization of a very fast memory cell in the optical domain is very challenging. Recently different theoretical proposals based on combinational and sequential logic circuits for developing all optical flip flops as well as memory cells have been reported by different authors. Here, the authors have proposed a new scheme of an all optical frequency encoded dibit based latch circuit using a reflective semiconductor optical amplifier and an add/drop multiplexer with its proper simulation. The use of the dibit representation technique along with the optical frequency encoding technique makes the system very fast, reduces the bit error problem, and increases the signal to noise ratio.

OCIS codes: (190.0190) Nonlinear optics; (190.4360) Nonlinear optics, devices.

https://doi.org/10.1364/JOT.84.000631

1. INTRODUCTION

The all optical data processing technique is the most alternative and successful replacement to overcome speed related problems as light has the inherent character of parallelism [1]. Different types of all optical logic gates and memory circuits are the fundamental building blocks for optical data processors and communication systems [2–4]. Again, the dibit representation technique provides the benefits of a low bit error problem by increasing the high signal to noise ratio. Here, the authors have proposed a new scheme of an all optical frequency encoded latch by reflective semiconductor optical amplifier (RSOA) and add/drop multiplexer (ADM) blocks with the dibit representation technique [5], where digital value '0' is represented as [0][1] logic states and digital value '1' is represented as [1][0], respectively. In other words, the presence of the two frequencies side by side $[v_1][v_2]$ represents digital logic state '0' and $[v_2][v_1]$ does the same as digital logic state '1'. To implement the all optical dibit based latch circuit, the RSOA and the ADM are two important optical switches, which are discussed below.

A. Reflective Semiconductor Optical Amplifier

A reflective semiconductor optical amplifier is an optical switch [6], which is shown in Fig. 1. If a weak probe beam of light of frequency v_1 and a strong pump beam of light of frequency v_2 are inserted into the input terminals, then this block will provide the output beam in the form of a frequency of the probe beam along with the power of the pump beam. Here, it will provide the output light beam of frequency v_1. But, if the frequencies of the pump and probe beam of light are interchanged, then the opposite incidence happens; i.e., now, it will provide the output light beam of frequency v_2. So, this could be established as a very promising optical device for conducting many all optical logical operations.

B. Add/Drop Multiplexer

Optical ADM [7] is a frequency selective switch. Now, if it is tuned with a particular biasing current (I_1, I_2, etc.), then it reflects a particular frequency of light and passes all other frequencies of light. If it is biased by biasing current I_1, then it reflects frequency v_1 of the light beam and passes all other frequencies of light beams. But, when it is biased by biasing current I_2, then it reflects frequency v_2 of the light beam and passes all other frequencies of light beams. Different incidence happens if the biasing current changes. This block is shown in Fig. 2.

2. PRINCIPLE OPERATION OF THE FREQUENCY ENCODED ALL OPTICAL NOT BASED DIBIT LATCH

To develop a complete unit of a frequency encoded all optical memory cell, the first step is to develop a latch or a memory

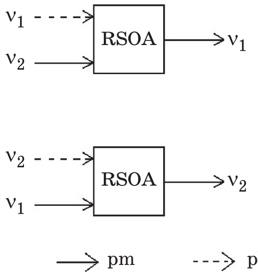


Fig. 1. Block diagram of the RSOA. Probe beam—pb, pump beam—pm.

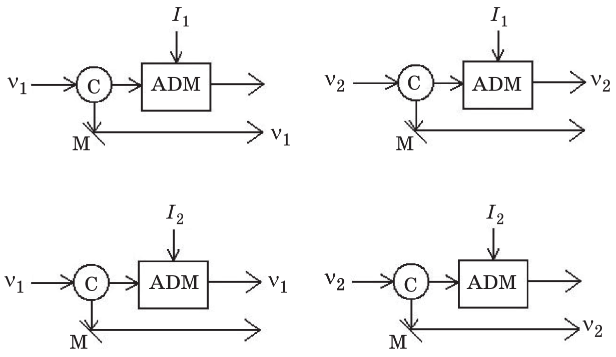


Fig. 2. Block diagram of the ADM. C—calculator, M—mirror.

unit as it can store a dibit. The proposed system described here is based on the frequency encoding principle, shown in Fig. 3. Here we have used the dibit representation technique [8]. So, dibit state [0][1] or [v_1][v_2] represents digital logic state ‘0’ and dibit state [1][0] or [v_2][v_1] represents digital logic state ‘1’. Here, in our proposed system, ‘I′’ and ‘I″’ represent the 1st bit and 2nd bit of the dibit input and ‘O′’ and ‘O″’ are the dibit output terminals, respectively. For better understanding about the state change of the latch circuit, we have considered the NOT logic gate based system. To implement the optical NOT based latch logic with the dibit technique, beam splitters, mirrors, RSOAs, and ADMs are used at different positions in the system.

Here, optical wave beams in the form of ‘I′’ = v_1 and ‘‘I″’ = v_2 frequencies are applied at the input terminal. Now, frequency v_1 of the light beam is moved as the weak probe beam and frequency v_2 of the light beam is sent as the strong pump beam to RSOA$_1$. So, according to the principle of a RSOA, we get frequency v_1 of the light beam at the output of RSOA$_1$. This frequency of the light beam enters ADM$_1$, which is biased by biasing current I$_2$. So it passes frequency v_1 of the light beam to RSOA$_2$ as a pump beam. But there is a constant probe beam of frequency v_2 of the light beam at RSOA$_2$. For this reason, the output becomes in the form of frequency v_2 of the light beam and goes to output terminal ‘O′’.

Again a portion of this output frequency of the light beam goes to RSOA$_3$ as a pump beam by the feedback path. Since there is a constant source of the probe beam of frequency v_1 of light, frequency v_1 of the light beam comes out from RSOA$_3$ and this light beam of frequency v_1 goes to another output terminal ‘O″’. Now, to sustain the output continuously, there is a feedback process, where the output light beam of frequency v_1 from ‘O″’ goes to the pump beam terminal of RSOA$_2$. After getting both the inputs, RSOA$_2$ provides frequency v_2 of the light beam at the output terminal, which comes again in the form of the output to ‘O′’ and from this light a portion of the light beam comes again to the RSOA$_3$, where there is a fixed input in the form of the probe beam. So, this RSOA$_3$ block again produces frequency v_1 of the light beam at the output. In this way, we get continuous output of frequencies v_2 and v_1 of the light beam at the terminals ‘O′’ and ‘O″’, respectively, with given [v_1][v_2] input, and this output is sustained, even if the input frequency of the light beam is absent.

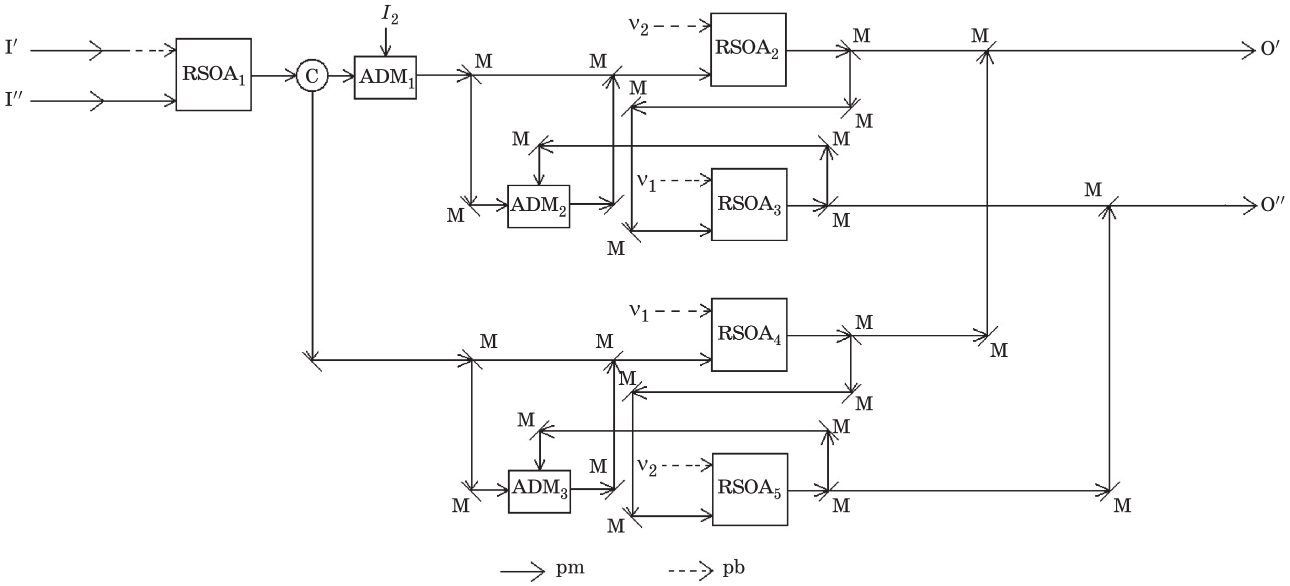


Fig. 3. Block diagram of the frequency encoded NOT based dibit latch. C—calculator, M—mirror.

Table 1. Truth Table of the NOT Based Dibit Latch

Dibit			Dibit		
Based on I′	**Input I″**	**Digital Input**	**Based on O′**	**Output O″**	**Digital Output**
$v_1[0]$	$v_2[1]$	0	$v_2[1]$	$v_1[0]$	1
$v_2[1]$	$v_1[0]$	1	$v_1[0]$	$v_2[1]$	0

Now, we apply an optical light beam in the form of ‘I″ = v_2 frequency and ‘I‴’ = v_1 frequency at the input terminal. This input light beam is the opposite of the first case. It is noted that frequency v_2 and frequency v_1 of the light beam are moved as the weak probe beam and the strong pump beam to the RSOA$_1$, respectively. According to the principle of a RSOA, it provides frequency v_2 of the light beam at the output of RSOA$_1$ and it comes to the input terminal of ADM$_1$. Here, frequency v_2 of the light beam is reflected by ADM$_1$ because it is biased by the optical light beam of frequency v_2. So frequency v_2 of light goes to RSOA$_4$ as a pump beam. Here, there is a constant probe beam in the form of frequency v_1 of the light beam. Then the output becomes frequency v_1 of the light beam and this light of frequency v_1 goes to output terminal ‘O″’. Now a part of this output light beam from the output of RSOA$_4$ goes to RSOA$_5$ as a pump beam by the feedback path, where there is a constant probe beam of frequency v_2 of light. So, frequency v_2 of the light beam coming from RSOA$_5$ goes to output terminal ‘O‴’. Again, a portion of this output of the light beam from ‘O‴’ goes to the pump beam terminal of RSOA$_4$. So, the output is maintained incessantly by this feedback process. Here, we get continuous output of v_1 and v_2 at terminals ‘O″’ and ‘O‴’, respectively; that means it is a NOT based latch circuit, so, with the given input of the light beam in the form of $[v_2][v_1]$, we get at the output of the light beam in the form of $[v_1][v_2]$. The output frequencies at both the terminals remain unchanged until or unless the input frequencies of the light beams are altered. This is the overall configuration of the whole scheme [9].

Now, to describe the operation, it can be said that when dibit logic state [0][1] is applied at the input terminal, the upper portion of the proposed scheme (shown in Fig. 3) is activated but the lower half is not. So one can ensure that the frequencies v_2 and v_1 of the light beam come at the output terminal ‘O″’ and ‘O‴’, respectively; i.e., ‘O″’ = digital logic state ‘1’ and ‘O‴’ = digital logic state ‘0’. So, dibit logic state [1][0] is obtained at the output terminal of this latch circuit. Similarly, when dibit logic state [1][0] is applied at the input terminal, the upper half is not activated, but the lower portion of the system is activated. Again, we get the output ‘O″’ = digital logic state ‘0’ and ‘O‴’ = digital logic state ‘1’; i.e., dibit logic state [0][1] is obtained. The input and output of the optical dibit based latch or memory cell is also shown in the truth table (Table 1), which satisfies the fundamental logic principle of a NOT based latch. Now, the most important and interesting point here is that if dibit logic states [0][1] or [1][0] are withdrawn from the input terminal of this latch circuit, this scheme will continue to show the last attended values at the output terminal ‘O″’ and ‘O‴’ simultaneously as the final output due to the feedback mechanisms. So, it can be said that the proposed scheme behaves as a frequency encoded all optical dibit based memory cell.

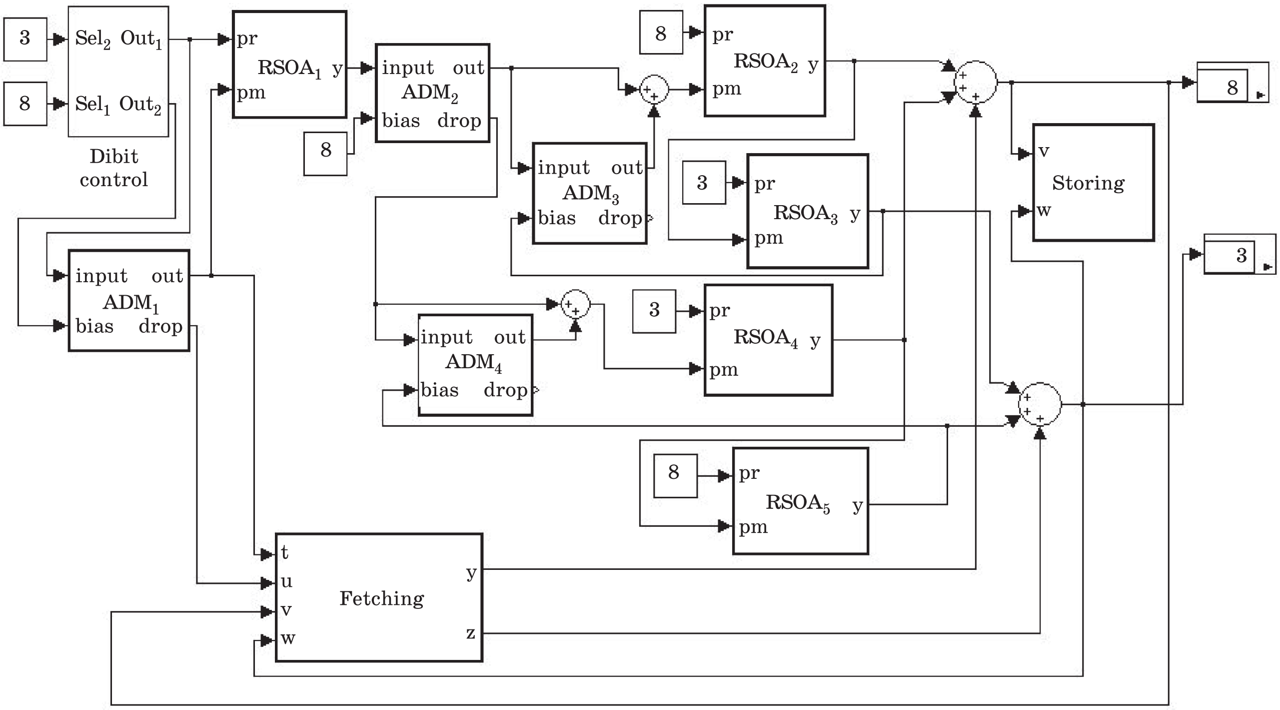


Fig. 4. Mathematical model of the all optical frequency encoded NOT based dibit latch. Frequency $3 = v_1 = \mathrm{DS} = 0$, frequency $8 = v_2 = \mathrm{DS} = 1$, DS—digital state, pb—probe beam, pm—pump beam.

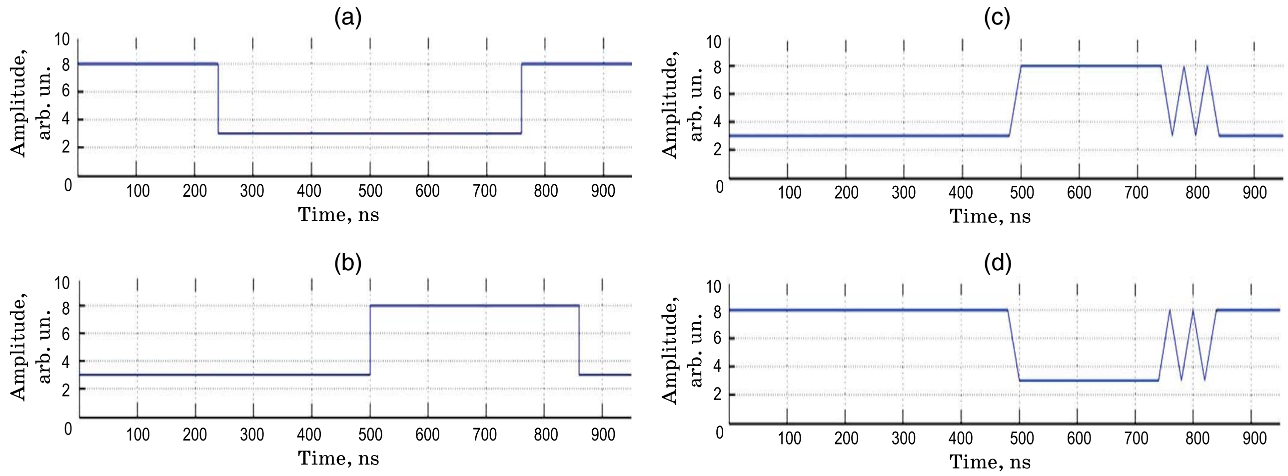


Fig. 5. Mathematical model of the all optical frequency encoded NOT based dibit latch. (a) Dibit input I′, (b) I″, (c) dibit output O′, (d) O″.

3. METHOD OF SIMULATION OF THE NOT BASED DIBIT LATCH

Now, following the block diagram of Fig. 3, we have simulated the dibit based optical latch circuit with MATLAB Simulink programming software in Fig. 4, where there are two output terminals, which provide the changeable output depending on the variation of inputs. For example, if we provide the dibit based input $[v_1][v_2]$ or [0][1] (here [3][8]) this simulated block provides the output in the form of $[v_2][v_1]$ or [1][0] (here [8][3]), as it is a NOT based latch circuit. Now, if we change the input, the output changes accordingly. Again, if there is no input given at the input terminal, this simulated block holds the previous output. Now, if we apply the input in the form of $[v_2][v_1]$ or [1][1] (here [8][8]), it is an abnormal input combination for a latch circuit; for this reason a toggle is ued as shown in Fig. 5.

This graphical representation of the input and output are shown in Fig. 5, which fully supports the truth table of the latch circuit (Table 1).

4. CONCLUSIONS

As the dibit representation technique is very much an accurate and reliable one, it supports reducing the bit error problem by increasing the high signal to noise ratio. It can also expect a high degree of parallelism. Also the truth table satisfies the dibit based latch logic circuit. Therefore its performance can directly be utilized for developing and verifying the performances of different logic devices based on the frequency encoding principle. Using this dibit representation one can implement other sequential and combinational all optical operations like flip flops, multivibrators, memories, etc.

REFERENCES

1. S. S. Pratim, B. Satpati, and S. Mukhopadhyay, “New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors,” J. Opt. **42**(4), 360–366 (2013).
2. P. P. Sarkar, B. Satpati, and S. Mukhopadhyay, “Analytical and simulative studies on optical NOR and controlled NOR logic gates with semiconductor optical amplifier,” Optik **125**(3), 1333–1336 (2014).
3. P. P. Sarkar, B. Satpati, and S. Mukhopadhydy, “Verification of all optical frequency encoded OR logic operation with its simulated result,” Int. J. Electron. Commun. Technol. **4**(1), 86–88 (2013).
4. S. Dutta and S. Mukhopadhyay, “Alternating approach of implementing frequency encoded all-optical logic gates and flip-flop using semiconductor optical amplifier,” Optik **122**(12), 1088–1094 (2011).
5. S. Mukhopadhyay, “Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems,” Appl. Opt. **31**(23), 4622–4623 (1992).
6. H. Kim, B. Kwon, M. Suh, D. S. Kang, Y. Kim, and D. Y. Jeon, “Degradation characteristics of red light-emitting $CuInS_2/ZnS$ quantum dots as a wavelength converter for LEDs,” Electrochem. Solid-State Lett. **14**(10), K55–K57 (2011).
7. K. Y. Wang and A. C. Foster, “Ultralow power continuous-wave frequency conversion in hydrogenated amorphous silicon waveguides,” Opt. Lett. **37**(8), 1331–1333 (2012).
8. B. Ghosh and S. Mukhopadhyay, “A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device,” Optik **124**(21), 4813–4815 (2013).
9. S. K. Chandra, P. P. Sarkar, S. Biswas, and S. Mukhopadhyay, “All-optical phase encoded 4-to-J phase multiplexer using four wave mixing in semiconductor optical amplifier,” Optik **125**(23), 6953–6957 (2014).

Simulative study of all optical frequency encoded dibit based universal NAND and NOR logic gates using a reflective semiconductor optical amplifier and an add/drop multiplexer

P. P. Sarkar,[1] B. Ghosh,[1] and S. Sankar Narayan Patra[2,3]

[1]*Department of Electronics and Communication Engineering, University Institute of Technology, University of Burdwan, West Bengal, India*
[2]*Department of Instrumentation Science, Jadavpur University, Kolkata—700032, India*
[3]*e-mail: psankarnarayan@isc.jdvu.ac.in*

(Received March 11, 2015)
Opticheskiĭ Zhurnal **83**, 80–87 (April 2016)

In the recent past, optics has been renowned as a powerful and potential candidate for implementation of logic gates, devices, optical computers, and communication for the benefit of speed of information processing. For the operation of a frequency encoded data processing system, optical logic gates based on the principle of frequency conversion of some nonlinear materials play the main role. Some papers have discussed the advantage of accuracy of dibit logic by implementing logic operations on dibit representation techniques, which provides the advantage of high-speed operation and reduces the bit error problem. Here, exploiting this phenomenon, frequency encoded all-optical dibit-based NAND and NOR logic gates using optical switches such as reflective semiconductor optical amplifiers and add/drop multiplexers with appropriate dibit checking facility are proposed by the authors. Also the authors have verified the operations through proper simulation using MATLAB (R2008a). © *2016 Optical Society of America.*

OCIS codes: (190.0190) Nonlinear optics; (190.4360) Nonlinear optics, devices.
http://dx.doi.org/10.1364/JOT.83.000257

1. INTRODUCTION

Generally, for super-fast information processing, a photon can be used as a very appropriate information transporter rather than an electron. For implementing frequency-encoded all-optical logic and arithmetic devices [1,2], different types of encoding techniques such as frequency encoding [3–5], intensity encoding, phase encoding, spatial encoding, polarization encoding [6], etc. are needed. The frequency encoding principle is the most reliable among all the other encoding principles because the frequency of light remains unaltered and unchanged under reflection, refraction, absorption, etc. Two different states of information can be represented by two different frequencies to use the frequency encoding/decoding technique at the time of data computation [7–9]. Now, the presence of a specific frequency of light is treated as digital logic state '1' and the other specific state is represented as digital logic state '0'.

Dibit representation can be done to symbolize a digit by two successive bit positions. These two positions may be considered as two different frequencies, say $\upsilon_1 = 195$ THz and $\upsilon_2 = 193$ THz. Now, if we consider that optical frequency of the light beam $\upsilon_1 =$ digital state '0' and $\upsilon_2 =$ digital state '1', then in dibit representation this digital state '0' is represented as [0][1] and digital state '1' is represented as [1][0], respectively. That means that the presence of the two frequencies side by side "$\upsilon_1\upsilon_2$" represents logic state '0' and "$\upsilon_2\upsilon_1$" does the same as logic state '1'. The dibit representation in optics for logical operation was first proposed by S. Mukhopadhyay [10]. In this paper, the authors have proposed a new concept of employing optical NAND and NOR logic gates with the help of all-optical switches such as reflective semiconductor optical amplifiers (or wavelength converters) and add/drop multiplexers developing the dibit representation with the appropriate dibit checking facility.

Already a few papers have been reported in different journals exploiting dibit-based logic gates [11]. But in this paper, the authors proposed frequency-encoded all-optical dibit-based universal logic gates with a novel modification of the dibit checking unit that prevents improper input to enter into the dibit-based logic gates. For example, if the input is in the form of digital logic state [0][0] and [1][1], the dibit checking unit restricts those inputs to operate as these are improper inputs in the case of the dibit system. These facilities provide the advantage of time management as well as increase the reliability of the logic gates.

A. Reflective Semiconductor Optical Amplifier (RSOA)

A reflective semiconductor optical amplifier [12,13] is an optical switch where a weak probe beam of light of wavelength, say, $\lambda_1 = 1540$ nm and a strong pump beam of light of wavelength $\lambda_2 = 1550$ nm are inserted into the input terminals. Then this system provides the output beam in the form of the frequency of the probe beam and the power of the pump beam. This could be established as a very promising optical device for conducting many all-optical logical operations.

B. Add/Drop Multiplexer (ADM)

An optical add/drop multiplexer [14–16] is a frequency-selective switch. Now, if it is tuned with a particular biasing

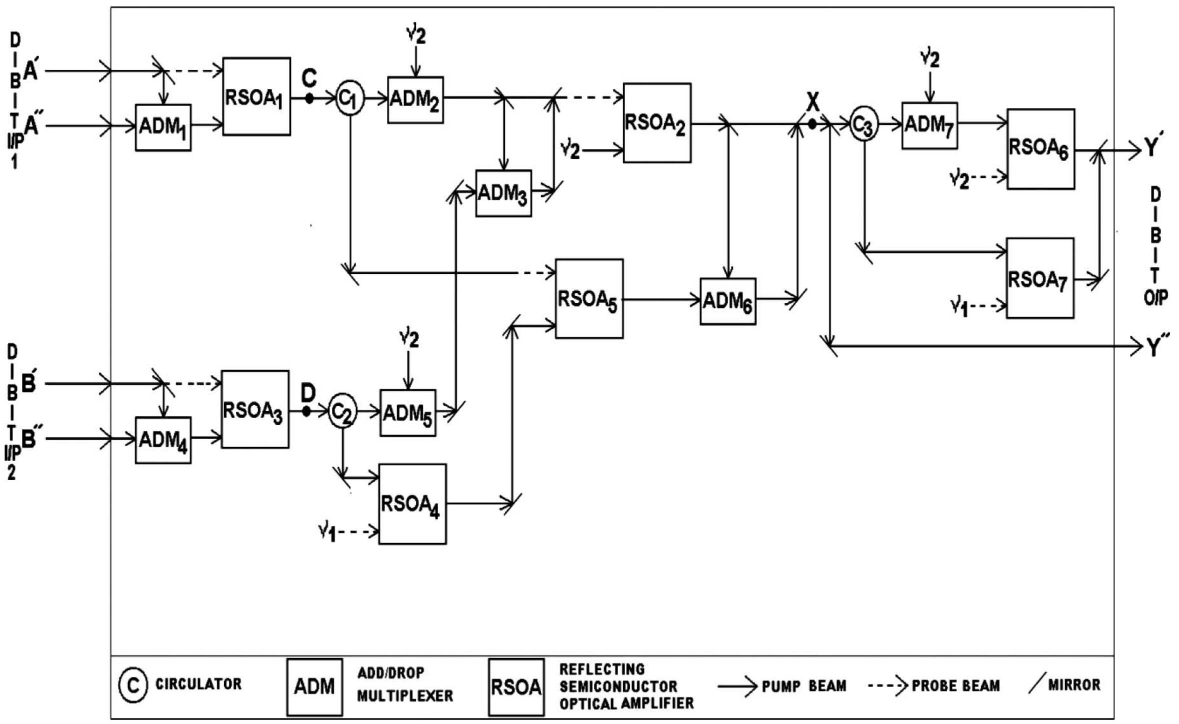


FIG. 1. Frequency encoded all optical dibit based NAND gate with dibit checking.

current, then it reflects a particular frequency of light and passes all other frequencies of light. Different incident happens if the biasing current changes.

2. SCHEME OF REALIZATION OF FREQUENCY-ENCODED DIBIT-BASED NAND LOGIC GATE WITH DIBIT CHECKING

In Fig. 1, to realize the dibit-based two-input NAND gate, the input channels are considered as ‘A’ and ‘B’, respectively. These two channels ‘A’ and ‘B’ are subdivided further as ‘A′’, ‘A″’, ‘B′’, ‘B″’, respectively, for providing dibit inputs. At first the υ_1 and υ_2 frequencies of light are given to the input channels of ‘A′’, ‘A″’ and ‘B′’, ‘B″’ simultaneously. Since there is a real dibit checking provision by the ADM_1 with RSOA_1 and ADM_4 with RSOA_3 blocks, it checks the real dibit input combinations. Therefore, dibit input [0][1] or the υ_1 frequency and υ_2 frequency of light are inserted in the form of a probe beam and a pump beam, respectively, at RSOA_1, and for this reason, the υ_1 frequency of light beam comes from RSOA_1 at point ‘C’. Similarly, the υ_1 frequency of light beam comes at point ‘D’ for the given input $[\upsilon_1][\upsilon_2]$. Now, from point ‘C’, the υ_1 frequency of light is passed by ADM_2 and it goes to RSOA_2 as the probe beam. Here, there is a constant pump beam of the υ_2 frequency of light beam. So, the υ_1 frequency of light beam comes as the output of RSOA_2 and it reaches to point ‘X’. Again, from point ‘D’, the υ_1 frequency of light beam is passed by ADM_5 and it goes to ADM_3, but, as ADM_3 is given the biasing by the υ_1 frequency, it does not pass any of the light beam. Also RSOA_4, RSOA_5, and ADM_6 do not work for the same reason. Now, the υ_1 frequency of light beam coming from point ‘X’ is passed by ADM_7 and goes to the input terminal of RSOA_6 as a pump beam. There is a fixed probe beam of the υ_2 frequency given at RSOA_6, so the υ_2 frequency of light comes out to the terminal ‘Y′’ in the form of final output. Again, the υ_1 frequency of light beam coming from point ‘X’ goes to terminal ‘Y″’ directly. For given dibit inputs of $[\upsilon_1][\upsilon_2]$ or [0][1] and $[\upsilon_1][\upsilon_2]$ or [0][1] or digital logic state combination ‘0’ and ‘0’ at input terminals ‘A’ and ‘B’, respectively, we get dibit output $[\upsilon_2][\upsilon_1]$ or [1][0] or digital logic state ‘1’ at the output terminal ‘Y’. In a similar way, the same output of the light beam is achieved for the combinations of dibit inputs $[\upsilon_1][\upsilon_2]$, $[\upsilon_2][\upsilon_1]$ or [0][1], [1][0] and $[\upsilon_2][\upsilon_1]$, $[\upsilon_1][\upsilon_2]$ or [1][0], [0][1], which is shown clearly in the truth table (Table 1).

TABLE 1. Truth Table of Dibit-Based Optical NAND Logic Gate

Dibit Input for Channel A		Digital Input for Channel A	Dibit Input for Channel B		Digital Input for Channel B	Dibit Output for Channel Y		Digital Output for Channel Y
A′	A″	A	B′	B″	B	Y′	Y″	Y
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0

TABLE 2. Truth Table of Dibit-Based Optical NOR Gate

Dibit Input for Channel A		Digital Input for Channel A	Dibit Input for Channel B		Digital Input for Channel B	Dibit Output for Channel Y		Digital Output for Channel Y
A′	A″	A	B′	B″	B	Y′	Y″	Y
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1
$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[1]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0	$\upsilon_1[0]$	$\upsilon_2[1]$	0
$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_2[1]$	$\upsilon_1[0]$	1	$\upsilon_1[0]$	$\upsilon_2[1]$	0

But if we apply dibit inputs $[\upsilon_2][\upsilon_1]$ and $[\upsilon_2][\upsilon_1]$, then after dibit checking by the ADM_1 with $RSOA_1$ and ADM_4 with $RSOA_3$ blocks, we get the υ_2 frequency of light beam at both point 'C' and 'D'. Now, from point 'C', ADM_2 reflects the υ_2 frequency to $RSOA_5$ as a probe beam. Here, ADM_3 and $RSOA_2$ do not work. Next, from point 'D', the υ_2 frequency of light beam is reflected by ADM_5 and acts as a pump beam of $RSOA_4$ and there is a fixed probe beam of the υ_1 frequency of light. So, this beam comes at the input of $RSOA_5$ as a pump beam. Now, the υ_2 frequency of light beam comes from $RSOA_5$ to ADM_6 and this υ_2 frequency of light beam is passed by ADM_6. So, we get the υ_2 frequency of light beam at 'X' from the output of ADM_6. This υ_2 frequency of light beam is dropped by ADM_7 and goes to $RSOA_7$ as a pump beam. But there is a fixed probe beam of the υ_1 frequency of light at $RSOA_6$. So, the υ_1 frequency of light beam comes at terminal 'Y′'. On the other side, the υ_2 frequency of light beam coming from point 'X' goes directly to terminal 'Y″'. Finally, we get dibit output $[\upsilon_1][\upsilon_2]$ or digital logic state '0' for given dibit inputs $[\upsilon_2][\upsilon_1]$, $[\upsilon_2][\upsilon_1]$ or [1][0], [1][0] or digital logic state '1', '1', which are shown in the truth table (Table 2).

A. Simulation Process of a Frequency-Encoded Dibit-Based NAND Logic Gate with Dibit Checking

The Simulink tools of MATLAB (R2008a) software have been used for simulation of a frequency-encoded all-optical dibit NAND logic gate with dibit checking using a reflective semiconductor optical amplifier (RSOA) and an add/drop multiplexer (ADM). Here, "DIBIT_INPUT 1" and "DIBIT_INPUT 2" dibit input units are used for applying dibit inputs and we get output from the "Dibit Output" unit, which consists of two consecutive bit positions "1st Bit" and "2nd Bit," respectively. Now, shown in Fig. 2, the RSOA blocks are properly programmed with the 'C' language for choosing the proper output at the output terminal. There are two inputs, namely, "pr" (probe beam) and "pm" (pump beam) and the output named by "y" in the RSOA blocks. The RSOA blocks are designed in such a way that the probe beam comes out at the output of the RSOA when both the inputs in the form of a pump beam and a probe beam are available. If a pump beam and a probe beam are considered as say "3 PHz" $= \upsilon_1 =$ digital logic state "0" and "8 PHz" $= \upsilon_2 =$ digital logic state "1", respectively, at the input terminals of the RSOA, then we get "8 PHz" $= \upsilon_2 =$ digital logic state "1" at the output terminal of these blocks. The value of the output changes if the values of the pump beam and probe beam are altered accordingly.

Similarly, an add/drop multiplexer (ADM) has been simulated in such a way that, if a sequence of frequencies are given at the input of the ADM, it passes all other frequencies and drops a particular frequency depending upon the biasing current. If the biasing current is changed, then the frequency of

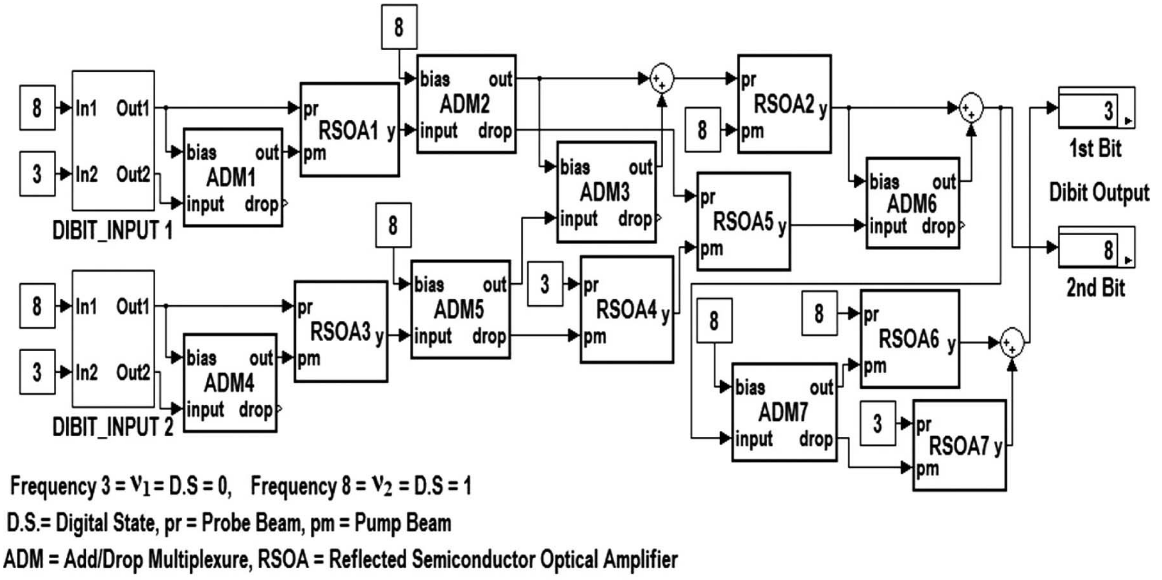


FIG. 2. Functional model of the dibit-based NAND gate with dibit checking.

the dropped terminal changed accordingly. Here, for a particular biasing current, this block drops one frequency and passes the other frequency if at the input terminal of the ADM there are available frequencies, say, “8 PHz” $= \upsilon_2 =$ digital logic state “1” and “3 PHz” $= \upsilon_1 =$ digital logic state “0”. If the value of the biasing current is changed, the opposite incident happens. Now these two types of blocks have been connected maintaining the similarity of the all-optical dibit-based NAND logic gate’s block diagram, which is shown in Fig. 1.

Now, if digital logic state “0”, “0” or $[\upsilon_1][\upsilon_2]$, $[\upsilon_1]$ $[\upsilon_2]$ here, [3][8], [3][8] are applied at the dibit input terminals of the simulated model, we get digital logic state “1” or $[\upsilon_2][\upsilon_1]$ here, and [8][3] at the output terminal of this simulated block. Similarly, for the combinations of digital logic state “0”, “1” and “1”, “0” or $[\upsilon_1][\upsilon_2]$, $[\upsilon_2][\upsilon_1]$, and $[\upsilon_2][\upsilon_1]$, $[\upsilon_1][\upsilon_2]$ the output repeats the same value, i.e., [8][3]. But at the output we get digital logic state “0” or $[\upsilon_1][\upsilon_2]$ here, [3][8] for the combination of dibit inputs, digital logic state “1”, “1”, or dibit states $[\upsilon_2][\upsilon_1]$, $[\upsilon_2][\upsilon_1]$.

Finally, this simulative functional model fully satisfies the truth table of the all-optical dibit-based NAND logic gate, which is shown in Table 1.

3. SCHEME OF REALIZATION OF A FREQUENCY-ENCODED DIBIT-BASED NOR LOGIC GATE WITH DIBIT CHECKING

Similarly, in Fig. 3, to realize the dibit-based two-input NOR gate, at first, the υ_1 and υ_2 frequency of light beams are given to the input channels of ‘A′’, ‘A″’ and ‘B′’, ‘B″’ simultaneously. Then it goes to the dibit-checking portion, where ADM_1 passes the υ_2 frequency of light beam. So, the υ_1 frequency and υ_2 frequency of light beams act as a probe beam and a pump beam, respectively, at $RSOA_1$ and that is why the υ_1 frequency of light beam comes from $RSOA_1$ at point ‘C’. Similarly, ADM_3 passes the υ_2 frequency of light beam for the given υ_1 frequency and υ_2 frequency of light beams at the ‘B’ terminal. Next, the υ_1 frequency and υ_2 frequency of light beams act as a probe beam and a pump beam, respectively, at $RSOA_3$ and the υ_1 frequency of light beam comes as the output from $RSOA_3$ at point ‘D’. Then, from point ‘C’, the υ_1 frequency of light is passed by ADM_2 and one part of this light beam goes to $RSOA_2$ as a pump beam and another part goes to $RSOA_4$ as a pump beam where there is a fixed probe beam given in the form of the υ_2 frequency. As a result, the υ_2 frequency of light comes out from $RSOA_4$ and goes to $RSOA_5$ as a pump beam. Now, from point ‘D’, the υ_1 frequency of light is passed by ADM_4 and it goes to $RSOA_5$ as a probe beam. So, the υ_1 frequency of light comes out from $RSOA_5$ and it goes to point ‘X’. On the other side, $RSOA_2$ does not work because there is no probe beam. Now, the υ_1 frequency of light coming from point ‘X’ is passed by ADM_5 and goes to $RSOA_6$ as a pump beam. As there is a fixed probe beam of the υ_2 frequency of light at $RSOA_6$, so the υ_2 frequency of light comes at output terminal ‘Y′’. On the other hand, the υ_1 frequency of light coming from point ‘X’ goes directly to the ‘Y″’ terminal. So, with the dibit inputs of $[\upsilon_1][\upsilon_2]$, $[\upsilon_1][\upsilon_2]$ or [0][1], [0][1] we get dibit output $[\upsilon_2][\upsilon_1]$ or [1][0] or digital logic state ‘1’ at the output terminal, shown in Fig. 3.

But if we apply dibit inputs $[\upsilon_1][\upsilon_2]$ and $[\upsilon_2][\upsilon_1]$, we get the υ_1 frequency of light at point ‘C’ and the υ_2 frequency of light at point ‘D’. Now, from point ‘C’, ADM_2 passes one part of the υ_1 frequency of light to $ROSA_2$ as a pump beam and the other part goes to $ROSA_4$ as a pump beam. As there is a fixed

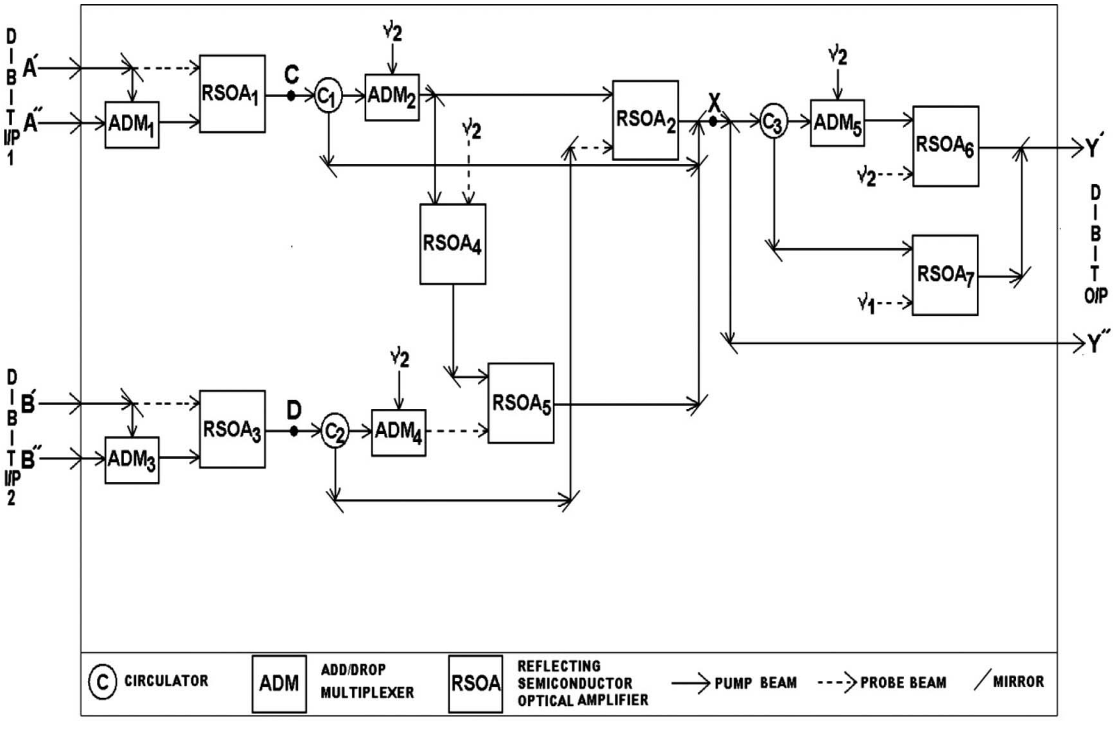


FIG. 3. Frequency-encoded optical dibit-based NOR gate with dibit checking.

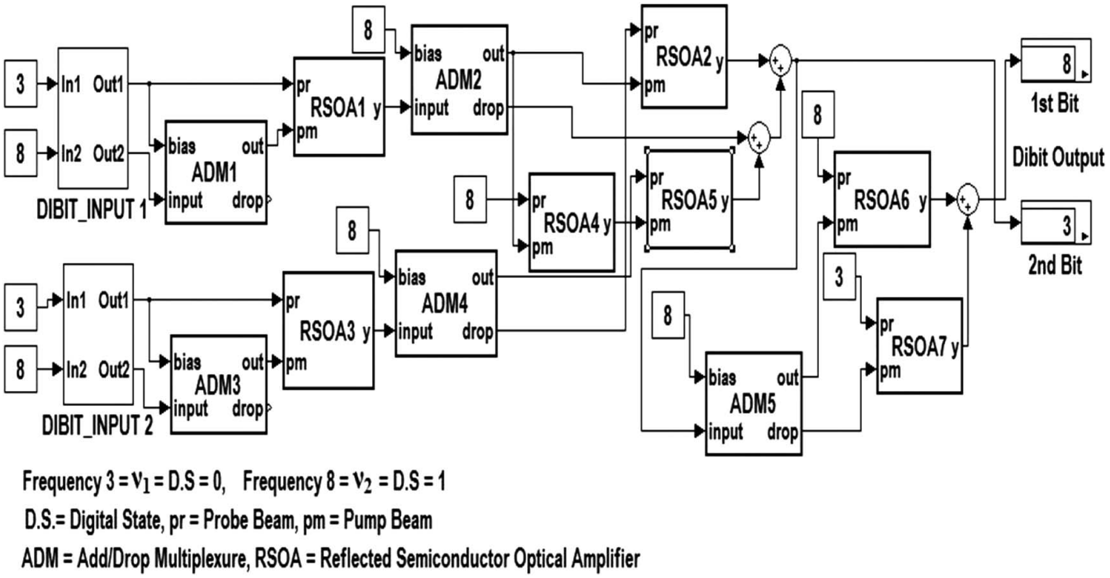


FIG. 4. Functional model of the dibit based NOR gate with dibit checking.

probe beam of the υ_2 frequency at RSOA$_4$, this υ_2 frequency of light beam goes to RSOA$_5$ as a pump beam. But, from point 'D', the υ_2 frequency of light beam is reflected by ADM$_4$ and acts as a probe beam of RSOA$_2$. This υ_2 frequency of light beam comes out from RSOA$_2$ at point 'X'. Now, this υ_2 frequency of light is reflected by ADM$_5$ and goes to RSOA$_7$ as a pump beam. But there is a fixed probe beam of the υ_1 frequency at RSOA$_6$, so the υ_1 frequency of light comes at the output terminal 'Y′'. On the other side, the υ_2 frequency of light coming from point 'X' goes to the output terminal 'Y″' directly. So, at the output finally we get dibit output $[\upsilon_1][\upsilon_2]$ or [0][1] or digital logic state '0' for the combination of dibit input $[\upsilon_1][\upsilon_2]$ or [0][1] and dibit input $[\upsilon_1][\upsilon_2]$ or [0][1] or for the digital logic state combination '0' and '1'. Similarly, this realization repeats the same output for the combinations of dibit inputs $[\upsilon_2][\upsilon_1]$, $[\upsilon_1][\upsilon_2]$ or [1][0], [0][1] and $[\upsilon_2][\upsilon_1]$, $[\upsilon_2][\upsilon_1]$ or [1][0], [1][0] or, for the digital logic state combinations '1', '0' and '1', '1', shown in the truth table (Table 2).

A. Simulation Process of a Frequency-Encoded Dibit-Based NOR Logic Gate with Dibit Checking

Similarly, in Fig. 4, the Simulink tools of MATLAB (R2008a) software were used for the simulation process of a frequency-encoded optical dibit NOR gate. Here also, "DIBIT_INPUT 1," "DIBIT_INPUT 2," and "Dibit Output" units are used for applying dibit inputs and taking dibit output. Now, RSOA and ADM blocks have been connected maintaining the similarity of the block diagram of an all-optical dibit-based NOR logic gate, which is shown in Fig. 3. Here, digital logic state "0" is considered as [3] and digital logic state "1" is considered as [8]. Now, if we apply to the input terminal, the dibit logic state $[\upsilon_1][\upsilon_2]$, $[\upsilon_1][\upsilon_2]$ here, [3][8], [3][8] we get dibit logic state $[\upsilon_2][\upsilon_1]$, here, [8][3] at the output terminal of this simulated block. But, for the remaining possible combinations of dibit logic states such as $[\upsilon_1][\upsilon_2]$, $[\upsilon_2][\upsilon_1]$ and $[\upsilon_2][\upsilon_1]$, $[\upsilon_1][\upsilon_2]$ and $[\upsilon_2][\upsilon_1]$, $[\upsilon_2][\upsilon_1]$, we get dibit logic state $[\upsilon_1][\upsilon_2]$, here, [3][8]. So, it can be said that, this simulated block fully satisfies the truth table of a frequency-encoded all-optical dibit-based NOR logic gate, which is shown in Table 2.

4. CONCLUSION

The advantages of a frequency encoding and dibit representation technique are exploited here to realize all-optical operations. This gives not only a trustworthy and faithful operation, but it also supports the reduction of the bit error problem by increasing the high signal-to-noise ratio. Here also the dibit checking part reduces errors in dibit inputs. One also can expect a high degree of parallelism with ultrafast operational speed. Again tri-state and quaternary state for other logic operations can be developed while occupying the least space in all-optical devices. This encoding technique helps with the implementation of the all-optical logical operations with faithful and reliable results. So, it is not only ultra-high-speed operation but also exhibits real-time operation with high reliability.

---

1. S. Mukhopadhyay, "Role of optics in super-fast information processing," Indian J. Phys. **84**(8), 1069–1074 (2010).
2. A. K. Ghosh, A. Bhattacharya, M. Raul, and A. Basuray, "Trinary arithmetic and logic unit (TALU) using Savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic," Opt. Laser Technol. **44**(5), 1583–1592 (2010).
3. P. P. Sarkar, B. Satpati, and S. Mukhopadhyay, "Verification of all optical frequency encoded OR logic operation with its simulated result," Int. J. Electron. Commun. Technol. **4**, Supplement 1, 86–88 (2013).
4. S. Dutta and S. Mukhopadhyay, "Alternating approach of implementing frequency encoded all-optical logic gates and flip-flop using semiconductor optical amplifier," Optik Int. J. Light Electron Opt. **122**(12), 1088–1094 (2011).
5. S. S. Pratim, B. Satpati, and S. Mukhopadhyay, "New simulative studies on performance of semiconductor optical amplifier based optical switches like frequency converter and add-drop multiplexer for optical data processors," J. Opt. **42**(4), 360–366 (2013).
6. L. Q. Guo and M. J. Connelly, "A Poincaré approach to investigate nonlinear polarization rotation in semiconductor optical amplifiers and its applications to all-optical wavelength conversion," Proc. SPIE. **6783**, 678325 (2007).

7. H. Q. Jin, J. R. He, Z. B. Cai, J. C. Liang, and L. Yi, "Analytical traveling wave and soliton solutions of the generalized nonautonomous nonlinear Schrödinger equation with an external potential," Indian J. Phys. **87**(12), 1243–1250 (2013).
8. B. Ghosh, R. R. Pal, and S. Mukhopadhyay, "An all-optical integrated system for implementing arithmetic operation in 2's complement method with the active participation of non-linear material based switches," Indian J. Phys. **84**(8), 1101–1109 (2010).
9. S. K. Garai and S. Mukhopadhyay, "A method of optical implementation of frequency encoded different logic operations using second harmonic and difference frequency generation techniques in non-linear material," Optik Int. J. Light Electron Opt. **121**(8), 715–721 (2010).
10. S. Mukhopadhyay, "Binary optical data subtraction by using a ternary dibit representation technique in optical arithmetic problems," Appl. Opt. **31**(23), 4622–4627 (1992).
11. B. Ghosh and S. Mukhopadhyay, "A novel realization of all-optical dibit represented frequency encoded Boolean and quaternary inverters without switching device," Optik Int. J. Light Electron Opt. **124**(21), 4813–4815 (2013).
12. P. P. Sarkar, B. Satpati, and S. Mukhopadhyay, "Analytical and simulative studies on optical NOR and controlled NOR logic gates with semiconductor optical amplifier," Optik Int. J. Light Electron Opt. **125**(3), 1333–1336 (2014).
13. H. Kim, B. H. Kwon, M. Suh, D. S. Kang, Y. Kim, and D. Y. Jeon, "Degradation characteristics of red light-emitting CuInS$_2$/ZnS quantum dots as a wavelength converter for LEDs," Electrochem. Solid-State Lett. **1410**, 55–57 (2011).
14. S. P. Singh, S. Kar, and V. K. Jain, "Performance of all-optical WDM network in presence of fourwave mixing, optical amplifier noise and wavelength converter noise," Fiber Integr. Opt. **26**(2), 79–97 (2007).
15. A. E. N. A. Mohammed, M. M. El-Halawany, A. N. Zaki Rashed, and M. M. Eid, "Optical add drop multiplexers with UW-DWDM technique in metro optical access communication networks," Nonlinear Opt. Quantum Opt. **42**(2), 145 (2012).
16. A. N. Z. Rashed, "Optical add drop multiplexer (OADM) based on dense wavelength division multiplexing technology in next generation optical networks," Int. J. Multimedia Ubiquitous Eng. **7**(1), (2012).

Bitan Ghosh
12.09.21