ABSTRACT

The information storage and transmission are the two most important responsibilities of any modern communication or computing device. The consistent operations of computing or communication device requires reliable operation of both storage and communication systems. The radiation-induced soft errors have been considered as the foremost issues against the reliable operations of storage system. The soft errors are the main cause of cell upsets in storage systems, whereas the performance of communication system is degraded due to channel noise, fading and interference. The Error Correction Codes (ECCs) are the universally accepted solution for enhancing reliability of both the storage and communication systems. The ECCs are preferred mostly for the applications in storage and communication systems which have lower implementation costs in terms of area, delay, power consumption, redundancy, mis-correction rates and Bit Error Rate (BER).

In this thesis, several improved schemes for adjacent and burst error correction codes and their competent Very Large Scale Integration (VLSI) implementations have been introduced for storage and communication systems. In addition, the performance of the soft decision decoding based Triple Adjacent Error Correction (TAEC) code and the combined ECC scheme consists of the 3-bit Burst Error Correction (BEC) and Single Error Correction-Double Adjacent Error Correction (SEC-DAEC) codes have been thoroughly examined for the Free Space Optical (FSO) communication system. This thesis presents the design and efficient VLSI implementation of various SEC-DAEC codes with the goal of lowering the overheads associated with the circuit design of encoders and decoders for memory application. Further, as an effort to reduce design overheads and the rate of mis-correction, a number of SEC-DED-DAEC codes have been developed and implemented in VLSI. Also, SEC-DAEC-TAEC and t-bit BEC codes have been designed and implemented to reduce the overheads associated with codec design. These codes can be used for protecting MCUs in memory applications. Moreover, the performance of a soft decision decoder based TAEC code and the combined ECC scheme with outer 3-bit BEC and inner SEC-DAEC codes for FSO communication channel have been presented in this thesis.