

**BACHELOR OF ENGINEERING (ELECTRICAL ENGINEERING) THIRD YEAR
FIRST SEMESTER SUPPLEMENTARY EXAM 2024**

SUBJECT: - ELECTRICAL INSTRUMENTATION

Time: Three hours

**Full Marks 100
(50 marks for each part)**

Use a separate Answer-Script for each part

No. of Questions	PART-I	Marks	
Answer any two		25 × 2 = 50	
1. a)	Prove that Butterworth poles are situated on an s -plane unit circle.	(7+18=25)	
b)	Design a low pass maximally flat filter with the following specifications: a) 3 dB cut-off frequency (ω_c) = 1500 rad/s. b) maximum attenuation in the pass band is 0.5 dB for $\omega \leq 0.5\omega_c$ rad/s. c) minimum attenuation in the stop band is 20 dB for $\omega \geq 4\omega_c$ rad/s d) pass band gain = 2		
2. a)	What are <i>Rounding off</i> and <i>Truncation</i> type Analog to Digital converters (ADCs)?		6
b)	Explain the operation of successive approximation type ADC for 3 bits.		8
c)	Obtain a 4-bit binary representation of an analog signal value of 12.5 V using successive approximation type ADC. Reference voltage is 14 V. Find out the conversion time in seconds and quantization error in volts. The clock frequency is 2kHz.	6	
d)	What are gain and offset errors of ADC?	5	
3. a)	The input resistance and capacitance of a Cathode Ray Oscilloscope (CRO) are 1.0 μ F and 2.0 M Ω . What is the matched capacitance of the probe for proper compensation assuming 10k Ω probe resistance? Explain necessary formula.	6	
b)	What are the functions of time base generator and Trigger in a Cathode Ray Oscilloscope (CRO)?	5+5	
c)	What are <i>lock range</i> and <i>capture range</i> of a Phase Locked Loop (PLL)? How can you use a PLL as frequency demodulator?	4+5	
4.	Write notes on any <i>two</i>	(12½X2=25)	
a)	Operation of a 3-bit unipolar R-2R ladder network based DAC		
b)	Linear model of phase locked loop (PLL)		
c)	Storage Oscilloscope		

BACHELOR OF ENGINEERING (ELECTRICAL ENGINEERING) THIRD YEAR FIRST
SEMESTER SUPPLEMENTARY EXAMINATION

SUBJECT: - ELECTRICAL INSTRUMENTATION

Time: Three hours

Full Marks 100
(50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
	<p><i>Answer any THREE questions.</i></p> <p><i>Two marks reserved for neat and well organized answer.</i></p>	
1.	(a) Draw the circuit diagram used for asynchronous demodulation of LVDT. Explain with necessary expressions and waveform the operation of the entire scheme.	8
	(b) A resistive voltmeter is connected to the secondary coils of LVDT following standard method of connection. How do you introduce phase compensation of the arrangement?	8
2.	(a) Draw neatly a schematic diagram showing essential details of constructions for LVDT. Mention the purpose of using each of these elements in its construction.	8
	(b) "In synchronous demodulation, proper adjustment of the cut off frequency is required in the low pass filter used so that the output voltage can successfully track the position and direction of core in linear variable differential transformer." – State the correctness of the statement and justify in favour of your comment.	8
3.	(a) Describe with necessary circuit diagram, derivation and expressions the operating principle of capacitive transducer that works on the change in overlapping area.	8
	(b) How do you measure the liquid level using a capacitive transducer? Explain the method.	8
4.	(a) Derive the expression of capacitance for a variable air-gap transducer with composite dielectric. Obtain an expression of its sensitivity.	8
	(b) What is a guard electrode? What is the purpose of using it? Draw a circuit involving guard electrode that can fulfill the purpose of its use.	8

	<p>5. Write short notes on any TWO:</p> <ul style="list-style-type: none">(a) Angular displacement sensor(b) Phase compensation of LVDT(c) Advantages of capacitive sensor	<p>8 + 8</p>
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